

Power Management Integrated Circuit (PMIC) for i.MX50/53 Families

The 34709 is the Power Management Integrated Circuit (PMIC) designed primarily for use with the Freescale i.MX50 and i.MX53 families. It offers a low cost solution targeting embedded applications that do not require a battery charger. However, it can be easily combined with an external charger, allowing flexibility for either single or multi-cell Li-Ion battery configurations. It supports both consumer and industrial applications with a single 130-pin 8x8 MAPBGA 0.5 mm pitch package that is easily routable in low cost board designs.

Features

- Six multi-mode buck regulators for direct supply of the processor core, memory, and peripherals.
- Boost regulator for USB PHY domain on i.MX processors.
- Eight LDO regulators with internal and external pass devices for thermal budget optimization and DDR memory voltage reference
- 10-bit ADC for monitoring battery and other inputs
- Real time clock and crystal oscillator circuitry with a coin cell backup/charger
- SPI/I²C bus for control and register interface
- Four general purpose low-voltage I/Os with interrupt capability
- Two PWM outputs

34709

POWER MANAGEMENT



VK SUFFIX (PB-FREE)
98ASA00333D
130 MAPBGA
8.0 X 8.0 (0.5 MM PITCH)

Applications

| |
|--------------------------------|
| Tablets |
| Smart Mobile Devices |
| Patient Monitors |
| Digital Signage |
| Human Machine Interfaces (HMI) |

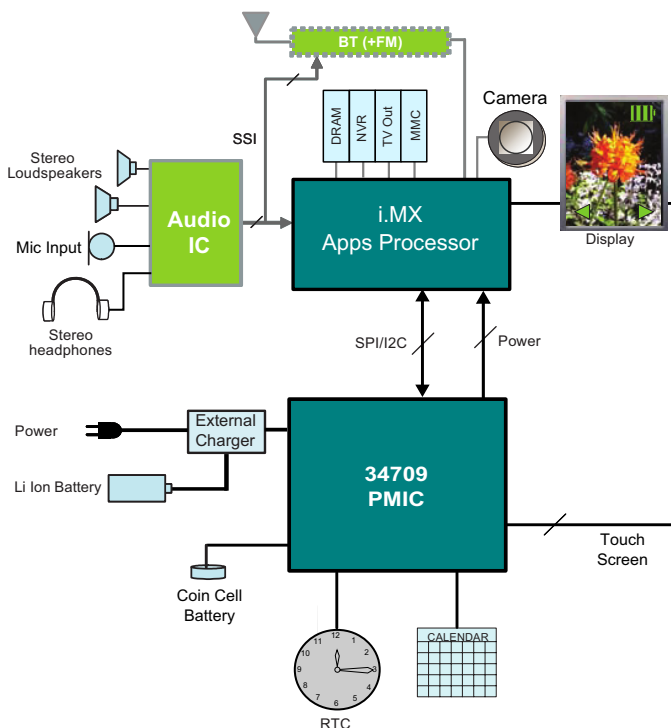


Figure 1. Simplified Application Diagram

* This document contains certain information on a new product. Specifications and information herein are subject to change without notice.

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1 Orderable Parts

This section describes the part numbers available to be purchased, along with their differences. Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to <http://www.freescale.com> and perform a part number search for the following device numbers.

Table 1. Orderable Part Variations

| Part Number ⁽¹⁾ | Temperature (T _A) | Package |
|----------------------------|-------------------------------|--|
| MC34709VK | -40 to 85 °C | 130 MAPBGA - 8.0 x 8.0 mm - 0.5 mm Pitch |

Notes

1. To Order parts in Tape & Reel, add the R2 suffix to the part number.

2 Part Identification

This section provides an explanation of the part numbers and their alpha numeric breakdown.

2.1 Description

Part numbers for the chips have fields that identify the specific part configuration. You can use the values of these fields to determine the specific part you have received.

2.2 Format and Examples

Part numbers for a given device have the following format, followed by a device example:

[Table 2 - Part Numbering - Analog:](#)

MC tt xxx r v PP RR - MC34709VKR2

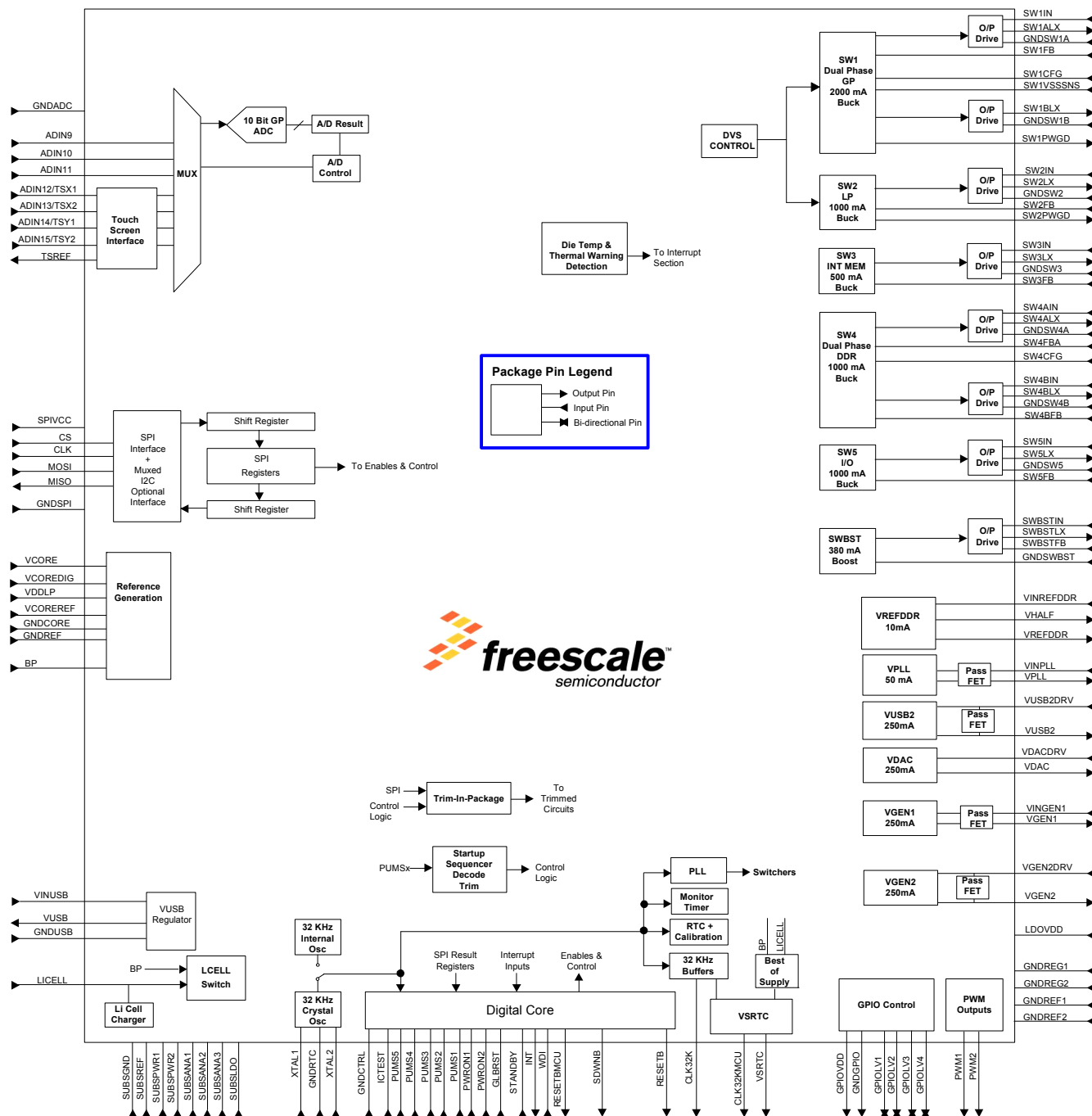
2.3 Fields

These tables list the possible values for each field in the part number (not all combinations are valid).

Table 2: Part Numbering - Analog

| FIELD | DESCRIPTION | VALUES |
|-------|-------------------------|--|
| MC | Product Category | <ul style="list-style-type: none"> MC- Qualified Standard PC- Prototype Device |
| tt | Temperature Range | <ul style="list-style-type: none"> 33 = -40 °C to > 105 °C 34 = -40 °C to ≤ 105 °C 35 = -55 °C to ≥ 125 °C |
| xxx | Product Number | <ul style="list-style-type: none"> Assigned by Marketing |
| r | Revision | <ul style="list-style-type: none"> (default blank) |
| v | Variation | <ul style="list-style-type: none"> (default blank) |
| PP | Package Identifier | <ul style="list-style-type: none"> Varies by package |
| RR | Tape and Reel Indicator | <ul style="list-style-type: none"> R2 = 13 inch reel hub size |

3 Internal Block Diagram



4 Pin Connections

4.1 Ballmap

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
|---|----------|--------|-----------|--------|-----------|---------|---------|----------|----------|----------|----------|----------|----------|-----------|---------|
| A | | MISO | GNDSP1 | SP1VCC | GLBRST | PWRON1 | PWM2 | PWM1 | ICTEST | SW2LX | | SW2FB | SW2PWGD | NC_2 | |
| B | CLK | CS | MOSI | INT | RESETB | GNDCTRL | GPIOLV1 | | GPIOLV2 | GNDSW2 | SW2IN | GNDREF2 | SW3FB | | NC_3 |
| C | GNDUSB | | | | | | GPIOLV0 | GPIOVDD | GNDGPIO | | | | | | |
| D | VINUSB | VUSB | | | RESETBMCU | SDWNB | | | | | | | | GNDSW3 | SW3LX |
| E | XTAL1 | | CLK32K | | PWRON2 | PUMS5 | | SUBSPWR1 | | GPIOLV3 | SUBSPWR2 | | | SW3IN | |
| F | GNDRTC | | CLK32KVCC | | PUMS4 | PUMS3 | | SUBSPWR1 | SUBSPWR1 | SUBSANA2 | | | | GNDSWBST | SWBSTIN |
| G | XTAL2 | | CLK32KMCU | | PUMS2 | PUMS1 | | SUBSPWR1 | SUBSPWR1 | SUBSPWR3 | | | | SWBSTLX | |
| H | GNDCORE | VSRTC | | | GNDADC | ADIN9 | | SUBSPWR1 | SUBSPWR1 | SUBSLDO | | VGEN1 | | VINGEN1 | SWBSTFB |
| J | VCORED1G | VCORE | | | ADIN10 | ADIN11 | | SUBSGND | SUBSPWR1 | | | GNDREG2 | | VINREFDDR | VHALF |
| K | VCOREREf | | WDI | | TSX1 | TSREF | | SUBSREF | SUBSPWR | SW1PWGD | | SUBSANA1 | | VPLL | VREFDDR |
| L | VDDLp | | TSY2 | TSX2 | | TSY1 | | | | | | SW1CFG | | VGEN2DRV | VINPLL |
| M | GNDREF | LICELL | | | | SW4CFG | | SW5FB | | | | | | GNDREG1 | VGEN2 |
| N | BP | SW4AFB | | | | | | | GNDREF1 | | | | | VDACDRV | LDOVDD |
| P | STANDBY | SW4BFB | GNDSW4A | SW4AIN | SW4BIN | GNDSW4B | SW5IN | GNDSW5 | GNDSW1A | SW1IN | SW1IN | GNDSW1B | SW1FB | VUSB2DRV | VDAC |
| R | NC_1 | | SW4ALX | | | SW4BLX | | SW5LX | SW1ALX | | SW1BLX | | SW1VSSNS | VUSB2 | |

Figure 3. Top View Ballmap

4.2 Pin Definitions

Table 3. Pin Definitions

| Pin Number | Pin Name | Pin Function | Definition |
|-----------------------------|----------|--------------|---|
| Supply | | | |
| N1 | BP | I | 1. Application supply point 2. Input supply to the IC core circuitry |
| D6 | SDWNB | O | Indication of imminent system shutdown |
| IC Core | | | |
| J2 | VCORE | O | Regulated supply for the IC analog core circuitry |
| J1 | VCOREDIG | O | Regulated supply for the IC digital core circuitry |
| K1 | VCOREREF | O | Main bandgap reference |
| L1 | VDDL | O | VDDL reference |
| H1 | GNDCORE | GND | Ground for the IC core circuitry |
| M1 | GNDREF | GND | Ground reference for IC core circuitry |
| Switching Regulators | | | |
| P10 P11 | SW1IN | I | Regulator 1 input ⁽²⁾ |
| R9 | SW1ALX | O | Regulator 1A switch node connection ⁽²⁾ |
| P13 | SW1FB | I | Regulator 1 feedback ⁽²⁾ |
| P9 | GNDSW1A | GND | Ground for Regulator 1A |
| R13 | SW1VSSNS | GND | Regulator 1 sense |
| K10 | SW1PWGD | O | Power good signal for SW1 ⁽²⁾ |
| R11 | SW1BLX | O | Regulator 1B switch node connection ⁽²⁾ |
| P12 | GNDSW1B | GND | Ground for Regulator 1B |
| L12 | SW1CFG | I | Regulator 1A/B mode configuration ⁽²⁾ |
| B11 | SW2IN | I | Regulator 2 input ⁽²⁾ |
| A10 | SW2LX | O | Regulator 2 switch node connection ⁽²⁾ |
| A12 | SW2FB | I | Regulator 2 feedback ⁽²⁾ |
| B10 | GNDSW2 | GND | Ground for Regulator 2 |
| A13 | SW2PWGD | O | Power good signal for SW2 ⁽²⁾ |
| E14 | SW3IN | I | Regulator 3 input ⁽²⁾ |
| D15 | SW3LX | O | Regulator 3 switch node connection ⁽²⁾ |
| B13 | SW3FB | I | Regulator 3 feedback ⁽²⁾ |
| D14 | GNDSW3 | GND | Ground for Regulator 3 |
| B12 | GNDREF2 | GND | Ground reference for Regulators |
| P4 | SW4AIN | I | Regulator 4A input ⁽²⁾ |
| R3 | SW4ALX | O | Regulator 4A switch node connection ⁽²⁾ |
| N2 | SW4AFB | I | Regulator 4A feedback ⁽²⁾ |
| P3 | GNDSW4A | GND | Ground for Regulator 4A |

Table 3. Pin Definitions (continued)

| Pin Number | Pin Name | Pin Function | Definition |
|------------|----------|--------------|--|
| P5 | SW4BIN | I | Regulator 4B input ⁽²⁾ |
| R6 | SW4BLX | O | Regulator 4B switch node connection ⁽²⁾ |
| P2 | SW4BFB | I | Regulator 4B feedback ⁽²⁾ |
| P6 | GNDSW4B | GND | Ground for Regulator 4B |
| M6 | SW4CFG | I | Regulator 4A/B mode configuration ⁽²⁾ |
| P7 | SW5IN | I | Regulator 5 input ⁽²⁾ |
| R8 | SW5LX | O | Regulator 5 output ⁽²⁾ |
| M8 | SW5FB | I | Regulator 5 feedback ⁽²⁾ |
| P8 | GNDSW5 | GND | Ground for Regulator 5 |
| N9 | GNDREF1 | GND | Ground reference for regulators |
| F15 | SWBSTIN | I | Boost Regulator BP supply ⁽²⁾ |
| G14 | SWBSTLX | O | SWBST switch node connection ⁽²⁾ |
| H15 | SWBSTFB | I | Boost Regulator feedback ⁽²⁾ |
| F14 | GNDSWBST | GND | Ground for regulator boost |

LDO Regulators

| | | | |
|-----|-----------|-----|--|
| J14 | VINREFDDR | I | VREFDDR input supply |
| K15 | VREFDDR | O | VREFDDR regulator output |
| J15 | VHALF | O | Half supply reference for VREFDDR |
| L15 | VINPLL | I | VPLL input supply |
| K14 | VPLL | O | VPLL regulator output |
| N14 | VDACDRV | O | Drive output for VDAC regulator using an external PNP device |
| P15 | VDAC | O | VDAC regulator output |
| N15 | LDOVDD | I | Supply pin for VUSB2, VDAC, and VGEN2 Must be always connected to the same supply as the PNP emitter. Recommended to use BP as the LDOVDD supply. See Figure 24 for a typical connection diagram. |
| D2 | VUSB | O | USB transceiver regulator output |
| D1 | VINUSB | I | VUSB input supply |
| C1 | GNDUSB | GND | Ground for VUSB LDO |
| P14 | VUSB2DRV | I | VUSB2 input using internal PMOS FET |
| | | O | Drive output for VUSB2 regulator using an external PNP device |
| R14 | VUSB2 | O | VUSB2 regulator output |
| H14 | VINGEN1 | I | VGEN1 input supply |
| H12 | VGEN1 | O | VGEN1 regulator output |
| L14 | VGEN2DRV | I | VGEN2 input using internal PMOS FET |
| | | O | Drive output for VGEN2 regulator using an external PNP device |
| M15 | VGEN2 | O | VGEN2 regulator output |
| H2 | VSRTC | O | Output regulator for SRTC module on processor |
| M14 | GNDREG1 | GND | Ground for Regulator 1 |
| J12 | GNDREG2 | GND | Ground for Regulator 2 |

Table 3. Pin Definitions (continued)

| Pin Number | Pin Name | Pin Function | Definition |
|------------|----------|--------------|--------------------------------|
| C8 | GPIOVDD | I | Supply for GPIOLV pins |
| C7 | GPIOLV0 | I/O | General purpose input/output 1 |
| B7 | GPIOLV1 | I/O | General purpose input/output 2 |
| B9 | GPIOLV2 | I/O | General purpose input/output 3 |
| E10 | GPIOLV3 | I/O | General purpose input/output 4 |
| A8 | PWM1 | O | PWM output 1 |
| A7 | PWM2 | O | PWM output 2 |
| C9 | GNDGPIO | GND | GPIO ground |

Clock/RTC/Coin Cell

| | | | |
|----|-----------|-----|--|
| M2 | LICELL | I | 1. Coin cell supply input |
| | | O | 2. Coin cell charger output |
| E1 | XTAL1 | I | 32.768 kHz Oscillator crystal connection 1 |
| G1 | XTAL2 | I | 32.768 kHz Oscillator crystal connection 2 |
| F1 | GNDRTC | GND | Ground for the RTC block |
| F3 | CLK32KVCC | I | Supply voltage for 32 k buffer |
| E3 | CLK32K | O | 32 kHz Clock output for peripherals |
| G3 | CLK32KMCU | O | 32 kHz Clock output for processor |

Control Logic

| | | | |
|----|-----------|-----|-------------------------------------|
| B5 | RESETB | O | Reset output for peripherals |
| D5 | RESETBMCU | O | Reset output for processor |
| K3 | WDI | I | Watchdog input |
| P1 | STANDBY | I | Standby input signal from processor |
| B4 | INT | O | Interrupt to processor |
| A6 | PWRON1 | I | Power on/off button connection 1 |
| E5 | PWRON2 | I | Power on/off button connection 2 |
| A5 | GLBRST | I | Global Reset |
| G6 | PUMS1 | I | Power up mode supply setting 1 |
| G5 | PUMS2 | I | Power up mode supply setting 2 |
| F6 | PUMS3 | I | Power up mode supply setting 3 |
| F5 | PUMS4 | I | Power up mode supply setting 4 |
| E6 | PUMS5 | I | Power up mode supply setting 5 |
| A9 | ICTEST | I | Connect to GND for normal operation |
| B6 | GNDCTRL | GND | Ground for control logic |
| A4 | SPIVCC | I | Supply for SPI bus |
| B2 | CS | I | Primary SPI select input |
| B1 | CLK | I | Primary SPI clock input |
| B3 | MOSI | I | Primary SPI write input |
| A2 | MISO | O | Primary SPI read output |

Table 3. Pin Definitions (continued)

| Pin Number | Pin Name | Pin Function | Definition |
|------------|----------|--------------|--------------------------|
| A3 | GNDSPI | GND | Ground for SPI interface |

A to D Converter

| | | | |
|----|--------|-----|---|
| H6 | ADIN9 | I | ADC generic input channel 9 |
| J5 | ADIN10 | I | ADC generic input channel 10 |
| J6 | ADIN11 | I | ADC generic input channel 11 |
| K5 | TSX1 | I | Touch Screen Interface X1 or ADC generic input channel 12 |
| L4 | TSX2 | I | Touch Screen Interface X2 or ADC generic input channel 13 |
| L6 | TSY1 | I | Touch Screen Interface Y1 or ADC generic input channel 14 |
| L3 | TSY2 | I | Touch Screen Interface Y2 or ADC generic input channel 15 |
| K6 | TSREF | O | Touch screen reference |
| H5 | GNDADC | GND | Ground for A to D circuitry |

Substrate Grounds

| | | | |
|--|----------|-----|-----------------------------|
| K8 | SUBSREF | GND | Substrate ground connection |
| K9 | SUBSPWR | GND | Substrate ground connection |
| E8 F8 F9 G8 G9 H8 H9 J9 | SUBSPWR1 | GND | Substrate ground connection |
| E11 | SUBSPWR2 | GND | Substrate ground connection |
| G10 | SUBSPWR3 | GND | Substrate ground connection |
| H10 | SUBSLDO | GND | Substrate ground connection |
| K12 | SUBSANA1 | GND | Substrate ground connection |
| F10 | SUBSANA2 | GND | Substrate ground connection |
| J8 | SUBSGND | GND | Substrate ground connection |

No connects

| | | | |
|------------------|----|---|----------------|
| A14 B15 R1 | NC | - | Do not connect |
|------------------|----|---|----------------|

Notes

- If a switching regulator is not used, connect the regulator pins as follows:
SWxVIN = BP, SWxLX = NC, SWxFB = GND, SWxPWGD = NC, SWxCFG = GND

5 General Product Characteristics

5.1 Maximum Ratings

Table 4. Maximum Ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Symbol | Description (Rating) | Min. | Max. | Unit | Notes |
|---------------------------|---|-----------------------|---------------------------------|------|------------|
| ELECTRICAL RATINGS | | | | | |
| V_{BP} V_{LCELL} | Input Supply Pins <ul style="list-style-type: none"> BP LICELL | - - | 4.8 4.8 | V | |
| | IC Core Reference <ul style="list-style-type: none"> VCOREREFF VCOREDIG, VDDL VCORE | - - - | 1.5 1.6 3.6 | V | |
| | Switching Regulators Pins <ul style="list-style-type: none"> SWxIN, SWxLX, SWBSTFB SWxPB, SWxPWGD, SWxCFG SWBSTLX | - - - | 5.5 3.6 7.5 | V | |
| | LDO Regulator Pins <ul style="list-style-type: none"> VREFDDR, VHALF VPLL, VGEN1, VINGEN1, VSRTC VINREFDDR, VDACC, VUSB2, VGEN2, VUSB VINPLL, VDACC, VUSB2, VGEN2, VUSB LDOVDD, VINUSB | - - - - - | 1.5 2.5 3.6 4.8 5.5 | V | |
| | GPIO Pins <ul style="list-style-type: none"> GPIOVDD, GPIOVx, PWMx | - | 2.5 | V | |
| | Control Logic Pins <ul style="list-style-type: none"> ICTEST XTAL1, XTAL2 CLK32KVCC, CLK32K, CLK32KMCU, WDI, STANDBY, INT, PWRON1, PWRON2, GLBRST, PUMSx, SPIVCC, CS, CLK, MOSI, MISO, SDWNB | - - - | 1.8 2.5 3.6 | V | |
| | ADC Interface Pins <ul style="list-style-type: none"> ADINx, TSX1/ADIN12, TSX2/ADIN13, TSY1/ADIN14, TSY2/ADIN15, TSREF | - | 4.8 | V | (4), (5) |
| V_{ESD} | ESD Ratings <ul style="list-style-type: none"> Human Body Model All pins Charge Device Model All pins | - - | ± 2000 ± 500 | V | (3) (3) |

Notes

- ESD testing is performed in accordance with the Human Body Model (HBM) ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500$ Ω), and the Charge Device Model (CDM), Robotic ($C_{ZAP} = 4.0$ pF).
- ADINx must not exceed BP.
- TSXx and TSYx must not exceed BP or VCORE.

5.2 Thermal Characteristics

The thermal rating data of the packages has been simulated with the results listed in [Table 5](#).

Table 5. Thermal Ratings

| Symbol | Description (Rating) | Min. | Max. | Unit | Notes |
|---|---|------|--------|------|-----------|
| THERMAL RATINGS | | | | | |
| T_A | Ambient Operating Temperature Range | -40 | 85 | °C | |
| T_J | Operating Junction Temperature Range | -40 | 125 | °C | |
| T_{ST} | Storage Temperature Range | -65 | 150 | °C | |
| T_{PPRT} | Peak Package Reflow Temperature During Reflow | - | Note 6 | °C | (6), (7) |
| THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS | | | | | |
| $R_{\theta JA}$ | Junction to Ambient Natural Convection • Single layer board (1s) | - | 93 | °C/W | (8), (9) |
| $R_{\theta JMA}$ | Junction to Ambient Natural Convection • Four layer board (2s2p) | - | 53 | °C/W | (8), (10) |
| $R_{\theta JMA}$ | Junction to Ambient (@200 ft/min.) • Single layer board (1s) | - | 80 | °C/W | (8), (10) |
| $R_{\theta JMA}$ | Junction to Ambient (@200 ft/min.) • Four layer board (2s2p) | - | 49 | °C/W | (8), (10) |
| $R_{\theta JB}$ | Junction to Board | - | 34 | °C/W | (11) |
| $R_{\theta JC}$ | Junction to Case | - | 25 | °C/W | (12) |
| THERMAL RESISTANCE AND PACKAGE DISSIPATION RATINGS (CONTINUED) | | | | | |
| Ψ_{JT} | Junction to Package Top • Natural Convection | - | 6.0 | °C/W | (13) |

Notes

- Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.
- Freescall's Package Reflow capability meets the Pb-free requirements for JEDEC standard J-STD-020C, for Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL).
- Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
- Per JEDEC JESD51-6 with the board horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Junction to Ambient Thermal Resistance Nomenclature: the JEDEC specification reserves the symbol $R_{\theta JA}$ or θJA (Theta-JA) strictly for junction-to-ambient thermal resistance on a 1s test board in natural convection environment. $R_{\theta JMA}$ or θJMA (Theta-JMA) will be used for both junction-to-ambient on a 2s2p test board in natural convection and for junction-to-ambient with forced convection on both 1s and 2s2p test boards. It is anticipated that the generic name, Theta-JA, will continue to be commonly used.

The JEDEC standards can be consulted at <http://www.jedec.org/>

5.2.1 Estimation of Junction Temperature

An estimation of the chip junction temperature T_J can be obtained from the equation

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

- T_A = Ambient temperature for the package in °C
- $R_{\theta JA}$ = Junction to ambient thermal resistance in °C/W
- P_D = Power dissipation in the package in W

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board $R_{\theta JA}$ and the value obtained on a four layer board $R_{\theta JMA}$. Actual application PCBs show a performance close to the simulated four layer board value although this may be somewhat degraded in case of significant power dissipated by other components placed close to the device.

At a known board temperature, the junction temperature T_J is estimated using the following equation

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where

- T_B = Board temperature at the package perimeter in °C
- $R_{\theta JB}$ = Junction to board thermal resistance in °C/W
- P_D = Power dissipation in the package in W

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made.

5.2.2 Power Dissipation

During operation, the temperature of the die should not exceed the maximum junction temperature. To optimize thermal management and avoid overheating, the 34709 PMIC provides a thermal management system. The thermal protection is based on a circuit with a voltage output that is proportional to the absolute temperature. This voltage can be read via the ADC for specific temperature readouts, see [Analog to Digital Converter](#).

This voltage is monitored by an integrated comparator. Interrupts THERM110, THERM120, THERM125, and THERM130 will be generated when crossing in either direction of the thresholds specified in [Table 6](#). The temperature range can be determined by reading the THERMxxxS bits.

Thermal protection is integrated to power off the 34709 PMIC, in case of over dissipation. This thermal protection will act above the maximum junction temperature to avoid any unwanted power downs. The protection is debounced for 8.0 ms in order to suppress any thermal noise. This protection should be considered as a fail-safe mechanism and therefore the application should be designed such that this protection is not tripped under normal conditions. The temperature thresholds and the sense bit assignment are listed in [Table 6](#).

Table 6. Thermal Protection Thresholds

| Parameter | Min | Typ | Max | Units | Notes |
|-------------------------------------|-----|-----|-----|-------|-------|
| Thermal 110 °C threshold (THERM110) | 105 | 110 | 115 | °C | |
| Thermal 120 °C threshold (THERM120) | 115 | 120 | 125 | °C | |
| Thermal 125 °C threshold (THERM125) | 120 | 125 | 130 | °C | |
| Thermal 130 °C threshold (THERM130) | 125 | 130 | 135 | °C | |
| Thermal warning hysteresis | 2.0 | - | 4.0 | °C | (14) |
| Thermal protection threshold | 130 | 140 | 150 | °C | |

Notes

14. Equivalent to approx. 30 mW min, 60 mW max

5.3 Electrical Characteristics

5.3.1 Recommended Operating Conditions

Table 7. Recommended Operating Conditions

| Symbol | Description (Rating) | Min. | Max. | Unit | Notes |
|---------------------|-----------------------|------|------|------|-------|
| V _{BP} | Main Input Supply | 3.0 | 4.5 | V | |
| V _{LICELL} | LICELL Backup Battery | 1.8 | 3.6 | V | |
| T _A | Ambient Temperature | -40 | 85 | °C | |

5.3.2 General PMIC Specifications

Table 8. Pin Logic Thresholds

| Pin Name | Internal Termination ⁽¹⁹⁾ | Parameter | Load Condition | Min | Max ⁽²²⁾ | Unit | Notes |
|---|--------------------------------------|-------------|----------------|-----------------|---------------------|------|------------|
| PWRON1, PWRON2, GLBRST | Pull-up | Input Low | 47 kOhm | 0.0 | 0.3 | V | (16) |
| | | Input High | 1.0 MOhm | 1.0 | VCOREDIG | V | (16) |
| STANDBY, WDI | Weak Pull-down | Input Low | - | 0.0 | 0.3 | V | (21) |
| | | Input High | - | 0.9 | 3.6 | V | (21) |
| CLK32K | CMOS | Output Low | -100 µA | 0.0 | 0.2 | V | |
| | | Output High | 100 µA | CLK32KVCC - 0.2 | CLK32KVCC | V | |
| CLK32KMCU | CMOS | Output Low | -100 µA | 0.0 | 0.2 | V | |
| | | Output High | 100 µA | VSRTC - 0.2 | VSRTC | V | |
| RESETB, RESETBMCU, SDWNB, SW1PWGD, SW2PWGD | Open-drain | Output Low | -2.0 mA | 0.0 | 0.4 | V | (20) |
| | | Output High | Open-drain | - | 3.6 | V | (20) |
| GPIOLV1,2,3,4 | CMOS | Input Low | - | 0.0 | 0.3 * GPIOVDD | V | |
| | | Input High | - | 0.7 * GPIOVDD | GPIOVDD + 0.3 | V | |
| | | Output Low | - | 0.0 | 0.2 | V | |
| | | Output High | - | GPIOVDD - 0.2 | GPIOVDD | V | |
| | Open-drain | Output Low | -2.0 mA | 0.0 | 0.4 | V | |
| | | Output High | Open-drain | - | GPIOVDD + 0.3 | V | |
| PWM1, PWM2 | CMOS | Output Low | - | 0.0 | 0.2 | V | |
| | | Output High | - | GPIOVDD - 0.2 | GPIOVDD | V | |
| CLK, MOSI | | Input Low | - | 0.0 | 0.3 * SPIVCC | V | (15) |
| | | Input High | - | 0.7 * SPIVCC | SPIVCC + 0.3 | V | (15) |
| CS | Weak Pull-down | Input Low | - | 0.0 | 0.4 | V | (15) |
| | | Input High | - | 1.1 | SPIVCC + 0.3 | V | (15) |
| CS, MOSI (at Booting for SPI / I ² C decoding) | Weak Pull-down on CS | Input Low | - | 0.0 | 0.3 * VCOREDIG | V | (15), (23) |
| | | Input High | - | 0.7 * VCOREDIG | VCOREDIG | V | (15), (23) |

Table 8. Pin Logic Thresholds

| Pin Name | Internal Termination ⁽¹⁹⁾ | Parameter | Load Condition | Min | Max ⁽²²⁾ | Unit | Notes |
|----------------|--------------------------------------|--------------------------|----------------|--------------|---------------------|------|---------------------------|
| MISO, INT | CMOS | Output Low | -100 μ A | 0.0 | 0.2 | V | MISO ^{(15) (24)} |
| | | Output High | 100 μ A | SPIVCC - 0.2 | SPIVCC | V | MISO ^{(15) (24)} |
| PUMS1,2,3,4,5 | | Input Low PUMSxS = 0 | - | 0.0 | 0.3 | V | ⁽¹⁷⁾ |
| | | Input High PUMSxS = 1 | - | 1.0 | VCOREDIG | V | ⁽¹⁷⁾ |
| ICTEST | | Input Low | - | 0.0 | 0.3 | V | ⁽¹⁸⁾ |
| | | Input High | - | 1.1 | 1.7 | V | ⁽¹⁸⁾ |
| SW1CFG, SW4CFG | | Input Low | - | 0.0 | 0.3 | V | |
| | | Input Mid | - | 1.3 | 2.0 | V | |
| | | Input High | - | 2.5 | 3.1 | V | |

Notes

15. SPIVCC is typically connected to the output of buck regulator SW5 and set to 1.800 V
16. Input has internal pull-up to VCOREDIG equivalent to 200 kOhm
17. Input state is latched in first phase of cold start, refer to [Serial Interfaces](#) for a description of the PUMS configuration
18. Input state is not latched
19. A weak pull-down represents a nominal internal pull-down of 100 nA, unless otherwise noted
20. RESETB, RESETBMCU, SDWNB, SW1PWGD, SW2PWGD have open-drain outputs, external pull-ups are required
21. SPIVCC needs to remain enabled for proper detection of WDI High to avoid involuntary shutdown
22. The maximum should never exceed the maximum rating of the pin as given in [Pin Connections](#)
23. The weak pull-down on CS is disabled if a VIH is detected at start-up to avoid extra consumption in I²C mode
24. The output drive strength is programmable

5.3.3 Current Consumption

[Table 9](#) provides the current consumption for standard use cases.

Table 9. Current Consumption Summary ⁽²⁷⁾

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Mode | Description | Typ | Max | Unit | Notes |
|--------------------|---|-----|-----|------|-------|
| RTC / Power cut | All blocks disabled, BP=0, coin cell is attached to LICELL (at 25 °C only) <ul style="list-style-type: none"> • RTC Logic • VCORE Module • VSRTC • 32 k Oscillator • CLK32KMCU buffer active(10 pF load) | 4.0 | 8.0 | μA | |
| OFF (good battery) | All blocks disabled, BP>3.0 V(at 25 °C only) <ul style="list-style-type: none"> • Digital Core • RTC Logic • VCORE Module • VSRTC • 32 k Oscillator • CLK32KMCU buffer active (10 pF load) • COINCHEN = 0 | 20 | 55 | μA | |
| ON Standby | Low-power Mode (Standby pin asserted and ON_STBY_LP=1) <ul style="list-style-type: none"> • Digital core • RTC logic • VCORE module • VSRTC • CLK32KMCU/CLK32K active (10 pF load) • 32 k oscillator • I_{REF} • SW1, SW2, SW3, SW4A, SW4B, SW5 in PFM ^{(26),(29)} • VDDREF, VPLL, VGEN1, VGEN2, VUSB2, VDACC • SWBST off in low-power mode ^{(25),(28)} | 260 | 650 | μA | |

Table 9. Current Consumption Summary ⁽²⁷⁾

Characteristics noted under conditions BP = 3.6 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

| Mode | Description | Typ | Max | Unit | Notes |
|------------|--|-----|-----|------|-------|
| ON Standby | <ul style="list-style-type: none"> • Digital core • RTC logic • VCORE module • VSRTC • CLK32KMCU/CLK32K active (10 pF load) • 32 k oscillator • Digital • I_{REF} • SW1, SW2, SW3, SW4A, SW4B, SW5 in PFM ^{(26),(29)} • VDDREF, VPLL, VGEN1, VGEN2, VUSB2, VDAC on in low-power mode ^{(26),(28)} • SWBST off • PLL | 370 | 750 | μA | |

Notes

- 25. Equivalent to approx. 30 mW min, 60 mW max
- 26. Current in RTC Mode is from LICELL=2.5 V; in all other modes from BP = 3.6 V.
- 27. External loads are not included
- 28. VUSB2, VGEN2 external pass PNPs
- 29. SW4A output 2.5 V

6 General Description

6.1 Features

Power Generation

- Six buck switching regulators
 - Two single/dual phase buck regulators
 - Three single phase buck regulators
 - Up to six independent outputs
 - PFM/PWM operation mode
 - Dynamic voltage scaling
- Boost regulator
 - Support for USB physical layer on i.MX processor (USB PHY)
- Eight LDO regulators
 - Two with selectable internal or external pass devices
 - Four with embedded pass devices
 - One with an external PNP device
 - Voltage reference for DDR memory with internal PMOS device

Analog to Digital Converter

- Seven general purpose channels
- Dedicated channels for monitoring die temperature and coin cell voltage
- Resistive touchscreen interface

Auxiliary Circuits

- General purpose I/Os
- PWM outputs

Clocking and Oscillators

- Real time clock
 - Time and day counters
 - Time of day alarm
- 32.768 kHz crystal oscillator
 - Coin cell battery backup and charger

Serial Interface

- SPI
- I²C

6.2 Block Diagram

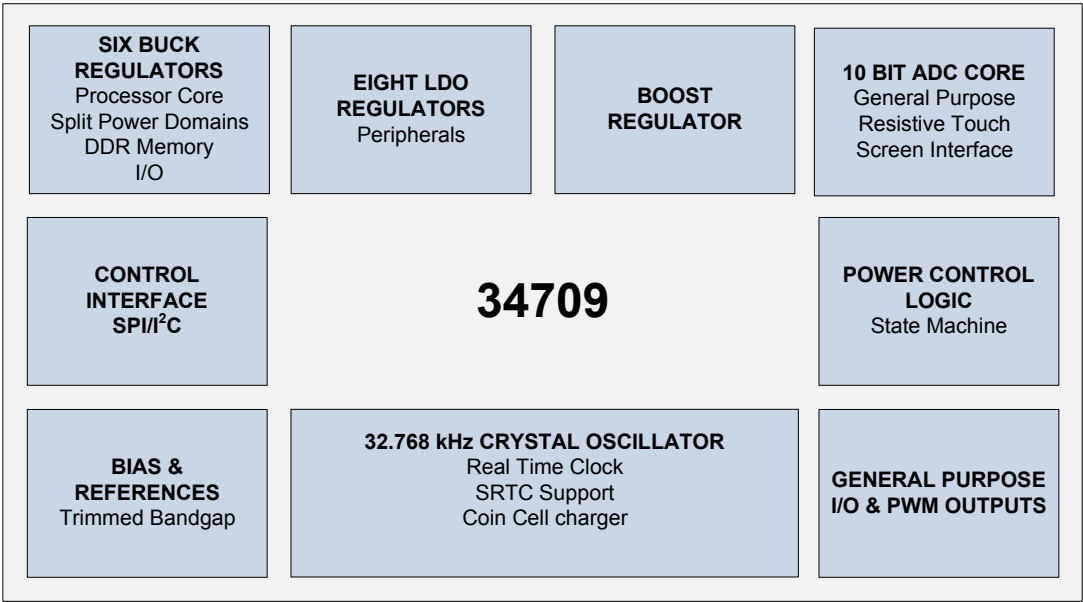


Figure 4. Functional Block Diagram

7 Functional Block Description

7.1 Start-up Requirements

Upon application of power, there is an initial delay of 8.0 ms during which the core circuitry is enabled. Then the switching and linear regulators are sequentially enabled in time slots of 2.0 ms steps. This allows the PMIC to limit the inrush current.

The outputs of the switching regulators not enabled, are discharged with weak pull-downs on the output to ensure a proper power-up sequence. Any under-voltage detection at BP is masked while the power-up sequencer is running. When the switching regulators are enabled, they will start in PWM mode. After 3.0 ms the switching regulators will transition to the mode programmed in the SPI register map.

The Power-up Mode Select pins PUMSx (x = 1,2,3,4,5) are used to configure the start-up characteristics of the regulators. Supply enabling and output level options are selected by hardwiring the PUMSx pins. It is recommended to minimize the load during system boot-up by supplying only the essential voltage domains. This allows the start-up transients to be minimized after which the rest of the system power tree can be brought up by software. The PUMSx pins also allows optimization of the supply sequence and default values. Software code can load the required programmable options without any change to hardware.

The state of the PUMSx pins are latched before any of the regulators are enabled, with the exception of VCORE. PUMSx options and start-up configurations are robust to a PCUT event, whether occurring during normal operation or during the 8.0 ms of pre-sequencer initialization, i.e. the system will not end up in an unexpected / undesirable consumption state.

[Table 10](#) shows the initial setup for the voltage level of the switching and linear regulators, and whether they get enabled or not.

Table 10. Power-up Defaults

| i.MX | Reserved | 53 LPM | 53 DDR2 | 53 DDR3 | 53 LVDDR3 | 53 LVDDR2 | 50 mDDR | 50 LPDDR2 | 50 LPDDR2 | 50 mDDR | 50 LPDDR2 | 50 mDDR |
|--------------------------------|-----------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|---------------|
| PUMS[4:1] | 0000-0100 | 0101 | 0110 | 0111 | 1000 | 1001 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
| PUMS5=0 VUSB2 VGEN2 | Reserved | Ext PNP | Ext PNP | Ext PNP | Ext PNP | Ext PNP | Ext PNP | Ext PNP | Ext PNP | Ext PNP | Ext PNP | Ext PNP |
| PUMS5=1 VUSB2 VGEN2 | Reserved | Internal PMOS | Internal PMOS | Internal PMOS | Internal PMOS | Internal PMOS | Internal PMOS | Internal PMOS | Internal PMOS | Internal PMOS | Internal PMOS | Internal PMOS |
| SW1A (VDDGP) | Reserved | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 |
| SW1B (VDDGP) | Reserved | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 | 1.1 |
| SW2 ⁽³⁰⁾ (VCC) | Reserved | 1.225 | 1.3 | 1.3 | 1.3 | 1.3 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| SW3 ⁽³⁰⁾ (VDDA) | Reserved | 1.2 | 1.3 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| SW4A ⁽³⁰⁾ (DDR/SYS) | Reserved | 1.5 | 1.8 | 1.5 | 1.35 | 1.2 | 1.8 | 1.2 | 3.15 | 3.15 | 3.15 | 3.15 |
| SW4B ⁽³⁰⁾ (DDR/SYS) | Reserved | 1.5 | 1.8 | 1.5 | 1.35 | 1.2 | 1.8 | 1.2 | 1.2 | 1.8 | 1.2 | 1.8 |
| SW5 ⁽³⁰⁾ (I/O) | Reserved | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 |
| SWBST | Reserved | Off | Off | Off | Off | Off | Off | Off | Off | Off | Off | Off |
| VUSB ⁽³¹⁾ | Reserved | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 |
| VUSB2 | Reserved | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 |

Table 10. Power-up Defaults

| i.MX | Reserved | 53 LPM | 53 DDR2 | 53 DDR3 | 53 LVDDR3 | 53 LVDDR2 | 50 mDDR | 50 LPDDR2 | 50 LPDDR2 | 50 mDDR | 50 LPDDR2 | 50 mDDR |
|---------|----------|--------|---------|---------|-----------|-----------|---------|-----------|-----------|---------|-----------|---------|
| VSRTC | Reserved | 1.2 | 1.3 | 1.3 | 1.3 | 1.3 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| VPLL | Reserved | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 | 1.8 |
| VREFDDR | Reserved | On | On | On | On | On | On | On | On | On | On | On |
| VDAC | Reserved | 2.775 | 2.775 | 2.775 | 2.775 | 2.775 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 |
| VGEN1 | Reserved | 1.2 | 1.3 | 1.3 | 1.3 | 1.3 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 | 1.2 |
| VGEN2 | Reserved | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 3.1 | 3.1 | 3.1 | 3.1 | 2.5 | 2.5 |

Notes

30. The SWx node are activated in APS mode when enabled by the start-up sequencer.
31. VUSB is supplied by SWBST.

The power-up sequence is shown in [Tables 11](#) and [12](#). VCOREDIG, VSRTC, and VCORE, are brought up in the pre-sequencer start-up.

Table 11. Power-up Sequence i.MX53

| Tap x 2.0 ms | PUMS [4:1] = [0101,0110,0111,1000,1001] (i.MX53) |
|--------------|--|
| 0 | SW2 (VCC) |
| 1 | VPLL (NVCC_CKIH = 1.8 V) |
| 2 | VGEN2 (VDD_REG= 2.5 V, external PNP) |
| 3 | SW3 (VDDA) |
| 4 | SW1A/B (VDDGP) |
| 5 | SW4A/B, VREFDDR (DDR/SYS) |
| 6 | |
| 7 | SW5 (I/O), VGEN1 |
| 8 | VUSB, VUSB2 |
| 9 | VDAC |

Table 12. Power-up Sequence i.MX50

| Tap x 2.0 ms | PUMS [4:1] = [0100, 1011, 1100, 1101, 1110, 1111] (i.MX50/I.MX53) |
|--------------|---|
| 0 | SW2 |
| 1 | SW3 |
| 2 | SW1A/B |
| 3 | VDAC |
| 4 | SW4A/B, VREFDDR |
| 5 | SW5 |
| 6 | VGEN2, VUSB2 |
| 7 | VPLL |
| 8 | VGEN1 |
| 9 | VUSB |

7.2 Bias and References Block

All regulators use the main bandgap as the reference. The main bandgap is bypassed with a capacitor at VCOREREf. The bandgap and the rest of the core circuitry is supplied from VCore. The performance of the regulators is directly dependent on the performance of VCore and the bandgap. No external DC loading is allowed on VCOREDIG or VCOREREf. VCOREDIG is kept powered as long as there is a valid supply and/or coin cell. [Table 13](#) shows the main characteristics of the core circuitry.

Table 13. Core Voltages Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---|---|-----|-------|-----|------|-------|
| VCOREDIG (DIGITAL CORE SUPPLY) | | | | | | |
| V _{COREDIG} | Output voltage | - | 1.5 | - | V | (32) |
| | • ON mode • OFF with good battery and RTC mode | - | 1.2 | - | | |
| C _{COREDIG} | V _{COREDIG} bypass capacitor | - | 1.0 | - | μF | |
| VDDL (DIGITAL CORE SUPPLY - LOWER POWER) | | | | | | |
| V _{DLL} | Output voltage | - | 1.5 | - | V | (33) |
| | • ON mode with good battery | - | 1.2 | - | | |
| | • OFF mode with good battery • RTC mode | - | 1.2 | - | | |
| C _{DLL} | V _{DLL} bypass capacitor | - | 100 | - | pF | (34) |
| VCore (ANALOG CORE SUPPLY) | | | | | | |
| V _{Core} | Output voltage | - | 2.775 | - | V | (32) |
| | • ON mode and charging • OFF and RTC mode | - | 0.0 | - | | |
| C _{Core} | V _{Core} bypass capacitor | - | 1.0 | - | μF | |
| VCOREREf (BANDGAP / REGULATOR REFERENCE) | | | | | | |
| V _{COREREf} | Output voltage | - | 1.2 | - | V | (32) |
| | Absolute accuracy | - | 0.5 | - | % | |
| | Temperature drift | - | 0.25 | - | % | |
| C _{COREREf} | V _{COREREf} bypass capacitor | - | 100 | - | nF | |

Notes

32. $3.0\text{ V} < \text{BP} < 4.5\text{ V}$, no external loading on VCOREDIG, VDDL, VCore, or VCOREREf. Extended operation down to UVDET, but no system malfunction.
33. Powered by VCOREDIG
34. Maximum capacitance on VDDL should not exceed 1000 pF, including the board capacitance.

7.3 Clocking and Oscillators

7.3.1 Clock Generation

A system clock is generated for internal digital circuitry as well as for external applications utilizing the clock output pins. A crystal oscillator is used for the 32.768 kHz time base and generation of related derivative clocks. If the crystal oscillator is not running (for example, if the crystal is not present), an internal 32 kHz oscillator will be used instead.

Support is also provided for an external Secure Real Time Clock (SRTC), which may be integrated on a companion system processor IC. For media protection in compliance with Digital Rights Management (DRM) system requirements, the CLK32KMCU can be provided as a reference to the SRTC module where tamper protection is implemented.

7.3.1.1 Clocking Scheme

The internal 32 kHz oscillator is an integrated backup for the crystal oscillator, and provides a 32.768 kHz nominal frequency at $\pm 60\%$ accuracy, if running. The internal oscillator only runs if a valid supply is available at BP, and would not be used as long as the crystal oscillator is active. In absence of a valid supply at the BP supply node (for instance due to a dead battery), the crystal oscillator continues running supplied from the coin cell battery. All control functions will run off the crystal derived frequency, occasionally referred to as “32 kHz” for brevity’s sake.

During the switchover between the two clock sources (such as when the crystal oscillator is starting up), the output clock is maintained at a stable active low or high phase of the internal 32 kHz clock to avoid any clocking glitches. If the XLTAL clock source suddenly disappears during operation, the IC will revert back to the internal clock source. Given the unpredictable nature of the event and the start-up times involved, the clock may be absent long enough for the application to shut down during this transition.

A status bit, CLKS, is available to indicate to the processor which clock is currently selected: CLKS=0 when the internal RC is used and CLKS=1 if the crystal source is used. The CLKI interrupt bit will be set whenever a change in the clock source occurs, and an interrupt will be generated if the corresponding CLKM mask bit is cleared.

7.3.1.2 Oscillator Specifications

The crystal oscillator has been optimized for use in conjunction with the Micro Crystal CC7V-T1A32.768 kHz-9.0 pF-30 ppm or equivalent (such as Micro Crystal CC5V-T1A or Epson FC135) and is capable of handling its parametric variations. Ensure that the chosen crystal has a typical drive level of 0.5 μ W or above to ensure proper operation of the crystal oscillator. Using a crystal with a lower drive level can cause overtone oscillations

The electrical characteristics of the 32 kHz Crystal oscillator are given in the following table, taking into account the crystal characteristics noted above. The oscillator accuracy depends largely on the temperature characteristics of the used crystal. Application circuits can be optimized for required accuracy by adapting the external crystal oscillator network (via component accuracy and/or tuning). Additionally, a clock calibration system is provided to adjust the 32,768 cycle counter that generates the 1.0 Hz timer and RTC registers; see [SRTC Support](#) for more detail.

Table 14. Oscillator and Clock Main Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|------------------------------------|--|------------|--------|------------|---------|-------|
| OSCILLATOR AND CLOCK OUTPUT | | | | | | |
| V_{INRTC} | Operating Voltage | | | | | |
| | <ul style="list-style-type: none"> Oscillator and RTC Block from BP Oscillator and RTC Block from LICELL | 1.8 1.8 | - - | 4.5 3.6 | V | |
| I_{INRTC} | Operating Current Crystal Oscillator and RTC Module | | | | | |
| | <ul style="list-style-type: none"> All blocks disabled, no main battery attached, coin cell is attached to LICELL | - | 2.0 | 5.0 | μ A | |

Table 14. Oscillator and Clock Main Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|------------------------|---|-----|-----|-----|------|-------|
| $t_{\text{START-RTC}}$ | RTC oscillator start-up time • Upon application of power | - | - | 1.0 | sec | |

OSCILLATOR AND CLOCK OUTPUT (CONTINUED)

| | | | | | | |
|--------------------|---|----------------------------|--------|--------------------|---|--|
| V_{RTCLO} | Output Low • CLK32K Output sink 100 μA • CLK32KMCU Output source 50 μA | 0.0 | - | 0.2 | V | |
| V_{RTCHI} | Output High • CLK32K Output source 100 μA • CLK32KMCU Output sink 50 μA | CLK32KVCC-0.2 VSRTC-0.2 | - - | CLK32KVCC VSRTC | V | |

OSCILLATOR AND CLOCK OUTPUT (CONTINUED)

| | | | | | | |
|---|---|------------------|--------------------------|------------------|-----------|--|
| t_{CLK32KET} | CLK32K Rise and Fall Time, CL = 50 pF • CLK32KDRV [1:0] = 00 • CLK32KDRV [1:0] = 01 (default) • CLK32KDRV [1:0] = 10 • CLK32KDRV [1:0] = 11 | - - - - | 6.0 2.5 3.0 2.0 | - - - - | ns | |
| $t_{\text{CKL32KMCUET}}$ | CLK32KMCU Rise and Fall Time • CL = 12 pF | - | 22 | - | ns | |
| CLK32K _{DC} / CLK32K MCU _{DC} | CLK32K and CLK32KMCU Output Duty Cycle • Crystal on XTAL1, XTAL2 pins | 45 | - | 55 | % | |
| | RMS Output Jitter • 1 Sigma for Gaussian distribution | - | - | 30 | ns RMS | |

7.3.2 SRTC Support

When configured for DRM mode (SPI bit DRM = 1), the CLK32KMCU driver will be kept enabled through all operational states to ensure that the SRTC module always has its reference clock. If DRM = 0, the CLK32KMCU driver will not be maintained in the Off state.

It is also necessary to provide a means for the processor to do an RTC initiated wake-up of the system if it has been programmed for such capability. This can be accomplished by connecting an open-drain NMOS driver to the PWRON pin of the 34709 PMIC, so that, there is a parallel path for the power key. The 34709 PMIC will not be able to discern the turn on event from a normal power key initiated turn on, but the processor should have the knowledge, since the RTC initiated turn on is generated locally.

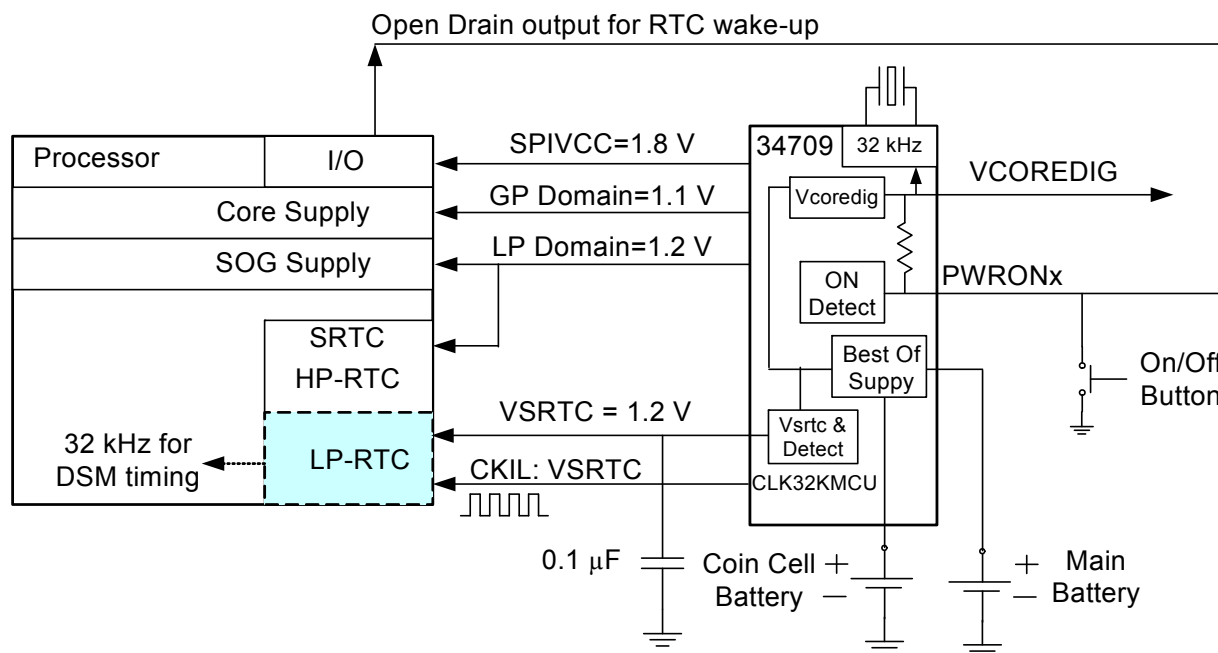


Figure 5. SRTC Block Diagram

7.3.2.1 VSRTC

The VSRTC regulator provides the CLK32KMCU output level. Additionally, it is used to bias the Low-power SRTC domain of the SRTC module integrated on certain FSL processors. The VSRTC regulator is enabled as soon as the RTCPORB is detected. VSRTC cannot be disabled.

Depending on the configuration of the PUMS[4:0] pins, the VSRTC voltage will be set to 1.3 or 1.2 V.

1. With PUMS[4:0] = (0110, 0111, 1000, or 1001) VSRTC will be set to 1.3 V in on mode (on, on standby and on standby low-power modes), and it will drop to 1.2 V in off and coin cell modes.
2. With PUMS[4:0] different than (0110, 0111, 1000, or 1001), VSRTC will be set to 1.2 V for all modes (on, on standby, on standby low-power mode, off, and coin cell).

Table 15. VSRTC Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------|----------------|-----|-----|-----|------|-------|
|--------|----------------|-----|-----|-----|------|-------|

GENERAL

| | | | | | | |
|---------------------|---|------------|--------|------------|----|------|
| V _{SRTCIN} | Operating Input Voltage Range <ul style="list-style-type: none"> Valid Coin Cell range Valid BP | 1.8 1.8 | - - | 3.6 4.5 | V | |
| I _{SRTC} | Operating Current Load Range | 0.0 | - | 50 | μA | (35) |
| CO _{SRTC} | Bypass Capacitor Value | - | 0.1 | - | μF | |

VSRTC - ACTIVE MODE - DC

| | | | | | | |
|-------------------|---|------|------|------|---|--|
| V _{SRTC} | <p>Output Voltage</p> <ul style="list-style-type: none"> • V_{SRTCINMIN} < V_{SRTCIN} < V_{SRTCINMAX} • I_{SRTCIN} < I_{SRTC} < I_{SRTCINMAX} • Off and coin cell mode | 1.15 | 1.20 | 1.28 | V | |
|-------------------|---|------|------|------|---|--|

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Table 15. VSRTC Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---|--|------|-----|------|---------------|-------|
| VSRTC - ACTIVE MODE - DC (CONTINUED) | | | | | | |
| V_{SRTC} | Output Voltage <ul style="list-style-type: none"> $V_{\text{SRTCINMIN}} < V_{\text{STRCIN}} < V_{\text{SRTCINMAX}}$ $I_{\text{SRTCIN}} < I_{\text{SRTC}} < I_{\text{SRTCINMAX}}$ PUMS[4:0] \neq (0110, 0111, 1000, 1001) On, Standby, and Standby LPM modes | 1.15 | 1.2 | 1.25 | V | |
| V_{SRTC} | Output Voltage <ul style="list-style-type: none"> $V_{\text{SRTCINMIN}} < V_{\text{STRCIN}} < V_{\text{SRTCINMAX}}$ $I_{\text{SRTCIN}} < I_{\text{SRTC}} < I_{\text{SRTCINMAX}}$ PUMS[4:0] = (0110, 0111, 1000, 1001) On, Standby, and Standby LPM modes | 1.25 | 1.3 | 1.35 | V | |
| I_{SRTCQ} | Active Mode Quiescent Current <ul style="list-style-type: none"> $V_{\text{SRTCINMIN}} < V_{\text{STRCIN}} < V_{\text{SRTCINMAX}}$ $I_{\text{SRTC}} = 0$ | - | 0.8 | - | μA | |
| V_{SRTCOS} | Start-up Overshoot (IL = 0.0 mA) <ul style="list-style-type: none"> Battery insertion Coin cell insertion Switchover Overshoot (IL = 0.0 mA) <ul style="list-style-type: none"> Battery to coin cell Coin cell to battery | - | - | 1.42 | V | (36) |

Notes

35. Valid for BP > 2.4 V and/or LICELL > 2.0 V
36. See workaround [Figure 24](#).

7.3.2.2 Real Time Clock

A Real Time Clock (RTC) is provided with time and day counters as well as an alarm function. The RTC utilizes the 32.768 kHz crystal oscillator for the time base and is powered by the coin cell backup supply when BP has dropped below operational range. In configurations where the SRTC is used, the RTC can be disabled to conserve current drain by setting the RTCDIS bit to a 1 (defaults on at power up).

Time and Day Counters

The 32.768 kHz clock is divided into a 1.0 Hz time tick which drives a 17-bit Time Of Day (TOD) counter. The TOD counter counts the seconds during a 24 hour period from 0 to 86,399 and will then roll over to 0. When the roll over occurs, it increments the 15-bit DAY counter. The DAY counter can count up to 32767 days. The 1.0 Hz time tick can be used to generate a 1HZI interrupt if unmasked.

Time Of Day Alarm

A Time Of Day Alarm (TODA) function can be used to turn on the application and alert the processor. If the application is already on, the processor will be interrupted. The TODA and DAYA registers are used to set the alarm time. When the TOD counter is equal to the value in TODA and the DAY counter is equal to the value in DAYA, the TODAI interrupt will be generated.

Timer Reset

As long as the supply at BP is valid, the real time clock will be supplied from VCOREDIG. If BP is not valid, the real time clock can be backed up from a coin cell via the LICELL pin. When the VSRTC voltage drops to the range of 0.9 V to 0.8 V, the RTPORB reset signal is generated and the contents of the RTC will be reset. Additional registers backed up by coin cell will also reset with RTPORB. To inform the processor that the contents of the RTC are no longer valid due to the reset, a timer reset interrupt function is implemented with the RTCRSTI bit.

RTC Timer Calibration

A clock calibration system is provided to adjust the 32,768 cycle counter that generates the 1.0 Hz timer for RTC timing registers. The general implementation relies on the system processor to measure the 32.768 kHz crystal oscillator against a higher frequency and more accurate system clock, such as a TCXO. If the RTC timer needs a correction, a 5-bit 2's complement calibration word can be sent via the SPI, to compensate the RTC for inaccuracy in its reference oscillator.

Table 16. RTC calibration Settings

| Code in RTCCAL[4:0] | Correction in Counts per 32768 | Relative correction in ppm |
|---------------------|--------------------------------|----------------------------|
| 01111 | +15 | +458 |
| 00011 | +3 | +92 |
| 00001 | +1 | +31 |
| 00000 | 0 | 0 |
| 11111 | -1 | -31 |
| 11101 | -3 | -92 |
| 10001 | -15 | -458 |
| 10000 | -16 | -488 |

The available correction range should be sufficient to ensure drift accuracy in compliance with standards for DRM time keeping. Note that the 32.768 kHz oscillator is not affected by RTCCAL settings; calibration is only applied to the RTC time base counter. Therefore, the frequency at the clock output CLK32K is not affected.

The RTC system calibration is enabled by programming the RTCCALMODE[1:0] for desired behavior by operational mode.

Table 17. RTC Calibration Enabling

| RTCCALMODE | Function |
|------------|--|
| 00 | RTC Calibration disabled (default) |
| 01 | RTC Calibration enabled in all modes except coin cell only |
| 10 | Reserved for future use. Do not use. |
| 11 | RTC Calibration enabled in all modes |

The RTC Calibration circuitry can be automatically disabled when main battery contact is lost or if it is so deeply discharged that RTC power draw is switched to the coin cell (configured with RTCCALMODE=01).

Because of the low RTC consumption, RTC accuracy can be maintained through long periods of the application being shut down, even after the main battery has discharged. However, it is noted that the calibration can only be as good as the RTCCAL data that has been provided, so occasional refreshing is recommended to ensure that any drift influencing environmental factors have not skewed the clock beyond desired tolerances.

7.3.3 Coin Cell Battery Backup

The LICELL pin provides a connection for a coin cell backup battery or supercap. If the main battery is deeply discharged, removed, or contact-bounced (for example during a power cut), the RTC system and the logic maintained by the coin cell will switch over to the LICELL for backup power. This switch over occurs for a BP below 1.8 V threshold with LICELL greater than 1.8 V. A 0.1 μ F capacitor should be placed from LICELL to ground under all circumstances.

Upon initial insertion of the coin cell, it is not immediately connected to the on chip circuitry. The cell gets connected when the IC powers on, or after enabling the coin cell charger when the IC was already on.

The coin cell charger circuit will function as a current-limited voltage source, resulting in the CC/CV taper characteristic typically used for rechargeable Lithium-Ion batteries. The coin cell charger is enabled via the COINCHEN bit. The coin cell voltage is programmable through the VCOIN[2:0] bits. The coin cell charger voltage is programmable in the ON state where the charge current is fixed at ICOINH1.

If COINCHEN=1 when the system goes into an Off or User Off state, the coin cell charger will continue to charge to the predefined voltage setting, but at a lower maximum current ICOINLO. This compensates for self discharge of the coin cell and ensures that when the main cell gets depleted, the coin cell will be topped off for maximum RTC retention. The coin cell charging will be stopped for the BP below UVDET. The bit COINCHEN itself is only cleared when an RTCPORB occurs.

Table 18. Coin Cell Voltage Specifications

| VCOIN[2:0] | Output Voltage |
|------------|----------------|
| 000 | 2.50 |
| 001 | 2.70 |
| 010 | 2.80 |
| 011 | 2.90 |
| 100 | 3.00 |
| 101 | 3.10 |
| 110 | 3.20 |
| 111 | 3.30 |

Table 19. Coin Cell Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------------------------|--|-----|-----|-----|---------------|-------|
| COIN CELL CHARGER | | | | | | |
| V_{LCELLACC} | Voltage Accuracy | - | 100 | - | mV | |
| I_{LCELLON} | Coin Cell Charge Current in On and Watchdog modes ICOINH1 | - | 60 | - | μA | |
| I_{LCELLOFF} | Coin Cell Charge Current in Off, cold start/warm start, and Low-power Off modes (User Off / Memory Hold) ICOINLO | - | 10 | - | μA | |
| I_{LCELLACC} | Current Accuracy | - | 30 | - | % | |
| CO_{LCELL} | LICELL Bypass Capacitor | - | 100 | - | nF | |
| | LICELL Bypass Capacitor as coin cell replacement | - | 4.7 | - | μF | |

7.4 Interrupt Management

7.4.1 Control

The system is informed about important events based on interrupts. Unmasked interrupt events are signaled to the processor by driving the INT pin high; this is true whether the communication interface is configured for SPI or I²C.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain set until cleared. Each interrupt can be cleared by writing a 1 to the appropriate bit in the Interrupt Status register, which will also cause the interrupt line to go low. If a new interrupt occurs while the processor clears an existing interrupt bit, the interrupt line will remain high.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when a masked interrupt bit goes high, the interrupt line will not go high. A masked interrupt can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the IC. The IC powers up with all interrupts masked, so the processor must initially poll the device to determine if any interrupts are active. Alternatively, the processor can unmask the interrupt bits of interest. If a masked interrupt bit was already high, the interrupt line will go high after unmasking.

The sense registers contain status and input sense bits, so the system processor can poll the current state of interrupt sources. They are read only, and not latched or clearable.

Interrupts generated by external events are debounced, therefore, the event needs to be stable throughout the debounce period before an interrupt is generated. Nominal debounce periods for each event are provided in [Table 20](#). Due to the asynchronous nature of the debounce timer, the effective debounce time can vary slightly.

7.4.2 Interrupt Bit Summary

[Table 20](#) summarizes all interrupt, mask, and sense bits associated with INT control. For more detailed behavioral descriptions, refer to the related chapters.

Table 20. Interrupt, Mask and Sense Bits

| Interrupt | Mask | Sense | Purpose | Trigger | Debounce Time |
|-----------|-----------|-----------|---|--------------|---------------------------|
| ADCDONEI | ADCDONEM | - | ADC has finished requested conversions | L2H | 0.0 |
| TSDONEI | TSDONEM | - | Touch screen has finished conversion | L2H | 0.0 |
| TSPENDET | TSPENDETM | - | Touch screen pen detect | Dual | 1.0 ms |
| LOWBATT | LOWBATTM | - | Low battery detect Sense is 1 if below LOWBATT threshold | H2L | Programmable VBATTDDB |
| SCPI | SCPM | - | Regulator short-circuit protection tripped | L2H | min. 4.0 ms max 8.0 ms |
| 1HZI | 1HZM | - | 1.0 Hz time tick | L2H | 0.0 |
| TODAI | TODAM | - | Time of day alarm | L2H | 0.0 |
| PWRON1I | PWRON1M | PWRON1S | Power on button 1 event Sense is 1 if PWRON1 is high. | H2L | 30 ms ⁽³⁷⁾ |
| | | | | L2H | 30 ms |
| PWRON2I | PWRON2M | PWRON2S | Power on button 2 event Sense is 1 if PWRON2 is high. | H2L | 30 ms ⁽³⁷⁾ |
| | | | | L2H | 30 ms |
| SYSRSTI | SYSRSTM | - | System reset through PWRONx pins | L2H | 0.0 |
| WDIRESETI | WDIRESETM | - | WDI silent system restart | L2H | 0.0 |
| PCI | PCM | - | Power cut event | L2H | 0.0 |
| WARMI | WARMM | - | Warm Start event | L2H | 0.0 |
| MEMHLDI | MEMHLDM | - | Memory Hold event | L2H | 0.0 |
| CLKI | CLKM | CLKS | 32 kHz clock source change Sense is 1 if source is XTAL | Dual | 0.0 |
| RTCSTI | RTCSTM | - | RTC reset has occurred | L2H | 0.0 |
| THERM110 | THERM110M | THERM110S | Thermal 110 °C threshold Sense is 1 if above threshold | Dual | 30 ms |
| THERM120 | THERM120M | THERM120S | Thermal 120 °C threshold Sense is 1 if above threshold | Dual | 30 ms |
| THERM125 | THERM125M | THERM125S | Thermal 125 °C threshold Sense is 1 if above threshold | Dual | 30 ms |
| THERM130 | THERM130M | THERM130S | Thermal 130 °C threshold Sense is 1 if above threshold | Dual | 30 ms |
| GPIOLVxI | GPIOLVxM | GPIOLVxS | General Purpose input interrupt | Programmable | Programmable |

Notes

37. Debounce timing for the falling edge can be extended with PWRONxDBNC[1:0]; refer to [Turn On Events](#) for details.

7.5 Power Generation

The 34709 PMIC provides reference and supply voltages for the application processor as well as peripheral device.

Six buck (step down) converters and one boost (step up) converters are included. One of the buck regulators can be configured in dual phase, single phase mode, or operate as separate independent outputs (in this case, there are six buck converters). The buck converters provide the supply to processor cores and to other low-voltage circuits such as IO and memory. Dynamic voltage scaling is provided to allow controlled supply rail adjustments for the processor cores and/or other circuitry. The boost converter supplies the VUSB regulator for the USB PHY on the processor. The VUSB regulator is powered from the boost to ensure sufficient headroom for the LDO through the normal discharge range of the main battery.

Linear regulators could be supplied directly from the battery or from one of the switching regulator, and provide supplies for IO and peripherals, such as audio, camera, Bluetooth, Wireless LAN, etc. Naming conventions are suggestive of typical or possible use case applications, but the switching and linear regulators may be utilized for other system power requirements within the guidelines of specified capabilities.

Four general purpose I/Os are available. When configured as inputs they can be used as external interrupts.

7.5.1 Power Tree

[Table 21](#) summarizes the available power supplies. Refer to sections [Buck Switching Regulators](#), [Boost Switching Regulator](#), and [Linear Regulators \(LDOs\)](#) for detailed information on performance metrics and operating ranges of each individual supply.

Table 21. Power Tree Summary

| Supply | Purpose (typical application) | Output Voltage (in V) | Load Capability (in mA) |
|---------|---|-------------------------------------|-------------------------|
| SW1 | Buck regulator for processor VDDGP domain | 0.650 – 1.4375 | 2000 |
| SW2 | Buck regulator for processor VCC domain | 0.650 – 1.4375 | 1000 |
| SW3 | Buck regulator for processor VDD domain and peripherals | 0.650 – 1.425 | 500 |
| SW4A | Buck regulator for DDR memory and peripherals | 1.200 – 1.85: 2.5/3.15 | 500 |
| SW4B | Buck regulator for DDR memory and peripherals | 1.200 – 1.85: 2.5/3.15 | 500 |
| SW5 | Buck regulator for I/O domain | 1.200 – 1.85 | 1000 |
| SWBST | Boost regulator for USB PHY support | 5.00/5.05/5.10/5.15 | 380 |
| VSRTC | Secure Real Time Clock supply | 1.2 | 0.05 |
| VPLL | Quiet Analog supply | 1.2/1.25/1.5/1.8 | 50 |
| VREFDDR | DDR Ref supply | 0.6 – 0.9 | 10 |
| VDAC | TV DAC supply, external PNP | 2.5/2.6/2.7/2.775 | 250 |
| VUSB2 | VUSB/peripherals supply, internal PMOS | 2.5/2.6/2.75/3.0 | 65 |
| | VUSB/peripherals external PNP | 2.5/2.6/2.75/3.0 | 350 |
| VGEN1 | General peripherals supply #1 | 1.2/1.25/1.3/1.35/1.4/1.45/1.5/1.55 | 250 |
| VGEN2 | General peripherals supply #2, internal PMOS | 2.5/2.7/2.8/2.9/3.0/3.1/3.15/3.3 | 50 |
| | General peripherals supply #2, external PNP | 2.5/2.7/2.8/2.9/3.0/3.1/3.15/3.3 | 250 |
| VUSB | USB Transceiver supply | 3.3 | 100 |

7.5.2 Modes of Operation

The 34709 PMIC is fully programmable via the SPI interface and associated register map. Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset. Default start-up of the device is selectable by hardwiring the Power-up Mode Select (PUMS) pins.

Power cycling of the application is driven by the 34709 PMIC. It also ensures uninterrupted supply of the Real Time Clock (RTC), critical internal logic, and other circuits from the coin cell, in case of brief interruptions from the main battery. A charger for the coin cell is included to ensure that it is kept charged until needed.

The 34709 PMIC provides the timekeeping based on an integrated low-power oscillator running with a standard watch crystal. This oscillator is used for the internal clocking and the control logic, as well as a reference for the switching PLL. The timekeeping is backed up by the coin cell and it includes time of day, calendar and alarm. The clock is driven to the processor for reference and deep sleep mode clocking.

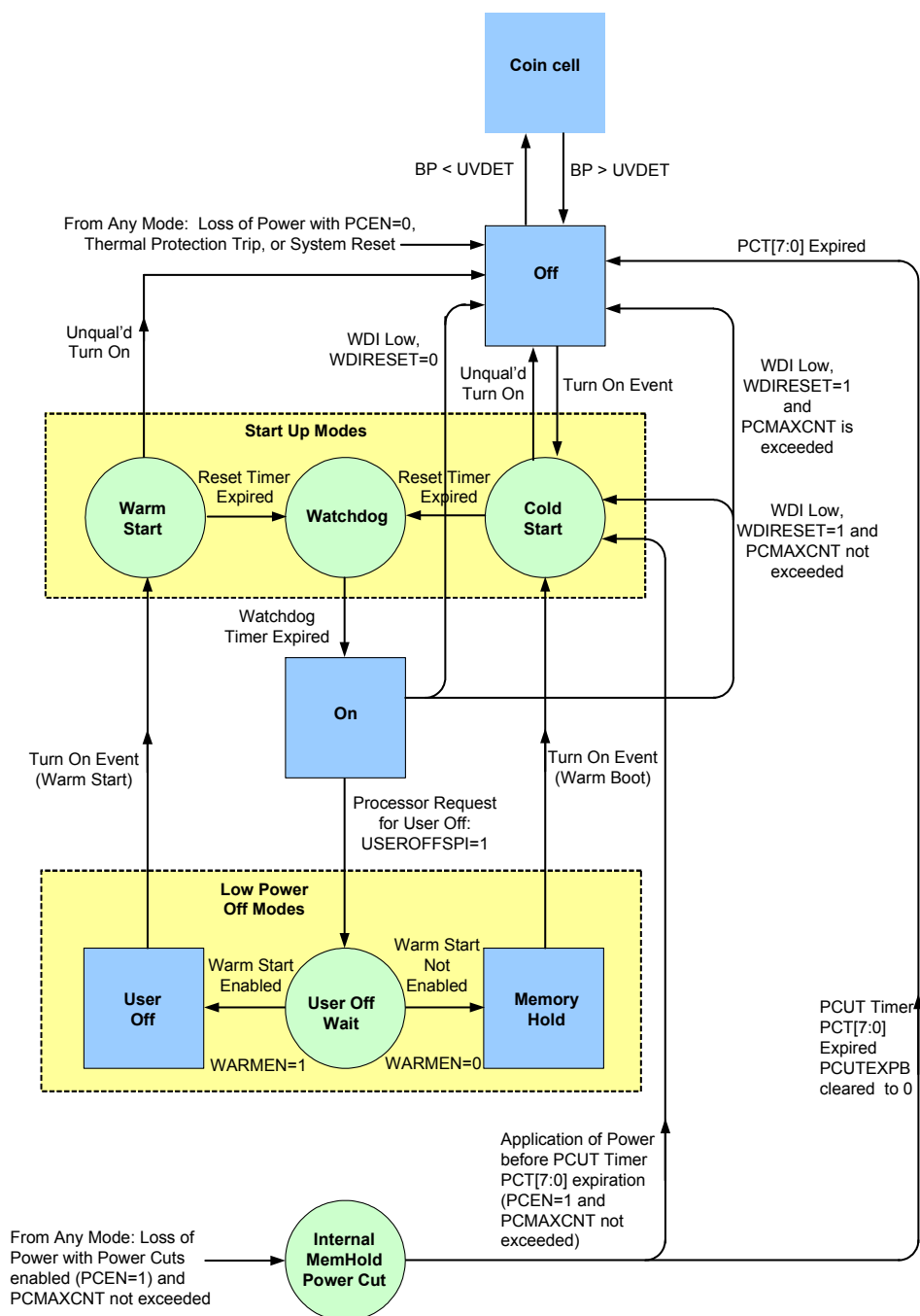


Figure 6. Power Control State Machine Flow Diagram

Figure 6 show the flow diagram of the power control state machine, and each state is described in detailed on the following sections. Note that the SPI control is only possible in the Watchdog, On and User Off Wait states, and that the interrupt line INT is kept low in all states except for Watchdog and On.

7.5.2.1 Coin Cell

The RTC module is powered from the coin cell due to insufficient voltage at BP and the PMIC not being in a Power Cut. In this state, no Turn On event is accepted and transitioning to the Off state would require BP restoration with a threshold above UVDET. RESETB, and RESETBMCU are held low in this mode.

The RTC module remains active (32 kHz oscillator + RTC timers), along with BP level detection to qualify exit to the Off state. VCOREDIG is off and the VDDL regulator is on, the rest of the system is put into its lowest power configuration.

If the coin cell is depleted (VSTRC drops below 0.9 V while in the Coin Cell state), a complete system reset will occur. At next Turn On event, the system will power-up reinitialized with all SPI bits, including those that reset on RTCPORB, restored to their default states.

7.5.2.2 Off (with good battery)

If BP is above the UVDET threshold, only the core circuitry at VCOREDIG and the RTC module are powered, all other supplies are inactive. To exit the Off mode, a valid turn on event is required. If BP is below the UVDET threshold, no turn on events are accepted. If a valid coin cell is present, the core gets powered from LICELL. The only active circuitry is the RTC module and the detection VCORE module powering VCOREDIG at 1.5 V.

No specific timer is running in this mode. RESETB and RESETBMCU are held low while in Off mode.

7.5.2.3 Cold Start

Cold Start is entered upon a Turn On event from Off, Warm Boot, successful PCUT, or a Silent System Restart. The first 8.0 ms are used for initialization, which includes bias generation, PUMSx configuration latching, and qualification of the BP supply level. The switching and linear regulators are then powered up sequentially to limit the inrush current; see [Start-up Requirements](#) section for sequencing and default level details. The reset signals RESETB and RESETBMCU are kept low. The Reset timer starts running when entering Cold Start. The Cold Start state exits to the Watchdog state and both RESETB and RESETBMCU become high (open-drain output with external pull-ups) when the reset timer is expired. The input control pins WDI, and STANDBY are ignored.

7.5.2.4 Watchdog

The system is fully powered and under SPI control. RESETB and RESETBMCU are high. The Watchdog timer starts running when entering the Watchdog state. When the watchdog timer is expired, the system transitions to the On state, where WDI will be checked and monitored. The input control pins WDI and STANDBY are ignored while in the Watchdog state.

7.5.2.5 On Mode

The system is fully powered and under SPI control. RESETB and RESETBMCU are high. The WDI pin must be high to stay in this mode. The WDI IO supply voltage is referenced to SPIVCC (normally connected to SW5 = 1.8 V); SPIVCC must therefore remain enabled to allow for proper WDI detection. If WDI goes low, the system will transition to the Off state or Cold Start depending on the configuration; refer to the section [Silent System Restart with WDI Event](#) for details.

7.5.2.6 User Off Wait

The system is fully powered and under SPI control. The WDI pin no longer has control over the part.

The Wait mode is entered by a processor request for user off by setting the USEROFFSPI bit high. This is normally initiated by the end user via the power key; upon receiving the corresponding interrupt, the system will determine if the product has been configured for User Off or Memory Hold states (both of which first require passing through User Off Wait) or just transition to the Off mode.

The Wait timer starts running when entering User Off Wait mode. This leaves the processor time to suspend or terminate its tasks. When expired, the Wait mode exits to User Off mode or Memory Hold mode depending on warm starts being enabled or not via the WARMEN bit. The USEROFFSPI bit is being reset at this point by RESETB going low.

7.5.2.7 Memory Hold and User Off (Low-power Off states)

As noted in the User Off Wait description, the system is directed into low-power Off states based on a SPI command in response to an intentional turn off by the end user, therefore the only way to exit this mode will be through a turn on event.

To the end user, the Memory Hold and User Off states look like the product has been shut down completely. However, a faster start-up is facilitated by maintaining external memory in self-refresh mode (Memory Hold and User Off mode) as well as powering portions of the processor core for state retention (User Off only). The switching regulator mode control bits allow selective powering of the buck regulators for optimizing the supply behavior in the low-power Off modes. Linear regulators and most functional blocks are disabled except for the RTC module, SPI bits resetting with RTCPORB, and Turn On event detection, which are maintained powered.

As an example, the following descriptions assume the typical use case where SW1 supplies the processor core(s), SW2 is applied to the processor's VCC domain, SW3 supplies the processors internal memory/peripherals, SW4 supplies the external memory, and SW5 supplies the I/O rail. The buck regulators are intended for direct connection to the aforementioned loads.

7.5.2.8 Memory Hold

RESETB and RESETBMCU are low, and both CLK32K and CLK32KMCU are disabled (CLK32KMCU active if DRM is set). To ensure that SW1, SW2, SW3, and SW5 shut off in Memory Hold, appropriate mode settings should be used such as SW1MHMODE, = SW2MHMODE, = SW3MHMODE, = SW5MHMODE set to = 0 (refer to [General Control](#) section). Since SW4 should be powered in PFM mode, SW4MHMODE could be set to 1.

Upon a Turn On event, the Cold Start state is entered, the default power-up values are loaded, and the MEMHLDI interrupt bit is set. A Cold Start out of the Memory Hold state will result in shorter boot times compared to starting out of the Off state, since software does not have to be loaded and expanded from flash. The start-up out of Memory Hold is also referred to as Warm Boot. No specific timer is running in this mode.

Buck regulators that are configured to stay on in MEMHOLD mode by their SWxMHMODE settings will not be turned off when coming out of MEMHOLD and entering a Warm Boot. The switching regulators will be reconfigured to their default settings in their corresponding time slot defined by the PUMSx pins.

7.5.2.9 User Off

RESETB is low and RESETBMCU is kept high. The 32 kHz peripheral clock driver CLK32K is disabled; CLK32KMCU (connected to the processor's CKIL input) is maintained in this mode if the CLK32KMCUEN and USEROFFCLK bits are both set, or if DRM is set.

The memory domain is held up by setting SW4UOMODE = 1. Similarly, the SW1 and/or SW2 and/or SW3 supply domains can be configured for SWxUOMODE=1 to keep them powered through the User Off event. If one of the switching regulators can be shut down on in User Off, its mode bits would typically be set to 0.

Since power is maintained for the core (which is put into its lowest power state), and since RESETBMCU does not trip, the processor's state may be quickly recovered when exiting USEROFF upon a turn on event. The CLK32KMCU clock can be used for very low frequency / low-power idling of the core(s), minimizing battery drain, while allowing a rapid recovery from where the system left off before the USEROFF command.

Upon a turn on event, Warm Start state is entered, and the default power-up values are loaded. A Warm Start out of User Off will result in an almost instantaneous start-up of the system, since the internal states of the processor were preserved along with external memory. No specific timer is running in this mode.

7.5.2.10 Warm Start

Entered upon a Turn On event from User Off. The first 8.0 ms is used for initialization, which includes bias generation, PUMSx latching, and qualification of the BP supply level. The switching and linear regulators are then powered up sequentially to limit the inrush current; see [Start-up Requirements](#) for sequencing and default level details. If SW1, SW2, SW3, SW4, and/or SW5, were configured to stay on in User Off mode by their SWxUOMODE settings, they will not be turned off when coming out of User Off and entering a Warm Start. The buck regulators will be reconfigured for their default settings as selected by the PUMSx pins in the respective time slot defined in the sequencer selection.

RESETB is kept low and RESETBMCU is kept high. CLK32KMCU is kept active if CLK32KMCU was set. The reset timer starts running when entering Warm Start. When expired, the Warm Start state exits to the Watchdog state, a WARMI interrupt is generated, and RESETB will go high.

7.5.2.11 Internal MemHold Power Cut

As described in the [Power Cut Description](#), a momentary power interruption will put the system into the Internal MemHold Power Cut state if PCUTs are enabled. The backup coin cell will now supply the 34709 core along with the 32 kHz crystal oscillator, the RTC system, and coin cell backed up registers. All regulators will be shut down to preserve the coin cell and RTC as long as possible.

Both RESETB and RESETBMCU are tripped, bringing the entire system down along with the supplies and external clock drivers, so the only recovery out of a Power Cut state is to reestablish power and initiate a Cold Start.

If the PCT timer expires before power is re-established, the system transitions to the Off state and awaits a sufficient supply recovery.

7.5.3 Power Control Logic

7.5.3.1 Power Cut Description

When the BP drops below the UVDET threshold, due to battery bounce or battery removal, the Internal MemHold Power Cut mode is entered and a Power Cut (PCUT) timer starts running. The backup coin cell will now supply the RTC as well as the on chip memory registers and some other power control related bits. All other supplies will be disabled.

The maximum duration of a power cut is determined by the PCUT timer PCT [7:0] preset via the SPI. When a PCUT occurs, the PCUT timer will be started. The contents of PCT [7:0] does not reflect the actual count down value, but will keep the programmed value, and therefore does not have to be reprogrammed after each power cut.

If power is not re-established above the 3.0 V threshold before the PCUT timer expires, the state machine transitions to the Off mode at expiration of the counter and it clears the PCUTEXB bit by setting it to 0. This transition is referred to as an “unsuccessful” PCUT. In addition, the PMIC will bring the SDWNB pin low for one 32 kHz clock cycle before powering down.

Upon re-application of power before expiration (a “successful PCUT”, defined as BP first rising above the UVDET threshold and then battery above the 3.0 V threshold before the PCUT timer expires), a Cold Start is engaged after the UVTIMER has expired.

In order to distinguish a non-PCUT initiated Cold Start from a Cold Start after a PCUT, the PCI interrupt should be checked by software. The PCI interrupt is cleared by software or when cycling through the Off state.

Because the PCUT system quickly disables the entire power tree, the battery voltage may recover to a level with the appearance of a valid supply once the battery is unloaded. However, upon a restart of the PMIC and power sequencer, the surge of current through the battery and trace impedances can once again cause the BP node to droop below UVDET. This chain of cyclic power down / power-up sequences is referred to as “ambulance mode”, and the power control system includes strategies to minimize the chance of a product falling into and getting stuck in ambulance mode.

First, the successful recovery out of a PCUT requires the BP node to rise above LOBATT threshold, providing hysteretic margin from the LOBATT (H to L) threshold. Secondly, the number of times the PCUT mode is entered is counted with the counter PCCOUNT [3:0], and the allowed count is limited to PCMAXCNT [3:0] set through the SPI. When the contents of both become equal, then the next PCUT will not be supported and the system will go to Off mode, after the PCUT time expires.

After a successful power-up from a PCUT (i.e., valid power is re-established, the system comes out of reset and the processor re-assumes control), software should clear the PCCOUNT [3:0] counter. Counting of PCUT events is enabled via the PCCOUNTEN bit. This mode is only supported if the power cut mode feature is enabled by setting the PCEN bit. When not enabled, then in case of a power failure, the state machine will transition to the Off mode. SPI control is not possible during a PCUT event and the interrupt line is kept low. SPI configuration for PCUT support should also include setting the PCUTEXPB = 1 (See [Silent Restart from PCUT Event](#)).

7.5.3.2 Silent Restart from PCUT Event

If a short duration power cut event occurs (such as from a battery bounce, for example), it may be desirable to perform a silent restart, so the system is reinitialized without alerting the user. This can be facilitated by setting the PCUTEXPB bit to “1” at booting or after a Cold Start. This bit resets on RTCPORB, therefore any subsequent Cold Start can first check the status of PCUTEXPB and the PCI bit. The PCUTEXPB is cleared to “0” when transitioning from PCUT to Off. If there was a PCUT interrupt and PCUTEXPB is still “1”, then the state machine has not transitioned through Off, which confirms that the PCT timer has not expired during the PCUT event (successful power cut). In this case, a silent restart may be appropriate.

If PCUTEXPB is found to be “0” after the Cold Start where PCI is found to be “1”, then it is inferred that the PCT timer has expired before power was re-established, flagging an unsuccessful power cut or first power-up, so the start-up user greeting may be desirable for playback.

7.5.3.3 Silent System Restart with WDI Event

A mechanism is provided for recovery if the system software somehow gets into an abnormal state which requires a system reset, but it is desired to make the reset a silent event so as to happen without end user awareness. The default response to WDI going low is for the state machine to transition to the Off mode (when WDIRESET = 0). However, if WDIRESET = 1, the state machine will go to Cold Start without passing through Off mode (i.e., does not generate an OFFB signal).

A WDIRESET event will generate a maskable WDIRESETI interrupt and also increment the PCCOUNT counter. This function is unrelated to PCUTs, but it shares the PCUT counter so that the number of silent system restarts can be limited by the programmable PCMAXCNT counter.

When PCUT support is used, the software should set the PCUTEXPB bit to “1”. Since this bit resets with RTCPORB, it will not be reset to “0” if a WDI falls and the state machine goes straight to the Cold Start state. Therefore, upon a restart, software can discern a silent system restart if there is a WDIRESETI interrupt and PCUTEXPB = 1. The application may then determine that an inconspicuous restart without fanfare may be more appropriate than launching into the welcoming routine.

A PCUT event does not trip the WDIRESETI bit.

Note that the system response to WDI is gated by the Watchdog timer—once the timer has expired, then the system will respond as programmed by WDIRESET and described above.

Applications should make sure there is time for switching regulator outputs to discharge before re-asserting WDI.

7.5.3.4 Turn On Events

When in Off mode, the circuit can be powered on via a Turn On event. To indicate to the processor what event caused the system to power on, an interrupt bit is associated with each of the Turn On events. Masking the interrupts related to the turn on events will not prevent the part to turn on, except for the time of day alarm. If the part was already on at the time of the turn on event, the interrupt is still generated. The possible Turn On events are:

- **Power Button Press:** PWRON1, or PWRON2 pulled low with corresponding interrupts and sense bits PWRON1I or PWRON2I, and PWRON1S or PWRON2S. A power on/off button is connected from PWRONx to ground. The PWRONx can be hardware debounced through a programmable debouncer PWRONxDBNC [1:0] to avoid a response upon a very short unintentional key press. BP should be above UVDET to allow a power-up. The PWRONxI interrupt is generated for both the falling and the rising edge of the PWRONx pin. By default, a 30 ms interrupt debounce is applied to both falling and rising edges. The falling edge debounce timing can be extended with PWRONxDBNC[1:0] as defined in the following table. The PWRONxI interrupt is cleared by software or when cycling through the Off mode.

Table 22. PWRONx Hardware Debounce Bit Settings⁽³⁸⁾

| Bits | State | Turn On Debounce (ms) | Falling Edge INT Debounce (ms) | Rising Edge INT Debounce (ms) |
|-----------------|-------|-----------------------|--------------------------------|-------------------------------|
| PWRONxDBNC[1:0] | 00 | 0.0 | 31.25 | 31.25 |
| | 01 | 31.25 | 31.25 | 31.25 |
| | 10 | 125 | 125 | 31.25 |
| | 11 | 750 | 750 | 31.25 |

Notes

38. The sense bit PWRONxS is not debounced and follows the state of the PWRONx pin.

- **Battery Attach:** This occurs when BP crosses the 3.0V threshold and the UVDET rising threshold which is equivalent to attaching a charged battery or supply to the product.
- **RTC Alarm:** TOD and DAY become equal to the alarm setting programmed. This allows powering up a product at a preset time. BP should be above 3.0V, and BP should have crossed the UVDET rising threshold and not transitioned below the UVDET falling threshold.
- **System Restart:** A system restart may occur after a system reset as described earlier in this section. This is an optional function, see [Turn Off Events](#). BP should be above 3.0 V and BP should have crossed the UVDET rising threshold and not transitioned below the UVDET falling threshold.
- **Global System Reset:** The global reset feature powers down the part, resets the SPI registers to their default value including all the RTCPORB registers (except the DRM bit, and the RTC registers), and then powers back on. To enable a global reset, the GLBRST pin needs to be pulled low for greater than GLBRSTTMR [1:0] seconds and then pulled back high (defaults to 12 s). BP should be above 3.0 V.

Table 23. Global Reset Time Settings

| Bits | State | Time (s) |
|----------------|--------------|----------|
| GLBRSTTMR[1:0] | 00 | Invalid |
| | 01 | 4.0 |
| | 10 | 8.0 |
| | 11 (default) | 12 |

7.5.3.5 Turn Off Events

- **Power Button Press (via WDI):** User shut down of a product is typically done by pressing the power button connected to the PWRONx pin. This will generate an interrupt (PWRONxI), but will not directly power off the part. The product is powered off by the processor's response to this interrupt, which will be to pull WDI low. Pressing the power button is therefore under normal circumstances not considered as a turn off event for the state machine. However, since the button press power down is the most common turn off method for end products, it is described in this section as the product implementation for a WDI initiated Turn Off event. Note that the software can configure an user initiated power down, via a power button press for transition to a Low-power Off mode (Memory Hold or User Off) for a quicker restart than the default transition into the Off state.
- **Power Button System Reset:** A secondary application of the PWRONx pins is the option to generate a system reset. This is recognized as a Turn Off event. By default, the system reset function is disabled but can be enabled by setting the PWRONxRSTEN bits. When enabled, a four second long press on the power button will cause the device to go to the Off mode, and as a result, the entire application will power down. An interrupt SYSRSTI is generated upon the next power-up. Alternatively, the system can be configured to restart automatically by setting the RESTARTEN bit.
- **Thermal Protection:** If the die gets overheated, the thermal protection will power off the part to avoid damage. A Turn On event will not be accepted while the thermal protection is still being tripped. The part will remain in Off mode until cooling sufficiently to accept a Turn On event. There are no specific interrupts related to this other than the warning interrupts.
- **Under-voltage Detection:** When the voltage at BP drops below the under-voltage detection threshold UVDET, the state machine will transition to Off mode if PCUT is not enabled or if the PCT timer expires when PCUT is enabled. The SDWNB pin is used to notify to the processor that the PMIC is going to immediately shut down. The PMIC will bring the SDWNB pin low for one 32 kHz clock cycle before powering down. This signal will then be brought back high in the power Off state.

7.5.3.6 Timers

The different timers as used by the state machine are listed on [Table 24](#); this listing does not include RTC timers for timekeeping. A synchronization error of up to one clock period may occur with respect to the occurrence of an asynchronous event, the duration listed on [Table 24](#) is therefore the effective minimum time period.

Table 24. Timer Main Characteristics

| Timer | Duration | Clock |
|---------------------|--|-----------|
| Under-voltage Timer | 4.0 ms | 32 k/32 |
| Reset Timer | 40 ms | 32 k/32 |
| Watchdog Timer | 128 ms | 32 k/32 |
| Power Cut Timer | Programmable 0 to 8 seconds in 31.25 ms steps | 32 k/1024 |

7.5.3.6.1 Timing Diagrams

A Turn On event timing diagrams shown in [Figure 7](#).

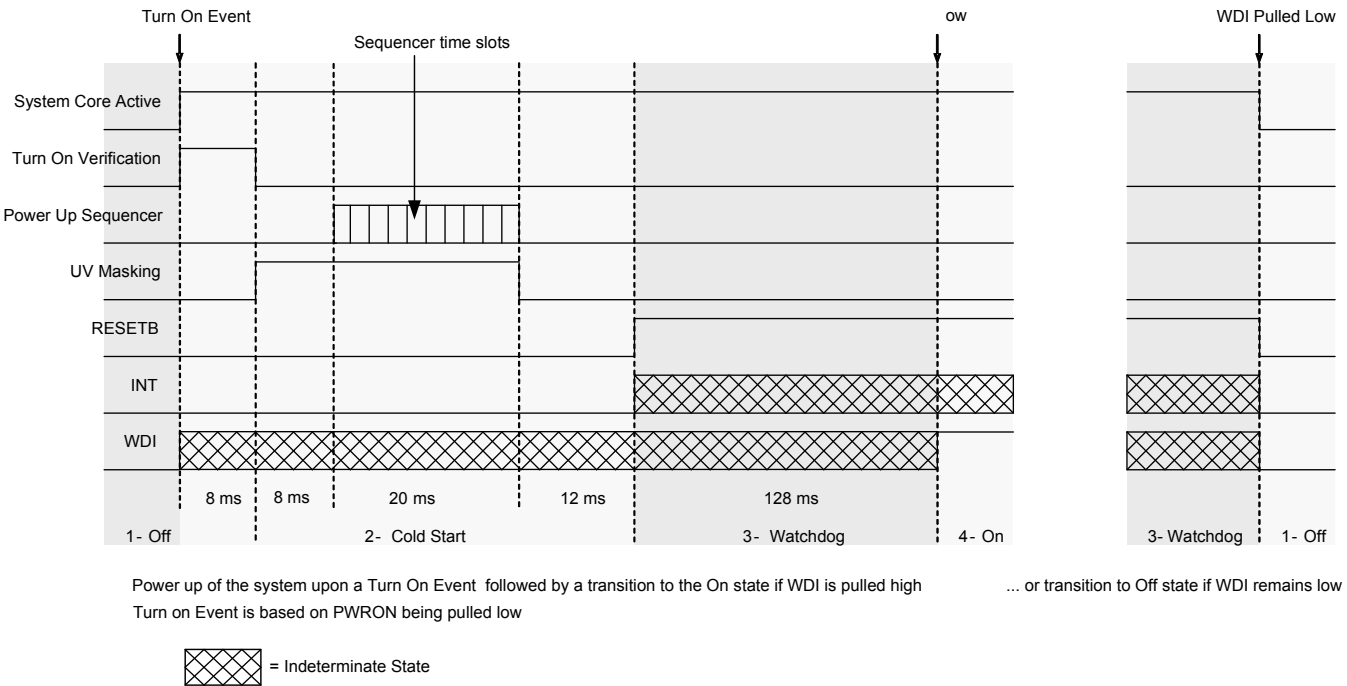


Figure 7. Power-up Timing Diagram

7.5.3.7 Power Monitoring

The voltage at BP is monitored by detectors as summarized in [Table 25](#).

Table 25. LOWBATT Detection Thresholds

| Threshold | Voltage (V) |
|---|-------------|
| Power on | 3.0 |
| Low input supply warning • BP (H to L) ⁽³⁹⁾ | 2.9 |
| UVDET rising ⁽⁴⁰⁾ | 3.0 |
| UVDET Falling ⁽⁴⁰⁾ | 2.65 |

Notes

39. 50 mV hysteresis is applied.

40. ± 4.0 % tolerance

The UVDET and Power on thresholds are related to the power on/off events as described earlier in this chapter. In order for the IC to power on, BP must rise above the UVDET rising threshold, and the power on threshold (3.0 V). When the BP node decreases below the 2.9 V threshold, a low input supply warning will be sent to the processor via the LOWBATTI interrupt.

The LOWBATTI detection threshold is debounced by the VBATTDB[2:0] SPI bits shown in [Table 26](#).

Table 26. VBATTDB Debounce Times

| VBATTDB[1:0] | Debounce Time (ms) |
|--------------|--------------------|
| 00 | 0.1 |
| 01 | 1.0 |
| 10 | 2.5 |
| 11 (default) | 3.9 |

7.5.3.8 Power Saving

7.5.3.8.1 System Standby

A product may be designed to enter in Deep Sleep Modes (DSM) after periods of inactivity, the STANDBY pin is provided for board level control of timing in and out of such deep sleep modes.

When a product is in DSM, it may be able to reduce the overall platform current by lowering the regulator output voltage, changing the operating mode of the switching regulators, or disabling some regulators. This can be obtained by controlling the STANDBY pin. The configuration of the regulators in standby is pre-programmed through the SPI.

With the ON_STBY_LP SPI bit set and the STANDBY pin asserted, a lower power standby will be entered. In the Standby Low-power mode, the switching regulators should be programmed into PFM mode, and the LDO's should be configured to operate in the Low-power mode when the STANDBY pin is asserted. The PLL is disabled in this mode

Note that the STANDBY pin is programmable for active high or active low polarity, and the decoding of a Standby event will take into account the programmed input polarity associated with each pin. For simplicity, Standby will generally be referred to as active high throughout this document, but as defined in [Table 27](#), active low operation can be programmed. Finally, since the STANDBY pin activity is driven asynchronously to the system, a finite time is required for the internal logic to qualify and respond to the pin level changes.

Table 27. Standby Pin and Polarity Control

| STANDBY (Pin) | STANDBYINV (SPI bit) | STANDBY Control ⁽⁴¹⁾ |
|---------------|----------------------|---------------------------------|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Notes

41. STANDBY = 0: System is not in Standby STANDBY = 1: System is in Standby

The state of the STANDBY pin only has influence in On mode, therefore it is ignored during start-up and in the Watchdog phase. This allows the system to power-up without concern of the required Standby polarities since software can make adjustments accordingly as soon as it is running.

A command to transition to one of the low-power Off states (User Off or Memory Hold, initiated with USEROFFSPI=1) redefines the power tree configuration based on SWxMODE programming, and has priority over Standby, which also influences the power tree configuration.

7.5.3.8.2 Standby Delay

A provision to delay the Standby response is included. This allows the processor and peripherals, some time after a Standby instruction has been received, to terminate processes to facilitate seamless Standby exiting and re-entrance into Normal operating mode.

A programmable delay is provided to hold off the system response to a Standby event. When enabled (STBYDLY[1:0] = 01, 10, or 11), it will delay the STANDBY initiated response for the entire PMIC until the STBYDLY counter expires.

The STBYDLY delay is applied only when going into Standby, and no delay is applied when coming out of Standby. Also, an allowance should be accounted for synchronization of the asynchronous Standby event and the internal clocking edges (up to a full 32 k cycle of additional delay).

Table 28. Delay of STANDBY- Initiated Response

| STBYDLY[1:0] | Function |
|--------------|---------------------------|
| 00 | No Delay |
| 01 | One 32 k period (default) |
| 10 | Two 32 k periods |
| 11 | Three 32 k periods |

7.5.4 Buck Switching Regulators

Six buck switching regulators are provided with integrated power switches and synchronous rectification. In a typical application, SW1 and SW2 are used for supplying the application processor core power domains. Split power domains allow independent DVS control for processor power optimization, or to support technologies with a mix of device types with different voltage ratings. SW3 is used for powering internal processor memory as well as low-voltage peripheral devices and interfaces which can run at the same voltage level. SW4A/B is used for powering external DDR memory as well as low-voltage peripheral devices and interfaces, which can run at the same voltage level. SW5 is used to supply the I/O domain for the system.

The buck regulators are supplied from the system supply BP, which is drawn from the main battery

The switching regulators can operate in different modes depending on the load conditions. These modes can be set through the SPI and include a PFM mode, an Automatic Pulse Skipping mode (APS), and a PWM mode.

Table 29. Buck Operating Modes

| Mode | Description |
|------|---|
| OFF | The regulator is switched off and the output voltage is discharged |
| PFM | Pulse Frequency Modulation: The regulator is switched on and set to PFM mode operation. In this mode, the regulator is always running in PFM mode. Useful at light loads for optimized efficiency. |
| APS | Automatic Pulse Skip: The regulator is switched on and set to Automatic Pulse Skipping. In this mode the regulator moves automatically between pulse skipping and full PWM mode depending on load conditions. |
| PWM | Pulse Width Modulation: The regulator is switched on and set to PWM mode. In this mode the regulator is always in full PWM mode operation regardless of load conditions. |

Buck modes of operation are programmable for explicitly defined or load-dependent control.

During soft-start of the buck regulators, the controller transitions through the PFM, APS, and PWM switching modes. 3.0 ms (typical) after the output voltage reaches regulation, the controller transitions to the selected switching mode. Depending on the particular switching mode selected, additional ripple may be observed on the output voltage rail as the controller transitions between switching modes. By default the regulators are turned on in APS mode. After the start-up sequence is complete, all switching regulators should be set to PFM/PWM mode depending on system load for best performance.

Point of Load feedback is intended for minimizing errors due to board level IR drops.

7.5.4.1 General Control

Operational modes of the Buck regulators can be controlled by direct SPI programming, altered by the state of the STANDBY pin, by direct state machine influence such as entering Off or low-power Off modes, or by load current magnitude when so configured (APS). Available modes include PWM, PFM, APS, and OFF. For light loads, the regulators should be put into PFM mode to optimize efficiency.

SW1A/B, SW2, SW3, SW4A/B, and SW5, can be configured for mode switching with STANDBY or autonomously, based on load current Auto pulse skip mode. Additionally, provisions are made for maintaining PFM operation in User off and Memhold modes, to support state retention for faster start-up from the Low-power Off modes for Warm Start or Warm Boot. SWxMODE[3:0] bits will be reset to their default values defined by PUMSx settings by the start-up sequencer.

[Table 30](#) summarizes the Buck regulators programmability for Normal and Standby modes.

Table 30. Switching regulator Mode Control for Normal and Standby Operation

| SWxMODE[3:0] | Normal Mode | Standby Mode |
|--------------|-------------|--------------|
| 0000 | Off | Off |
| 0001 | PWM | Off |
| 0010 | Reserved | Reserved |
| 0011 | PFM | Off |
| 0100 | APS | Off |
| 0101 | PWM | PWM |
| 0110 | PWM | APS |
| 0111 | Off | Off |
| 1000 | APS | APS |
| 1001 | Reserved | Reserved |
| 1010 | Reserved | Reserved |
| 1011 | Reserved | Reserved |
| 1100 | APS | PFM |

Table 30. Switching regulator Mode Control for Normal and Standby Operation

| SWxMODE[3:0] | Normal Mode | Standby Mode |
|--------------|-------------|--------------|
| 1101 | PWM | PFM |
| 1110 | Reserved | Reserved |
| 1111 | PFM | PFM |

In addition to controlling the operating mode in Standby, the voltage setting can be changed. The voltage transition slope is controlled by DVS, see [Dynamic Voltage Scaling](#) section for details. Each regulator has an associated set of SPI bits for Standby mode set points. By default, the Standby settings are identical to the non-standby settings which are initially defined by PUMSx programming.

The actual operating mode of the Switching regulators as a function of the STANDBY pin is not reflected through the SPI. In other words, the SPI will read what is programmed in SWxMODE[3:0], not the actual state that may be altered as described previously.

[Table 31](#) and [Table 32](#) provide the mode control in the low-power Off states. Note that a low-power Off activated SWx should use the Standby set point as programmed by SWxSTBY[4:0]. The activated regulator(s) will maintain settings for mode and voltage until the next start-up event. When the respective time slot of the start-up sequencer is reached for a given regulator, its mode and voltage settings will be updated the same as if starting in the Off state. The exception is switching regulators that are active through a low-power Off mode will remain on when the start-up sequencer is started.

Table 31. Switching regulator Control In Memory Hold

| SWxMHMODE | Memory Hold Operational Mode ⁽⁴²⁾ |
|-----------|--|
| 0 | Off |
| 1 | PFM |

Notes:

42. For Memory Hold mode, an activated SWx should use the Standby set point as programmed by SWxSTBY[4:0].

Table 32. Switching regulator Control In User Off

| SWxUOMODE | User Off Operational Mode ⁽⁴³⁾ |
|-----------|---|
| 0 | Off |
| 1 | PFM |

Notes:

43. For User Off mode, an activated SWx should use the Standby set point as programmed by SWxSTBY[4:0].

In normal steady state operating mode, the SWxPWGD pin is pulled high. During DVS the SWxPWGD is asserted low.

7.5.4.2 Switching Frequency

A PLL generates the switching system clocking from the 32.768 kHz crystal oscillator reference. The switching frequency can be programmed to 2.0 MHz or 4.0 MHz by setting the PLLX SPI bit as shown in [Table 33](#).

Table 33. Buck Regulator Frequency

| PLLX | Switching Frequency (Hz) |
|------|--------------------------|
| 0 | 2 000 000 |
| 1 | 4 000 000 |

The clocking system provides a near instantaneous activation when the switching regulators are enabled or when exiting PFM operation to PWM mode. The PLL can be configured for continuous operation with PLLEN = 1.

7.5.4.3 SW1

SW1 is a fully integrated synchronous buck PWM voltage mode controlled DC/DC regulator. It can be operated in single phase/dual phase mode. The operating mode of the switching regulator is configured by the SW1CFG pin. The SW1CFG pin is sampled at start-up.

Table 34. SW1 Configuration

| | |
|---------------|----------------------------------|
| SW1CFG | SW1A/B Configuration Mode |
| VCOREDIG | Single Phase Mode |
| Ground | Dual Phase Mode |

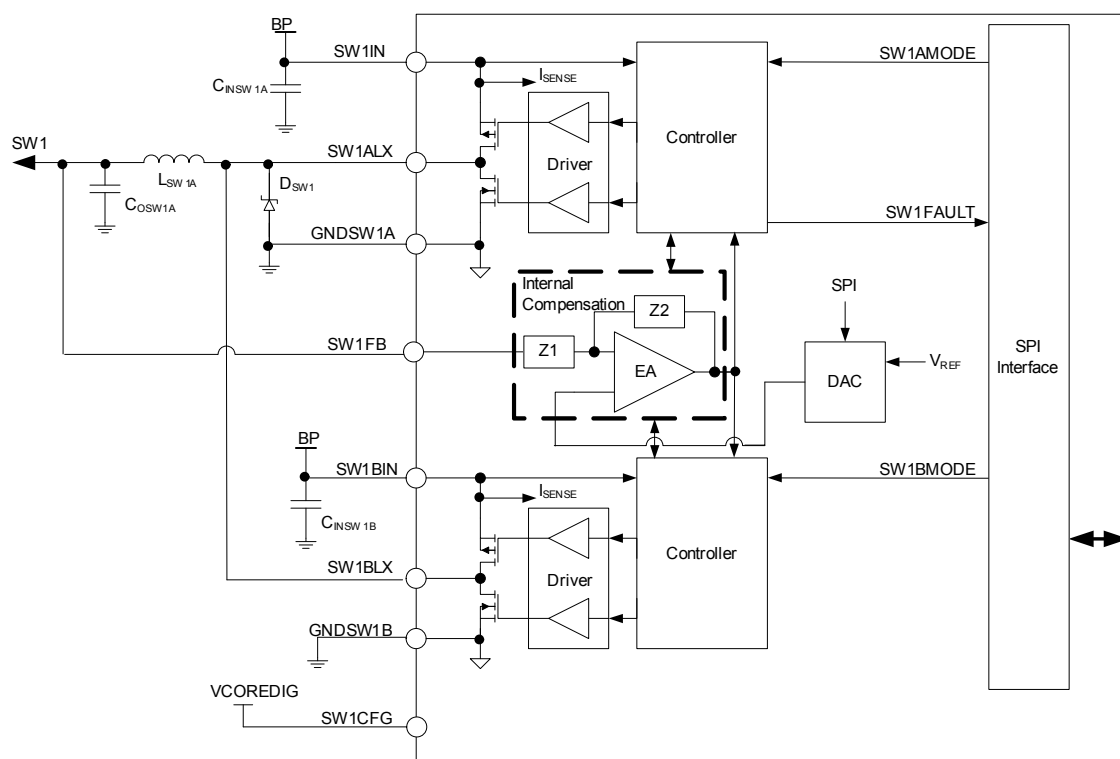


Figure 8. SW1 Single Phase Output Mode Block Diagram

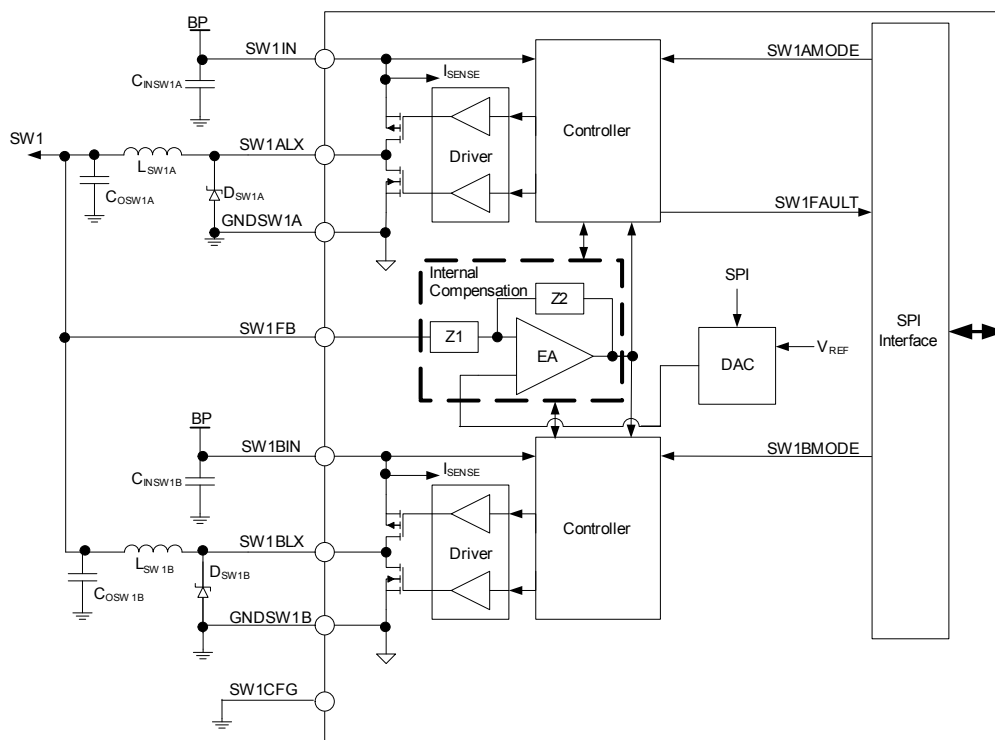


Figure 9. SW1 Dual Phase Output Mode Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected the regulator will limit the current through cycle by cycle operation and alert the system through the SW1FAULT SPI bit and issue an SCPI interrupt via the INT pin.

SW1A/B output voltage is SPI configurable in step sizes of 12.5 mV as shown in the table below. The SPI bits SW1A[5:0] set the output voltage for both the SW1A and SW1B.

Table 35. SW1A/B Output Voltage Programmability

| Set Point | SW1A[5:0] | SW1A/B Output (V) | Set Point | SW1A[5:0] | SW1A/B Output (V) |
|-----------|-----------|-------------------|-----------|-----------|-------------------|
| 0 | 000000 | 0.6500 | 32 | 100000 | 1.0500 |
| 1 | 000001 | 0.6625 | 33 | 100001 | 1.0625 |
| 2 | 000010 | 0.6750 | 34 | 100010 | 1.0750 |
| 3 | 000011 | 0.6875 | 35 | 100011 | 1.0875 |
| 4 | 000100 | 0.7000 | 36 | 100100 | 1.1000 |
| 5 | 000101 | 0.7125 | 37 | 100101 | 1.1125 |
| 6 | 000110 | 0.7250 | 38 | 100110 | 1.1250 |
| 7 | 000111 | 0.7375 | 39 | 100111 | 1.1375 |
| 8 | 001000 | 0.7500 | 40 | 101000 | 1.1500 |
| 9 | 001001 | 0.7625 | 41 | 101001 | 1.1625 |
| 10 | 001010 | 0.7750 | 42 | 101010 | 1.1750 |
| 11 | 001011 | 0.7875 | 43 | 101011 | 1.1875 |
| 12 | 001100 | 0.8000 | 44 | 101100 | 1.2000 |

Table 35. SW1A/B Output Voltage Programmability

| Set Point | SW1A[5:0] | SW1A/B Output (V) | Set Point | SW1A[5:0] | SW1A/B Output (V) |
|-----------|-----------|-------------------|-----------|-----------|-------------------|
| 13 | 001101 | 0.8125 | 45 | 101101 | 1.2125 |
| 14 | 001110 | 0.8250 | 46 | 101110 | 1.2250 |
| 15 | 001111 | 0.8375 | 47 | 101111 | 1.2375 |
| 16 | 010000 | 0.8500 | 48 | 110000 | 1.2500 |
| 17 | 010001 | 0.8625 | 49 | 110001 | 1.2625 |
| 18 | 010010 | 0.8750 | 50 | 110010 | 1.2750 |
| 19 | 010011 | 0.8875 | 51 | 110011 | 1.2875 |
| 20 | 010100 | 0.9000 | 52 | 110100 | 1.3000 |
| 21 | 010101 | 0.9125 | 53 | 110101 | 1.3125 |
| 22 | 010110 | 0.9250 | 54 | 110110 | 1.3250 |
| 23 | 010111 | 0.9375 | 55 | 110111 | 1.3375 |
| 24 | 011000 | 0.9500 | 56 | 111000 | 1.3500 |
| 25 | 011001 | 0.9625 | 57 | 111001 | 1.3625 |
| 26 | 011010 | 0.9750 | 58 | 111010 | 1.3750 |
| 27 | 011011 | 0.9875 | 59 | 111011 | 1.3875 |
| 28 | 011100 | 1.0000 | 60 | 111100 | 1.4000 |
| 29 | 011101 | 1.0125 | 61 | 111101 | 1.4125 |
| 30 | 011110 | 1.0250 | 62 | 111110 | 1.4250 |
| 31 | 011111 | 1.0375 | 63 | 111111 | 1.4375 |

Table 36. SW1A/B Electrical Specification

Characteristics noted under conditions BP = $V_{SW1XIN} = 3.6\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = $V_{SW1XIN} = 3.6\text{ V}$ and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------|----------------|-----|-----|-----|------|-------|
|--------|----------------|-----|-----|-----|------|-------|

SW1A/B BUCK REGULATOR

| | | | | | | |
|-------------------|--|------------------|------------|------------------|----|------|
| V_{SW1IN} | Operating Input Voltage <ul style="list-style-type: none"> PWM operation, $0\text{ mA} < I_L < I_{MAX}$ PFM operation, $0\text{ mA} < I_L < I_{LMAX}$ | 3.0 2.8 | - - | 4.5 4.5 | V | |
| V_{SW1ACC} | Output Voltage Accuracy <ul style="list-style-type: none"> PWM mode including ripple, load regulation, and transients PFM Mode, including ripple, load regulation, and transients | Nom-25 Nom-25 | Nom Nom | Nom+25 Nom+25 | mV | (44) |
| I_{SW1} | Continuous Output Load Current, $V_{INMIN} < BP < 4.5\text{ V}$ <ul style="list-style-type: none"> PWM mode single/dual phase (parallel) SW1 in PFM mode | - - | - 50 | 2000 - | mA | |
| $I_{SW1PEAK}$ | Current Limiter Peak Current Detection <ul style="list-style-type: none"> $V_{SW1XIN} = 3.6\text{ V}$, Current through Inductor | - | 4.0 | - | A | |
| $V_{SW1OS-START}$ | Start-up Overshoot <ul style="list-style-type: none"> $I_L = 0\text{ mA}$ | - | | 25 | mV | |

Table 36. SW1A/B Electrical Specification

Characteristics noted under conditions $BP = V_{SW1xIN} = 3.6 \text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise noted. Typical values at $BP = V_{SW1xIN} = 3.6 \text{ V}$ and $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--|--|------------------|----------------------|------------------|---------------|-------|
| SW1A/B BUCK REGULATOR (CONTINUED) | | | | | | |
| t_{ON-SW1} | Turn-on Time • Enable to 90% of end value $IL = 0 \text{ mA}$ | - | - | 500 | μs | |
| f_{SW1} | Switching Frequency • PLLX = 0 • PLLX = 1 | - - | 2.0 4.0 | - - | MHz | |
| I_{SW1Q} | Quiescent Current Consumption • APS Mode, $IL=0 \text{ mA}$; device not switching • PFM Mode, $IL=0 \text{ mA}$ | - - | 160 15 | - - | μA | |
| η_{SW1} | Efficiency, • PFM, 0.9 V, 1.0 mA • PWM, 1.1 V, 200 mA • PWM, 1.1 V, 800 mA • PWM, 1.1 V, 1600 mA | - - - - | 54 75 81 76 | - - - - | % | (45) |

Notes:

44. Transient loading for load steps of $IL_{MAX}/2$ at $100 \text{ mA}/\mu\text{s}$.
45. Efficiency numbers at $V_{SW1xIN} = 3.6 \text{ V}$, excludes the quiescent current

7.5.4.4 SW2

SW2 is a fully integrated synchronous buck PWM voltage mode controlled DC/DC regulator.

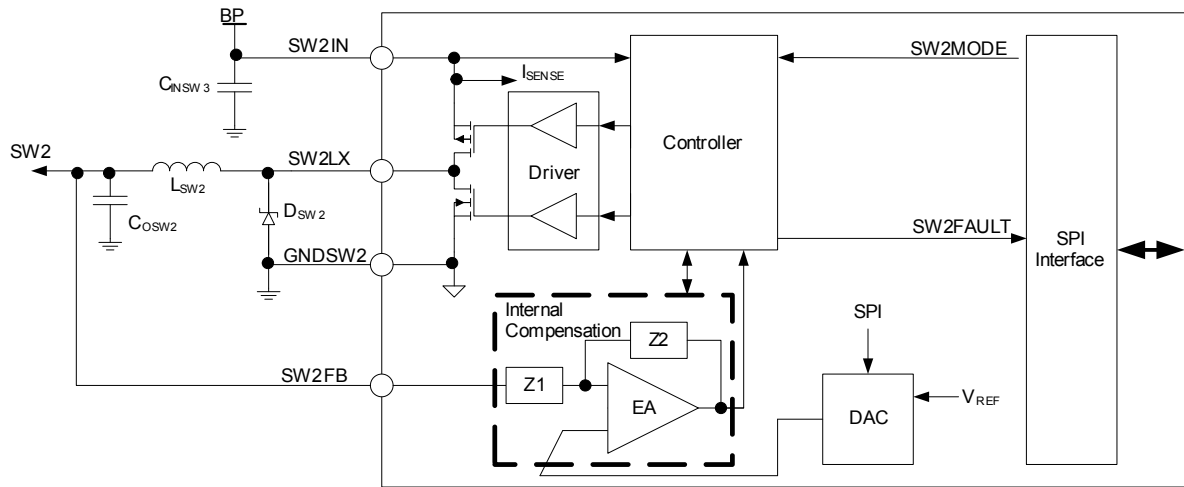


Figure 10. SW2 Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation, alert the system through the SW2FAULT SPI bit, and issue an SCPI interrupt via the INT pin.

SW2 can be programmed in step sizes of 12.5 mV as shown in [Table 37](#).

Table 37. SW2 Output Voltage Programmability

| Set Point | SW2[5:0] | SW2x Output (V) | Set Point | SW2[5:0] | SW2 Output (V) |
|-----------|----------|-----------------|-----------|----------|----------------|
| 0 | 000000 | 0.6500 | 32 | 100000 | 1.0500 |
| 1 | 000001 | 0.6625 | 33 | 100001 | 1.0625 |
| 2 | 000010 | 0.6750 | 34 | 100010 | 1.0750 |
| 3 | 000011 | 0.6875 | 35 | 100011 | 1.0875 |
| 4 | 000100 | 0.7000 | 36 | 100100 | 1.1000 |
| 5 | 000101 | 0.7125 | 37 | 100101 | 1.1125 |
| 6 | 000110 | 0.7250 | 38 | 100110 | 1.1250 |
| 7 | 000111 | 0.7375 | 39 | 100111 | 1.1375 |
| 8 | 001000 | 0.7500 | 40 | 101000 | 1.1500 |
| 9 | 001001 | 0.7625 | 41 | 101001 | 1.1625 |
| 10 | 001010 | 0.7750 | 42 | 101010 | 1.1750 |
| 11 | 001011 | 0.7875 | 43 | 101011 | 1.1875 |
| 12 | 001100 | 0.8000 | 44 | 101100 | 1.2000 |
| 13 | 001101 | 0.8125 | 45 | 101101 | 1.2125 |
| 14 | 001110 | 0.8250 | 46 | 101110 | 1.2250 |
| 15 | 001111 | 0.8375 | 47 | 101111 | 1.2375 |
| 16 | 010000 | 0.8500 | 48 | 110000 | 1.2500 |

Table 37. SW2 Output Voltage Programmability

| Set Point | SW2[5:0] | SW2x Output (V) | Set Point | SW2[5:0] | SW2 Output (V) |
|-----------|----------|-----------------|-----------|----------|----------------|
| 17 | 010001 | 0.8625 | 49 | 110001 | 1.2625 |
| 18 | 010010 | 0.8750 | 50 | 110010 | 1.2750 |
| 19 | 010011 | 0.8875 | 51 | 110011 | 1.2875 |
| 20 | 010100 | 0.9000 | 52 | 110100 | 1.3000 |
| 21 | 010101 | 0.9125 | 53 | 110101 | 1.3125 |
| 22 | 010110 | 0.9250 | 54 | 110110 | 1.3250 |
| 23 | 010111 | 0.9375 | 55 | 110111 | 1.3375 |
| 24 | 011000 | 0.9500 | 56 | 111000 | 1.3500 |
| 25 | 011001 | 0.9625 | 57 | 111001 | 1.3625 |
| 26 | 011010 | 0.9750 | 58 | 111010 | 1.3750 |
| 27 | 011011 | 0.9875 | 59 | 111011 | 1.3875 |
| 28 | 011100 | 1.0000 | 60 | 111100 | 1.4000 |
| 29 | 011101 | 1.0125 | 61 | 111101 | 1.4125 |
| 30 | 011110 | 1.0250 | 62 | 111110 | 1.4250 |
| 31 | 011111 | 1.0375 | 63 | 111111 | 1.4375 |

Table 38. SW2 Electrical Specifications

Characteristics noted under conditions $BP = V_{SW2IN} = 3.6 \text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise noted. Typical values at $BP = V_{SW2IN} = 3.6 \text{ V}$ and $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---------------------------|---|------------------|------------|------------------|---------------|-------|
| SW2 BUCK REGULATOR | | | | | | |
| V_{SW2IN} | Operating Input Voltage <ul style="list-style-type: none"> PWM operation, $0 \text{ mA} < I_L < I_{MAX}$ PFM operation, $0 \text{ mA} < I_L < I_{LMAX}$ | 3.0 2.8 | - - | 4.5 4.5 | V | |
| V_{SW2ACC} | Output Voltage Accuracy <ul style="list-style-type: none"> PWM mode including ripple, load regulation, and transients PFM Mode, including ripple, load regulation, and transients | Nom-25 Nom-25 | Nom Nom | Nom+25 Nom+25 | mV | (46) |
| I_{SW2} | Continuous Output Load Current, $V_{INMIN} < BP < 4.5 \text{ V}$ <ul style="list-style-type: none"> PWM mode PFM mode | - - | - 50 | 1000 - | mA | |
| $I_{SW2PEAK}$ | Current Limiter Peak Current Detection <ul style="list-style-type: none"> $V_{SW2IN} = 3.6 \text{ V}$ Current through Inductor | - | 2.0 | - | A | |
| $V_{SW2OS-START}$ | Start-up Overshoot <ul style="list-style-type: none"> $I_L = 0 \text{ mA}$ | - | - | 25 | mV | |
| t_{ON-SW2} | Turn-on Time <ul style="list-style-type: none"> Enable to 90% of end value $I_L = 0 \text{ mA}$ | - | - | 500 | μs | |
| f_{SW2} | Switching Frequency <ul style="list-style-type: none"> PLLX = 0 PLLX = 1 | - - | 2.0 4.0 | - - | MHz | |

Table 38. SW2 Electrical Specifications

Characteristics noted under conditions BP = V_{SW2IN} = 3.6 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = V_{SW2IN} = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---------------------------------------|--|-----|-----|-----|------|-------|
| SW2 BUCK REGULATOR (CONTINUED) | | | | | | |
| I _{SW2Q} | Quiescent Current Consumption <ul style="list-style-type: none"> • APS Mode, IL=0 mA; device not switching • PFM Mode, IL = 0 mA; device not switching | - | 160 | - | μA | |
| η _{SW2} | Efficiency <ul style="list-style-type: none"> • PFM, 0.9 V, 1.0 mA • PWM, 1.2 V, 120 mA • PWM, 1.2 V, 500 mA • PWM, 1.2 V, 1000 mA | - | 54 | - | % | (47) |
| | | - | 75 | - | | |
| | | - | 83 | - | | |
| | | - | 78 | - | | |

Notes:

- 46. Transient loading for load steps of ILMAX/2 at 100 mA/μs.
- 47. Efficiency numbers at V_{SW2IN} = 3.6 V, excludes the quiescent current.

7.5.4.5 SW3

SW3 is a fully integrated synchronous buck PWM voltage mode controlled DC/DC regulator.

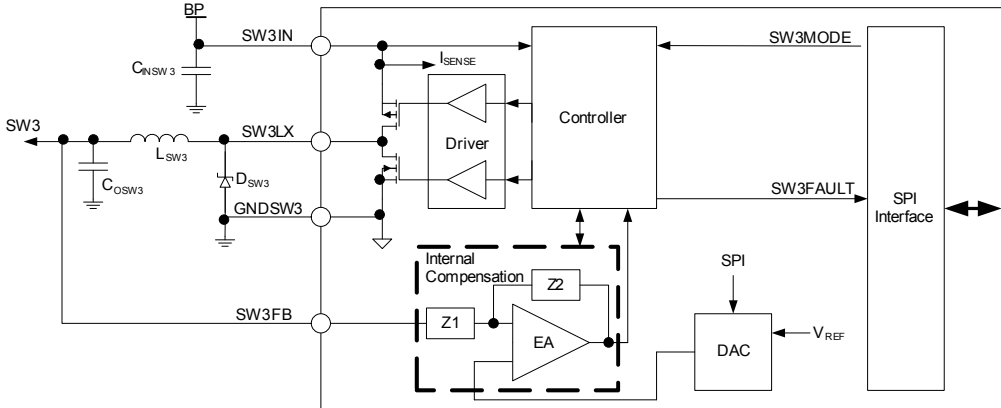


Figure 11. SW3 Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected the regulator will limit the current through cycle by cycle operation and alert the system through the SW3FAULT SPI bit and issue an SCPI interrupt via the INT pin.

SW3 can be programmed in step sizes of 25 mV as shown in [Table 39](#).

Table 39. SW3 Output Voltage Programmability

| Set Point | SW3[4:0] | SW3 Output (V) | Set Point | SW3[4:0] | SW3 Output (V) |
|-----------|----------|----------------|-----------|----------|----------------|
| 0 | 00000 | 0.650 | 16 | 10000 | 1.050 |
| 1 | 00001 | 0.675 | 17 | 10001 | 1.075 |
| 2 | 00010 | 0.700 | 18 | 10010 | 1.100 |
| 3 | 00011 | 0.725 | 19 | 10011 | 1.125 |
| 4 | 00100 | 0.750 | 20 | 10100 | 1.150 |
| 5 | 00101 | 0.775 | 21 | 10101 | 1.175 |
| 6 | 00110 | 0.800 | 22 | 10110 | 1.200 |
| 7 | 00111 | 0.825 | 23 | 10111 | 1.225 |
| 8 | 01000 | 0.850 | 24 | 11000 | 1.250 |
| 9 | 01001 | 0.875 | 25 | 11001 | 1.275 |
| 10 | 01010 | 0.900 | 26 | 11010 | 1.300 |
| 11 | 01011 | 0.925 | 27 | 11011 | 1.325 |
| 12 | 01100 | 0.950 | 28 | 11100 | 1.350 |
| 13 | 01101 | 0.975 | 29 | 11101 | 1.375 |
| 14 | 01110 | 1.000 | 30 | 11110 | 1.400 |
| 15 | 01111 | 1.025 | 31 | 11111 | 1.425 |

Table 40. SW3 Electrical Specification

Characteristics noted under conditions BP = $V_{SW3IN} = 3.6\text{ V}$, $-40\text{ °C} \leq T_A \leq 85\text{ °C}$, unless otherwise noted. Typical values at BP = $V_{SW3IN} = 3.6\text{ V}$ and $T_A = 25\text{ °C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------|----------------|-----|-----|-----|------|-------|
|--------|----------------|-----|-----|-----|------|-------|

SW3 BUCK REGULATOR

| | | | | | | |
|-------------------|---|------------------|------------|------------------|---------------|------|
| V_{SW3IN} | Operating Input Voltage <ul style="list-style-type: none"> PWM operation, $0\text{ mA} < I_L < I_{MAX}$ PFM operation, $0\text{ mA} < I_L < I_{LMAX}$ | 3.0 2.8 | - - | 4.5 4.5 | V | |
| V_{SW3ACC} | Output Voltage Accuracy <ul style="list-style-type: none"> PWM mode including ripple, load regulation, and transients PFM Mode, including ripple, load regulation, and transients | Nom-3% Nom-3% | Nom Nom | Nom+3% Nom+3% | mV | (48) |
| I_{SW3} | Continuous Output Load Current, $V_{INMIN} < BP < 4.5\text{ V}$ <ul style="list-style-type: none"> PWM mode PFM mode | - - | - 50 | 500 - | mA | |
| $I_{SW3PEAK}$ | Current Limiter Peak Current Detection <ul style="list-style-type: none"> $V_{SW3IN} = 3.6\text{ V}$ Current through Inductor | - | 1.0 | - | A | |
| $V_{SW3OS-START}$ | Start-up Overshoot <ul style="list-style-type: none"> $I_L = 0\text{ mA}$ | - | - | 25 | mV | |
| t_{ON-SW3} | Turn-on Time <ul style="list-style-type: none"> Enable to 90% of end value $I_L = 0\text{ mA}$ | - | - | 500 | μs | |

Table 40. SW3 Electrical Specification

Characteristics noted under conditions $BP = V_{SW3IN} = 3.6\text{ V}$, $-40\text{ °C} \leq T_A \leq 85\text{ °C}$, unless otherwise noted. Typical values at $BP = V_{SW3IN} = 3.6\text{ V}$ and $T_A = 25\text{ °C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---------------------------------------|--|------------------|----------------------|------------------|---------------|-------|
| SW3 BUCK REGULATOR (CONTINUED) | | | | | | |
| f_{SW3} | Switching Frequency <ul style="list-style-type: none"> • PLLX = 0 • PLLX = 1 | - - | 2.0 4.0 | - - | MHz | |
| I_{SW3Q} | Quiescent Current Consumption <ul style="list-style-type: none"> • APS Mode, $I_L=0\text{ mA}$; device not switching • PFM Mode, $I_L = 0\text{ mA}$; device not switching | - - | 160 15 | - - | μA | |
| η_{SW3} | Efficiency <ul style="list-style-type: none"> • PFM, 1.2 V, 1.0 mA • PWM, 1.2 V, 120 mA • PWM, 1.2 V, 250 mA • PWM, 1.2 V, 500 mA | - - - - | 71 79 82 81 | - - - - | % | (49) |

Notes:

48. Transient loading for load steps of $I_{LMAX}/2$ at $100\text{ mA}/\mu\text{s}$.
49. Efficiency numbers at $V_{SW3IN}=3.6\text{ V}$, Excludes the quiescent current,

7.5.4.6 SW4

SW4A/B is a fully integrated synchronous buck PWM voltage mode controlled DC/DC regulator. It can be operated in single/dual phase mode or as independent outputs. The operating mode of the switching regulator is configured by the SW4CFG pin. The SW4CFG pin is sampled at start-up.

Table 41. SW4A/B Configuration

| SW4CFG | SW4A/B Configuration Mode |
|----------|---------------------------|
| Ground | Independent output |
| VCOREDIG | Single phase |
| VCORE | Dual phase |

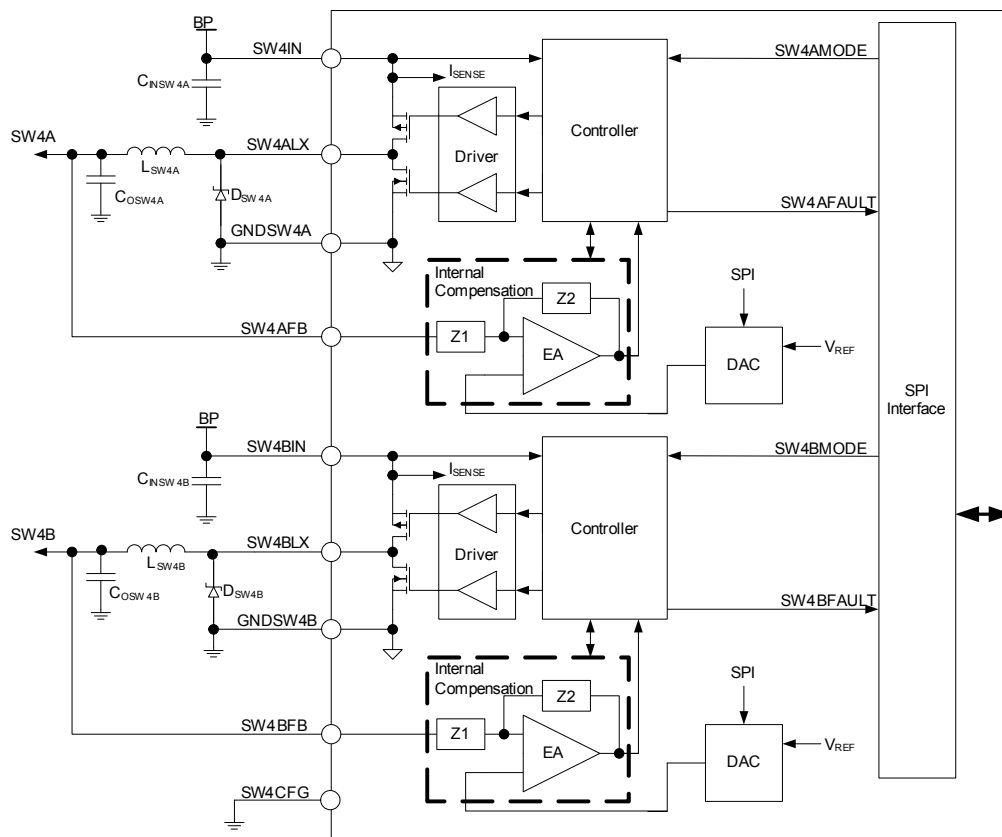


Figure 12. SW4A/B Independent Output Mode Block Diagram



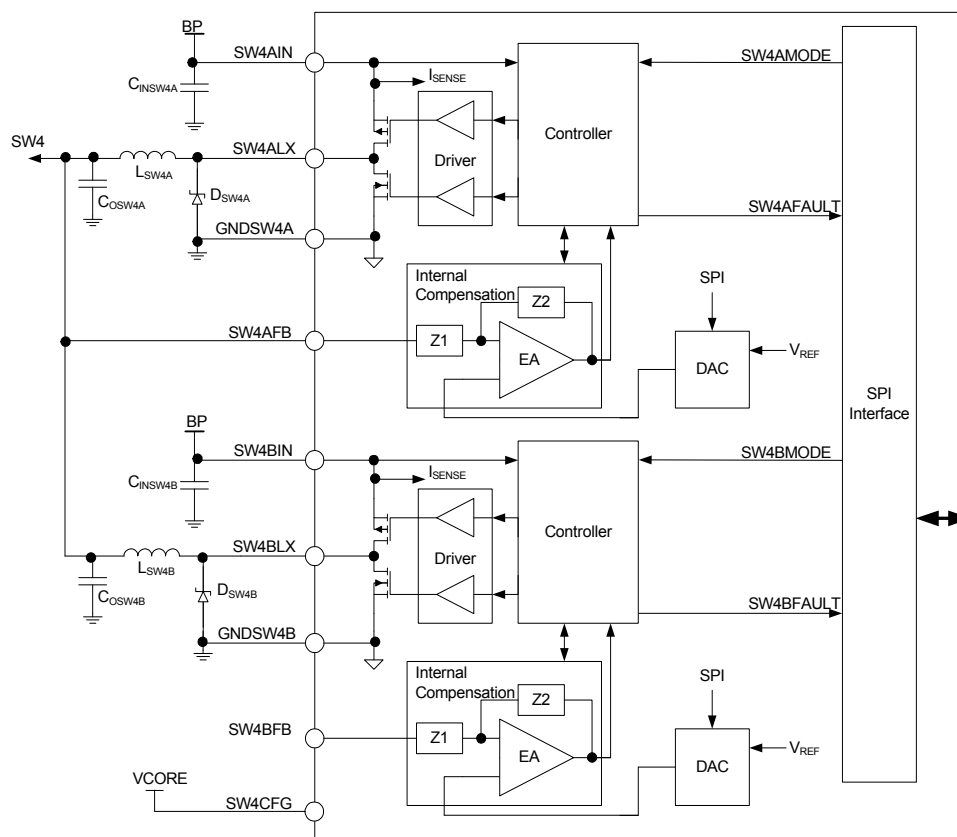


Figure 14. SW4 Dual Phase Output Mode Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected, the regulator will limit the current through cycle by cycle operation, alert the system through the SW4xFAULT SPI bit, and issue an SCPI interrupt via the INT pin.

SW4A/B has a high output range (2.5 V or 3.15 V) and a low output range (1.2 V to 1.85 V). The SW4A/B output range is set by the PUMS configuration at startup and cannot be changed dynamically by software. This means that if the PUMS are set to allow SW4A to come up in the high output voltage range, the output can only be changed between 2.5 V or 3.15 V and cannot be programmed in the low output range. If software sets the SW4AH[1:0] = 00, when the PUMS is set to come up into the high voltage range, the output voltage will only go as low as the lowest setting in the high range which is 2.5 V. If the PUMS are set to start up in the low output voltage range, the voltage is controlled through the SW4x[4:0] bits by software and cannot be programmed into the high voltage range. When changing the voltage within either the high or low voltage range, the switching regulator should be forced into PWM mode to change the voltage.

Table 42. SW4A/B Output Voltage Select

| SW4xHI[1:0] | Set point selected by | Output Voltage (V) |
|-------------|-----------------------|------------------------------|
| 00 | SW4x[4:0] | See Table 43 |
| 01 | SW4xHI[1:0] | 2.5 |
| 10 | SW4xHI[1:0] | 3.15 |

Table 43. SW4A/B Output Voltage Programmability

| Set Point | SW4x[4:0] | SW4x Output (V) | Set Point | SW4x[4:0] | SW4x Output (V) |
|-----------|-----------|-----------------|-----------|-----------|-----------------|
| 0 | 00000 | 1.200 | 16 | 10000 | 1.600 |
| 1 | 00001 | 1.225 | 17 | 10001 | 1.625 |
| 2 | 00010 | 1.250 | 18 | 10010 | 1.650 |
| 3 | 00011 | 1.275 | 19 | 10011 | 1.675 |
| 4 | 00100 | 1.300 | 20 | 10100 | 1.700 |
| 5 | 00101 | 1.325 | 21 | 10101 | 1.725 |
| 6 | 00110 | 1.350 | 22 | 10110 | 1.750 |
| 7 | 00111 | 1.375 | 23 | 10111 | 1.775 |
| 8 | 01000 | 1.400 | 24 | 11000 | 1.800 |
| 9 | 01001 | 1.425 | 25 | 11001 | 1.825 |
| 10 | 01010 | 1.450 | 26 | 11010 | 1.850 |
| 11 | 01011 | 1.475 | 27 | 11011 | Reserved |
| 12 | 01100 | 1.500 | 28 | 11100 | Reserved |
| 13 | 01101 | 1.525 | 29 | 11101 | Reserved |
| 14 | 01110 | 1.550 | 30 | 11110 | Reserved |
| 15 | 01111 | 1.575 | 31 | 11111 | Reserved |

Table 44. SW4A/B Electrical Specifications

Characteristics noted under conditions $BP = V_{SW4xIN} = 3.6\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at $BP = V_{SW4xIN} = 3.6\text{ V}$ and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------|----------------|-----|-----|-----|------|-------|
|--------|----------------|-----|-----|-----|------|-------|

SW4A/B Buck Regulator

| | | | | | | |
|--------------------|---|------------------|--------------|------------------|---------------|------|
| V_{SW4xIN} | Operating Input Voltage • PWM operation, $0\text{ mA} < I_L < I_{MAX}$ • PFM operation, $0\text{ mA} < I_L < I_{LMAX}$ | 3.0 2.8 | - - | 4.5 4.5 | V | (51) |
| $V_{SW4xACC}$ | Output Voltage Accuracy • PWM mode including ripple, load regulation, and transients • PFM Mode, including ripple, load regulation, and transients | Nom-3% Nom-3% | Nom Nom | Nom+3% Nom+3% | mV | (50) |
| I_{SW4x} | Continuous Output Load Current, $V_{INMIN} < BP < 4.5\text{ V}$ • PWM mode independent outputs • PWM mode single/dual phase • PFM mode | - - - | - - 50 | 500 1000 - | mA | |
| $I_{SW4xPEAK}$ | Current Limiter Peak Current Detection, $V_{IN} = 3.6\text{ V}$ • Current through inductor dual phase/independent outputs • Current through inductor single phase | - - | 1.0 2.0 | - - | A | |
| $V_{SW4xOS-START}$ | Start-up Overshoot • $I_L = 0\text{ mA}$ | - | - | 25 | mV | |
| $t_{ON-SW4x}$ | Turn-on Time • Enable to 90% of end value $I_L = 0\text{ mA}$ | - | - | 500 | μs | |

Table 44. SW4A/B Electrical Specifications

Characteristics noted under conditions $BP = V_{SW4xIN} = 3.6\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at $BP = V_{SW4xIN} = 3.6\text{ V}$ and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--|--|--------------------------------------|--|--------------------------------------|---------------|-------|
| SW4A/B Buck Regulator (CONTINUED) | | | | | | |
| f_{SW4} | Switching Frequency <ul style="list-style-type: none"> • PLLX = 0 • PLLX = 1 | - - | 2.0 4.0 | - - | MHz | |
| I_{SW4xQ} | Quiescent Current Consumption <ul style="list-style-type: none"> • APS Mode, $I_L = 0\text{ mA}$; device not switching • PFM Mode, $I_L = 0\text{ mA}$; device not switching | - - | 160 15 | - - | μA | |
| η_{SW4x} | Efficiency Independent Outputs <ul style="list-style-type: none"> • PFM, 3.15 V, 10 mA • PWM, 3.15 V, 50 mA • PWM, 3.15 V, 250 mA • PWM, 3.15 V, 500 mA • PFM, 1.2 V, 10 mA • PWM, 1.2 V, 50 mA • PWM, 1.2 V, 250 mA • PWM 1.2 V, 500 mA | - - - - - - - - | 79 93 92 82 72 71 81 78 | - - - - - - - - | % | (52) |

Notes:

50. Transient loading for load steps of $I_{LMAX} / 2$ at $100\text{ mA}/\mu\text{s}$.
51. When SW4A/B is set to 3.0 V and above the regulator may drop out of regulation when BP nears the output voltage.
52. Efficiency numbers at $V_{SW4xIN} = 3.6\text{ V}$, excludes the quiescent current.

7.5.4.7 SW5

SW5 is a fully integrated synchronous buck PWM voltage mode controlled DC/DC regulator.

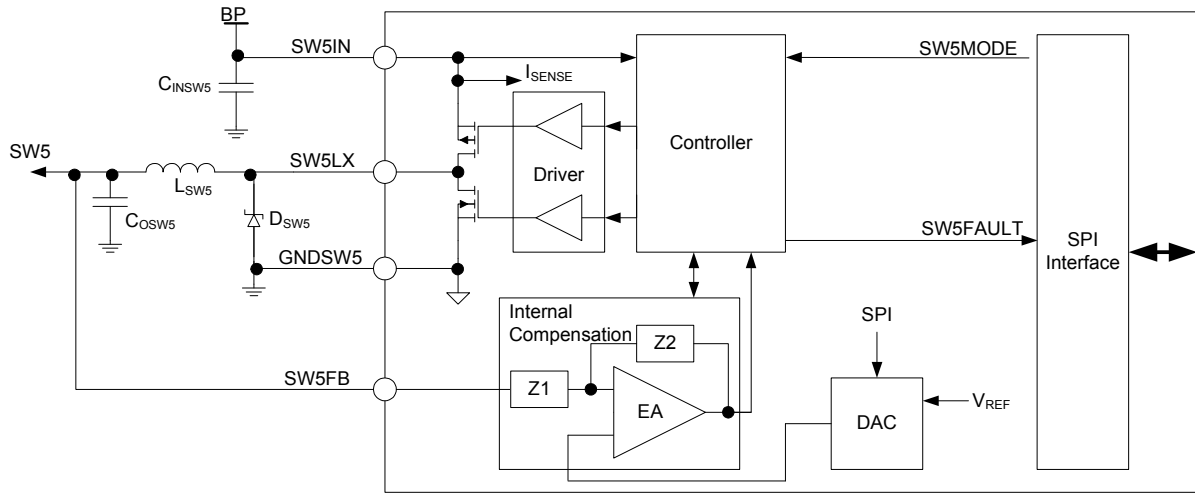


Figure 15. SW5 Block Diagram

The peak current is sensed internally for over-current protection purposes. If an over-current condition is detected the regulator will limit the current through cycle by cycle operation and alert the system through the SW5FAULT SPI bit and issue an SCPI interrupt via the INT pin.

SW5 can be programmed in step sizes of 25 mV as shown in [Table 45](#). If the software wants to change the output voltage after power-up, the regulator should be forced into PWM mode to change the voltage.

Table 45. SW5 Output Voltage Programmability

| Set Point | SW5[4:0] | SW5 Output (V) | Set Point | SW5[4:0] | SW5 Output (V) |
|-----------|----------|----------------|-----------|----------|----------------|
| 0 | 00000 | 1.200 | 16 | 10000 | 1.600 |
| 1 | 00001 | 1.225 | 17 | 10001 | 1.625 |
| 2 | 00010 | 1.250 | 18 | 10010 | 1.650 |
| 3 | 00011 | 1.275 | 19 | 10011 | 1.675 |
| 4 | 00100 | 1.300 | 20 | 10100 | 1.700 |
| 5 | 00101 | 1.325 | 21 | 10101 | 1.725 |
| 6 | 00110 | 1.350 | 22 | 10110 | 1.750 |
| 7 | 00111 | 1.375 | 23 | 10111 | 1.775 |
| 8 | 01000 | 1.400 | 24 | 11000 | 1.800 |
| 9 | 01001 | 1.425 | 25 | 11001 | 1.825 |
| 10 | 01010 | 1.450 | 26 | 11010 | 1.850 |
| 11 | 01011 | 1.475 | 27 | 11011 | Reserved |
| 12 | 01100 | 1.500 | 28 | 11100 | Reserved |
| 13 | 01101 | 1.525 | 29 | 11101 | Reserved |
| 14 | 01110 | 1.550 | 30 | 11110 | Reserved |
| 15 | 01111 | 1.575 | 31 | 11111 | Reserved |

Table 46. SW5 Electrical Specifications

Characteristics noted under conditions $BP = V_{SW5IN} = 3.6 \text{ V}$, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, unless otherwise noted. Typical values at $BP = V_{SW5IN} = 3.6 \text{ V}$ and $T_A = 25^\circ\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---------------------------|--|------------------|----------------------|------------------|---------------|-------|
| SW5 BUCK REGULATOR | | | | | | |
| V_{SW5IN} | Operating Input Voltage <ul style="list-style-type: none"> PWM operation, $0 \text{ mA} < I_L < I_{LMAX}$ PFM operation, $0 \text{ mA} < I_L < I_{LMAX}$ | 3.0 2.8 | - - | 4.5 4.5 | V | |
| V_{SW5ACC} | Output Voltage Accuracy <ul style="list-style-type: none"> PWM mode including ripple, load regulation, and transients PFM Mode, including ripple, load regulation, and transients | Nom-3% Nom-3% | Nom Nom | Nom+3% Nom+3% | mV | (53) |
| I_{SW5} | Continuous Output Load Current, $V_{INMIN} < BP < 4.5 \text{ V}$ <ul style="list-style-type: none"> PWM mode PFM mode | - - | - 50 | 1000 - | mA | |
| $I_{SW5PEAK}$ | Current Limiter Peak Current Detection <ul style="list-style-type: none"> $V_{SW5IN} = 3.6 \text{ V}$, Current through Inductor | - | 2.0 | - | A | |
| V_{SW5} OS-START | Start-up Overshoot <ul style="list-style-type: none"> $I_L = 0 \text{ mA}$ | - | - | 25 | mV | |
| t_{ON-SW5} | Turn-on Time <ul style="list-style-type: none"> Enable to 90% of end value $I_L = 0 \text{ mA}$ | - | - | 500 | μs | |
| f_{SW5} | Switching Frequency <ul style="list-style-type: none"> PLLX = 0 PLLX = 1 | - - | 2.0 4.0 | - - | MHz | |
| I_{SW5Q} | Quiescent Current Consumption <ul style="list-style-type: none"> APS Mode, $I_L = 0 \text{ mA}$; device not switching PFM Mode, $I_L = 0 \text{ mA}$; device not switching | - - | 160 15 | - - | μA | |
| η_{SW5} | Efficiency <ul style="list-style-type: none"> PFM, 1.8 V, 1.0 mA PWM, 1.8 V, 50 mA PWM, 1.8 V, 500 mA PWM, 1.8 V, 1000 mA | - - - - | 80 79 86 82 | - - - - | % | (54) |

Notes

53. Transient Loading for load Steps of $I_{LMAX}/2$ at $100 \text{ mA}/\mu\text{s}$.
54. Efficiency numbers at $V_{SW5IN} = 3.6 \text{ V}$, Excludes the quiescent current.

7.5.4.8 Dynamic Voltage Scaling

To reduce overall power consumption, processor core voltages can be varied depending on the mode or activity level of the processor. SW1A/B and SW2 allow for two different set points with controlled transitions to avoid sudden output voltage changes, which could cause logic disruptions on their loads.

Preset operating points for SW1A/B and SW2 can be set up for:

- Normal operation: output value selected by SPI bits SWx[5:0], refer to [Table 47](#).
- Standby mode: can be higher or lower than normal operation, but is typically selected to be the lowest state retention voltage for a given processor. The voltage set points are controlled by SPI bits SWxSTBY[5:0] and a Standby event.

Voltage transitions are governed by the SWxDVSSPEED[1:0] SPI bits shown in [Table 48](#).

Table 47. DVS Control Logic Table for SW1A/B and SW2

| STANDBY | Set Point Selected by |
|---------|-----------------------|
| 0 | SWx[4:0] |
| 1 | SWxSTBY[4:0] |

Table 48. DVS Speed Selection

| SWxDVSSPEED[1:0] | Function |
|------------------|--------------------------------|
| 00 | 12.5 mV step each 2.0 μ s |
| 01 (default) | 12.5 mV step each 4.0 μ s |
| 10 | 12.5 mV step each 8.0 μ s |
| 11 | 12.5 mV step each 16.0 μ s |

The regulator has a strong sourcing and sinking capability in the PWM mode. Therefore, the rising/falling slope is determined by the regulator in PWM mode. However, if the regulators are programmed in PFM, or APS mode during a DVS transition, the falling slope can be influenced by the load. Additionally, as the current capability in PFM mode is reduced, controlled DVS transitions in PFM mode could be affected. Critically timed DVS transitions are best assured with PWM mode operation.

Voltage transitions programmed through SPI(SWx[4:0]) on SW3 and SW5 will step in increments of 25 mV per 4.0 μ s, SW4A/B will step in increments of 25 mV per 8.0 μ s when SW4xHI[1:0]=00, and SW4A/B will step in increments of 25 mV per 16 μ s when SW4xHI[1:0]≠00. Additionally, SW3, SW4/B, and SW5 include standby mode set point programmability.

[Figure 16](#) shows the general behavior for the switching regulators when initiated with SPI programming or standby control.

SW1 and SW2 also contain Power Good. The power good signal is an active high open drain signal. When SWxPWGD is high, it means the regulator output has reached its programmed voltage. The SWxPWGD voltage outputs will be low during the DVS period and if the current limit is reached on the switching regulator. During the DVS period, the overcurrent condition on the switching regulator should be masked. If the current limit is reached outside of a DVS period, the SWxPWGD pin will stay low until the current limit condition is removed.

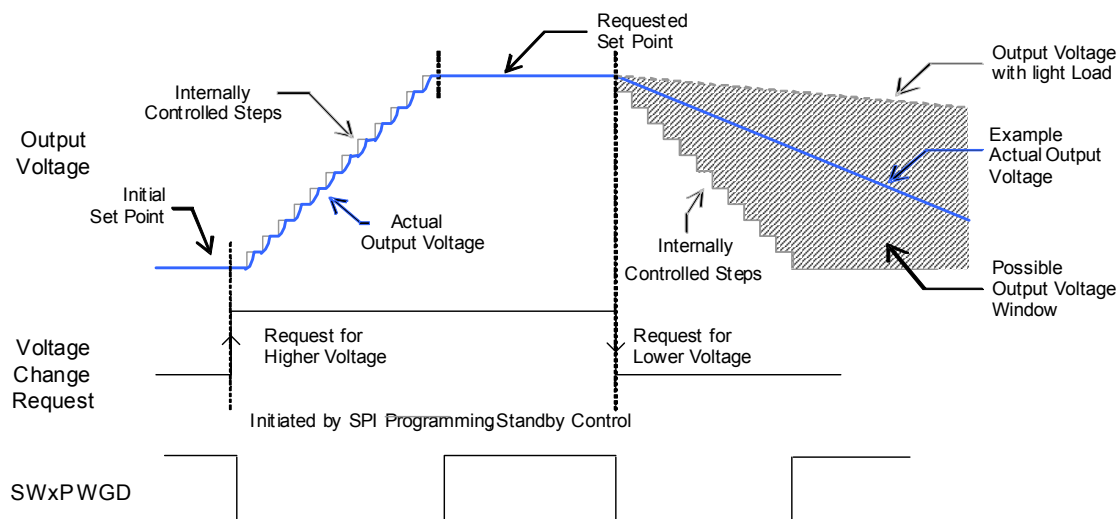


Figure 16. Voltage Stepping with DVS

7.5.5 Boost Switching Regulator

SWBST is a boost switching regulator with a programmable output, which defaults to 5.0 V on power-up, operating at 2.0 MHz. It integrates the switching NMOS transistor on-chip, and requires an external fly back schottky diode, inductor, and input/output capacitors. The parasitic leakage path for a boost regulator will cause the output voltage SWBSTOUT and SWBSTFB to sit at a schottky voltage drop below the battery voltage whenever SWBST is disabled.

SWBST supplies the VUSB regulator for the USB PHY.

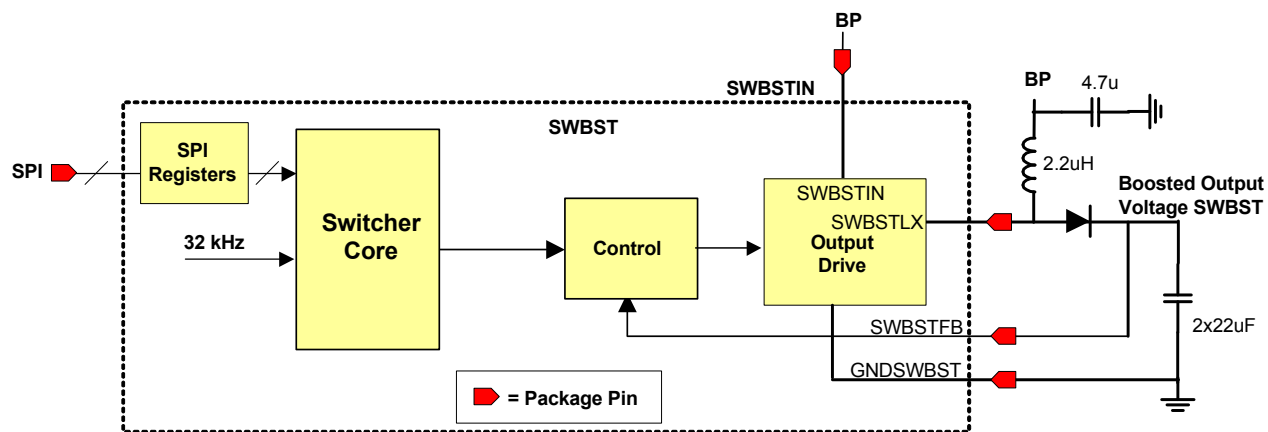


Figure 17. Boost Regulator Architecture

SWBST output voltage is programmable via the SWBST[1:0] SPI bits as shown in [Table 49](#).

Table 49. SWBST Voltage Programming

| Parameter | Voltage | SWBST Output Voltage |
|------------|---------|----------------------|
| SWBST[1:0] | 00 | 5.00 (default) |
| | 01 | 5.05 |
| | 10 | 5.10 |
| | 11 | 5.15 |

SWBST can be controlled by SPI programming in PFM, APS, and Auto mode. Auto mode transitions between PFM and APS mode based on the load current. By default SWBST is powered up in Auto mode.

Table 50. SWBST Mode Control

| Parameter | Voltage | SWBST Mode |
|--------------------------------------|---------|----------------|
| SWBSTMODE[1:0] SWBSTSTBYMODE[1:0] | 00 | Off |
| | 01 | PFM |
| | 10 | Auto (default) |
| | 11 | APS |

Table 51. SWBST Electrical Specifications

Characteristics noted under conditions BP = $S_{WBSTIN} = 3.6\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = $S_{WBSTIN} = 3.6\text{ V}$ and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---------------------------------|---|--------|-----------|--------|---------------|-------|
| SWITCH MODE SUPPLY SWBST | | | | | | |
| V_{SWBST} | Average Output Voltage • $3.0\text{ V} < V_{IN} < 4.5\text{ V}$, $0\text{ mA} < I_L < I_{LMAX}$ | Nom-4% | V_{NOM} | Nom+3% | V | (55) |
| $V_{SWBSTACC}$ | Output Ripple • $3.0\text{ V} < V_{IN} < 4.5\text{ V}$, $0\text{ mA} < I_L < I_{LMAX}$, excluding reverse recovery of Schottky diode | - | - | 120 mV | Vp-p | |
| $SWBST_{ACC}$ | Average Load Regulation • $V_{IN} = 3.6\text{ V}$, $0\text{ mA} < I_L < I_{LMAX}$ | - | 0.5 | - | mV/mA | |
| $V_{SWBSTLINEAREG}$ | Average Line Regulation • $3.0\text{ V} < V_{IN} < 4.5\text{ V}$, $I_L = I_{LMAX}$ | - | 50 | - | mV | |
| I_{SWBST} | Continuous Load Current • $3.0\text{ V} < V_{IN} < 4.5\text{ V}$, $V_{OUT} = 5.0\text{ V}$ | - | - | 380 | mA | |
| $I_{SWBSTPEAK}$ | Peak Inductor Current Limit • $V_{IN} = 3.6\text{ V}$ | - | 1800 | - | mA | |
| $V_{SWBSTOS-START}$ | Start-up Overshoot • $I_L = 0\text{ mA}$ | - | - | 500 | mV | |
| $t_{ON-SWBST}$ | Turn-on Time • Enable to 90% of V_{OUT} $I_L = 0\text{ mA}$ | - | - | 2.0 | ms | |
| f_{SWBST} | Switching Frequency | - | 2.0 | - | MHz | |
| $V_{SWBSTTRANSIENT}$ | Transient Load Response, I_L from 1.0 mA to 100 mA in 1.0 μs steps • Maximum transient Amplitude | - | - | 300 | mV | |
| $V_{SWBSTTRANSIENT}$ | Transient Load Response, I_L from 100 mA to 1.0 mA in 1.0 μs steps • Maximum transient Amplitude | - | - | 300 | mV | |
| $V_{SWBSTTRANSIENT}$ | Transient Load Response, I_L from 1.0mA to 100 mA in 1.0 μs steps • Time to settle 80% of transient | - | - | 500 | μs | |
| $V_{SWBSTTRANSIENT}$ | Transient Load Response, I_L from 100 mA to 1.0 mA in 1.0 μs steps • Time to settle 80% of transient | - | - | 20 | ms | |
| η_{SWBST} | Efficiency, $I_L = I_{LMAX}$ | 65 | 80 | - | % | |

Table 51. SWBST Electrical Specifications

Characteristics noted under conditions BP = $S_{WBSTIN} = 3.6\text{ V}$, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = $S_{WBSTIN} = 3.6\text{ V}$ and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---|---|-----|-----|-----|---------------|-------|
| SWITCH MODE SUPPLY SWBST (CONTINUED) | | | | | | |
| $I_{SWBSTBIAS}$ | Bias Current Consumption • PFM or Auto mode | - | 35 | - | μA | |
| $I_{LEAK-SWBST}$ | NMOS Off Leakage • $S_{WBSTIN} = 4.5\text{ V}$, $S_{WBSTMODE} [1:0] = 00$ | - | 1.0 | 6.0 | μA | |

Notes:

55. V_{IN} is the low side of the inductor that is connected to BP.

7.5.6 Linear Regulators (LDOs)

This section describes the linear regulators provided. For convenience, these regulators are named to indicate their typical or possible applications, but the supplies are not limited to these uses and may be applied to any loads within the specified regulator capabilities.

A low-power standby mode controlled by STANDBY is provided for the regulators with an external pass device, in which the bias current is aggressively reduced. This mode is useful for deep sleep operation, where certain supplies cannot be disabled, but active regulation can be tolerated with less parametric requirements. The output drive capability and performance are limited in this mode.

7.5.6.1 General Guidelines

The following applies to all linear regulators, unless otherwise specified.

- Parametric specifications assume the use of low ESR X5R/X7R ceramic capacitors with 20% accuracy and 15% temperature spread, for a worst case stack up of 35% from the nominal value. Use of other types with wider temperature variation may require a larger room temperature nominal capacitance value to meet performance specs over temperature. Capacitor derating as a function of DC bias voltage requires special attention. Minimum bypass capacitor guidelines are provided for stability and transient performance. However larger values may be applied, but performance metrics may be altered and generally improved and should be confirmed in system applications.
- Regulators with an external PNP transistor require an equivalent resistance (including the ESR) in series with the output capacitor, as noted in the specific regulator sections.
- Output voltage tolerance specified for each of the linear regulators include process variation, temperature range, static line regulation, and static load regulation.
- In the Low-power mode, the output performance is degraded. Only those parameters listed in the Low-power mode section are guaranteed. In this mode, the output current is limited to much lower levels than in the active mode.
- When a regulator gets disabled, the output will be pulled to ground by an internal pull-down. The pull-down is also activated when RESETB goes low.

7.5.6.2 LDO Regulator Control

The regulators with embedded pass devices (VPLL, VGEN1, and VUSB) have an adaptive biasing scheme thus, there are no distinct operating modes such as a Normal mode and a Low-power mode. Therefore, no specific control is required to put these regulators in a Low-power mode.

The external pass regulator (VDAC) can operate in both normal or low-power mode. Since a load current detection cannot be performed for this regulator, the transition between both modes is not automatic and is controlled by setting the corresponding mode bits for the desired operational behavior.

The regulators VUSB2, and VGEN2 can be configured for using the internal or external pass device. For both configurations, the transition between normal and Low-power modes is controlled by setting the $VxMODE$ bit for the specific regulator. If configured with an internal pass device, the transition between normal and low-power mode will be automatic. If configured with an external pass device, the transition between modes must be manually controlled.

The regulators can be disabled and the general purpose outputs can be forced low when going into Standby, note that the Standby response timing can be modified with the STBYDLY function, as described in the [Power Saving](#) section. Each regulator has an associated SPI bit for this. When the bit is not set, STANDBY is of no influence. The actual operating mode of the regulators as a function of STANDBY is not reflected through SPI, in other words, the SPI will read what is programmed and not the actual state.

Table 52. LDO Regulator Control (External Pass Device LDOs)

| VxEN | VxMODE | VxSTBY | STANDBY ⁽⁵⁶⁾ | Regulator Vx |
|------|--------|--------|-------------------------|--------------|
| 0 | X | X | X | Off |
| 1 | 0 | 0 | X | On |
| 1 | 1 | 0 | X | Low-power |
| 1 | X | 1 | 0 | On |
| 1 | 0 | 1 | 1 | Off |
| 1 | 1 | 1 | 1 | Low-power |

Notes

56. STANDBY refers to a Standby event as described in [Power Saving](#)

For regulators operating with internal pass devices, only VxEN and VxSTBY bits will impact the state of the respective LDO in normal or Standby mode, as shown in [Table 53](#).

Table 53. LDO Regulator Control (internal pass device LDOs)

| VxEN | VxSTBY | STANDBY ⁽⁵⁷⁾ | Regulator Vx |
|------|--------|-------------------------|--------------|
| 0 | X | X | Off |
| 1 | 0 | X | On |
| 1 | 1 | 0 | On |
| 1 | 1 | 1 | Off |

Notes

57. STANDBY refers to a Standby event as described in [Power Saving](#)

7.5.6.3 Transient Response Waveforms

The transient load and line response are specified with the waveforms depicted in [Figure 18](#). Note, the transient load response refers to the overshoot only, and excludes the DC shift. The transient line response refers to the sum of both, overshoot and DC shift. These conditions are also valid for the mode transition response.

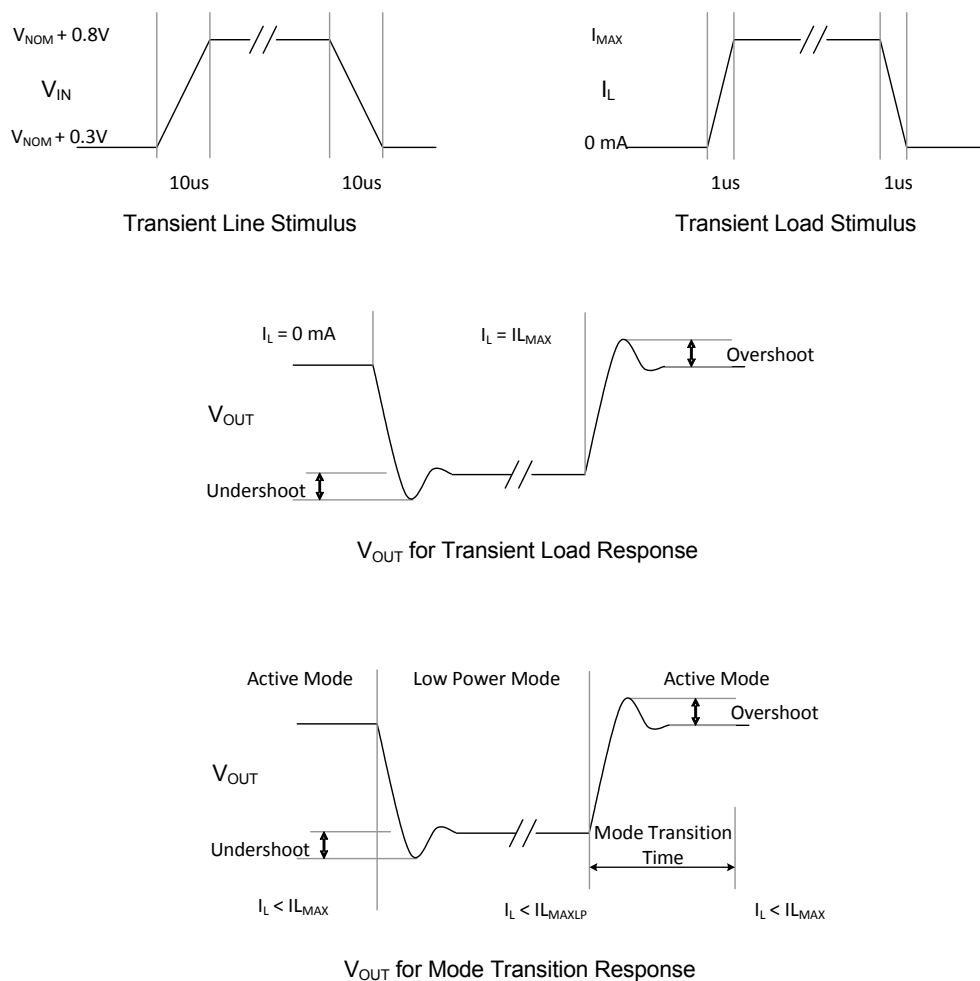


Figure 18. Transient Waveforms

7.5.6.4 Short-circuit Protection

The higher current LDOs, and those most accessible in product applications, include short-circuit detection and protection (VDAC, VUSB, VUSB2, VGEN1, and VGEN2). The short-circuit protection (SCP) system includes debounced fault condition detection, regulator shutdown, and processor interrupt generation, to contain failures and minimize the chance of product damage. If a short-circuit condition is detected, typically 20% above I_{L_MAX} , the LDO will be disabled by resetting its V_{xEN} bit, while at the same time, an interrupt SCPI will be generated to flag the fault to the system processor. The SCPI interrupt is maskable through the SCPM mask bit.

The SCP feature is enabled by setting the REGSCPEN bit. If this bit is not set, then not only is no interrupt generated, but also the regulators will not automatically be disabled upon a short-circuit detection. However, the built-in current limiter will continue to limit the output current of the regulator. Note that by default, the REGSCPEN bit is not set, so at start-up, none of the regulators in an overload condition are disabled.

7.5.6.5 VPLL

VPLL is provided for isolated biasing of the application processors' PLLs that serves as the clock generation in support of protocol and peripheral needs. Depending on the application and power requirements, this supply may be considered for sharing with other loads, but noise injection must be avoided and filtering added if necessary to ensure suitable PLL performance.

The VPLL regulator has a dedicated input supply pin. VINPLL can be connected to either BP or a 1.8 V switched mode power supply rail such as from SW5 for the two lower set points of the VPLL regulator (VPLL[1:0] = 00, 01). In addition, when the two upper set points (VPLL[1:0] = 10, 11) are used, the VINPLL inputs can be connected to either BP or a 2.2 V nominal external supply rail, to improve power dissipation.

Table 54. VPLL Voltage Control

| Parameter | Value | Function | ILoad max | Input Supply |
|-----------|-------|-----------------|-----------|-----------------------|
| VPLL[1:0] | 00 | output = 1.2 V | 50 mA | BP or 1.8 V |
| | 01 | output = 1.25 V | 50 mA | BP or 1.8 V |
| | 10 | output = 1.50 V | 50 mA | BP or External supply |
| | 11 | output = 1.8 V | 50 mA | BP or External supply |

Table 55. VPLL Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------|----------------|-----|-----|-----|------|-------|
|--------|----------------|-----|-----|-----|------|-------|

GENERAL

| | | | | | | |
|-------------|---|-----------------------|-----------------|-------------------|----|--|
| V_{INPLL} | Operating Input Voltage Range V_{INMIN} to V_{INMAX} <ul style="list-style-type: none"> VPLL all settings, BP biased VPLL [1:0] = 00, 01 (SW5 = 1.8 V) VPLL, [1:0] = 10, 11, External Switch | UVDET 1.75 2.15 | - 1.8 2.2 | 4.5 4.5 4.5 | V | |
| I_{PLL} | Operating current Load range | - | - | 50 | mA | |

VPLL ACTIVE MODE – DC

| | | | | | | |
|----------------|---|------------------|-----------|------------------|---------------|--|
| V_{PLL} | Output Voltage V_{OUT} | $V_{NOM} - 0.05$ | V_{NOM} | $V_{NOM} + 0.05$ | V | |
| $V_{PLL-LOPP}$ | Load Regulation <ul style="list-style-type: none"> $1.0\text{ mA} < I_L < I_{LMAX}$ | - | 0.35 | - | mV/mA | |
| $V_{PLL-LIPP}$ | Line Regulation | - | 5.0 | - | mV | |
| I_{PLL-Q} | Quiescent Current <ul style="list-style-type: none"> $I_L = 0\text{ mA}$ | - | 8.0 | - | μA | |
| I_{PLLIM} | Current Limit <ul style="list-style-type: none"> Output voltage forced to $V_{PLL_{NOM}}/2$ | 54 | 78 | 120 | mA | |

VPLL ACTIVE MODE – AC

| | | | | | | |
|----------------|--|--------|----------|--------|----|--|
| $V_{PLL-PSRR}$ | PSRR $I_L = 75\%$ of I_{LMAX} , 20 Hz to 20 kHz <ul style="list-style-type: none"> $V_{INPLL} = UVDET$ $V_{INPLL} = V_{NOM} + 1.0\text{ V}, > UVDET$ | - - | 70 75 | - - | dB | |
|----------------|--|--------|----------|--------|----|--|

Table 55. VPLL Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--|---|------|-----|-----|---------------|-------|
| VPLL ACTIVE MODE – AC (CONTINUED) | | | | | | |
| $t_{\text{ON-VPLL}}$ | Turn-on Time • Enable to 90% of end value $V_{\text{INPLL}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_L = 0\text{ mA}$ | - | - | 140 | μs | |
| $t_{\text{OFF-VPLL}}$ | Turn-off Time • Disable to 10% of initial value $V_{\text{INPLL}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_L = 0\text{ mA}$ | 0.05 | - | 10 | ms | |
| $V_{\text{PLL-OS-START}}$ | Start-up Overshoot • $V_{\text{INPLL}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_L = 0\text{ mA}$ | - | 1.0 | 2.0 | % | |
| $V_{\text{PLL-LO-TRANSIENT}}$ | Transient Load Response • $V_{\text{INPLL}} = V_{\text{INMIN}}, V_{\text{INMAX}}$ | - | 50 | 70 | mV | |
| $V_{\text{PLL-LI-TRANSIENT}}$ | Transient Line Response • $I_L = 75\%$ of $I_{L\text{-MAX}}$ | - | 5.0 | 8.0 | mV | |

7.5.6.6 VREFDDR

VREFDDR is an internal PMOS half supply voltage follower. The output voltage is at one half the input voltage. It's typical application is as the V_{REF} for DDR memories. A filtered resistor divider is utilized to create a low frequency pole. This divider then uses a voltage follower to drive the load.

Table 56. VREFDDR Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---------------------------------|--|------|-------------------|-----|---------------|-------|
| GENERAL | | | | | | |
| V_{REFDDRIN} | Operating Input Voltage Range V_{INMIN} to V_{INMAX} | 1.2 | - | 1.8 | V | |
| I_{REFDDR} | Operating Current Load Range $I_{L\text{-MIN}}$ to $I_{L\text{-MAX}}$ | 0.0 | - | 10 | mA | |
| VREFDDR ACTIVE MODE – DC | | | | | | |
| V_{REFDDR} | Output Voltage V_{OUT} | - | $V_{\text{IN}}/2$ | - | V | |
| V_{REFDRTOL} | Output Voltage tolerance • $0.6\text{ mA} < I_L < 10\text{ mA}$ | -1.0 | - | 1.0 | % | |
| $V_{\text{REFDDR-LOPP}}$ | Load Regulation • $1.0\text{ mA} < I_L < I_{L\text{-MAX}}$ | - | 0.5 | - | mV/mA | |
| I_{REFDDRQ} | Quiescent Current • $I_L = 0\text{ mA}$ | - | 8.0 | - | μA | |
| $I_{\text{REFDDR LIM}}$ | Current Limit • Output voltage forced to $V_{\text{REFDDR-NOM}}/2$ | 12 | 28 | 55 | mA | |
| VREFDDR ACTIVE MODE – AC | | | | | | |
| $t_{\text{ON-VREFDDR}}$ | Turn-on Time • Enable to 90% of end value $V_{\text{REFDDRIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_L = 0\text{ mA}$ | - | - | 100 | μs | |

Table 56. VREFDDR Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|------------------------------------|--|------|-----|-----|------|-------|
| $t_{\text{OFF-}}^{\text{VREFDDR}}$ | Turn-off Time • Disable to 10% of initial value $V_{\text{REFDDRIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$ IL = 0 mA | 0.05 | - | 10 | ms | |

VREFDDR ACTIVE MODE – AC (CONTINUED)

| | | | | | | |
|--|--|---|-----|-----|----|--|
| $V_{\text{REFDDR}}^{\text{DROS}}$ | Start-up Overshoot • $V_{\text{REFDDRIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$ IL = 0 mA | - | 1.0 | 2.0 | % | |
| $V_{\text{REFDDR}}^{\text{DRL TRANSIENT}}$ | Transient Load Response • $V_{\text{REFDDRIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$ | - | 5.0 | - | mV | |

7.5.6.7 VUSB

The VUSB regulator is used to supply 3.3 V to the external USB PHY, it is powered from the SWBST boost supply to ensure current sourcing compliance through the normal discharge range of the battery/supply input. VUSB has an internal PMOS pass FET which will support loads of up to 100 mA.

Table 57. VUSB Electrical Characteristics

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------|----------------|-----|-----|-----|------|-------|
|--------|----------------|-----|-----|-----|------|-------|

VUSB REGULATOR

| | | | | | | |
|--------------------|---|--------------------------|---|--------------------------|----|--|
| V_{USBIN} | Operating Input Voltage Range V_{INMIN} to V_{INMAX} • Supplied by SWBST | $V_{\text{SWBST}} - 4\%$ | - | $V_{\text{SWBST}} + 3\%$ | V | |
| I_{USB} | Operating Current Load Range I_{LMIN} to I_{LMAX} | 0.0 | - | 100 | mA | |

VUSB ACTIVE MODE - DC

| | | | | | | |
|----------------------|---|------------------------|-----|------------------------|-------|--|
| V_{USB} | Output Voltage V_{OUT} | $V_{\text{NOM}} - 4\%$ | 3.3 | $V_{\text{NOM}} + 4\%$ | V | |
| V_{USBLOPP} | Load Regulation • $0\text{ mA} < I_L < I_{\text{LMAX}}$ from DM / DP | - | 1.0 | - | mV/mA | |
| V_{USBLIPP} | Line Regulation | - | - | 20 | mV | |
| I_{USBLIM} | Current Limit • Output voltage forced to $V_{\text{USBNOM}}/2$ | 120 | 180 | 225 | mA | |

VUSB ACTIVE MODE - AC

| | | | | | | |
|--------------------------------|--|---|----|---|----|--|
| $V_{\text{USB}}^{\text{PSRR}}$ | PSRR IL = 75% of I_{LMAX} 20 Hz to 20 kHz • $V_{\text{USBIN}} = V_{\text{INMIN}} + 100\text{ mV}$ | - | 65 | - | dB | |
|--------------------------------|--|---|----|---|----|--|

7.5.6.8 VUSB2

VUSB2 has an internal PMOS pass FET to support light loads. An external PNP configuration is offered to avoid excess on-chip power dissipation at high loads and large differentials between BP and output settings. The input pin for the integrated PMOS option is shared with the base current drive pin for the external PNP option. The external PNP configuration must be committed as a hardwired board level implementation. The recommended PNP device is the ON Semiconductor™ NSS12100XV6T1G, which is capable of handling up to 250 mW of continuous dissipation, at minimum footprint and 75 °C ambient temperature. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is the ON Semiconductor NSS12100UW3TCG. For stability reasons, a total resistance of 50 mΩ ±20% in series with the output capacitance is required. The total resistance includes the ESR of the capacitor plus an external resistance provided by a discrete resistor or PCB circuit trace.

The nominal output voltage of this regulator is configured through SPI, and can be selected among 2.5 V, 2.6 V, 2.75 V, or 3.0 V. The output current when working with the internal pass FET is 65 mA, and could be up to 350 mA when working with an external PNP.

Table 58. VUSB2 Voltage Control

| Bits | Value | Output Voltage | ILoad max | |
|------------|-------|----------------|------------------------------------|-------------------------------|
| | | | VUSB2CONFIG=0 Internal Pass FET | VUSB2CONFIG=1 External PNP |
| VUSB2[1:0] | 00 | 2.50 V | 65 mA | 350 mA |
| | 01 | 2.60 V | 65 mA | 350 mA |
| | 10 | 2.75 V | 65 mA | 350 mA |
| | 11 | 3.00 V | 65 mA | 350 mA |

Table 59. VUSB2 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---------------------|---|-------------------------|--------|-----------|------|-------|
| GENERAL | | | | | | |
| V _{USB2IN} | Operating Input Voltage Range V _{INMIN} to V _{INMAX} | V _{NOM} + 0.30 | - | 4.5 | V | |
| I _{USB2} | Operating Current Load Range I _{LMIN} to I _{LMAX} <ul style="list-style-type: none"> Internal pass FET External PNP Not exceeding PNP max power | 0.0 0.0 | - - | 65 350 | mA | |
| V _{USB2IN} | Extended Input Voltage Range <ul style="list-style-type: none"> Performance may be out of specification | UVDET | - | 4.5 | V | |

VUSB2 ACTIVE MODE - DC

| | | | | | | |
|-------------------------|---|-----------------------|------------------|-----------------------|-------|------|
| V _{USB2} | Output Voltage V _{OUT} | V _{NOM} - 3% | V _{NOM} | V _{NOM} + 3% | V | |
| V _{USB2LOPP} | Load Regulation <ul style="list-style-type: none"> 1.0 mA < I_L < I_{LMAX} | - | 0.25 | - | mV/mA | |
| V _{USB2LIPP} | Line Regulation | - | 8.0 | - | mV | |
| I _{USB2Q} | Active Mode Quiescent Current <ul style="list-style-type: none"> I_L = 0 mA, Internal PMOS configuration I_L = 0 mA, External PNP configuration | - - | 25 30 | - - | μA | |
| I _{USB2DRVLIM} | VUSB2DRV Base Drive Current Limit <ul style="list-style-type: none"> External PNP mode only | 3.36 | 4.62 | 6.10 | mA | (58) |

Table 59. VUSB2 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|----------------------------------|---|------------------------|------------------|------------------------|---------------|-------|
| VUSB2 LOW-POWER MODE - DC | | | | | | |
| V_{USB2} | Output Voltage V_{OUT} • $I_{\text{LMINLP}} < I_{\text{L}} < I_{\text{LMAXLP}}$ | $V_{\text{NOM}} - 3\%$ | V_{NOM} | $V_{\text{NOM}} + 3\%$ | V | |
| I_{USB2LP} | Current Load Range I_{LMINLP} to I_{LMAXLP} | 0.0 | - | 3.0 | mA | |
| I_{USB2Q} | Low-power Mode Quiescent Current • $I_{\text{L}} = 0\text{ mA}$ | - | 8.0 | - | μA | |
| VUSB2 ACTIVE MODE - AC | | | | | | |
| V_{USB2PSRR} | PSRR $I_{\text{L}} = 75\%$ of I_{LMAX} , 20 Hz to 20 kHz • $V_{\text{USB2IN}} = V_{\text{INMIN}} + 100\text{ mV}$ • $V_{\text{USB2IN}} = V_{\text{NOM}} + 1.0\text{ V}$ | - - | 30 30 | - - | dB | |
| $t_{\text{ON-VUSB2}}$ | Turn-on Time • Enable to 90% of end value, $V_{\text{USB2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_{\text{L}} = 0\text{ mA}$ | - | - | 1.0 | ms | |
| $t_{\text{OFF-VUSB2}}$ | Turn-off Time • Disable to 10% of initial value, $V_{\text{USB2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_{\text{L}} = 0\text{ mA}$ | 0.05 | - | 10 | ms | |
| $V_{\text{USB2OS-START}}$ | Start-up Overshoot • $I_{\text{L}} = 0\text{ mA}$ | - | 1.0 | 2.0 | % | |
| $V_{\text{USB2LO TRANSIENT}}$ | Transient Load Response $V_{\text{USB2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$ • VUSB2=01, 10, 11 • VUSB2=00 | - - | 1.0 50 | 2.0 70 | % mV | |
| $V_{\text{USB2LI TRANSIENT}}$ | Transient Line Response • $I_{\text{L}} = 75\%$ of I_{LMAX} | - | 5.0 | 8.0 | mV | |
| $t_{\text{MOD-VUSB2}}$ | Mode Transition Time • From low-power to active and from active to low-power $V_{\text{USB2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_{\text{L}} = I_{\text{LMAXLP}}$ | - | - | 100 | μs | |
| $V_{\text{USBMODE RES}}$ | Mode Transition Response • From low-power to active and from active to low-power $V_{\text{USB2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_{\text{L}} = I_{\text{LMAXLP}}$ | - | 1.0 | 2.0 | % | |

Notes

58. V_{USB2} current limit is given by $I_{\text{USB2DRVLIM}} \times \beta$ of external PNP transistor

7.5.6.9 VDAC

The primary applications of this power supply is the TV-DAC. However, these supplies could also be used for other peripherals if one of these functions is not required. Low-power modes and programmable standby options can be used to optimize power efficiency during deep sleep modes.

An external PNP is utilized for VDAC to avoid excess on-chip power dissipation at high loads and large differentials between BP and output settings. External PNP devices must always be connected to the BP line in the application. The recommended PNP device is the ON Semiconductor NSS12100XV6T1G, which is capable of handling up to 250 mW of continuous dissipation at minimum footprint and $75\text{ }^{\circ}\text{C}$ ambient temperature. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is the ON Semiconductor NSS12100UW3TCG. For stability reasons, a total resistance of 110 m Ω

±20% in series with the output capacitance is required. The total resistance includes the ESR of the capacitor plus an external resistance provided by a discrete resistor or PCB circuit trace.

The nominal output voltage of this regulator can be configured through SPI and can be 2.5 V, 2.6 V, 2.7 V, or 2.775 V. The maximum output current along the external PNP is 250 mA.

Table 60. VDAC Voltage Control

| Parameter | Value | Output Voltage | ILoad max |
|-----------|-------|----------------|-----------|
| VDAC[1:0] | 00 | 2.500 V | 250 mA |
| | 01 | 2.600 V | 250 mA |
| | 10 | 2.700 V | 250 mA |
| | 11 | 2.775 V | 250 mA |

Table 61. VDAC Electrical Specification

Characteristics noted under conditions BP = 3.6 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------|----------------|-----|-----|-----|------|-------|
|--------|----------------|-----|-----|-----|------|-------|

GENERAL

| | | | | | | |
|--------------------|--|-------------------------|---|-----|----|--|
| V _{DACIN} | Operating Input Voltage Range V _{INMIN} to V _{INMAX} | V _{NOM} + 0.25 | - | 4.5 | V | |
| I _{DAC} | Operating Current Load Range I _{LMIN} to I _{LMAX} • Not exceeding PNP max power | 0.0 | - | 250 | mA | |
| V _{DACIN} | Extended Input Voltage Range • Performance may be out of specification | UVDET | - | 4.5 | V | |

VDAC ACTIVE MODE – DC

| | | | | | | |
|------------------------|--|-----------------------|------------------|-----------------------|-------|------|
| V _{DAC} | Output Voltage V _{OUT} | V _{NOM} – 3% | V _{NOM} | V _{NOM} + 3% | V | |
| V _{DACLOPP} | Load Regulation • 1.0 mA < I _L < I _{LMAX} | - | 0.20 | - | mV/mA | |
| V _{DACLIPP} | Line Regulation | - | 5.0 | - | mV | |
| I _{DACQ} | Active Mode Quiescent Current • I _L = 0 mA | - | 30 | - | μA | |
| I _{DACDRVLIM} | VDACDRV Base Current Limit | - | 5.3 | - | mA | (59) |

VDAC LOW-POWER MODE – DC - VDACMODE=1

| | | | | | | |
|-------------------|---|-----------------------|------------------|-----------------------|----|--|
| V _{DAC} | Output Voltage V _{OUT} | V _{NOM} – 3% | V _{NOM} | V _{NOM} + 3% | V | |
| I _{DAC} | Current Load Range I _{LMINLP} to I _{LMAXLP} | 0.0 | - | 3.0 | mA | |
| I _{DACQ} | Low-power Mode Quiescent Current • I _L = 0 mA | - | 8.0 | - | μA | |

VDAC ACTIVE MODE – AC

| | | | | | | |
|----------------------|--|--------|----------|--------|----|--|
| V _{DACPSRR} | PSRR I _L = 75% of I _{LMAX} 20 Hz to 20 kHz • V _{DACIN} = V _{INMIN} + 100 mV • V _{DACIN} = V _{NOM} + 1.0 V | - - | 50 50 | - - | dB | |
| t _{ON-VDAC} | Turn-on Time • Enable to 90% of end value V _{DACIN} = V _{INMIN} , V _{INMAX} ; I _L = 0 mA | - | - | 1.0 | ms | |

Table 61. VDAC Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|-----------------------|---|------|-----|-----|------|-------|
| $t_{\text{OFF-VDAC}}$ | Turn-off Time • Disable to 10% of initial value $V_{\text{DACIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_L = 0\text{ mA}$ | 0.05 | - | 10 | ms | |

VDAC ACTIVE MODE – AC (CONTINUED)

| | | | | | | |
|-------------------------------------|--|---|-----|-----|---------------|--|
| $\text{VDAC}_{\text{OS-START}}$ | Start-up Overshoot • $V_{\text{DACIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_L = 0\text{ mA}$ | - | 1.0 | 2.0 | % | |
| $\text{VDAC}_{\text{LO-TRANSIENT}}$ | Transient Load Response • $V_{\text{DACIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$ | - | 1.0 | 2.0 | % | |
| $\text{VDAC}_{\text{LI-TRANSIENT}}$ | Transient Line Response • $I_L = 75\%$ of $I_{L\text{-MAX}}$ | - | 5.0 | 8.0 | mV | |
| $t_{\text{MODE-VDAC}}$ | Mode Transition Time • From low-power to active $V_{\text{DACIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_L = I_{L\text{-MAXLP}}$ | - | - | 100 | μs | |
| $\text{VDAC}_{\text{MODE-RES}}$ | Mode Transition Response • From low-power to active and from active to low-power $V_{\text{DACIN}} = V_{\text{INMIN}}, V_{\text{INMAX}}; I_L = I_{L\text{-MAXLP}}$ | - | 1.0 | 2.0 | % | |

Notes

59. V_{DAC} current limit is given by $I_{\text{DACDRVLM}} \times \beta$ of external PNP transistor

7.5.6.10 VGEN1, VGEN2

General purpose LDOs, VGEN1, and VGEN2, are provided for expansion of the power tree to support peripheral devices, which could include EMMC cards, WLAN, BT, GPS, or other functional modules. These regulators include programmable set points for system flexibility. VGEN1 has an internal PMOS pass FET, and is powered from the SW5 buck for an efficiency advantage and reduced power dissipation in the pass device. VGEN2 is powered directly from the battery.

VGEN2 has an internal PMOS pass FET, which will support loads up to 50 mA. For higher current capability, drive for an external PNP is provided. The external PNP is offered to avoid excess on-chip power dissipation at high loads and large differentials between BP and output settings. The input pin for the integrated PMOS option is shared with the base current drive pin for the PNP option. The external PNP device is always connected to the BP line in the application. The recommended PNP device is the ON Semiconductor NSS12100XV6T1G which is capable of handling up to 250 mW of continuous dissipation at minimum footprint and $75\text{ }^{\circ}\text{C}$ ambient temperature. For use cases where up to 500 mW of dissipation is required, the recommended PNP device is the ON Semiconductor NSS12100UW3TCG. For stability reasons, a total resistance of $60\text{ m}\Omega \pm 20\%$ in series with the output capacitance is required. The total resistance includes the ESR of the capacitor plus an external resistance provided by a discrete resistor or PCB circuit trace.

The nominal output voltage of both VGEN1 and VGEN2 are SPI configurable with the $\text{VGENx}[2:0]$ bits as shown in [Table 62](#) and [Table 63](#).

Table 62. VGEN1 Control Register Bit Assignments

| Parameter | Value | Output Voltage | ILoad max |
|-----------|-------|----------------|-----------|
|-----------|-------|----------------|-----------|

Table 62. VGEN1 Control Register Bit Assignments

| | | | |
|------------|-----|------|--------|
| VGEN1[2:0] | 000 | 1.20 | 250 mA |
| | 001 | 1.25 | 250 mA |
| | 010 | 1.30 | 250 mA |
| | 011 | 1.35 | 250 mA |
| | 100 | 1.40 | 250 mA |
| | 101 | 1.45 | 250 mA |
| | 110 | 1.50 | 250 mA |
| | 111 | 1.55 | 250 mA |

Table 63. VGEN2 Control Register Bit Assignments

| Parameter | Value | Output Voltage | ILoad max | |
|------------|-------|----------------|------------------------------------|-------------------------------|
| | | | VGEN2CONFIG=0 Internal Pass FET | VGEN2CONFIG=1 External PNP |
| VGEN2[2:0] | 000 | 2.50 | 50 mA | 250 mA |
| | 001 | 2.70 | 50 mA | 250 mA |
| | 010 | 2.80 | 50 mA | 250 mA |
| | 011 | 2.90 | 50 mA | 250 mA |
| | 100 | 3.00 | 50 mA | 250 mA |
| | 101 | 3.10 | 50 mA | 250 mA |
| | 110 | 3.15 | 50 mA | 250 mA |
| | 111 | 3.30 | 50 mA | 250 mA |

Table 64. VGEN1 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|--------|----------------|-----|-----|-----|------|-------|
|--------|----------------|-----|-----|-----|------|-------|

GENERAL

| | | | | | | |
|---------------------|--|------|-----|------|----|--|
| V_{GEN1IN} | Operating Input Voltage Range V_{INMIN} to V_{INMAX} • All settings | 1.75 | 1.8 | 1.85 | V | |
| I_{GEN1} | Operating Current Load Range I_{LMIN} to I_{LMAX} • Not exceeding PNP max power | 0.0 | - | 250 | mA | |

VGEN1 ACTIVE MODE – DC

| | | | | | | |
|-----------------------|--|------------------------|------------------|------------------------|---------------|--|
| V_{GEN1} | Output Voltage V_{OUT} | $V_{\text{NOM}} - 3\%$ | V_{NOM} | $V_{\text{NOM}} + 3\%$ | V | |
| V_{GEN1LOPP} | Load Regulation • $1.0\text{ mA} < I_L < I_{\text{LMAX}}$ | - | 0.25 | - | mV/mA | |
| V_{GEN1LIPP} | Line Regulation | - | 5.0 | - | mV | |
| I_{GEN1Q} | Active Mode Quiescent Current • $I_L = 0\text{ mA}$ | - | 12 | - | μA | |
| I_{GEN1LIM} | Current Limit • Output voltage forced to $V_{\text{GEN1NOM}}/2$ | - | 375 | - | mA | |

Table 64. VGEN1 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|-------------------------------|---|------|-----|-----|------|-------|
| VGEN1 ACTIVE MODE - AC | | | | | | |
| VGEN1 _{PSRR} | PSRR <ul style="list-style-type: none"> IL = 75% of IL_{MAX} 20 Hz to 20 kHz VGEN1[2:0] = 000-101 IL = 75% of IL_{MAX} 20 Hz to 20 kHz VGEN1[2:0] = 110-111 | - | 50 | - | dB | |
| t _{ON-VGEN1} | Turn-on Time <ul style="list-style-type: none"> Enable to 90% of end value V_{GEN1IN} = V_{INMIN}, V_{INMAX}; IL = 0 mA | - | - | 1.0 | ms | |
| t _{OFF-VGEN1} | Turn-off Time <ul style="list-style-type: none"> Disable to 10% of initial value V_{GEN1IN} = V_{INMIN}, V_{INMAX}; IL = 0mA | 0.01 | - | 10 | ms | |
| VGEN1 _{OS-START} | Start-up Overshoot <ul style="list-style-type: none"> V_{GEN1IN} = V_{INMIN}, V_{INMAX}; IL = 0 mA | - | 1.0 | 2.0 | % | |

VGEN1 ACTIVE MODE - AC (CONTINUED)

| | | | | | | |
|----------------------------------|---|---|-----|-----|----|--|
| VGEN1 _{LO} TRANSIENT | Transient Load Response <ul style="list-style-type: none"> V_{GEN1IN} = V_{INMIN}, V_{INMAX} | - | 1.0 | 2.0 | % | |
| V _{GEN1LI} TRANSIENT | Transient Line Response <ul style="list-style-type: none"> IL = 75% of IL_{MAX} | - | 5.0 | 8.0 | mV | |
| t _{MODE-VGEN1} | Mode Transition Time <ul style="list-style-type: none"> From low-power to active and from active to low-power V_{GEN1IN} = V_{INMIN}, V_{INMAX}; IL = IL_{MAXLP} | - | - | 100 | μs | |
| VGEN1 MODERES | Mode Transition Response <ul style="list-style-type: none"> From low-power to active and from active to low-power V_{GEN1IN} = V_{INMIN}, V_{INMAX}; IL = IL_{MAXLP} | - | 1.0 | 2.0 | % | |

Table 65. VGEN2 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|-------------------------------|---|---------------------------|------------------|-----------------------|-------|-------|
| VGEN2 | | | | | | |
| V _{GEN2IN} | Operating Input Voltage Range V _{INMIN} to V _{INMAX} <ul style="list-style-type: none"> All settings, BP biased | V _{NOM} +0.25 | - | 4.5 | V | |
| V _{GEN2IN} | Extended Input Voltage Range <ul style="list-style-type: none"> BP Biased, Performance may out of specification for output levels VGEN2 [2:0] = 010 to 111 | UVDET | - | 4.5 | mV/mA | |
| I _{GEN2} | Operating Current Load Range IL _{MI} to IL _{MAX} <ul style="list-style-type: none"> Internal Pass FET | 0.0 | - | 50 | mA | |
| I _{GEN2} | Operating Current Load Range IL _{MIN} to IL _{MAX} <ul style="list-style-type: none"> External PNP, Not exceeding PNP max power | 0.0 | - | 250 | mA | |
| VGEN2 ACTIVE MODE - DC | | | | | | |
| V _{GEN2} | Output Voltage V _{OUT} <ul style="list-style-type: none"> Output Voltage V_{OUT} | V _{NOM} - 3% | V _{NOM} | V _{NOM} + 3% | V | |

Table 65. VGEN2 Electrical Specification

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|-----------------------|--|-----|------|-----|---------------|-------|
| V_{GEN2LOPP} | Load Regulation • $1.0\text{ mA} < I_L < I_{L\text{MAX}}$ | - | 0.20 | - | mV/mA | |
| V_{GEN2LIPP} | • Line Regulation | - | 8.0 | - | mV | |
| I_{GEN2Q} | Active Mode Quiescent Current • $I_L = 0$ | - | 30 | - | μA | |

VGEN2 ACTIVE MODE - DC (CONTINUED)

| | | | | | | |
|-------------------------|---|-----|-----|-----|----|------|
| $I_{\text{GEN2DRVLIM}}$ | VGEN2DRV Base Drive Current Limit • External PNP mode only | 2.4 | 3.8 | 5.5 | mA | (60) |
|-------------------------|---|-----|-----|-----|----|------|

VGEN2 LOW-POWER MODE - DC - VGEN2MODE = 1

| | | | | | | |
|--------------------|---|------------------------|------------------|------------------------|---------------|--|
| V_{GEN2} | • Output Voltage V_{OUT} | $V_{\text{NOM}} - 3\%$ | V_{NOM} | $V_{\text{NOM}} + 3\%$ | V | |
| I_{GEN2} | Current Load Range $I_{L\text{MINLP}}$ to $I_{L\text{MAXLP}}$ | 0.0 | - | 3.0 | mA | |
| I_{GEN2Q} | Low-power Mode Quiescent Current • $I_L = 0\text{ mA}$ | - | 8.0 | - | μA | |

VGEN2 ACTIVE MODE - AC

| | | | | | | |
|-------------------------------|--|--------|----------|--------|---------------|--|
| V_{GEN2PSRR} | PSRR $I_L = 75\%$ of $I_{L\text{MAX}}$, 20 Hz to 20 kHz • $V_{\text{GEN2IN}} = V_{\text{INMIN}} + 100\text{ mV}$ • $V_{\text{GEN2IN}} = V_{\text{NOM}} + 1.0\text{ V}$ | - - | 40 50 | - - | dB | |
| $t_{\text{ON-VGEN22}}$ | Turn-on Time • Enable to 90% of end value $V_{\text{GEN2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$; $I_L = 0\text{ mA}$ | - | - | 1.0 | ms | |
| $t_{\text{OFF-VGEN2}}$ | Turn-off Time • Disable to 10% of initial value $V_{\text{GEN2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$; $I_L = 0\text{ mA}$ | 0.05 | - | 10 | ms | |
| $V_{\text{GEN2OS-START}}$ | Start-up Overshoot • $V_{\text{GEN2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$; $I_L = 0\text{ mA}$ | - | 1.0 | 2.0 | % | |
| $V_{\text{GEN2LO-TRANSIENT}}$ | Transient Load Response • $V_{\text{GEN2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$ | - | 1.0 | 2.0 | % | |
| $V_{\text{GEN2LI-TRANSIENT}}$ | Transient Line Response • $I_L = 75\%$ of $I_{L\text{MAX}}$ | - | 5.0 | 8.0 | mV | |
| $t_{\text{MODE-VGEN2}}$ | Mode Transition Time • From low-power to active $V_{\text{GEN2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$; $I_L = I_{L\text{MAXLP}}$ | - | - | 100 | μs | |
| $V_{\text{GEN2MODERES}}$ | Mode Transition Response • From low-power to active and from active to low-power $V_{\text{GEN2IN}} = V_{\text{INMIN}}, V_{\text{INMAX}}$; $I_L = I_{L\text{MAXLP}}$ | - | 1.0 | 2.0 | % | |

Notes

60. V_{GEN2} current limit is given by $I_{\text{GEN2DRVLIM}} \times \beta$ of external PNP transistor

7.6 Analog to Digital Converter

The ADC core is a 10 bit converter, supplied from V_{CORE}. The ADC core and logic run at an internally generated frequency of approximately 1.33 MHz and has an integrated auto calibration circuit which reduces the offset and gain errors.

7.6.1 Input Selector

The ADC has a total of 16 input channels (nine internal and seven external). [Table 66](#) gives an overview of the characteristics of each of these channels.

Table 66. ADC Inputs

| Channel | ADSELx[3:0] | Signal read | Input Level | Scaling | Scaled Version |
|---------|-------------|-------------------|--------------|----------|----------------------|
| 0 | 0000 | Reserved | Reserved | Reserved | Reserved |
| 1 | 0001 | Reserved | Reserved | Reserved | Reserved |
| 2 | 0010 | Reserved | Reserved | Reserved | Reserved |
| 3 | 0011 | Die temperature | -40 – 150 °C | | 1.2 – 2.4 V |
| 4 | 0100 | Reserved | Reserved | Reserved | Reserved |
| 5 | 0101 | Reserved | Reserved | Reserved | Reserved |
| 6 | 0110 | Reserved | Reserved | Reserved | Reserved |
| 7 | 0111 | Reserved | Reserved | Reserved | Reserved |
| 8 | 1000 | Coin cell Voltage | 0 – 3.6 V | X2/3 | 0 – 2.4 V |
| 9 | 1001 | ADIN9 | 0 – 2.4 V | x1 | 0 – 2.4 V |
| 10 | 1010 | ADIN10 | 0 – 2.4 V | x1 | 0 – 2.4 V |
| 11 | 1011 | ADIN11 | 0 – 2.4 V | x1 | 0 – 2.4 V |
| 12 | 1100 | ADIN12/TSX1 | 0 – 2.4 V | x1/x2 | 0 – 2.4 V / 0 -1.2 V |
| 13 | 1101 | ADIN13/TSX2 | 0 – 2.4 V | x1/x2 | 0 – 2.4 V / 0 -1.2 V |
| 14 | 1110 | ADIN14/TSY1 | 0 – 2.4 V | x1/x2 | 0 – 2.4 V / 0 -1.2 V |
| 15 | 1111 | ADIN15/TSY2 | 0 – 2.4 V | x1/x2 | 0 – 2.4 V / 0 -1.2 V |

Some of the internal signals are first scaled to adapt the signal range to the input range of the ADC. For details on scaling, see [Dedicated Readings](#).

Table 67. ADC Input Specification

| Parameter | Condition | Min | Typ | Max | Units |
|------------------|---------------------------------|-----|-----|-----|-------|
| Source Impedance | No bypass capacitor at input | - | - | 5.0 | kOhm |
| | Bypass capacitor at input 10 nF | - | - | 30 | kOhm |

When considerably exceeding the maximum input of the ADC at the scaled or unscaled inputs, the reading result will return a full scale. It has to be noted however, that this full scale does not necessarily yield a 1022 DEC reading due to the offsets and calibration applied. The same applies for when going below the minimum input where the corresponding 0000 DEC reading may not be returned.

7.6.2 Control

The ADC parameters are programmed by the processor via the SPI. When a reading sequence is finished, an interrupt ADCDONEI is generated. The interrupt can be masked with the ADCDONEM bit.

The ADC is enabled by setting ADEN bit high, then the ADC can start a series of conversions through SPI programming by setting the ADSTART bit. If the ADEN bit is low, the ADC will be disabled and in low-power mode. The ADC is automatically calibrated every time PMIC is powered.

The conversions will begin after a small analog synchronization of up to 30 microseconds, plus a programmable delay from 0 (default) up to 600 μ s, by programming the bits ADDLY1[3:0]. The ADDLY2[3:0] controls the delay between each of the conversions from 0 to 600 μ s. ADDLY3[3:0] controls the delay after the final conversion, and is only valid when ADCONT is high. ADDLY1, 2, and 3 are set to 0 by default.

Table 68. ADDLYx[3:0]

| ADDLYx[3:0] | Delay in μ s |
|-------------|------------------|
| 0000 | 0.0 |
| 0001 | 40 |
| 0010 | 80 |
| 0011 | 120 |
| 0100 | 160 |
| 0101 | 200 |
| 0110 | 240 |
| 0111 | 280 |
| 1000 | 320 |
| 1001 | 360 |
| 1010 | 400 |
| 1011 | 440 |
| 1100 | 480 |
| 1101 | 520 |
| 1110 | 560 |
| 1111 | 600 |

There is a max of 8 conversions that will take place when the ADC is started. The register ADSELx[3:0] selects the channel which the ADC will read and store in the ADRESULTx register. The ADC will always start at the channel indicated in ADSEL0, and read up to and including the channel set by the ADSTOP[2:0] bits. For example, when ADSTOP[2:0] = 010, it will request the ADC to read channels indicated in ADSEL0, ADSEL1, and ADSEL2. When ADSTOP[2:0] = 111, all eight channels programmed by the value in ADSEL0-7 will be read. When the ADCONT bit is set high, it allows the ADC to continuously loop and read the channels from address 0 to the stop address programmed in ADSTOP. By default, the ADCONT is set low (disabled). In the continuous mode, the ADHOLD bit will allow the software to hold the ADC sequencer from updating the results register while the ADC results are read. Once the sequence of A/D conversions is complete, the ADRESULTx results are stored in four SPI registers (ADC 4 - ADC 7).

7.6.3 Dedicated Readings

7.6.3.1 Channel 0 to 2 Reserved

Channel 0 to Channel 2 are reserved.

7.6.3.2 Channel 3 Die Temperature

The relation between the read out code and temperature is given in [Table 69](#).

Table 69. Die Temperature Voltage Reading

| Parameter | Min | Typ | Max | Unit |
|--|-----|--------|-----|---------|
| Die temperature read out code at 25 °C | - | 680 | - | Decimal |
| Slope temperature change per LSB | - | +0.426 | - | °C/LSB |
| Slope error | - | - | 5.0 | % |

The actual die temperature is obtained as follows: Die Temp = 25 + 0.426 * (ADC Code - 680)

7.6.3.3 Channel 4 to 7 Reserved

Channel 4 to Channel 7 are reserved.

7.6.3.4 Channel 8 Coin Cell Voltage

The voltage of the coin cell connected to the LICELL pin can be read on channel 8. Since the voltage range of the coin cell exceeds the input voltage range of the ADC, the LICELL voltage is scaled as $V(\text{LICELL}) * 2/3$. In case the voltage at LICELL drops below the coin cell disconnect threshold, the voltage at LICELL can still be read through the ADC.

Table 70. Coin Cell Voltage Reading Coding

| Conversion Code ADRESULTx[9:0] | Voltage at ADC input (V) | Voltage at LICELL (V) |
|-----------------------------------|--------------------------|-----------------------|
| 1 111 111 110 | 2.400 | 3.6 |
| 1 000 000 000 | 1.200 | 1.8 |
| 0 000 000 000 | 0.000 | 0 |

7.6.3.5 Channel 9-11 ADIN9-ADIN11

There are three general purpose analog input channels that can be measured through the ADIN9-ADIN11 pins.

7.6.3.6 Channel 12-15 ADIN12-ADIN15

If the touch screen is not used, the inputs TSX1, TSX2, TSY1, and TSY2 can be used as general purpose inputs. They are respectively mapped on ADC channels 12, 13, 14, and 15.

7.6.4 Touch Screen Interface

The touch screen interface provides all circuitry required for the readout of a four-wire resistive touch screen. The touch screen X plate is connected to TSX1 and TSX2, while the Y plate is connected to TSY1 and TSY2. A local supply TSREF will serve as a reference. Several readout possibilities are offered.

If the touchscreen is not used, the inputs TSX1, TSX2, TSY1, and TSY2 can be used as general purpose ADC inputs. They are respectively mapped on ADC channels 12, 13, 14, and 15.

Touch Screen Pen detection bias can be enabled via the TSPENDETEN bit in the AD0 register. When this bit is enabled and a pen touch is detected, the TSPENDET bit in the Interrupt STATUS 0 register is set and the INT pin is asserted - unless the interrupt is masked. Pen detection is only active when TSEN is low.

The reference for the touch screen (Touch Bias) is TSREF and is powered from VCORE. During touch screen operation, TSREF is a dedicated regulator. No loads other than the touch screen should be connected here. When the ADC performs non touch screen conversions, the ADC does not rely on TSREF and the reference is disabled.

The readouts are designed such that the on chip switch resistances are of no influence on the overall readout. The readout scheme does not account for contact resistances, as present in the touch screen connectors. The touch screen readings will have to be calibrated by the user or the factory, where one has to point with a stylus to the opposite corners of the screen. When reading the X-coordinate, the 10-bit ADC reading represents a 10-bit coordinate, with '0' for a coordinate equal to X-, and full scale '1023' when equal to X+. When reading the Y-coordinate, the 10-bit ADC reading represents a 10-bit coordinate, with '0' for a coordinate equal to Y-, and full scale '1023' when equal to Y+. When reading contact resistance, the 10-bit ADC reading represents the voltage drop over the contact resistance created by the known current source multiplied by 2.

The X-coordinate is determined by applying TSREF over the TSX1 and TSX2 pins, while performing a high-impedance reading on the Y-plate through TSY1. The Y-coordinate is determined by applying TSREF between TSY1 and TSY2, while reading the TSX1 pin. The contact resistance is measured by applying a known current into the TSY1 pin of the touch screen and through the TSX2 pin, which is grounded. The voltage difference between the two remaining terminals TSY2 and TSX1 is measured by the ADC, and equals the voltage across the contact resistance. Measuring the contact resistance helps determine if the touch screen is touched with a finger or a stylus.

The TSSELx[1:0] allows the application processor to select its own reading sequence. The TSSELx[1:0] determines what is read during the touch screen reading sequence, as shown in [Table 71](#). The touch screen will always start at TSSEL0 and read up to and including the channel set by TSSEL at the TSSTOP[2:0] bits. For example when TSSTOP[2:0] = 010, it will request the ADC to read channels indicated in TSSEL0, TSSEL1, and TSSEL2. When TSSTOP[2:0] = 111, all eight addresses will be read.

Table 71. Touch Screen Action Select

| TSSELx[1:0] | Signals Sampled |
|-------------|------------------------------|
| 00 | Dummy to discharge TSREF cap |
| 01 | X - plate |
| 10 | Y - plate |
| 11 | Contact |

The touch screen readings can be repeated, as in the following example readout sequence, to reduce the interrupt rate and to allow for easier noise rejection. The dummy conversion inserted between the different readings allows the references in the system to be pre-biased for the change in touch screen plate polarity. It will read as '0'.

A touch screen reading will take precedence over an ADC sequence. If an ADC reading is triggered during a touch screen event, the ADC sequence will be overwritten by the touch screen data.

The first touch screen conversion can be delayed from 0 (default) to 600 μ s by programming the TSDLY1[3:0] bits. The TSDLY2[3:0] controls the delay between each of the touch screen conversions from 0 to 600 μ s. TSDLY[2:0] sets the delay after the last address is converted. TSDLY1, 2, and 3 are set to 0 by default.

Table 72. TSDLYx[3:0]

| TSDLYx[3:0] | Delay in μ S |
|-------------|------------------|
| 0000 | 0 |
| 0001 | 40 |
| 0010 | 80 |
| 0011 | 120 |
| 0100 | 160 |

Table 72. TSDLYx[3:0]

| TSDLYx[3:0] | Delay in μs |
|-------------|------------------------|
| 0101 | 200 |
| 0110 | 240 |
| 0111 | 280 |
| 1000 | 320 |
| 1001 | 360 |
| 1010 | 400 |
| 1011 | 440 |
| 1100 | 480 |
| 1101 | 520 |
| 1110 | 560 |
| 1111 | 600 |

To perform a touch screen reading, the processor must do the following:

1. Enable the touch screen with TSEN
2. Select the touch screen sequence by programming the TSSEL0-TSSEL7 SPI bits.
3. Program the TSSTOP[2:0]
4. Program the delay between the conversion via the TSDLY1 and TSDLY2 settings.
5. Trigger the ADC via the TSSTART SPI bit
6. Wait for an interrupt indicating the conversion is done TSDONEI
7. And then read out the data in the ADRESULTx registers

7.6.5 ADC Specifications

Table 73. ADC Electrical Specifications

Characteristics noted under conditions BP = 3.6 V, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$, unless otherwise noted. Typical values at BP = 3.6 V and $T_A = 25\text{ }^{\circ}\text{C}$ under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|-------------------------|---|-------------|--------|------------|---------------|-------|
| ADC | | | | | | |
| I_{CONVERT} | Conversion Current | - | 1.0 | - | mA | |
| V_{ADCIN} | Converter Core Input Range <ul style="list-style-type: none"> • Single-ended voltage readings • Differential readings | 0.0 -1.2 | - - | 2.4 1.2 | V | |
| t_{CONVERT} | Conversion Time per channel | - | - | 10 | μs | |
| | Integral Non-linearity | - | - | 3 | LSB | |
| | Differential Non-linearity | - | - | 1 | LSB | |
| | Zero Scale Error (Offset) | - | - | ± 5 | LSB | |
| | Full Scale Error (Gain) | - | - | ± 10 | LSB | |
| | Drift Over-temperature | - | - | 10 | LSB | |
| $t_{\text{ON-OFF-ADC}}$ | Turn On/Off Time | - | - | 31 | μs | |

7.7 Auxiliary Circuits

7.7.1 General Purpose I/Os

The 34709 contains four configurable GPIO input/outputs for general purpose use. When configured as outputs, they can be configured as open-drain (OD) or CMOS (push-pull outputs). These GPIOs are low-voltage capable (1.2 or 1.8 V). In open-drain configuration these outputs can only be pulled up to 2.5 V maximum.

Each individual GPIO has a dedicated 16-bit control register. [Table 74](#) provides the detailed bit descriptions.

Table 74. GPIOLVx Control ⁽⁶¹⁾

| SPI Bit | Description |
|-----------|--|
| DIR | GPIOLVx direction 0: Input (default) 1: Output |
| DIN | Input state of the GPIOLVx pin 0: Input low 1: Input High |
| DOUT | Output state of GPIOLVx pin 0: Output Low 1: Output High |
| HYS | Hysteresis 0: CMOS in 1: Hysteresis (default) |
| DBNC[1:0] | GPIOLVx input debounce time 00: no debounce (default) 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce |
| INT[1:0] | GPIOLVx interrupt control 00: None (default) 01: Falling edge 10: Rising edge 11: Both edges |
| PKE | Pad keep enable 0: Off (default) 1: On |
| ODE | Open-drain enable 0: CMOS (default) 1: OD |
| DSE | Drive strength enable 0: 4.0 mA (default) 1: 8.0 mA |
| PUE | Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default) |
| PUS[1:0] | Pull-up/Pull-down enable 00: 10 K active pull-down 01: 10 K active pull-up 10: 100 K active pull-down 11: 100 K active pull-up (default) |

Table 74. GPIOLVx Control ⁽⁶¹⁾

| SPI Bit | Description |
|----------|---|
| SRE[1:0] | Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast |

Notes

61. x= 0, 1, 2, or 3 depending of the GPIO channel it is being used

7.7.2 PWM Outputs

There are two PWM outputs on the 34709 PWM1 and PWM2 and which are controlled by the PWMxDUTY and PWMxCLKDIV registers shown in [Table 75](#). The base clock will be the 2.0 MHz divided by 32.

Table 75. PWMx Duty Cycle Programming

| PWMxDC[5:0] ⁽⁶²⁾ | Duty Cycle |
|-----------------------------|------------------------|
| 000000 | 0/32, Off (default) |
| 000001 | 1/32 |
| ... | ... |
| 010000 | 16/32 |
| ... | ... |
| 011111 | 31/32 |
| 1xxxxx | 32/32, Continuously On |

Notes

62. "x" represent 1 and 2

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Table 76. PWMx Clock Divider Programming

| PWMxCLKDIV[5:0] ⁽⁶³⁾ | Duty Cycle |
|---------------------------------|-----------------|
| 000000 | Base Clock |
| 000001 | Base Clock / 2 |
| ... | ... |
| 001111 | Base Clock / 16 |
| ... | ... |
| 111111 | Base Clock / 64 |

Notes

63. "x" represent 1 and 2

7.8 Serial Interfaces

The IC contains a number of programmable registers for control and communication. The majority of registers are accessed through a SPI interface in a typical application. The same register set may alternatively be accessed with an I²C interface that is muxed on SPI pins. [Table 77](#) describes the muxed pin options for the SPI and I²C interfaces; further details for each interface mode follow.

Table 77. SPI / I²C Bus Configuration

| Pin Name | SPI Mode Functionality | I ² C Mode Functionality |
|----------|---|--------------------------------------|
| CS | Configuration ⁽⁶⁴⁾ , Chip Select | Configuration ⁽⁶⁵⁾ |
| CLK | SPI Clock | SCL: I ² C bus clock |
| MISO | Master In, Slave Out (data output) | SDA: Bi-directional serial data line |
| MOSI | Master Out, Slave In (data input) | A0 Address selection ⁽⁶⁶⁾ |

Notes

- 64. CS held low at Cold Start, configures the interface for SPI mode; once activated, CS functions as the SPI Chip Select.
- 65. CS tied to VCOREDIG at Cold Start, configures the interface for I²C mode; the pin is not used in I²C mode, other than for configuration.
- 66. In I²C mode, the MOSI pin is hardwired to ground, or VCOREDIG is used to select between two possible addresses.

7.8.1 SPI Interface

The SPI interface port allows access by a processor to the register set. Via these registers the resources of the IC can be controlled. The registers also provide status information about how the IC is operating, as well as information on external signals.

Because the SPI interface pins can be reconfigured for reuse as an I²C interface, a configuration protocol mandates that the CS pin is held low during a turn on event for the IC (a weak pull-down is integrated on the CS pin). The state of CS is latched in during the initialization phase of a Cold Start sequence, ensuring that the I²C bus is configured before the interface is activated. With the CS pin held low during start-up (as would be the case if connected to the CS driver of an unpowered processor due to the integrated pull-down), then the bus configuration will be latched for SPI mode.

The SPI port utilizes 32-bit serial data words comprised of 1 write/read_b bit, 6 address bits, 1 null bit, and 24 data bits. The addressable register map spans 64 registers of 24 data bits each. The map is not fully populated, but it follows the legacy conventions for bit positions corresponding to common functionality with previous generation FSL products.

7.8.1.1 SPI Interface Description

For a SPI read, the first bit sent to the IC must be a zero indicating a SPI read cycle. Next, the six bit address is sent MSB first. This is followed by one dead bit to allow for more address decode time. The 34709 will clock the above bits in on the rising edge of the SPI clock. Then the 24 data bits are driven out on the MISO pin on the falling edge of the SPI clock so the master can clock them in on the rising edge of the SPI clock.

For each MOSI SPI transfer, first a one is written to the write/read_b bit if this SPI transfer is to be a write. A zero is written to the write/read_b bit if this is to be a read command. If a zero is written, then any data sent after the address bits are ignored and the internal contents of the field addressed do not change when the 32nd CLK is sent.

For a SPI write the first bit sent to the 34709 must be a one indicating a SPI write cycle. Next the six bit address is sent MSB first. This is followed by one dead bit to allow for more address decode time. Then the data is sent MSB first. The SPI data is written to the SPI register whose address was sent at the start of the SPI cycle on the falling edge of the 32nd SPI clock. Additionally, whenever a SPI write cycle is taking place the SPI read data is shifted out for the same address as for the write cycle. Next the 6-bit address is written, MSB first. Finally, data bits are written, MSB first. Once all the data bits are written then the data is transferred into the actual registers on the falling edge of the 32nd CLK.

The CS polarity is active high. The CS line must remain high during the entire SPI transfer. For a write sequence it is possible for the written data to be corrupted, if after the falling edge of the 32nd clock the CS goes low before it's required time. CS can go low before this point and the SPI transaction will be ignored, but after that point the write process is started and cannot be stopped because the write strobe pulse is already being generated and CS going low may cause a runt pulse that may or may not be wide

enough to clock all 24 data bits properly. To start a new SPI transfer, the CS line must be toggled low and then pulled high again. The MISO line will be tri-stated while CS is low.

The register map includes bits that are read/write, read only, read/write “1” to clear (i.e., Interrupts), and clear on read, reserved, and unused. Refer to the [SPI/I2C Register Map](#) and the individual subcircuit descriptions to determine the read/write capability of each bit. All unused SPI bits in each register must be written to as zeroes. A SPI read back of the address field and unused bits are returned as zeroes. To read a field of data, the MISO pin will output the data field pointed to by the 6 address bits loaded at the beginning of the SPI sequence.

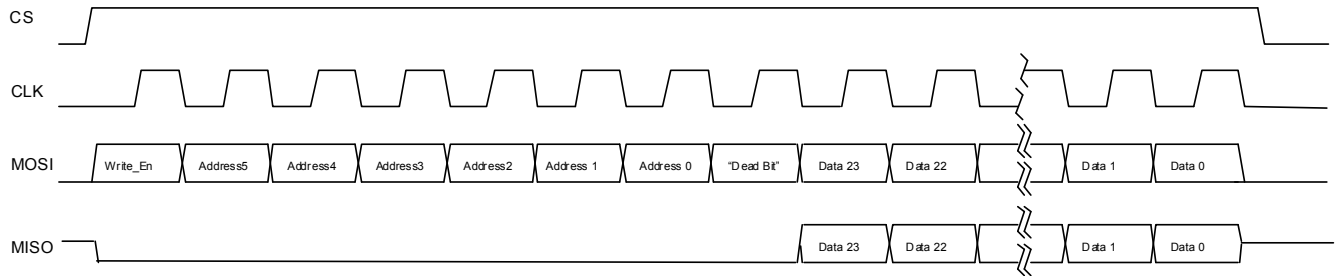


Figure 19. SPI Transfer Protocol Single Read/Write Access

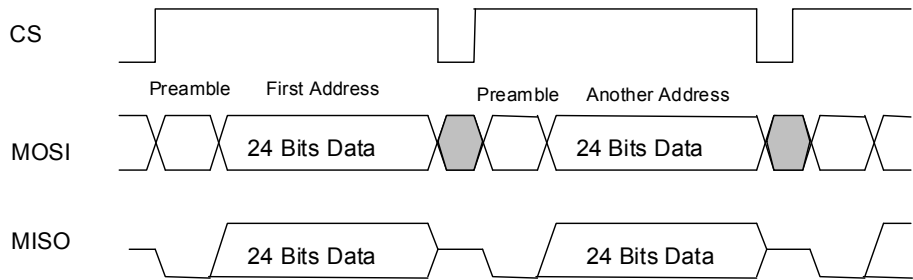


Figure 20. SPI Transfer Protocol Multiple Read/Write Access

7.8.1.2 SPI Timing Requirements

[Figure 21](#) and [Table 78](#) summarize the SPI timing requirements. The SPI input and output levels are set via the SPIVCC pin, by connecting it to the desired supply. This would typically be tied to SW5 and programmed for 1.80 V. The strength of the MISO driver is programmable through the SPIDRV [1:0] bits. See [Table 79](#) for detailed SPI electrical characteristics.

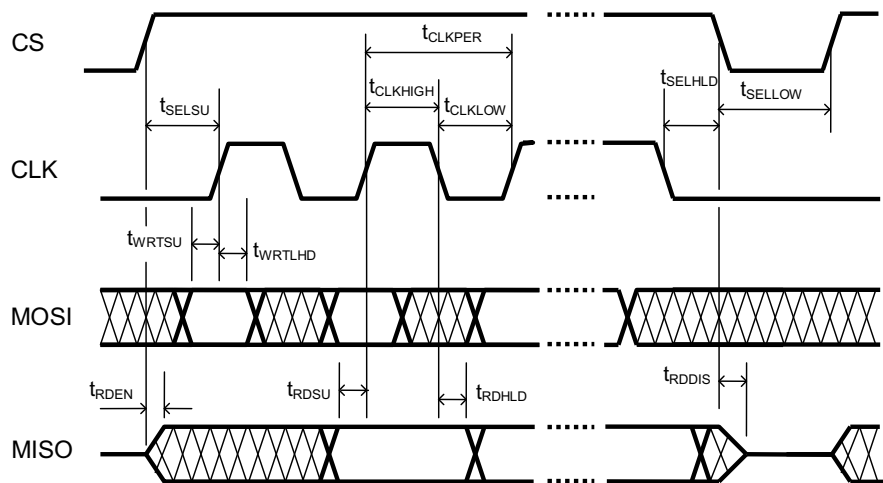


Figure 21. SPI Interface Timing Diagram

Table 78. SPI Interface Timing Specifications⁽⁶⁷⁾

| Parameter | Description | t _{MIN} (ns) |
|----------------------|---|-----------------------|
| t _{SELSU} | Time CS has to be high before the first rising edge of CLK | 15 |
| t _{SELHLD} | Time CS has to remain high after the last falling edge of CLK | 15 |
| t _{SELLOW} | Time CS has to remain low between two transfers | 15 |
| t _{CLKPER} | Clock period of CLK | 38 |
| t _{CLKHIGH} | Part of the clock period where CLK has to remain high | 15 |
| t _{CLKLOW} | Part of the clock period where CLK has to remain low | 15 |
| t _{WRTSU} | Time MOSI has to be stable before the next rising edge of CLK | 4.0 |
| t _{WRTHLD} | Time MOSI has to remain stable after the rising edge of CLK | 4.0 |
| t _{RDSU} | Time MISO will be stable before the next rising edge of CLK | 4.0 |
| t _{RDHLD} | Time MISO will remain stable after the falling edge of CLK | 4.0 |
| t _{RDEN} | Time MISO needs to become active after the rising edge of CS | 4.0 |
| t _{RDDIS} | Time MISO needs to become inactive after the falling edge of CS | 4.0 |

Notes

67. This table reflects a maximum SPI clock frequency of 26 MHz.

7.8.2 I²C Interface

7.8.2.1 I²C Configuration

When configured for I²C mode, the interface may be used to access the complete register map previously described for SPI access. Since SPI configuration is more typical, references within this document will generally refer to the common register set as a “SPI map” and bits as “SPI bits”; however, it should be understood that access reverts to I²C mode when configured as such.

The SPI pins CLK and MISO are reused for the SCL and SDA lines respectively. Selection of I²C mode for the interface is configured by hard-wiring the CS pin to VCOREDIG on the application board. The state of CS is latched during the initialization phase of a Cold Start sequence, so the CS bit is defined for bus configuration before the interface is activated. The pull-down on CS will be deactivated if the high state is detected (indicating I²C mode).

In I²C mode, the MISO pin is connected to the bus as an open-drain driver, and the logic level is set by an external pull-up. The part can function only as an I²C slave device, not as a host.

7.8.2.2 I²C Device ID

I²C interface protocol requires a device ID for addressing the target IC on a multi-device bus. To allow flexibility in addressing for bus conflict avoidance, pin programmable selection is provided to allow configuration for the address LSB(s). This product supports 7-bit addressing only; support is not provided for 10-bit or general Call addressing.

Because the MOSI pin is not utilized for I²C communication, it is reassigned for pin programmable address selection by hardwiring to VCOREDIG or GND at the board level when configured for I²C mode. MOSI will act as Bit 0 of the address. The I²C address assigned to FSL PM ICs (shared amongst our portfolio) is given as follows:

00010-A1-A0, the A1 and A0 bits are allowed to be configured for either 1 or 0. The A1 address bit is internally hardwired as a “0”, leaving the LSB A0 for board level configuration. The designated address then is defined as: 000100-A0.

7.8.2.3 I²C Operation

The I²C mode of the interface is implemented generally following the Fast Mode definition which supports up to 400 kbits/s operation. (Exceptions to the standard are noted to be 7-bit only addressing, and no support for general Call addressing) Timing diagrams, electrical specifications, and further details on this bus standard, is available on the internet, by typing "I²C specification" in the web search string field.

Standard I²C protocol utilizes bytes of eight bits, with an acknowledge bit (ACK) required between each byte. However, the number of bytes per transfer is unrestricted. The register map is organized in 24-bit registers which corresponds to the 24-bit words supported by the SPI protocol of this product. To ensure that I²C operation mimics SPI transactions in behavior of a complete 24-bit word being written in one transaction, software is expected to perform write transactions to the device in 3-byte sequences, beginning with the MSB. Internally, data latching will be gated by the acknowledge at the completion of writing the third consecutive byte.

Failure to complete a 3-byte write sequence will abort the I²C transaction and the register will retain its previous value. This could be due to a premature STOP command from the master, for example.

I²C read operations are also performed in byte increments separated by an ACK. Read operations also begin with the MSB and 3-bytes will be sent out unless a STOP command or NACK is received prior to completion.

The following examples show how to write and read data to the IC. The host initiates and terminates all communication. The host sends a master command packet after driving the start condition. The device will respond to the host if the master command packet contains the corresponding slave address. In the following examples, the device is shown always responding with an ACK to transmissions from the host. If at any time a NAK is received, the host should terminate the current transaction and retry the transaction.

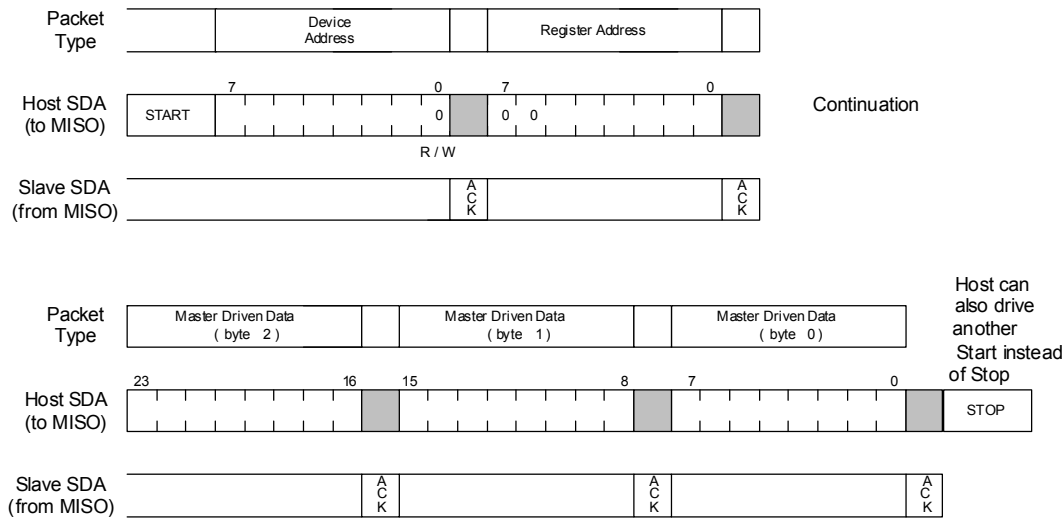


Figure 22. I²C 3-byte Write Example

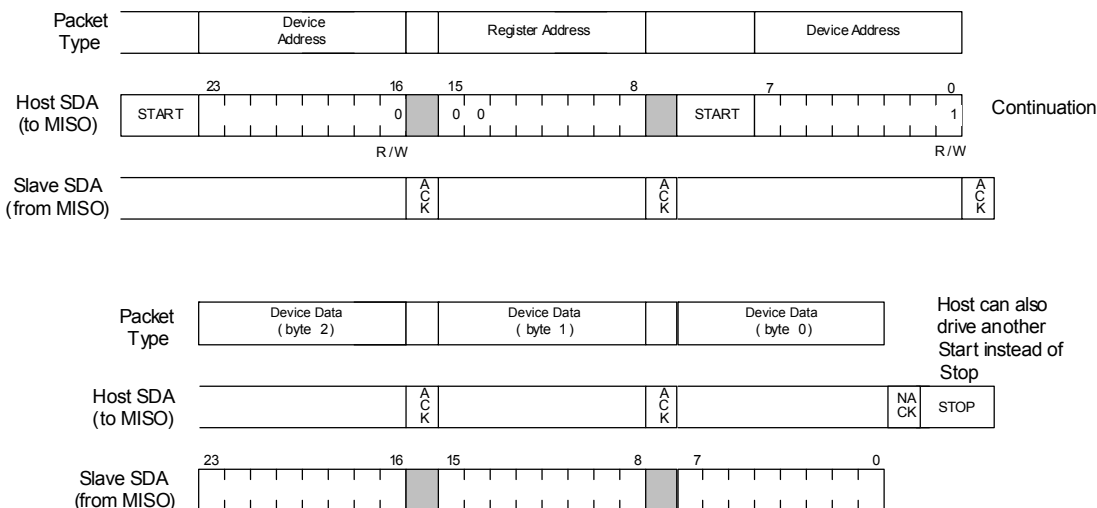


Figure 23. I²C 3-byte Read Example

7.8.3 SPI/I²C Specification

Table 79. SPI/I²C Electrical Characteristics

Characteristics noted under conditions BP = 3.6 V, -40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values at BP = 3.6 V and T_A = 25 °C under nominal conditions, unless otherwise noted.

| Symbol | Characteristic | Min | Typ | Max | Unit | Notes |
|---|---|------------------|--------------------------|------------------|------|-------|
| SPI Interface Logic IO | | | | | | |
| V _{INCSLO} | Input Low CS | 0.0 | - | 0.4 | V | |
| V _{INCSHI} | Input High CS | 1.1 | - | SPIVCC+0.3 | V | |
| V _{INMOSILO} / V _{INCLKLO} | Input Low, MOSI, CLK | 0.0 | - | 0.3*SPIVCC | V | |
| V _{INMOSIHI} / V _{INCLKHI} | Input High, MOSI, CLK | 0.7*SPIVCC | - | SPIVCC+0.3 | V | |
| V _{MISOLO} / V _{INTLO} | Output Low MISO, INT • Output sink 100 μA | 0.0 | - | 0.2 | V | |
| V _{MISOHI} / V _{INTHI} | Output High MISO, INT • Output source 100 μA | SPIVCC-0.2 | - | SPIVCC | V | |
| V _{CC-SPI} | SPIVCC Operating Range | 1.75 | - | 3.6 | V | |
| t _{MISOET} | MISO Rise and Fall Time, CL = 50 pF, SPIVCC = 1.8 V • SPIDRV [1:0] = 00 • SPIDRV [1:0] = 01 (default) • SPIDRV [1:0] = 10 • SPIDRV [1:0] = 11 | - - - - | 6.0 2.5 3.0 2.0 | - - - - | ns | |

7.9 Configuration Registers

7.9.1 Register Set structure

The general structure of the register set is given in [Table 80](#). Expanded bit descriptions are included in the following functional sections for application guidance. For brevity's sake, references are occasionally made herein to the register set as the "SPI map" or "SPI bits", but note that bit access is also possible through the I²C interface option so such references are implied as generically applicable to the register set accessible by either interface.

Table 80. Register Set

| | Register | | Register | | Register | | Register |
|----|-----------------------|----|---------------------------|----|------------------|----|-----------------|
| 0 | Interrupt Status 0 | 16 | Memory A | 32 | Regulator Mode 0 | 48 | ADC5 |
| 1 | Interrupt Mask 0 | 17 | Memory B | 33 | GPIOLV0 Control | 49 | ADC6 |
| 2 | Interrupt Sense 0 | 18 | Memory C | 34 | GPIOLV1 Control | 50 | ADC7 |
| 3 | Interrupt Status 1 | 19 | Memory D | 35 | GPIOLV2 Control | 51 | Reserved |
| 4 | Interrupt Mask 1 | 20 | RTC Time | 36 | GPIOLV3 Control | 52 | Supply Debounce |
| 5 | Interrupt Sense 1 | 21 | RTC Alarm | 37 | Reserved | 53 | Reserved |
| 6 | Power Up Mode Sense | 22 | RTC Day | 38 | Reserved | 54 | Reserved |
| 7 | Identification | 23 | RTC Day Alarm | 39 | Reserved | 55 | PWM Control |
| 8 | Regulator Fault Sense | 24 | Regulator 1 A/B Voltage | 40 | Reserved | 56 | Unused |
| 9 | Reserved | 25 | Regulator 2 & 3 Voltage | 41 | Unused | 57 | Unused |
| 10 | Reserved | 26 | Regulator 4 A/B Voltage | 42 | Unused | 58 | Unused |
| 11 | Reserved | 27 | Regulator 5 Voltage | 43 | ADC 0 | 59 | Unused |
| 12 | Unused | 28 | Regulator 1 & 2 Mode | 44 | ADC 1 | 60 | Unused |
| 13 | Power Control 0 | 29 | Regulator 3, 4 and 5 Mode | 45 | ADC 2 | 61 | Unused |
| 14 | Power Control 1 | 30 | Regulator Setting 0 | 46 | ADC 3 | 62 | Unused |
| 15 | Power Control 2 | 31 | SWBST Control | 47 | ADC4 | 63 | Unused |

7.9.2 Specific Registers

7.9.2.1 IC and Version Identification

The IC and other version details can be read via the identification bits. These are hardwired on the chip and described in [Table 81](#).

Table 81. IC Revision Bit Assignment

| Identifier | Value | Purpose |
|----------------------|-------|--|
| FULL_LAYER_REV[2:0] | XXX | Represents the full mask revision Pass 1.0 = 001 |
| METAL_LAYER_REV[2:0] | XXX | Represents the full Metal revision Pass 1.1 = 001 Pass 1.2 = 010 |
| FIN[2:0] | 000 | Options within same Reticle Pass 1.0 = 000 |
| FAB[2:0] | 000 | Wafer manufacturing facility Pass 1.0 = 000 |

7.9.2.2 Embedded Memory

There are four register banks of general purpose embedded memory to store critical data. The data written to MEMA[23:0], MEMB[23:0], MEMC[23:0], and MEMD[23:0] is maintained by the coin cell when the main battery is deeply discharged, removed, or contact-bounced (i.e., during a power cut). The contents of the embedded memory are reset by RTCPORB. A known pattern can be maintained in these registers to validate confidence in the RTC contents when power is restored after a power cut event. Alternatively, the banks can be used for any system need for bit retention with coin cell backup.

7.9.3 SPI/I²C Register Map

The complete SPI bitmap is given in [Table 82](#).

Table 82. SPI/I²C Register Map

| Register Types | | Register Values | Reset |
|----------------|---------------------|-----------------|---|
| R/W | Read / Write | 0 = low | Bits Loaded at Cold Start based on PUMS Value |
| R/W/M | Read / Write Modify | 1 = High | Bits Reset by POR or Global Reset |
| W1C | Write One to Clear | X = Variable | RESETB / Green Reset Bits Reset by POR or Global or Green Reset |
| RO | Read Only | | Bits Reset by RTCPORB or Global Reset |
| NU | Not Used | | Bits Reset by POR or OFFB |
| | | | Bits Reset by RTCPORB Only |

| Address | Register Name | Type | Default | 34709 SPI Register Map Rev 0.1 | | | | | | | |
|---------|--|------|-----------|--------------------------------|------------|-----------|-----------|-----------|-----------|----------|----------|
| 0x00 | Interrupt Status 0 Table 83 | W1C | h00_00_00 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | LOWBATT | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x01 | Interrupt Mask 0 Table 84 | R/W | h00_20_07 | - | - | - | - | - | TSPENDET | TSDONEI | ADCDONEI |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | LOWBATTM | - | - | - | - | - |
| 0x02 | Reserved Table 85 | NU | h00_00_00 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | - | - | - | - | TSPENDETM | TSDONEM | ADCDONEM |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| 0x03 | Interrupt Status 1 Table 86 | W1C | h40_80_80 | - | - | - | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | BATTDETBI | - | GPIOLV3I | GPIOLV2I | GPIOLV1I | GPIOLV0I | SCPI |
| 0x04 | Interrupt Mask 1 Table 87 | R/W | h5F_FF_FB | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | CLKI | THERM130 | THERM125 | THERM120 | THERM110 | MEMHLDI | WARMI | PCI |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | RTCRSTI | SYSRSTI | WDIRESTI | PWRON2I | PWRON1I | - | TODAI | 1HZI |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| 0x04 | Interrupt Mask 1 Table 87 | R/W | h5F_FF_FB | - | BATTDETBIM | - | GPIOLV3M | GPIOLV2M | GPIOLV1M | GPIOLV0M | SCPM |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | CLKM | THERM130M | THERM125M | THERM120M | THERM110M | MEMHLDLM | WARMM | PCM |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | RTCRSTM | SYSRSTM | WDIRESTM | PWRON2M | PWRON1M | - | TODAM | 1HZM |

| | | | | | | | | | | | |
|--------------|---|-----|-----------|-----------------|-------------|---------------------|--------------|------------|----------------------|----------------|-----------|
| 0x05 | Interrupt Sense 1 Table 88 | RO | hXX_XX_XX | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | GPIOLV3S | GPIOLV2S | GPIOLV1S | GPIOLV0S | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | CLKS | THERM130S | THERM125S | THERM120S | THERM110S | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x06 | Power Up Mode Sense Table 89 | RO | h00_00_XX | - | - | - | PWRON2S | PWRON1S | - | - | - |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | - | - |
| 0x07 | Identification Table 90 | RO | h00_0X_XX | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | - | PUMS5S | PUMS4S | PUMS3S | PUMS2S | PUMS1S | ICTESTS |
| | | | | PAGE[4:0] | | | | | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | FAB[2:0] | | | FIN[2] |
| 0x08 | Regulator Fault Sense Table 91 | RO | h00_XX_XX | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | FIN[1:0] | | FULL_LAYER_REV[2:0] | | | METAL_LAYER_REV[2:0] | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | REGSCPEN | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| 0x09 To 0x0C | Unused | NU | h00_00_00 | - | - | - | VGEN2FAULT | VGEN1FAULT | VDACFAULT | VUSB2FAULT | VUSBFAULT |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | SWBSTFAULT | SW5FAULT | SW4BFAULT | SW4AFAULT | SW3FAULT | SW2FAULT | RSVD | SW1FAULT |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| 0x0D | Power Control 0 Table 94 | R/W | h00_00_40 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | PCUTXPB | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | CLK32KMCUEN | USEROFFCLK | DRM | USEROFFSPI | WARMEN | PCCOUNTEN | PCEN |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| 0x0E | Power Control 1 Table 95 | R/W | h00_00_00 | COINCHEN | VCOIN[2:0] | | | - | - | - | - |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x0F | Power Control 2 Table 96 | R/W | h42_23_00 | PCMAXCNT[3:0] | | | PCCOUNT[3:0] | | | | |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | PCT[7:0] | | | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| 0x0F | Power Control 2 Table 96 | R/W | h42_23_00 | STBYDLY[1:0] | | ON_STBY_LP | - | - | CLKDRV[1:0] | | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | SPIDRV[1:0] | | WDIRESET | - | STANDBYINV | GLBRSTTMR[1:0] | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | PWRON2DBNC[1:0] | | PWRON1BDBNC[1:0] | | - | PWRON2RSTEN | PWRON1RSTEN | RESTARTEN |

| | | | | | | | | | | | |
|------|--|-----|-----------|-----------------|------------|-------------|-------|-------|-------|-------|----------|
| 0x10 | Memory A Table 97 | R/W | h00_00_00 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | MEMA[23:16] | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | MEMA[15:8] | | | | | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x11 | Memory B Table 98 | R/W | h00_00_00 | MEMA[7:0] | | | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | MEMB[23:16] | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | MEMB[15:8] | | | | | | | |
| 0x12 | Memory C Table 99 | R/W | h00_00_00 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | MEMB[7:0] | | | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | MEMC[23:16] | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| 0x13 | Memory D Table 100 | R/W | h00_00_00 | MEMC[15:8] | | | | | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | MEMC[7:0] | | | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | MEMD[23:16] | | | | | | | |
| 0x14 | RTC Time Table 101 | R/W | h0X_XX_XX | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | MEMD[15:8] | | | | | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | MEMD[7:0] | | | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| 0x15 | RTC Alarm Table 102 | R/W | h01_FF_FF | RTCCALMODE[1:0] | | RTCCAL[4:0] | | | | | TOD[16] |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | TOD[15:8] | | | | | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | TOD[7:0] | | | | | | | |
| 0x16 | RTC Day Table 103 | R/W | h00_XX_XX | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | RTCDIS | SPARE | SPARE | SPARE | SPARE | SPARE | SPARE | TODA[16] |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | TODA[15:8] | | | | | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x17 | RTC Day Alarm Table 104 | R/W | h00_7F_FF | TODA[7:0] | | | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | DAY[14:8] | | | | | | |
| 0x18 | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | DAY[7:0] | | | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| 0x19 | | | | - | DAYA[14:8] | | | | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | DAYA[7:0] | | | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |

| 0x18 | Regulator 1A/B Voltage Table 105 | R/W/M | hXX_XX_XX | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|------|---|-------|-----------|------------------|--------------------|--------------------|----------------|---------------|----------------|---------------|------------|
| | | | | RSVD[5:0] | | | | | RSVD[5:4] | | |
| 0x19 | Regulator 2&3 Voltage Table 106 | R/W/M | hXX_XX_XX | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | RSVD[3:0] | | | | SW1ASTBY[5:2] | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | SW1ASTBY[1:0] | | SW1A[5:0] | | | | | |
| 0x1A | Regulator 4 Voltage Table 107 | R/W/M | hXX_XX_XX | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | SW3STBY[4:0] | | | | | - | SW3[4] |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | SW3[3:0] | | | | SW2STBY[5:2] | | | |
| 0x1B | Regulator 5 Voltage Table 108 | R/W/M | h00_XX_XX | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | SW2STBY[1:0] | | SW2[5:0] | | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | SW4BHI[1:0] | | SW4BSTBY[4:0] | | | | | SW4B[4] |
| 0x1C | Regulator 1, 2 Mode Table 109 | R/W/M | h52_80_48 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | SW4B[3:0] | | | | SW4AHI[1:0] | | SW4ASTBY[4:3] | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | SW4ASTBY[2:0] | | | SW4A[4:0] | | | | |
| 0x1D | Regulator 3, 4, 5 Mode Table 110 | R/W/M | h52_08_48 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | SW5TBY[4:0] | | | | | - | - |
| 0x1E | Regulator Setting 0 Table 111 | R/W/M | h00_XX_XX | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | - | - | SW5[4:0] | | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | PLLX | PLLEN | SW2DVSSPEED[1:0] | | SW2UOMODE | SW2MHMODE | SW2MODE[3:2] | |
| 0x1F | SWBST Control Table 112 | R/W/M | h00_00_0X | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | SW2MODE[1:0] | | - | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | SW1DVSSPEED[1:0] | | SW1AUOMODE | SW1AMHMODE | SW1AMODE[3:0] | | | |
| 0x18 | Regulator 1A/B Voltage Table 105 | R/W/M | hXX_XX_XX | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | SW5UOMODE | SW5MHMODE | SW5MODE[3:0] | | | SW4BUOMODE | SW4BMHMODE | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | SW4BMODE[3:0] | | | SW4AUOMODE | SW4AMHMODE | SW4AMODE[3:2] | | |
| 0x19 | Regulator 2&3 Voltage Table 106 | R/W/M | hXX_XX_XX | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | SW4AMODE[1:0] | | SW3UOMODE | SW3MHMODE | SW3MODE[3:0] | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| 0x1A | Regulator 4 Voltage Table 107 | R/W/M | hXX_XX_XX | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | VUSB2[1:0] | | VPLL[1:0] | | VGEN2[2] |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | VGEN2[1:0] | | VDAC[1:0] | | - | VGEN1[2:0] | | |
| 0x1B | Regulator 5 Voltage Table 108 | R/W/M | h00_XX_XX | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | - | - |
| 0x1C | Regulator 1, 2 Mode Table 109 | R/W/M | h52_80_48 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | SPARE | | SWBSTSTBYMODE[1:0] | | SPARE | SWBSTMODE[1:0] | | SWBST[1:0] |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| 0x1D | Regulator 3, 4, 5 Mode Table 110 | R/W/M | h52_08_48 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | SPARE | SWBSTSTBYMODE[1:0] | SPARE | SWBSTMODE[1:0] | SWBST[1:0] | | | |

| | | | | | | | | | | | |
|--------------|---|-------|-----------|-------------|-------------|-----------|------------|-------------|-------------|-------------|----------|
| 0x20 | Regulator Mode 0 Table 113 | R/W/M | h0X_XX_XX | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | VUSB2MODE | VUSB2STBY | VUSB2EN | VUSB2CONFIG | VPLLSTBY |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | VPLLEN | VGEN2MODE | VGEN2STBY | VGEN2EN | VGEN2CONFIG | VREFDDREN | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x21 | GPIOLV0 Control Table 114 | R/W | h00_38_0X | - | VDACMODE | VDACSTBY | VDACEN | VUSBEN | - | VGEN1STBY | VGEN1EN |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | SPARE |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | SRE1 | SRE0 | PUS1 | PUS0 | PUE | DSE | ODE | PKE |
| 0x22 | GPIOLV1 Control Table 115 | R/W | h00_38_0X | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | INT1 | INT0 | DBNC1 | DBNC0 | HYS | DOOUT | DIN | DIR |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | SPARE |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| 0x23 | GPIOLV2 Control Table 116 | R/W | h00_38_0X | SRE1 | SRE0 | PUS1 | PUS0 | PUE | DSE | ODE | PKE |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | INT1 | INT0 | DBNC1 | DBNC0 | HYS | DOOUT | DIN | DIR |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | SPARE |
| 0x24 | GPIOLV3 Control Table 117 | R/W | h00_38_0X | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | SRE1 | SRE0 | PUS1 | PUS0 | PUE | DSE | ODE | PKE |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | INT1 | INT0 | DBNC1 | DBNC0 | HYS | DOOUT | DIN | DIR |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| 0x25 to 0x2A | Unused | NU | h00_00_00 | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | - | - | - | - | - | - | - |
| 0x2B | ADC 0 Table 120 | R/W | h00_00_00 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | SPARE | SPARE | SPARE | TSPENDETEN | SPARE | TSSTOP[2:0] | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | TSHOLD | TSCONT | TSSTART | TSEN | SPARE | SPARE | SPARE | THERM |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x2C | ADC 1 Table 121 | R/W | h00_00_00 | SPARE | ADSTOP[2:0] | | | ADHOLD | ADCONT | ADSTART | ADEN |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | TSDLY3[3:0] | | | | TSDLY2[3:0] | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | TSDLY1[3:0] | | | | ADDLY3[3:0] | | | |
| 0x2D | ADC 2 Table 122 | R/W | h00_00_00 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | ADDLY2[3:0] | | | | ADDLY1[3:0] | | | |

| | | | | | | | | | | | |
|------|---|-----|-----------|----------------|----|-------------|----|----------------|----|-------------|----|
| 0x2D | ADC 2 Table 122 | R/W | h00_00_00 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | ADSEL5[3:0] | | | | ADSEL4[3:0] | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | ADSEL3[3:0] | | | | ADSEL2[3:0] | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x2E | ADC 3 Table 123 | R/W | h00_00_00 | ADSEL1[3:0] | | | | ADSEL0[3:0] | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | TSSEL7[1:0] | | TSSEL6[1:0] | | TSSEL5[1:0] | | TSSEL4[1:0] | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | TSSEL3[1:0] | | TSSEL2[1:0] | | TSSEL1[1:0] | | TSSEL0[1:0] | |
| 0x2F | ADC 4 Table 124 | R/W | h00_00_00 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | ADSEL7[3:0] | | | | ADSEL6[3:0] | | | |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | ADRESULT1[9:2] | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| 0x30 | ADC 5 Table 125 | R/W | h00_00_00 | ADRESULT1[1:0] | | - | - | ADRESULT0[9:6] | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | ADRESULT0[5:0] | | | | | | - | - |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | ADRESULT3[9:2] | | | | | | | |
| 0x31 | ADC 6 Table 126 | R/W | h00_00_00 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | ADRESULT3[1:0] | | - | - | ADRESULT2[9:6] | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | ADRESULT2[5:0] | | | | | | - | - |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| 0x32 | ADC 7 Table 127 | R/W | h00_00_00 | ADRESULT5[9:2] | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | ADRESULT5[1:0] | | - | - | ADRESULT4[9:6] | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | ADRESULT4[5:2] | | | | | | - | - |
| 0x33 | Unused | NU | h00_00_00 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | ADRESULT7[9:2] | | | | | | | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | ADRESULT7[9:2] | | - | - | ADRESULT6[9:6] | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x34 | Supply Debounce Table 129 | R/W | h03_00_00 | ADRESULT6[5:0] | | | | | | - | - |
| | | | | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | - | - |
| 0x34 | Supply Debounce Table 129 | R/W | h03_00_00 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | - | - | - | - | - | - | - | - |
| | | | | - | - | - | - | - | - | - | - |
| | | | | - | - | - | - | VBATTDB[1:0] | | - | - |

| | | | | | | | | | | | |
|--------------|--|-----|-----------|-----------------|----|---------------|----|-----------------|----|---------------|----|
| 0x35 to 0x36 | Unused | NU | h00_00_00 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | - | - | - | - | - | - | - |
| 0x37 | PWM Control Table 131 | R/W | h00_00_00 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | PWM2CLKDIV[5:0] | | | | | | PWM2DUTY[5:4] | |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | PWM2DUTY[3:0] | | | | PWM1CLKDIV[5:2] | | | |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | PWM1CLKDIV[1:0] | | PWM1DUTY[5:0] | | | | | |
| 0x38 to 0x3F | Unused | NU | h00_00_00 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| | | | | - | - | - | - | - | - | - | - |
| | | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | - | - | - | - | - | - | - | - |

7.9.4 SPI Register's Bit Description

Table 83. Register 0, Interrupt Status 0

| Name | Bit # | R/W | Reset | Default | Description |
|----------|-------|------|--------|---------|--|
| ADCDONEI | 0 | RW1C | RESETB | 0 | ADC has finished requested conversions |
| TSDONEI | 1 | RW1C | RESETB | 0 | Touchscreen has finished requested conversions |
| TSPENDET | 2 | RW1C | RESETB | 0 | Touch screen pen detection |
| Reserved | 12-3 | R | - | - | Reserved |
| LOWBATT | 13 | RW1C | RESETB | 0 | Low battery threshold warning |
| Reserved | 23-14 | R | - | - | Reserved |

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Table 84. Register 1, Interrupt Mask 0

| Name | Bit # | R/W | Reset | Default | Description |
|-----------|-------|-----|--------|---------|----------------------------------|
| ADCDONEM | 0 | R/W | RESETB | 1 | ADCDONEI mask bit |
| TSDONEM | 1 | R/W | RESETB | 1 | TSDONEI mask bit |
| TSPENDETM | 2 | R/W | RESETB | 1 | Touch screen pen detect mask bit |
| Reserved | 12-3 | R | - | - | Reserved |
| LOWBATTM | 13 | R/W | RESETB | 1 | LOBATLI mask bit |
| Reserved | 23-14 | R | - | - | Reserved |

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Table 85. Register 2, Reserved

| Name | Bit # | R/W | Reset | Default | Description |
|----------|-------|-----|-------|---------|-------------|
| Reserved | 23-0 | R | - | - | Reserved |

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Table 86. Register 3, Interrupt Status 1

| Name | Bit # | R/W | Reset | Default | Description |
|-----------|-------|------|---------|---------|---|
| 1HZI | 0 | RW1C | RTCPORB | 0 | 1.0 Hz time tick |
| TODAI | 1 | RW1C | RTCPORB | 0 | Time of day alarm |
| Unused | 2 | R | | 0 | Not available |
| PWRON1I | 3 | RW1C | OFFB | 0 | PWRON1 event |
| PWRON2I | 4 | RW1C | OFFB | 0 | PWRON2 event |
| WDIRESETI | 5 | RW1C | RTCPORB | 0 | WDI system reset event |
| SYSRSTI | 6 | RW1C | RTCPORB | 0 | PWRON system reset event |
| RTCSTI | 7 | RW1C | RTCPORB | 1 | RTC reset event |
| PCI | 8 | RW1C | OFFB | 0 | Power cut event |
| WARMI | 9 | RW1C | RTCPORB | 0 | Warm start event |
| MEMHLDI | 10 | RW1C | RTCPORB | 0 | Memory hold event |
| THERM110 | 11 | RW1C | RESETB | 0 | 110 °C thermal threshold |
| THERM120 | 12 | RW1C | RESETB | 0 | 120 °C thermal threshold |
| THERM125 | 13 | RW1C | RESETB | 0 | 125 °C thermal threshold |
| THERM130 | 14 | RW1C | RESETB | 0 | 130 °C thermal threshold |
| CLKI | 15 | RW1C | RESETB | 0 | Clock source change |
| SCPI | 16 | RW1C | RESETB | 0 | Short-circuit protection trip detection |
| GPIOLV1I | 17 | RW1C | RESETB | 0 | GPIOLV1 interrupt |
| GPIOLV2I | 18 | RW1C | RESETB | 0 | GPIOLV2 interrupt |
| GPIOLV3I | 19 | RW1C | RESETB | 0 | GPIOLV3 interrupt |
| GPIOLV4I | 20 | RW1C | RESETB | 0 | GPIOLV4 interrupt |
| Unused | 21 | R | - | 0 | Not available |
| Reserved | 22 | R | - | - | Reserved |
| Unused | 23 | R | RESETB | 0 | Not available |

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Table 87. Register 4, Interrupt Mask 1

| Name | Bit # | R/W | Reset | Default | Description |
|---------|-------|-----|---------|---------|-----------------|
| 1HZM | 0 | R/W | RTCPORB | 1 | 1HZI mask bit |
| TODAM | 1 | R/W | RTCPORB | 1 | TODAI mask bit |
| Unused | 2 | R | | 1 | Not available |
| PWRON1M | 3 | R/W | OFFB | 1 | PWRON1 mask bit |

Table 87. Register 4, Interrupt Mask 1

| Name | Bit # | R/W | Reset | Default | Description |
|-----------|-------|-----|---------|---------|--|
| PWRON2M | 4 | R/W | OFFB | 1 | PWRON2 mask bit |
| WDIRESETM | 5 | R/W | RTCPORB | 1 | WDIRESETI mask bit |
| YSRSTM | 6 | R/W | RTCPORB | 1 | YSRSTI mask bit |
| RTCRSTM | 7 | R/W | RTCPORB | 1 | RTCRSTI mask bit |
| PCM | 8 | R/W | OFFB | 1 | PCI mask bit |
| WARMM | 9 | R/W | RTCPORB | 1 | WARMI mask bit |
| MEMHLD | 10 | R/W | RTCPORB | 1 | MEMHLDI mask bit |
| THERM110M | 11 | R/W | RESETB | 1 | THERM110 mask bit |
| THERM120M | 12 | R/W | RESETB | 1 | THERM120 mask bit |
| THERM125M | 13 | R/W | RESETB | 1 | THERM125 mask bit |
| THERM130M | 14 | R/W | RESETB | 1 | THERM130 mask bit |
| CLKM | 15 | R/W | RESETB | 1 | CLKI mask bit |
| SCPM | 16 | R/W | RESETB | 1 | Short-circuit protection trip mask bit |
| GPIOLV1M | 17 | R/W | RESETB | 1 | GPIOLV1 interrupt mask bit |
| GPIOLV2M | 18 | R/W | RESETB | 1 | GPIOLV2 interrupt mask bit |
| GPIOLV3M | 19 | R/W | RESETB | 1 | GPIOLV3 interrupt mask bit |
| GPIOLV4M | 20 | R/W | RESETB | 1 | GPIOLV4 interrupt mask bit |
| Unused | 21 | R | | 0 | Not available |
| Reserved | 22 | R | - | - | Reserved |
| Unused | 23 | R | | 1 | Not available |

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Table 88. Register 5, Interrupt Sense 1

| Name | Bit # | R/W | Reset | Default | Description |
|-----------|-------|-----|-------|---------|--------------------|
| Unused | 2-0 | R | | 0 | Not available |
| PWRON1S | 3 | R | NONE | S | PWRON1I sense bit |
| PWRON2S | 4 | R | NONE | S | PWRON2I sense bit |
| Unused | 10-5 | R | | 0 | Not available |
| THERM110S | 11 | R | NONE | S | THERM110 sense bit |
| THERM120S | 12 | R | NONE | S | THERM120 sense bit |
| THERM125S | 13 | R | NONE | S | THERM125 sense bit |
| THERM130S | 14 | R | NONE | S | THERM130 sense bit |
| CLKS | 15 | R | NONE | 0 | CLKI sense bit |
| Unused | 21-16 | R | | 0 | Not available |
| Reserved | 22 | R | - | - | Reserved |
| Unused | 23 | R | NONE | 0 | Not available |

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Table 89. Register 6, Power-up Mode Sense

| Name | Bit # | R/W | Reset | Default | Description |
|----------|-------|-----|-------|---------|--------------------|
| ICTESTS | 0 | R | NONE | S | ICTEST sense state |
| PUMS1S | 1 | R | NONE | L | PUMS1 state |
| PUMS2S | 2 | R | NONE | L | PUMS2 state |
| PUMS3S | 3 | R | NONE | L | PUMS3 state |
| PUMS4S | 4 | R | NONE | L | PUMS4 state |
| PUMS5S | 5 | R | NONE | L | PUMS5 state |
| Unused | 8-6 | R | | 0 | Not available |
| Reserved | 9 | R | - | - | Reserved |
| Unused | 23-10 | R | | 0 | Not available |

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Table 90. Register 7, Identification

| Name | Bit # | R/W | Reset | Default | Description |
|------------------|-------|-----|-----------|---------|---|
| METAL_LAYER_REV0 | 0 | R | NONE | X | Metal Layer version Pass 1.1 = 001 Pass 1.2 = 010 |
| METAL_LAYER_REV1 | 1 | R | NONE | X | |
| METAL_LAYER_REV2 | 2 | R | NONE | X | |
| FULL_LAYER_REV0 | 3 | R | NONE | X | Full Layer version Pass 1.0 = 001 |
| FULL_LAYER_REV1 | 4 | R | NONE | X | |
| FULL_LAYER_REV2 | 5 | R | NONE | X | |
| FIN0 | 6 | R | NONE | X | FIN version Pass 1.0 = 000 |
| FIN1 | 7 | R | NONE | X | |
| FIN2 | 8 | R | NONE | X | |
| FAB0 | 9 | R | NONE | X | FAB version Pass 1.0 = 000 |
| FAB1 | 10 | R | NONE | X | |
| FAB2 | 11 | R | NONE | X | |
| Unused | 18-12 | R | | 0 | Not available |
| PAGE0 | 19 | R/W | DIGRESETB | 0 | SPI Page |
| PAGE1 | 20 | R/W | DIGRESETB | 0 | |
| PAGE2 | 21 | R/W | DIGRESETB | 0 | |
| PAGE3 | 22 | R/W | DIGRESETB | 0 | |
| PAGE4 | 23 | R/W | DIGRESETB | 0 | |

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Table 91. Register 8, Regulator Fault Sense

| Name | Bit # | R/W | Reset | Default | Description |
|------------|-------|-----|--------|---------|--|
| SW1FAULT | 0 | R | NONE | S | SW1 fault detection |
| Reserved | 1 | R | - | - | Reserved |
| SW2FAULT | 2 | R | NONE | S | SW2 fault detection |
| SW3FAULT | 3 | R | NONE | S | SW3 fault detection |
| SW4AFAULT | 4 | R | NONE | S | SW4A fault detection |
| SW4BFAULT | 5 | R | NONE | S | SW4B fault detection |
| SW5FAULT | 6 | R | NONE | S | SW5 fault detection |
| SWBSTFAULT | 7 | R | NONE | S | SWBST fault detection |
| VUSBFAULT | 8 | R | NONE | S | VUSB fault detection |
| VUSB2FAULT | 9 | R | NONE | S | VUSB2 fault detection |
| VDACFAULT | 10 | R | NONE | S | VDAC fault detection |
| VGEN1FAULT | 11 | R | NONE | S | VGEN1 fault detection |
| VGEN2FAULT | 12 | R | NONE | S | VGEN2 fault detection |
| Unused | 13-22 | R | | 0 | Not available |
| REGSCPEN | 23 | R/W | RESETB | 0 | Register short-circuit protect enable. This bit should be set to 1 to reduce power dissipation on the external pass LDOs (VUSB2, VGEN2, and VDAC). When a short-circuit condition is detected, the LDO's VxEN bit is set to 0, disabling the LDO and an SCPI interrupt will be generated |

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Table 92. Register 9, Reserved

| Name | Bit # | R/W | Reset | Default | Description |
|----------|-------|-----|-------|---------|-------------|
| Reserved | 23-0 | R | - | - | Reserved |

Table 93. Register 10 to 12, Unused

| Name | Bit # | R/W | Reset | Default | Description |
|----------|-------|-----|-------|---------|-------------|
| Reserved | 23-0 | R | - | - | Reserved |

Table 94. Register 13, Power Control 0

| Name | Bit # | R/W | Reset | Default | Description |
|-------------|-------|-----|-------------------------|---------|---|
| PCEN | 0 | R/W | RTCPORB | 0 | Power cut enable |
| PCCOUNTEN | 1 | R/W | RTCPORB | 0 | Power cut counter enable |
| WARMEN | 2 | R/W | RTCPORB | 0 | Warm start enable |
| USEROFFSPI | 3 | R/W | RESETB | 0 | SPI command for entering user off modes |
| DRM | 4 | R/W | RTCPORB ⁽⁶⁸⁾ | 0 | Keeps VSRTC and CLK32KMCU on for all states |
| USEROFFCLK | 5 | R/W | RTCPORB | 0 | Keeps the CLK32KMCU active during user off |
| CLK32KMCUEN | 6 | R/W | RTCPORB | 1 | Enables the CLK32KMCU |

Table 94. Register 13, Power Control 0

| Name | Bit # | R/W | Reset | Default | Description |
|----------|-------|-----|---------|---------|--|
| Unused | 8-7 | R | | 0 | Not available |
| PCUTEXPB | 9 | R/W | RTCPORB | 0 | PCUTEXPB=1 at a start-up event indicates that PCUT timer did not expire (assuming it was set to 1 after booting) |
| Unused | 18-10 | R | | 0 | Not available |
| Reserved | 19 | R | - | - | Reserved |
| VCOIN0 | 20 | R/W | RTCPORB | 0 | Coin cell charger voltage setting |
| VCOIN1 | 21 | R/W | RTCPORB | 0 | |
| VCOIN2 | 22 | R/W | RTCPORB | 0 | |
| COINCHEN | 23 | R/W | RTCPORB | 0 | Coin cell charger enable |

Notes:

68. Reset by RTCPORB but not during a GLBRST (global reset).

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Table 95. Register 14, Power Control 1

| Name | Bit # | R/W | Reset | Default | Description |
|-----------|-------|-----|---------|---------|--------------------------------------|
| PCT0 | 0 | R/W | RTCPORB | 0 | Power cut timer |
| PCT1 | 1 | R/W | RTCPORB | 0 | |
| PCT2 | 2 | R/W | RTCPORB | 0 | |
| PCT3 | 3 | R/W | RTCPORB | 0 | |
| PCT4 | 4 | R/W | RTCPORB | 0 | |
| PCT5 | 5 | R/W | RTCPORB | 0 | |
| PCT6 | 6 | R/W | RTCPORB | 0 | |
| PCT7 | 7 | R/W | RTCPORB | 0 | |
| PCCOUNT0 | 8 | R/W | RTCPORB | 0 | Power cut counter |
| PCCOUNT1 | 9 | R/W | RTCPORB | 0 | |
| PCCOUNT2 | 10 | R/W | RTCPORB | 0 | |
| PCCOUNT3 | 11 | R/W | RTCPORB | 0 | |
| PCMAXCNT0 | 12 | R/W | RTCPORB | 0 | Maximum allowed number of power cuts |
| PCMAXCNT1 | 13 | R/W | RTCPORB | 0 | |
| PCMAXCNT2 | 14 | R/W | RTCPORB | 0 | |
| PCMAXCNT3 | 15 | R/W | RTCPORB | 0 | |
| Unused | 23-16 | R | | 0 | Not available |

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Table 96. Register 15, Power Control 2

| Name | Bit # | R/W | Reset | Default | Description |
|-------------|-------|-----|---------|---------|--|
| RESTARTEN | 0 | R/W | RTCPORB | 0 | Enables automatic restart after a system reset |
| PWRON1RSTEN | 1 | R/W | RTCPORB | 0 | Enables system reset on PWRON1 pin |
| PWRON2RSTEN | 2 | R/W | RTCPORB | 0 | Enables system reset on PWRON2 pin |
| Unused | 3 | R | | 0 | Not available |
| PWRON1DBNC0 | 4 | R/W | RTCPORB | 0 | Sets debounce time on PWRON1 pin |
| PWRON1DBNC1 | 5 | R/W | RTCPORB | 0 | |
| PWRON2DBNC0 | 6 | R/W | RTCPORB | 0 | Sets debounce time on PWRON2 pin |
| PWRON2DBNC1 | 7 | R/W | RTCPORB | 0 | |
| GLBRSTTMR0 | 8 | R/W | RTCPORB | 1 | Sets Global reset time |
| GLBRSTTMR1 | 9 | R/W | RTCPORB | 1 | |
| STANDBYINV | 10 | R/W | RTCPORB | 0 | If set then STANDBY is interpreted as active low |
| Unused | 11 | R | | 0 | Not available |
| WDIRESET | 12 | R/W | RESETB | 0 | Enables system reset through WDI |
| SPIDRV0 | 13 | R/W | RTCPORB | 1 | SPI drive strength |
| SPIDRV1 | 14 | R/W | RTCPORB | 0 | |
| Unused | 16-15 | R | | 0 | Not available |
| CLK32KDRV0 | 17 | R/W | RTCPORB | 1 | CLK32K and CLK32KMCU drive strength (master control bits) |
| CLK32KDRV1 | 18 | R/W | RTCPORB | 0 | |
| Unused | 20-19 | R | | 0 | Not available |
| ON_STBY_LP | 21 | R/W | RESETB | 0 | On Standby Low-power Mode 0 = Low-power mode disabled 1 = Low-power mode enabled |
| STBYDLY0 | 22 | R/W | RESETB | 1 | Standby delay control |
| STBYDLY1 | 23 | R/W | RESETB | 0 | |

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Table 97. Register 16, Memory A

| Name | Bit # | R/W | Reset | Default | Description |
|--------|-------|-----|---------|---------|-----------------|
| MEMA0 | 0 | R/W | RTCPORB | 0 | Backup memory A |
| MEMA1 | 1 | R/W | RTCPORB | 0 | |
| MEMA2 | 2 | R/W | RTCPORB | 0 | |
| MEMA3 | 3 | R/W | RTCPORB | 0 | |
| MEMA4 | 4 | R/W | RTCPORB | 0 | |
| MEMA5 | 5 | R/W | RTCPORB | 0 | |
| MEMA6 | 6 | R/W | RTCPORB | 0 | |
| MEMA7 | 7 | R/W | RTCPORB | 0 | |
| MEMA8 | 8 | R/W | RTCPORB | 0 | |
| MEMA9 | 9 | R/W | RTCPORB | 0 | |
| MEMA10 | 10 | R/W | RTCPORB | 0 | |
| MEMA11 | 11 | R/W | RTCPORB | 0 | |
| MEMA12 | 12 | R/W | RTCPORB | 0 | |
| MEMA13 | 13 | R/W | RTCPORB | 0 | |
| MEMA14 | 14 | R/W | RTCPORB | 0 | |
| MEMA15 | 15 | R/W | RTCPORB | 0 | |
| MEMA16 | 16 | R/W | RTCPORB | 0 | |
| MEMA17 | 17 | R/W | RTCPORB | 0 | |
| MEMA18 | 18 | R/W | RTCPORB | 0 | Backup memory A |
| MEMA19 | 19 | R/W | RTCPORB | 0 | |
| MEMA20 | 20 | R/W | RTCPORB | 0 | |
| MEMA21 | 21 | R/W | RTCPORB | 0 | |
| MEMA22 | 22 | R/W | RTCPORB | 0 | |
| MEMA23 | 23 | R/W | RTCPORB | 0 | |

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Table 98. Register 17, Memory B

| Name | Bit # | R/W | Reset | Default | Description |
|--------|-------|-----|---------|---------|-----------------|
| MEMB0 | 0 | R/W | RTCPORB | 0 | Backup memory B |
| MEMB1 | 1 | R/W | RTCPORB | 0 | |
| MEMB2 | 2 | R/W | RTCPORB | 0 | |
| MEMB3 | 3 | R/W | RTCPORB | 0 | |
| MEMB4 | 4 | R/W | RTCPORB | 0 | |
| MEMB5 | 5 | R/W | RTCPORB | 0 | |
| MEMB6 | 6 | R/W | RTCPORB | 0 | |
| MEMB7 | 7 | R/W | RTCPORB | 0 | |
| MEMB8 | 8 | R/W | RTCPORB | 0 | |
| MEMB9 | 9 | R/W | RTCPORB | 0 | |
| MEMB10 | 10 | R/W | RTCPORB | 0 | |
| MEMB11 | 11 | R/W | RTCPORB | 0 | |
| MEMB12 | 12 | R/W | RTCPORB | 0 | |
| MEMB13 | 13 | R/W | RTCPORB | 0 | |
| MEMB14 | 14 | R/W | RTCPORB | 0 | |
| MEMB15 | 15 | R/W | RTCPORB | 0 | |
| MEMB16 | 16 | R/W | RTCPORB | 0 | |
| MEMB17 | 17 | R/W | RTCPORB | 0 | |
| MEMB18 | 18 | R/W | RTCPORB | 0 | |
| MEMB19 | 19 | R/W | RTCPORB | 0 | |
| MEMB20 | 20 | R/W | RTCPORB | 0 | |
| MEMB21 | 21 | R/W | RTCPORB | 0 | |
| MEMB22 | 22 | R/W | RTCPORB | 0 | |
| MEMB23 | 23 | R/W | RTCPORB | 0 | |

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Table 99. Register 18, Memory C

| Name | Bit # | R/W | Reset | Default | Description |
|--------|-------|-----|---------|---------|-----------------|
| MEMC0 | 0 | R/W | RTCPORB | 0 | Backup memory C |
| MEMC1 | 1 | R/W | RTCPORB | 0 | |
| MEMC2 | 2 | R/W | RTCPORB | 0 | |
| MEMC3 | 3 | R/W | RTCPORB | 0 | |
| MEMC4 | 4 | R/W | RTCPORB | 0 | |
| MEMC5 | 5 | R/W | RTCPORB | 0 | |
| MEMC6 | 6 | R/W | RTCPORB | 0 | |
| MEMC7 | 7 | R/W | RTCPORB | 0 | |
| MEMC8 | 8 | R/W | RTCPORB | 0 | |
| MEMC9 | 9 | R/W | RTCPORB | 0 | |
| MEMC10 | 10 | R/W | RTCPORB | 0 | |
| MEMC11 | 11 | R/W | RTCPORB | 0 | |
| MEMC12 | 12 | R/W | RTCPORB | 0 | |
| MEMC13 | 13 | R/W | RTCPORB | 0 | |
| MEMC14 | 14 | R/W | RTCPORB | 0 | |
| MEMC15 | 15 | R/W | RTCPORB | 0 | |
| MEMC16 | 16 | R/W | RTCPORB | 0 | |
| MEMC17 | 17 | R/W | RTCPORB | 0 | |
| MEMC18 | 18 | R/W | RTCPORB | 0 | |
| MEMC19 | 19 | R/W | RTCPORB | 0 | |
| MEMC20 | 20 | R/W | RTCPORB | 0 | |
| MEMC21 | 21 | R/W | RTCPORB | 0 | |
| MEMC22 | 22 | R/W | RTCPORB | 0 | |
| MEMC23 | 23 | R/W | RTCPORB | 0 | |

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Table 100. Register 19, Memory D

| Name | Bit # | R/W | Reset | Default | Description |
|--------|-------|-----|---------|---------|-----------------|
| MEMD0 | 0 | R/W | RTCPORB | 0 | Backup memory D |
| MEMD1 | 1 | R/W | RTCPORB | 0 | |
| MEMD2 | 2 | R/W | RTCPORB | 0 | |
| MEMD3 | 3 | R/W | RTCPORB | 0 | |
| MEMD4 | 4 | R/W | RTCPORB | 0 | |
| MEMD5 | 5 | R/W | RTCPORB | 0 | |
| MEMD6 | 6 | R/W | RTCPORB | 0 | |
| MEMD7 | 7 | R/W | RTCPORB | 0 | |
| MEMD8 | 8 | R/W | RTCPORB | 0 | |
| MEMD9 | 9 | R/W | RTCPORB | 0 | |
| MEMD10 | 10 | R/W | RTCPORB | 0 | Backup memory D |
| MEMD11 | 11 | R/W | RTCPORB | 0 | |
| MEMD12 | 12 | R/W | RTCPORB | 0 | |
| MEMD13 | 13 | R/W | RTCPORB | 0 | |
| MEMD14 | 14 | R/W | RTCPORB | 0 | |
| MEMD15 | 15 | R/W | RTCPORB | 0 | |
| MEMD16 | 16 | R/W | RTCPORB | 0 | |
| MEMD17 | 17 | R/W | RTCPORB | 0 | |
| MEMD18 | 18 | R/W | RTCPORB | 0 | |
| MEMD19 | 19 | R/W | RTCPORB | 0 | |
| MEMD20 | 20 | R/W | RTCPORB | 0 | |
| MEMD21 | 21 | R/W | RTCPORB | 0 | |
| MEMD22 | 22 | R/W | RTCPORB | 0 | |
| MEMD23 | 23 | R/W | RTCPORB | 0 | |

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Table 101. Register 20, RTC Time

| Name | Bit # | R/W | Reset | Default | Description |
|-------------|-------|-----|-------------------------|---------|-----------------------|
| TOD0 | 0 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | Time of day counter |
| TOD1 | 1 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD2 | 2 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD3 | 3 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD4 | 4 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD5 | 5 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD6 | 6 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD7 | 7 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD8 | 8 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD9 | 9 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD10 | 10 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD11 | 11 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD12 | 12 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD13 | 13 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD14 | 14 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD15 | 15 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| TOD16 | 16 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| RTCCAL0 | 17 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | RTC calibration count |
| RTCCAL1 | 18 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| RTCCAL2 | 19 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| RTCCAL3 | 20 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| RTCCAL4 | 21 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |
| RTCCALMODE0 | 22 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | RTC calibration mode |
| RTCCALMODE1 | 23 | R/W | RTCPORB ⁽⁶⁹⁾ | 0 | |

Notes

69. Reset by RTCPORB but not during a GLBRST (global reset)

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Table 102. Register 21, RTC Alarm

| Name | Bit # | R/W | Reset | Default | Description |
|--------|--------|-----|-------------------------|---------|-------------------|
| TODA0 | 0 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | Time of day alarm |
| TODA1 | 1 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA2 | 2 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA3 | 3 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA4 | 4 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA5 | 5 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA6 | 6 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA7 | 7 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA8 | 8 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA9 | 9 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA10 | 10 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA11 | 11 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA12 | 12 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA13 | 13 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA14 | 14 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA15 | 15 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| TODA16 | 16 | R/W | RTCPORB ⁽⁷⁰⁾ | 1 | |
| Unused | 17- 22 | R | | 0 | Not available |
| RTCDIS | 23 | R/W | RTCPORB ⁽⁷⁰⁾ | 0 | Disable RTC |

Notes

70. Reset by RTCPORB but not during a GLBRST (global reset)

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Table 103. Register 22, RTC Day

| Name | Bit # | R/W | Reset | Default | Description |
|--------|---------|-----|-------------------------|---------|---------------|
| DAY0 | 0 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | Day counter |
| DAY1 | 1 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY2 | 2 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY3 | 3 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY4 | 4 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY5 | 5 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY6 | 6 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY7 | 7 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY8 | 8 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY9 | 9 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY10 | 10 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY11 | 11 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY12 | 12 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY13 | 13 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| DAY14 | 14 | R/W | RTCPORB ⁽⁷¹⁾ | 0 | |
| Unused | 15 - 23 | R | | 0 | Not available |

Notes

71. Reset by RTCPORB but not during a GLBRST (global reset)
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Table 104. Register 23, RTC Day Alarm

| Name | Bit # | R/W | Reset | Default | Description |
|--------|---------|-----|-------------------------|---------|---------------|
| DAYA0 | 0 | R/W | RTCPORB ⁽⁷²⁾ | 1 | Day alarm |
| DAYA1 | 1 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA2 | 2 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA3 | 3 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA4 | 4 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA5 | 5 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA6 | 6 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA7 | 7 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA8 | 8 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA9 | 9 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA10 | 10 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA11 | 11 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA12 | 12 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA13 | 13 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| DAYA14 | 14 | R/W | RTCPORB ⁽⁷²⁾ | 1 | |
| Unused | 15 - 23 | R | | 0 | Not available |

Notes

72. Reset by RTCPORB but not during a GLBRST (global reset)

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Table 105. Register 24, Regulator 1A/B Voltage

| Name | Bit # | R/W | Reset | Default | Description |
|-----------|---------|------|-------|---------|-----------------------------|
| SW1A0 | 0 | R/WM | NONE | * | SW1 setting in normal mode |
| SW1A1 | 1 | R/WM | NONE | * | |
| SW1A2 | 2 | R/WM | NONE | * | |
| SW1A3 | 3 | R/WM | NONE | * | |
| SW1A4 | 4 | R/WM | NONE | * | |
| SW1A5 | 5 | R/WM | NONE | * | |
| SW1ASTBY0 | 6 | R/WM | NONE | * | SW1 setting in Standby mode |
| SW1ASTBY1 | 7 | R/WM | NONE | * | |
| SW1ASTBY2 | 8 | R/WM | NONE | * | |
| SW1ASTBY3 | 9 | R/WM | NONE | * | |
| SW1ASTBY4 | 10 | R/WM | NONE | * | |
| SW1ASTBY5 | 11 | R/WM | NONE | * | |
| Reserved | 12 - 23 | R | - | - | Reserved |

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Table 106. Register 25, Regulator 2 & 3 Voltage

| Name | Bit # | R/W | Reset | Default | Description |
|----------|-------|------|-------|---------|-----------------------------|
| SW20 | 0 | R/WM | NONE | * | SW2 setting in normal mode |
| SW21 | 1 | R/WM | NONE | * | |
| SW22 | 2 | R/WM | NONE | * | |
| SW23 | 3 | R/WM | NONE | * | |
| SW24 | 4 | R/WM | NONE | * | |
| SW25 | 5 | R/WM | NONE | * | |
| SW2STBY0 | 6 | R/WM | NONE | * | SW2 setting in Standby mode |
| SW2STBY1 | 7 | R/WM | NONE | * | |
| SW2STBY2 | 8 | R/WM | NONE | * | |
| SW2STBY3 | 9 | R/WM | NONE | * | |
| SW2STBY4 | 10 | R/WM | NONE | * | |
| SW2STBY5 | 11 | R/WM | NONE | * | |
| SW30 | 12 | R/WM | NONE | * | SW3 setting in normal mode |
| SW31 | 13 | R/WM | NONE | * | |
| SW32 | 14 | R/WM | NONE | * | |
| SW33 | 15 | R/WM | NONE | * | |
| SW34 | 16 | R/WM | NONE | * | |
| Unused | 17 | R | | 0 | Not available |
| SW3STBY0 | 18 | R/WM | NONE | * | SW3 setting in standby mode |
| SW3STBY1 | 19 | R/WM | NONE | * | |
| SW3STBY2 | 20 | R/WM | NONE | * | |
| SW3STBY3 | 21 | R/WM | NONE | * | |
| SW3STBY4 | 22 | R/WM | NONE | * | |
| Unused | 23 | R | | 0 | Not available |

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Table 107. Register 26, REgulator 4A/B

| Name | Bit # | R/W | Reset | Default | Description |
|-------|-------|------|-------|---------|-----------------------------|
| SW4A0 | 0 | R/WM | NONE | * | SW4A setting in normal mode |
| SW4A1 | 1 | R/WM | NONE | * | |
| SW4A2 | 2 | R/WM | NONE | * | |
| SW4A3 | 3 | R/WM | NONE | * | |
| SW4A4 | 4 | R/WM | NONE | * | |

Table 107. Register 26, REgulator 4A/B

| Name | Bit # | R/W | Reset | Default | Description |
|-----------|-------|------|--------|---------|------------------------------|
| SW4ASTBY0 | 5 | R/WM | NONE | * | SW4A setting in Standby mode |
| SW4ASTBY1 | 6 | R/WM | NONE | * | |
| SW4ASTBY2 | 7 | R/WM | NONE | * | |
| SW4ASTBY3 | 8 | R/WM | NONE | * | |
| SW4ASTBY4 | 9 | R/WM | NONE | * | |
| SW4AHIO | 10 | R/WM | NONE | * | SW4A high setting |
| SW4AHI1 | 11 | R/WM | NONE | * | |
| SW4B0 | 12 | R/WM | NONE | * | SW4B setting in normal mode |
| SW4B1 | 13 | R/WM | NONE | * | |
| SW4B2 | 14 | R/WM | NONE | * | |
| SW4B3 | 15 | R/WM | NONE | * | |
| SW4B4 | 16 | R/WM | RESETB | * | |
| SW4BSTBY0 | 17 | R/WM | RESETB | * | SW4B setting in Standby mode |
| SW4BSTBY1 | 18 | R/WM | RESETB | * | |
| SW4BSTBY2 | 19 | R/WM | RESETB | * | |
| SW4BSTBY3 | 20 | R/WM | RESETB | * | |
| SW4BSTBY4 | 21 | R/WM | RESETB | * | |
| SW4BHI0 | 22 | R/WM | RESETB | * | SW4B high setting |
| SW4BHI1 | 23 | R/WM | RESETB | * | |

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Table 108. Register 27, REgulator 5 Voltage

| Name | Bit # | R/W | Reset | Default | Description |
|----------|-------|------|-------|---------|-----------------------------|
| SW50 | 0 | R/WM | NONE | * | SW4 setting in normal mode |
| SW51 | 1 | R/WM | NONE | * | |
| SW52 | 2 | R/WM | NONE | * | |
| SW53 | 3 | R/WM | NONE | * | |
| SW54 | 4 | R/WM | NONE | * | |
| Unused | 5-9 | R | | * | Not available |
| SW5STBY0 | 10 | R/WM | NONE | * | SW5 setting in Standby mode |
| SW5STBY1 | 11 | R/WM | NONE | * | |
| SW5STBY2 | 12 | R/WM | NONE | * | |
| SW5STBY3 | 13 | R/WM | NONE | * | |
| SW5STBY4 | 14 | R/WM | NONE | * | |
| Unused | 15-23 | R | | 0 | Not available |

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Table 109. Register 28, Regulators 1 & 2 Operating Mode

| Name | Bit # | R/W | Reset | Default | Description |
|--------------------------|--------|-----|--------|---------|---------------------------|
| SW1AMODE0 | 0 | R/W | RESETB | 0 | SW1A operating mode |
| SW1AMODE1 | 1 | R/W | RESETB | 0 | |
| SW1AMODE2 | 2 | R/W | RESETB | 0 | |
| SW1AMODE3 | 3 | R/W | RESETB | 1 | |
| SW1AMHMODE | 4 | R/W | OFFB | 0 | SW1A Memory Hold mode |
| SW1AUOMODE | 5 | R/W | OFFB | 0 | SW1A User Off mode |
| SW1DVSSPEED0 | 6 | R/W | RESETB | 1 | SW1 DVS1 speed |
| SW1DVSSPEED1 | 7 | R/W | RESETB | 0 | |
| Unused | 8 - 13 | R | | 0 | Not available |
| SW2MODE0 ⁽⁷³⁾ | 14 | R/W | RESETB | 0 | SW2 operating mode |
| SW2MODE1 ⁽⁷³⁾ | 15 | R/W | RESETB | 0 | |
| SW2MODE2 ⁽⁷³⁾ | 16 | R/W | RESETB | 0 | |
| SW2MODE3 ⁽⁷³⁾ | 17 | R/W | RESETB | 1 | |
| SW2MHMODE | 18 | R/W | OFFB | 0 | SW2 Memory Hold mode |
| SW2UOMODE | 19 | R/W | OFFB | 0 | SW2 User Off mode |
| SW2DVSSPEED0 | 20 | R/W | RESETB | 1 | SW2 DVS1 speed |
| SW2DVSSPEED1 | 21 | R/W | RESETB | 0 | |
| PLLEN | 22 | R/W | RESETB | 1 | PLL enable |
| PLLX | 23 | R/W | RESETB | 0 | PLL multiplication factor |

Notes

73. SWxMODE[3:0] bits will be reset to their default values by the start-up sequencer, based on PUMS settings. On start-up all switching regulators will default to APS mode for both Normal and Standby operation.

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Table 110. Register 29, Regulators 3, 4, and 5 Operating Mode

| Name | Bit # | R/W | Reset | Default | Description |
|------------|-------|-----|--------|---------|-----------------------|
| SW3MODE0 | 0 | R/W | RESETB | 0 | SW3 operating mode |
| SW3MODE1 | 1 | R/W | RESETB | 0 | |
| SW3MODE2 | 2 | R/W | RESETB | 0 | |
| SW3MODE3 | 3 | R/W | RESETB | 1 | |
| SW3MHMODE | 4 | R/W | OFFB | 0 | SW3 Memory Hold mode |
| SW3UOMODE | 5 | R/W | OFFB | 0 | SW3 User Off mode |
| SW4AMODE0 | 6 | R/W | RESETB | 0 | SW4A operating mode |
| SW4AMODE1 | 7 | R/W | RESETB | 0 | |
| SW4AMODE2 | 8 | R/W | RESETB | 0 | |
| SW4AMODE3 | 9 | R/W | RESETB | 1 | |
| SW4AMHMODE | 10 | R/W | OFFB | 0 | SW4A Memory Hold mode |
| SW4AUOMODE | 11 | R/W | OFFB | 0 | SW4A User Off mode |

Table 110. Register 29, Regulators 3, 4, and 5 Operating Mode

| | | | | | |
|--------------------------|----|-----|--------|---|-----------------------|
| SW4BMODE0 | 12 | R/W | RESETB | 0 | SW4B operating mode |
| SW4BMODE1 | 13 | R/W | RESETB | 0 | |
| SW4BMODE2 | 14 | R/W | RESETB | 0 | |
| SW4BMODE3 | 15 | R/W | RESETB | 1 | |
| SW4BMHMODE | 16 | R/W | OFFB | 0 | SW4B Memory Hold mode |
| SW4BUOMODE | 17 | R/W | OFFB | 0 | SW4B User Off mode |
| SW5MODE0 ⁽⁷⁴⁾ | 18 | R/W | RESETB | 0 | SW5 operating mode |
| SW5MODE1 ⁽⁷⁴⁾ | 19 | R/W | RESETB | 0 | |
| SW5MODE2 ⁽⁷⁴⁾ | 20 | R/W | RESETB | 0 | |
| SW5MODE3 ⁽⁷⁴⁾ | 21 | R/W | RESETB | 1 | |
| SW5MHMODE | 22 | R/W | OFFB | 0 | SW5 Memory Hold mode |
| SW5UOMODE | 23 | R/W | OFFB | 0 | SW5 User Off mode |

Notes

74. SWxMODE[3:0] bits will be reset to their default values by the start-up sequencer, based on PUMS settings. On start-up all switching regulators will default to APS mode for both Normal and Standby operation.

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Table 111. Register 30, Regulator Setting 0

| Name | Bit # | R/W | Reset | Default | Description |
|--------|--------|------|--------|---------|---------------|
| VGEN10 | 0 | R/WM | RESETB | * | VGEN1 setting |
| VGEN11 | 1 | R/WM | RESETB | * | |
| VGEN12 | 2 | R/WM | RESETB | * | |
| Unused | 3 | R | | 0 | Not available |
| VDAC0 | 4 | R/WM | RESETB | * | VDAC setting |
| VDAC1 | 5 | R/WM | RESETB | * | |
| VGEN20 | 6 | R/WM | RESETB | * | VGEN2 setting |
| VGEN21 | 7 | R/WM | RESETB | * | |
| VGEN22 | 8 | R/WM | RESETB | * | |
| VPLL0 | 9 | R/WM | RESETB | * | VPLL setting |
| VPLL1 | 10 | R/WM | RESETB | * | |
| VUSB20 | 11 | R/WM | RESETB | * | VUSB2 setting |
| VUSB21 | 12 | R/WM | RESETB | * | |
| Unused | 13 -23 | R | | 0 | Not available |

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Table 112. Register 31, SWBST Control

| Name | Bit # | R/W | Reset | Default | Description |
|----------------|--------|-----|--------|---------|--------------------|
| SWBST0 | 0 | R/W | NONE | * | SWBST setting |
| SWBST1 | 1 | R/W | NONE | * | |
| SWBSTMODE0 | 2 | R/W | RESETB | 0 | SWBST mode |
| SWBSTMODE1 | 3 | R/W | RESETB | 1 | |
| Spare | 4 | R/W | RESETB | 0 | Not available |
| SWBSTSTBYMODE0 | 5 | R/W | RESETB | 0 | SWBST standby mode |
| SWBSTSTBYMODE1 | 6 | R/W | RESETB | 1 | |
| Spare | 7 | R/W | RESETB | 0 | Not available |
| Unused | 8 - 23 | R | | 0 | Not available |

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Table 113. Register 32, Regulator Mode 0

| Name | Bit # | R/W | Reset | Default | Description |
|-------------|-------|-----|--------|---------|--|
| VGEN1EN | 0 | R/W | NONE | * | VGEN1 enable |
| VGEN1STBY | 1 | R/W | RESETB | 0 | VGEN1 controlled by standby |
| Unused | 2 | R | | 0 | Not available |
| VUSBEN | 3 | R/W | RESETB | 1 | VUSB enable (PUMS4:1=[0100]). |
| VDACEN | 4 | R/W | NONE | * | VDAC enable |
| VDACSTBY | 5 | R/W | RESETB | 0 | VDAC controlled by standby |
| VDACMODE | 6 | R/W | RESETB | 0 | VDAC operating mode |
| Unused | 9-7 | R | | 0 | Not available |
| VREFDDR | 10 | R/W | NONE | * | VREFDDR enable |
| VGEN2CONFIG | 11 | R/W | NONE | * | PUMS5 Tied to ground = 0: VGEN2 with external PNP PUMS5 Tied to VCROREDIG =1: VGEN2 internal PMOS |
| VGEN2EN | 12 | R/W | NONE | * | VGEN2 enable |
| VGEN2STBY | 13 | R/W | RESETB | 0 | VGEN2 controlled by standby |
| VGEN2MODE | 14 | R/W | RESETB | 0 | VGEN2 operating mode |
| VPLEN | 15 | R/W | NONE | * | VPLL enable |
| VPLLSTBY | 16 | R/W | RESETB | 0 | VPLL controlled by standby |
| VUSB2CONFIG | 17 | R/W | NONE | * | PUMS5 Tied to ground = 0: VUSB2 with external PNP PUMS5 Tied to VCROREDIG =1: VUSB2 internal PMOS |
| VUSB2EN | 18 | R/W | NONE | * | VUSB2 enable |
| VUSB2STBY | 19 | R/W | RESETB | 0 | VUSB2 controlled by standby |
| VUSB2MODE | 20 | R/W | RESETB | 0 | VUSB2 operating mode |
| Unused | 23-21 | R | | 0 | Not available |

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Table 114. Register 33, GPIOLV0 Control

| Name | Bit # | R/W | Reset | Default | Description |
|--------|---------|-----|--------|---------|--|
| DIR | 0 | R/W | RESETB | 0 | GPIOLV0 direction 0: Input 1: Output |
| DIN | 1 | R/W | RESETB | 0 | Input state of GPIOLV0 pin 0: Input low 1: Input High |
| DOUT | 2 | R/W | RESETB | 0 | Output state of GPIOLV0 pin 0: Output Low 1: Output High |
| HYS | 3 | R/W | RESETB | 1 | Hysteresis 0: CMOS in 1: Hysteresis |
| DBNC0 | 4 | R/W | RESETB | 0 | GPIOLV0 input debounce time 00: no debounce 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce |
| DBNC1 | 5 | R/W | RESETB | 0 | |
| INT0 | 6 | R/W | RESETB | 0 | GPIOLV0 interrupt control 00: None 01: Falling edge 10: Rising edge 11: Both edges |
| INT1 | 7 | R/W | RESETB | 0 | |
| PKE | 8 | R/W | RESETB | 0 | Pad keep enable 0: Off 1: On |
| ODE | 9 | R/W | RESETB | 0 | Open-drain enable 0: CMOS 1: OD |
| DSE | 10 | R/W | RESETB | 0 | Drive strength enable 0: 4.0 mA 1: 8.0 mA |
| PUE | 11 | R/W | RESETB | 1 | Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default) |
| PUS0 | 12 | R/W | RESETB | 1 | Pull-up/Pull-down select 00: 10 K pull-down 01: 100 K pull-down 10: 10 K pull-up 11: 100 K pull-up |
| PUS1 | 13 | R/W | RESETB | 1 | |
| SRE0 | 14 | R/W | RESETB | 0 | Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast |
| SRE1 | 15 | R/W | RESETB | 0 | |
| Unused | 16 - 23 | R | | 0 | Not available |

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Table 115. Register 34, GPIOLV1 Control

| Name | Bit # | R/W | Reset | Default | Description |
|--------|---------|-----|--------|---------|--|
| DIR | 0 | R/W | RESETB | 0 | GPIOLV1 direction 0: Input 1: Output |
| DIN | 1 | R/W | RESETB | 0 | Input state of GPIOLV1 pin 0: Input low 1: Input High |
| DOUT | 2 | R/W | RESETB | 0 | Output state of GPIOLV1 pin 0: Output Low 1: Output High |
| HYS | 3 | R/W | RESETB | 1 | Hysteresis 0: CMOS in 1: Hysteresis |
| DBNC0 | 4 | R/W | RESETB | 0 | GPIOLV1 input debounce time 00: no debounce 01: 10 ms debounce 10: 20 ms debounce 11: 30 ms debounce |
| DBNC1 | 5 | R/W | RESETB | 0 | |
| INT0 | 6 | R/W | RESETB | 0 | GPIOLV1 interrupt control 00: None 01: Falling edge 10: Rising edge 11: Both edges |
| INT1 | 7 | R/W | RESETB | 0 | |
| PKE | 8 | R/W | RESETB | 0 | Pad keep enable 0: Off 1: On |
| ODE | 9 | R/W | RESETB | 0 | Open-drain enable 0: CMOS 1: OD |
| DSE | 10 | R/W | RESETB | 0 | Drive strength enable 0: 4.0 mA 1: 8.0 mA |
| PUE | 11 | R/W | RESETB | 1 | Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default) |
| PUS0 | 12 | R/W | RESETB | 1 | Pull-up/Pull-down select 00: 10 K pull-down 01: 100 K pull-down 10: 10 K pull-up 11: 100 K pull-up |
| PUS1 | 13 | R/W | RESETB | 1 | |
| SRE0 | 14 | R/W | RESETB | 0 | Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast |
| SRE1 | 15 | R/W | RESETB | 0 | |
| Unused | 16 - 23 | R | | 0 | Not available |

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Table 116. Register 35, GPIOLV2 Control

| Name | Bit # | R/W | Reset | Default | Description |
|--------|---------|-----|--------|---------|--|
| DIR | 0 | R/W | RESETB | 0 | GPIOLV2 direction 0: Input 1: Output |
| DIN | 1 | R/W | RESETB | 0 | Input state of GPIOLV2 pin 0: Input low 1: Input High |
| DOUT | 2 | R/W | RESETB | 0 | Output state of GPIOLV2 pin 0: Output Low 1: Output High |
| HYS | 3 | R/W | RESETB | 1 | Hysteresis 0: CMOS in 1: Hysteresis |
| DBNC0 | 4 | R/W | RESETB | 0 | GPIOLV2 input debounce time 00: no debounce 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce |
| DBNC1 | 5 | R/W | RESETB | 0 | |
| INT0 | 6 | R/W | RESETB | 0 | GPIOLV2 interrupt control 00: None 01: Falling edge 10: Rising edge 11: Both edges |
| INT1 | 7 | R/W | RESETB | 0 | |
| PKE | 8 | R/W | RESETB | 0 | Pad keep enable 0: Off 1: On |
| ODE | 9 | R/W | RESETB | 0 | Open-drain enable 0: CMOS 1: OD |
| DSE | 10 | R/W | RESETB | 0 | Drive strength enable 0: 4.0 mA 1: 8.0 mA |
| PUE | 11 | R/W | RESETB | 1 | Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default) |
| PUS0 | 12 | R/W | RESETB | 1 | Pull-up/Pull-down select 00: 10 K pull-down 01: 100 K pull-down 10: 10 K pull-up 11: 100 K pull-up |
| PUS1 | 13 | R/W | RESETB | 1 | |
| SRE0 | 14 | R/W | RESETB | 0 | Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast |
| SRE1 | 15 | R/W | RESETB | 0 | |
| Unused | 16 - 23 | R | | 0 | Not available |

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Table 117. Register 36, GPIOLV3 Control

| Name | Bit # | R/W | Reset | Default | Description |
|--------|---------|-----|--------|---------|--|
| DIR | 0 | R/W | RESETB | 0 | GPIOLV3 direction 0: Input 1: Output |
| DIN | 1 | R/W | RESETB | 0 | Input state of GPIOLV3 pin 0: Input low 1: Input High |
| DOUT | 2 | R/W | RESETB | 0 | Output state of GPIOLV3 pin 0: Output Low 1: Output High |
| HYS | 3 | R/W | RESETB | 1 | Hysteresis 0: CMOS in 1: Hysteresis |
| DBNC0 | 4 | R/W | RESETB | 0 | GPIOLV3 input debounce time 00: no debounce 01: 10 ms debounce 10: 20 ms debounce 11: 30 mS debounce |
| DBNC1 | 5 | R/W | RESETB | 0 | |
| INT0 | 6 | R/W | RESETB | 0 | GPIOLV3 interrupt control 00: None 01: Falling edge 10: Rising edge 11: Both edges |
| INT1 | 7 | R/W | RESETB | 0 | |
| PKE | 8 | R/W | RESETB | 0 | Pad keep enable 0: Off 1: On |
| ODE | 9 | R/W | RESETB | 0 | Open-drain enable 0: CMOS 1: OD |
| DSE | 10 | R/W | RESETB | 0 | Drive strength enable 0: 4.0 mA 1: 8.0 mA |
| PUE | 11 | R/W | RESETB | 1 | Pull-up/down enable 0: pull-up/down off 1: pull-up/down on (default) |
| PUS0 | 12 | R/W | RESETB | 1 | Pull-up/Pull-down select 00: 10 K pull-down 01: 100 K pull-down 10: 10 K pull-up 11: 100 K pull-up |
| PUS1 | 13 | R/W | RESETB | 1 | |
| SRE0 | 14 | R/W | RESETB | 0 | Slew rate enable 00: slow (default) 01: normal 10: fast 11: very fast |
| SRE1 | 15 | R/W | RESETB | 0 | |
| Unused | 16 - 23 | R | | 0 | Not available |

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Table 118. Register 37 - 40, Reserved

| Name | Bit # | R/W | Reset | Default | Description |
|--------|--------|-----|-------|---------|---------------|
| Unused | 0 - 23 | R | | 0 | Not available |

Table 119. Register 41 - 42, Unused

| Name | Bit # | R/W | Reset | Default | Description |
|--------|-------|-----|-------|---------|---------------|
| Unused | 0-23 | R | | 0 | Not available |

Table 120. Register 43, ADC 0

| Name | Bit # | R/W | Reset | Default | Description |
|------------|-------|-----|-----------|---------|---|
| ADEN | 0 | R/W | DIGRESETB | 0 | Enables ADC from the low-power mode |
| ADSTART | 1 | R/W | DIGRESETB | 0 | Request a start of the ADC Reading Sequencer |
| ADCONT | 2 | R/W | DIGRESETB | 0 | Run ADC reads continuously when high or one time when low. Note that the TSSTART request will have higher priority |
| ADHOLD | 3 | R/W | DIGRESETB | 0 | Hold the ADC reading Sequencer while saved ADC results are read from SPI |
| ADSTOP0 | 4 | R/W | DIGRESETB | 0 | Channel Selection to stop when complete. Always start at 000 and read up to and including this channel value. |
| ADSTOP1 | 5 | R/W | DIGRESETB | 0 | |
| ADSTOP2 | 6 | R/W | DIGRESETB | 0 | |
| Spare | 7 | R/W | DIGRESETB | 0 | Not available |
| THERM | 8 | R/W | DIGRESETB | 0 | 0: NTCREF not forced on 1: Force NTCREF on |
| Spare | 11-9 | R/W | DIGRESETB | 0 | Not available |
| TSEN | 12 | R/W | DIGRESETB | 0 | Enable the touch screen from low-power mode. |
| TSSTART | 13 | R/W | DIGRESETB | 0 | Request a start of the ADC Reading Sequencer for touch screen readings. |
| TSCONT | 14 | R/W | DIGRESETB | 0 | Run ADC reads of touch screen continuously when high or one time when low. |
| TSHOLD | 15 | R/W | DIGRESETB | 0 | Hold the ADC reading Sequencer while saved touch screen results are read from SPI |
| TSSTOP0 | 16 | R/W | DIGRESETB | 0 | Just like the ADSTOP above, but for the touch screen read programming. This will allow independent code for ADC Sequence readings and touch screen ADC Sequence readings. |
| TSSTOP1 | 17 | R/W | DIGRESETB | 0 | |
| TSSTOP2 | 18 | R/W | DIGRESETB | 0 | |
| Spare | 19 | R/W | DIGRESETB | 0 | Not available |
| TSPENDETEN | 20 | R/W | DIGRESETB | 0 | Enable the touch screen Pen Detection. Note that TSEN must be off for Pen Detection. |
| Spare | 23-21 | R/W | DIGRESETB | 0 | Not available |

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Table 121. Register 44, ADC 1

| Name | Bit # | R/W | Reset | Default | Description |
|---------|-------|-----|-----------|---------|---|
| ADDLY10 | 0 | R/W | DIGRESETB | 0 | This will allow delay before the ADC readings. |
| ADDLY11 | 1 | R/W | DIGRESETB | 0 | |
| ADDLY12 | 2 | R/W | DIGRESETB | 0 | |
| ADDLY13 | 3 | R/W | DIGRESETB | 0 | |
| ADDLY20 | 4 | R/W | DIGRESETB | 0 | This will allow delay between each of ADC readings in a set. |
| ADDLY21 | 5 | R/W | DIGRESETB | 0 | |
| ADDLY22 | 6 | R/W | DIGRESETB | 0 | |
| ADDLY23 | 7 | R/W | DIGRESETB | 0 | |
| ADDLY30 | 8 | R/W | DIGRESETB | 0 | This will allow delay after the set of ADC readings. This delay is only valid between subsequent wrap around reading sequences with ADCONT |
| ADDLY31 | 9 | R/W | DIGRESETB | 0 | |
| ADDLY32 | 10 | R/W | DIGRESETB | 0 | |
| ADDLY33 | 11 | R/W | DIGRESETB | 0 | |
| TSDLY10 | 12 | R/W | DIGRESETB | 0 | This will allow delay before the ADC touch screen readings. This is like the ADDLY1, but allows independent programming of touch screen readings from general purpose ADC readings to prevent code replacement in the system. |
| TSDLY11 | 13 | R/W | DIGRESETB | 0 | |
| TSDLY12 | 14 | R/W | DIGRESETB | 0 | |
| TSDLY13 | 15 | R/W | DIGRESETB | 0 | |
| TSDLY20 | 16 | R/W | DIGRESETB | 0 | This will allow delay between each of ADC touch screen readings in a set. This is like the ADDLY2, but allows independent programming of touch screen readings from general purpose ADC readings to prevent code replacement in the system. |
| TSDLY21 | 17 | R/W | DIGRESETB | 0 | |
| TSDLY21 | 18 | R/W | DIGRESETB | 0 | |
| TSDLY23 | 19 | R/W | DIGRESETB | 0 | |
| TSDLY30 | 20 | R/W | DIGRESETB | 0 | This will allow delay after the set of ADC touch screen readings. This delay is only valid between subsequent wrap around reading sequences with TSCONT mode. This is like the ADDLY3, but allows independent programming of touch screen readings from general purpose ADC readings to prevent code replacement in the system. |
| TSDLY31 | 21 | R/W | DIGRESETB | 0 | |
| TSDLY31 | 22 | R/W | DIGRESETB | 0 | |
| TSDLY33 | 23 | R/W | DIGRESETB | 0 | |

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Table 122. Register 45, ADC 2

| Name | Bit # | R/W | Reset | Default | Description |
|---------|-------|-----|-----------|---------|---|
| ADSEL00 | 0 | R/W | DIGRESETB | 0 | Channel Selection to place in ADRESULT0 |
| ADSEL01 | 1 | R/W | DIGRESETB | 0 | |
| ADSEL02 | 2 | R/W | DIGRESETB | 0 | |
| ADSEL03 | 3 | R/W | DIGRESETB | 0 | |
| ADSEL10 | 4 | R/W | DIGRESETB | 0 | Channel Selection to place in ADRESULT1 |
| ADSEL11 | 5 | R/W | DIGRESETB | 0 | |
| ADSEL12 | 6 | R/W | DIGRESETB | 0 | |
| ADSEL13 | 7 | R/W | DIGRESETB | 0 | |

Table 122. Register 45, ADC 2

| Name | Bit # | R/W | Reset | Default | Description |
|---------|-------|-----|-----------|---------|---|
| ADSEL20 | 8 | R/W | DIGRESETB | 0 | Channel Selection to place in ADRESULT2 |
| ADSEL21 | 9 | R/W | DIGRESETB | 0 | |
| ADSEL22 | 10 | R/W | DIGRESETB | 0 | |
| ADSEL23 | 11 | R/W | DIGRESETB | 0 | |
| ADSEL30 | 12 | R/W | DIGRESETB | 0 | Channel Selection to place in ADRESULT3 |
| ADSEL31 | 13 | R/W | DIGRESETB | 0 | |
| ADSEL32 | 14 | R/W | DIGRESETB | 0 | |
| ADSEL33 | 15 | R/W | DIGRESETB | 0 | |
| ADSEL40 | 16 | R/W | DIGRESETB | 0 | Channel Selection to place in ADRESULT4 |
| ADSEL41 | 17 | R/W | DIGRESETB | 0 | |
| ADSEL42 | 18 | R/W | DIGRESETB | 0 | |
| ADSEL43 | 19 | R/W | DIGRESETB | 0 | |
| ADSEL50 | 20 | R/W | DIGRESETB | 0 | Channel Selection to place in ADRESULT5 |
| ADSEL51 | 21 | R/W | DIGRESETB | 0 | |
| ADSEL52 | 22 | R/W | DIGRESETB | 0 | |
| ADSEL53 | 23 | R/W | DIGRESETB | 0 | |

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Table 123. Register 46, ADC 3

| Name | Bit # | R/W | Reset | Default | Description |
|---------|-------|-----|-----------|---------|--|
| ADSEL60 | 0 | R/W | DIGRESETB | 0 | Channel Selection to place in ADRESULT6 |
| ADSEL61 | 1 | R/W | DIGRESETB | 0 | |
| ADSEL62 | 2 | R/W | DIGRESETB | 0 | |
| ADSEL63 | 3 | R/W | DIGRESETB | 0 | |
| ADSEL70 | 4 | R/W | DIGRESETB | 0 | Channel Selection to place in ADRESULT7 |
| ADSEL71 | 5 | R/W | DIGRESETB | 0 | |
| ADSEL72 | 6 | R/W | DIGRESETB | 0 | |
| ADSEL73 | 7 | R/W | DIGRESETB | 0 | |
| TSSEL00 | 8 | R/W | DIGRESETB | 0 | Touch screen Selection to place in ADRESULT0. |
| TSSEL01 | 9 | R/W | DIGRESETB | 0 | Select the action for the Touch screen; 00 = dummy to discharge TSREF capacitance, 01 = to read X-plate, 10 = to read Y-plate, and 11 = to read Contact. |
| TSSEL10 | 10 | R/W | DIGRESETB | 0 | Touch screen Selection to place in ADRESULT1. |
| TSSEL11 | 11 | R/W | DIGRESETB | 0 | See TSSEL0 for modes. |
| TSSEL20 | 12 | R/W | DIGRESETB | 0 | Touch screen Selection to place in ADRESULT2. |
| TSSEL21 | 13 | R/W | DIGRESETB | 0 | See TSSEL0 for modes. |
| TSSEL30 | 14 | R/W | DIGRESETB | 0 | Touch screen Selection to place in ADRESULT3. |
| TSSEL31 | 15 | R/W | DIGRESETB | 0 | See TSSEL0 for modes. |

Table 123. Register 46, ADC 3

| Name | Bit # | R/W | Reset | Default | Description |
|---------|-------|-----|-----------|---------|--|
| TSSEL40 | 16 | R/W | DIGRESETB | 0 | Touch screen Selection to place in ADRESULT4. See TSSEL0 for modes. |
| TSSEL41 | 17 | R/W | DIGRESETB | 0 | |
| TSSEL50 | 18 | R/W | DIGRESETB | 0 | Touch screen Selection to place in ADRESULT5. See TSSEL0 for modes. |
| TSSEL51 | 19 | R/W | DIGRESETB | 0 | |
| TSSEL60 | 20 | R/W | DIGRESETB | 0 | Touch screen Selection to place in ADRESULT6. See TSSEL0 for modes. |
| TSSEL61 | 21 | R/W | DIGRESETB | 0 | |
| TSSEL70 | 22 | R/W | DIGRESETB | 0 | Touch screen Selection to place in ADRESULT7. See TSSEL0 for modes. |
| TSSEL71 | 23 | R/W | DIGRESETB | 0 | |

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Table 124. Register 47, ADC 4

| Name | Bit # | R/W | Reset | Default | Description |
|------------|-------|-----|-----------|---------|-----------------------|
| Unused | 1-0 | R | | 0 | Not available |
| ADRESULT00 | 2 | R | DIGRESETB | 0 | ADC Result for ADSEL0 |
| ADRESULT01 | 3 | R | DIGRESETB | 0 | |
| ADRESULT02 | 4 | R | DIGRESETB | 0 | |
| ADRESULT03 | 5 | R | DIGRESETB | 0 | |
| ADRESULT04 | 6 | R | DIGRESETB | 0 | |
| ADRESULT05 | 7 | R | DIGRESETB | 0 | |
| ADRESULT06 | 8 | R | DIGRESETB | 0 | |
| ADRESULT07 | 9 | R | DIGRESETB | 0 | |
| ADRESULT08 | 10 | R | DIGRESETB | 0 | |
| ADRESULT09 | 11 | R | DIGRESETB | 0 | |
| Unused | 13-12 | R | | 0 | Not available |
| ADRESULT10 | 14 | R | DIGRESETB | 0 | ADC Result for ADSEL1 |
| ADRESULT11 | 15 | R | DIGRESETB | 0 | |
| ADRESULT12 | 16 | R | DIGRESETB | 0 | |
| ADRESULT13 | 17 | R | DIGRESETB | 0 | |
| ADRESULT14 | 18 | R | DIGRESETB | 0 | |
| ADRESULT15 | 19 | R | DIGRESETB | 0 | |
| ADRESULT16 | 20 | R | DIGRESETB | 0 | |
| ADRESULT17 | 21 | R | DIGRESETB | 0 | |
| ADRESULT18 | 22 | R | DIGRESETB | 0 | |
| ADRESULT19 | 23 | R | DIGRESETB | 0 | |

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Table 125. Register 48, ADC5

| Name | Bit # | R/W | Reset | Default | Description |
|------------|-------|-----|-----------|---------|-----------------------|
| Unused | 1-0 | R | | 0 | Not available |
| ADRESULT20 | 2 | R | DIGRESETB | 0 | ADC Result for ADSEL2 |
| ADRESULT21 | 3 | R | DIGRESETB | 0 | |
| ADRESULT22 | 4 | R | DIGRESETB | 0 | |
| ADRESULT23 | 5 | R | DIGRESETB | 0 | |
| ADRESULT24 | 6 | R | DIGRESETB | 0 | |
| ADRESULT25 | 7 | R | DIGRESETB | 0 | |
| ADRESULT26 | 8 | R | DIGRESETB | 0 | |
| ADRESULT27 | 9 | R | DIGRESETB | 0 | |
| ADRESULT28 | 10 | R | DIGRESETB | 0 | |
| ADRESULT29 | 11 | R | DIGRESETB | 0 | |
| Unused | 13-12 | R | | 0 | Not available |
| ADRESULT30 | 14 | R | DIGRESETB | 0 | ADC Result for ADSEL3 |
| ADRESULT31 | 15 | R | DIGRESETB | 0 | |
| ADRESULT32 | 16 | R | DIGRESETB | 0 | |
| ADRESULT33 | 17 | R | DIGRESETB | 0 | |
| ADRESULT34 | 18 | R | DIGRESETB | 0 | |
| ADRESULT35 | 19 | R | DIGRESETB | 0 | |
| ADRESULT36 | 20 | R | DIGRESETB | 0 | |
| ADRESULT37 | 21 | R | DIGRESETB | 0 | |
| ADRESULT38 | 22 | R | DIGRESETB | 0 | |
| ADRESULT39 | 23 | R | DIGRESETB | 0 | |

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Table 126. Register 49, ADC6

| Name | Bit # | R/W | Reset | Default | Description |
|------------|-------|-----|-----------|---------|-----------------------|
| Unused | 1-0 | R | | 0 | Not available |
| ADRESULT40 | 2 | R | DIGRESETB | 0 | ADC Result for ADSEL4 |
| ADRESULT41 | 3 | R | DIGRESETB | 0 | |
| ADRESULT42 | 4 | R | DIGRESETB | 0 | |
| ADRESULT43 | 5 | R | DIGRESETB | 0 | |
| ADRESULT44 | 6 | R | DIGRESETB | 0 | |
| ADRESULT45 | 7 | R | DIGRESETB | 0 | |
| ADRESULT46 | 8 | R | DIGRESETB | 0 | |
| ADRESULT47 | 9 | R | DIGRESETB | 0 | |
| ADRESULT48 | 10 | R | DIGRESETB | 0 | |
| ADRESULT49 | 11 | R | DIGRESETB | 0 | |
| Unused | 13-12 | R | | 0 | Not available |
| ADRESULT50 | 14 | R | DIGRESETB | 0 | ADC Result for ADSEL5 |
| ADRESULT51 | 15 | R | DIGRESETB | 0 | |
| ADRESULT52 | 16 | R | DIGRESETB | 0 | |
| ADRESULT53 | 17 | R | DIGRESETB | 0 | |
| ADRESULT54 | 18 | R | DIGRESETB | 0 | |
| ADRESULT55 | 19 | R | DIGRESETB | 0 | |
| ADRESULT56 | 20 | R | DIGRESETB | 0 | |
| ADRESULT57 | 21 | R | DIGRESETB | 0 | |
| ADRESULT58 | 22 | R | DIGRESETB | 0 | |
| ADRESULT59 | 23 | R | DIGRESETB | 0 | |

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Table 127. Register 50, ADC7

| Name | Bit # | R/W | Reset | Default | Description |
|------------|-------|-----|-----------|---------|-----------------------|
| Unused | 1-0 | R | | 0 | Not available |
| ADRESULT60 | 2 | R | DIGRESETB | 0 | ADC Result for ADSEL6 |
| ADRESULT61 | 3 | R | DIGRESETB | 0 | |
| ADRESULT62 | 4 | R | DIGRESETB | 0 | |
| ADRESULT63 | 5 | R | DIGRESETB | 0 | |
| ADRESULT64 | 6 | R | DIGRESETB | 0 | |
| ADRESULT65 | 7 | R | DIGRESETB | 0 | |
| ADRESULT66 | 8 | R | DIGRESETB | 0 | |
| ADRESULT67 | 9 | R | DIGRESETB | 0 | |
| ADRESULT68 | 10 | R | DIGRESETB | 0 | |
| ADRESULT69 | 11 | R | DIGRESETB | 0 | |
| Unused | 13-12 | R | | 0 | Not available |
| ADRESULT70 | 14 | R | DIGRESETB | 0 | ADC Result for ADSEL7 |
| ADRESULT71 | 15 | R | DIGRESETB | 0 | |
| ADRESULT72 | 16 | R | DIGRESETB | 0 | |
| ADRESULT73 | 17 | R | DIGRESETB | 0 | |
| ADRESULT74 | 18 | R | DIGRESETB | 0 | |
| ADRESULT75 | 19 | R | DIGRESETB | 0 | |
| ADRESULT76 | 20 | R | DIGRESETB | 0 | |
| ADRESULT77 | 21 | R | DIGRESETB | 0 | |
| ADRESULT78 | 22 | R | DIGRESETB | 0 | |
| ADRESULT79 | 23 | R | DIGRESETB | 0 | |

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Table 128. Register 51, Reserved

| Name | Bit # | R/W | Reset | Default | Description |
|--------|--------|-----|-------|---------|---------------|
| Unused | 0 - 23 | R | | 0 | Not Available |

Table 129. Register 52, Supply Debounce

| Name | Bit # | R/W | Reset | Default | Description |
|----------|--------|-----|--------|---------|---------------------------------|
| Reserved | 1-0 | R | - | - | Reserved |
| VBATTDB0 | 2 | R/W | RESETB | 1 | Low input warning (BP) debounce |
| VBATTDB1 | 3 | R/W | RESETB | 1 | |
| Reserved | 4 - 23 | R | - | - | Reserved |

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Table 130. Register 53 - 54, Reserved

| Name | Bit # | R/W | Reset | Default | Description |
|--------|--------|-----|-------|---------|---------------|
| Unused | 0 - 23 | R | | 0 | Not Available |

Table 131. Register 55, PWM Control

| Name | Bit # | R/W | Reset | Default | Description |
|-------------|-------|-----|--------|---------|---------------------------|
| PWM1DUTY0 | 0 | R/W | RESETB | 0 | PWM1 Duty Cycle |
| PWM1DUTY1 | 1 | R/W | RESETB | 0 | |
| PWM1DUTY2 | 2 | R/W | RESETB | 0 | |
| PWM1DUTY3 | 3 | R/W | RESETB | 0 | |
| PWM1DUTY4 | 4 | R/W | RESETB | 0 | |
| PWM1DUTY5 | 5 | R/W | RESETB | 0 | |
| PWMCLKDIV0 | 6 | R/W | RESETB | 0 | PWM1 Clock Divide Setting |
| PWMCLKDIV1 | 7 | R/W | RESETB | 0 | |
| PWMCLKDIV2 | 8 | R/W | RESETB | 0 | |
| PWMCLKDIV3 | 9 | R/W | RESETB | 0 | |
| PWMCLKDIV4 | 10 | R/W | RESETB | 0 | |
| PWMCLKDIV5 | 11 | R/W | RESETB | 0 | |
| PWM2DUTY0 | 12 | R/W | RESETB | 0 | PWM2 Duty Cycle |
| PWM2DUTY1 | 13 | R/W | RESETB | 0 | |
| PWM2DUTY2 | 14 | R/W | RESETB | 0 | |
| PWM2DUTY3 | 15 | R/W | RESETB | 0 | |
| PWM2DUTY4 | 16 | R/W | RESETB | 0 | |
| PWM2DUTY5 | 17 | R/W | RESETB | 0 | |
| PWM2CLKDIV0 | 18 | R/W | RESETB | 0 | PWM2 Clock Divide Setting |
| PWM2CLKDIV1 | 19 | R/W | RESETB | 0 | |
| PWM2CLKDIV2 | 20 | R/W | RESETB | 0 | |
| PWM2CLKDIV3 | 21 | R/W | RESETB | 0 | |
| PWM2CLKDIV4 | 22 | R/W | RESETB | 0 | |
| PWM2CLKDIV5 | 23 | R/W | RESETB | 0 | |

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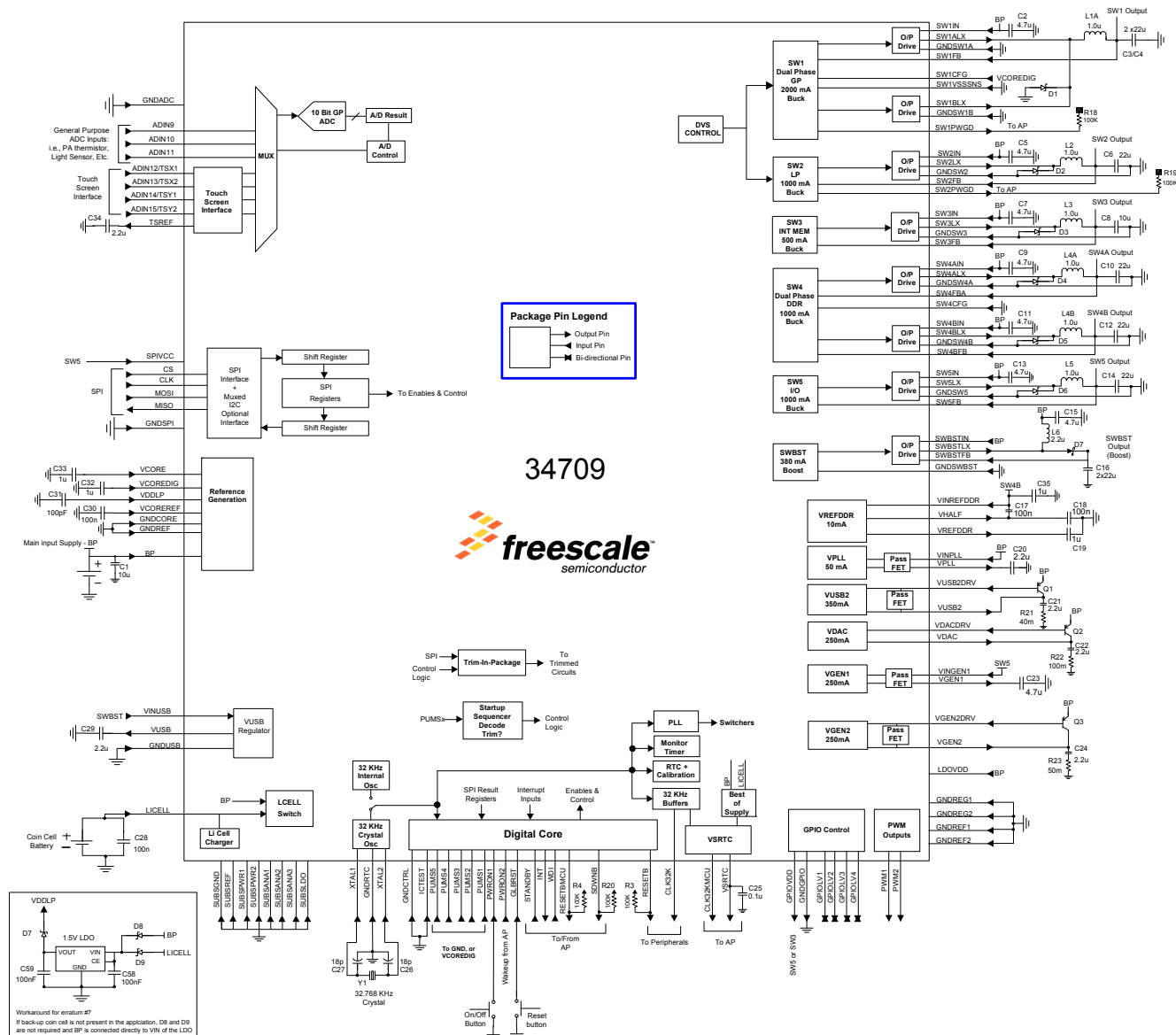
Table 132. Register 56 - 63, Unused

| Name | Bit # | R/W | Reset | Default | Description |
|--------|-------|-----|-------|---------|---------------|
| Unused | 0-23 | R | | 0 | Not available |

8 Typical Applications

Figure 24 gives a typical application diagram of the 34709 PMIC together with its functional components. For details on component references and additional components such as filters, refer to the individual sections.

8.1 Application Diagram



8.2 Bill of Material

Table 133 provides a complete list of the recommended components on a full featured system using the 34709 Device. Critical components such as inductors, transistors, and diodes are provided with a recommended part number, but equivalent components may be used.

Table 133. 34709 Bill of Material (75)

| Item | Reference | Quantity | Description | Vendor | Comments |
|------|-----------|----------|-------------|-----------|----------|
| 1 | U1 | 1 | 34709 | Freescale | PMIC |

Battery/supply input

| | | | | | |
|---|----|---|------------|-----|----------------|
| 2 | C1 | 1 | 10 μ F | TDK | Battery Filter |
|---|----|---|------------|-----|----------------|

Miscellaneous

| | | | | | |
|----|----------|---|------------------------|--|----------------------------|
| 3 | C25 | 1 | 100 nF | | VSRTC |
| 4 | C33 | 1 | 1.0 μ F | | VCORE |
| 5 | C32 | 1 | 1.0 μ F | | VCOREDIG |
| 6 | C31 | 1 | 100 pF | | VDDL |
| 7 | C30 | 1 | 100 nF | | VCORERE |
| 8 | C34 | 1 | 2.2 μ F | | TSREF |
| 9 | C28 | 1 | 100 nF | | Coin cell |
| 10 | Y1 | 1 | Crystal 32.768 kHz CC7 | | Oscillator |
| 11 | C26, C27 | 2 | 18 pF | | Oscillator load capacitors |
| 12 | R3, R4 | 2 | 100 k | | RESETB, RESETBMCU Pull-ups |
| 13 | R20 | 1 | 100 k | | SDWNB Pull-up |

Boost

| | | | | | |
|----|-----|---|--------------------------------|-----------|------------------------|
| 14 | L6 | 1 | 2.2 μ H • LPS3015-222ML | Coilcraft | Boost Inductor |
| 15 | D7 | 1 | Diode BAS52 | Infineon | Boost diode |
| 16 | C16 | 2 | 22 μ F 16 V | | Boost Output Capacitor |
| 17 | C15 | 1 | 4.7 μ F | | Boost Input Capacitor |

SW1

| | | | | | |
|----|----------|---|-----------------------------------|----------|---|
| 18 | L1A, L1B | 2 | 1.0 μ H • VLS201612ET-1R0N | TDK | Buck 1 Inductor ($I_{MAX} < 1.6$ Amps) Alternate part numbers: • 1.0 μ H VLS252010ET-1R0N (TDK) • 1.0 μ H BRL3225T1ROM (Taiyo Yuden) • 1.0 μ H LPS4012-102NL (Coilcraft) |
| 19 | C3, C4 | 2 | 22 μ F | | Buck 1 Output Capacitor |
| 20 | C2 | 1 | 4.7 μ F | | Buck 1 Input Capacitor |
| 21 | D1 | 1 | Diode • BAS3010-03LRH | Infineon | SW1LX diode |

Table 133. 34709 Bill of Material (75)

| Item | Reference | Quantity | Description | Vendor | Comments |
|-------------|-----------|----------|-----------------------------------|----------|---|
| SW2 | | | | | |
| 22 | L2 | 1 | 1.0 μ H • VLS252010ET-1R0N | TDK | Buck 2 Inductor |
| 23 | C6 | 1 | 22 μ F | | Buck 2 Output Capacitor |
| 24 | C5 | 1 | 4.7 μ F | | Buck 2 Input Capacitor |
| 25 | D2 | 1 | Diode • BAS3010-03LRH | Infineon | SW2LX diode |
| SW3 | | | | | |
| 26 | L3 | 1 | 1.0 μ H • VLS201612ET-1R0N | TDK | Buck 3 Inductor |
| 27 | C8 | 1 | 10 μ F | | Buck 3 Output Capacitor |
| 28 | C7 | 1 | 4.7 μ F | | Buck 3 Input Capacitor |
| 29 | D3 | 1 | Diode • BAS3010-03LRH | Infineon | SW3LX diode |
| SW4A | | | | | |
| 30 | L4A | 1 | 1.0 μ H • VLS201612ET-1R0N | TDK | Buck 4A Inductor Alternate Part number: • 1.0 μ H VLS252010ET-1R0N (TDK) |
| 31 | C10 | 1 | 22 μ F | | Buck 4A Output Capacitor |
| 32 | C9 | 1 | 4.7 μ F | | Buck 4A Input Capacitor |
| 33 | D4 | 1 | Diode • BAS3010-03LRH | Infineon | SW4ALX diode |
| SW4B | | | | | |
| 34 | L4B | 1 | 1.0 μ H • VLS201612ET-1R0N | TDK | Buck 4B Inductor Alternate Part numbers: • 1.0 μ H VLS252010ET-1R0N (TDK) |
| 35 | C12 | 1 | 22 μ F | | Buck 4B Output Capacitor |
| 36 | C11 | 1 | 4.7 μ F | | Buck 4B Input Capacitor |
| 37 | D5 | 1 | Diode • BAS3010-03LRH | Infineon | SW4BLX diode |
| SW5 | | | | | |
| 38 | L5 | 1 | 1.0 μ H • VLS252010ET-1R0N | TDK | Buck 5 Inductor |
| 39 | C14 | 1 | 22 μ F | | Buck 5 Output Capacitor |
| 40 | C13 | 1 | 4.7 μ F | | Buck 5 Input Capacitor |
| 41 | D6 | 1 | Diode • BAS3010-03LRH | Infineon | SW5LX diode |

Table 133. 34709 Bill of Material (75)

| Item | Reference | Quantity | Description | Vendor | Comments |
|----------------|-----------|----------|---|--|--|
| VPLL | | | | | |
| 42 | C20 | 1 | 2.2 μ F | | VPLL output capacitor |
| VREFDDR | | | | | |
| 43 | C18 | 1 | 100 nF | | VHALF 0.1 μ F capacitor |
| 44 | C19 | 1 | 1.0 μ F | | VREFDDR output Capacitor |
| 45 | C17 | 1 | 100 nF | | VINREFDDR/VHALF decoupling capacitor |
| 46 | C35 | 1 | 1.0 μ F | | VREFDDR input Capacitor |
| VDAC | | | | | |
| 47 | Q2 | 1 | PNP NSS12100UW3TCG PNP NSS12100XV6T1G 2SB1733 | On Semiconductor On Semiconductor Rohm | VDAC PNP - 500 mW dissipation VDAC PNP - 250 mW dissipation - Alternate VDAC PNP - 500 mW dissipation - Alternate |
| 48 | C22 | 1 | 2.2 μ F | | VDAC output Capacitor |
| 49 | R21 | 1 | 100 m Ω | | Connect this resistor in series with the output capacitor to provide an extra series resistance of 100 m Ω for LDO stability. |
| VUSB2 | | | | | |
| 50 | Q1 | 1 | PNP NSS12100UW3TCG PNP NSS12100XV6T1G 2SB1733 | On Semiconductor On Semiconductor Rohm | VDAC PNP - 500 mW dissipation VDAC PNP - 250 mW dissipation - Alternate VDAC PNP - 500 mW dissipation - Alternate |
| 51 | C21 | 1 | 2.2 μ F | | VUSB2 output Capacitor |
| 52 | R22 | 1 | 40 m Ω | | Connect this resistor in series with the output capacitor to provide an extra series resistance of 40 m Ω for LDO stability. |
| VUSB | | | | | |
| 53 | C29 | 1 | 2.2 μ F | | VUSB output Capacitor |
| VGEN1 | | | | | |
| 54 | C23 | 1 | 4.7 μ F | | VGEN1 output Capacitor |
| VGEN2 | | | | | |
| 55 | Q3 | 1 | PNP NSS12100UW3TCG PNP NSS12100XV6T1G 2SB1733 | On Semiconductor On Semiconductor Rohm | VDAC PNP - 500 mW dissipation VDAC PNP - 250 mW dissipation - Alternate VDAC PNP - 500 mW dissipation - Alternate |
| 56 | C24 | 1 | 2.2 μ F | | VGEN2 output Capacitor |
| 57 | R23 | 1 | 50 m Ω | | Connect this resistor in series with the output capacitor to provide an extra series resistance of 50 m Ω for LDO stability. |

Notes

75. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.

8.3 34709 Layout Guidelines

8.3.1 General board recommendations

1. It is recommended to use an 4 layer board stack-up arranged as follows:
 - High-current signal
 - GND
 - Signal
 - High-current signal
2. Allocate TOP and BOTTOM PCB Layers for POWER ROUTING (high-current signals), copper-pour the unused area.
3. Add one GND inner layer to reduce Current loops to the maximum between layers.

8.3.2 General Routing Requirements

1. Some recommended things to keep in mind for manufacturability:
 - Via in pads require a 4.5 mil Minimum annular ring. Pad must be 9.0 mils larger than the hole
 - Max copper thickness for lines less than 5.0 mils wide is 0.6 oz copper
 - Minimum allowed spacing between line and hole pad is 3.5 mils
 - Minimum allowed spacing between line and line is 3.0 mils
2. Care must be taken with SWx_{FB} pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high-power signals, like the ones on the SWx_{IN}, SWx, SWx_{LX}, SWBST_{IN}, SWBST, and SWBST_{LX} pins.
3. Shield feedback traces of the switching regulators and keep them as short as possible (trace them on the bottom so the ground and power planes shield these traces).
4. Avoid coupling trace between important signal/low noise supplies (like VCOR_{REF}, VCORE, VCORE_{DIG}) from any switching node (i.e. SW1_{ALX}, SW2_{LX}, SW3_{LX}, SW4_{ALX}, SW4_{BLX}, SW5_{LX}, and SWBST_{LX}).
5. Make sure that all components related to an specific block are referenced to the corresponding ground, e.g. all components related to the SW1 converter must referenced to GND_{SW1A1} and GND_{SW1A2}.

8.3.3 Parallel Routing Requirements

1. SPI/I²C signal routing:
 - CLK is the fastest signal of the system, so it must be given special care. Here are some tips for routing the communication signals:
 - To avoid contamination of these delicate signals by nearby high-power or high-frequency signals, it is a good practice to shield them with ground planes placed on adjacent layers. Make sure the ground plane is uniform throughout the whole signal trace length.

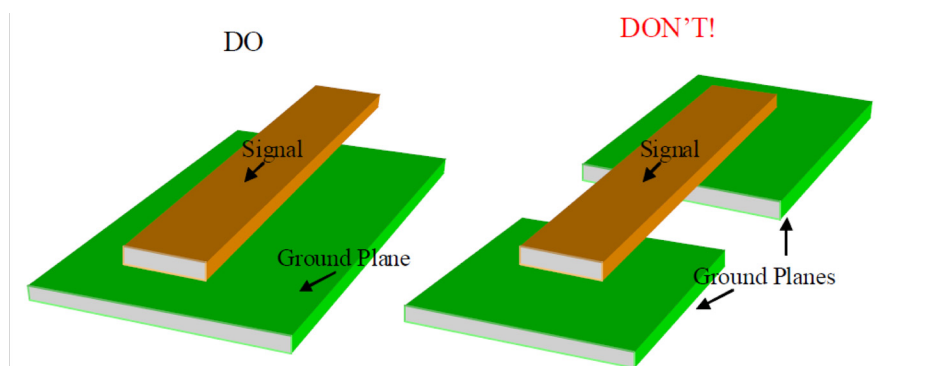


Figure 25. Recommended Shielding for Critical Signals.

- These signals can be placed on an outer layer of the board to reduce their capacitance in respect to the ground plane.

2. The crystal connected to the XTAL1 and XTAL2 pins must not have a ground plane directly below.
3. The following are clock signals: CLK, CLK32K, CLK32KMCU, XTAL1, and XTAL2. These signals must not run parallel to each other, or in the same routing layer. If it is necessary to run clock signals parallel to each other, or parallel to any other signal, then follow a MAX PARALLEL rule as follows:
 - Up to one inch parallel length – 25 mil minimum separation
 - Up to two inches parallel length – 50 mil minimum separation
 - Up to three inches parallel length – 100 mil minimum separation
 - Up to four inches parallel length – 250 mil minimum separation
- Care must be taken with these signals not to contaminate analog signals, as they are high-frequency signals. Another good practice is to trace them perpendicularly on different layers, so there is a minimum area of proximity between signals.

8.3.4 Switching Regulator Layout Recommendations

1. Per design, the 34709 is designed to operate with only one input bulk capacitor. However, it is recommended to add a high-frequency filter input capacitor (C_{IN_HF}), to filter out any noise at the regulator input. This capacitor should be in the range of 100 nF and should be placed right next to or under the IC, closest to the IC pins.
2. Make high-current ripple traces low inductance (short, high W/L ratio).
3. Make high-current traces wide or copper islands.
4. Make high-current traces SYMMETRICAL for dual-phase regulators (SW1, SW4).

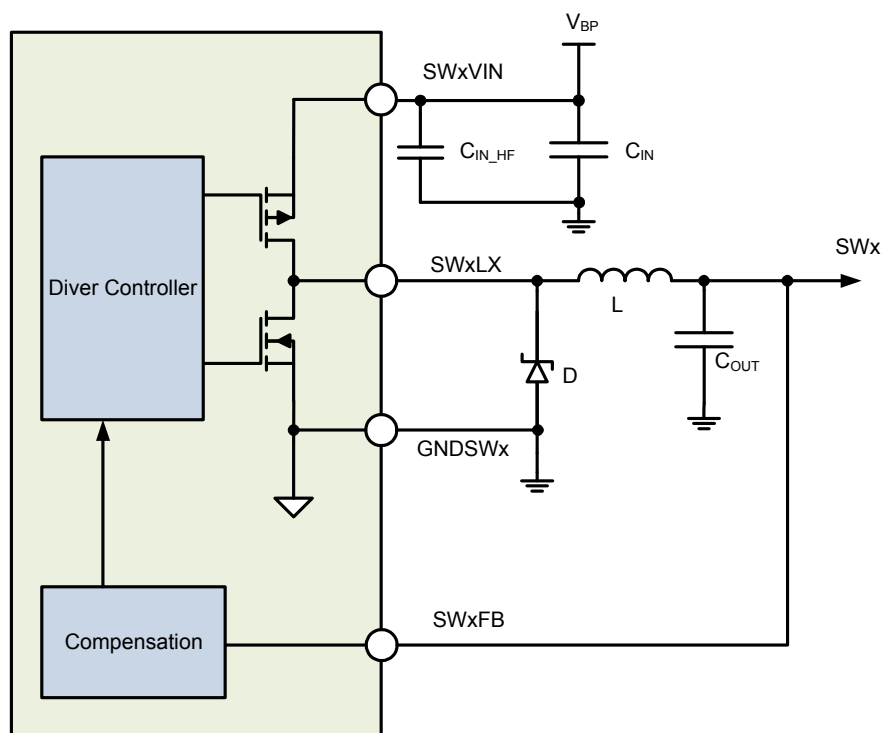


Figure 26. Generic Buck Regulator Architecture

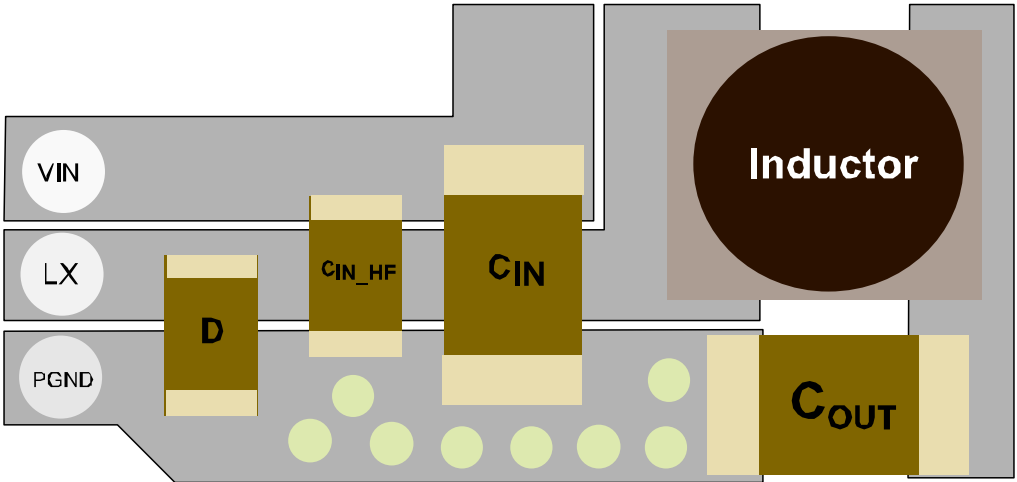


Figure 27. Recommended Layout for Switching Regulators.

9 Packaging

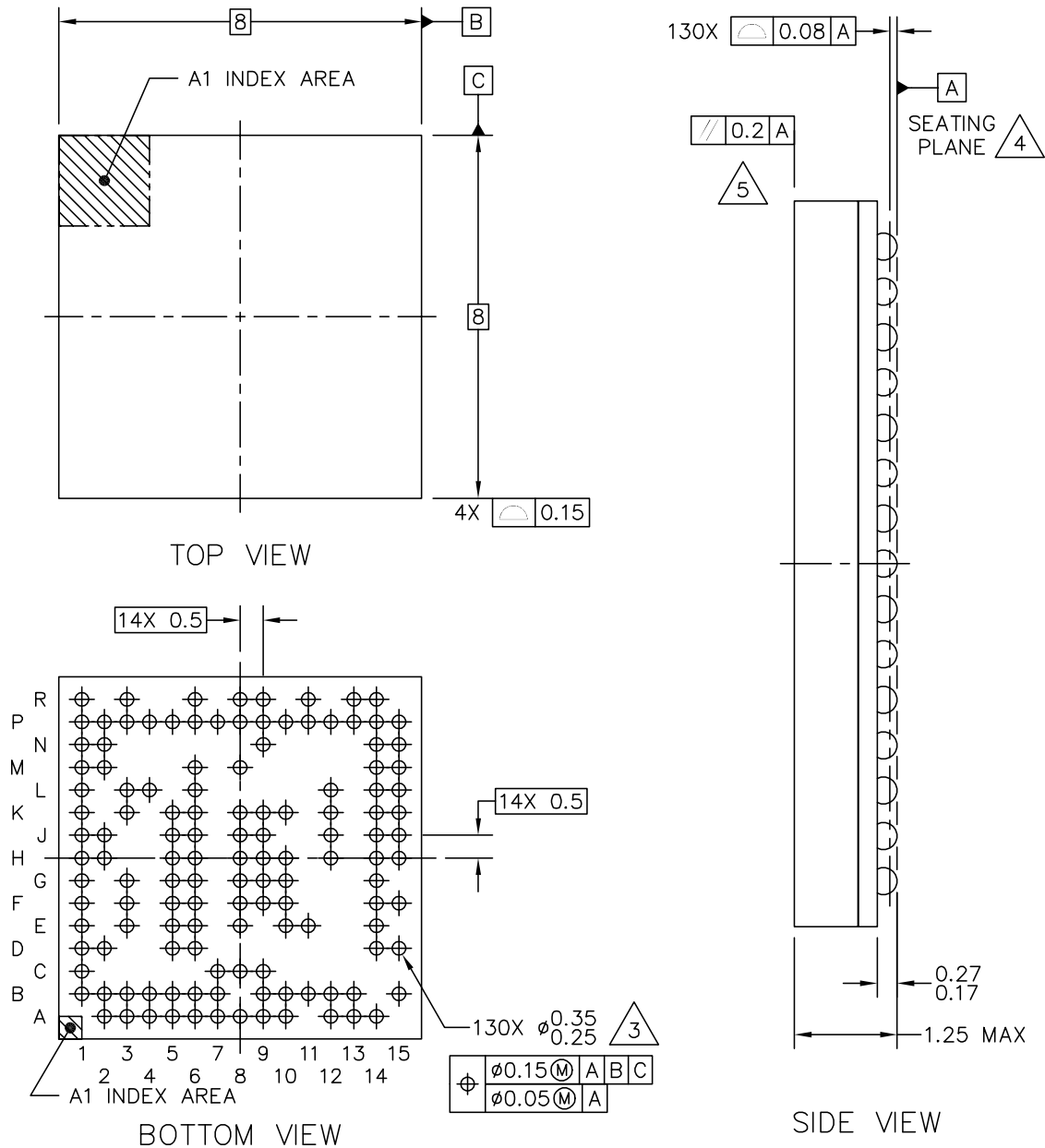
9.1 Packaging Mechanical Dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.freescale.com and perform a keyword search for the drawing's document number.

Table 134. Package Drawing Information

| Package | Suffix | Package Outline Drawing Number |
|---|--------|--------------------------------|
| 130-pin MAPBGA (8 x 8 mm), 0.5 mm pitch | VK | 98ASA00333D |

Dimensions shown are provided for reference ONLY (For Layout and Design, refer to the Package Outline Drawing listed in the following figures).



| | | | |
|--|-------------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: PBGA, THIN PROFILE, FINE PITCH, 130 I/O, 8 X 8 PKG, 0.5 MM PITCH (MAP) | DOCUMENT NO: 98ASA00333D | | REV: 0 |
| | CASE NUMBER: 2200-01 | | 02 MAY 2011 |
| | STANDARD: JEDEC MO-275-CCCE-1 | | |

VK SUFFIX
130-PIN
98ASA00333D
REVISION 0

Figure 28. 8 x 8 Package Mechanical Dimension

NOTES:

- 1. ALL DIMENSIONS IN MILLIMETERS.
- 2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
- 3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
- 4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
- 5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

| | | | | | |
|---|--|--------------------|-------------------------------|----------------------------|-------------|
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| TITLE: PBGA, THIN PROFILE, FINE PITCH, 130 I/O, 8 X 8 PKG, 0.5 MM PITCH (MAP) | | | DOCUMENT NO: 98ASA00333D | | REV: 0 |
| | | | CASE NUMBER: 2200–01 | | 02 MAY 2011 |
| | | | STANDARD: JEDEC MO–275–CCCE–1 | | |

VK SUFFIX
130-PIN
98ASA00333D
REVISION 0

Figure 29. 8 x 8 Package Mechanical Dimension

10 Reference Section

Table 135. MC34709 Reference Documents

| Reference | Description |
|-----------|----------------------|
| MC34709FS | Freescale Fact Sheet |
| MC34709ER | Freescale Errata |

11 Revision History

| REVISION | DATE | DESCRIPTION OF CHANGES |
|----------|---------|---|
| 1.0 | 8/2012 | <ul style="list-style-type: none"> Initial release Corrected doc number to MC34709, corrected part number PC34709VK |
| 2.0 | 10/2012 | <ul style="list-style-type: none"> Deleted columns Rating and Balls from Table 3 Updated table 4 with Maximum Rating for all pins <ul style="list-style-type: none"> Updated BP max rating to 4.8 Updated LICELL Max rating to 3.8V Added table 7. Recommended operational conditions Renamed Table 8 from General Electrical Characteristics to Pin Logic Threshold Table 9, Updated maximum current consumption on RTC/POWER cut mode to 8.0uA Table 9, Removed current consumption in ON mode. Table 13, Typical voltage of VCOREDIG in Off with good battery and RTC mode corrected to 1.2 V Removed PWMPS switching mode, not supported Removed $I_{SWxTRANSIENT}$ specification from all SWx regulators Updated Table 43, Reserved set point 27 through 31 Updated Table 45, Reserved set point 27 through 31 Updated Boost output capacitor to 2 x 22uF (Figure 17, Table 133) Removed Short Circuit Protection section, SCP no longer supported. Specification removed from VUSB, VUSB2, VDAC, VGEN1 and VGEN2 Updated LDOS current limit specification, added Min and Max. (Tables 55, 56, 57, 64) Corrected LDOs with external FET current limit to show base drive current limit specification (VUSB2, VDAC, VGEN2). Added Min and Max specification Corrected maximum pin Ratings on table 4. <ul style="list-style-type: none"> LICELL = 4.8 V VCOREREF = 1.5 V VDDL, VCOREDIG = 1.6 V VINPLL, VDACDRV, VUSB2DRV, VGEN2DRV = 4.8 V Removed section 6.3 Table 51: deleted typical value of I_{SWBST} and added maximum = 380 mA Updated LDOS current limit specification, removed Min and Max, added Typ. (Tables 55, 56, 57, 64) Corrected LDOs base drive current limit specification (VUSB2, VDAC, VGEN2). removed Min and Max value and added Typ. Modify External components values on Figure 24. Update values on figure 24 and Table 33. Bill of Material. |
| 3.0 | 2/2013 | <ul style="list-style-type: none"> Removed min and max on Output Voltage VOUT, and changed typical on Load Regulation. Removed note on Tables 56 |
| 4.0 | 11/2013 | <ul style="list-style-type: none"> Updated section Oscillator Specifications Added note ⁽³⁵⁾ to the VSRTC Electrical Specifications table |

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Rev. 4.0
11/2013

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