

**FEATURES**

1 pC charge injection  
 $\pm 0.1$  nA maximum at 25°C leakage currents  
85  $\Omega$  on resistance  
Rail-to-rail switching operation  
Fast switching times  
16-lead TSSOP  
Typical power consumption:  $\leq 11$  nW  
TTL-/CMOS-compatible inputs  
 $V_{SS}$  to  $V_{DD}$  analog signal range  
 $\pm 2.7$  V to  $\pm 5.5$  V dual supply operation  
2.7 V to 5.5 V single-supply operation  
Fully specified at  $\pm 5$  V, 3 V, and 5 V

**ENHANCED PRODUCT FEATURES**

Supports defense and aerospace applications  
(AQEC standard)  
Military temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$   
Controlled manufacturing baseline  
1 assembly site  
1 test site  
1 fabrication site  
Enhanced product change notification  
Qualification data available on request

**APPLICATIONS**

Automatic test equipment  
Data acquisition systems  
Battery-powered systems  
Communications systems  
Sample-and-hold systems  
Audio signal routing  
Relay replacement  
Avionics

**GENERAL DESCRIPTION**

The **ADG613-EP** is a monolithic CMOS device containing four independently selectable switches. This switch offers ultralow charge injection of 1 pC over the full input signal range and typical leakage currents of 0.01 nA at 25°C.

The device is fully specified for  $\pm 5$  V, 5 V, and 3 V supplies. It contains four independent single-pole, single-throw (SPST) switches. The **ADG613-EP** contains two switches with digital control logic that turns on with logic low and two switches in which the logic is inverted.

Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The

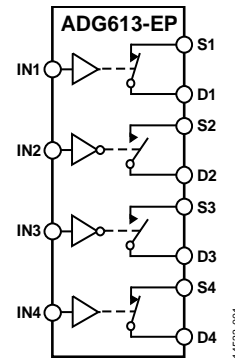
**FUNCTIONAL BLOCK DIAGRAM**

Figure 1.

**ADG613-EP** exhibits break-before-make switching action.

The **ADG613-EP** is available in a small, 16-lead TSSOP package.

The **ADG613-EP** is also a TTL-compatible device.

Additional application and technical information can be found in the **ADG613** data sheet.

**PRODUCT HIGHLIGHTS**

1. Ultralow charge injection (1 pC typically).
2. Dual  $\pm 2.7$  V to  $\pm 5.5$  V or single 2.7 V to 5.5 V operation.
3. Temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .
4. Small, 16-lead TSSOP.

Rev. A

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**REVISION HISTORY**

**10/2016—Rev. 0 to Rev. A**

|   |   |
|---|---|
| Changes to Features Section and Enhanced Product<br>Features Section..... | 1 |
|---|---|

**6/2016—Revision 0: Initial Revision**

## SPECIFICATIONS

### DUAL-SUPPLY OPERATION

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.  $V_S$  is the source voltage.  $V_D$  is the drain voltage.

Table 1.

| Parameter  | 25°C       | -55°C to +125°C      | Unit              | Test Conditions/Comments   |
|--|------------|----------------------|-------------------|--|
| <b>ANALOG SWITCH</b>   |            |                      |                   |  |
| Analog Signal Range  |            | $V_{SS}$ to $V_{DD}$ | V                 |  |
| On Resistance, $R_{ON}$  | 85         |                      | $\Omega$ typ      | $V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 14  |
|  | 115        | 160                  | $\Omega$ max      | $V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 14  |
| On-Resistance Match Between Channels, $\Delta R_{ON}$                | 2          |                      | $\Omega$ typ      | $V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$  |
|  | 4          | 6.5                  | $\Omega$ max      | $V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$  |
| On-Resistance Flatness, $R_{FLAT(ON)}$                               | 25         |                      | $\Omega$ typ      | $V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$  |
|  | 40         | 60                   | $\Omega$ max      | $V_S = \pm 3\text{ V}$ , $I_S = -1\text{ mA}$  |
| <b>LEAKAGE CURRENTS</b>  |            |                      |                   |  |
| Source Off Leakage, $I_{S(OFF)}$                                     | $\pm 0.01$ |                      | nA typ            | $V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$<br>$V_D = \pm 4.5\text{ V}$ , $V_S = \mp 4.5\text{ V}$ ; see Figure 15 |
|  | $\pm 0.1$  | $\pm 2$              | nA max            | $V_D = \pm 4.5\text{ V}$ , $V_S = \mp 4.5\text{ V}$ ; see Figure 15  |
| Drain Off Leakage, $I_{D(OFF)}$                                      | $\pm 0.01$ |                      | nA typ            | $V_D = \pm 4.5\text{ V}$ , $V_S = \mp 4.5\text{ V}$ ; see Figure 15  |
|  | $\pm 0.1$  | $\pm 2$              | nA max            | $V_D = \pm 4.5\text{ V}$ , $V_S = \mp 4.5\text{ V}$ ; see Figure 15  |
| Channel On Leakage, $I_{D(ON)}$ , $I_{S(ON)}$                        | $\pm 0.01$ |                      | nA typ            | $V_D = V_S = \pm 4.5\text{ V}$ ; see Figure 16   |
|  | $\pm 0.1$  | $\pm 6$              | nA max            | $V_D = V_S = \pm 4.5\text{ V}$ ; see Figure 16   |
| <b>DIGITAL INPUTS</b>  |            |                      |                   |  |
| Input High Voltage, $V_{INH}$  |            | 2.4                  | V min             |  |
| Input Low Voltage, $V_{INL}$   |            | 0.8                  | V max             |  |
| Input Current, $I_{INL}$ or $I_{INH}$                                | 0.005      |                      | $\mu\text{A}$ typ | $V_{IN} = V_{INL}$ or $V_{INH}$  |
|  |            | $\pm 0.1$            | $\mu\text{A}$ max | $V_{IN} = V_{INL}$ or $V_{INH}$  |
| Digital Input Capacitance, $C_{IN}$                                  | 2          |                      | pF typ            |  |
| <b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>                           |            |                      |                   |  |
| Delay from Digital Control Input and Output Switching On, $t_{ON}$   | 45         |                      | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3.0\text{ V}$ ; see Figure 17  |
|  | 65         | 90                   | ns max            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3.0\text{ V}$ ; see Figure 17  |
| Delay from Digital Control Input and Output Switching Off, $t_{OFF}$ | 25         |                      | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3.0\text{ V}$ ; see Figure 17  |
|  | 40         | 50                   | ns max            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3.0\text{ V}$ ; see Figure 17  |
| Break-Before-Make Time Delay, $t_{BBM}$                              | 15         |                      | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3.0\text{ V}$ ; see Figure 18                              |
|  |            | 10                   | ns min            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3.0\text{ V}$ ; see Figure 18                              |
| Charge Injection   | -0.5       |                      | pC typ            | $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 19   |
| Off Isolation  | -65        |                      | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ ; see Figure 20   |
| Channel to Channel Crosstalk   | -90        |                      | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ ; see Figure 21   |
| -3 dB Bandwidth  | 680        |                      | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 22   |
| Off Switch Source Capacitance, $C_{S(OFF)}$                          | 5          |                      | pF typ            | $f = 1\text{ MHz}$   |
| Off Switch Drain Capacitance, $C_{D(OFF)}$                           | 5          |                      | pF typ            | $f = 1\text{ MHz}$   |
| On Switch Capacitance, $C_{D(ON)}$ , $C_{S(ON)}$                     | 5          |                      | pF typ            | $f = 1\text{ MHz}$   |
| <b>POWER REQUIREMENTS</b>  |            |                      |                   |  |
| Positive Supply Current, $I_{DD}$                                    | 0.001      |                      | $\mu\text{A}$ typ | $V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$<br>Digital inputs = 0 V or 5.5 V                                       |
|  |            | 1.0                  | $\mu\text{A}$ max | Digital inputs = 0 V or 5.5 V  |
| Negative Supply Current, $I_{SS}$                                    | 0.001      |                      | $\mu\text{A}$ typ | Digital inputs = 0 V or 5.5 V  |
|  |            | 1.0                  | $\mu\text{A}$ max | Digital inputs = 0 V or 5.5 V  |
| $V_{DD}/V_{SS}$  |            | $\pm 2.7$            | V min             |  |
|  |            | $\pm 5.5$            | V max             |  |
| Power Consumption  | 11         |                      | nW typ            |  |
|  | 11         |                      | $\mu\text{W}$ max |  |

<sup>1</sup> Guaranteed by design; not subject to production test.

## SINGLE-SUPPLY OPERATION

$V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.  $V_S$  is the source voltage.  $V_D$  is the drain voltage.

Table 2.

| Parameter  | 25°C       | -55°C to +125°C | Unit              | Test Conditions/Comments   |
|--|------------|-----------------|-------------------|--|
| <b>ANALOG SWITCH</b>                                     |            |                 |                   |  |
| Analog Signal Range                                      |            | 0 to $V_{DD}$   | V                 |  |
| On Resistance, $R_{ON}$                                  | 210        |                 | $\Omega$ typ      | $V_S = 3.5\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 14  |
|  | 290        | 380             | $\Omega$ max      | $V_S = 3.5\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 14  |
| On-Resistance Match<br>Between Channels, $\Delta R_{ON}$ | 3          |                 | $\Omega$ typ      | $V_S = 3.5\text{ V}$ , $I_S = -1\text{ mA}$  |
|  | 10         | 13              | $\Omega$ max      | $V_S = 3.5\text{ V}$ , $I_S = -1\text{ mA}$  |
| <b>LEAKAGE CURRENTS</b>                                  |            |                 |                   |  |
| Source Off Leakage, $I_{S(OFF)}$                         | $\pm 0.01$ |                 | nA typ            | $V_{DD} = 5.5\text{ V}$<br>$V_S = 1\text{ V}$ or $4.5\text{ V}$ , $V_D = 4.5\text{ V}$ or $1\text{ V}$ ; see Figure 15 |
|  | $\pm 0.1$  | $\pm 2$         | nA max            | $V_S = 1\text{ V}$ or $4.5\text{ V}$ , $V_D = 4.5\text{ V}$ or $1\text{ V}$ ; see Figure 15                            |
| Drain Off Leakage, $I_{D(OFF)}$                          | $\pm 0.01$ |                 | nA typ            | $V_S = 1\text{ V}$ or $4.5\text{ V}$ , $V_D = 4.5\text{ V}$ or $1\text{ V}$ ; see Figure 15                            |
|  | $\pm 0.1$  | $\pm 2$         | nA max            | $V_S = 1\text{ V}$ or $4.5\text{ V}$ , $V_D = 4.5\text{ V}$ or $1\text{ V}$ ; see Figure 15                            |
| Channel On Leakage, $I_{D(ON)}$ , $I_{S(ON)}$            | $\pm 0.01$ |                 | nA typ            | $V_S = V_D = 1\text{ V}$ or $4.5\text{ V}$ ; see Figure 16   |
|  | $\pm 0.1$  | $\pm 6$         | nA max            | $V_S = V_D = 1\text{ V}$ or $4.5\text{ V}$ ; see Figure 16   |
| <b>DIGITAL INPUTS</b>                                    |            |                 |                   |  |
| Input High Voltage, $V_{INH}$                            |            | 2.4             | V min             |  |
| Input Low Voltage, $V_{INL}$                             |            | 0.8             | V max             |  |
| Input Current, $I_{INL}$ or $I_{INH}$                    | 0.005      |                 | $\mu\text{A}$ typ | $V_{IN} = V_{INL}$ or $V_{INH}$  |
|  |            | $\pm 0.1$       | $\mu\text{A}$ max | $V_{IN} = V_{INL}$ or $V_{INH}$  |
| Digital Input Capacitance, $C_{IN}$                      | 2          |                 | pF typ            |  |
| <b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>               |            |                 |                   |  |
| $t_{ON}$   | 70         |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3.0\text{ V}$ ; see Figure 17                                      |
|  | 100        | 150             | ns max            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3.0\text{ V}$ ; see Figure 17                                      |
| $t_{OFF}$  | 25         |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3.0\text{ V}$ ; see Figure 17                                      |
|  | 40         | 50              | ns max            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 3.0\text{ V}$ ; see Figure 17                                      |
| Break-Before-Make Time Delay, $t_{BBM}$                  | 25         |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3.0\text{ V}$ ; see Figure 18                          |
|  |            | 10              | ns min            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3.0\text{ V}$ ; see Figure 18                          |
| Charge Injection   | 1          |                 | pC typ            | $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 19   |
| Off Isolation  | -62        |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ ; see Figure 20   |
| Channel to Channel Crosstalk                             | -90        |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ ; see Figure 21   |
| -3 dB Bandwidth  | 680        |                 | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 22   |
| $C_{S(OFF)}$   | 5          |                 | pF typ            | $f = 1\text{ MHz}$   |
| $C_{D(OFF)}$   | 5          |                 | pF typ            | $f = 1\text{ MHz}$   |
| $C_{D(ON)}$ , $C_{S(ON)}$                                | 5          |                 | pF typ            | $f = 1\text{ MHz}$   |
| <b>POWER REQUIREMENTS</b>                                |            |                 |                   |  |
| $I_{DD}$   | 0.001      |                 | $\mu\text{A}$ typ | $V_{DD} = 5.5\text{ V}$<br>Digital inputs = 0 V or 5.5 V   |
|  |            | 1.0             | $\mu\text{A}$ max | Digital inputs = 0 V or 5.5 V  |
| $V_{DD}$   |            | 2.7             | V min             |  |
|  |            | 5.5             | V max             |  |
| Power Consumption  | 5.5        |                 | nW typ            |  |
|  | 5.5        |                 | $\mu\text{W}$ max |  |

<sup>1</sup> Guaranteed by design; not subject to production test.

$V_{DD} = 3\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.  $V_S$  is the source voltage.  $V_D$  is the drain voltage.

Table 3.

| Parameter                                     | 25°C       | -55°C to +125°C | Unit              | Test Conditions/Comments   |
|---|------------|-----------------|-------------------|--|
| <b>ANALOG SWITCH</b>                          |            |                 |                   |  |
| Analog Signal Range                           |            | 0 to $V_{DD}$   | V                 |  |
| On Resistance, $R_{ON}$                       | 380        | 460             | $\Omega$ typ      | $V_S = 1.5\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 14  |
| <b>LEAKAGE CURRENTS</b>                       |            |                 |                   |  |
| Source Off Leakage, $I_{S(OFF)}$              | $\pm 0.01$ |                 | nA typ            | $V_{DD} = 3.3\text{ V}$<br>$V_S = 1\text{ V}$ or $3\text{ V}$ , $V_D = 3\text{ V}$ or $1\text{ V}$ ; see Figure 15 |
|   | $\pm 0.1$  | $\pm 2$         | nA max            | $V_S = 1\text{ V}$ or $3\text{ V}$ , $V_D = 3\text{ V}$ or $1\text{ V}$ ; see Figure 15                            |
| Drain Off Leakage, $I_{D(OFF)}$               | $\pm 0.01$ |                 | nA typ            | $V_S = 1\text{ V}$ or $3\text{ V}$ , $V_D = 3\text{ V}$ or $1\text{ V}$ ; see Figure 15                            |
|   | $\pm 0.1$  | $\pm 2$         | nA max            | $V_S = 1\text{ V}$ or $3\text{ V}$ , $V_D = 3\text{ V}$ or $1\text{ V}$ ; see Figure 15                            |
| Channel On Leakage, $I_{D(ON)}$ , $I_{S(ON)}$ | $\pm 0.01$ |                 | nA typ            | $V_S = V_D = 1\text{ V}$ or $3\text{ V}$ ; see Figure 16   |
|   | $\pm 0.1$  | $\pm 6$         | nA max            | $V_S = V_D = 1\text{ V}$ or $3\text{ V}$ ; see Figure 16   |
| <b>DIGITAL INPUTS</b>                         |            |                 |                   |  |
| Input High Voltage, $V_{INH}$                 |            | 2.0             | V min             |  |
| Input Low Voltage, $V_{INL}$                  |            | 0.8             | V max             |  |
| Input Current, $I_{INL}$ or $I_{INH}$         | 0.005      |                 | $\mu\text{A}$ typ | $V_{IN} = V_{INL}$ or $V_{INH}$  |
|   |            | $\pm 0.1$       | $\mu\text{A}$ max | $V_{IN} = V_{INL}$ or $V_{INH}$  |
| Digital Input Capacitance, $C_{IN}$           | 2          |                 | pF typ            |  |
| <b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>    |            |                 |                   |  |
| $t_{ON}$                                      | 130        |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 2\text{ V}$ ; see Figure 17                                    |
|   | 185        | 260             | ns max            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 2\text{ V}$ ; see Figure 17                                    |
| $t_{OFF}$                                     | 40         |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 2\text{ V}$ ; see Figure 17                                    |
|   | 55         | 65              | ns max            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_S = 2\text{ V}$ ; see Figure 17                                    |
| Break-Before-Make Time Delay, $t_{BBM}$       | 50         | 10              | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 2\text{ V}$ ; see Figure 18                        |
|   |            |                 | ns min            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 2\text{ V}$ ; see Figure 18                        |
| Charge Injection                              | 1.5        |                 | pC typ            | $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 19                                       |
| Off Isolation                                 | -62        |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ ; see Figure 20                                     |
| Channel to Channel Crosstalk                  | -90        |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 10\text{ MHz}$ ; see Figure 21                                     |
| -3 dB Bandwidth                               | 680        |                 | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 22   |
| $C_{S(OFF)}$                                  | 5          |                 | pF typ            | $f = 1\text{ MHz}$   |
| $C_{D(OFF)}$                                  | 5          |                 | pF typ            | $f = 1\text{ MHz}$   |
| $C_{D(ON)}$ , $C_{S(ON)}$                     | 5          |                 | pF typ            | $f = 1\text{ MHz}$   |
| <b>POWER REQUIREMENTS</b>                     |            |                 |                   |  |
| $I_{DD}$                                      | 0.001      |                 | $\mu\text{A}$ typ | $V_{DD} = 3.3\text{ V}$  |
|   |            | 1.0             | $\mu\text{A}$ max | Digital inputs = 0 V or 3.3 V  |
| $V_{DD}$                                      |            | 2.7             | V min             | Digital inputs = 0 V or 3.3 V  |
|   |            | 5.5             | V max             |  |
| Power Consumption                             | 3.3        |                 | nW typ            |  |
|   | 3.3        |                 | $\mu\text{W}$ max |  |

<sup>1</sup> Guaranteed by design; not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted

Table 4.

| Parameter                             | Rating  |
|---------------------------------------|---|
| $V_{DD}$ to $V_{SS}$ <sup>1</sup>     | 13 V  |
| $V_{DD}$ to GND <sup>1</sup>          | -0.3 V to +6.5 V  |
| $V_{SS}$ to GND <sup>1</sup>          | +0.3 V to -6.5 V  |
| Analog Inputs <sup>2</sup>            | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$                      |
| Digital Inputs <sup>2</sup>           | GND - 0.3 V to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first |
| Peak Current, Sx or Dx                | 20 mA (pulsed at 1 ms, 10% duty cycle maximum)                          |
| Continuous Current, Sx or Dx          | 10 mA   |
| 3 V Operation, 85°C to 125°C          | 7.5 mA  |
| Operating Temperature Range           | -55°C to +125°C   |
| Storage Temperature Range             | -65°C to +150°C   |
| Junction Temperature                  | 150°C   |
| $\theta_{JA}$ Thermal Impedance       |   |
| 16-Lead TSSOP                         | 150.4°C/W   |
| Lead Soldering                        |   |
| Lead Temperature, Soldering (10 sec)  | 300°C   |
| IR Reflow, Peak Temperature (<20 sec) | 220°C   |
| Pb-Free Soldering                     |   |
| Reflow, Peak Temperature              | 260 (+0/-5)°C   |
| Time at Peak Temperature              | 20 sec to 40 sec  |

<sup>1</sup> Tested at -55°C to +125°C.

<sup>2</sup> Overvoltages at INx, Sx, or Dx are clamped by internal diodes. Limit the current to the maximum ratings given. Tested at -55°C to +125°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

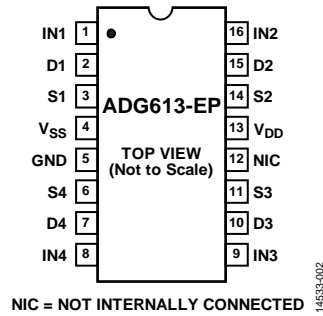


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic        | Description   |
|---------|-----------------|---|
| 1       | IN1             | Switch 1 Digital Control Input.   |
| 2       | D1              | Drain Terminal of Switch 1. This pin can be an input or output.   |
| 3       | S1              | Source Terminal of Switch 1. This pin can be an input or output.  |
| 4       | V <sub>SS</sub> | Most Negative Power Supply Terminal. Tie this pin to GND when using the device with single-supply voltages. |
| 5       | GND             | Ground (0 V) Reference.   |
| 6       | S4              | Source Terminal of Switch 4. This pin can be an input or output.  |
| 7       | D4              | Drain Terminal of Switch 4. This pin can be an input or output.   |
| 8       | IN4             | Switch 4 Digital Control Input.   |
| 9       | IN3             | Switch 3 Digital Control Input.   |
| 10      | D3              | Drain Terminal of Switch 3. This pin can be an input or output.   |
| 11      | S3              | Source Terminal of Switch 3. This pin can be an input or output.  |
| 12      | NIC             | Not Internally Connected.   |
| 13      | V <sub>DD</sub> | Most Positive Power Supply Terminal.  |
| 14      | S2              | Source Terminal of Switch 2. This pin can be an input or output.  |
| 15      | D2              | Drain Terminal of Switch 2. This pin can be an input or output.   |
| 16      | IN2             | Switch 2 Digital Control Input.   |

Table 6. Truth Table

| Logic | S1 and S4 | S2 and S3 |
|-------|-----------|-----------|
| 0     | Off       | On        |
| 1     | On        | Off       |

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 3. On Resistance vs.  $V_D, V_S$ ; Dual Supplies



Figure 6. On Resistance vs.  $V_D, V_S$  for Various Temperatures, Single Supply

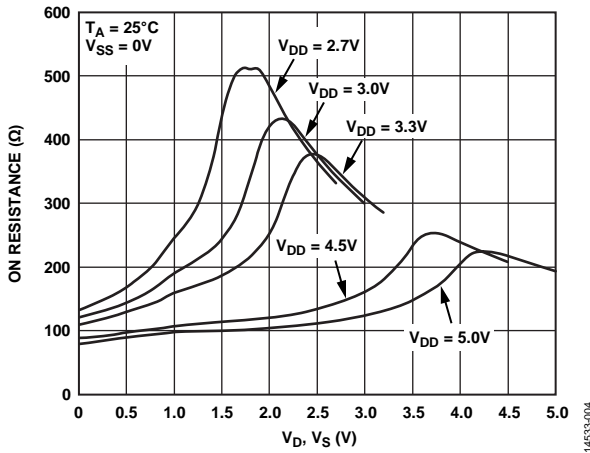


Figure 4. On Resistance vs.  $V_D, V_S$ ; Single Supply

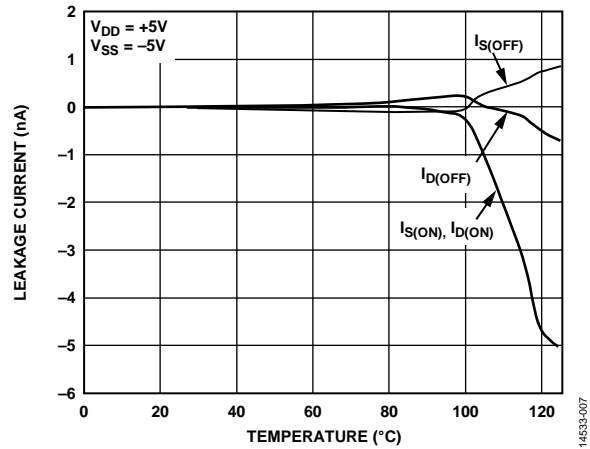


Figure 7. Leakage Current vs. Temperature, Dual Supplies



Figure 5. On Resistance vs.  $V_D, V_S$  for Various Temperatures, Dual Supplies



Figure 8. Leakage Current vs. Temperature, Single Supply





Figure 9. Charge Injection ( $Q_{INJ}$ ) vs. Source Voltage ( $V_S$ )

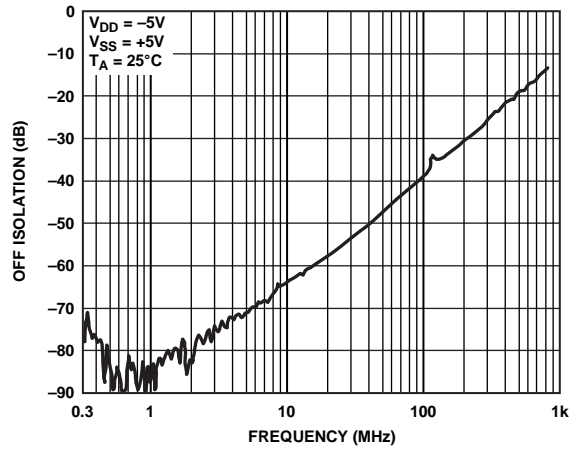


Figure 12. Off Isolation vs. Frequency

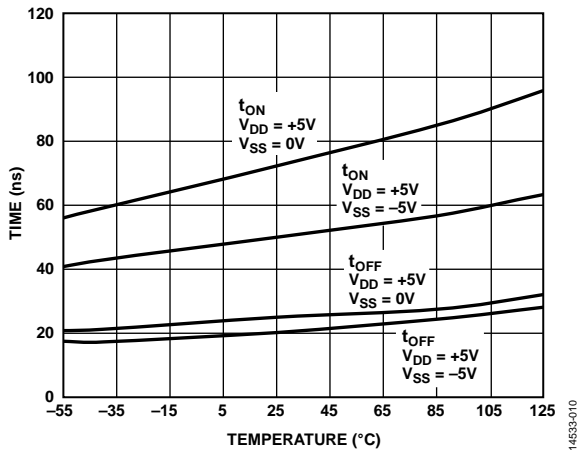


Figure 10.  $t_{ON}/t_{OFF}$  Times vs. Temperature

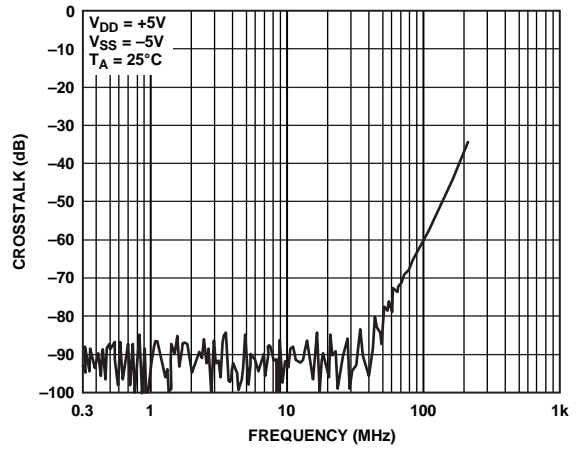


Figure 13. Crosstalk vs. Frequency



Figure 11. On Response vs. Frequency

TEST CIRCUITS

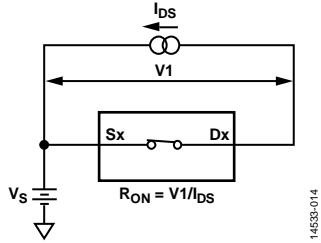


Figure 14. On Resistance



Figure 15. Off Leakage



Figure 16. On Leakage

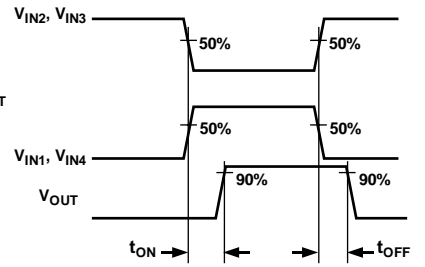
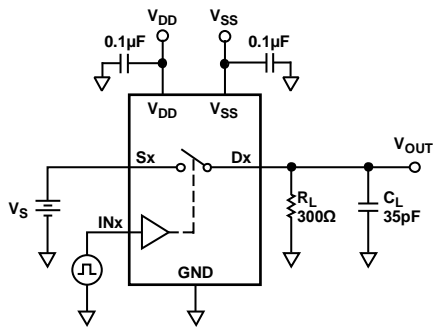


Figure 17. Switching Times

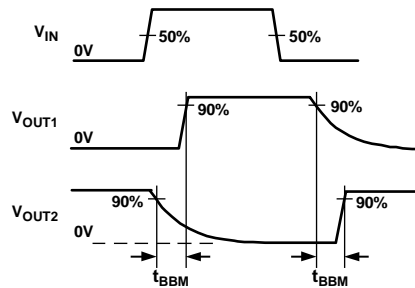
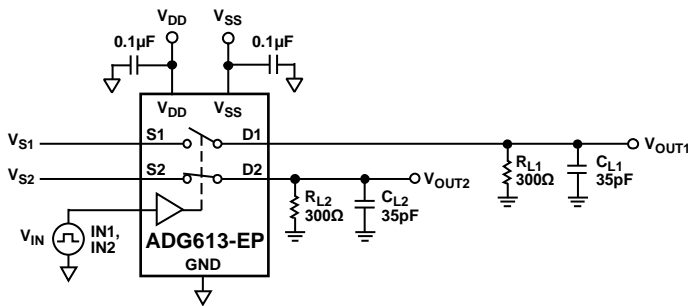


Figure 18. Break-Before-Make Time Delay

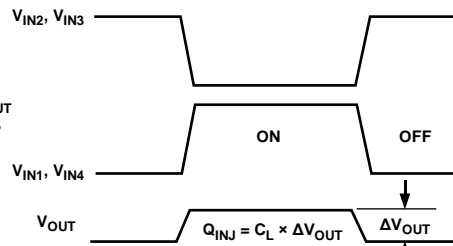
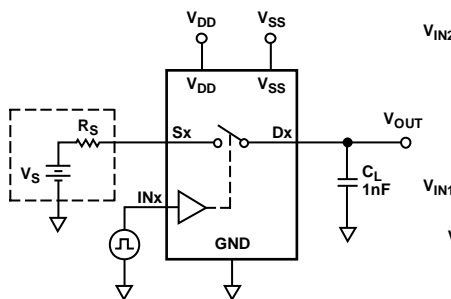


Figure 19. Charge Injection



Figure 20. Off Isolation



Figure 22. Bandwidth



Figure 21. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 23. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters

ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                               | Package Option |
|--------------------|-------------------|---|----------------|
| ADG613SRUZ-EP      | -55°C to +125°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16          |
| ADG613SRUZ-EP-RL7  | -55°C to +125°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP] | RU-16          |

<sup>1</sup> Z = RoHS Compliant Part.

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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