

General Description

The SY89251V is a differential PECL/ECL receiver/buffer in a space saving (2mm x 2mm) DFN package. The device is functionally equivalent to the SY100EL16VC, except for an active HIGH enable pin and a 70% smaller footprint. It is also equivalent to the SY89250V, except for an active HIGH enable pin. It provides a V_{BB} output for either single-ended application or as a DC bias for AC-coupling to the device.

The SY89251V provides an EN input which is synchronized with the data input (D) signal in a way that provides glitchless gating of the Q_{HG} and $/Q_{HG}$ outputs.

When the EN signal is HIGH, the input is passed to the outputs and the data output equals the data input. When the data input is HIGH and the EN goes LOW, it will force the Q_{HG} LOW and the $/Q_{HG}$ HIGH on the next negative transition of the data input. If the data input is LOW when the EN goes LOW, the next data transition to a HIGH is ignored and Q_{HG} remains LOW and $/Q_{HG}$ remains HIGH.

The next positive transition of the data input is not passed on to the data outputs under these conditions. The Q_{HG} and $/Q_{HG}$ outputs remain in their disabled state as long as the EN input is held LOW. The EN input has no influence on the $/Q$ output and the data input is passed on (inverted) to this output whether EN is HIGH or LOW. This configuration is ideal for crystal oscillator applications, where the oscillator can be free running and gated on and off synchronously without adding extra counts to the output.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

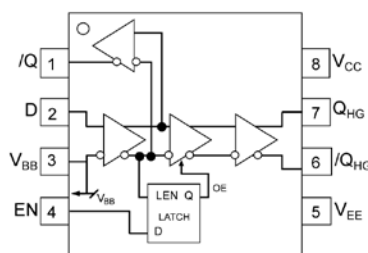
Features

- 3.3V and 5V power supply options
- 250ps propagation delay
- Very high voltage gain
- Ideal for pulse amplifier and limiting amplifier applications
- Data synchronous enable/disable (EN) on Q_{HG} and $/Q_{HG}$ provides for complete glitchless gating of the outputs
- Ideal for gating timing signals
- Complete solution for high quality, high frequency crystal oscillator applications
- Available in an ultra-small 8-pin (2mm x 2mm) DFN package

Applications

- Oscillator modules

Block Diagram



Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89251VMI	DFN-8	Industrial	251	Sn-Pb
SY89251VMITR ⁽²⁾	DFN-8	Industrial	251	Sn-Pb
SY89251VMG	DFN-8	Industrial	251 with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY89251VMGTR ⁽²⁾	DFN-8	Industrial	251 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

- Contact factory for die availability. Dice are guaranteed at $T_A = 25^\circ\text{C}$, DC electricals only.
- Tape and Reel.

Pin Configuration



**8-Pin DFN
(Ultra-Small Outline)**

Truth Table

EN	QHG Output
0	Logic Low
1	Data

Pin Description

Pin Number	Pin Name	Type	Pin Function
1	/Q	100k	Single-Ended PECL/ECL Feedback Output.
2	D	100k	Single-Ended PECL/ECL Input: The signal input includes an internal 75k Ω pull-down resistor. If input is left open, Q output will default to LOW.
3	VBB	Reference Output Voltage	Bias Voltage: $V_{CC}-1.3\text{V}$. Used as reference voltage when AC-coupling to the D input. Max sink/source current is $\pm 0.5\text{mA}$.
4	EN	Enable Input	EN Input which is synchronized with data input (D) signal in a way that provides glitchless gating of Q_{HG} and $/Q_{HG}$ outputs. Includes internal 75k Ω pull-up resistor. Default is HIGH.
5	VEE Exposed Pad	Negative Power Supply	Negative Power Supply: V_{EE} and exposed pad must be tied to most negative supply. For PECL/LVPECL connect to ground.
6, 7	/QHG, QHG	100k	Differential PECL/ECL Output: QHG defaults to LOW and /QHG defaults to HIGH if D input is left open. See "Output Interface Applications" section for recommendations on terminations.
8	VCC	Positive Power Supply	Positive Power Supply: Bypass with 0.1 μF //0.01 μF low ESR capacitors as close to VCC pin as possible.

Absolute Maximum Ratings⁽¹⁾

Power Supply Voltage (V_{CC})	-0.5V to +6.0V
ECL Input Voltage (V_{IN})	0V to $V_{CC} + 0.5V$
Voltage Applied to Output at HIGH State (V_{OUT})	-0.5V to V_{CC}
Output Current (I_{OUT})	
Continuous	50mA
Surge	100mA
Lead Temperature (soldering, 20 sec.)	260°C
Storage Temperature (T_S)	-65°C to +150°C

Operating Ratings⁽²⁾

Power Supply Voltage $ V_{CC}-V_{EE} $	3.3V $\pm 10\%$ or 5V $\pm 10\%$
Ambient Temperature (T_A)	-40°C to +85°C
Package Thermal Resistance, ⁽³⁾	
DFN (θ_{JA}) Still-Air	93°C/W
DFN (ψ_{JB})	60°C/W

DC Electrical Characteristics⁽⁴⁾

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{EE}	Power Supply	$ V_{CC}-V_{EE} $	3.0	3.3	3.6	V
		$ V_{CC}-V_{EE} $	4.5	5.0	5.5	V
I_{EE}	Power Supply Current				46	mA
I_{IL}	Input Low Current	EN	-150			μA
V_{BB}	Output Reference Voltage		$V_{CC} - 1.38$	$V_{CC} - 1.32$	$V_{CC} - 1.26$	V

DC Electrical Characteristics⁽⁴⁾

$V_{CC} = +3.3V \pm 10\%$ or $+5V \pm 10\%$ and $V_{EE} = 0V$; $V_{CC} = 0V$ and $V_{EE} = -3.3V \pm 10\%$ or $-5V \pm 10\%$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	Note 4	$V_{CC} - 1.085$		$V_{CC} - 0.880$	V
V_{OL}	Output LOW Voltage	Note 4	$V_{CC} - 1.830$		$V_{CC} - 1.555$	V
V_{IH}	Input HIGH Voltage		$V_{CC} - 1.165$		$V_{CC} - 0.880$	V
V_{IL}	Input LOW Voltage		$V_{CC} - 1.810$		$V_{CC} - 1.475$	V
V_{PP}	Minimum Input Swing		150			mV
I_{IH}	Input HIGH Current	D			150	μA
I_{IL}	Input LOW Current	D	0.5			μA

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. Output loaded with 50 Ω to $V_{CC} - 2V$.

AC Electrical Characteristics

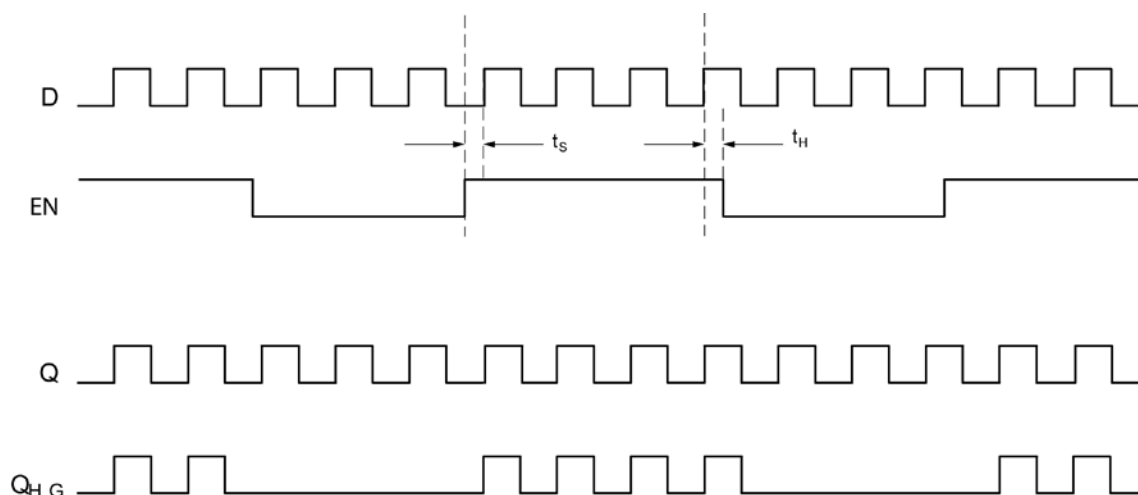
$V_{EE} = V_{EE}(\text{min})$ to $V_{EE}(\text{max})$; $V_{CC} = \text{GND}$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
t_{pd}	Propagation Delay to: /Q Output	D (Diff)			380	ps
		D (SE)			430	ps
	QHG, /QHG Output	D (Diff)			730	ps
		D (SE)			780	ps
t_S	Set-Up Time	EN	150			ps
t_H	Hold Time	EN	150			ps
t_{SKEW}	Duty Cycle Skew	(Diff)	Note 5	5	20	ps
V_{PP}	Minimum Input Swing	Note 6	150			mV
V_{CMR}	Common Mode Range	Note 7	-1.3		-0.4	V
t_r, t_f	Output /Q and QHG, /QHG Rise/Fall Times (20% to 80%)	At full output swing	100	225	350	ps

Notes:

- Duty cycle skew is the difference between a t_{pd} propagation delay through a device.
- Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ≈ 40 to Q, /Q outputs and a DC gain of ≈ 200 or higher to /Q_{HG}, Q_{HG} outputs.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{pp}(\text{min})$ and 1V. The lower end of the CMR range varies 1:1 with V_{EE} . The numbers in the spec table assume a nominal $V_{EE} = -3.3\text{V}$. Note for PECL operation, the $V_{CMR}(\text{min})$ will be fixed at $3.3\text{V} - |V_{CMR}(\text{min})|$.

Timing Diagram



Output Interface Applications

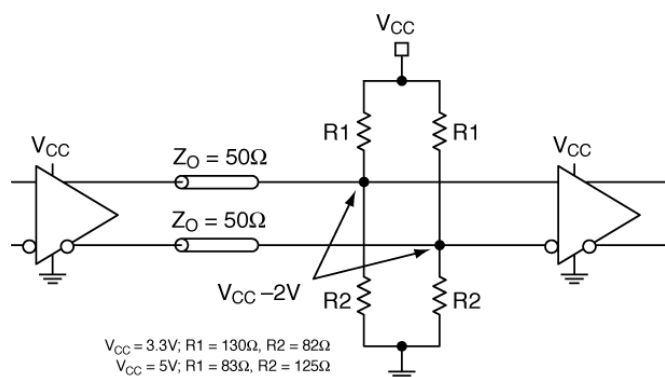


Figure 1a. Parallel Thevenin-Equivalent Termination

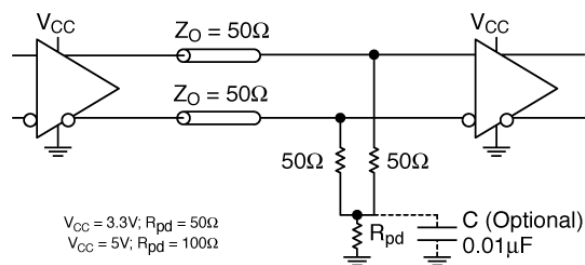


Figure 1b. Three Resistor "Y" Termination

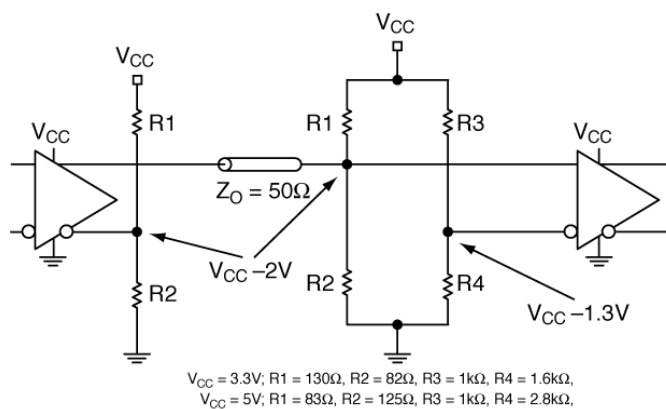
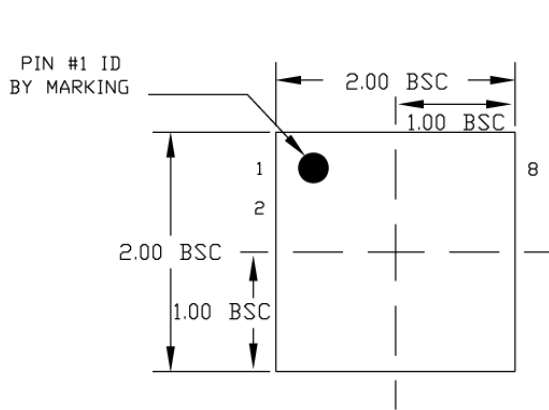
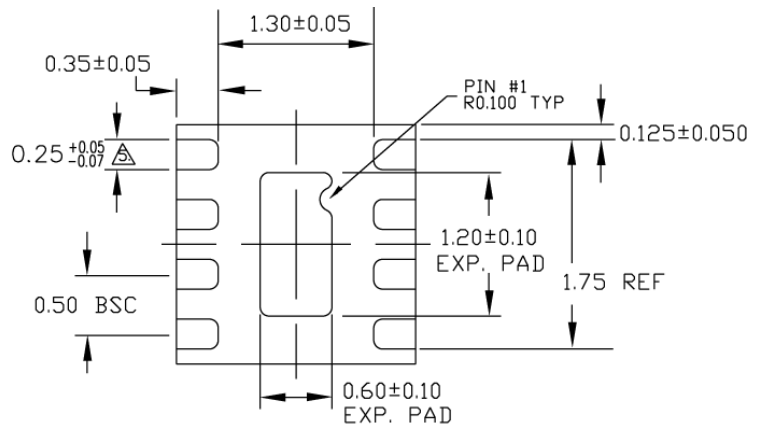


Figure 1c. Terminating Unused I/O

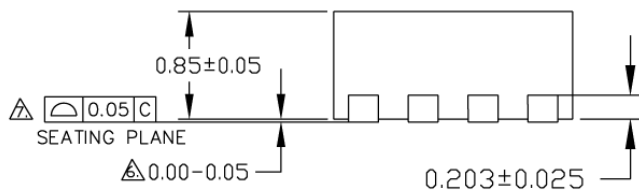
Package Information



TOP VIEW



BOTTOM VIEW

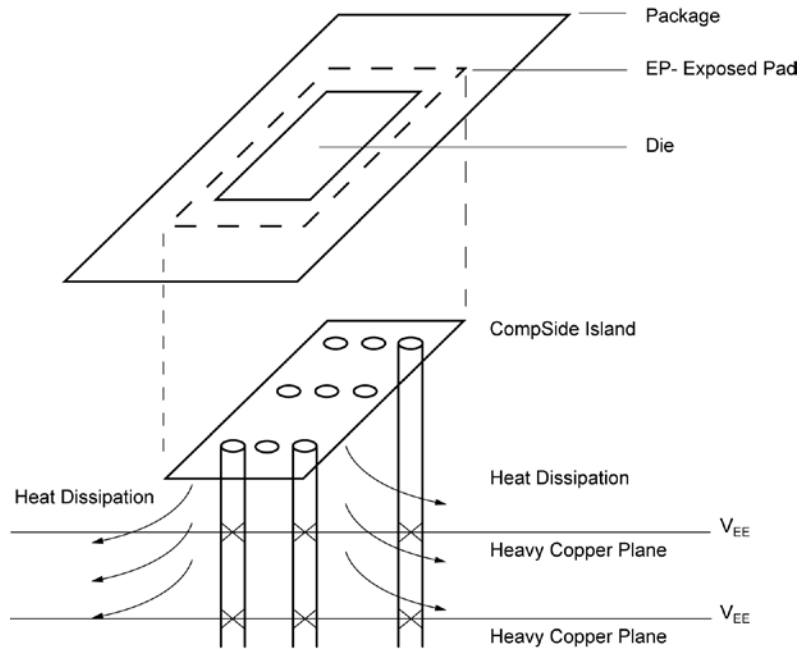


SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
 2. MAX. PACKAGE WARPAGE IS 0.05 mm.
 3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
 4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- △ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
 - △ APPLIED ONLY FOR TERMINALS.
 - △ APPLIED FOR EXPOSED PAD AND TERMINALS.

8-Pin Ultra-Small EPAD-DFN



PCB Thermal Consideration for 8-Pin DFN Package

Package Notes:

1. Packaging meets Leve 2 qualification.
2. All pasrts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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