

## ADG431/ADG432/ADG433

### FEATURES

- 44 V Supply Maximum Ratings**
- ±15 V Analog Signal Range**
- Low On Resistance (<24 Ω)**
- Ultralow Power Dissipation (3.9 μW)**
- Low Leakage (<0.25 nA)**
- Fast Switching Times**
  - $t_{ON} < 165 \text{ ns}$
  - $t_{OFF} < 130 \text{ ns}$
- Break-Before-Make Switching Action**
- TTL/CMOS Compatible**
- Plug-in Replacement for DG411/DG412/DG413**

### APPLICATIONS

- Audio and Video Switching**
- Automatic Test Equipment**
- Precision Data Acquisition**
- Battery Powered Systems**
- Sample Hold Systems**
- Communication Systems**

### GENERAL DESCRIPTION

The ADG431, ADG432 and ADG433 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC<sup>2</sup>MOS process which provides low power dissipation yet gives high switching speed and low on resistance.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. Fast switching speed coupled with high signal bandwidth also make the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

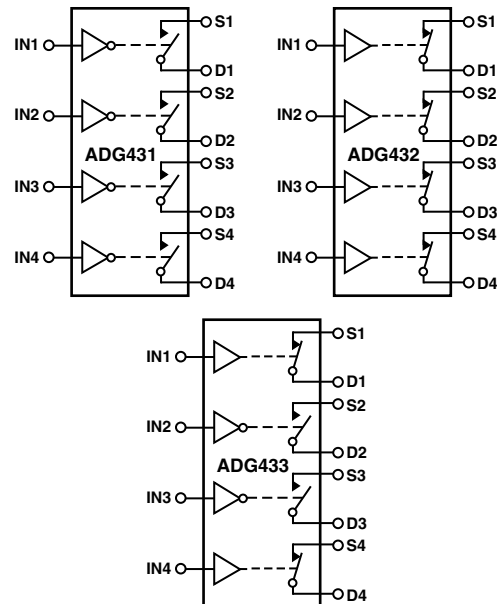
The ADG431, ADG432 and ADG433 contain four independent SPST switches. The ADG431 and ADG432 differ only in that the digital control logic is inverted. The ADG431 switches are turned on with a logic low on the appropriate control input, while a logic high is required for the ADG432. The ADG433 has two switches with digital control logic similar to that of the ADG431 while the logic is inverted on the other two switches.

Each switch conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break before make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

### REV. C

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### FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

### PRODUCT HIGHLIGHTS

1. **Extended Signal Range**  
The ADG431, ADG432 and ADG433 are fabricated on an enhanced LC<sup>2</sup>MOS process giving an increased signal range which extends fully to the supply rails.
2. **Ultralow Power Dissipation**
3. **Low R<sub>ON</sub>**
4. **Break-Before-Make Switching**  
This prevents channel shorting when the switches are configured as a multiplexer.
5. **Single Supply Operation**  
For applications where the analog signal is unipolar, the ADG431, ADG432, and ADG433 can be operated from a single rail power supply. The parts are fully specified with a single 12 V power supply and will remain functional with single supplies as low as 5 V.

# ADG431/ADG432/ADG433—SPECIFICATIONS<sup>1</sup>

**Dual Supply** ( $V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = +5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments	
	+25°C	-40°C to +85°C			
<b>ANALOG SWITCH</b>					
Analogue Signal Range		$V_{DD}$ to $V_{SS}$	V	$V_D = \pm 8.5\text{ V}$ , $I_S = -10\text{ mA}$ ; $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$	
$R_{ON}$	17		$\Omega$ typ		
	24	26	$\Omega$ max		
$R_{ON}$ vs. $V_D$ ( $V_S$ )	15		% typ		
$R_{ON}$ Drift	0.5		%/°C typ		
$R_{ON}$ Match	5		% typ	$V_D = 0\text{ V}$ , $I_S = -10\text{ mA}$	
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.05$		nA typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ $V_D = \pm 15.5\text{ V}$ , $V_S = \mp 15.5\text{ V}$ ; Test Circuit 2	
	$\pm 0.25$	$\pm 2$	nA max		
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.05$		nA typ		
	$\pm 0.25$	$\pm 2$	nA max		
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.1$		nA typ		$V_D = V_S = \pm 15.5\text{ V}$ ; Test Circuit 3
	$\pm 0.35$	$\pm 3$	nA max		
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$		2.4	V min	$V_{IN} = V_{INL}$ or $V_{INH}$	
Input Low Voltage, $V_{INL}$		0.8	V max		
Input Current					
$I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ		
		$\pm 0.02$	$\mu\text{A}$ max		
$C_{IN}$ Digital Input Capacitance	9		pF typ		
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>					
$t_{ON}$	90		ns typ	$V_{DD} = +15\text{ V}$ , $V_{SS} = -15\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = \pm 10\text{ V}$ ; Test Circuit 4	
		165	ns max		
$t_{OFF}$	60		ns typ		
		130	ns max		
Break-Before-Make Time Delay, $t_D$ (ADG433 Only)	25		ns typ		$V_S = \pm 10\text{ V}$ ; Test Circuit 4 $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = +10\text{ V}$ ; Test Circuit 5
Charge Injection	5		pC typ		
OFF Isolation	68		dB typ		$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 10\text{ nF}$ ; Test Circuit 6
Channel-to-Channel Crosstalk	85		dB typ		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
$C_S$ (OFF)	9		pF typ		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8
$C_D$ (OFF)	9		pF typ		$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	35		pF typ	$f = 1\text{ MHz}$	
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.0001		$\mu\text{A}$ typ	$V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ Digital Inputs = 0 V or 5 V	
	0.1	0.2	$\mu\text{A}$ max		
$I_{SS}$	0.0001		$\mu\text{A}$ typ		
	0.1	0.2	$\mu\text{A}$ max		
$I_L$	0.0001		$\mu\text{A}$ typ		
	0.1	0.2	$\mu\text{A}$ max		
Power Dissipation		7.7	$\mu\text{W}$ max		

## NOTES

<sup>1</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**Single Supply** ( $V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = 5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
$R_{ON}$	28		$\Omega$ typ	$0 < V_D < 8.5\text{ V}$ , $I_S = -10\text{ mA}$ ; $V_{DD} = 10.8\text{ V}$
	42	45	$\Omega$ max	
$R_{ON}$ vs. $V_D$ ( $V_S$ )	20		% typ	
$R_{ON}$ Drift	0.5		%/°C typ	
$R_{ON}$ Match	5		% typ	$V_D = 0\text{ V}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.04$		nA typ	$V_{DD} = 13.2\text{ V}$ $V_D = 12.2/1\text{ V}$ , $V_S = 1/12.2\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 2$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.04$		nA typ	$V_D = 12.2/1\text{ V}$ , $V_S = 1/12.2\text{ V}$ ; Test Circuit 2
	$\pm 0.25$	$\pm 2$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$		nA typ	$V_D = V_S = 12.2\text{ V}/1\text{ V}$ ; Test Circuit 3
	$\pm 0.3$	$\pm 3$	nA max	
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current				$V_{IN} = V_{INL}$ or $V_{INH}$
$I_{INL}$ or $I_{INH}$	0.005		$\mu\text{A}$ typ	
		$\pm 0.01$	$\mu\text{A}$ max	
$C_{IN}$ Digital Input Capacitance	9		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>				
$t_{ON}$	165		ns typ	$V_{DD} = 12\text{ V}$ , $V_{SS} = 0\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 8\text{ V}$ ; Test Circuit 4
		240	ns max	
$t_{OFF}$	60		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = 8\text{ V}$ ; Test Circuit 4
		115	ns max	
Break-Before-Make Time Delay, $t_D$ (ADG433 Only)	25		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = V_{S2} = 10\text{ V}$ ; Test Circuit 5
Charge Injection	25		pC typ	
OFF Isolation	68		dB typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 10\text{ nF}$ ; Test Circuit 6
Channel-to-Channel Crosstalk	85		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 7
$C_S$ (OFF)	9		pF typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; Test Circuit 8
$C_D$ (OFF)	9		pF typ	
$C_D$ , $C_S$ (ON)	35		pF typ	
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.0001		$\mu\text{A}$ typ	$V_{DD} = 13.2\text{ V}$ Digital Inputs = 0 V or 5 V
	0.03	0.1	$\mu\text{A}$ max	
$I_L$	0.0001		$\mu\text{A}$ typ	$V_L = 5.25\text{ V}$
	0.03	0.1	$\mu\text{A}$ max	
Power Dissipation		1.9	$\mu\text{W}$ max	

NOTES

<sup>1</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

Truth Table (ADG431/ADG432)

ADG431 In	ADG432 In	Switch Condition
0	1	ON
1	0	OFF

Truth Table (ADG433)

Logic	Switch 1, 4	Switch 2, 3
0	OFF	ON
1	ON	OFF

# ADG431/ADG432/ADG433

## ABSOLUTE MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted.)

$V_{DD}$ to $V_{SS}$ .....	44 V
$V_{DD}$ to GND .....	-0.3 V to +25 V
$V_{SS}$ to GND .....	+0.3 V to -25 V
$V_L$ to GND .....	-0.3 V to $V_{DD} + 0.3$ V
Analog, Digital Inputs <sup>2</sup> .....	$V_{SS} - 2$ V to $V_{DD} + 2$ V or 30 mA, Whichever Occurs First
Continuous Current, S or D .....	30 mA
Peak Current, S or D .....	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Operating Temperature Range	
Industrial (B Version) .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	150°C

Plastic Package, Power Dissipation .....	470 mW
$\theta_{JA}$ , Thermal Impedance .....	117°C/W
Lead Temperature, Soldering (10 sec) .....	260°C
SOIC Package, Power Dissipation .....	600 mW
$\theta_{JA}$ , Thermal Impedance .....	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) .....	215°C
Infrared (15 sec) .....	220°C

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

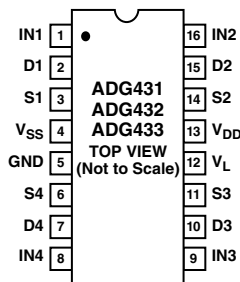
<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG431/ADG432/ADG433 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION (DIP/SOIC)



## ORDERING GUIDE

Model	Temperature Range	Package Option <sup>1</sup>
ADG431BN	-40°C to +85°C	N-16
ADG431BR	-40°C to +85°C	R-16A
ADG431ABR	-40°C to +85°C	R-16A <sup>2</sup>
ADG432BN	-40°C to +85°C	N-16
ADG432BR	-40°C to +85°C	R-16A
ADG432ABR	-40°C to +85°C	R-16A <sup>2</sup>
ADG433BN	-40°C to +85°C	N-16
ADG433BR	-40°C to +85°C	R-16A
ADG433ABR	-40°C to +85°C	R-16A <sup>2</sup>

## NOTES

<sup>1</sup>N = Plastic DIP; R = 0.15" Small Outline IC (SOIC).

<sup>2</sup>Trench isolated, latch-up proof parts. See Trench Isolation section.

## TERMINOLOGY

$V_{DD}$	Most positive power supply potential.	$C_S$ (OFF)	"OFF" switch source capacitance.
$V_{SS}$	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to GND.	$C_D$ (OFF)	"OFF" switch drain capacitance.
$V_L$	Logic power supply (5 V).	$C_D, C_S$ (ON)	"ON" switch capacitance.
GND	Ground (0 V) reference.	$C_{IN}$	Input Capacitance to ground of a digital input.
S	Source terminal. May be an input or output.	$t_{ON}$	Delay between applying the digital control input and the output switching on.
D	Drain terminal. May be an input or output.	$t_{OFF}$	Delay between applying the digital control input and the output switching off.
IN	Logic control input.	$t_D$	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
$R_{ON}$	Ohmic resistance between D and S.	Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
$R_{ON}$ vs. $V_D$ ( $V_S$ )	The variation in $R_{ON}$ due to a change in the analog input voltage with a constant load current.	Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
$R_{ON}$ Drift	Change in $R_{ON}$ vs. temperature.	Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
$R_{ON}$ Match	Difference between the $R_{ON}$ of any two switches.		
$I_S$ (OFF)	Source leakage current with the switch "OFF."		
$I_D$ (OFF)	Drain leakage current with the switch "OFF."		
$I_D, I_S$ (ON)	Channel leakage current with the switch "ON."		
$V_D$ ( $V_S$ )	Analog voltage on terminals D, S.		

# Typical Performance Characteristics—ADG431/ADG432/ADG433



TPC 1. On Resistance as a Function of  $V_D$  ( $V_S$ ) Dual Supplies



TPC 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) Single Supply



TPC 2. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures



TPC 5. Supply Current vs. Input Switching Frequency

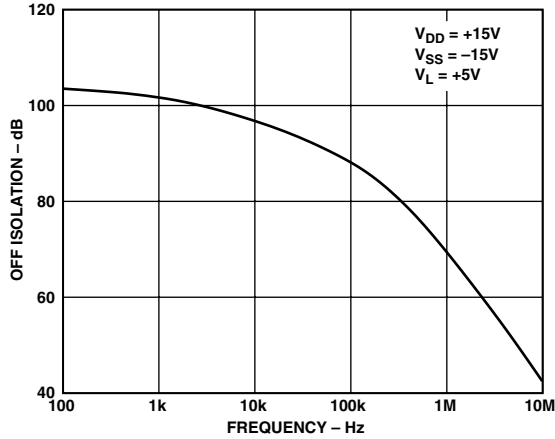


TPC 3. Leakage Currents as a Function of Temperature



TPC 6. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

# ADG431/ADG432/ADG433



TPC 7. Off Isolation vs. Frequency



TPC 8. Crosstalk vs. Frequency

## TRENCH ISOLATION

In the ADG431A, ADG432A and ADG433A, an insulating oxide layer (trench) is placed between the NMOS and PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, the result being a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch up. With trench isolation, this diode is removed, the result being a latch-up proof switch.



Figure 1. Trench Isolation

## APPLICATION

Figure 2 illustrates a precise, fast sample-and-hold circuit. An AD845 is used as the input buffer while the output operational amplifier is an AD711. During the track mode, SW1 is closed and the output  $V_{OUT}$  follows the input signal  $V_{IN}$ . In the hold mode, SW1 is opened and the signal is held by the hold capacitor  $C_H$ .

Due to switch and capacitor leakage, the voltage on the hold capacitor will decrease with time. The ADG431/ADG432/ADG433 minimizes this droop due to its low leakage specifications. The droop rate is further minimized by the use of a polystyrene hold capacitor. The droop rate for the circuit shown is typically  $30 \mu\text{V}/\mu\text{s}$ .

A second switch SW2, which operates in parallel with SW1, is included in this circuit to reduce pedestal error. Since both switches will be at the same potential, they will have a differential effect on the op amp AD711 which will minimize charge injection effects. Pedestal error is also reduced by the compensation network  $R_C$  and  $C_C$ . This compensation network also reduces the hold time glitch while optimizing the acquisition time. Using the illustrated op amps and component values, the pedestal error has a maximum value of 5 mV over the  $\pm 10 \text{ V}$  input range. Both the acquisition and settling times are 850 ns.

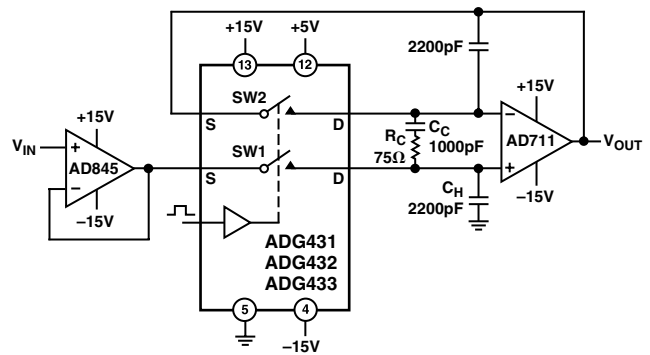
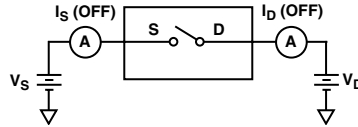


Figure 2. Fast, Accurate Sample-and-Hold

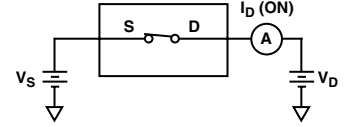
## Test Circuits



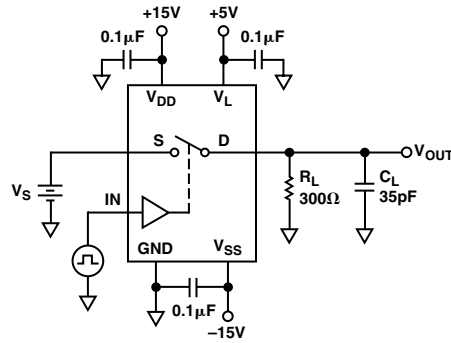
Test Circuit 1. On Resistance



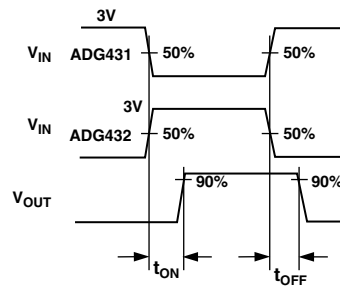
Test Circuit 2. Off Leakage



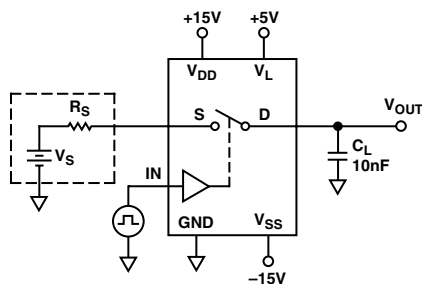
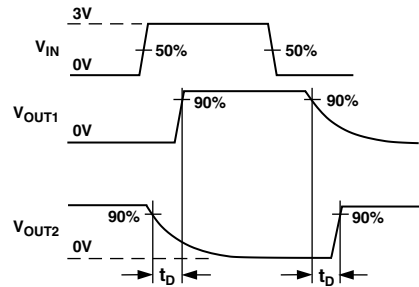
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times



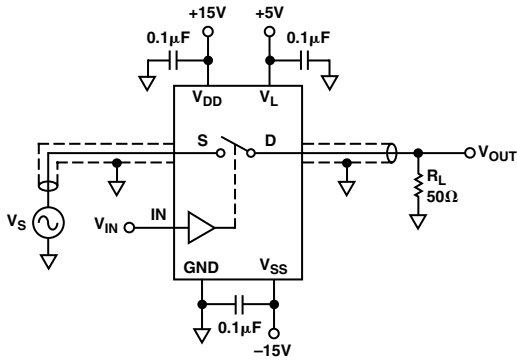
Test Circuit 5. Break-Before-Make Time Delay



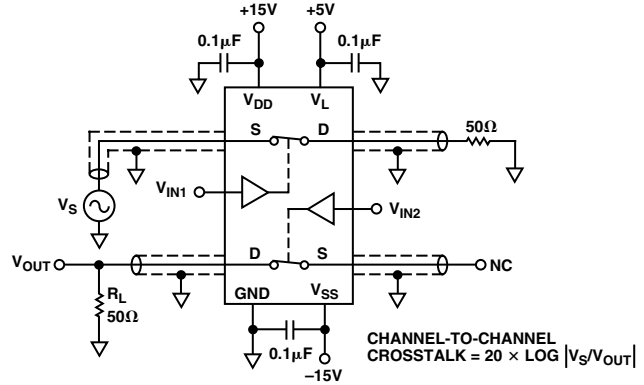
Test Circuit 6. Charge Injection



# ADG431/ADG432/ADG433



Test Circuit 7. Off Isolation



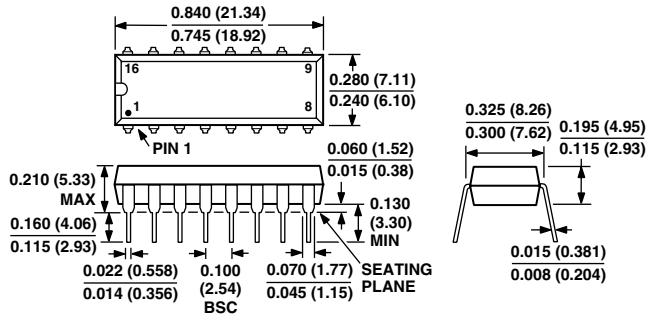
Test Circuit 8. Channel-to-Channel Crosstalk

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

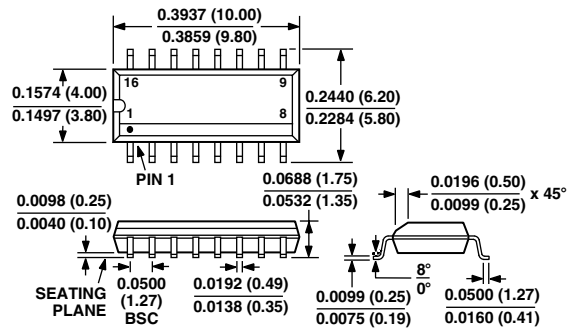
### 16-Lead Plastic DIP (Narrow)

(N-16)



### 16-Lead SOIC

(R-16A)



## ADG431/ADG432/ADG433—Revision History

### Location

Location	Page
Data Sheet changed from REV. B to REV. C.	
Changes to Specifications Table (Dual Supply) . . . . .	2
Changes to Specifications Table (Single Supply) . . . . .	3
Changes to Absolute Maximum Ratings . . . . .	4
Changes to Ordering Guide . . . . .	4
16-Lead Cerdip deleted from Outline Dimensions . . . . .	8



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- Изготовление тестовой платы монтаж и пусконаладочные работы.



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