

AT90-1283

Digital Attenuator
15.5 dB, 5-Bit, TTL Driver, DC-3.5 GHz

Rev. V11

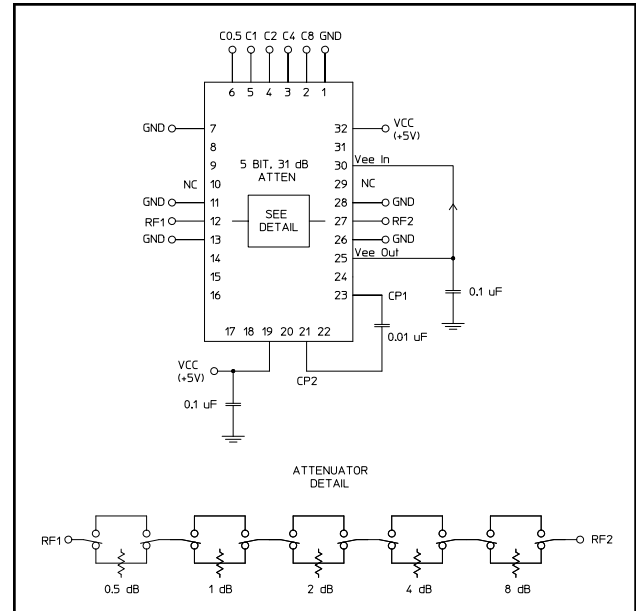
Features

- Attenuation: 0.5 dB Steps to 15.5 dB
- Single Positive Supply
- Contains Internal DC to DC Converter
- Low DC Power Consumption
- Small Footprint, JEDEC Package
- Integral TTL Driver
- 50 ohm Impedance
- CSP-1 Package

Description

M/A-COM's AT90-1283 is a GaAs FET 5-bit digital attenuator with integral TTL driver. Step size is 0.5 dB providing a 15.5 dB total attenuation range. This device is in an PQFN plastic surface mount package. The AT90-1283 is ideally suited for use where accuracy, fast speed, very low power consumption and low costs are required. For dual supply designs without switching noise, use AT90-0283.

Schematic with Off-Chip Components



Pin Configuration³

Pin No.	Function	Pin No.	Function
1	GND	17	NC
2	C8	18	NC
3	C4	19	Vcc
4	C2	20	NC
5	C1	21	Cp
6	C0.5	22	NC
7	GND	23	Cp
8	NC	24	NC
9	NC	25	V _{EE} ²
10	NC ¹	26	GND
11	GND	27	RF2
12	RF1	28	GND
13	GND	29	NC ¹
14	NC	30	V _{EE} ²
15	NC	31	NC
16	NC	32	Vcc

1. Pins 10 and 29 must be isolated.
2. V_{EE} is produced internally and requires a .1 μ F cap to GND. Generated noise is typical of switching DC-DC Converters.
3. The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages)

Ordering Information

Part Number	Package
AT90-1283	Bulk Packaging
AT90-1283TR	1000 piece reel
AT90-1283-TB	Sample Test Board

Note: Reference Application Note M513 for reel size information.

ADVANCED: Data Sheets contain information regarding a product M/A-COM Technology Solutions is considering for development. Performance is based on target specifications, simulated results, and/or prototype measurements. Commitment to develop is not guaranteed.
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Electrical Specifications: $T_A = +25^\circ\text{C}$

Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss	—	DC - 3.5 GHz	dB	—	2.8	3.2
Attenuation Accuracy	Individual Bits 0.5-1-4-8 dB Individual Bit 2 dB Any Combination of Bits 1 to 15.5 dB	DC - 3.5 GHz DC - 3.5 GHz DC - 3.5 GHz	dB dB dB	— — —	— — —	$\pm(3 + 5\%$ of atten setting) $\pm(4 + 10\%$ of atten setting) $\pm(5 + 7\%$ of atten setting)
VSWR	Full Range	DC - 3.5 GHz	Ratio	—	1.6:1	1.8:1
Switching Speed	50% Cntl to 90%/10% RF 10% to 90% or 90% to 10%	— —	ns ns	— —	75 20	150 50
1 dB Compression	— —	50 MHz 0.5 - 3.5 GHz	dBm dBm	— —	+21 +29	— —
Input IP_3	Two-tone inputs up to +5 dBm	50 MHz 0.5-3.5 GHz	dB dB	— —	+35 +48	— —
V_{CC}	—	—	V	4.75	5.0	5.25
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	— —	V V	0.0 2.0	— —	0.8 5.0
I_{in} (Input Leakage Current)	$V_{in} = V_{CC}$ or GND	—	μA	-1.0	—	1.0
I_{CC}^4	V_{CC} min to max, Logic "0" or "1"	—	mA	—	6	10
Turn-on Current ⁵	For guaranteed start-up	—	mA	—	—	125
ΔI_{CC} (Additional Supply Current Per TTL Input Pin)	$V_{CC} = \text{Max}$, $V_{cntrl} = V_{CC} - 2.1 \text{ V}$	—	mA	—	—	1.0
Switching Noise	Generated from DC-DC Converter with recommended capacitors	3.5 MHz	dBm	—	-93	—
Thermal Resistance θ_{jc}	—	—	$^\circ\text{C/W}$	—	15	—

- During turn-on, the device requires an initial start up current (I_{CC}) specified as "Turn-on Current". Once operational, I_{CC} will drop to the specified levels.
- The DC-DC converter is guaranteed to start in 100 μs as long as the power supplies have the maximum turn-on current available for start-up.

Absolute Maximum Ratings ^{6,7}

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 3.5 GHz	+27 dBm +34 dBm
V_{CC}	$-0.5\text{V} \leq V_{CC} \leq +6.0\text{V}$
V_{in}^8	$-0.5\text{V} \leq V_{in} \leq V_{CC} + 0.5\text{V}$
Operating Temperature	-40°C to $+85^\circ\text{C}$
Storage Temperature	-65°C to $+125^\circ\text{C}$

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Handling Procedures

Please observe the following precautions to avoid damage:

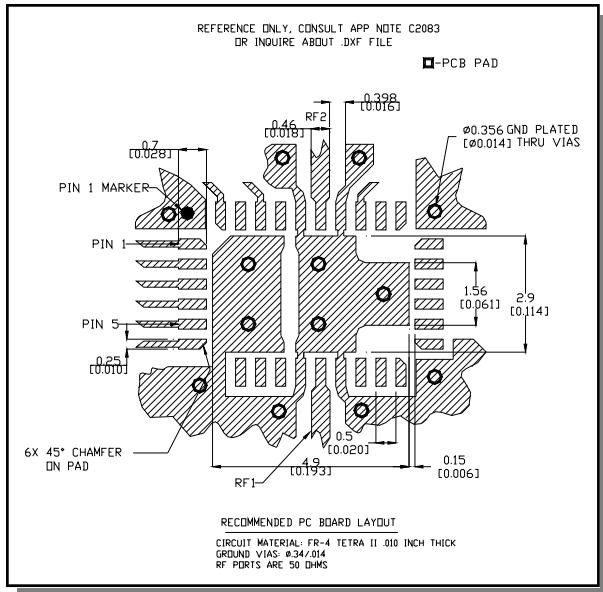
Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

Moisture Sensitivity

The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

Recommended PCB Configuration⁹



9. Application Note C2083 is available on line at www.macom.com

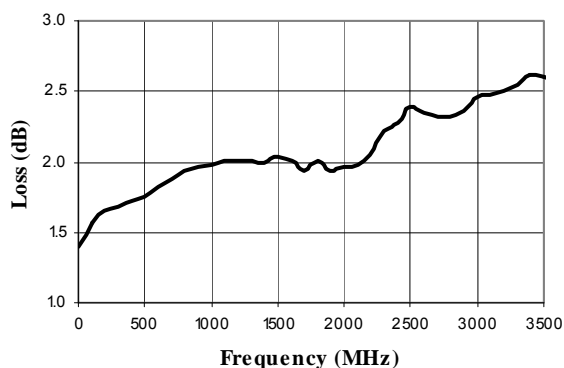
Truth Table (Digital Attenuator)

C8	C4	C2	C1	C0.5	Attenuation
0	0	0	0	0	Loss, Reference
0	0	0	0	1	0.5 dB
0	0	0	1	0	1.0 dB
0	0	1	0	0	2.0 dB
0	1	0	0	0	4.0 dB
1	0	0	0	0	8.0 dB
1	1	1	1	1	15.5 dB

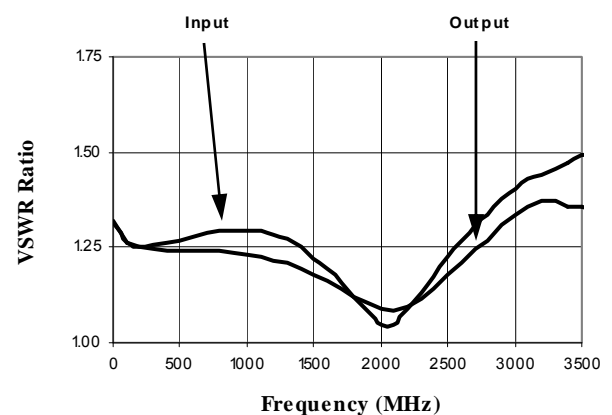
0 = TTL Low; 1 = TTL High

Typical Performance Curves

Insertion Loss

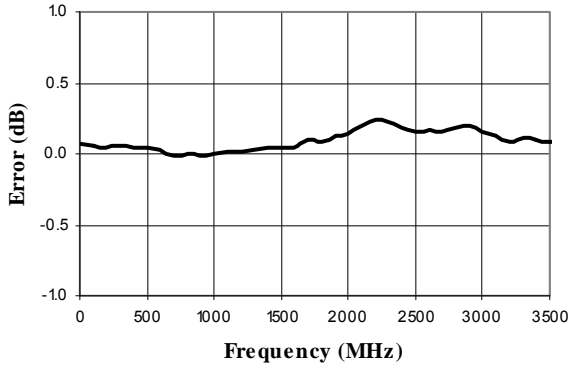


VSWR @ Insertion Loss

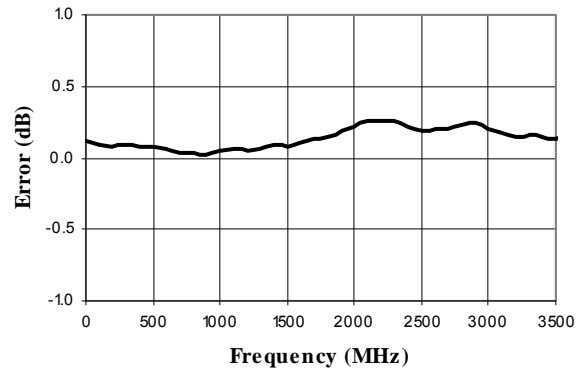


Typical Performance Curves

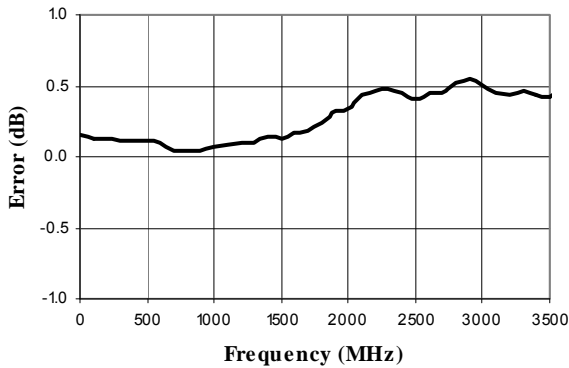
Attenuation Error, 0.5 dB Bit



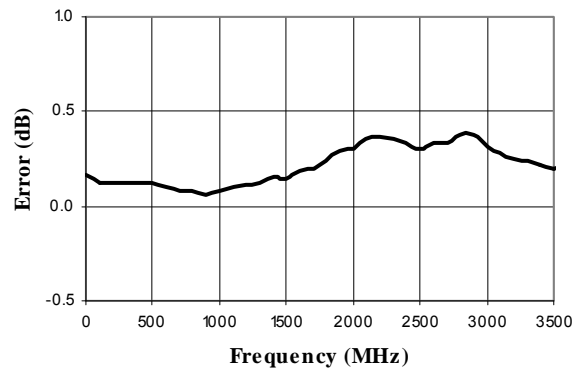
Attenuation Error, 1 dB Bit



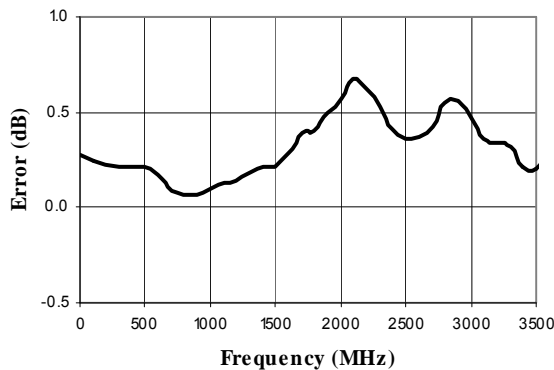
Attenuation Error, 2 dB Bit



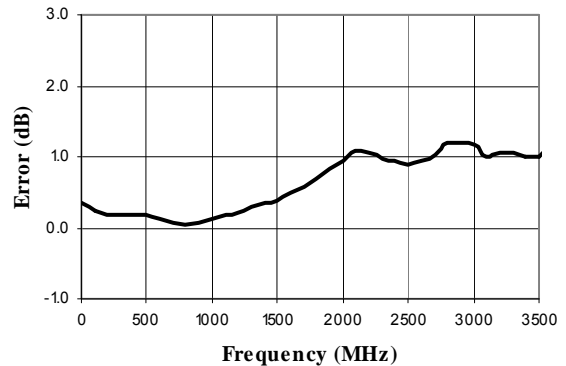
Attenuation Error, 4 dB Bit



Attenuation Error, 8 dB Bit

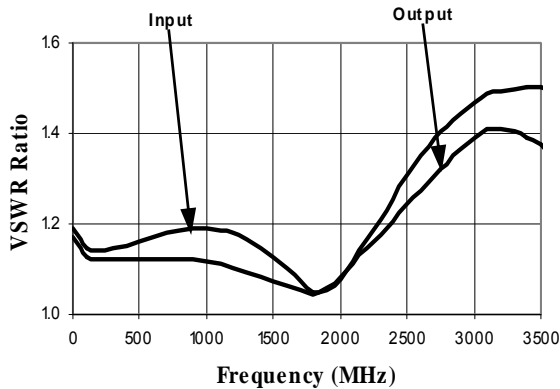


Attenuation Error, Max. Attenuation

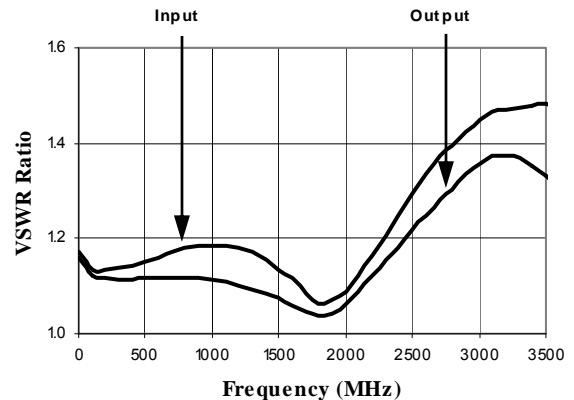


Typical Performance Curves

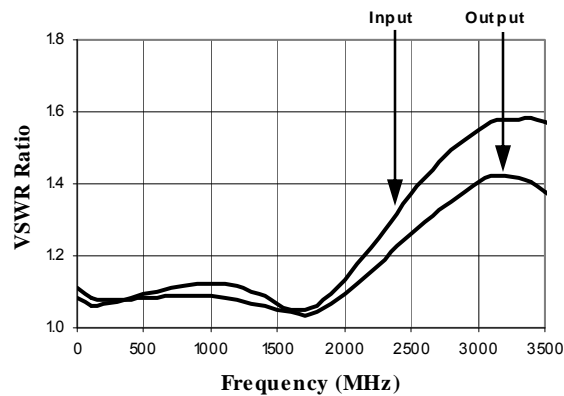
VSWR, 0.5 dB Bit



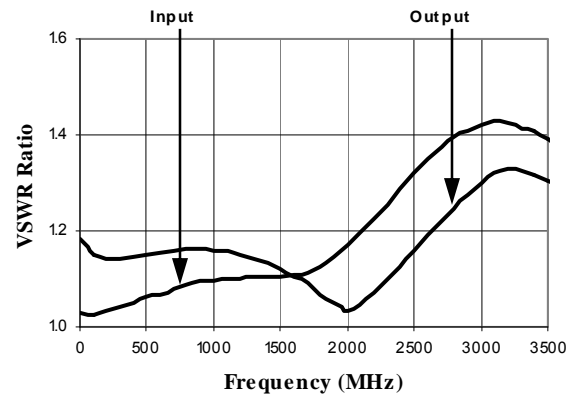
VSWR, 1 dB Bit



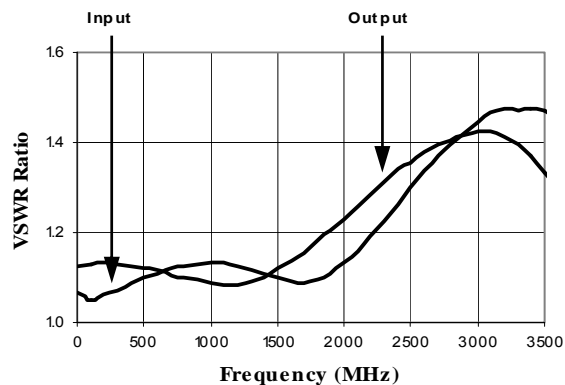
VSWR, 2 dB Bit



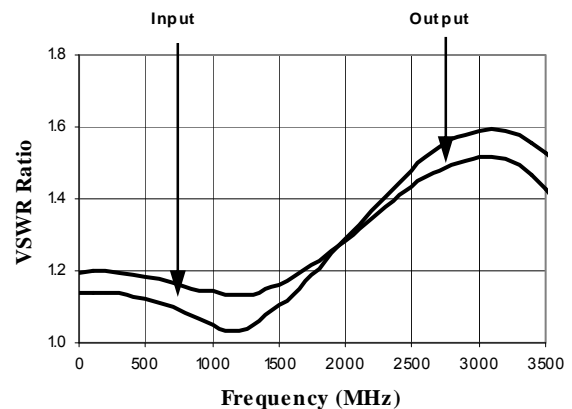
VSWR, 4 dB Bit



VSWR, 8 dB Bit



VSWR, Maximum Attenuation

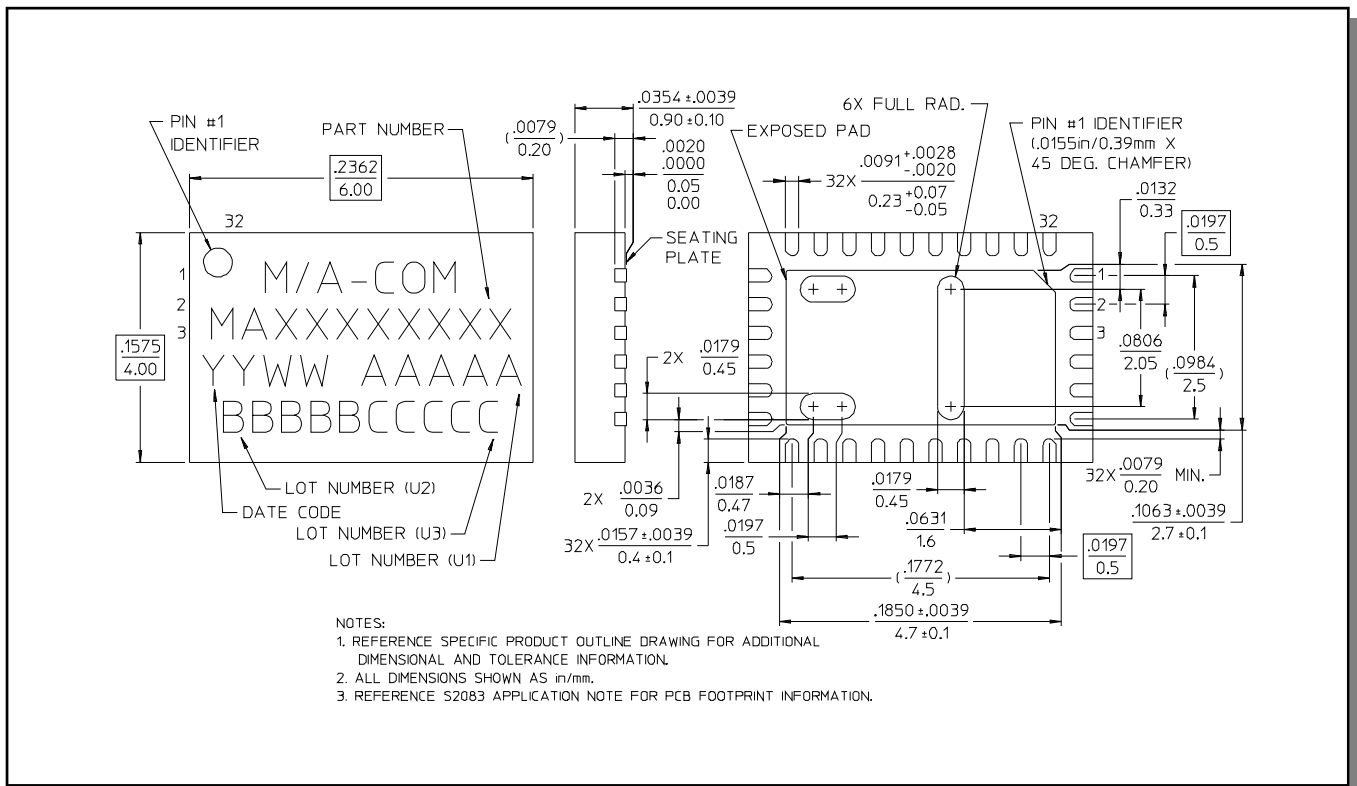


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CSP-1, 4 x 6 mm, 32-lead PQFN†



† Reference Application Note M538 for lead-free solder reflow recommendations.

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Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru