NCN5192

HART Modem

Description

The NCN5192 is a single−chip, CMOS modem for use in highway addressable remote transducer (HART) field instruments and masters. The modem and a few external passive components provide all of the functions needed to satisfy HART physical layer requirements including modulation, demodulation, receive filtering, carrier detect, and transmit−signal shaping. In addition, the NCN5192 also has an integrated DAC for low-BOM current loop slave transmitter implementation.

The NCN5192 uses phase continuous frequency shift keying (FSK) at 1200 bits per second. To conserve power the receive circuits are disabled during transmit operations and vice versa. This provides the half−duplex operation used in HART communications.

Features

- Single−chip, Half−duplex 1200 Bits per Second FSK Modem
- Bell 202 Shift Frequencies of 1200 Hz and 2200 Hz
- 3.0 V – 5.5 V Power Supply
- Transmit−signal Wave Shaping
- Receive Band−pass Filter
- Low Power: Optimal for Intrinsically Safe Applications
- Compatible with 3.3 V or 5 V Microcontroller
- Internal Oscillator Requires 460.8 kHz, 920 kHz or 1.8 MHz Crystal or Ceramic Resonator
- SPI Communication
- Integrated 16 bit Sigma-Delta DAC
- Meets HART Physical Layer Requirements
- Industrial Temperature Range of −40°C to +85°C
- Available in 32−pin NQFP Package
- These are Pb−Free Devices

Applications

- HART Multiplexers
- HART Modem Interfaces
- 4 – 20 mA Loop Powered Transmitters

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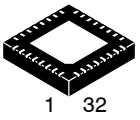
MARKING DIAGRAM



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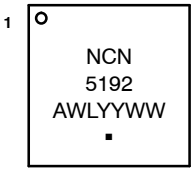


NCN5192 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

BLOCK DIAGRAM

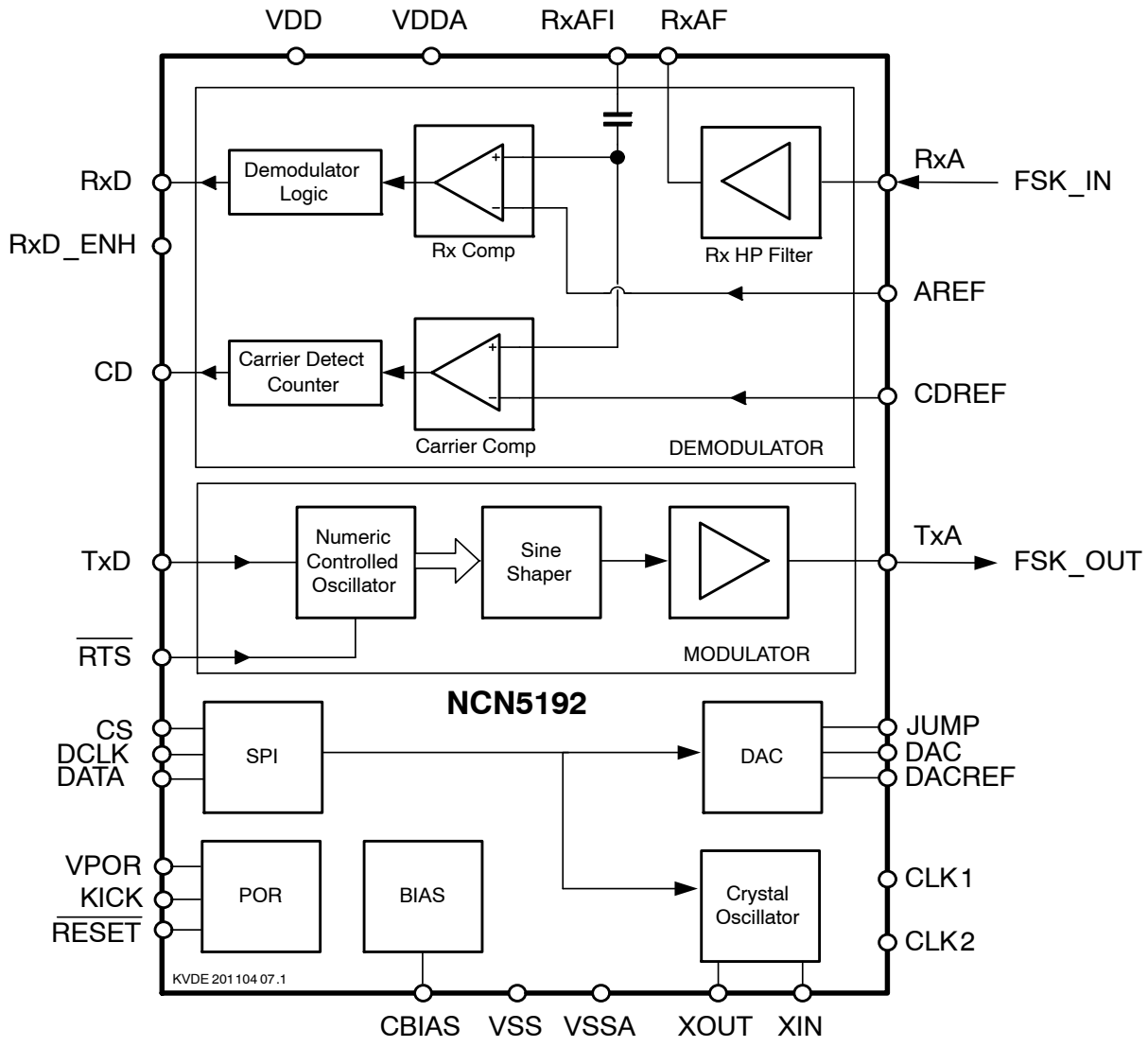


Figure 1. Block Diagram NCN5192

ELECTRICAL SPECIFICATIONS

Table 1. ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature	−40	+85	°C
T_S	Storage Temperature	−55	+150	°C
V_{DD}	Supply Voltage	−0.3	6.0	V
V_{IN}, V_{OUT}	DC Input, Output	−0.3	V_{DD} + 0.3	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. CMOS devices are damaged by high−energy electrostatic discharge. Devices must be stored in conductive foam or with all pins shunted. Precautions should be taken to avoid application of voltages higher than the maximum rating. Stresses above absolute maximum ratings may result in damage to the device.
2. Remove power before insertion or removal of this device.

Table 2. DC CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C)

Symbol	Parameter	V_{DD}	Min	Typ	Max	Units
V_{DD}	DC Supply Voltage		3.0		5.5	V
V_{IL}	Input Voltage, Low	3.0 – 5.5 V			0.3 * V_{DD}	V
V_{IH}	Input Voltage, High	3.0 – 5.5 V	0.7 * V_{DD}			V
V_{OL}	Output Voltage, Low (I_{OL} = 0.67 mA)	3.0 – 5.5 V			0.4	V
V_{OH}	Output Voltage, High (I_{OH} = −0.67 mA)	3.0 – 5.5 V	2.4			V
C_{IN}	Input Capacitance of: Analog Inputs RxA Digital Inputs			 2.9 25 3.5		 pF pF pF
I_{IL}/I_{IH}	Input Leakage Current				±500	nA
I_{OLL}	Output Leakage Current				±10	μA
I_{DD}	Total Power Supply Current		175	350	600	μA
I_{DDA}	Static Analog Supply Current	3.3 V 5.0 V	150 150		330 370	μA μA
I_{DDQ}	Static Digital Current		0		30	μA
I_{DDD}	Dynamic Digital Current	5.0 V	25		200	μA
A_{REF}	Analog Reference	3.3 V 5.0 V	1.2	1.235 2.5	2.6	V V
CD_{REF} (Note 3)	Carrier Detect Reference (IAREF – 0.08 V)	3.3 V 5.0 V		1.15 2.42		V
C_{BIAS}	Comparator Bias Current (RBIAS = 500 kΩ, IAREF = 1.235 V)			2.5		μA

3. The HART specification requires carrier detect (CD) to be active between 80 and 120 mVp−p. Setting CDREF at AREF − 0.08 VDC will set the carrier detect to a nominal 100 mVp−p.

Table 3. AC CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C) (Note 4)

Pin Name	Description	Min	Typ	Max	Units
RxA	Receive analog input Leakage current Frequency – mark (logic 1) Frequency – space (logic 0)	 1190 2180	 1200 2200	 ±150 1210 2220	 nA Hz Hz
RxAF	Output of the high−pass filter Slew rate Gain bandwidth (GBW) Voltage range	 150 0.15	 0.025 	 V_{DD} – 0.15	 V/ms kHz V/ms
RxAFI	Carrier detect and receive filter input Leakage current			 ±500	 nA
TxA	Modulator output Frequency – mark (logic 1) Frequency – space (logic 0) Amplitude (IAREF 1.235 V) Slew Rate – mark (logic 1) Slew Rate – space (logic 0) Loading (IAREF = 1.235 V)	 30	 1196.9 2194.3 500 1860 3300 	 	 Hz Hz mV V/s V/s kΩ
RxD	Receive digital output Rise/fall time	 20			ns
CD	Carrier detect output Rise/fall time	 20			ns

4. The modulator output frequencies are proportional to the input clock frequency (460.8 kHz/920 kHz/1.8 MHz).

Table 4. MODEM CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C)

Parameter	Min	Typ	Max	Units
Demodulator jitter Conditions 1. Input frequencies at 1200 Hz ± 10 Hz, 2200 Hz ± 20 Hz 2. Clock frequency of 460.8 kHz ± 0.1% 3. Input (RxA) asymmetry, 0			12	% of 1 bit

Table 5. CERAMIC RESONATOR AND CRYSTAL – External Clock Specifications
(V_{DD} = 3.0 V to 5.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C)

Parameter	Min	Typ	Max	Units
Resonator Tolerance Frequency		 460.8	 1.0	 % kHz
Crystal or Resonator, 920 kHz Tolerance Frequency		 921.6	 1.0	 % kHz
Crystal, 1.8 MHz Tolerance Frequency		 1.843	 1.0	 % MHz
External Duty cycle Amplitude	 40	 50 $V_{OH} - V_{OL}$	 60	 % V

Table 6. DAC CHARACTERISTICS (V_{DD} = 3.0 V to 5.5 V, V_{SS} = 0 V, T_A = −40°C to +85°C)

Parameter	Min	Typ	Max	Units
Bandwidth		10		Hz
Accuracy Return−to−Zero Non Return−to−Zero		 16 14		 Bit Bit
Maximum Output Return−to−Zero Non Return−to−Zero		 AVDD/2 AVDD		 V V
Differential Non−linearity Return−to−Zero Non Return−to−Zero		 0.5 0.25	 0.75 0.75	 LSB LSB
Integral Non−linearity Return−to−Zero Non Return−to−Zero		 2.0 1.0	 4.0 2.0	 LSB LSB

TYPICAL APPLICATION

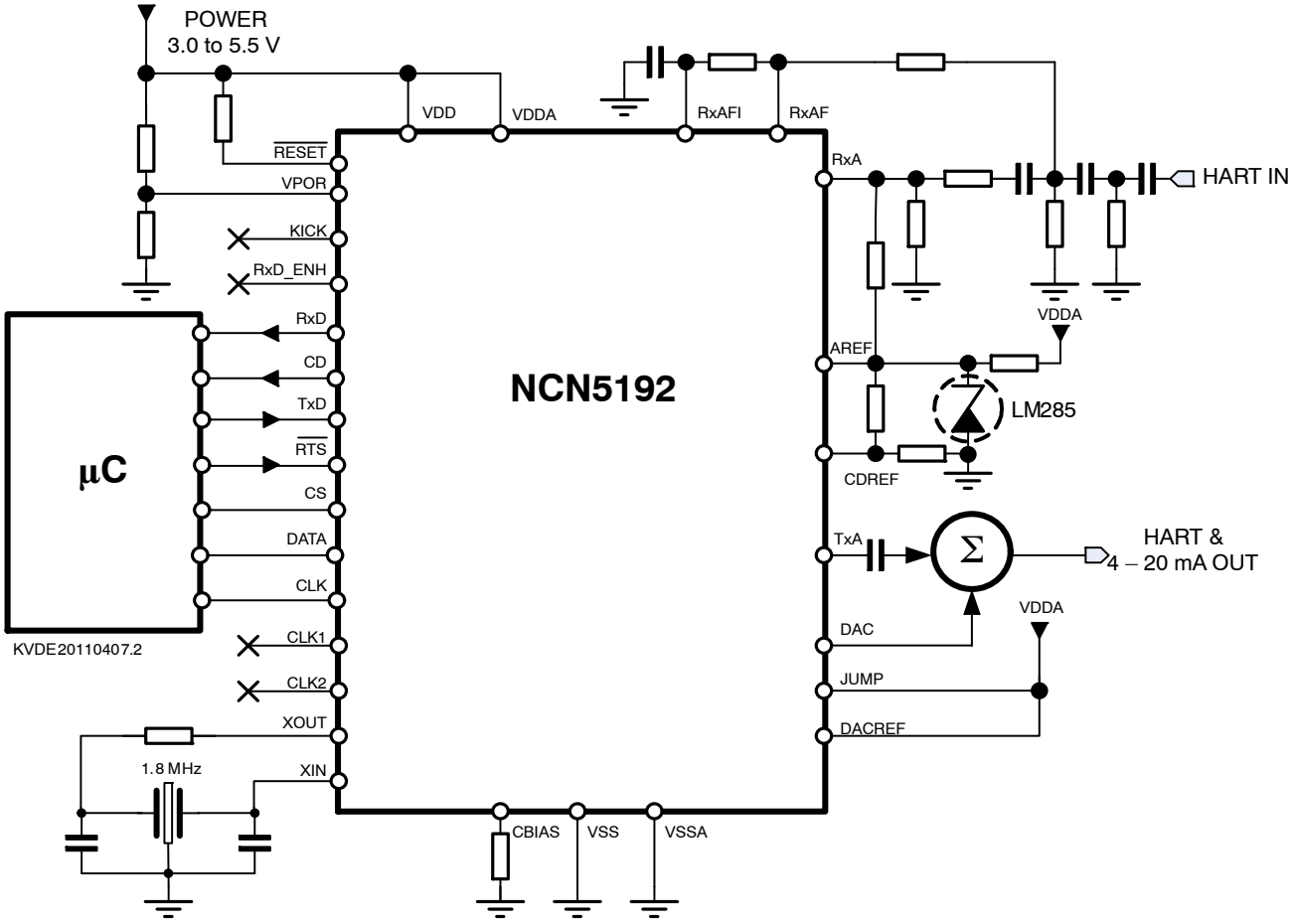


Figure 2. Application Diagram NCN5192

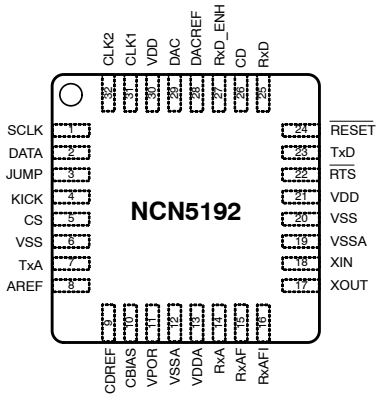


Figure 3. Pin Out NCN5192 in 32-pin NQFP (top view)

Table 7. PIN OUT SUMMARY 32−PIN NQFP

Pin No.	Signal Name	Type	Pin Description
1	SCLK	Input	SPI Serial Clock
2	DATA	Input	SPI Serial Data
3	JUMP	Input	Sigma−Delta Modulator Alarm condition value
4	KICK	Input	Watchdog kick
5	CS	Input	SPI Serial Chip Select
6	VSS	Ground	Ground
7	TxA	Output	Transmit Data Modulator output
8	AREF	Input	Analog reference voltage
9	CDREF	Input	Carrier detect reference voltage
10	CBIAS	Output	Comparator bias current
11	VPOR	Input	POR measurement point
12	VSSA	Ground	Analog ground
13	VDDA	Power	Analog supply voltage
14	RxA	Input	Receive Data Modulator input
15	RxAF	Output	Analog receive filter input
16	RxAFI	Input	Analog receive comparator input
17	XOUT	Output	Crystal oscillator output
18	XIN	Input	Crystal oscillator input
19	VSSA	Ground	Analog ground
20	VSS	Ground	Ground
21	VDD	Power	Digital supply voltage
22	RTSB	Input	Request to send
23	TxD	Input	Input transmit data, transmit HART data stream from microcontroller
24	RESETB	Open Drain	Reset all digital logic when low
25	RxD	Output	Received demodulated HART data to microcontroller
26	CD	Output	Carrier detect output
27	RxD_ENH	Output	not[CD] or RxD
28	DACREF	Input	Sigma−Delta Modulator Reference Voltage
29	DAC	Output	Sigma−Delta Modulator Output
30	VDD	Power	Digital supply voltage
31	CLK1	Output	Programmable Clock Output 1
32	CLK2	Output	Programmable Clock Output 2

Pin Descriptions

Table 8. PIN DESCRIPTIONS

Symbol	Pin Name	Description
AREF	Analog reference voltage	Receiver Reference Voltage. Normally 1.23 V is selected (in combination with VDDA = 3.3 V). See Table 2.
CDREF	Carrier detect reference voltage	Carrier Detect Reference voltage. The value should be 85 mV below AREF to set the carrier detection to a nominal of 100 mV_{p-p}.
RESETB	Reset digital logic	When at logic low (V_{SS}) this input holds all the digital logic in reset. During normal operation RESETB should be at V_{DD}. RESETB should be held low for a minimum of 10 nS after V_{DD} = 2.5 V as shown in Figure NO TAG.
RTSB	Request to send	Active−low input selects the operation of the modulator. TxA is enabled when this signal is low. This signal must be held high during power−up.
RxA	Analog receive input	Receive Data Demodulator Input. Accepts a HART 1200 / 2200 Hz FSK modulated square wave serial data stream as input.
RxAFI	Analog receive comparator input	Positive input of the carrier detect comparator and the receiver filter comparator.
TxD	Digital transmit input	Input to the modulator accepts digital data in NRZ form. When TxD is low, the modulator output frequency is 2200 Hz. When TxD is high, the modulator output frequency is 1200 Hz.
XIN	Oscillator input	Input to the internal oscillator must be connected to a parallel mode ceramic resonator when using the internal oscillator or grounded when using an external clock signal.
XOUT	Oscillator output	Output from the internal oscillator must be connected to an external clock signal or to a parallel mode ceramic resonator when using the internal oscillator.
CLK1	Programmable Clock Output	Output signal derived from oscillator output, frequency division set by internal register.
CLK2	Programmable Clock Output	Output signal derived from oscillator output, frequency division set by internal register. As this signal is also used internally, the division should be set so that the output frequency is 460.8 kHz
CBIAS	Comparator bias current	Connection to the external bias resistor. R_{BIAS} should be selected such that AREF / R_{BIAS} = 2.5 μA ± 5 %
CD	Carrier detect output	Output goes high when a valid input is recognized on RxA. If the received signal is greater than the threshold specified on CDREF for four cycles of the RxA signal, the valid input is recognized.
RxAF	Analog receive filter output	The output of the three pole high pass receive data filter
RxD	Digital receive output	Signal outputs the digital receive data. When the received signal (RxA) is 1200 Hz, RxD outputs logic high. When the received signal (RxA) is 2200 Hz, RxD outputs logic low. The HART receive data stream is only active if Carrier Detect (CD) is high.
RxD_ENH	Digital receive output, alternative	Not(OCD) or RXD
TxA	Analog transmit output	Transmit Data Modulator Output. A trapezoidal shaped waveform with a frequency of 1200 Hz or 2200 Hz corresponding to a data value of 1 or 0 respectively applied to TxD. TxA is active when RTSB is low. TxA equals 0.5 V when RTSB is high.
SCLK	SPI bus clock line	Serial communication clock line
DATA	SPI bus data line	Serial communication data line. Frames transmitted can either be 8 bit or 16 bit long.
CS	SPI bus chip select	Serial communication chip select line. Pulled high by microcontroller while a frame is transmitted.
JUMP	DAC Alarm value	When a problem is detected, such as a clock failure or the watchdog going off, the DAC will jump to the value set on this pin.
DACREF	DAC Reference	This is the high value of the output and can be connected to any voltage between AREF and VDD.
DAC	DAC Output	Output of a 16 bit Sigma−Delta Modulator
KICK	Watchdog Kick	Periodically a pulse should be provided to reset the watchdog. This can be configured in internal registers for an internal 1.8kHz signal, or to an external signal provided to this pin.
VPOR	POR Input	Input to the POR comparator. The voltage on this pin is compared with AREF. An external resistor divider should divide the supply voltage to this pin.
VDD	Digital power	Power for the digital modem circuitry
VDDA	Analog supply voltage	Power for the analog modem circuitry
VSS	Ground	Digital ground (and Analog ground in the case of PLCC package)
VSSA	Analog ground	Analog ground

Functional Description

The NCN5192 is a single-chip modem for use in Highway Addressable Remote Transducer (HART) field instruments and masters. The modem IC contains a transmit data modulator with signal shaper, carrier detect circuitry, an analog receiver, demodulator circuitry and an oscillator, as shown in the block diagram in Figure 1.

The modulator accepts digital data at its digital input TxD and generates a trapezoidal shaped FSK modulated signal at the analog output TxA. A digital “1” or mark is represented with a frequency of 1200 Hz. A digital “0” or space is represented with a frequency of 2200 Hz. The used bit rate is 1200 baud.

The demodulator receives the FSK signal at its analog input, filters it with a band-pass filter and generates 2 digital signals: RxD: Received Data and CD: Carrier Detect. At the digital output RxD the original modulated signal is received. CD outputs the Carrier Detect signal. It goes logic high if the received signal is above 100 mVpp during 4 consecutive carrier periods.

The oscillator provides the modem with a stable time base using either a simple external resonator or an external clock source.

Detailed Description

Modulator

The modulator accepts digital data in NRZ form at the TxD input and generates the FSK modulated signal at the TxA output.

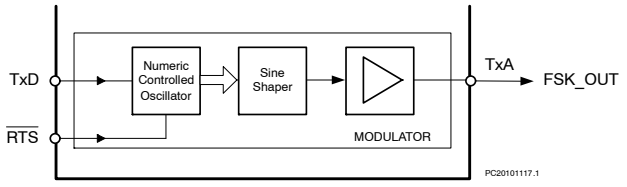


Figure 4. Modulator Block Diagram

A logic “1” or mark is represented by a frequency f_m = 1200 Hz. A logic “0”or space is represented by a frequency f_s = 2200 Hz.

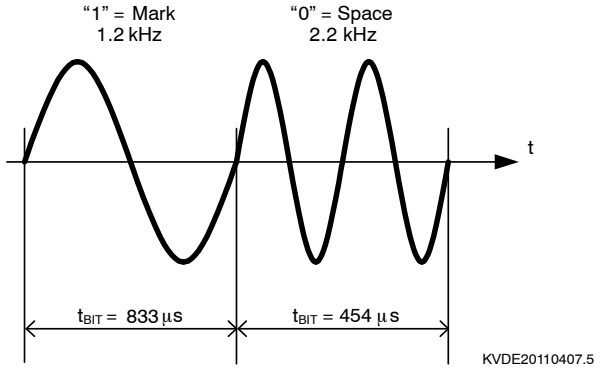


Figure 5. Modulation Timing

The Numeric Controlled Oscillator (NCO) works in a phase continuous mode preventing abrupt phase shifts when switching between mark and space frequency. The control signal “Request To Send” (RTSB) enables the NCO. When RTSB is logic low the modulator is active and NCN5192 is in transmit mode. When RTSB is logic high the modulator is disabled and NCN5192 is in receive mode.

The digital outputs of the NCO are shaped in the Wave Shaper block to a trapezoidal signal. This circuit controls the rising and falling edge to be inside the standard HART waveshape limits. Figure 6 shows the transmit-signal forms captured at TxA for mark and space frequency. The slew rates are SR_m = 1860 V/s at the mark frequency and SR_s = 3300 V/s at the space frequency. For AREF = 1.235 V, TxA will have a voltage swing from approximately 0.25 to 0.75 V_{DC}.

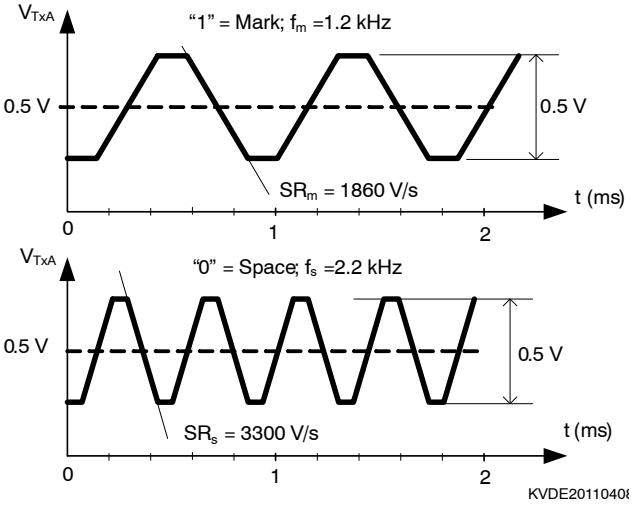


Figure 6. Modulator shaped output signal for Mark and Space frequency at TxA pin.

Demodulator

The demodulator accepts a FSK signal at the RxA input and reconstructs the original modulated signal at the RxD output. Figure 7 illustrates the demodulation process.

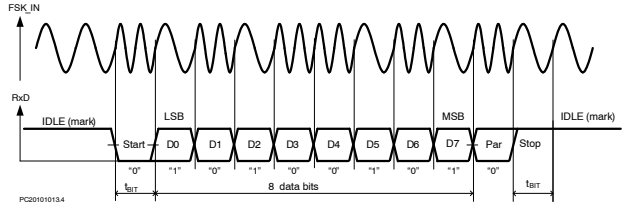


Figure 7. Modulation Timing

This HART bit stream follows a standard 11-bit UART frame with Start, Stop, 8 Data – and 1 Parity bit. The communication speed is 1200 baud.

Receive Filter and Comparator

The received FSK signal first is filtered using a band-pass filter build around the low noise receiver operational amplifier “Rx HP filter”. This filter blocks interferences outside the HART signal band.

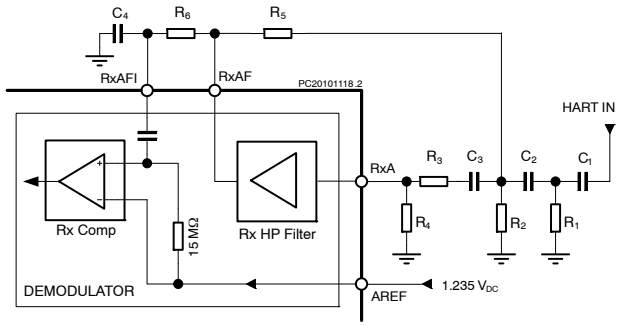


Figure 8. Demodulator Receive Filter and Signal Comparator

The filter output is fed into the Rx comparator. The threshold value equals the analog ground making the comparator to toggle on every zero crossing of the filtered FSK signal. The maximum demodulator jitter is 12 % of one bit given the input frequencies are within the HART specifications, a clock frequency of 460.8 kHz (±1.0 %) and zero input (RxA) asymmetry.

Carrier Detect Circuitry

Low HART input signal levels increases the risk for the generation of bit errors. Therefore the minimum signal amplitude is set to 80−120 mVpp. If the received signal is below this level the demodulator is disabled.

This level detection is done in the Carrier Detector. The output of the demodulator is qualified with the carrier detect signal (CD), therefore, only RxA signals large enough to be detected (100 mV_{p-p} typically) by the carrier detect circuit produce received serial data at RxD.

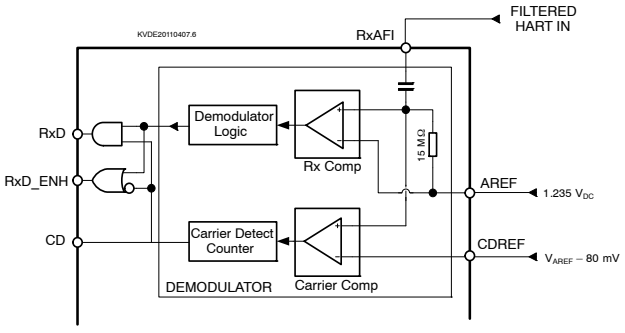


Figure 9. Demodulator Carrier and Signal Comparator

The carrier detect comparator shown in Figure 9 generates logic low output if the RxAFI voltage is below CDREF. The comparator output is fed into a carrier detect block. The carrier detect block drives the carrier detect output pin CD high if RTSB is high and four consecutive pulses out of the comparator have arrived. CD stays high as long as RTSB is high and the next comparator pulse is received in less than 2.5 ms. Once CD goes inactive, it takes four consecutive pulses out of the comparator to assert CD again. Four consecutive pulses amount to 3.33 ms when the received signal is 1200 Hz and to 1.82 ms when the received signal is 2200 HZ. The difference between RxD and RxD_ENH is evident when CD is low: RxD is then also low, while RxD_ENH is then high. When CD is high, RxD and RxD_ENH have the same output.

Miscellaneous Analog Circuitry

Voltage References

The NCN5192 requires two voltage references, AREF and CDREF. AREF sets the DC operating point of the internal operational amplifiers and is the reference for the Rx comparator. If NCN5192 operates at V_{DD} = 3.3 V the ON Semiconductor LM285D 1.235 V reference is recommended.

The level at which CD (Carrier Detect) becomes active is determined by the DC voltage difference (CDREF - AREF). Selecting a voltage difference of 80 mV will set the carrier detect to a nominal 100 mV_{p-p}.

Bias Current Resistor

The NCN5192 requires a bias current resistor R_{BIAS} to be connected between CBIAS and V_{SS}. The bias current controls the operating parameters of the internal operational amplifiers and comparators and should be set to 2.5 μA.

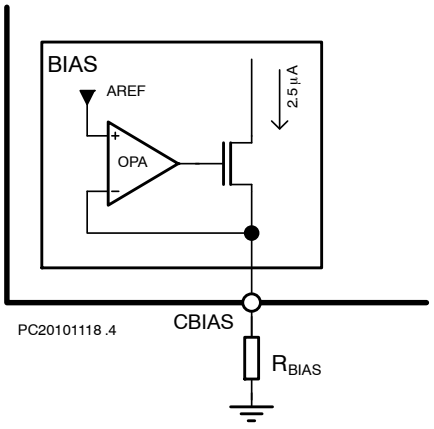


Figure 10. Bias Circuit

The value of the bias current resistor is determined by the reference voltage AREF and the following formula:

$$R_{BIAS} = \frac{AREF}{2.5\ \mu A}$$

The recommended bias current resistor is 500 KΩ when AREF is equal to 1.235 V.

Oscillator

The clock signal used by NCN5192 can either be 460.8 kHz, 921.6 kHz or 1.8432 MHz. This can be provided by an external clock or a resonator or crystal connected to the internal oscillator.

Internal Oscillator Option

The oscillator cell will function with a 460.8 kHz, 921.6 kHz or 1.8432 MHz crystal or ceramic resonator. A parallel resonant ceramic resonator can be connected between XIN and XOUT. Figure 11 illustrates the crystal option for clock generation using a 460.8 kHz (±1% tolerance) parallel resonant crystal and two tuning capacitors C_X. The actual values of the capacitors may depend on the recommendations of the manufacturer of the resonator. Typically, capacitors in the range of 100 pF to 470 pF are used. Additionally, a resistor may be required between XOUT and the crystal terminal, depending on manufacturer recommendation.

The NCN5192 IC uses CLK2 as clock signal for the wave shaping and digital logic. This signal must be set 460.8 kHz by activating the proper frequency division in the internal register (bit 1 and 2). The CLK1 frequency division (bit 3 and 4) can be freely chosen. This programmable clock signal can be used to drive other ICs such as a microcontroller and is not used internally in the NCN5192.

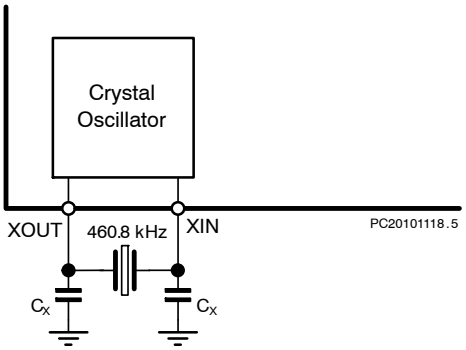


Figure 11. Crystal Oscillator

External Clock Option

It may be desirable to use an external clock as shown in Figure 12 rather than the internal oscillator. In addition, the NCN5192 consumes less current when an external clock is used. Minimum current consumption occurs with the clock connected to XOUT and XIN connected to V_{SS}.

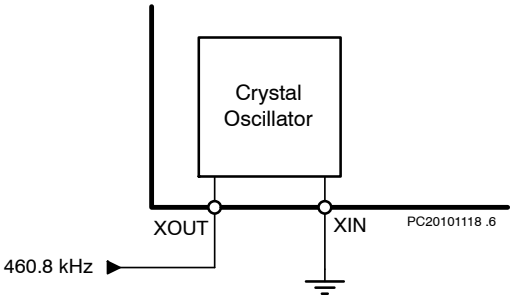


Figure 12. Oscillator with External Clock

Reset

The NCN5192 modem includes a Power on Reset block. An external resistor division of the supply voltage is required, and should be tied to pin VPOR. This pin is attached to an internal comparator, and is compared to the AREF voltage. When this comparator trips, the RESETB pin will be pulled low and the IC will reset. After VPOR returns to a valid level, the RESETB pin will be held low for at least an additional 35 ms (may be longer depending on clock frequency). The RESETB pin will also be pulled low when a microcontroller failure is detected. A watchdog will guard microcontroller communication by looking at the KICK pin. When the microcontroller fails to provide a periodical pulse on this pin, the watchdog will pull down the RESETB pin for 140 μs. A rising edge should be provided to the IC at least every 53 ms. A 1.8 kHz kick can also be provided internally if bit 5 of the internal register is set. If the watchdog kick is provided internally, the KICK pin should be tied to Vss.

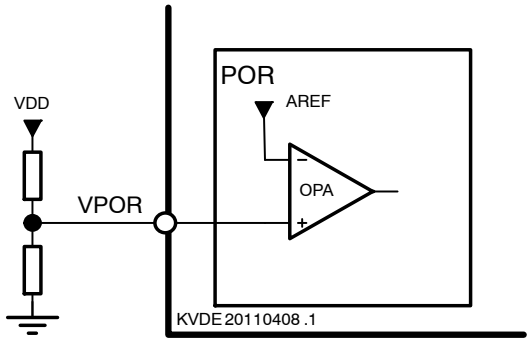


Figure 13. Power on Reset Block

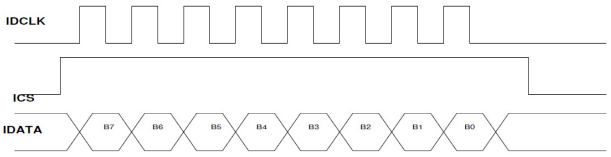


Figure 14. 8 Bit SPI Frame

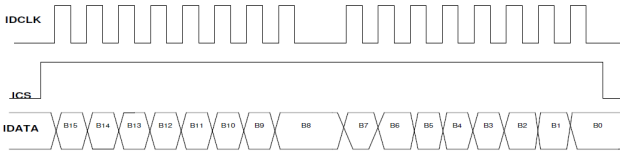


Figure 15. 16 Bit SPI Frame

SPI Communication

The SPI bus on the NCN5192 is made up of three signals; DATA, SCLK, and CS. The data is either 8 bits or 16 bits. In the case of 8 bits CS will go high for eight clock cycles of SCLK and in the case of 16 bits CS will be high for 16 clock cycles of SCLK, as can be seen on Figures 14 and 15.

CS should first go high at least one clock cycle before the other signals change. One clock cycle is 2.17 μs at a master

clock frequency of 460.8 kHz. CS is clocked in at the falling edge of the CLK1 clock to detect if the data is for the mode register or the DAC.

SCLK can begin to clock in DATA serially to the chip on the falling edge of SCLK. SCLK should have a maximum frequency of 460.8 kHz. The format of the data should be either 8 or 16 bits with the most significant bit first.

DATA is shifted into the chip on the falling edge of SCLK, and thus for correct operation DATA should change only on the rising edge of SCLK. The first bit shifted in is the MSB. If 14 bit DAC communication is utilized, then two 0's should precede the 14 bits, and 16 clock cycles on SCLK should occur. Once the data is shifted in, CS should go low no sooner than one clock cycle after the last rising edge of SCLK.

Table 9. INTERNAL REGISTER DESCRIPTION

Bit	Description
0 (LSB)	0 = DAC in 14−bit mode 1 = DAC in 16−bit mode
1 2	Set the crystal divide so that CLK2 is 460.8 kHz Bit 2 Bit 1 0 0 Crystal/2 0 1 Crystal/4 1 0 Crystal/1 1 1 Crystal/4
3 4	Set the crystal divide for CLK1 Bit 4 Bit 3 0 0 Crystal/2 0 1 Crystal/4 1 0 Crystal/1 1 1 Crystal/4
5	0 = Watchdog kick external (pin) 1 = Watchdog kick internal (1.8 kHz)
6	0 = RTZ output format on DAC 1 = Non RTZ output format on DAC
7 (MSB)	0 = RxD is low when carrier is off 1 = RxD is high when carrier is off Setting this bit, changes the function of RxD to the function of RxD_ENH

Internal Register

The NCN5192 has an 8 bit register to setup its internal operation. An 8 bit SPI communication method is used to write to the mode register. If CS goes low after only 8 clock cycles of SCLK the Mode register will latch in the 8 bits which are shifted into the SPI shift register. In table x an explanation of the usage of each bit is given. All bits are set to '0' at reset.

Sigma Delta DAC

The NCN5192 Modem has an integrated Sigma−Delta Modulator for use in a current loop slave transmitter. Through this DAC, an analog value can be set and transmitted across the current loop. For more information on how to create a current loop slave transmitter, see application notes on the ON Semi website. The DAC output will switch between 0 V and the voltage provided to DACREF. To achieve maximum accuracy, the DACREF voltage should be kept stable, so that power supply variations are not visible in the DAC output. The Sigma−Delta modulator output can be set through SPI frames containing 14 or 16 significant bits. The length of the data frames can be set through bit 0 is the status register. The output of the DAC can be set return to zero (RTZ) or non−RTZ. This is important when the rise and fall time of the signal are not identical. This will cause a DC offset depending on the number of rising and falling edges. As the output bits of a sigma−delta modulator are randomly arranged (ie. for the same setting we could get 01110000 or 01010100), the number of edges might vary over time for a non return to zero signal. Setting the DAC to "return to zero" forces the output to have a rising and falling edge for each logic "1" bit, so that no offset from pulse asymmetry can occur. However, this will decrease the range of the modulator to 50% of DACREF, as the maximum duty cycle is 50% instead of 100% for NRZ. When a clock failure is detected, using an internal oscillator, the DAC output will jump to the level set by the JUMP pin, until the IC is reset or a rising flank is detected on KICK.

Table 10. SPI FRAME FORMAT

Description	Bits	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode Register	8									Mode Register Data							
DAC − 14 bits mode	16	0	0	DAC Output Word													
DAC − 16 bits mode	16	DAC Output Word															

Ordering Information

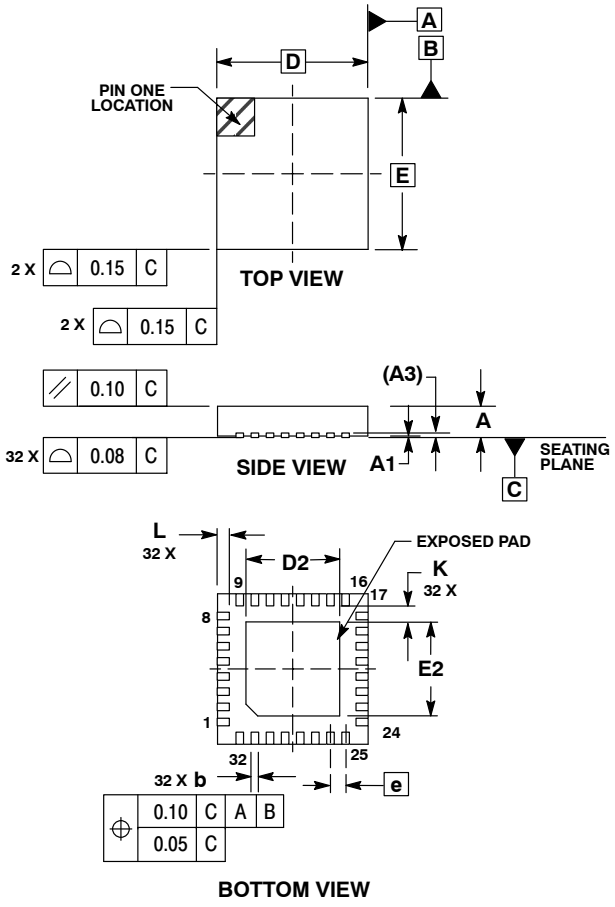
The NCN5192 is available in a 32−pin no lead quad flat pack (NQFP). Use the following part numbers when ordering. Contact your local sales representative for more information: www.onsemi.com.

Table 11. ORDERING INFORMATION

Part Number	Package	Shipping Configuration	Temperature Range
NCN5192MNG	32−pin NQFP Green/RoHS compliant	____ Tube/Tray	−40°C to +85°C (Industrial)
NCN5192MNRG	32−pin NQFP Green/RoHS compliant	____ Tape & Reel	−40°C to +85°C (Industrial)

PACKAGE DIMENSIONS

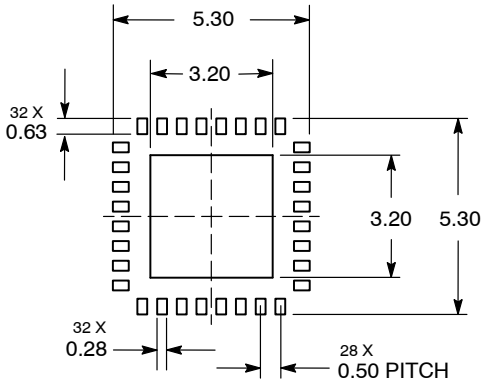
QFN32 5*5*1 0.5 P
CASE 488AM−01
ISSUE O



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.800	0.900	1.000
A1	0.000	0.025	0.050
A3		0.200 REF	
b	0.180	0.250	0.300
D		5.00 BSC	
D2	2.950	3.100	3.250
E		5.00 BSC	
E2	2.950	3.100	3.250
e		0.500 BSC	
K	0.200	−−−	−−−
L	0.300	0.400	0.500

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
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