# PEEL™ 18CV8Z-25
# CMOS Programmable Electrically Erasable Logic Device

## Features

**Ultra Low Power Operation**
- Vcc = 5 Volts ±10%
- Icc = 10 µA (typical) at standby
- Icc = 2 mA (typical) at 1 MHz

**CMOS Electrically Erasable Technology**
- Superior factory testing
- Reprogrammable in plastic package
- Reduces retrofit and development costs

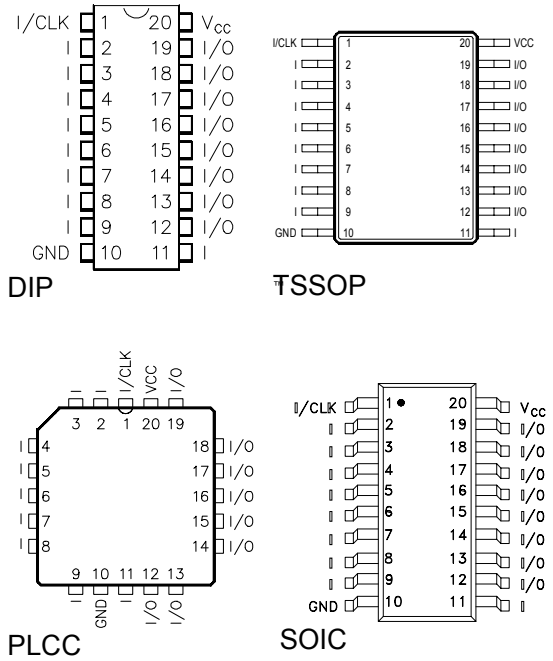
**Application Versatility**
- Replaces random logic
- Super set of standard PLDs
- Pin and JEDEC compatible with 16V8
- Ideal for use in power-sensitive systems

**Architectural Flexibility**
- Enhanced architecture fits in more logic
- 113 product terms x 36 input AND array
- 10 inputs and 8 I/O pins
- 12 possible macrocell configurations
- Asynchronous clear, Synchronous preset
- Independent output enables
- Programmable clock; pin 1 or p-term
- Programmable clock polarity
- 20 Pin DIP/SOIC/TSSOP and PLCC

## General Description

The PEEL™18CV8Z is a Programmable Electrically Erasable Logic (PEEL™) SPLD (Simple Programmable Logic Device) that features ultra-low, automatic "zero" power-down operation. The "zero power" (100 µA max. Icc) power-down mode makes the PEEL™18CV8Z ideal for a broad range of battery-powered portable equipment applications, from hand-held meters to PCM-CIA modems. EE-reprogrammability provides both the convenience of fast reprogramming for product development and quick product personalization in manufacturing, including Engineering Change Orders.

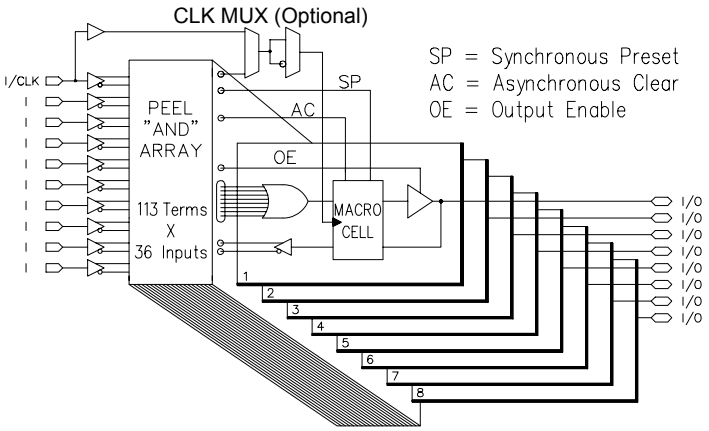
### Figure 7 Pin Configuration




The PEEL™18CV8Z is logically and functionally similar to Anachip's 5 Volt PEEL™18CV8 and 3 Volt PEEL™18LV8Z. The differences between the PEEL™18CV8Z and PEEL™18CV8 include the addition of programmable clock polarity, a product term clock, and variable width product terms in the AND/OR Logic Array.

Like the PEEL™18CV8, the PEEL™18CV8Z is logical superset of the industry standard PAL16V8 SPLD. The PEEL™18CV8Z provides additional architectural features that allow more logic to be incorporated into the design. Anachip's JEDEC file translator allows easy conversion of existing 20 pin PLD designs to the PEEL™18CV8Z architecture without the need for redesign. The PEEL™18CV8Z architecture allows it to replace over twenty standard 20-pin DIP, SOIC, TSSOP and PLCC packages.

### Figure 8 Block Diagram

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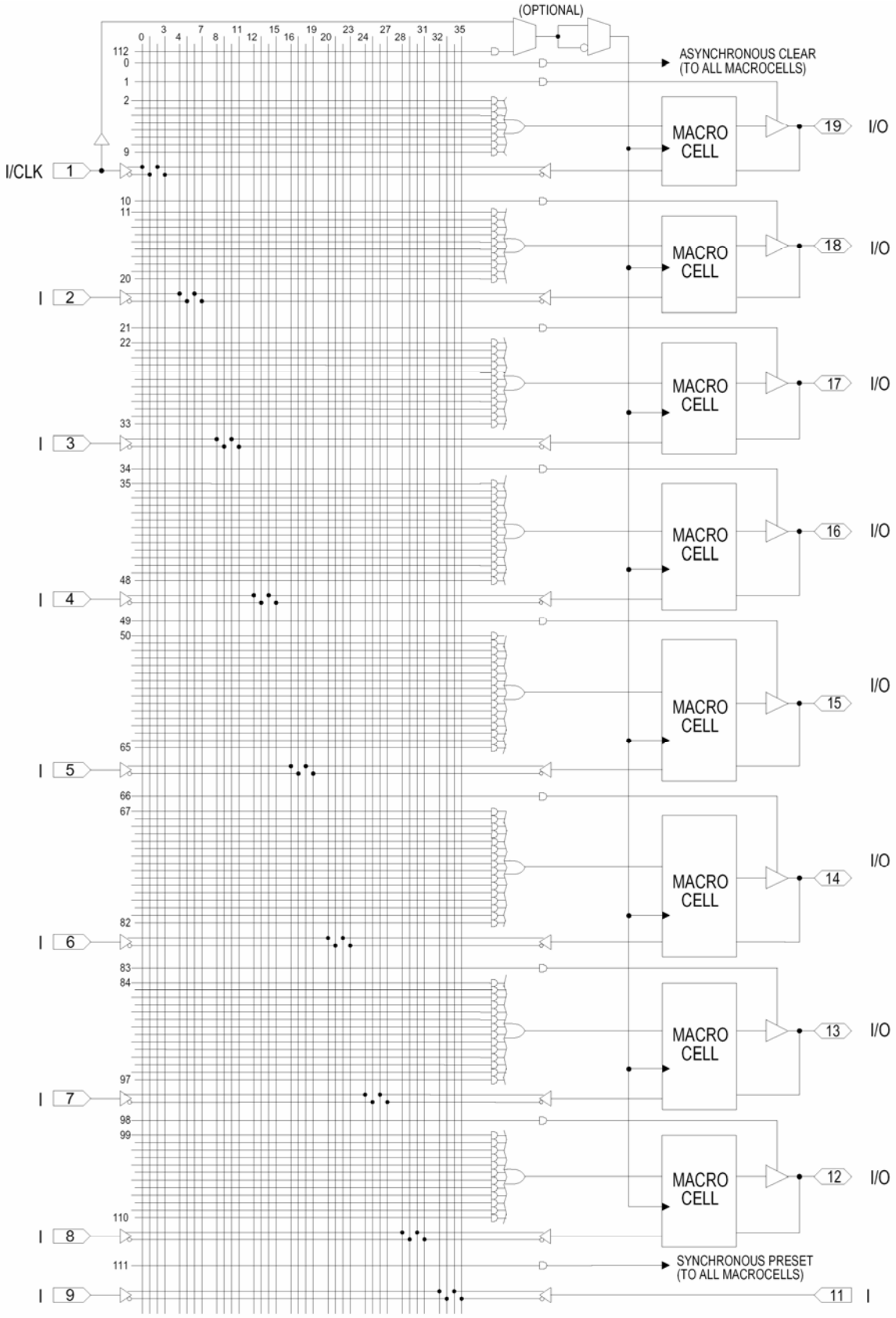



**Figure 9 PEEL™18CV8Z Logic Array Diagram**

## Function Description

The PEEL™18CV8Z implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

## Architecture Overview

The PEEL™18CV8Z architecture is illustrated in the block diagram of Figure 8. Ten dedicated inputs and 8 I/Os provide up to 18 inputs and 8 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array that drives a fixed OR array. With this structure, the PEEL™18CV8Z can implement up to eight sum-of-products logic expressions.

Associated with each of the eight OR functions is an I/O macrocell that can be independently programmed to one of 12 different configurations. The programmable macrocells allow each I/O to be used to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

## AND/OR Logic Array

The programmable AND array of the PEEL™18CV8Z (shown in Figure 9) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

**36 Input Lines:**

– 20 input lines carry the true and complement of the signals applied to the 10 input pins
– 16 additional lines carry the true and complement values of feedback or input signals from the 8 I/Os

**113 product terms:**

– 102 product terms are used to form sum of product functions
– 8 output enable terms (one for each I/O)
– 1 global synchronous preset term
– 1 global asynchronous clear term
– 1 programmable clock term

At each input-line/product-term intersection, there is an EEPROM memory cell that determines whether or not there is a logical connection at that intersection. Each product term is essentially a 36-input AND gate. A product term that is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a "don't care" state exists and that term will always be TRUE. When programming the PEEL™18CV8Z, the device program- mer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by pro- gramming selected connections in the AND array. (Note that PEEL™ device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function).

## Variable Product Term Distribution

The PEEL™18CV8Z provides 113 product terms to drive the eight OR functions. These product terms are distributed among the outputs in groups of 8, 10, 12, 14, and 16 to form logical sums (see Figure 9). This distribution allows optimum use of the device resources.

## Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently lets you to tailor the configuration of the PEEL™18CV8Z to the precise requirements of your design.

## Macrocell Architecture

Each I/O macrocell, as shown in Figure 9, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine output polarity, output type (registered or non-registered) and input-feedback path (bidirectional I/O, combinatorial feedback). Refer to Table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 11. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10), the macrocell provides eight additional configurations. When creating a PEEL™ device design, the desired macrocell configuration is generally specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

## Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register is set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear sets Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

## Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

## Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to

the I/O pin. Otherwise, the output buffer is switched into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/ O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will always be logically false and the I/O will function as a dedicated input.

## Input/Feedback Select

The PEEL™18CV8Z macrocell also provides control over the feedback path. The input/feedback signal associated with each I/ O macrocell can be obtained from three different locations; from the I/O input pin, from the Q output of the flip-flop (registered feedback), or directly from the OR gate (combinatorial feedback).

## Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with a bi-directional I/O, refer to Figure 9).

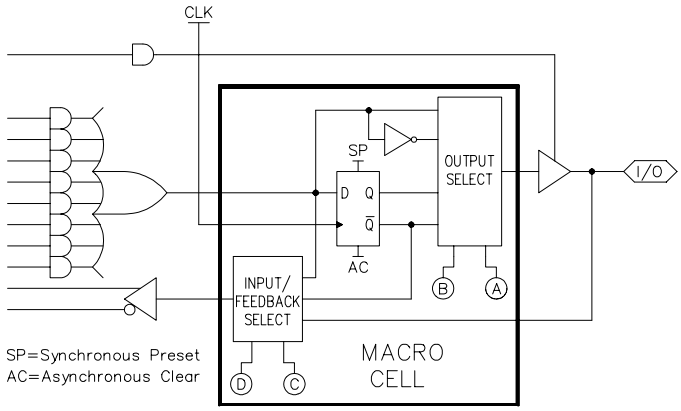
## Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output of the OR gate, bypassing the output buffer, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in Figure 11.)

## Figure 9 Block Diagram of the PEEL™18CV8Z I/O Macrocell

## Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is programmed to be combinatorial or registered. When implementing a combinatorial output function, registered feedback allows for the internal latching of states without giving up the use of the external output.




## Programmable Clock Options

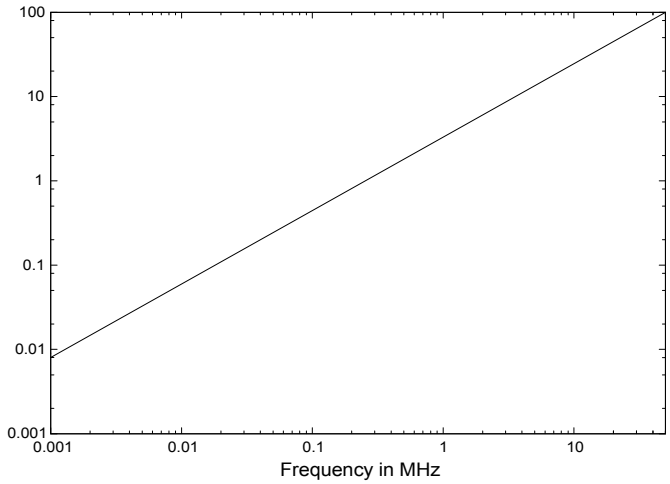
A unique feature of the PEEL™18CV8Z is a programmable clock multiplexer that allows the user to select true or complement forms of either input pin or product-term clock sources.

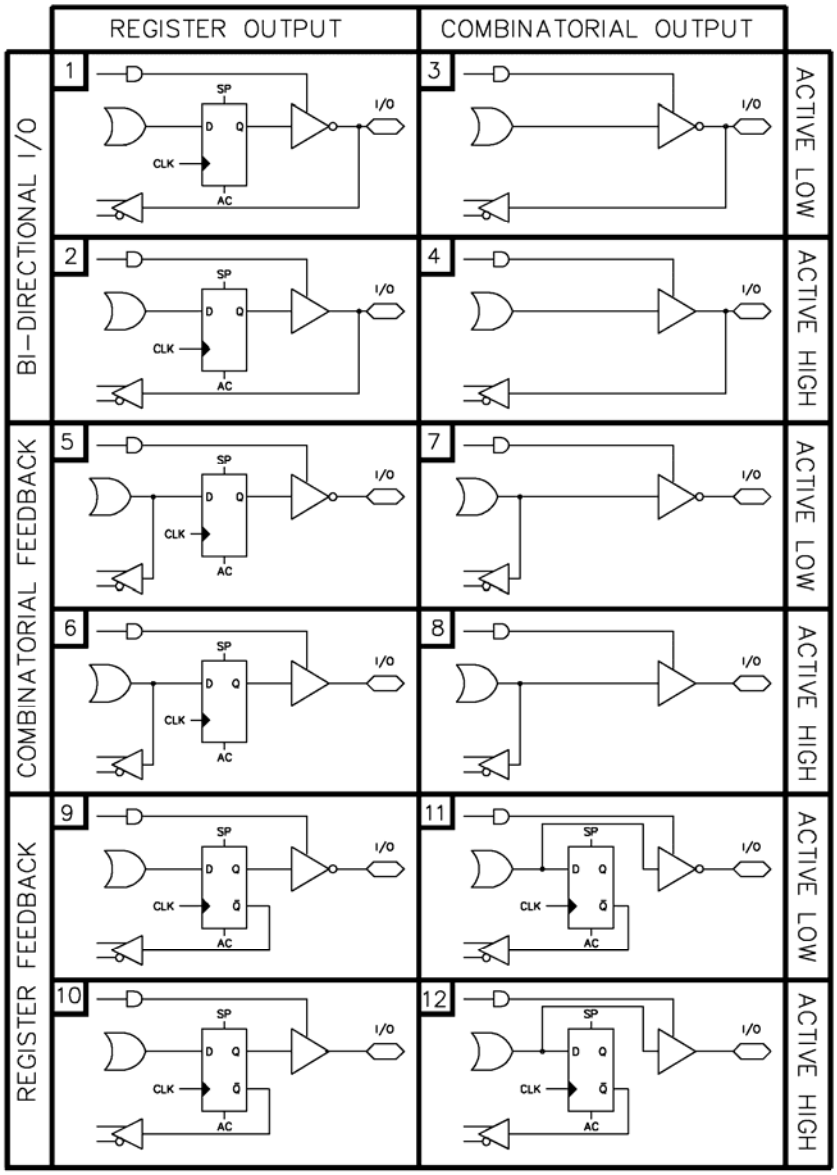
## Zero Power Feature

The CMOS PEEL™18CV8Z features "Zero-Power" standby operation for ultra-low power consumption. With the "Zero-Power" feature, transition-detection circuitry monitors the inputs, I/Os (including CLK) and feedbacks. If these signals do not change for a period of time greater than approximately two $t_{PD}$'s, the outputs are latched in their current state and the device automatically powers down. When the next signal transition is detected, the device will "wake up" for active operation until the signals stop switching long enough to trigger the next power-down. (Note that the tPD is approximately 5 ns. slower on the first transition from sleep mode.)

As a result of the "Zero-Power" feature, significant power savings can be realized for combinatorial or sequential operations when the inputs or clock change at a modest rate. See Figure 5.

## Figure 10 Typical ICC vs. Input Clock Frequency for the 18CV8Z






| Configuration | | | | | Input/Feedback Select | Output Select | |
|---|---|---|---|---|---|---|---|
| # | A | B | C | D | | | |
| 1 | 0 | 0 | 1 | 0 | Bi-directional I/O | Register | Active Low |
| 2 | 1 | 0 | 1 | 0 | | | Active High |
| 3 | 0 | 1 | 0 | 0 | | Combinatorial | Active Low |
| 4 | 1 | 1 | 0 | 0 | | | Active High |
| 5 | 0 | 0 | 1 | 1 | Combinatorial Feedback | Register | Active Low |
| 6 | 1 | 0 | 1 | 1 | | | Active High |
| 7 | 0 | 1 | 1 | 1 | | Combinatorial | Active Low |
| 8 | 1 | 1 | 1 | 1 | | | Active High |
| 9 | 0 | 0 | 0 | 0 | Register Feedback | Register | Active Low |
| 10 | 1 | 0 | 0 | 0 | | | Active High |
| 11 | 0 | 1 | 1 | 0 | | Combinatorial | Active Low |
| 12 | 1 | 1 | 1 | 0 | | | Active High |

## Design Security

The PEEL™18CV8Z provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL™ until the entire device has first been erased with the bulk-erase function.

## Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL™18CV8Z if the software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

## Programming Support

Anachip's JEDEC file translator allows easy conversion of existing 20 pin PLD designs to the PEEL™18CV8Z, without the need for redesign. Anachip also offers (for free) its proprietary Win-PLACE software, an easy-to-use entry level PC-based software development system.

Programming support includes all the popular third party programmers such as BP Microsystems, System General, Logical Devices, and numerous others.

This device has been designed and tested for the specified operating ranges. Improper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

## Absolute Maximum Ratings

| Symbol | Parameter | Conditions | Rating | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Relative to Ground | -0.5 to +7.0 | V |
| $V_I$ , $V_O$ | Voltage Applied to Any Pin[2] | Relative to Ground[1] | -0.5 to $V_{CC}$+0.6 | V |
| $I_O$ | Output Current | Per Pin ($I_{OL}$, $I_{OH}$) | ±25 | mA |
| $T_{ST}$ | Storage Temperature | | -65 to +150 | °C |
| $T_{LT}$ | Lead Temperature | Soldering 10 Seconds | +300 | °C |

## Operating Range

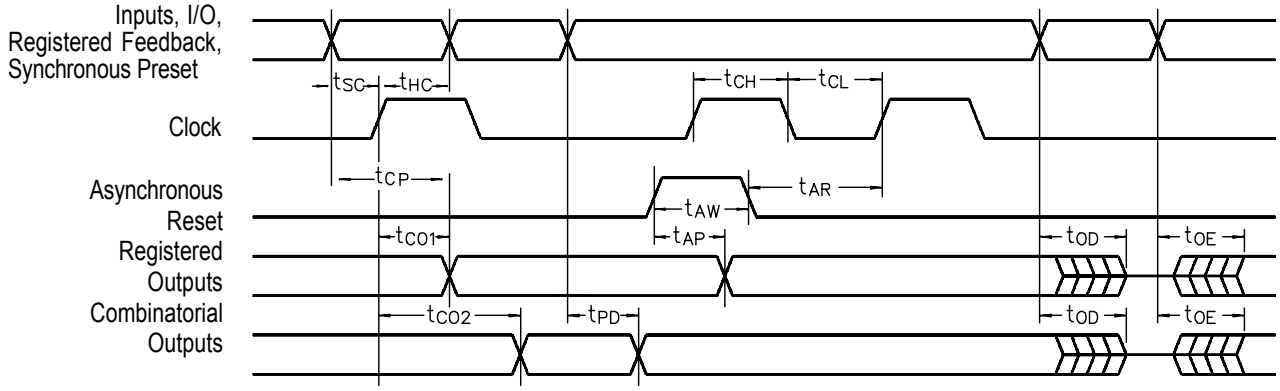
| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | Commercial | 4.75 | 5.25 | V |
| | | Industrial | 4.5 | 5.5 | V |
| $T_A$ | Ambient Temperature | Commercial | 0 | +70 | °C |
| | | Industrial | -40 | +85 | °C |
| $T_R$ | Clock Rise Time | See Note 3. | | 20 | ns |
| $T_F$ | Clock Fall Time | See Note 3. | | 20 | ns |
| $T_{RVCC}$ | $V_{CC}$ Rise Time | See Note 3. | | 250 | ms |

## D.C. Electrical Characteristics Over the operating range (Unless otherwise specified)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage – TTL | $V_{CC}$ = Min, $I_{OH}$ = -4.0 mA | 2.4 | | V |
| $V_{OHC}$ | Output HIGH Voltage – CMOS | $V_{CC}$ = Min, $I_{OH}$ = -10.0µA | $V_{CC}$-0.3 | | V |
| $V_{OL}$ | Output LOW Voltage – TTL | $V_{CC}$ = Min, $I_{OL}$ = 16.0 mA | | 0.5 | V |
| $V_{OLC}$ | Output LOW Voltage – CMOS | $V_{CC}$ = Min, $I_{OL}$ = 10.0µA | | 0.15 | V |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | $V_{CC}$+0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | -0.3 | 0.8 | V |
| $I_{IL}$ | Input and I/O Leakage Current | $V_{CC}$=Max, GND≤$V_{IN}$ ≤$V_{CC}$, I/O = High Z | | ±10 | µA |
| $I_{SC}$[9] | Output Short Circuit Current | $V_{CC}$ = Max, $V_O$ = 0.5V, $T_A$ = 25°C | -30 | -135 | mA |
| $I_{CCS}$ | $V_{CC}$ Current, Standby | $V_{IN}$ = 0V or $V_{CC}$, All Outputs disabled[4] | 10 (typ) | 100 | µA |
| $I_{CC}$[10] | $V_{CC}$ Current, f=1MHz | $V_{IN}$ = 0V or $V_{CC}$, All Outputs disabled[4] | 2 (typ) | 5 | mA |
| $C_{IN}$[7] | Input Capacitance | $T_A$ = 25°C, $V_{CC}$ = Max @ f = 1 MHz | | 6 | pF |
| $C_{OUT}$[7] | Output Capacitance | | | 12 | pF |

| Symbol | Parameter | -25 / I-25 | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{PD}$ | Input[5] to non-registered output | | 25 | ns |
| $t_{OE}$ | Input[5] to output enable[6] | | 25 | ns |
| $t_{OD}$ | Input[5] to output disable[6] | | 25 | ns |
| $t_{CO1}$ | Clock to Output | | 15 | ns |
| $t_{CO2}$ | Clock to comb. output delay via internal registered feedback | | 35 | ns |
| $t_{CF}$ | Clock to Feedback | | 9 | ns |
| $t_{SC}$ | Input[5] or feedback setup to clock | 15 | | ns |
| $t_{HC}$ | Input[5] hold after clock | 0 | | ns |
| $t_{CL}$, $t_{CH}$ | Clock low time, clock high time[8] | 13 | | ns |
| $t_{CP}$ | Min clock period Ext ($t_{SC} + t_{CO1}$) | 30 | | ns |
| $f_{MAX1}$ | Internal feedback ($1/t_{SC} + t_{CF}$)[11] | 41.6 | | MHz |
| $f_{MAX2}$ | External feedback ($1/t_{CP}$)[11] | 33.3 | | MHz |
| $f_{MAX3}$ | No feedback ($1/t_{CL} + t_{CH}$)[11] | 38.4 | | MHz |
| $t_{AW}$ | Asynchronous Reset Pulse Width | 25 | | ns |
| $t_{AP}$ | Input[5] to Asynchronous Reset | | 25 | ns |
| $t_{AR}$ | Asynchronous Reset recovery time | | 25 | ns |
| $t_{RESET}$ | Power-on reset time for registers in clear state[12] | | 5 | µs |

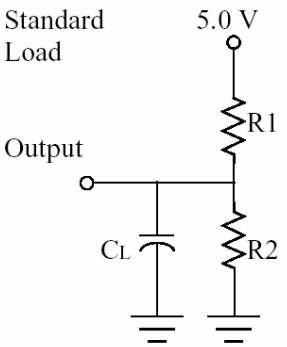
## Switching Waveforms

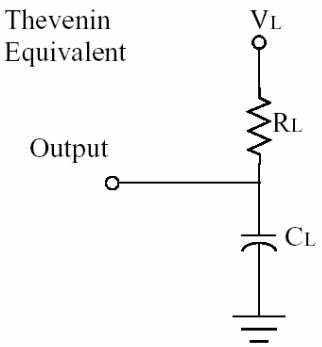



Notes:

1. Minimum DC input is -0.5V, however, inputs may undershoot to -2.0V for periods less than 20 ns.
2. VI and VO are not specified for program/verify operation.
3. Test Points for Clock and VCC in tR and tF are referenced at the 10% and 90% levels.
4. I/O pins are 0V and VCC.
5. "Input" refers to an input pin signal.
6. tOE is measured from input transition to VREF±0.1V,
TOD is measured from input transition to VOH-0.1V or VOL+0.1V; VREF=VL.
7. Capacitances are tested on a sample basis.
8. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (Unless otherwise specified).
9. Test one output at a time for a duration of less than 1 second.
10. ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
11. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design process modification that might affect operational frequency.
12. All input at GND.

## PEEL™ Device and Array Test Loads



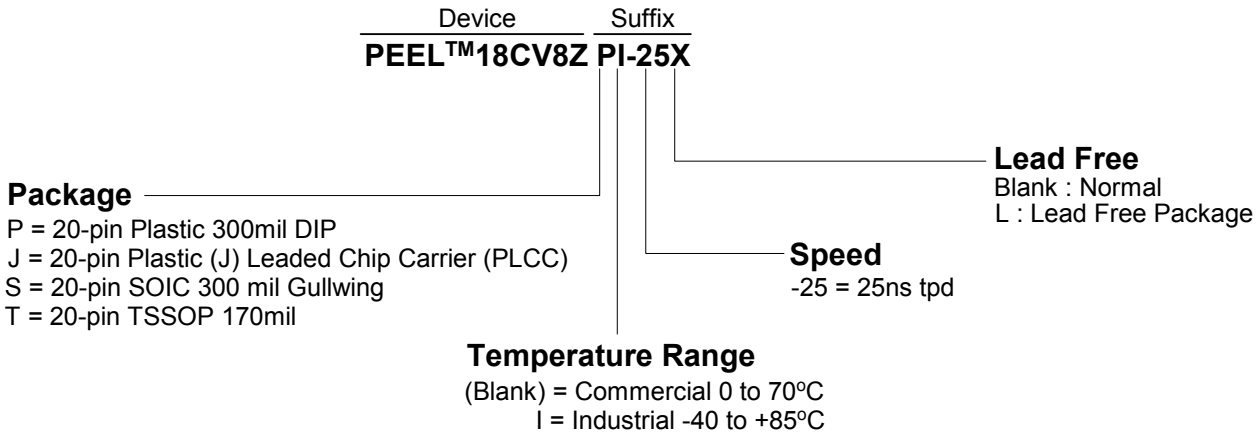




| Technology | R1 | R2 | $R_L$ | $V_L$ | $C_L$ |
|---|---|---|---|---|---|
| CMOS | 480kΩ | 480kΩ | 228Ω | 2.375V | 33 pF |
| TTL | 235Ω | 159Ω | 95Ω | 2.02V | 33 pF |

## Ordering Information

| Part Number | Speed | Temperature | Package |
|---|---|---|---|
| PEEL18CV8ZP-25 (L) | 25ns | Commercial | 20-pin Plastic DIP |
| PEEL18CV8ZJ-25 (L) | 25ns | Commercial | 20-pin PLCC |
| PEEL18CV8ZS-25 (L) | 25ns | Commercial | 20-pin SOIC |
| PEEL18CV8ZT-25 (L) | 25ns | Commercial | 20-pin TSSOP |
| PEEL18CV8ZPI-25 (L) | 25ns | Industrial | 20-pin Plastic DIP |
| PEEL18CV8ZJI-25 (L) | 25ns | Industrial | 20-pin PLCC |
| PEEL18CV8ZSI-25 (L) | 25ns | Industrial | 20-pin SOIC |
| PEEL18CV8ZTI-25 (L) | 25ns | Industrial | 20-pin TSSOP |

## Part Number



Anachip Corp.
Head Office,
2F, No. 24-2, Industry E. Rd. IV, Science-Based
Industrial Park, Hsinchu, 300, Taiwan
Tel: +886-3-5678234
Fax: +886-3-5678368

Anachip USA
780 Montague Expressway, #201
San Jose, CA 95131
Tel: (408) 321-9600
Fax: (408) 321-9696

Email: sales_usa@anachip.com
Website: http://www.anachip.com

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