

MC74VHC1GT04

Inverting Buffer / CMOS Logic Level Shifter LSTTL-Compatible Inputs

The MC74VHC1GT04 is a single gate inverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output.

The device input is compatible with TTL-type input thresholds and the output has a full 5 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic-level translator from 3 V CMOS logic to 5 V CMOS Logic or from 1.8 V CMOS logic to 3 V CMOS Logic while operating at the high-voltage power supply.

The MC74VHC1GT04 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT04 to be used to interface 5 V circuits to 3 V circuits. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 3.8$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 1$ μ A (Max) at $T_A = 25^\circ$ C
- TTL-Compatible Inputs: $V_{IL} = 0.8$ V; $V_{IH} = 2$ V
- CMOS-Compatible Outputs: $V_{OH} > 0.8 V_{CC}$; $V_{OL} < 0.1 V_{CC}$ @ Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 105; Equivalent Gates = 26
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

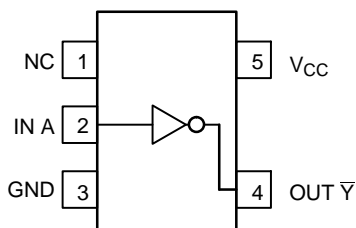


Figure 1. Pinout (Top View)

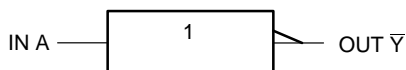


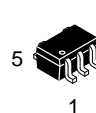
Figure 2. Logic Symbol



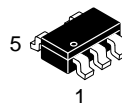
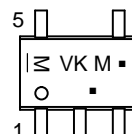
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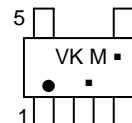
MARKING DIAGRAMS



SC-88A
DF SUFFIX
CASE 419A



TSOP-5
DT SUFFIX
CASE 483



VK = Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN ASSIGNMENT

| PIN ASSIGNMENT | |
|----------------|---------------|
| 1 | NC |
| 2 | IN A |
| 3 | GND |
| 4 | OUT \bar{Y} |
| 5 | V_{CC} |

FUNCTION TABLE

| A Input | \bar{Y} Output |
|---------|------------------|
| L | H |
| H | L |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MC74VHC1GT04

MAXIMUM RATINGS

| Symbol | Characteristics | Value | Unit |
|---------------|---|--|------|
| V_{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V_{IN} | DC Input Voltage | -0.5 to +7.0 | V |
| V_{OUT} | DC Output Voltage | $V_{CC} = 0$ High or Low State -0.5 to 7.0 -0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | Input Diode Current | -20 | mA |
| I_{OK} | Output Diode Current | $V_{OUT} < GND; V_{OUT} > V_{CC}$ +20 | mA |
| I_{OUT} | DC Output Current, per Pin | +25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND | +50 | mA |
| P_D | Power dissipation in still air | SC-88A, TSOP-5 200 | mW |
| θ_{JA} | Thermal resistance | SC-88A, TSOP-5 333 | °C/W |
| T_L | Lead temperature, 1 mm from case for 10 s | 260 | °C |
| T_J | Junction temperature under bias | +150 | °C |
| T_{stg} | Storage temperature | -65 to +150 | °C |
| V_{ESD} | ESD Withstand Voltage | Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3) 2000 200 N/A | V |
| $I_{Latchup}$ | Latchup Performance | Above V_{CC} and Below GND at 125°C (Note 4) ± 100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|------------|-----------------------------|--|-----------------|------|
| V_{CC} | DC Supply Voltage | 3.0 | 5.5 | V |
| V_{IN} | DC Input Voltage | 0.0 | 5.5 | V |
| V_{OUT} | DC Output Voltage | $V_{CC} = 0$ High or Low State 0.0 0.0 | 5.5 V_{CC} | V |
| T_A | Operating Temperature Range | -55 | +125 | °C |
| t_r, t_f | Input Rise and Fall Time | $V_{CC} = 3.3 V \pm 0.3 V$ $V_{CC} = 5.0 V \pm 0.5 V$ 0 0 | 100 20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

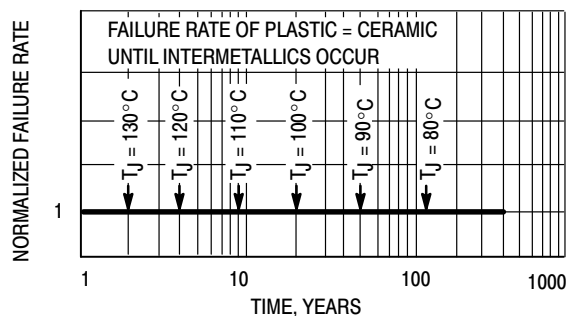


Figure 3. Failure Rate vs. Time Junction Temperature

MC74VHC1GT04

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | -55 ≤ T _A ≤ 125°C | | Unit |
|--------------------|---|--|---------------------|-----------------------|------------|--------------------|-----------------------|--------------------|------------------------------|--------------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 3.0 4.5 5.5 | 1.4 2.0 2.0 | | | 1.4 2.0 2.0 | | 1.4 2.0 2.0 | V | |
| V _{IL} | Maximum Low-Level Input Voltage | | 3.0 4.5 5.5 | | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | | 0.53 0.8 0.8 | V |
| V _{OH} | Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 3.0 4.5 | 2.9 4.4 | 3.0 4.5 | | 2.9 4.4 | | 2.9 4.4 | V | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | 2.34 3.66 | V | |
| V _{OL} | Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 3.0 4.5 | | 0.0 0.0 | 0.1 0.1 | | 0.1 0.1 | | 0.1 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 4.0 mA I _{OL} = 8.0 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | | 0.52 0.52 | V |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 1.0 | | 20 | | 40 | μA |
| I _{CC(T)} | Quiescent Supply Current | Input: V _{IN} = 3.4 V | 5.5 | | | 1.35 | | 1.50 | | 1.65 | mA |
| I _{OPD} | Output Leakage Current | V _{OUT} = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS C_{load} = 50 pF, Input t_r = t_f = 3.0 ns

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A ≤ 85°C | | -55 ≤ T _A ≤ 125°C | | Unit |
|--|---|---|-----------------------|------------|--------------|-----------------------|--------------|------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A to Y | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 5.0 6.2 | 10.0 13.5 | | 11.0 15.0 | | 13.0 17.5 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 3.8 4.2 | 6.7 7.7 | | 7.5 8.5 | | 8.5 9.5 | |
| C _{IN} | Maximum Input Capacitance | | | 5.0 | 10 | | 10 | | 10 | pF |

| C _{PD} | Power Dissipation Capacitance (Note 5) | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
|-----------------|--|---|--|----|
| | | 10 | | |
| | | | | |

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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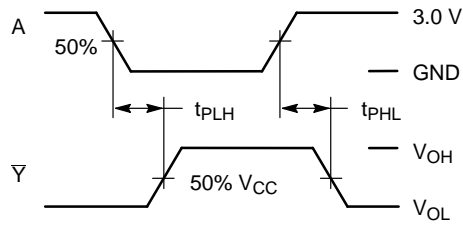
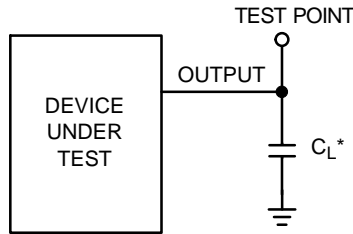


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance

Figure 5. Test Circuit

ORDERING INFORMATION

| Device | Package Type | Package [†] |
|-------------------|---------------------|----------------------|
| M74VHC1GT04DFT1G | SC-88A (Pb-Free) | 3000 / Tape & Reel |
| NLVVHC1GT04DFT1G* | | |
| M74VHC1GT04DFT2G | | |
| NLVVHC1GT04DFT2G* | | |
| M74VHC1GT04DFT3G | TSOP-5 (Pb-Free) | |
| M74VHC1GT04DFT1G | | |
| NLVVHC1GT04DFT1G* | | |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

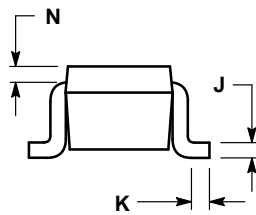
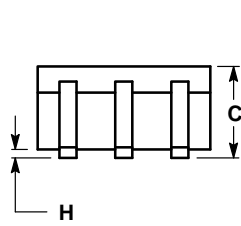
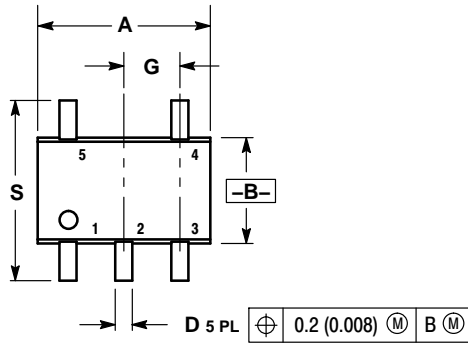
MC74VHC1GT04

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)

CASE 419A-02

ISSUE L

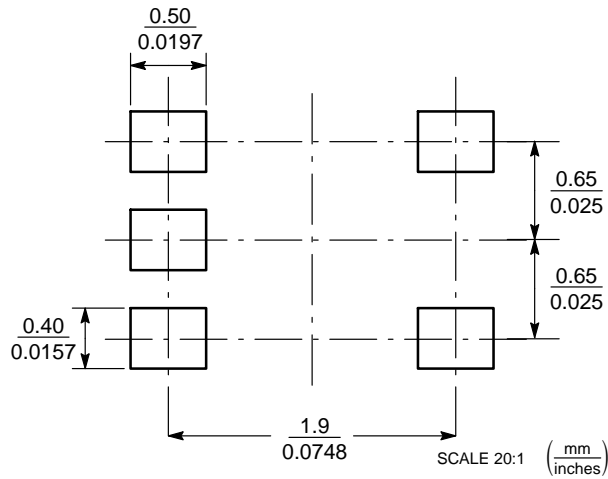


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

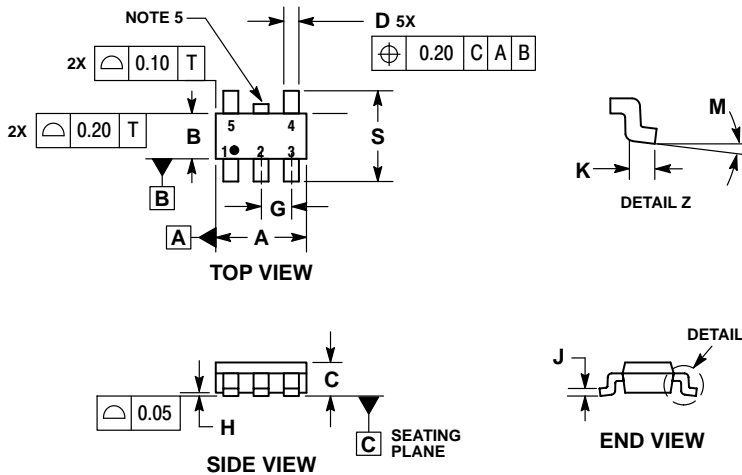
SOLDER FOOTPRINT



MC74VHC1GT04

PACKAGE DIMENSIONS

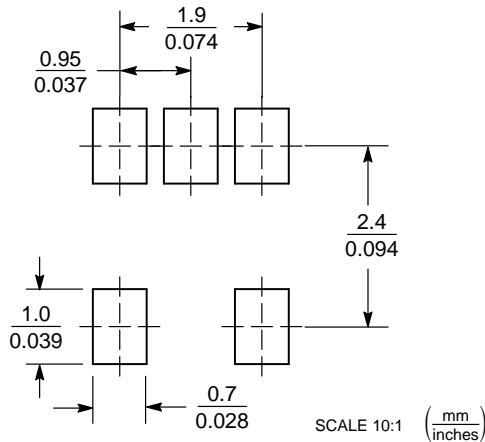
TSOP-5
CASE 483
ISSUE M



NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: MILLIMETERS.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
- DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
- OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Специальные условия для постоянных клиентов.
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- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
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- Наличие сертификата ISO.

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- Техническую поддержку проекта.
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- Изготовление тестовой платы монтаж и пусконаладочные работы.



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