

# TPH2R903PL

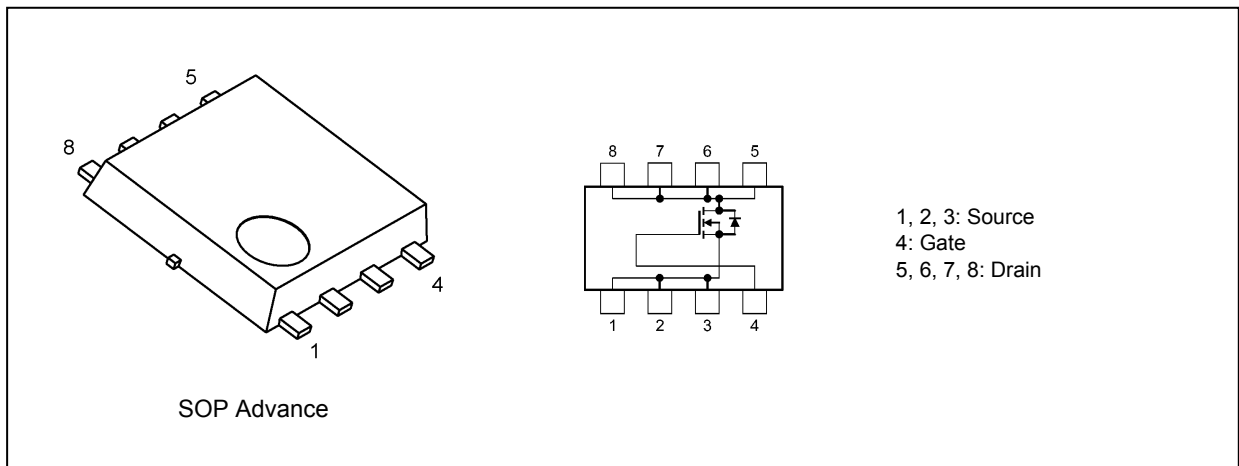
## 1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

## 2. Features

- (1) High-speed switching
- (2) Small gate charge:  $Q_{SW} = 5.6 \text{ nC (typ.)}$
- (3) Small output charge:  $Q_{OSS} = 17 \text{ nC (typ.)}$
- (4) Low drain-source on-resistance:  $R_{DS(ON)} = 2.1 \text{ m}\Omega \text{ (typ.) (} V_{GS} = 10 \text{ V)}$
- (5) Low leakage current:  $I_{DSS} = 10 \text{ }\mu\text{A (max) (} V_{DS} = 30 \text{ V)}$
- (6) Enhancement mode:  $V_{th} = 1.1 \text{ to } 2.1 \text{ V (} V_{DS} = 10 \text{ V, } I_D = 0.2 \text{ mA)}$

## 3. Packaging and Internal Circuit



Start of commercial production

2016-08

**4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	30	V
Gate-source voltage (Note 1)	$V_{GSS}$	$\pm 20$	
Drain current (DC) ( $T_c = 25\text{ }^\circ\text{C}$ ) (Note 2)	$I_D$	70	A
Drain current (DC) (Silicon limit) (Note 2), (Note 3)	$I_D$	124	
Drain current (pulsed) ( $t = 100\text{ }\mu\text{s}$ ) (Note 2)	$I_{DP}$	250	
Power dissipation ( $T_c = 25\text{ }^\circ\text{C}$ )	$P_D$	81	W
Power dissipation (Note 4)	$P_D$	3	
Power dissipation (Note 5)	$P_D$	0.96	
Single-pulse avalanche energy (Note 6)	$E_{AS}$	25	mJ
Single-pulse avalanche current (Note 6)	$I_{AS}$	70	A
Channel temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to 175	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**5. Thermal Characteristics**

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance ( $T_c = 25\text{ }^\circ\text{C}$ )	$R_{th(ch-c)}$	1.83	$^\circ\text{C/W}$
Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^\circ\text{C}$ ) (Note 4)	$R_{th(ch-a)}$	50	
Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^\circ\text{C}$ ) (Note 5)	$R_{th(ch-a)}$	156	

Note 1: +20V /-16V ensured at DC condition.

-20V ensured at pulse condition(duty 5%).

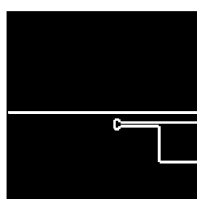
Note 2: Ensure that the channel temperature does not exceed 175  $^\circ\text{C}$ .

Note 3: Limited by silicon chip capability.

Note 4: Device mounted on a glass-epoxy board (a), Figure 5.1

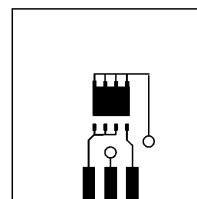
Note 5: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 6:  $V_{DD} = 24\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (initial),  $L = 4\text{ }\mu\text{H}$ ,  $I_{AS} = 70\text{ A}$



FR-4  
25.4 × 25.4 × 1.6  
(Unit: mm)  
2oz copper

**Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)**



FR-4  
25.4 × 25.4 × 1.6  
(Unit: mm)  
2oz copper

**Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)**

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

**6. Electrical Characteristics**

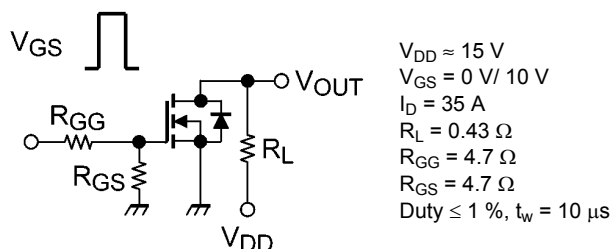
**6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	—	—	$\pm 0.1$	$\mu\text{A}$
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	—	—	10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$	30	—	—	V
Drain-source breakdown voltage (Note 7)	$V_{(BR)DSX}$	$I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$	15	—	—	
Gate threshold voltage	$V_{th}$	$V_{DS} = 10\text{ V}, I_D = 0.2\text{ mA}$	1.1	—	2.1	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = 4.5\text{ V}, I_D = 30\text{ A}$	—	3.0	4.1	$\text{m}\Omega$
		$V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	—	2.1	2.9	

Note 7: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

**6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	$C_{iss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	1780	2300	$\text{pF}$
Reverse transfer capacitance	$C_{rss}$		—	60	115	
Output capacitance	$C_{oss}$		—	620	—	
Gate resistance	$r_g$	—	—	1.2	1.8	$\Omega$
Switching time (rise time)	$t_r$	See Fig. 6.2.1	—	4.7	—	ns
Switching time (turn-on time)	$t_{on}$		—	12	—	
Switching time (fall time)	$t_f$		—	8.2	—	
Switching time (turn-off time)	$t_{off}$		—	30	—	



**Fig. 6.2.1 Switching Time Test Circuit**

**6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

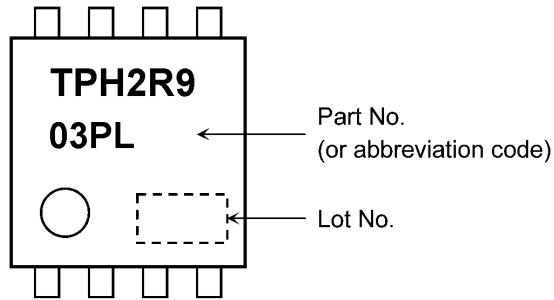
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	$Q_g$	$V_{DD} \approx 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	—	26	—	nC
		$V_{DD} \approx 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 35\text{ A}$	—	12	—	
Gate-source charge 1	$Q_{gs1}$	$V_{DD} \approx 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 35\text{ A}$	—	5.9	—	
Gate-drain charge	$Q_{gd}$		—	2.5	—	
Gate switch charge	$Q_{sw}$		—	5.6	—	
Output charge	$Q_{oss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	17	—	

**6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note 8)	$I_{DRP}$ ( $t = 100\text{ }\mu\text{s}$ )	—	—	—	250	A
Diode forward voltage	$V_{DSF}$	$I_{DR} = 70\text{ A}$ , $V_{GS} = 0\text{ V}$	—	—	-1.2	V
Reverse recovery time	$t_{rr}$	$I_{DR} = 17.5\text{ A}$ , $V_{GS} = 0\text{ V}$ , $-di_{DR}/dt = 100\text{ A}/\mu\text{s}$	—	28	—	ns
Reverse recovery charge	$Q_{rr}$		—	17	—	nC

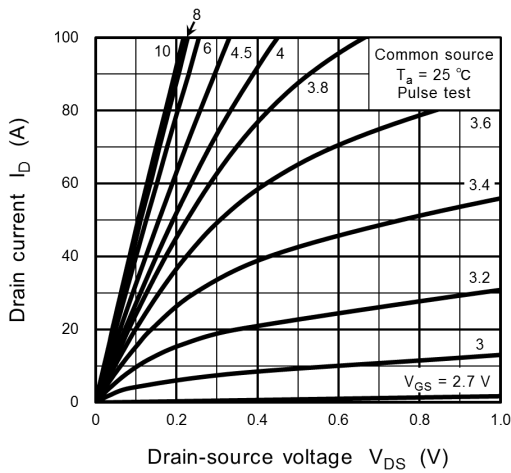
Note 8: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

**7. Marking**

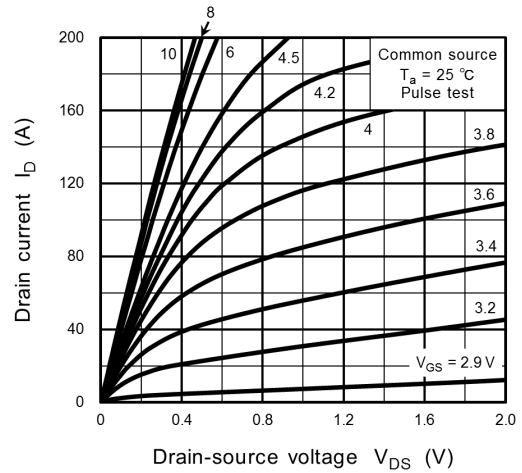


**Fig. 7.1 Marking**

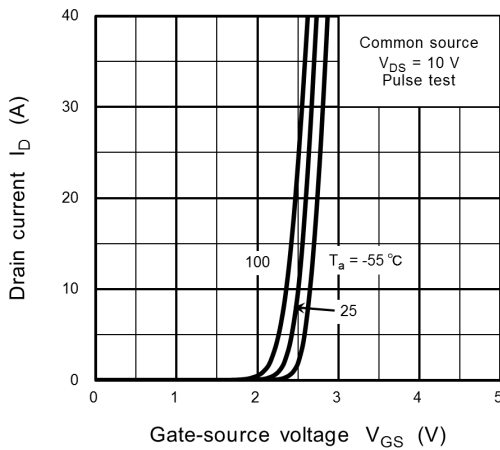
**8. Characteristics Curves (Note)**



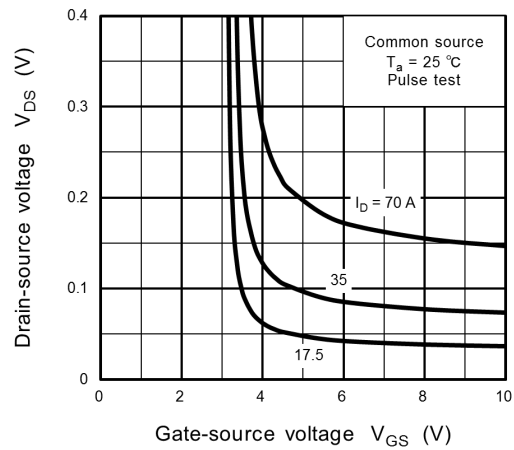
**Fig. 8.1  $I_D - V_{DS}$**



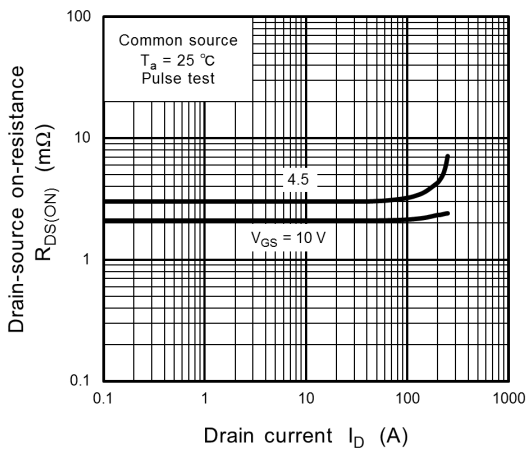
**Fig. 8.2  $I_D - V_{DS}$**



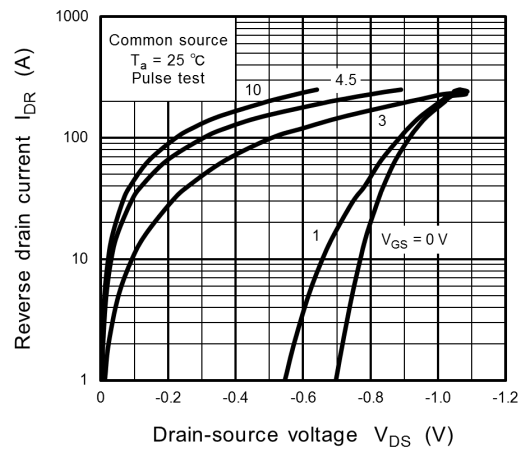
**Fig. 8.3  $I_D - V_{GS}$**



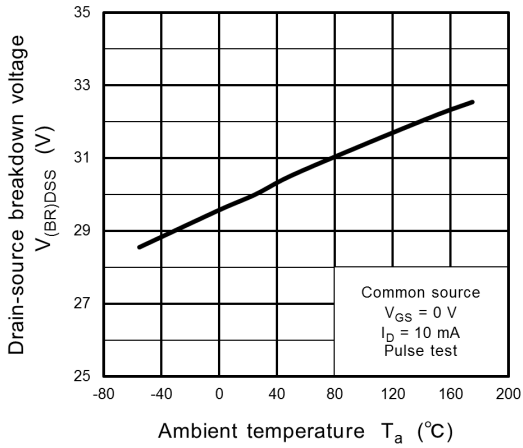
**Fig. 8.4  $V_{DS} - V_{GS}$**



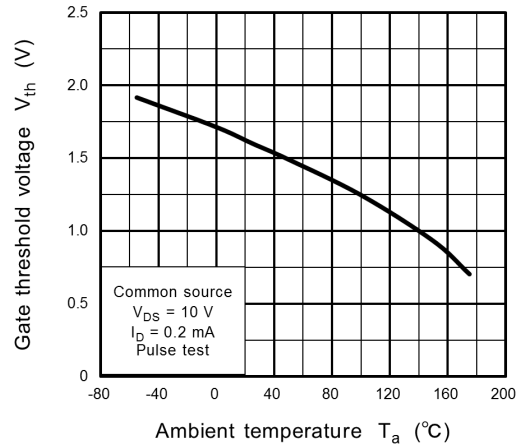
**Fig. 8.5  $R_{DS(ON)} - I_D$**



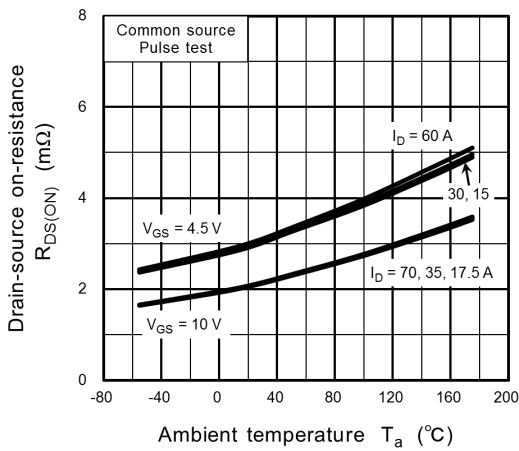
**Fig. 8.6  $I_{DR} - V_{DS}$**



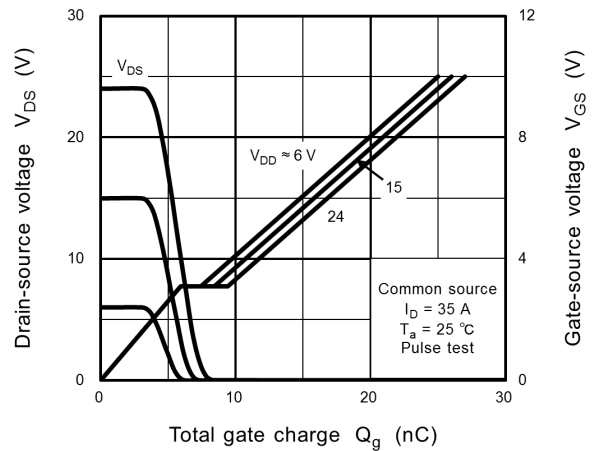
**Fig. 8.7  $V_{(BR)DSS} - T_a$**



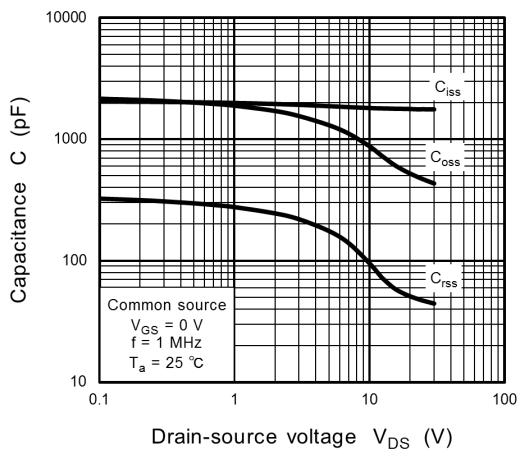
**Fig. 8.8  $V_{th} - T_a$**



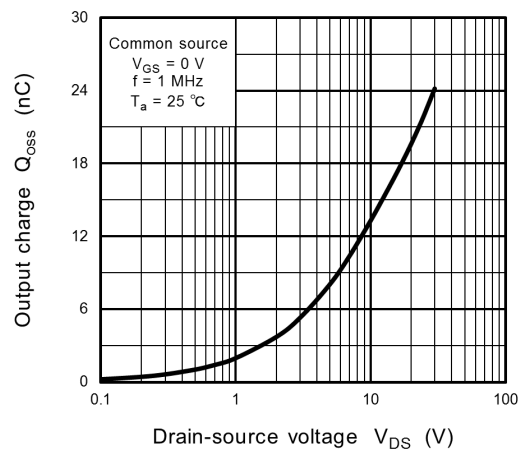
**Fig. 8.9  $R_{DS(ON)} - T_a$**



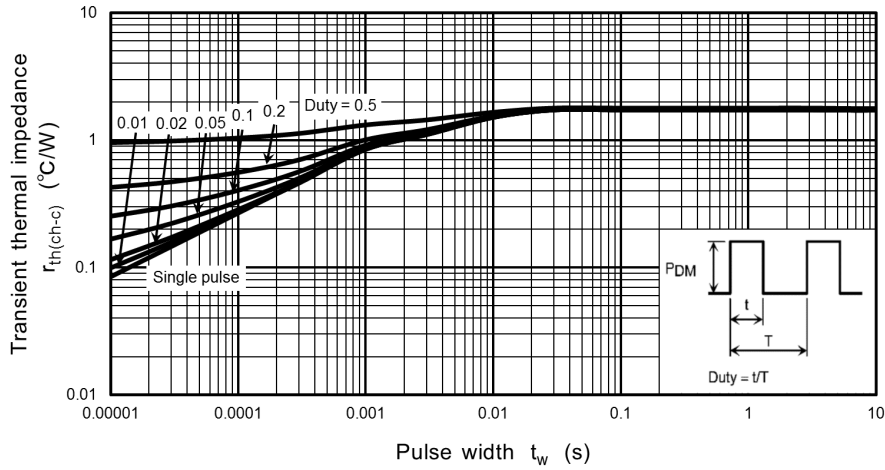
**Fig. 8.10 Dynamic Input/Output Characteristics**



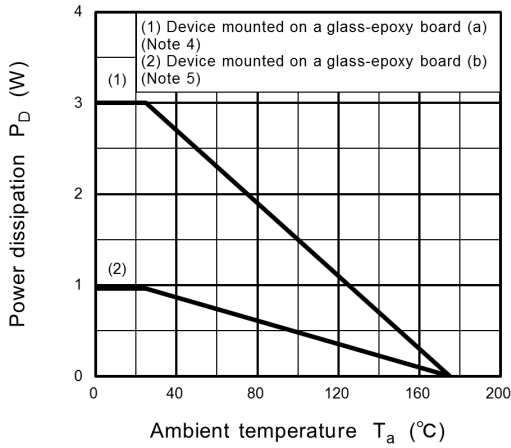
**Fig. 8.11 Capacitance -  $V_{DS}$**



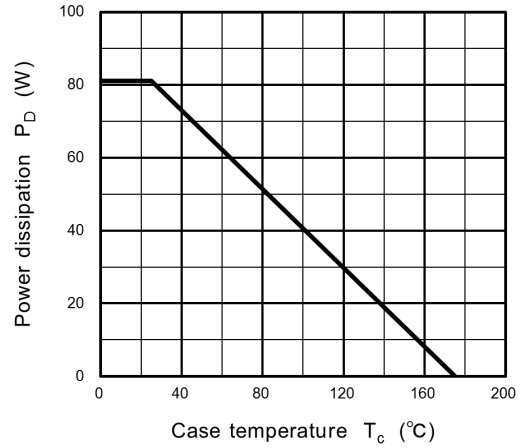
**Fig. 8.12  $Q_{oss} - V_{DS}$**



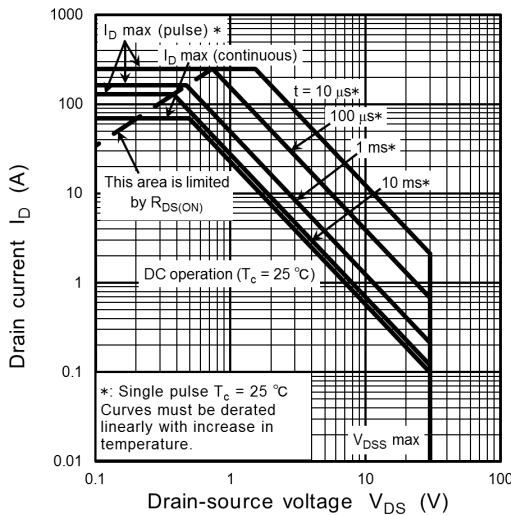
**Fig. 8.13  $r_{th} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.14  $P_D - T_a$**   
(Guaranteed Maximum)



**Fig. 8.15  $P_D - T_c$**   
(Guaranteed Maximum)



**Fig. 8.16 Safe Operating Area**  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.





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