



PN7462 family

NFC Cortex-M0 microcontroller

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406345

Product data sheet
COMPANY PUBLIC

1 General description

The PN7462 family is a family of 32-bit Arm Cortex-M0-based NFC microcontrollers offering high performance and low power consumption. It has a simple instruction set and memory addressing along with a reduced code size compared to existing architectures. PN7462 family offers an all in one solution, with features such as NFC, supporting all NFC Forum modes, microcontroller, optional contact smart card reader, and software in a single chip. It operates at CPU frequencies of up to 20 MHz.

Table 1. Comparison of the PN7462 family members

| | PN7462AUHN | PN7462AUEV | PN7412AUHN | PN7362AUHN | PN7362AUEV | PN7360AUHN | PN7360AUEV |
|---------------------------|---------------|-------------|---------------|-------------|-------------|-------------|-------------|
| Contact smart card reader | Class A, B, C | No | Class A, B, C | No | No | No | No |
| ISO/IEC 7816 UART | Yes | Yes | Yes | No | No | No | No |
| Contactless interface | Yes | Yes | No | Yes | Yes | Yes | Yes |
| Available Flash memory | 160 kB | 160 kB | 160 kB | 160 kB | 160 kB | 80 kB | 80 kB |
| SRAM data memory | 12 kB | 12 kB | 12 kB | 12 kB | 12 kB | 12 kB | 12 kB |
| General purposes I/O | 12 up-to 21 | 14 up-to 21 | 12 up-to 21 | 14 up-to 21 | 14 up-to 21 | 14 up-to 21 | 14 up-to 21 |
| Package type | HVQFN64 | VFBGA64 | HVQFN64 | HVQFN64 | VFBGA64 | HVQFN64 | VFBGA64 |

Having the differences listed in the table above, all products within the PN7462 family are equipped with 12 kB of SRAM data memory and 4 kB EEPROM. All products within the family also include one host interface with either high-speed mode I²C-bus, SPI, USB or high-speed UART, and two master interfaces, SPI and Fast-mode Plus I²C-bus. Four general-purpose counter/timers, a random number generator, one CRC coprocessor and up to 21 general-purpose I/O pins.

The PN7462 family NFC microcontroller offers a one chip solution to build contactless, or contact and contactless applications. It is equipped with a highly integrated high-power output NFC-IC for contactless communication at 13.56 MHz enabling EMV-compliance on RF level, without additional external active components.

By integrating a contact ISO/IEC 7816 interface on a single chip, the PN7462AUHN provides a solution for dual interface smart card readers. Whereas the PN7412AUHN offers a solution for a contact reader only. The PN7462AUHN and PN7412AUHN contact



interfaces offer a high level of security for the card by performing current limiting, short-circuit detection, ESD protection as well as supply supervision. On PN7462AUHN, PN7412AUHN and PN7462AUEV, an additional UART output is also implemented to address applications where more than one contact card slot is needed. It enables an easy connection to multiple smart card slot interfaces like TDA8026.

PN7462AUHN and PN7412AUHN provide thermal and short-circuit protection on all card contacts. It also provides automatic activation and deactivation sequences initiated by software or hardware.

2 Features and benefits

2.1 Integrated contact interface frontend

This chapter applies to the products with contact interface only.

- Class A, B, and C cards can work on 1.8 V, 3 V, and 5 V supply
- Specific ISO UART, variable baud rate through frequency or division ratio programming, error management at character level for T = 0, and extra guard time register
- DC-to-DC converter for class A support starting at 3 V, and class B support starting at 2.7 V
- Thermal and short-circuit protection on contact cards
- Automatic activation and deactivation sequence, initiated by software or by hardware in case of short-circuit, card removal, overheating, and V_{DD} or V_{DD} drop-out
- Enhanced ESD protection (> 12 kV)
- ISO/IEC 7816 compliant
- Compliance with EMV contact protocol specification
- Clock generation up to 13.56 MHz
- Synchronous card support
- Possibility to extend the number of contact interfaces, with the addition of slot extenders such as TDA8026

2.2 Integrated ISO/IEC 7816-3&4 UART interface

This chapter applies to the products with Integrated ISO/IEC 7816 UART interface only.

The PN7462 family offers the possibility to extend the number of contact interfaces available. It uses an I/O auxiliary interface to connect a slot extension (TDA8035 - 1 slot, TDA8020 - 2 slots, and TDA8026 - 5 slots).

- Class A (5 V), class B (3 V), and class C (1.8 V) smart card supply
- Protection of smart card
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7, and C8)
- Compliant with ISO/IEC 7816 and EMVCo standards

2.3 Integrated contactless interface frontend

This chapter applies to the products with integrated contactless interface only.

- High RF output power frontend IC for transfer speed up to 848 kbit/s
- NFC IP1 and NFC IP2 support
- Full NFC Forum tag support (type 1, type 2, type 3, type 4A, type 4B and type 5)
- P2P active and passive, target, and initiator
- Card emulation ISO14443 type A
- ISO/IEC 14443 type A and type B
- MIFARE products using Crypto 1
- ISO/IEC 15693, and ISO/IEC 18000-3 mode 3
- Low-power card detection
- Dynamic Power Control (DPC)

- Adaptive Wave Control (AWC)
- Adaptive Range Control (ARC)
- Compliance with EMV contactless protocol specification

2.4 Cortex-M0 microcontroller

- Processor core
 - Arm Cortex: 32-bit M0 processor
 - Built-in Nested Vectored Interrupt Controller (NVIC)
 - Non-maskable interrupt
 - 24-bit system tick timer
 - Running frequency of up to 20 MHz
 - Clock management to enable low power consumption
- Memory
 - Flash: 160 kB / 80 kB
 - SRAM: 12 kB
 - EEPROM: 4 kB
 - 40 kB boot ROM included, including USB mass storage primary boot loader for code download
- Debug option
 - Serial Wire Debug (SWD) interface
- Peripherals
 - *Host interface:*
 - USB 2.0 full speed with USB 3.0 hub connection capability
 - HSUART for serial communication, supporting standard speeds from 9600 bauds to 115200 bauds, and faster speed up to 1.288 Mbit/s
 - SPI with half-duplex and full duplex capability with speeds up to 7 Mbit/s
 - I²C supporting standard mode, fast mode, and high-speed mode with multiple address supports
 - *Master interface:*
 - SPI with half-duplex capability from 1 Mbit/s to 6.78 Mbit/s
 - I²C supporting standard mode, fast mode, fast mode plus, and clock stretching
- Up to 21 General-Purpose I/O (GPIO) with configurable pull-up/pull-down resistors
- GPIO1 to GPIO12 can be used as edge and level sensitive interrupt sources
- Power
 - Two reduced power modes: standby mode and hard power-down mode
 - Supports suspend mode for USB host interface
 - Processor wake-up from hard power-down mode, standby mode, suspend mode via host interface, GPIOs, RF field detection
 - Integrated PMU to adjust internal regulators automatically, to minimize the power consumption during all possible power modes
 - Power-on reset
 - RF supply: external, or using an integrated LDO (TX LDO, configurable with 3 V, 3.3 V, 3.6 V, 4.5 V, and 4.75 V)
 - Pad voltage supply: external 3.3 V or 1.8 V, or using an integrated LDO (3.3 V supply)
- Timers
 - Four general-purpose timers

- Programmable Watchdog Timer (WDT)
- CRC coprocessor
- Random number generator
- Clocks
 - Crystal oscillator at 27.12 MHz
 - Dedicated PLL at 48 MHz for the USB
 - Integrated HFO 20 MHz and LFO 365 kHz
- General
 - HVQFN64 package
 - VFBGA64 package
 - Temperature range: -40 °C to +85 °C

3 Applications

- Physical access control
- Gaming
- USB NFC reader, including dual interface smart card readers
- Home banking, payment readers EMVCo compliant
- High integration devices
- NFC applications

4 Quick reference data

Table 2. Quick reference data

Operating range: -40 °C to +85 °C unless specified; contact interface: $V_{DDP(VBUSP)} = V_{DDP(VBUS)}$; contactless interface: internal LDO not used

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|----------------------------------|---|------|-----|------|------|
| $V_{DDP(VBUS)}$ | power supply voltage on pin VBUS | card emulation, passive target (PLM) | 2.3 | - | 5.5 | V |
| | | all RF modes; class B and class C contact interface support | 2.7 | - | 5.5 | V |
| | | all RF modes; class A, class B and class C contact interface support | 3 | - | 5.5 | V |
| $V_{DD(PVDD)}$ | PVDD supply voltage | 1.8 V | 1.65 | 1.8 | 1.95 | V |
| | | 3.3 V | 3 | 3.3 | 3.6 | V |
| $I_{DDP(VBUS)}$ | power supply current on pin VBUS | in hard power-down mode; T = 25 °C; $V_{DDP(VBUS)} = 5.5$ V; RST_N = 0 | - | 12 | 18 | μA |
| | | stand by mode; T = 25 °C; $V_{DDP(VBUS)} = 3.3$ V; external PVDD LDO used | - | 18 | - | μA |
| | | stand by mode; T = 25 °C; $V_{DDP(VBUS)} = 5.5$ V; internal PVDD LDO used | - | 55 | - | μA |
| | | suspend mode, USB interface; $V_{DDP(VBUS)} = 5.5$ V; external PVDD supply; T = 25 °C | - | 120 | 250 | μA |
| $I_{DD(TVDD)}$ | TVDD supply current | on pin TVDD_IN; maximum supported operating current by the contactless interface | - | - | 250 | mA |
| P_{max} | maximum power dissipation | | - | - | 1050 | mW |
| T_{amb} | ambient temperature | JEDEC PCB | -40 | - | +85 | °C |

5 Ordering information

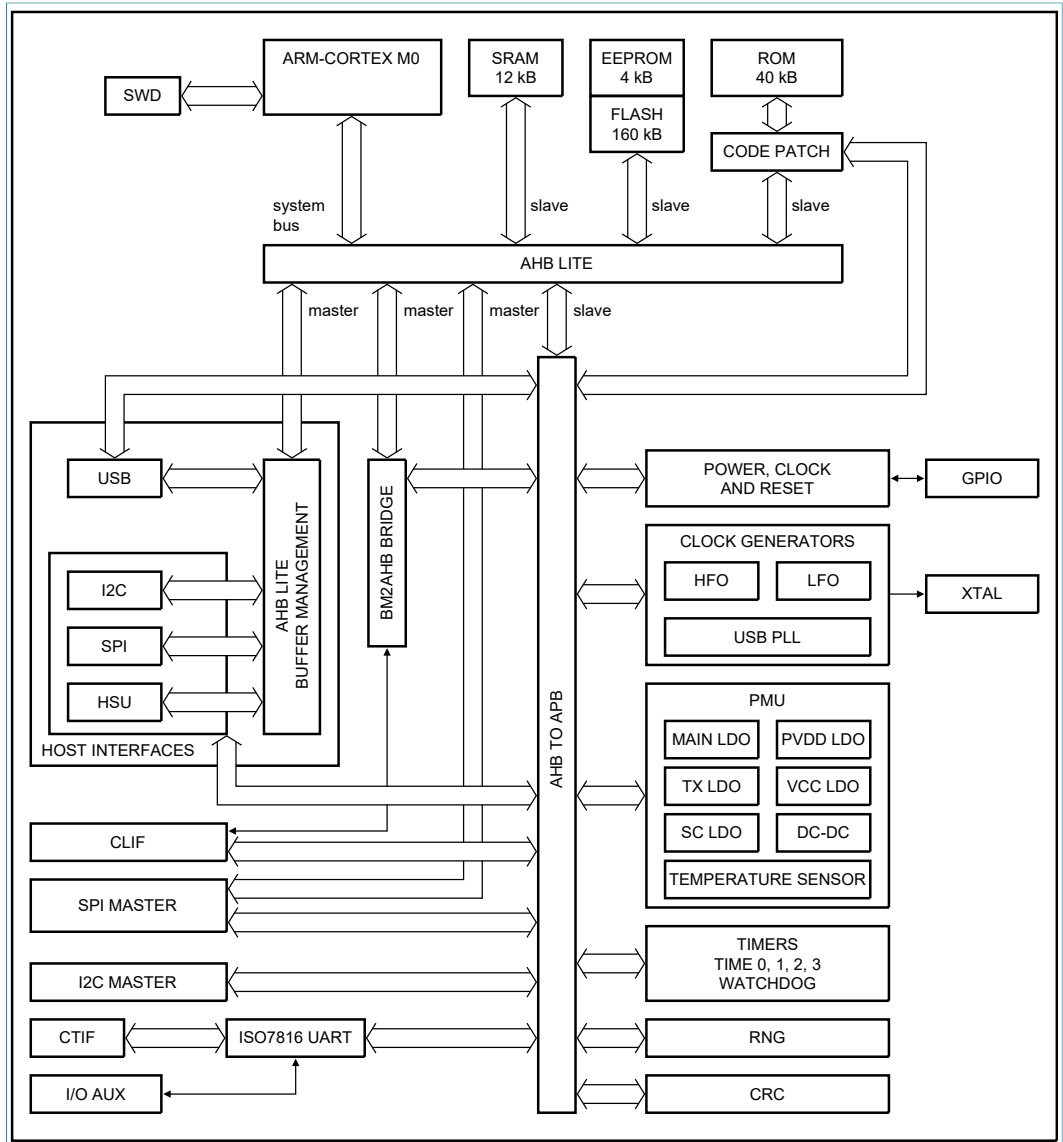
The table below lists the ordering information of the PN7462 family.

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|---|-----------|
| | Name | Description | Version |
| PN7462AUHN | HVQFN64 | 160 kB memory; contact interface; ISO/IEC 7816-3&4 UART interface; plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm | SOT804-4 |
| PN7462AUEV | VFBGA64 | 160 kB memory; no contact interface; ISO/IEC 7816-3&4 UART interface; plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm | SOT1307-2 |
| PN7412AUHN | HVQFN64 | 160 kB memory; contact interface; ISO/IEC 7816-3&4 UART interface; no contactless interface plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm | SOT804-4 |
| PN7362AUHN | HVQFN64 | 160 kB memory; no contact interface; no ISO/IEC 7816-3&4 UART interface; plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm | SOT804-4 |
| PN7362AUEV | VFBGA64 | 160 kB memory; no contact interface; no ISO/IEC 7816-3&4 UART interface; plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm | SOT1307-2 |
| PN7360AUHN | HVQFN64 | 80 kB memory; no contact interface; no ISO/IEC 7816-3&4 UART interface; plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm | SOT804-4 |
| PN7360AUEV | VFBGA64 | 80 kB memory; no contact interface; no ISO/IEC 7816-3&4 UART interface; plastic very thin fine-pitch ball grid array package; 64 balls; 4.5 mm x 4.5 mm x 0.80 mm | SOT1307-2 |

6 Block diagram

6.1 Block diagram PN7462 HVQFN64



aaa-021334

Figure 1. Block diagram

6.2 Block diagram PN7462 VFBGA64

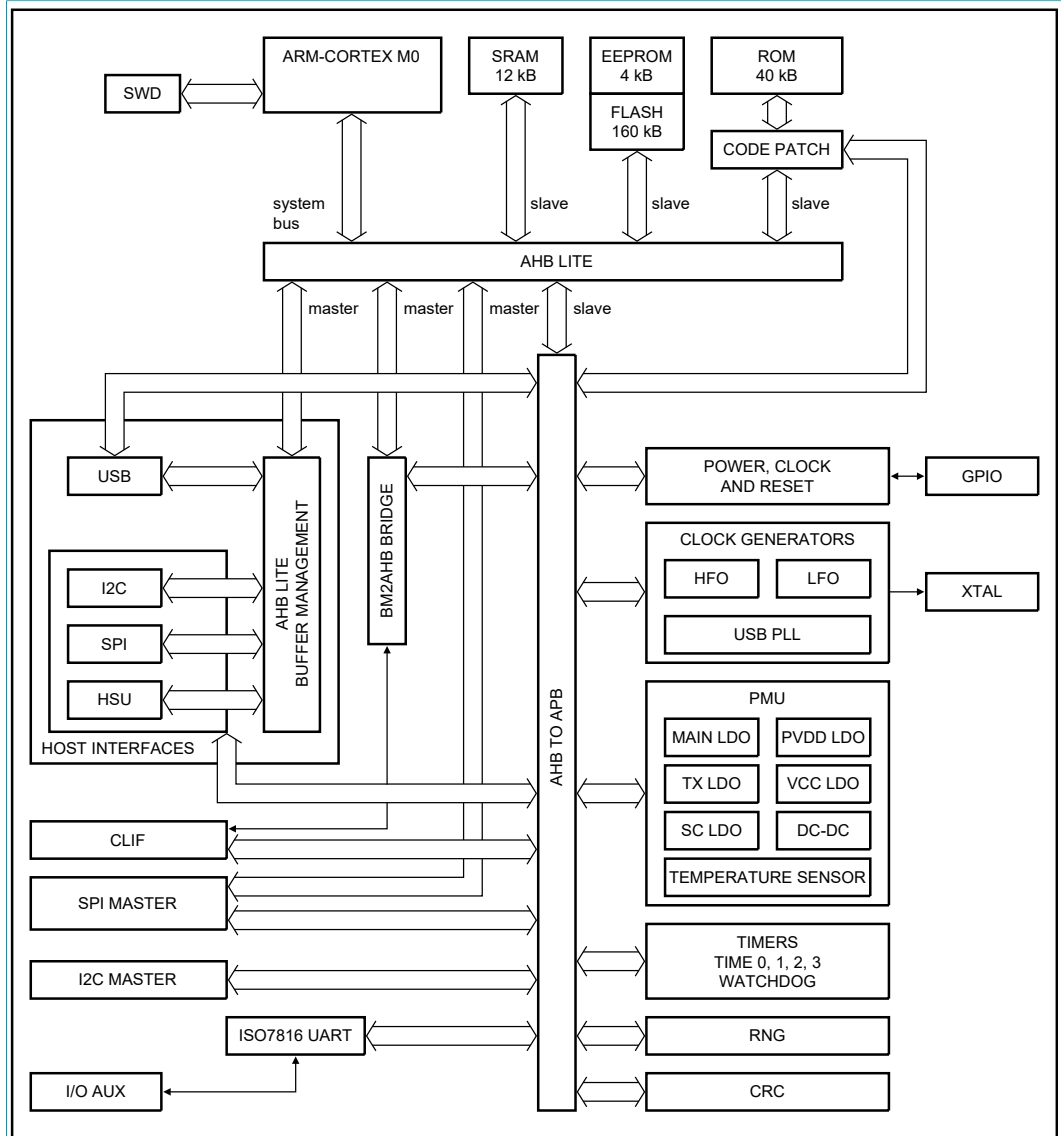
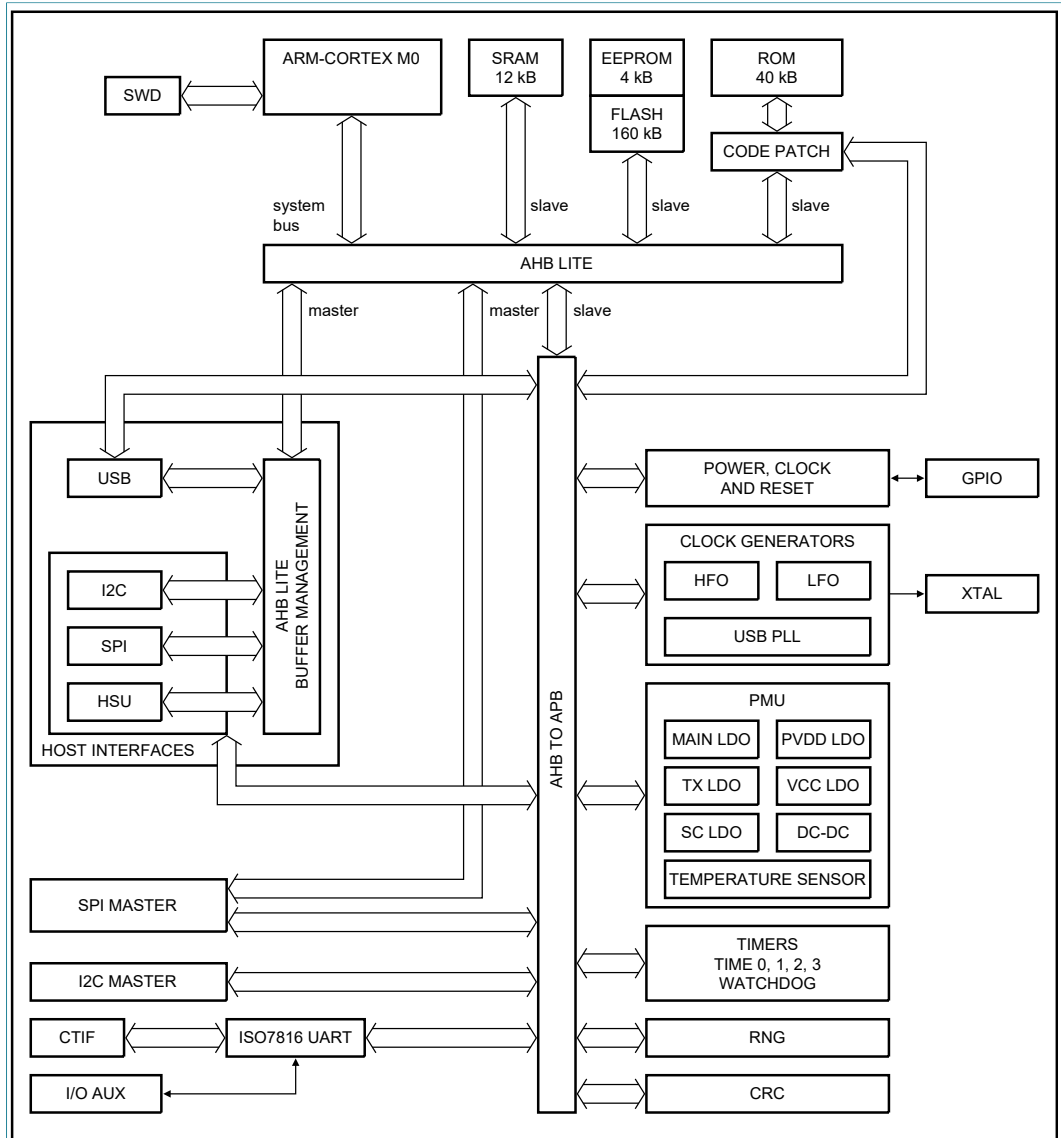


Figure 2. Block diagram

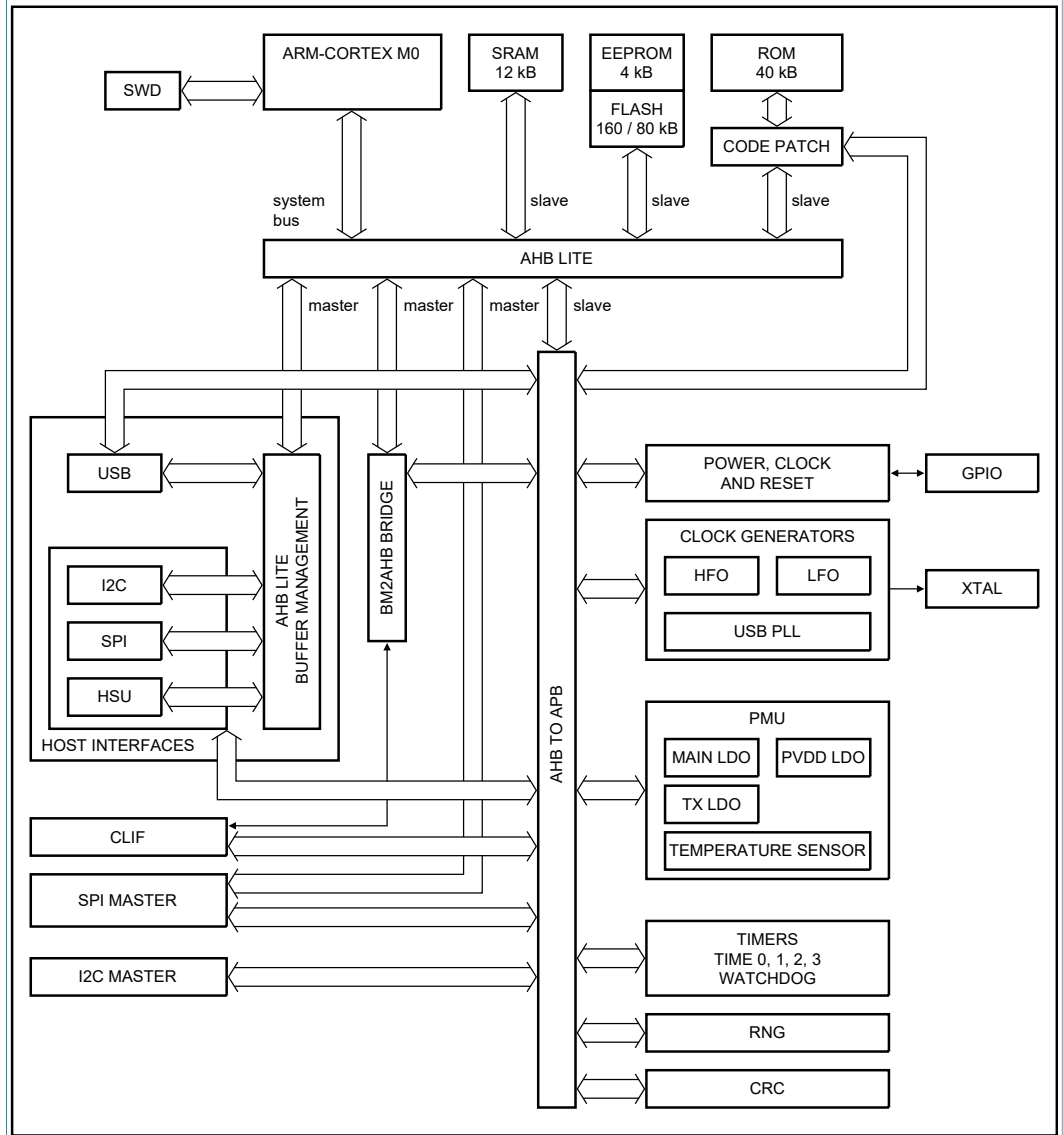
6.3 Block diagram PN7412 HVQFN64



aaa-030118

Figure 3. Block diagram

6.4 Block diagram PN736X



aaa-025625

Figure 4. Block diagram

7 Pinning information

7.1 Pinning HVQFN64

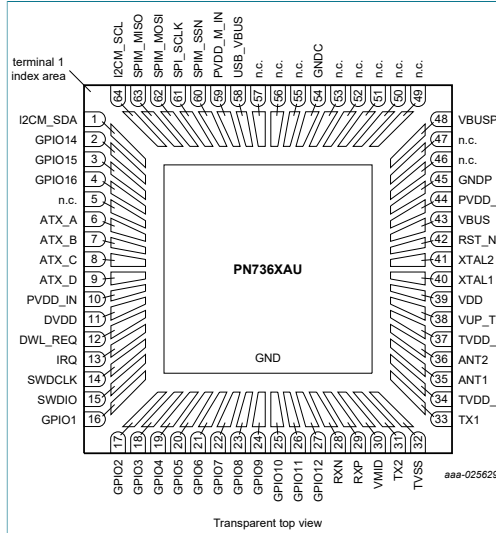


Figure 5. Pin configuration PN736X

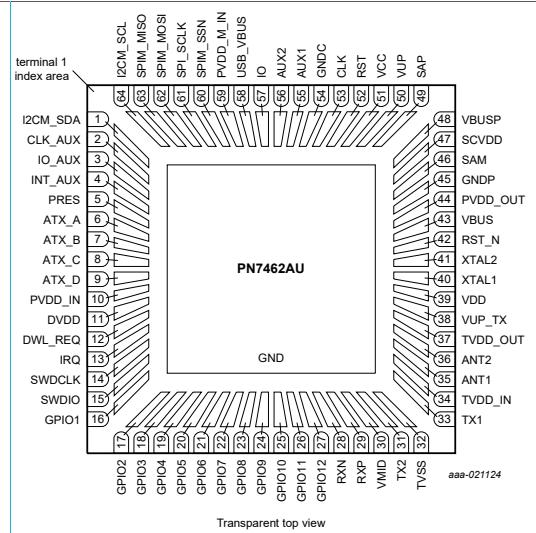


Figure 6. Pin configuration PN7462

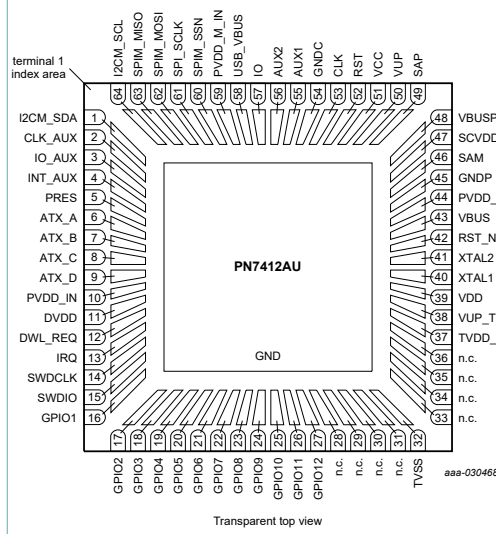


Figure 7. Pin configuration PN7412

Important note: the inner leads below the package are internally connected to the PIN. Special care needs to be taken during the design so that no conductive part is present under these PINS, which could cause short cuts.

7.2 Pin description HVQFN64

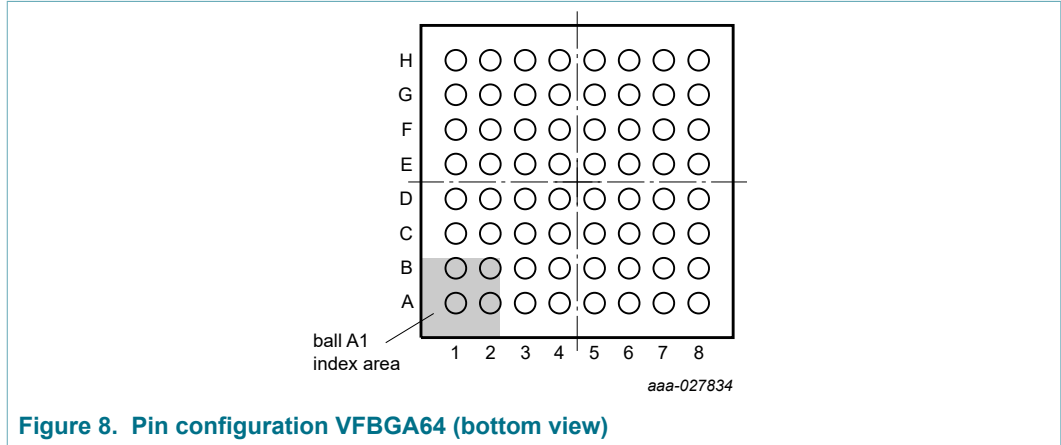
Table 4. Pin description

| Pin | Symbol PN736X | Description PN736X | Symbol PN7462 | Description PN7462 | Symbol PN7412 | Description PN7412 |
|-----|------------------|--|------------------|--|------------------|--|
| 1 | I2CM_ SDA | I ² C-bus serial data I/O master/GPIO13 | I2CM_ SDA | I ² C-bus serial data I/O master/GPIO13 | I2CM_ SDA | I ² C-bus serial data I/O master/GPIO13 |
| 2 | CLK_ AUX | GPIO14 | CLK_ AUX | auxiliary card contact clock/ GPIO14 | CLK_ AUX | auxiliary card contact clock/ GPIO14 |
| 3 | IO_AUX | GPIO15 | IO_AUX | auxiliary card contact I/O/ GPIO15 | IO_AUX | auxiliary card contact I/O/ GPIO15 |
| 4 | INT_ AUX | GPIO16 | INT_ AUX | auxiliary card contact interrupt/GPIO16 | INT_ AUX | auxiliary card contact interrupt/GPIO16 |
| 5 | n.c. | not connected | PRES | card presence | PRES | card presence |
| 6 | ATX_A | SPI slave select input (NSS_S)/I ² C-bus serial clock input (SCL_S)/ HSUART RX | ATX_A | SPI slave select input (NSS_S)/I ² C-bus serial clock input (SCL_S)/ HSUART RX | ATX_A | SPI slave select input (NSS_S)/I ² C-bus serial clock input (SCL_S)/ HSUART RX |
| 7 | ATX_B | SPI slave data input (MOSI_S)/I ² C-bus serial data I/O (SDA_S)/HSUART TX | ATX_B | SPI slave data input (MOSI_S)/I ² C-bus serial data I/O (SDA_S)/HSUART TX | ATX_B | SPI slave data input (MOSI_S)/I ² C-bus serial data I/O (SDA_S)/HSUART TX |
| 8 | ATX_C | USB D+/SPI slave data output (MISO_S)/I ² C-bus address bit0 input/HSUART RTS | ATX_C | USB D+/SPI slave data output (MISO_S)/I ² C-bus address bit0 input/HSUART RTS | ATX_C | USB D+/SPI slave data output (MISO_S)/I ² C-bus address bit0 input/HSUART RTS |
| 9 | ATX_D | USB D-/SPI clock input (SCK_S)/I ² C-bus address bit1 input/HSUART CTS | ATX_D | USB D-/SPI clock input (SCK_S)/I ² C-bus address bit1 input/HSUART CTS | ATX_D | USB D-/SPI clock input (SCK_S)/I ² C-bus address bit1 input/HSUART CTS |
| 10 | PVDD_ IN | pad supply voltage input | PVDD_ IN | pad supply voltage input | PVDD_ IN | pad supply voltage input |
| 11 | DVDD | digital core logic supply voltage input | DVDD | digital core logic supply voltage input | DVDD | digital core logic supply voltage input |
| 12 | DWL_ REQ | entering in download mode | DWL_ REQ | entering in download mode | DWL_ REQ | entering in download mode |
| 13 | IRQ | interrupt request output | IRQ | interrupt request output | IRQ | interrupt request output |
| 14 | SWDC LK | SW serial debug line clock | SWDC LK | SW serial debug line clock | SWDC LK | SW serial debug line clock |
| 15 | SWDIO | SW serial debug line input/ output | SWDIO | SW serial debug line input/ output | SWDIO | SW serial debug line input/ output |
| 16 | GPIO1 | general-purpose I/O/SPI master select2 output | GPIO1 | general-purpose I/O/SPI master select2 output | GPIO1 | general-purpose I/O/SPI master select2 output |
| 17 | GPIO2 | general-purpose I/O | GPIO2 | general-purpose I/O | GPIO2 | general-purpose I/O |
| 18 | GPIO3 | general-purpose I/O | GPIO3 | general-purpose I/O | GPIO3 | general-purpose I/O |
| 19 | GPIO4 | general-purpose I/O | GPIO4 | general-purpose I/O | GPIO4 | general-purpose I/O |
| 20 | GPIO5 | general-purpose I/O | GPIO5 | general-purpose I/O | GPIO5 | general-purpose I/O |
| 21 | GPIO6 | general-purpose I/O | GPIO6 | general-purpose I/O | GPIO6 | general-purpose I/O |

| Pin | Symbol PN736X | Description PN736X | Symbol PN7462 | Description PN7462 | Symbol PN7412 | Description PN7412 |
|-----|------------------|---|------------------|---|------------------|--|
| 22 | GPIO7 | general-purpose I/O | GPIO7 | general-purpose I/O | GPIO7 | general-purpose I/O |
| 23 | GPIO8 | general-purpose I/O | GPIO8 | general-purpose I/O | GPIO8 | general-purpose I/O |
| 24 | GPIO9 | general-purpose I/O | GPIO9 | general-purpose I/O | GPIO9 | general-purpose I/O |
| 25 | GPIO10 | general-purpose I/O | GPIO10 | general-purpose I/O | GPIO10 | general-purpose I/O |
| 26 | GPIO11 | general-purpose I/O | GPIO11 | general-purpose I/O | GPIO11 | general-purpose I/O |
| 27 | GPIO12 | general-purpose I/O | GPIO12 | general-purpose I/O | GPIO12 | general-purpose I/O |
| 28 | RXN | receiver input | RXN | receiver input | n.c. | See UM10858 for connection details |
| 29 | RXP | receiver input | RXP | receiver input | n.c. | See UM10858 for connection details |
| 30 | VMID | receiver reference voltage input | VMID | receiver reference voltage input | n.c. | See UM10858 for connection details |
| 31 | TX2 | antenna driver output | TX2 | antenna driver output | n.c. | keep unconnected |
| 32 | TVSS | ground for antenna power supply | TVSS | ground for antenna power supply | TVSS | ground for antenna power supply |
| 33 | TX1 | antenna driver output | TX1 | antenna driver output | n.c. | keep unconnected |
| 34 | TVDD_ IN | antenna driver supply voltage input | TVDD_ IN | antenna driver supply voltage input | n.c. | Connect to GND |
| 35 | ANT1 | antenna connection for load modulation in card emulation and P2P passive target modes | ANT1 | antenna connection for load modulation in card emulation and P2P passive target modes | n.c. | See UM10858 for connection details |
| 36 | ANT2 | antenna connection for load modulation in card emulation and P2P passive target modes | ANT2 | antenna connection for load modulation in card emulation and P2P passive target modes | n.c. | See UM10858 for connection details |
| 37 | TVDD_ OUT | antenna driver supply, output of TX_LDO | TVDD_ OUT | antenna driver supply, output of TX_LDO | TVDD_ OUT | antenna driver supply, output of TX_LDO |
| 38 | VUP_ TX | supply of the contactless TX_LDO | VUP_ TX | supply of the contactless TX_LDO | VUP_ TX | supply of the contactless TX_LDO |
| 39 | VDD | 1.8 V regulator output for digital blocks | VDD | 1.8 V regulator output for digital blocks | VDD | 1.8 V regulator output for digital blocks |
| 40 | XTAL1 | 27.12 MHz clock input for crystal | XTAL1 | 27.12 MHz clock input for crystal | XTAL1 | 27.12 MHz clock input for crystal |
| 41 | XTAL2 | 27.12 MHz clock input for crystal | XTAL2 | 27.12 MHz clock input for crystal | XTAL2 | 27.12 MHz clock input for crystal |
| 42 | RST_N | reset pin | RST_N | reset pin | RST_N | reset pin |
| 43 | VBUS | main supply voltage input of microcontroller | VBUS | main supply voltage input of microcontroller | VBUS | main supply voltage input of microcontroller |
| 44 | PVDD_ OUT | output of PVDD_LDO for pad voltage supply | PVDD_ OUT | output of PVDD_LDO for pad voltage supply | PVDD_ OUT | output of PVDD_LDO for pad voltage supply |
| 45 | GNDP | Ground | GNDP | Ground | GNDP | Ground |

| Pin | Symbol PN736X | Description PN736X | Symbol PN7462 | Description PN7462 | Symbol PN7412 | Description PN7412 |
|---------|---------------|---|---------------|---|---------------|---|
| 46 | n.c. | not connected | SAM | DC-to-DC converter connection | SAM | DC-to-DC converter connection |
| 47 | n.c. | not connected | SCVDD | input LDO for DC-to-DC converter | SCVDD | input LDO for DC-to-DC converter |
| 48 | VBUSP | Connected to VBUS | VBUSP | main supply for the contact interface | VBUSP | main supply for the contact interface |
| 49 | n.c. | not connected | SAP | DC-to-DC converter connection | SAP | DC-to-DC converter connection |
| 50 | n.c. | not connected | VUP | reserved; connected to GND through a decoupling capacitance | VUP | reserved; connected to GND through a decoupling capacitance |
| 51 | n.c. | not connected | VCC | card supply output of contact interface | VCC | card supply output of contact interface |
| 52 | n.c. | not connected | RST | reset pin of contact interface | RST | reset pin of contact interface |
| 53 | n.c. | not connected | CLK | clock pin of contact interface | CLK | clock pin of contact interface |
| 54 | GNDC | connected to the ground | GNDC | connected to the ground | GNDC | connected to the ground |
| 55 | n.c. | not connected | AUX1 | C4 card I/O pin of contact interface | AUX1 | C4 card I/O pin of contact interface |
| 56 | n.c. | not connected | AUX2 | C8 card I/O pin of contact interface | AUX2 | C8 card I/O pin of contact interface |
| 57 | n.c. | not connected | IO | card I/O | IO | card I/O |
| 58 | USB_VBUS | used for USB VBUS detection | USB_VBUS | used for USB VBUS detection | USB_VBUS | used for USB VBUS detection |
| 59 | PVDD_M_IN | pad supply voltage input for master interfaces | PVDD_M_IN | pad supply voltage input for master interfaces | PVDD_M_IN | pad supply voltage input for master interfaces |
| 60 | SPIM_SSN | SPI master select 1 output/ GPIO17 | SPIM_SSN | SPI master select 1 output/ GPIO17 | SPIM_SSN | SPI master select 1 output/ GPIO17 |
| 61 | SPI_SCLK | SPI master clock output/ GPIO18 | SPI_SCLK | SPI master clock output/ GPIO18 | SPI_SCLK | SPI master clock output/ GPIO18 |
| 62 | SPIM_MOSI | SPI master data output/ GPIO19 | SPIM_MOSI | SPI master data output/ GPIO19 | SPIM_MOSI | SPI master data output/ GPIO19 |
| 63 | SPIM_MISO | SPI master data input/ GPIO20 | SPIM_MISO | SPI master data input/ GPIO20 | SPIM_MISO | SPI master data input/ GPIO20 |
| 64 | I2CM_SCL | I ² C-bus serial clock output master/ GPIO21 | I2CM_SCL | I ² C-bus serial clock output master/ GPIO21 | I2CM_SCL | I ² C-bus serial clock output master/ GPIO21 |
| Die pad | GND | Ground | GND | Ground | GND | Ground |

7.3 Pinning VFBGA64



7.4 Pin description VFBGA64

Table 5. Pin description

| Pin | Symbol PN736X | Description PN736X | Symbol PN7462 | Description PN7462 |
|-----|---------------|--|---------------|--|
| A1 | I2CM_SDA | I ² C-bus serial data I/O master/GPIO13 | I2CM_SDA | I ² C-bus serial data I/O master/GPIO13 |
| A2 | SPIM_MISO | SPI master data input/GPIO20 | SPIM_MISO | SPI master data input/GPIO20 |
| A3 | PVDD_M_IN | pad supply voltage input for master interfaces | PVDD_M_IN | pad supply voltage input for master interfaces |
| A4 | VBUSP | Connected to VBUS | VBUSP | Connected to VBUS |
| A5 | VBUS | main supply voltage input of microcontroller | VBUS | main supply voltage input of microcontroller |
| A6 | PVSS | Pad ground | PVSS | Pad ground |
| A7 | PVDD_OUT | output of PVDD_LDO for pad voltage supply | PVDD_OUT | output of PVDD_LDO for pad voltage supply |
| A8 | XTAL2 | 27.12 MHz clock input for crystal | XTAL2 | 27.12 MHz clock input for crystal |
| B1 | INT_AUX | GPIO16 | INT_AUX | auxiliary card contact interrupt/GPIO16 |
| B2 | ATX_A | SPI slave select input (NSS_S)/I ² C-bus serial clock input (SCL_S)/HSUART RX | ATX_A | SPI slave select input (NSS_S)/I ² C-bus serial clock input (SCL_S)/HSUART RX |
| B3 | SPIM_MOSI | SPI master data output/GPIO19 | SPIM_MOSI | SPI master data output/GPIO19 |
| B4 | SPIM_SSN | SPI master select 1 output/GPIO17 | SPIM_SSN | SPI master select 1 output/GPIO17 |
| B5 | USB_VBUS | used for USB VBUS detection | USB_VBUS | used for USB VBUS detection |
| B6 | PVSS | Pad ground | PVSS | Pad ground |
| B7 | PVSS | Pad ground | PVSS | Pad ground |
| B8 | XTAL1 | 27.12 MHz clock input for crystal | XTAL1 | 27.12 MHz clock input for crystal |
| C1 | CLK_AUX | GPIO14 | CLK_AUX | auxiliary card contact clock/GPIO14 |
| C2 | ATX_B | SPI slave data input (MOSI_S)/I ² C-bus serial data I/O (SDA_S)/HSUART TX | ATX_B | SPI slave data input (MOSI_S)/I ² C-bus serial data I/O (SDA_S)/HSUART TX |

| Pin | Symbol PN736X | Description PN736X | Symbol PN7462 | Description PN7462 |
|-----|------------------|---|------------------|---|
| C3 | I2CM_SCL | I ² C-bus serial clock output master/ GPIO21 | I2CM_SCL | I ² C-bus serial clock output master/ GPIO21 |
| C4 | SPI_SCLK | SPI master clock output/GPIO18 | SPI_SCLK | SPI master clock output/GPIO18 |
| C5 | DVSS | Digital ground | DVSS | Digital ground |
| C6 | PVSS | Pad ground | PVSS | Pad ground |
| C7 | RST_N | reset pin | RST_N | reset pin |
| C8 | VDD | 1.8 V regulator output for digital blocks | VDD | 1.8 V regulator output for digital blocks |
| D1 | PVDD_IN | pad supply voltage input | PVDD_IN | pad supply voltage input |
| D2 | ATX_C | USB D+/SPI slave data output (MISO_S)/I ² C-bus address bit0 input/ HSUART RTS | ATX_C | USB D+/SPI slave data output (MISO_S)/I ² C-bus address bit0 input/ HSUART RTS |
| D3 | IRQ | interrupt request output | IRQ | interrupt request output |
| D4 | IO_AUX | GPIO15 | IO_AUX | auxiliary card contact I/O/GPIO15 |
| D5 | DVSS | Digital ground | DVSS | Digital ground |
| D6 | PVSS | Pad ground | PVSS | Pad ground |
| D7 | PVSS | Pad ground | PVSS | Pad ground |
| D8 | VUP_TX | supply of the contactless TX_LDO | VUP_TX | supply of the contactless TX_LDO |
| E1 | DVDD | digital core logic supply voltage input | DVDD | digital core logic supply voltage input |
| E2 | ATX_D | USB D-/SPI clock input (SCK_S)/I ² C-bus address bit1 input/HSUART CTS | ATX_D | USB D-/SPI clock input (SCK_S)/I ² C-bus address bit1 input/HSUART CTS |
| E3 | GPIO1 | general-purpose I/O/SPI master select2 output | GPIO1 | general-purpose I/O/SPI master select2 output |
| E4 | GPIO5 | general-purpose I/O | GPIO5 | general-purpose I/O |
| E5 | DVSS | Digital ground | DVSS | Digital ground |
| E6 | AVSS | Analog ground | AVSS | Analog ground |
| E7 | ANT2 | antenna connection for load modulation in card emulation and P2P passive target modes | ANT2 | antenna connection for load modulation in card emulation and P2P passive target modes |
| E8 | TVDD_OUT | antenna driver supply, output of TX_LDO | TVDD_OUT | antenna driver supply, output of TX_LDO |
| F1 | DWL_REQ | entering in download mode | DWL_REQ | entering in download mode |
| F2 | SWDIO | SW serial debug line input/output | SWDIO | SW serial debug line input/output |
| F3 | GPIO6 | general-purpose I/O | GPIO6 | general-purpose I/O |
| F4 | GPIO9 | general-purpose I/O | GPIO9 | general-purpose I/O |
| F5 | GPIO12 | general-purpose I/O | GPIO12 | general-purpose I/O |
| F6 | AVSS | Analog ground | AVSS | Analog ground |
| F7 | ANT1 | antenna connection for load modulation in card emulation and P2P passive target modes | ANT1 | antenna connection for load modulation in card emulation and P2P passive target modes |
| F8 | TVDD_IN | antenna driver supply voltage input | TVDD_IN | antenna driver supply voltage input |

| Pin | Symbol PN736X | Description PN736X | Symbol PN7462 | Description PN7462 |
|-----|------------------|----------------------------------|------------------|----------------------------------|
| G1 | SWDCLK | SW serial debug line clock | SWDCLK | SW serial debug line clock |
| G2 | GPIO4 | general-purpose I/O | GPIO4 | general-purpose I/O |
| G3 | GPIO7 | general-purpose I/O | GPIO7 | general-purpose I/O |
| G4 | GPIO8 | general-purpose I/O | GPIO8 | general-purpose I/O |
| G5 | GPIO10 | general-purpose I/O | GPIO10 | general-purpose I/O |
| G6 | GPIO11 | general-purpose I/O | GPIO11 | general-purpose I/O |
| G7 | AVSS | Analog ground | AVSS | Analog ground |
| G8 | TX1 | antenna driver output | TX1 | antenna driver output |
| H1 | GPIO3 | general-purpose I/O | GPIO3 | general-purpose I/O |
| H2 | GPIO2 | general-purpose I/O | GPIO2 | general-purpose I/O |
| H3 | VMID | receiver reference voltage input | VMID | receiver reference voltage input |
| H4 | RXN | receiver input | RXN | receiver input |
| H5 | RXP | receiver input | RXP | receiver input |
| H6 | TVSS | Antenna driver ground | TVSS | Antenna driver ground |
| H7 | TX2 | antenna driver output | TX2 | antenna driver output |
| H8 | TVSS | Antenna driver ground | TVSS | Antenna driver ground |

8 Functional description

8.1 Arm Cortex-M0 microcontroller

The PN7462 family is an Arm Cortex-M0-based 32-bit microcontroller, optimized for low-cost designs, high energy efficiency, and simple instruction set.

The CPU operates on an internal clock, which can be configured to provide frequencies such as 20 MHz, 10 MHz, and 5 MHz.

The peripheral complement of the PN7462 family includes a 160 kB flash memory, a 12 kB SRAM, and a 4 kB EEPROM. It also includes one configurable host interface (Fast-mode Plus and high-speed I²C, SPI, HSUART, and USB), two master interfaces (Fast-mode Plus I²C, SPI), 4 timers, 12 general-purpose I/O pins, one ISO/IEC 7816 contact card interface (PN7462AUHN only), one ISO/IEC 7816-3&4 UART (PN7462AUHN and PN7462AUEV only) and one 13.56 MHz NFC interface.

8.2 Memories

8.2.1 On-chip flash programming memory

The PN7462 family contains 160 / 80 kB on-chip flash program memory depending on the version. The flash can be programmed using In-System Programming (ISP) or In-Application Programming (IAP) via the on-chip boot loader software.

The flash memory is divided into two instances of 80 kB each, with each sector consisting of individual pages of 64 bytes.

8.2.1.1 Memory mapping

The flash memory mapping is described in [Figure 9](#).

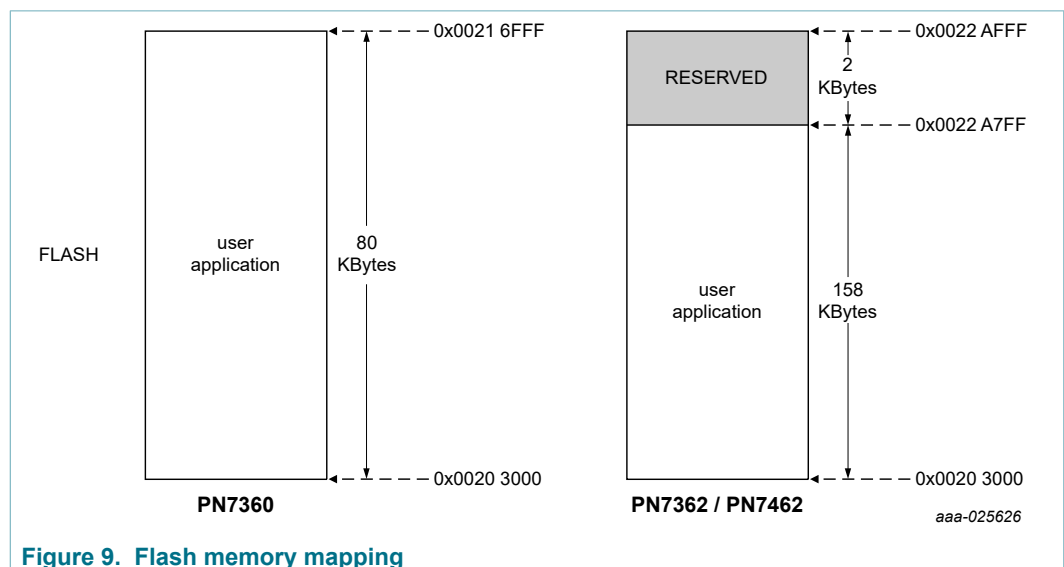


Figure 9. Flash memory mapping

8.2.2 EEPROM

The PN7462 family embeds 4 kB of on-chip byte-erasable and byte-programmable EEPROM data memory.

The EEPROM can be programmed using In-System Programming (ISP).

8.2.2.1 Memory mapping

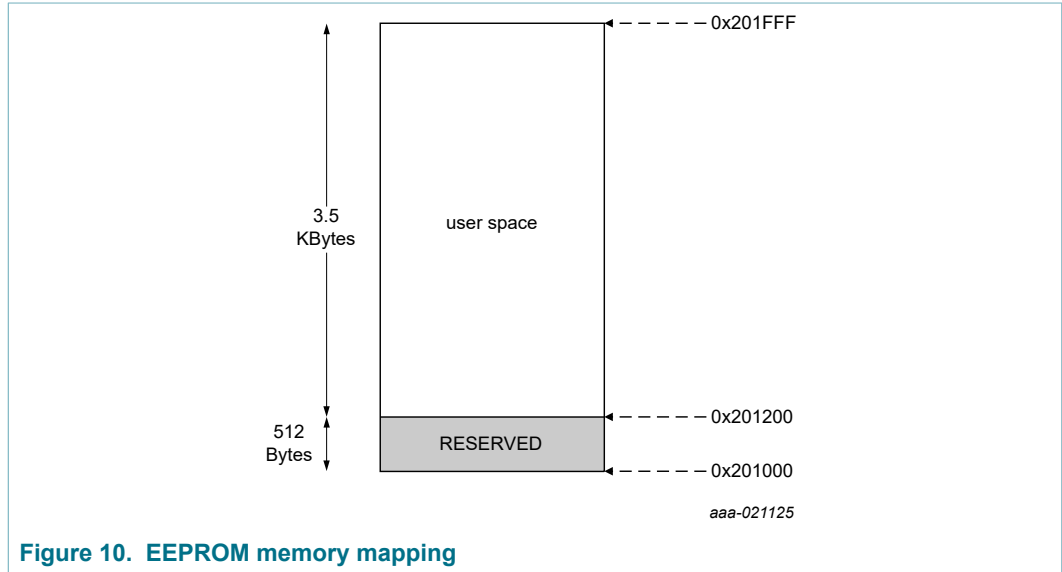


Figure 10. EEPROM memory mapping

8.2.3 SRAM

The PN7462 family contains a total of 12 kB on-chip static RAM memory.

8.2.3.1 Memory mapping

The SRAM memory mapping is shown in [Figure 11](#).

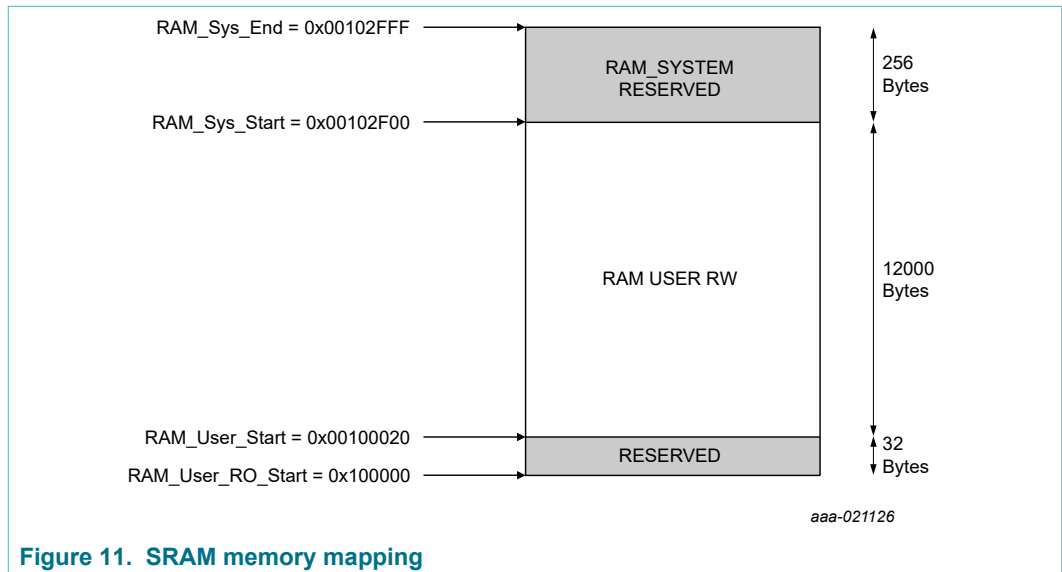


Figure 11. SRAM memory mapping

8.2.4 ROM

The PN7462 family contains 40 kB of on-chip ROM memory. The on-chip ROM contains boot loader, USB mass storage primary download, and the following Application Programming Interfaces (APIs):

- In-Application Programming (IAP) support for flash
- Lifecycle management of debug interface, code write protection of flash memory and USB mass storage primary download
- USB descriptor configuration
- Configuration of timeout and source of pad supply

8.2.5 Memory map

The PN7462 family incorporates several distinct memory regions. [Figure 12](#) shows the memory map, from the user program perspective, following reset.

The APB peripheral area is 512 kB in size, and is divided to allow up to 32 peripherals. Only peripherals from 0 to 15 are accessible. Each peripheral allocates 16 kB, which simplifies the address decoding for the peripherals. APB memory map is described in [Figure 13](#) and [Figure 14](#).

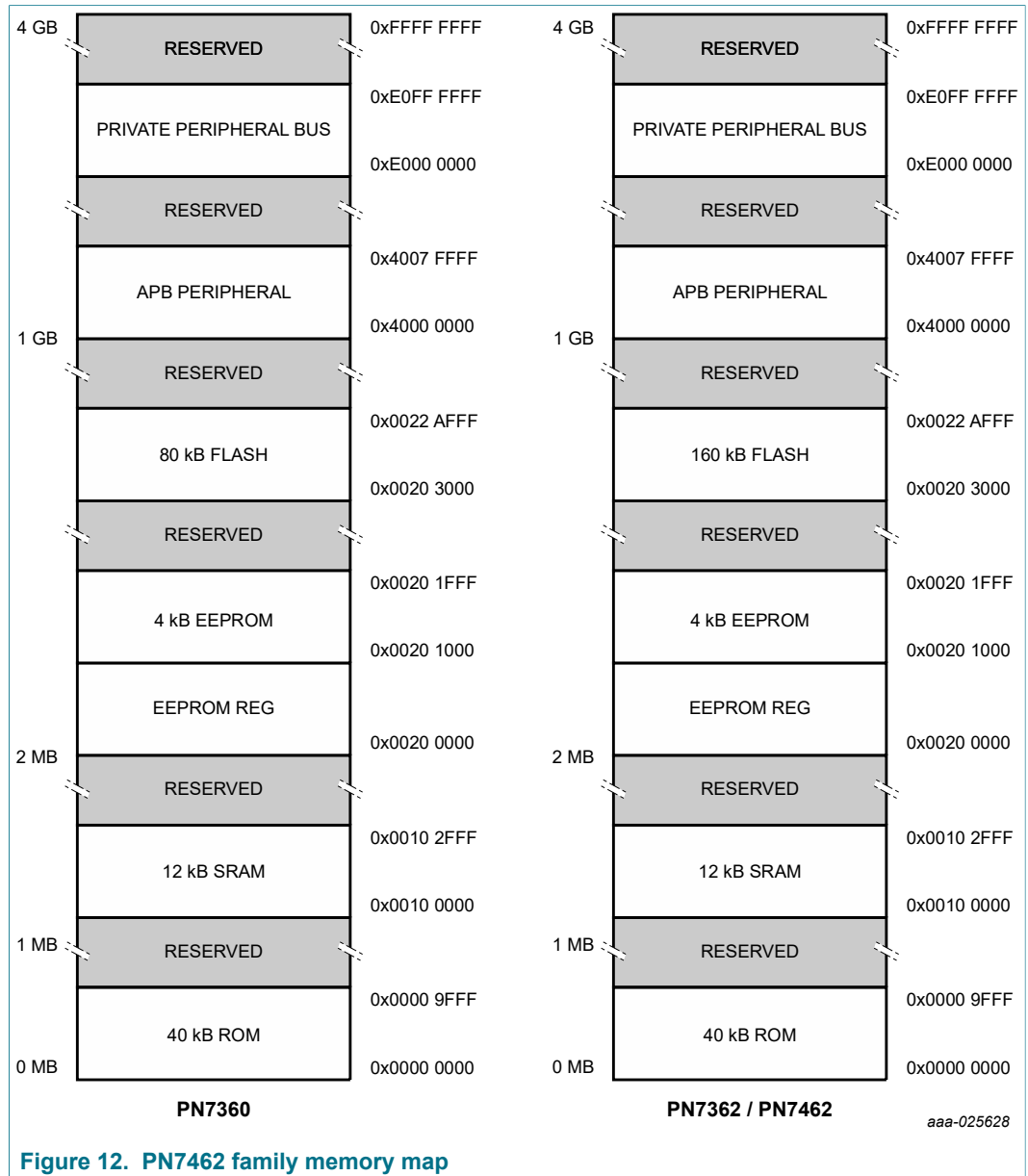


Figure 12. PN7462 family memory map

| APB ID | APB IF name | Connected IP | |
|----------|---------------|--------------------------------|-------------|
| 16 to 31 | Reserved | | 0x4004 8000 |
| 15 | Reserved | | 0x4004 0000 |
| 14 | Reserved | | 0x4003 C000 |
| 13 | SPIMASTER_APB | SPI Master IF | 0x4003 8000 |
| 12 | I2CMASTER_APB | I2C Master IF | 0x4003 4000 |
| 11 | Reserved | | 0x4003 0000 |
| 10 | USB_APB | HostIF (USB) IP | 0x4002 C000 |
| 9 | PCR_APB | PowerClockResetModule IP | 0x4002 8000 |
| 8 | HOST_APB | HostIF (I2C/SPI/HSU/BufMgt) IP | 0x4002 4000 |
| 7 | TIMERS_APB | Timer IP | 0x4002 0000 |
| 6 | RNG_APB | RNG IP | 0x4001 C000 |
| 5 | Reserved | | 0x4001 8000 |
| 4 | CLOCKGEN_APB | Clock Gen module | 0x4001 4000 |
| 3 | CRC_APB | CRC IP | 0x4001 0000 |
| 2 | PMU_APB | PMU modules | 0x4000 C000 |
| 1 | CL_APB | Contactless IP | 0x4000 8000 |
| 0 | Reserved | | 0x4000 4000 |

aaa-021127

Figure 13. APB memory map PN736X

| APB ID | APB IF name | Connected IP | |
|----------|---------------|--------------------------------|-------------|
| 16 to 31 | Reserved | | 0x4004 8000 |
| 15 | Reserved | | 0x4004 0000 |
| 14 | Reserved | | 0x4003 C000 |
| 13 | SPIMASTER_APB | SPI Master IF | 0x4003 8000 |
| 12 | I2CMASTER_APB | I2C Master IF | 0x4003 4000 |
| 11 | Reserved | | 0x4003 0000 |
| 10 | USB_APB | HostIF (USB) IP | 0x4002 C000 |
| 9 | PCR_APB | PowerClockResetModule IP | 0x4002 8000 |
| 8 | HOST_APB | HostIF (I2C/SPI/HSU/BufMgt) IP | 0x4002 4000 |
| 7 | TIMERS_APB | Timer IP | 0x4002 0000 |
| 6 | RNG_APB | RNG IP | 0x4001 C000 |
| 5 | CTUART_APB | Contact UART IP | 0x4001 8000 |
| 4 | CLOCKGEN_APB | Clock Gen module | 0x4001 4000 |
| 3 | CRC_APB | CRC IP | 0x4001 0000 |
| 2 | PMU_APB | PMU modules | 0x4000 C000 |
| 1 | CL_APB | Contactless IP | 0x4000 8000 |
| 0 | Reserved | | 0x4000 4000 |

aaa-028697

Figure 14. APB memory map PN7462

| APB ID | APB IF name | Connected IP | |
|----------|---------------|--------------------------------|-------------|
| 16 to 31 | Reserved | | 0x4004 8000 |
| 15 | Reserved | | 0x4004 0000 |
| 14 | Reserved | | 0x4003 C000 |
| 13 | SPIMASTER_APB | SPI Master IF | 0x4003 8000 |
| 12 | I2CMaster_APB | I2C Master IF | 0x4003 4000 |
| 11 | Reserved | | 0x4003 0000 |
| 10 | USB_APB | HostIF (USB) IP | 0x4002 C000 |
| 9 | PCR_APB | PowerClockResetModule IP | 0x4002 8000 |
| 8 | HOST_APB | HostIF (I2C/SPI/HSU/BufMgt) IP | 0x4002 4000 |
| 7 | TIMERS_APB | Timer IP | 0x4002 0000 |
| 6 | RNG_APB | RNG IP | 0x4001 C000 |
| 5 | CTUART_APB | Contact UART IP | 0x4001 8000 |
| 4 | CLOCKGEN_APB | Clock Gen module | 0x4001 4000 |
| 3 | CRC_APB | CRC IP | 0x4001 0000 |
| 2 | PMU_APB | PMU modules | 0x4000 C000 |
| 1 | Reserved | | 0x4000 8000 |
| 0 | Reserved | | 0x4000 4000 |
| | | | 0x4000 0000 |

aaa-030119

Figure 15. APB memory map PN7412

8.3 Nested Vectored Interrupt Controller (NVIC)

Cortex-M0 includes a Nested Vectored Interrupt Controller (NVIC). The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

8.3.1 NVIC features

- System exceptions and peripheral interrupts control
- Support 32 vectored interrupts
- Four interrupt priority levels with hardware priority level masking
- One Non-Maskable Interrupt (NMI) connected to the watchdog interrupt
- Software interrupt generation

8.3.2 Interrupt sources

The following table lists the interrupt sources available in the PN7462 family microcontroller.

Table 6. Interrupt sources

| EIRQ# | Source | Description |
|-------|---------------|--|
| 0 | timer 0/1/2/3 | general-purpose timer 0/1/2/3 interrupt |
| 1 | - | reserved |
| 2 | CLIF | NFC interface module interrupt |
| 3 | EECTRL | EEPROM controller |
| 4 | - | reserved |
| 5 | - | reserved |
| 6 | host IF | TX or RX buffer from I ² C, SPI, HSU, or USB module |

| EIRQ# | Source | Description |
|--------------------|-------------------------|--|
| 7 | contact IF | ISO7816 contact module interrupt |
| 8 | - | reserved |
| 9 | PMU | power management unit (temperature sensor, over current, overload, and VBUS level) |
| 10 | SPI master | TX or RX buffer from SPI master module |
| 11 | I ² C master | TX or RX buffer from I ² C master module |
| 12 | PCR | high temperature from temperature sensor 0 and 1; interrupt to CPU from PCR to indicate wake-up from suspend mode; out of standby; out of suspend; event on GPIOs configured as inputs |
| 13 | PCR | interrupt common GPIO1 to GPIO12 |
| 14 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO1 |
| 15 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO2 |
| 16 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO3 |
| 17 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO4 |
| 18 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO5 |
| 19 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO6 |
| 20 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO7 |
| 21 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO8 |
| 22 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO9 |
| 23 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO10 |
| 24 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO11 |
| 25 | PCR | interrupt (rise/fall/both-edge/level-high/level-low interrupt as programmed) GPIO12 |
| 26 | - | reserved |
| 27 | - | reserved |
| 28 | - | reserved |
| 29 | - | reserved |
| 30 | - | reserved |
| 31 | - | reserved |
| NMI ^[1] | WDT | watchdog interrupt is connected to the non-maskable interrupt pin |

[1] The NMI is not available on an external pin.

8.4 GPIOs

The PN7462 family has up to 21 general-purpose I/O (GPIO) with configurable pull-up and pull-down resistors, up to 9 of those GPIOs are multiplexed with SPI master, I²C-bus master and AUX pins (if available).

Pins can be dynamically configured as inputs or outputs. GPIO read/write are made by the FW using dedicated registers that allow reading, setting, or clearing inputs. The value of the output register can be read back, as well as the current state of the input pins.

8.4.1 GPIO features

- Dynamic configuration as input or output
- 3.3 V and 1.8 V signaling
- Programmable weak pull-up and weak pull-down
- Independent interrupts for GPIO1 to GPIO12
- Interrupts: edge or level sensitive
- GPIO1 to GPIO12 can be programmed as wake-up sources
- Programmable spike filter (3 ns)
- Programmable slew rate (3 ns and 10 ns)
- Hysteresis receiver with disable option

8.4.2 GPIO configuration

The GPIO configuration is done through the PCR module (power, clock, and reset).

8.4.3 GPIO interrupts

GPIO1 to GPIO12 can be programmed to generate an interrupt on a level, a rising or falling edge or both.

8.5 CRC engine 16/32 bits

The PN7462 family has a configurable 16/32-bit parallel CRC coprocessor.

The 16-bit CRC is compliant to X.25 (CRC-CCITT, ISO/IEC 13239) standard with a generator polynomial of:

$$g(x) = x^{16} + x^{12} + x^5 + 1$$

The 32-bit CRC is compliant to the ethernet/AAL5 (IEEE 802.3) standard with a generator polynomial of:

$$g(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

CRC calculation is performed in parallel, meaning that one CRC calculation is performed in one clock cycle. The standard CRC 32 polynomial is compliant with FIPS140-2.

Note: No final XOR calculation is performed.

Following are the CRC engine features:

- Configurable CRC preset value
- Selectable LSB or MSB first
- CRC 32 calculation based on 32-bit, 16-bit, and 8-bit words
- CRC16 calculation based on 32-bit, 16-bit, and 8-bit words
- Supports bit order reverse

8.6 Random Number Generator (RNG)

The PN7462 family integrates a random number generator. It consists of an analog True Random Number Generator (TRNG), and a digital Pseudo Random Number Generator (PRNG). The TRNG is used for loading a new seed in the PRNG.

The random number generator features:

- 8-bit random number
- Compliant with FIPS 140-2
- Compliant with BSI AIS20 and SP800-22

8.7 Master interfaces

8.7.1 I²C master interface

8.7.1.1 I²C features

The I²C master interface supports the following features:

- Standard I²C-compliant bus interface with open-drain pins
- Standard-mode, fast mode, and fast mode plus (up to 1 Mbit/s).
- Support I²C master mode only.
- Programmable clocks allowing versatile rate control.
- Clock stretching
- 7-bit and 10-bit I²C slave addressing
- LDM/STM instruction support
- Maximum data frame size up to 1024 bytes

8.7.2 SPI interface

The PN7462 family contains one SPI master controller and one SPI slave controller.

The SPI master controller transmits the data from the system RAM to the SPI external slaves. Similarly, it receives data from the SPI external slaves and stores them into the system RAM. It can compute a CRC for received frames and automatically compute and append CRC for outgoing frames (optional feature).

8.7.2.1 SPI features

The SPI master interface provides the following features:

- SPI master interface: synchronous, half-duplex
- Supports Motorola SPI frame formats only (SPI block guide V04.0114 (Freescale) specification)
- Maximum SPI data rate of 6.78 Mbit/s

- Multiple data rates such as 1, 1.51, 2.09, 2.47, 3.01, 4.52, 5.42 and 6.78 Mbit/s
- Up to two slaves select with selectable polarity
- Programmable clock polarity and phase
- Supports 8-bit transfers only
- Maximum frame size: 511 data bytes payload + 1 CRC byte
- Optional 1 byte CRC calculation on all data of TX and RX buffer
- AHB master interface for data transfer

8.8 Host interfaces

The PN7462 family embeds four different interfaces for host connection: USB, HSUART, I²C, and SPI.

The four interfaces share the buffer manager and the pins; see [Table 7](#).

Table 7. Pin description for host interface

| Name | SPI | I ² C | USB | HSU |
|-------|--------|-----------------------|-----|-----------|
| ATX_A | NSS_S | SCL_S | - | HSU_RX |
| ATX_B | MOSI_S | SDA_S | - | HSU_TX |
| ATX_C | MISO_S | I ² C_ADR0 | DP | HSU_RTS_N |
| ATX_D | SCK_S | I ² C_ADR1 | DM | HSU_CTS_N |

The interface selection is done by configuring the Power Clock Reset (PCR) registers.

Note: The host interface pins should not be kept floating.

8.8.1 High-speed UART

The PN7462 family has a high-speed UART which can operate in slave mode only.

Following are the HSUART features:

- Standard bit-rates are 9600, 19200, 38400, 57600, 115200, and up to 1.288 Mbit/s
- Supports full duplex communication
- Supports only one operational mode: start bit, 8 data bits (LSB), and stop bits
- The number of "stop bits" programmable for RX and TX is 1 stop bit or 2 stop bits
- Configurable length of EOF (1-bit to 122-bits)

Table 8. HSUART baudrates

| Bit rate (kBd) |
|----------------|
| 9.6 |
| 19.2 |
| 38.4 |
| 57.6 |
| 115.2 |
| 230.4 |
| 460.8 |
| 921.6 |
| 1288 K |

8.8.2 I²C host interface controller

The I²C-bus is bidirectional and uses only two wires: a Serial Clock Line (SCL) and a Serial Data Line (SDA). I²C standard mode (100 kbit/s), fast mode (400 kbit/s and up to 1 Mbit/s), and high-speed mode (3.4 Mbit/s) are supported.

8.8.2.1 I²C host interface features

The PN7462 family I²C slave interface supports the following features:

- Support slave I²C bus
- Standard mode, fast mode (extended to 1 Mbit/s support), and high-speed modes
- Supports 7-bit addressing mode only
- Selection of the I²C address done by two pins
 - It supports multiple addresses
 - The upper bits of the I²C slave address are hard-coded. The value corresponds to the NXP identifier for I²C blocks. The value is 0101 0XXb.
- General call (software reset only)
- Software reset (in standard mode and fast mode only)

Table 9. I²C interface addressing

| I ² C_ADR1 | I ² C_ADR0 | I ² C address (R/W = 0, write) | I ² C address (R/W = 0, read) |
|-----------------------|-----------------------|---|--|
| 0 | 0 | 0 × 28 | 0 × 28 |
| 0 | 1 | 0 × 29 | 0 × 29 |
| 1 | 0 | 0 × 2A | 0 × 2A |
| 1 | 1 | 0 × 2B | 0 × 2B |

8.8.3 SPI host/Slave interface

The PN7462 family host interface can be used as SPI slave interface.

The SPI slave controller operates on a four wire SSI: Master In Slave Out (MISO), Master Out Slave In (MOSI), Serial Clock (SCK), and Not Slave Select (NSS). The SPI slave select polarity is fixed to positive polarity.

8.8.3.1 SPI host interface features

The SPI host/slave interface has the following features:

- SPI speeds up to 7 Mbit/s
- Slave operation only
- 8-bit data format only
- Programmable clock polarity and phase
- SPI slave select polarity selection fixed to positive polarity
- Half-duplex in HDLL mode
- Full-duplex in native mode

If no data is available, the MISO line is kept idle by making all the bits high (0xFF). Toggling the NSS line indicates a new frame.

Note: Programmable echo-back operation is not supported.

Table 10. SPI configuration

| connection |
|--|
| CPHA switch: Clock phase: Defines the sampling edge of MOSI data <ul style="list-style-type: none"> • CPHA = 1: Data are sampled on MOSI on the even clock edges of SCK, after NSS goes low • CPHA = 0: Data are sampled on MOSI on the odd clock edges of SCK, after NSS goes low |
| CPOL switch: Clock polarity <ul style="list-style-type: none"> • IFSEL1 = 0: The clock is idle low, and the first valid edge of SCK is a rising one • IFSEL1 = 1: The clock is idle high, and the first valid edge of SCK is a falling one |

8.8.4 USB interface

The Universal Serial Bus (USB) is a 4-wire bus that supports communication between a host and up to 127 peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot-plugging and dynamic configuration of devices. The host controller initiates all transactions. The PN7462 family USB interface consists of a full-speed device controller with on-chip PHY (physical layer) for device functions.

8.8.4.1 Full speed USB device controller

The PN7462 family embeds a USB device peripheral, compliant with USB 2.0 specification, full speed. It is interoperable with USB 3.0 host devices.

The device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of a register interface, serial interface engine, and endpoint buffer memory. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer.

The status of a completed USB transfer or error condition is indicated via status registers. If enabled, an interrupt is generated.

Following are the USB interface features:

- Fully compliant with USB 2.0 specification (full speed)
- Dedicated USB PLL available
- Supports 14 physical (7 logical) endpoints including one control endpoint
- Each non-control endpoint supports bulk, interrupt, or isochronous endpoint types
- Single or double buffering allowed
- Support wake-up from suspend mode on USB activity and remote wake-up
- Soft-connect supported

8.9 Contact interface

Note: This following chapter applies to PN7462AUHN, PN7412AUHN and PN7462AUEV only. PN7462AUHN and PN7412AUHN embed a contact interface and I/O auxiliary interface. PN7462AUEV embeds the I/O auxiliary interface only.

The PN7462 and PN7412 integrate an ISO/IEC 7816 interface to enable the communication with a contact smart card. It does not require addition of an external contact frontend for reading payment cards, SAM for secure applications, etc. It offers a high level of security for the card by performing current limitation, short-circuit detection, ESD protection as well as supply supervision.

PN7462 and PN7412 also offer the possibility to extend the number of contact interfaces available. They use an I/O auxiliary interface to connect a slot extension (TDA8035 - 1 slot, TDA8020 - 2 slots, and TDA8026 - 5 slots).

- Class A (5 V), class B (3 V), and class C (1.8 V) smart card supply
- Protection of smart card
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7, and C8)
- Compliant with ISO/IEC 7816 and EMVCo 4.3 standards

8.9.1 Contact interface features and benefits

- Protection of the smart card
 - Thermal and current limitation in the event of short-circuit (pins I/O, V_{CC})
 - V_{CC} regulation: 5 V, 3 V, and 1.8 V
 - Automatic deactivation initiated by hardware in the event of a short-circuit, card take-off, overheating, falling of PN7462 supply
 - Enhanced card-side ElectroStatic Discharge (ESD) protection of greater than 8 kV
- Support of class A, class B, and class C contact smart cards
- DC-to-DC converter for V_{CC} generation to enable support of class A and class B cards with low input voltages
- Built-in debouncing on card presence contact
- Compliant with ISO/IEC 7816 and EMVCo 4.3 standards
- Card clock generation up to 13.56 MHz using external crystal oscillator (27.12 MHz); provides synchronous frequency changes of $f_{XTAL} / 2$, $f_{XTAL} / 3$, $f_{XTAL} / 4$, $f_{XTAL} / 5$, $f_{XTAL} / 6$, $f_{XTAL} / 8$, and $f_{XTAL} / 16$
- Specific ISO/IEC UART with APB access for automatic convention processing, variable baud rate through frequency or division ratio programming, error management at character level for T = 0 and extra guard time register
 - FIFO 1 character to 32 characters in both reception and transmission mode
 - Parity error counter in reception mode and transmission mode with automatic retransmission
 - Cards clock stop (at HIGH or LOW level)
 - Automatic activation and deactivation sequence through a sequencer
 - Supports the asynchronous protocols T = 0 and T = 1 in accordance with ISO/IEC 7816 and EMV
 - Versatile 24-bit timeout counter for Answer To Reset (ATR) and waiting times processing
 - Specific Elementary Time Unit (ETU) counter for Block Guard Time (BGT); 22 ETU in T = 1 and 16 ETU in T = 0
 - Supports synchronous cards

8.9.2 Voltage supervisor

The PN7462 integrates a voltage monitor to ensure that sufficient voltage is available for the contact interface; see [Section 8.15.4](#) and [Section 9.1.3](#).

In order to provide the right voltage needed for the various ISO/IEC 7816 contact card classes (A, B, or C), the following voltages are needed:

- $V_{DDP}(V_{BUSP}) > 2.7$ V for support of class B and class C contact cards
- $V_{DDP}(V_{BUSP}) > 3$ V for support of class A contact cards

- **Remark:** To support class A cards, DC-to-DC converter is used in doubler mode. To support class B cards with $V_{DDP(VBUSP)} < 3.9\text{ V}$, DC-to-DC converter is used in doubler mode. To support class B cards with $V_{DDP(VBUSP)} > 3.9\text{ V}$, DC-to-DC converter is used in follower mode.

Figure 16 shows the classes that are supported, depending on $V_{DDP(VBUSP)}$.

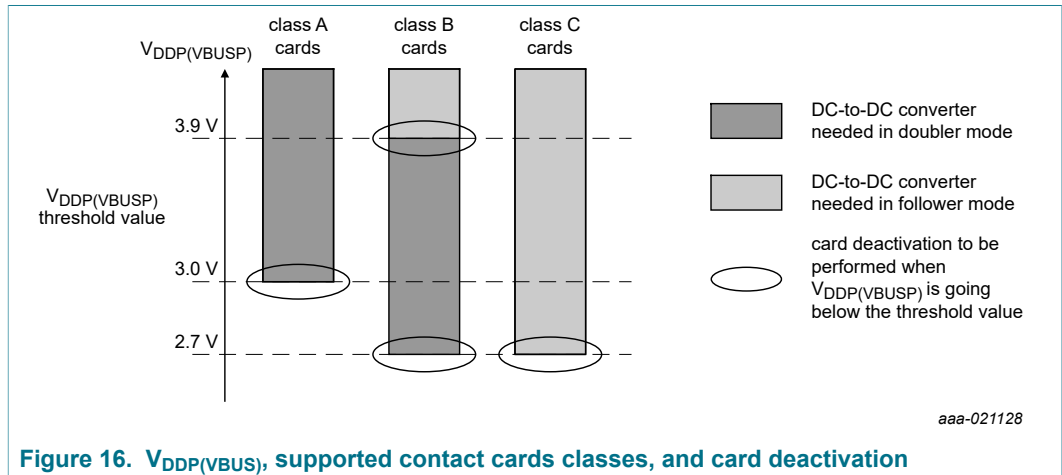


Figure 16. $V_{DDP(VBUS)}$, supported contact cards classes, and card deactivation

When the $V_{DDP(VBUSP)}$ is going below the threshold value, in the one of the conditions indicated below, a card deactivation is performed:

- Class A card activated, and $V_{DDP(VBUSP)}$ going below 3 V
- Class B card activated, and $V_{DDP(VBUSP)}$ going below 3.9 V (DC-to-DC converter in follower mode)
- Class B card activated, and $V_{DDP(VBUSP)}$ going below 2.7 V (DC-to-DC converter in doubler mode)
- Class C card activated, and $V_{DDP(VBUSP)}$ going below 2.7 V

The VBUSP voltage monitor can be configured so that an automatic "card deactivation" sequence is performed automatically when $V_{DDP(VBUSP)}$ is going below the threshold value.

8.9.3 Clock circuitry

The card clock is generated from the crystal oscillator, connected on the pin XTAL1 and XTAL2.

The card frequency is configured through the contact interface registers. The following value can be chosen: $f_{XTAL} / 2$, $f_{XTAL} / 3$, $f_{XTAL} / 4$, $f_{XTAL} / 5$, $f_{XTAL} / 6$, $f_{XTAL} / 8$, and $f_{XTAL} / 16$.

It is possible to put the card clock to a logical level 0 or 1 (clock stop feature).

The duty cycle on the pin CLK is between 45 % and 55 %, for all the available clock dividers.

8.9.4 I/O circuitry

The three data lines I/O, AUX1, and AUX2 are identical.

I/O is referenced to V_{CC} . To enter in the idle state, the I/O line is pulled HIGH via a 10 k Ω resistor (I/O to V_{CC}).

The active pull-up feature ensures fast LOW to HIGH transitions. At the end of the active pull-up pulse, the output voltage depends on the internal pull-up resistor and the load current.

The maximum frequency on these lines is 1.5 MHz.

8.9.5 VCC regulator

VCC regulator delivers up to 60 mA for class A cards (0 V to 5 V). It also delivers up to 55 mA for class B cards (0 V to 3 V) and up to 35 mA for class C cards (from 0 V to 1.8 V).

The VCC has an internal overload detection at approximately 110 mA for class A and B, and 90 mA for class C.

This detection is internally filtered, allowing the card to draw spurious current pulses as defined in EMVCo specification, without causing a deactivation. The average current value must remain below the maximum.

8.9.6 Activation sequence

The presence of a contact card is indicated to PN7462 through PRESN signal. If all supply conditions are met, the PN7462 may start an activation sequence. [Figure 17](#) shows the activation sequence.

The sequencer clock is based on the crystal oscillator: $f_{seq} = f_{XTAL} / 10$. When the contact interface is active, the period for activation phases is: $T = 64 / f_{seq} = 23.6 \mu s$.

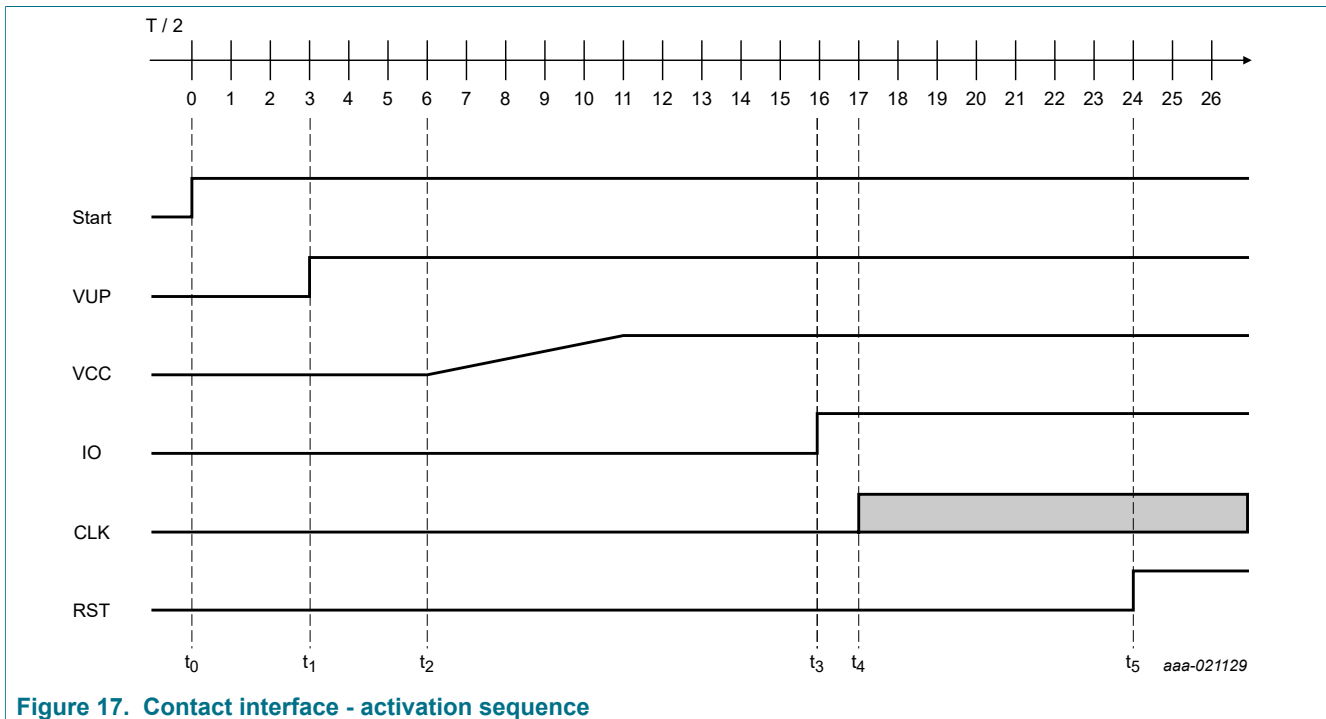


Figure 17. Contact interface - activation sequence

Once the activation sequence is triggered, the following sequence takes place:

- Contact LDOs and DC-to-DC converter (when relevant) starts at t_1
- VCC starts rising from 0 to the required voltage (5 V, 3 V, and 1.8 V) at t_2

- IO rises to VCC at t_3
- CLK starts at t_4
- RST pin is enabled at t_5

8.9.7 Deactivation sequence

When triggered by the PN7462, the deactivation following sequence takes place:

- Card reset (pin RST) status goes LOW
- Clock (CLK) stopped at LOW level
- Pin IO falls to 0 V
- VCC falls to 0 V

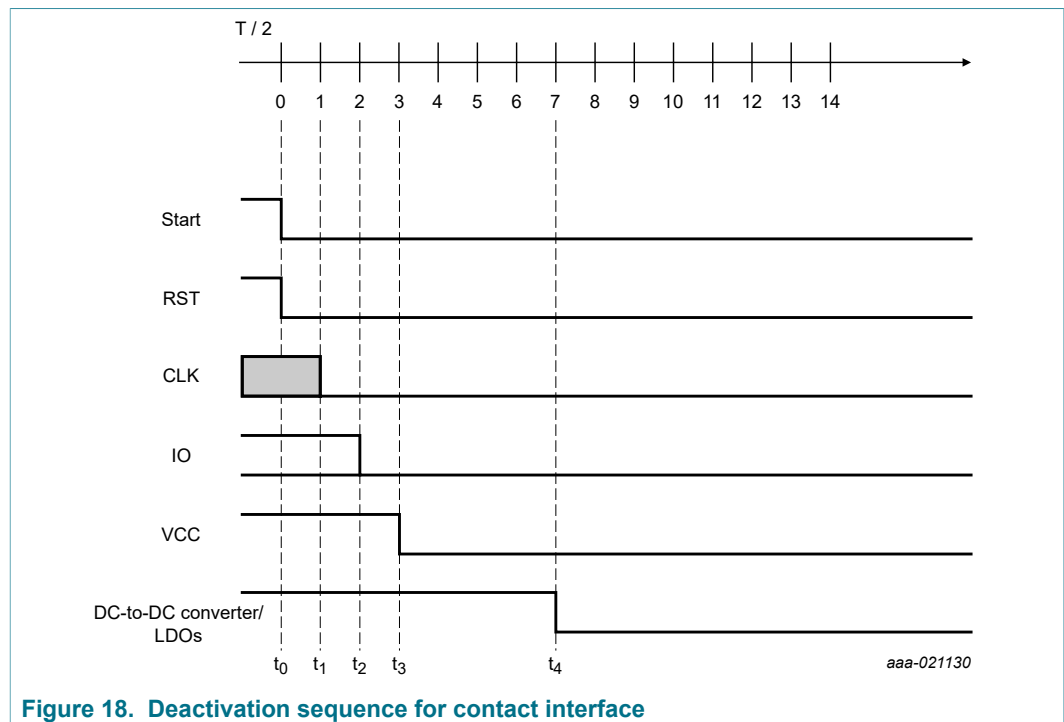


Figure 18. Deactivation sequence for contact interface

The deactivation sequence is performed in the following cases:

- Removal of card; generated automatically by the PN7462
- Overcurrent detection on pin VCC; generated automatically by the PN7462
- Overcurrent detection on pin IO; generated automatically by the PN7462
- Detection for overheating; generated automatically by the PN7462
- Pin VBUSP going below relevant voltage threshold (optional); part of the pin VBUSP monitor
- Reset request through software

8.9.8 I/O auxiliary - connecting TDA slot extender

To address applications where multiple ISO/IEC 7816 interfaces are needed, the PN7462 integrates the possibility to connect contact slot extenders like TDA8026, TDA8020, or TDA8035.

The following pins are available:

- INT_AUX
- CLK_AUX
- IO_AUX

For more details about the connection, refer to the slot extender documentation.

8.10 Contactless interface - 13.56 MHz

This chapter applies to the products with contactless interface only.

The PN7462 family embeds a high power 13.56 MHz RF frontend. The RF interface implements the RF functionality like antenna driving, the receiver circuitry, and all the low-level functionalities. It helps to realize an NFC forum or an EMVCo compliant reader.

The PN7462 family allows different voltages for the RF drivers. For information related to the RF interface supply, refer [Section 8.15](#).

The PN7462 family uses an external oscillator, at 27.12 MHz. It is a clock source for generating RF field and its internal operation.

Key features of the RF interface are:

- ISO/IEC 14443 type A & B compliant
- MIFARE functionality, including MIFARE Classic encryption in read/write mode
- ISO/IEC 15693 compliant
- NFC Forum - NFCIP-1 & NFCIP-2 compliant
 - P2P, active and passive mode
 - reading of NFC forum tag types 1, 2, 3, 4, and 5
- FeliCa
- ISO/IEC 18000-3 mode 3
- EMVCo contactless 2.6
 - RF level can be achieved without the need of booster circuitry (for some antenna topologies the EMV RF-level compliance might physically not be achievable)
- Card mode - enabling the emulation of an ISO/IEC 14443 type A card
 - Supports Passive Load Modulation (PLM) and Active Load Modulation (ALM)
- Low Power Card Detection (LPCD)
- Adjustable RX-voltage level

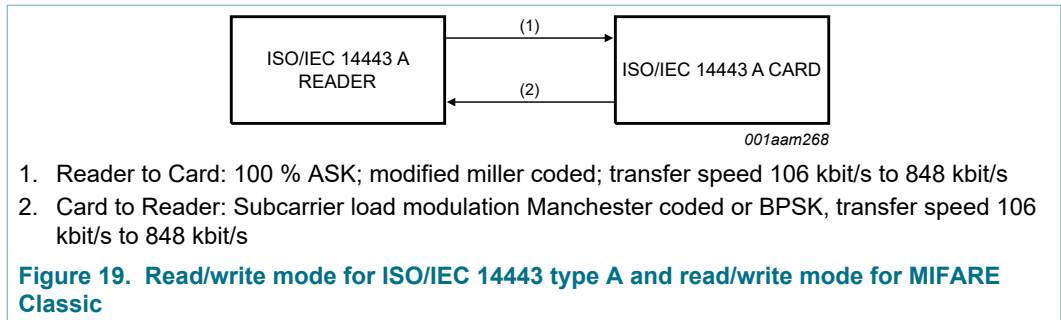
A minimum voltage of 2.3 V helps to use card emulation, and P2P passive target functionality in passive load modulation.

A voltage above 2.7 V enables all contactless functionalities.

8.10.1 RF functionality

8.10.1.1 Communication mode for ISO/IEC 14443 type A and for MIFARE Classic

The physical level of the communication is shown in [Figure 19](#).

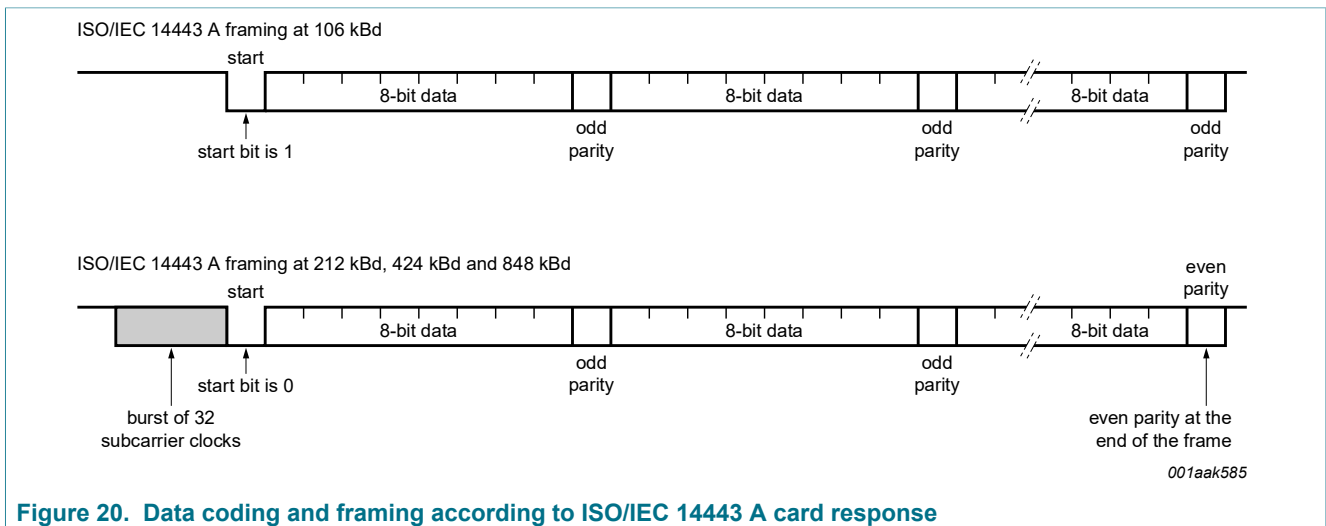


The physical parameters are described in [Table 11](#)

Table 11. Communication overview for ISO/IEC 14443 type A and read/write mode for MIFARE Classic

| Communication direction | Signal type | Transfer speed | | | |
|--|------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| | | 106 kbit/s | 212 kbit/s | 424 kbit/s | 848 kbit/s |
| reader to card (send data from the PN7462 family to a card) $f_c = 13.56$ MHz | reader side modulation | 100 % ASK | 100 % ASK | 100 % ASK | 100 % ASK |
| | bit encoding | modified miller encoding | modified miller encoding | modified miller encoding | modified miller encoding |
| | bit rate (kbit/s) | $f_c / 128$ | $f_c / 64$ | $f_c / 32$ | $f_c / 16$ |
| card to reader (PN7462 family receives data from a card) | card side modulation | sub carrier load modulation | sub carrier load modulation | sub carrier load modulation | sub carrier load modulation |
| | subcarrier frequency | $f_c / 16$ | $f_c / 16$ | $f_c / 16$ | $f_c / 16$ |
| | bit encoding | Manchester encoding | BPSK | BPSK | BPSK |

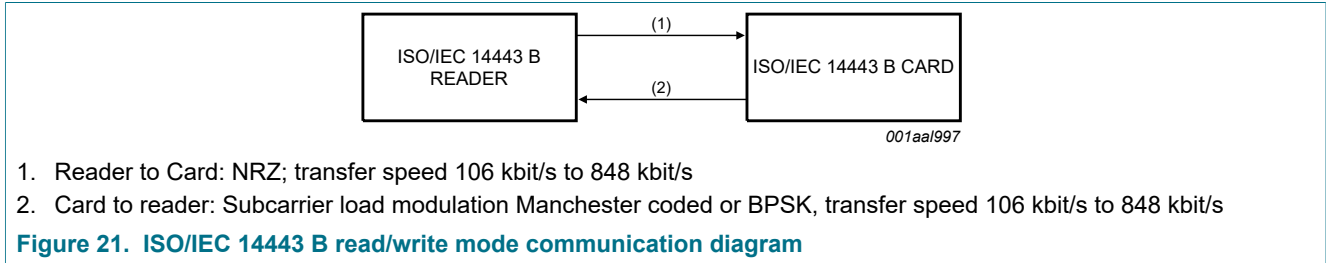
[Figure 20](#) shows the data coding and framing according to ISO/IEC 14443 A.



The internal CRC coprocessor calculates the CRC value based on the selected protocol. In card mode for higher baudrates, the parity is automatically inverted as end of communication indicator.

8.10.1.2 ISO/IEC14443 B functionality

The physical level of the communication is shown in [Figure 21](#)



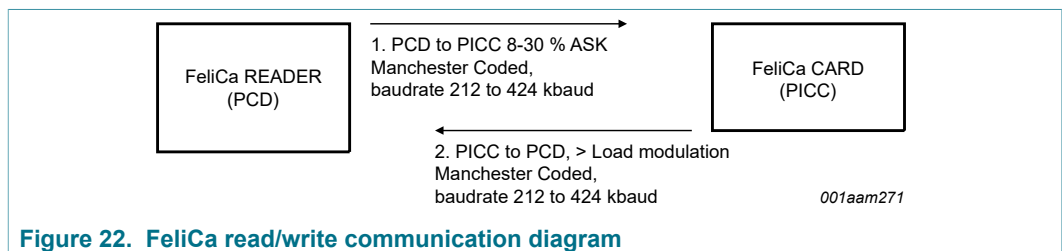
The physical parameters are described in [Table 12](#)

Table 12. Communication overview for ISO/IEC 14443 B reader/writer

| Communication direction | Signal type | Transfer speed | | | |
|--|------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| | | 106 kbit/s | 212 kbit/s | 424 kbit/s | 848 kbit/s |
| reader to card (send data from the PN7462 family to a card) $f_c = 13.56$ MHz | reader side modulation | 10 % ASK | 10 % ASK | 10 % ASK | 10 % ASK |
| | bit encoding | NRZ | NRZ | NRZ | NRZ |
| | bit rate [kbit/s] | $128/f_c$ | $64/f_c$ | $32/f_c$ | $16/f_c$ |
| card to reader (PN7462 family receives data from a card) | card side modulation | sub carrier load modulation | sub carrier load modulation | sub carrier load modulation | sub carrier load modulation |
| | sub carrier frequency | $f_c / 16$ | $f_c / 16$ | $f_c / 16$ | $f_c / 16$ |
| | bit encoding | BPSK | BPSK | BPSK | BPSK |

8.10.1.3 FeliCa functionality

The FeliCa mode is a general reader/writer to card communication scheme, according to the FeliCa specification. The communication on a physical level is shown in [Figure 22](#).



The physical parameters are described in [Table 13](#).

Table 13. Communication overview for FeliCa reader/writer

| Communication direction | Signal type | Transfer speed FeliCa | |
|--|------------------------|-----------------------|---|
| | | 212 kbit/s | FeliCa higher transfer speeds 424 kbit/s |
| reader to card (send data from the PN7462 family to a card) $f_c = 13.56 \text{ MHz}$ | reader side modulation | 8 % to 30 % ASK | 8 % to 30 % ASK |
| | bit encoding | Manchester encoding | Manchester encoding |
| | bit rate | $f_c / 64$ | $f_c / 32$ |
| card to reader (PN7462 family receives data from a card) | card side modulation | load modulation | load modulation |
| | bit encoding | Manchester encoding | Manchester encoding |

Note: The PN7462 family does not manage FeliCa security aspects.
PN7462 family supports FeliCa multiple reception cycles.

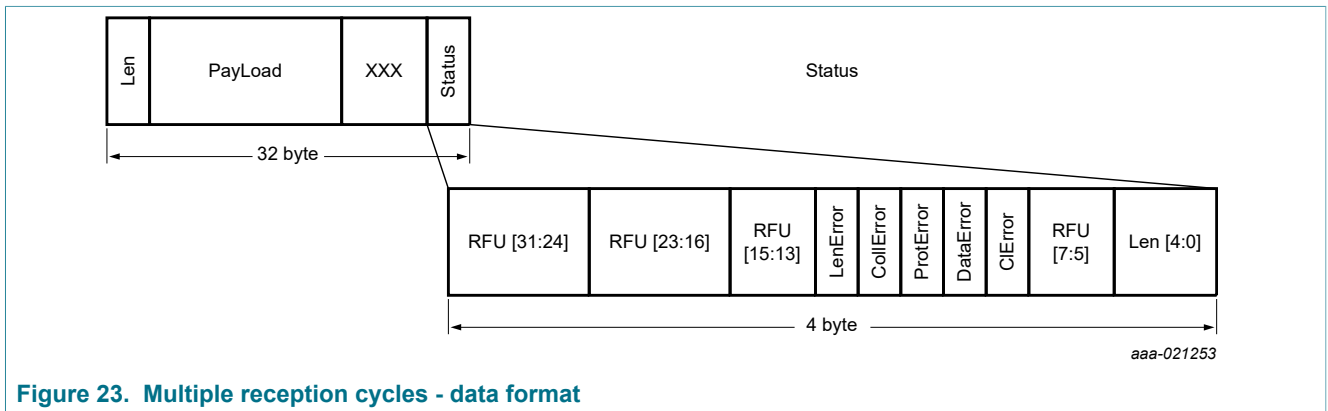


Figure 23. Multiple reception cycles - data format

8.10.1.4 ISO/IEC 15693 functionality

The physical level of the communication is shown in [Figure 24](#).

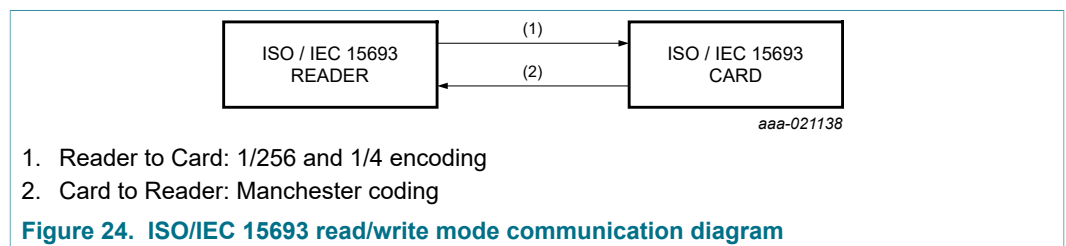


Figure 24. ISO/IEC 15693 read/write mode communication diagram

The physical parameters are described in [Table 14](#).

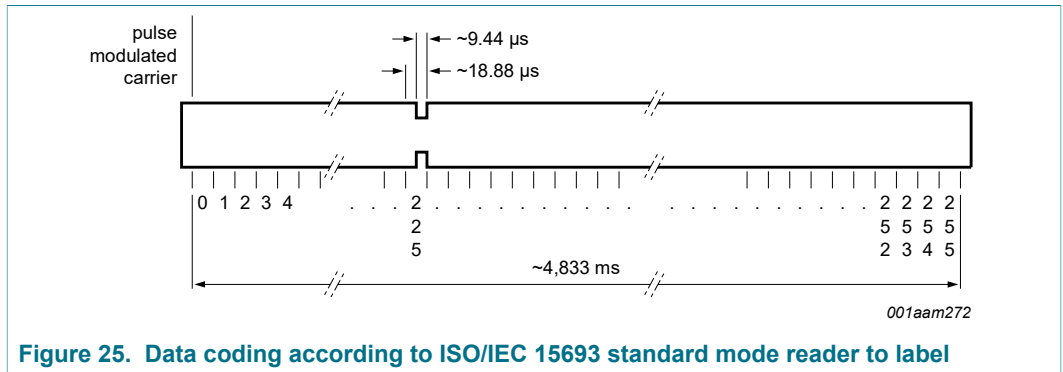
Table 14. Communication overview for ISO/IEC 15693 reader to label

| Communication direction | Signal type | Transfer speed | |
|--|------------------------|-------------------------------|---------------------------------------|
| | | $f_c / 8192 \text{ kbit/s}$ | $f_c / 512 \text{ kbit/s}$ |
| reader to label (send data from the PN7462 family to a card) | reader side modulation | 10 % to 30 % ASK or 100 % ASK | 10 % to 30 % ASK or 90 % to 100 % ASK |
| | bit encoding | 1/256 | 1/4 |
| | bit length | 4.833 μs | 302.08 μs |

Table 15. Communication overview for ISO/IEC 15693 label to reader

| Communication direction | Signal type | Transfer speed | | | |
|--|----------------------------|----------------|-----------------------------|---|--|
| | | 6.62 kbit/s | 13.24 kbit/s ^[1] | 26.48 kbit/s | 52.96 kbit/s |
| label to reader (PN7462 family receives data from a card) $f_c = 13.56$ MHz | card side modulation | not supported | not supported | single (dual) sub carrier load modulation ASK | single sub carrier load modulation ASK |
| | bit length (μ s) | - | - | 37.76 | 18.88 |
| | bit encoding | - | - | Manchester coding | Manchester coding |
| | subcarrier frequency (MHz) | - | - | $f_c / 32$ | $f_c / 32$ |

[1] Fast inventory (page) read command only (ICODE proprietary command).



8.10.1.5 ISO/IEC18000-3 mode 3 functionality

The ISO/IEC 18000-3 mode 3 is not described in this document. For a detailed explanation of the protocol, refer to the ISO/IEC 18000-3 standard.

PN7462 family supports the following features:

- TARI = 9.44 μ s or 18.88 μ s
- Downlink: Four subcarrier pulse Manchester and two subcarrier pulse Manchester
- Subcarrier: 423 kHz ($f_c / 32$) with DR = 0 kHz and 847 kHz ($f_c / 16$) with DR = 1

8.10.1.6 NFCIP-1 modes

The NFCIP-1 communication differentiates between an active and a passive communication mode.

- In active communication mode, both initiator and target use their own RF field to transmit data
- In passive communication mode, the target answers to an initiator command in a load modulation scheme. The initiator is active in terms of generating the RF field
- The initiator generates RF field at 13.56 MHz and starts the NFCIP-1 communication
- In passive communication mode, the target responds to initiator command in load modulation scheme. In active communication mode, it uses a self-generated and self-modulated RF field.

PN7462 family supports NFCIP-1 standard. It supports active and passive communication mode at transfer speeds of 106 kbit/s, 212 kbit/s, and 424 kbit/s, as defined in the NFCIP-1 standard.

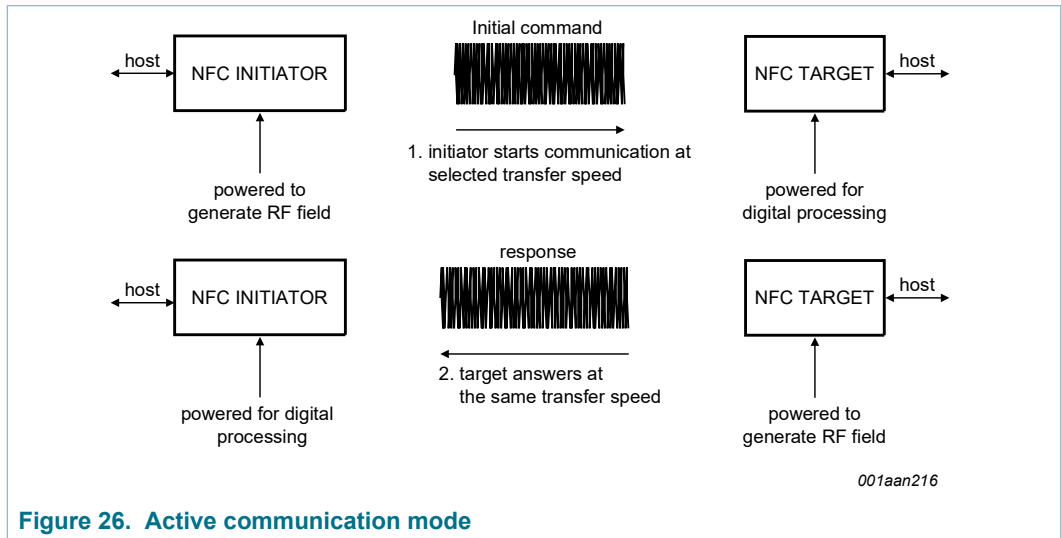


Figure 26. Active communication mode

Table 16. Communication overview for active communication mode

| Communication direction | Transfer speed | | |
|-------------------------|---|--|--|
| | 106 kbit/s | 212 kbit/s | 424 kbit/s |
| initiator to target | according to ISO/IEC 14443 A 100 % ASK, modified miller coded | according to FeliCa, 8-30 % ASK Manchester coded | according to FeliCa, 8-30 % ASK Manchester coded |
| target to initiator | | | |

Note: Transfer speeds above 424 kbit/s are not defined in the NFCIP-1 standard.

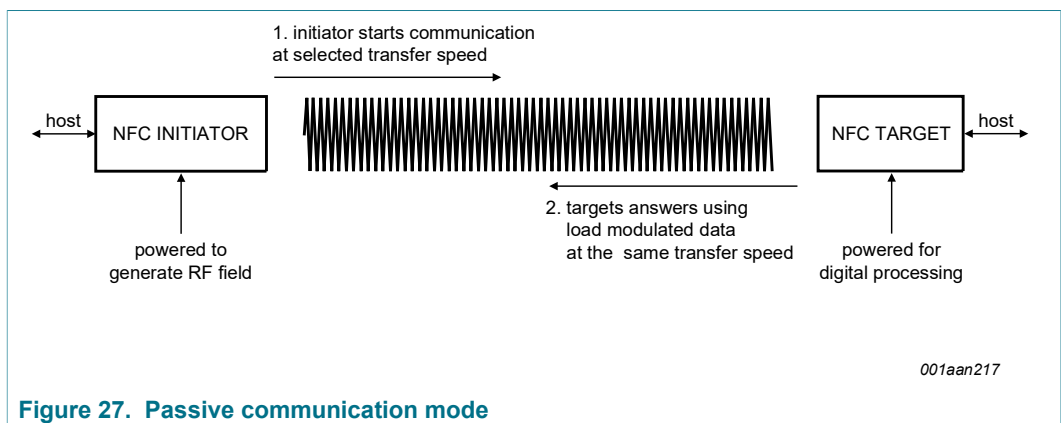


Figure 27. Passive communication mode

Table 17. Communication overview for passive communication mode

| Communication direction | Transfer speed | | |
|-------------------------|---|--|--|
| | 106 kbit/s | 212 kbit/s | 424 kbit/s |
| initiator to target | according to ISO/IEC 14443 A 100 % ASK, modified miller coded | according to FeliCa, 8-30 % ASK Manchester coded | according to FeliCa, 8-30 % ASK Manchester coded |
| target to initiator | according to ISO/IEC 14443 A @106 kB modified miller coded | according to FeliCa, > 12 % ASK Manchester coded | according to FeliCa, > 12 % ASK Manchester coded |

The NFCIP-1 protocol is managed in the PN7462 family customer application firmware.

Note: Transfer speeds above 424 kbit/s are not defined in the NFCIP-1 standard.

ISO/IEC14443 A card operation mode

PN7462 family can be addressed as a ISO/IEC 14443 A card. It means that it can generate an answer in a load modulation scheme according to the ISO/IEC 14443 A interface description.

Note: PN7462 family components do not support a complete card protocol. The NFC controller customer application firmware handles it.

The following table describes the physical layer of a ISO/IEC14443 A card mode:

Table 18. ISO/IEC14443 A card operation mode

| Communication direction | ISO/IEC 14443 A (transfer speed: 106 kbit per second) | |
|--------------------------------|---|-----------------------------|
| reader/writer to PN7462 family | modulation on reader side | 100 % ASK |
| | bit coding | modified miller |
| | bit length | 128/f _c |
| PN7462 family to reader/writer | modulation on PN7462 family side | sub carrier load modulation |
| | subcarrier frequency | f _c / 16 |
| | bit coding | Manchester coding |

NFCIP-1 framing and coding

The NFCIP-1 framing and coding in active and passive communication mode is defined in the NFCIP-1 standard.

PN7462 family supports the following data rates:

Table 19. Framing and coding overview

| Transfer speed | Framing and coding |
|----------------|--|
| 106 kbit/s | according to the ISO/IEC 14443 A/MIFARE scheme |
| 212 kbit/s | according to the FeliCa scheme |
| 424 kbit/s | according to the FeliCa scheme |

NFCIP-1 protocol support

The NFCIP-1 protocol is not elaborated in this document. The PN7462 family component does not implement any of the high-level protocol functions. These high-level protocol functions are implemented in the microcontroller. For detailed explanation of the protocol, refer to the NFCIP-1 standard. However, the datalink layer is according to the following policy:

- Speed shall not be changed while there is continuous data exchange in a transaction.
- Transaction includes initialization, anticollision methods, and data exchange (in a continuous way means no interruption by another transaction).

In order not to disturb current infrastructure based on 13.56 MHz, the following general rules to start NFCIP-1 communication are defined:

1. By default, NFCIP-1 device is in target mode. It means that its RF field is switched off.
2. The RF level detector is active.
3. Only if the application requires, the NFCIP-1 device switches to initiator mode.
4. An initiator shall only switch on its RF field if the RF level detector does not detect external RF field during a time of T_{IDT} .
5. The initiator performs initialization according to the selected mode.

8.10.2 NFC interface

8.10.2.1 Transmitter (TX)

The transmitter is able to drive an antenna circuit connected to outputs TX1 and TX2 with a 13.56 MHz carrier signal. The signal delivered on pins TX1 and pin TX2 is a 13.56 MHz carrier, modulated by an envelope signal for energy and data transmission. It can be used to drive an antenna directly, using a few passive components for matching and filtering. For a differential antenna configuration, either TX1 or TX2 can be configured to put out an inverted clock.

100 % modulation and several levels of amplitude modulation on the carrier can be performed to support 13.56 MHz carrier-based RF-reader/writer protocols. The standards ISO/IEC14443 A and B, FeliCa, and ISO/IEC18092 define the protocols.

The PN7462 family embeds an overshoot and undershoot protection. It is used to configure additional signals on the transmitter output, for controlling the signal shape at the antenna output.

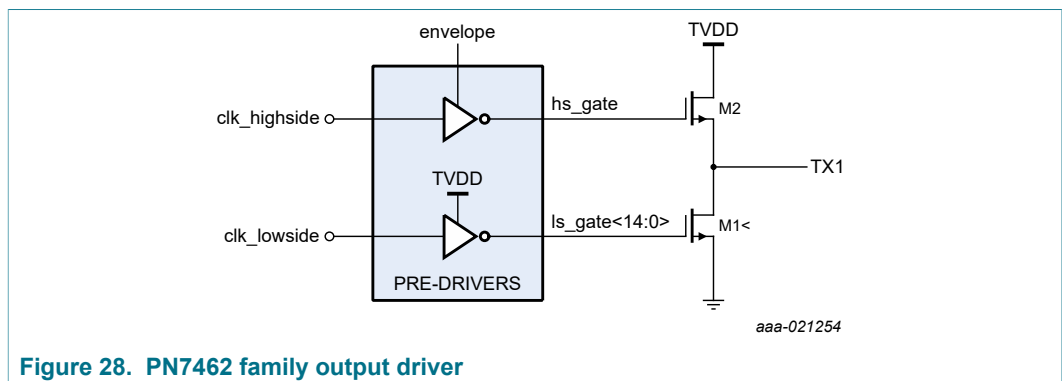


Figure 28. PN7462 family output driver

8.10.2.2 Receiver (RX)

In reader mode, the response of the PICC device is coupled from the PCB antenna to the differential input RXP/RXN. The reader mode receiver extracts this signal by first removing the carrier in passive mixers (direct conversion for I and Q). It then filters and amplifies the baseband signal before converting to digital values. The conversion to digital values is done with two separate ADCs, for I and Q channels. Both I and Q channels have a differential structure, which improves the signal quality.

The I/Q mixer mixes the differential input RF-signal down to the baseband. The mixer has a bandwidth of 2 MHz.

The down-mixed differential RX input signals are passed to the BBA and a band-pass filter. For considering all the protocols (type A/B, FeliCa), the high-pass cut-off frequency of BBA is configured between 45 kHz and 250 kHz. The configuration is done in four different steps. The low-pass cut-off frequency is greater than 2 MHz.

The output of band-pass filter is further amplified with a gain factor which is configurable between 30 dB and 60 dB. The baseband amplifier (BBA)/ADC I-channel and Q-channel can be enabled separately. It is required for ADC-based card mode functionality as only the I-channel is used in this case.

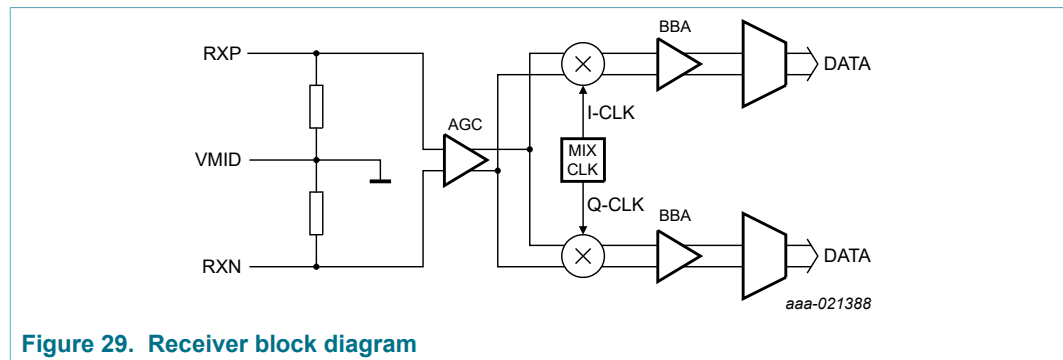


Figure 29. Receiver block diagram

VMID

A resistive divider between AVDD and GND generates VMID. The resistive divider is connected to the VMID pin. An external blocking capacitor of typical value 100 nF is connected.

Automatic Gain Control (AGC)

The NFC interface AGC is used to control the amplitude of 13.56 MHz sine-wave input signal received. The signal is received at the antenna connected between the pins RXP and RXN. A comparator is used to compare the peak value of the input signal with a reference voltage.

A voltage divider circuit is used to generate the reference voltage. An external resistor (typically 3.3 kΩ) is connected to the RX input, which forms a voltage divider with an on-chip variable resistor. The voltage divider circuit so formed has a 10-bit resolution.

Note: The comparator monitors the RXP signal only.

By varying the on-chip resistor, the amplitude of the input signal can be modified. The value of on-chip resistor is increased or decreased, depending on the output of the sampled comparator. The on-chip resistor value is adjusted until the peak of the input

signal matches the reference voltage. Thus, the AGC circuit automatically controls the amplitude of the RX input.

The internal amplitude controlling resistor in the AGC has a default value of 10 KΩ. It means that, when the resistor control bits in AGC_VALUE_REG <9:0> are all 0, the resistance is 10 KΩ. As the control bits are increased, resistors are switched in parallel to the 10 KΩ resistor. It lowers the resultant resistance value to 5 kΩ (AGC_VALUE_REG <9:0>, all bits set to 1).

Mode detector

The mode detector is a functional block of the PN7462 family which senses for an RF field generated by another device. The mode detector facilitates to distinguish between type A and FeliCa target mode. The host responds depending on the recognized protocol generated by an initiator peer device.

Note: The PN7462 family emulates type A cards and peer-to-peer active target modes according to ISO / IEC18092.

8.10.3 Low-Power Card Detection (LPCD)

The low-power card detection is an energy saving feature of the PN7462 family. It detects the presence of a card without starting a communication. Communication requires more energy to power the card and takes time, increasing the energy consumption.

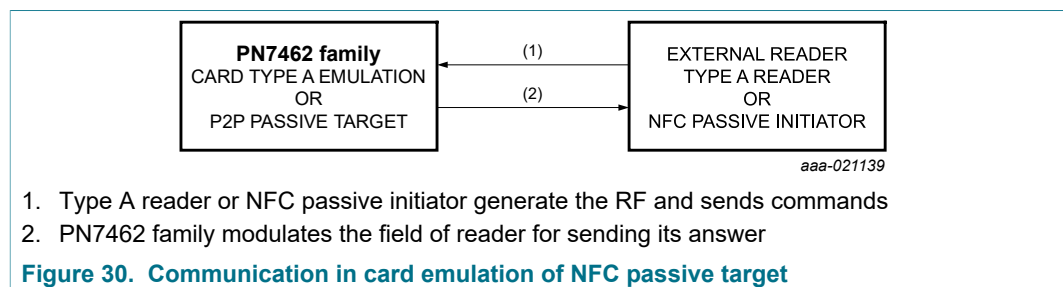
It is based on antenna detuning detection. When a card comes close to the reader, it affects the antenna tuning, which is detected by PN7462 family.

The sensitivity can be varied for adjusting to various environment and applications constraints.

Remark: Reader antenna detuning may have multiple sources such as cards and metal near the antenna. Hence it is important to adjust the sensitivity with care to optimize the detection and power consumption. As the generated field is limited, distance for card detection might be reduced compared to normal reader operation. Performances depend on the antenna and the sensitivity used.

8.10.4 Active Load Modulation (ALM)

When PN7462 family is used in card emulation mode or P2P passive target mode, it modulates the field emitted by the external reader or NFC passive initiator.



To modulate the field, PN7462 family offers two possibilities:

- **Passive Load Modulation (PLM):** The PN7462 family modifies the antenna characteristics, which are detected by the reader through antenna coupling.

- Active Load Modulation (ALM): The PN7462 family generates a small field, in phase opposition with the field emitted by the reader. This modulation is detected by the reader reception stage.

The modulation type to use depends on the external reader and the antenna of PN7462 family and the application.

8.10.5 Dynamic Power Control (DPC)

The PN7462 family supports the Dynamic Power Control (DPC) feature.

A lookup table is used to configure the output voltage and to control the transmitter current. In addition to the control of the transmitter current, wave shaping settings can be controlled as well, depending on the selected protocol and the measured antenna load.

8.10.5.1 RF output control

The DPC controls the RF output current and output voltage depending on the loading condition of the antenna.

8.10.5.2 Adaptive Waveform Control (AWC)

The DPC includes the Adaptive Waveform Control (AWC) feature.

Depending on the level of detected detuning on the antenna, RF wave shaping related register settings can be automatically updated, according to the selected protocol. A lookup table is used to configure the modulation index, the rise time and the fall time.

8.11 Timers

The PN7462 family includes two 12-bit general-purpose timers (on LFO clock domain) with match capabilities. It also includes two 32-bit general-purpose timers (on HFO clock domain) and a Watchdog Timer (WDT).

The timers and WDT can be configured through software via a 32-bit APB slave interface.

Table 20. Timer characteristics

| Name | Clock source | Frequency | Counter length | Resolution | Maximum delay | Chaining |
|----------|--------------|-----------|----------------|------------|---------------|----------|
| Timer 0 | LFO/2 | 182.5 kHz | 12 bit | 300 μs | 1.2 s | No |
| Timer 1 | LFO/2 | 182.5 kHz | 12 bit | 300 μs | 1.2 s | Yes |
| Timer 2 | HFO | 20 MHz | 32 bit | 50 ns | 214 s | No |
| Timer 3 | HFO | 20 MHz | 32 bit | 50 ns | 214 s | No |
| Watchdog | LFO/128 | 2.85 kHz | 10 bit | 21.5 ms | 22 s | No |

8.11.1 Features of timer 0 and timer 1

- 12-bit counters
- One match register per timer, no capture registers and capture trigger pins are needed
- One common output line gathering the four timers (Timer 0, Timer 1, Timer 2, and Timer 3)
- Interrupts

- Timer 0 and timer 1 can be concatenated (multiplied)
- Timer 0 and timer 1 have two count modes: single-shot or free-running
- Timer 0 and timer 1 timeout interrupts can be individually masked
- Timer 0 and timer 1 clock source is LFO clock ($LFO/2 = 182.5$ kHz)

Remark: The timers 0 and 1 are dedicated for NFC communication.

8.11.2 Features of timer 2 and timer 3

- 32-bit counters
- 1 match register per timer, no capture registers and capture trigger pins are needed
- 1 common output line gathering four timers (Timer 0, Timer 1, Timer 2, and Timer 3)
- Interrupts
- Timer 2 and timer 3 have two count modes: single-shot and free-running
- Timer 2 and timer 3 timeout interrupts can be individually masked
- Timer 2 and timer 3 clock source is the system clock

8.12 System tick timer

The PN7462 family microcontroller includes a standard Arm system tick timer (SYSTICK) that generates a dedicated SYSTICK exception.

8.13 Watchdog timer

If the microcontroller enters an erroneous state, the watchdog timer resets the microcontroller. When the watchdog timer is enabled, if the user program fails to "feed" (reload) the watchdog timer within a predetermined time, it generates a system reset.

The watchdog timer can be enabled through software. If there is a watchdog timeout leading to a system reset, the timer is disabled automatically.

- 10-bit counter
- Based on a 2.85 kHz clock
- Triggers an interrupt when a predefined counter value is reached
- Connected to the Arm subsystem NMI (non-maskable interrupt)
- If the watchdog timer is not periodically loaded, it resets PN7462 family

8.14 Clocks

The PN7462 family clocks are based on the following clock sources:

- 27.12 MHz external quartz
- 27.12 MHz crystal oscillator
- Internal oscillator: 20 MHz High Frequency Oscillator (HFO)
- Internal oscillator: 365 kHz Low Frequency Oscillator (LFO)
- Internal PLL at 48 MHz for the USB interface

[Figure 31](#) indicates the clocks used by each IP.

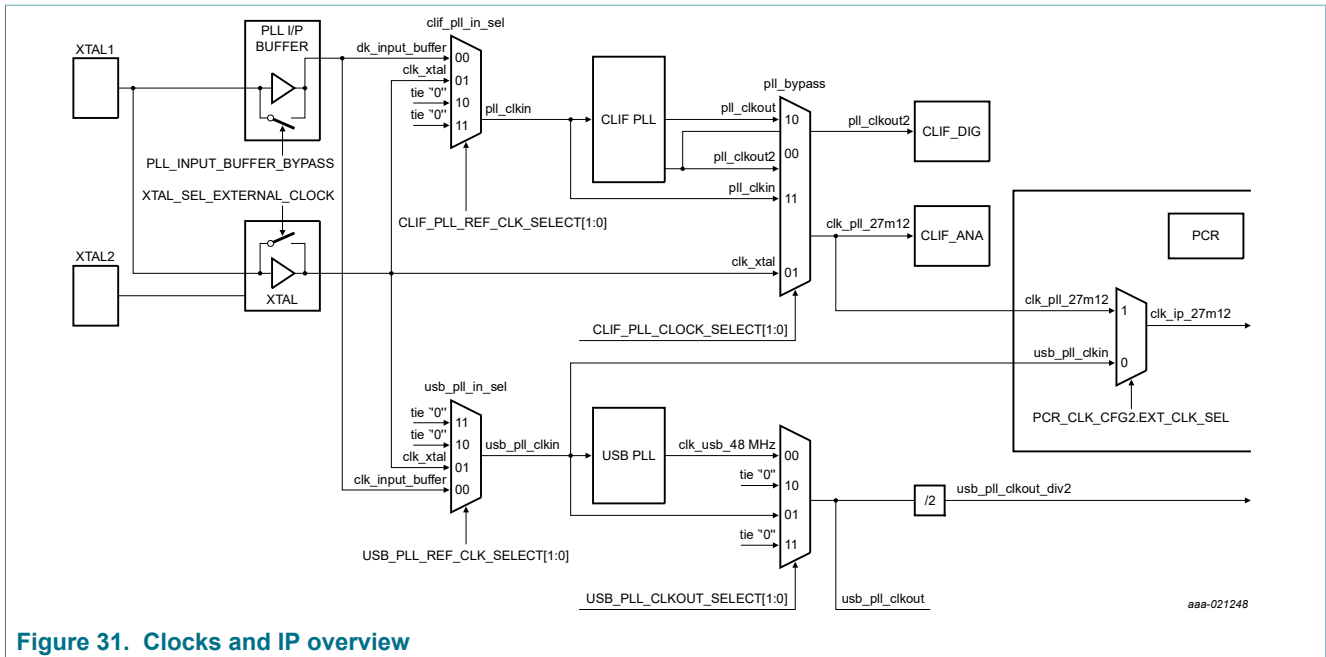


Figure 31. Clocks and IP overview

8.14.1 Crystal oscillator (27.12 MHz)

The 27.12 MHz quartz oscillator is used as a reference for all operations where the stability of the clock frequency is important for reliability. It includes contactless interface, SPI and I²C master interfaces, USB PLL for the USB interface, and HSUART.

Regular and low-power crystals can be used. Figure 32 shows the circuit for generating stable clock frequency. The quartz and trimming capacitors are off-chip.

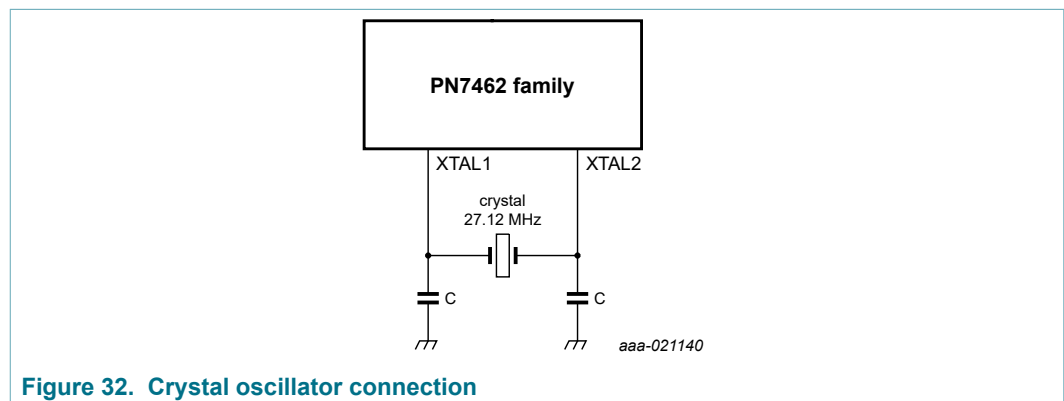


Figure 32. Crystal oscillator connection

Table 21 describes the levels of accuracy and stability required on the crystal.

Table 21. Crystal requirements

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------------|----------------------------|---------|-------|-----|----------|
| f_{xtal} | crystal frequency | ISO/IEC and FCC compliancy | - | 27.12 | - | MHz |
| Δf_{xtal} | crystal frequency accuracy | | [1] -50 | - | +50 | ppm |
| ESR | equivalent series resistance | | - | 50 | 100 | Ω |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|------------------|------------|-----|-----|-----|------|
| C _L | load capacitance | | - | 10 | - | pF |
| P _{drive} | drive power | | - | - | 100 | μW |

[1] This requirement is according to FCC regulations requirements. The frequency should be +/- 7 kHz.

8.14.2 USB PLL

The PN7462 family integrates a dedicated PLL to generate a low-noise 48 MHz clock, by using the 27.12 MHz from the external crystal. The 48 MHz clock generated is used as the USB main clock.

Following are the USB PLL features:

- Low-skew, peak-to-peak cycle-to-cycle jitter, 48 MHz output clock
- Low power in active mode, low power-down current
- On-chip loop filter, external RC components not needed

8.14.3 High Frequency Oscillator (HFO)

The PN7462 family has an internal low-power High Frequency Oscillator (HFO) that generates a 20 MHz clock. The HFO is used to generate the system clock. The system clock default value is 20 MHz, and it can be configured to 10 MHz and 5 MHz for reducing power consumption.

8.14.4 Low Frequency Oscillator (LFO)

The PN7462 family has an internal low-power Low Frequency Oscillator (LFO) that generates a 365 kHz clock. The LFO is used by EEPROM, POR sequencer, NFC interface, timers, and watchdog.

8.14.5 Clock configuration and clock gating

In order to reduce the overall power consumption, the PN7462 family facilitates adjustment of system clock. It integrates clock gating mechanisms.

The system clock can be configured to the following values: 20 MHz, 10 MHz, and 5 MHz.

The clock of the following blocks can be activated or deactivated, depending on the peripherals used:

- NFC interface
- Contact interface
- Host interfaces
- I²C master interface
- SPI master interface
- CRC engine
- Timers
- Random generator
- System clock
- EEPROM
- Flash memory

8.15 Power management

8.15.1 Power supply sources

The PN7462 family is powered using the following supply inputs:

- VBUS: main supply voltage for internal analog modules, digital logic, and memories
- VBUSP: supply voltage for the contact interface
- TVDD_IN: supply for the NFC interface
- PVDD_IN: pad voltage reference and supply of the host interface (HSU, USB, I²C, and SPI) and the GPIOs
PVDD_IN supply voltage is independent from VBUS supply level.
Note: Any digital IO pad (host interface, GPIO) must not be externally driven, when PVDD_IN supply voltage is absent.
- PVDD_M_IN: pad voltage reference and supply for the master interface (SPI and I²C)
Note: Any digital IO pad (master interface, IO_AUX) must not be externally driven, when PVDD_M_IN supply voltage is absent.
- DVDD: supply for the internal digital blocks

8.15.2 PN7462 Power Management Unit (PMU)

The integrated Power Management Unit (PMU) provides supply for internal analog modules, internal digital logic and memories, pads. It also provides supply voltages for the contactless and contact interface.

It automatically adjusts internal regulators to minimize power consumption during all possible power states.

The power management unit embeds a mechanism to prevent the IC from overheat, overconsumption, or overloading the DC-to-DC converter:

- TXLDO 5 V monitoring
- VCC current limiter
- DC-to-DC converter current overload
- SCVDD current overload
- Temperature sensor

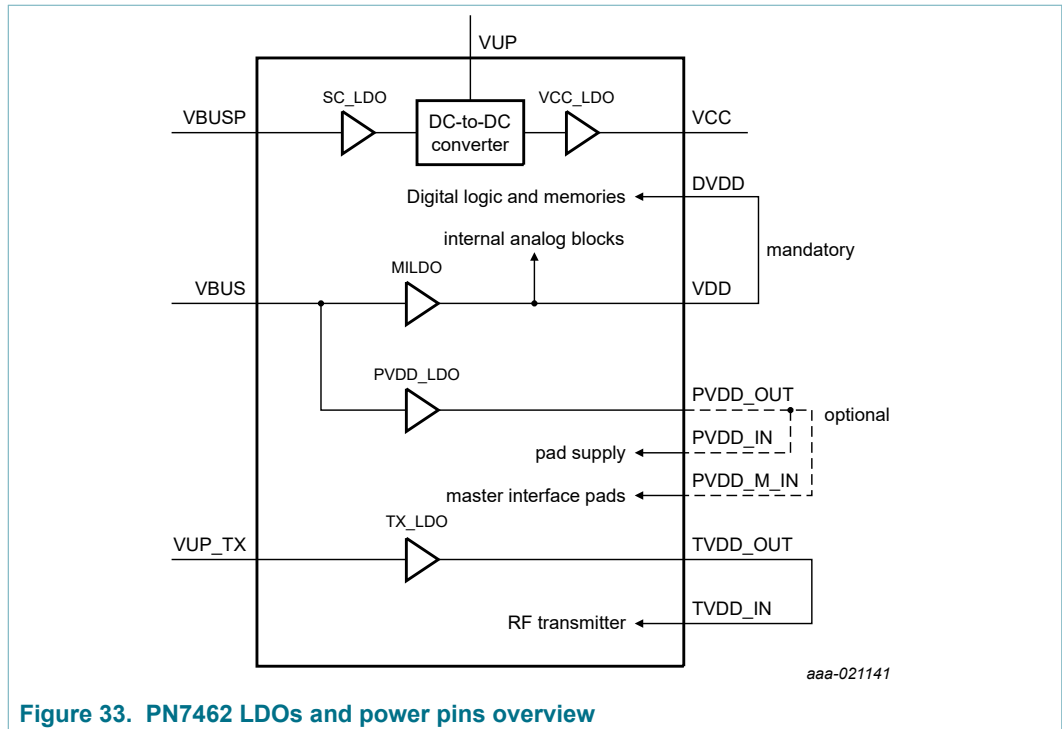


Figure 33. PN7462 LDOs and power pins overview

PN7462 embeds five Low Drop-Out regulators (LDO) for ensuring the stability of power supply, while the application is running.

- MLDO (main LDO): It provides 1.8 V supply for internal analog, digital and memory modules
- TXLDO: This LDO can be used to supply the RF transmitter
- PVDD_LDO: PVDD_LDO provides 3.3 V that can be used for all pads supply
- SCLDO: This LDO provides a 2.4 V output to be used for contact card supply. The main aim is to be able to address class B operation when the voltage available is below 3.9 V. It is achieved by providing a stable input voltage to the internal DC-to-DC converter.
- VCC_LDO: the VCC_LDO provides the supply for the contact smart card

Some are used while some are optional, like the TX_LDO which is proposed for the RF interface. It is up to the application designer to decide whether LDOs should be used.

8.15.2.1 Main LDO

The Main LDO (MLDO) provides a 1.8 V supply for all internal, digital and memory modules. It takes input from VBUS. MLDO includes a current limiter that avoids damage to the output transistors.

Output supply is available on VDD pin which must be connected externally to the DVDD pin.

Following are the main LDO features:

- Main Low-Drop-Out (MLDO) voltage regulator powered by VBUS (external supply)
- Current limiter to avoid damaging the output transistors

8.15.2.2 PVDD_LDO

The PVDD_LDO provides 3.3 V supply, that can be used for all digital pads. It may also be used to provide 3.3 V power to external components, avoiding an external LDO. It is supplied by VBUS, and requires a minimum voltage of 4 V to be functional. It delivers a maximum of 30 mA.

The output pin for PVDD_LDO is PVDD_OUT.

PVDD_LDO is used to provide the necessary supply to PVDD_IN and PVDD_M_IN (pad supply for master interfaces).

When an external supply is used, PVDD_OUT must be connected to the ground. When the LDO output is connected to the ground, the chip switches off the PVDD_LDO.

The PVDD_LDO has a low-power mode, which is used automatically when the chip is in standby mode or suspend mode. It facilitates supply to HOST pads and GPIOs, and to detect wake-up signals coming from these interfaces.

Following are the PVDD_LDO features:

- Low-Drop-Out voltage regulator powered by $V_{DDP(VBUS)}$ (external supply)
- Supports soft-start mode to limit inrush current during the initial charge of the external capacitance when the LDO is powered up
- Current limiter to avoid damaging the output transistors

Note: When PVDD_LDO is used, there must not be any load current drawn from PVDD_LDO during the soft start of the PVDD_LDO.

8.15.2.3 Contact interface - SCLDO LDO

The SCLDO provides a regulated voltage to the DC-to-DC converter, to enable class B operation when $V_{DDP(VBUS)}$ is in between 2.7 V to 3.9 V.

Following are the contact interface features:

- Current limiter for short circuit protection
- Supports soft-start mode to limit the inrush current during the initial charge of the external capacitance when the LDO is powered up

8.15.2.4 Contact interface DC-to-DC converter

The PN7462 includes a DC-to-DC converter that supports class A and class B cards, when the input voltage $V_{DDP(VBUSP)}$ is not sufficient.

The DC-to-DC converter is a capacitance voltage doubler. It takes power from the SCLDO. The DC-to-DC converter can be bypassed. Its output (VUP) is regulated between 3.3 V to 5.5 V.

The DC-to-DC converter can work in the following modes:

- Follower mode: This mode is used when $V_{DDP(VBUSP)}$ is high enough to provide the desired power to the VCC LDO
- Doubler mode: This mode is used when $V_{DDP(VBUSP)}$ is not high enough to supply the requested V_{CC} output

The doubler mode is used in the following conditions:

- Class A cards support
- Class B cards support, when $V_{DDP(VBUSP)}$ is less than 3.9 V

For class C cards, the DC-to-DC converter is always in a follower mode.

An external capacitor (470 nF) should be connected between SAM and SAP pins, to ensure the functioning of the DC-to-DC converter.

Table 22. SCLDO and DC-to-DC converter modes

| Supported card | $V_{DDP(VBUSP)}$ | SCLCO mode | DC-to-DC converter mode |
|----------------|--|---------------|-------------------------|
| Class A | > 3 V | follower mode | doubler mode |
| Class B | $2.7\text{ V} < V_{DDP(VBUSP)} < 3.9\text{ V}$ | LDO mode | doubler mode |
| Class B | > 3.9 V | follower mode | follower mode |
| Class C | > 2.7 V | follower mode | follower mode |

8.15.2.5 VCC LDO

The VCC LDO supplies contact interface supply V_{CC} .

Following are the VCC LDO features:

- Low drop-out voltage regulator
- Current limiter for chip and card protection
- Automatic deactivation in case of overload

8.15.2.6 TXLDO

The PN7462 family consists of an internal transmitter supply LDO. The TXLDO can be used to maintain a constant output voltage for the NFC interface.

The TXLDO is designed to protect the chip from voltage ripple introduced by the power supply on the pin VUP_TX. It is powered through the pin VUP_TX.

The programmable output voltages are: 3.0 V, 3.3 V, 3.6 V, 4.5 V, and 4.75 V.

For a given output voltage, VUP_TX shall always be higher than 0.3 V. In other words, to supply a 3 V output, the minimum voltage to be applied on VUP_TX is 3.3 V. If the voltage is not sufficient, then the voltage at the pin TVDD_OUT follows the voltage at the pin VUP_TX, lowered of 0.3 V.

When it is not used, TVDD_OUT shall be connected to TVDD_IN and VUP_TX, and TX_LDO shall be turned off. It must be ensured, that TVDD_IN and TVDD_OUT are never higher than VUP_TX.

Following are the TXLDO features:

- Low-Drop-Out (TXLDO) voltage regulator
- Supports soft-start mode to limit inrush current during the initial charge of the external capacitance
- Current limiter to avoid damaging the output transistors

8.15.3 PN736X Power Management Unit (PMU)

The integrated Power Management Unit (PMU) provides supply for internal analog modules, internal digital logic and memories, pads. It also provides supply voltages for the contactless interface.

It automatically adjusts internal regulators to minimize power consumption during all possible power states.

The power management unit embeds a mechanism to prevent the IC from overheat, overconsumption, or overloading the DC-to-DC converter:

- TXLDO 5 V monitoring
- Temperature sensor

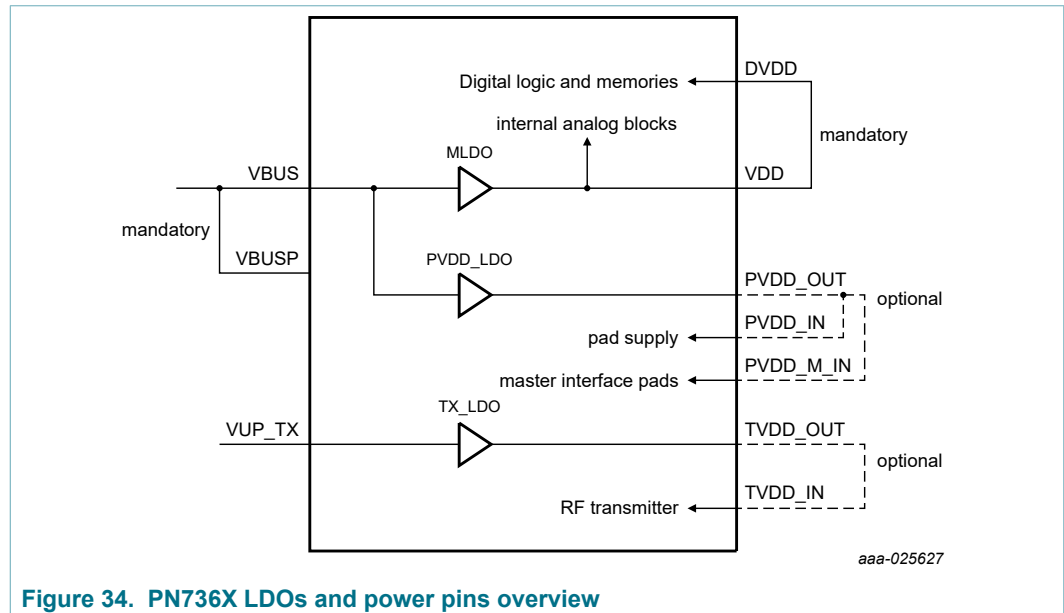


Figure 34. PN736X LDOs and power pins overview

PN736X embeds three Low Drop-Out regulators (LDO) for ensuring the stability of power supply, while the application is running.

- MLDO (main LDO): It provides 1.8 V supply for internal analog, digital and memory modules
- TXLDO: This LDO can be used to supply the RF transmitter
- PVDD_LDO: PVDD_LDO provides 3.3 V that can be used for all pads supply

Some are used while some are optional, like the TX_LDO which is proposed for the RF interface. It is up to the application designer to decide whether LDOs should be used.

8.15.3.1 Main LDO

The Main LDO (MLDO) provides a 1.8 V supply for all internal, digital and memory modules. It takes input from VBUS. MLDO includes a current limiter that avoids damage to the output transistors.

Output supply is available on VDD pin which must be connected externally to the DVDD pin.

Following are the main LDO features:

- Main Low-Drop-Out (MLDO) voltage regulator powered by VBUS (external supply)
- Current limiter to avoid damaging the output transistors

8.15.3.2 PVDD_LDO

The PVDD_LDO provides 3.3 V supply, that can be used for all digital pads. It may also be used to provide 3.3 V power to external components, avoiding an external LDO. It is supplied by VBUS, and requires a minimum voltage of 4 V to be functional. It delivers a maximum of 30 mA.

The output pin for PVDD_LDO is PVDD_OUT.

PVDD_LDO is used to provide the necessary supply to PVDD_IN and PVDD_M_IN (pad supply for master interfaces).

When an external supply is used, PVDD_OUT must be connected to the ground. When the LDO output is connected to the ground, the chip switches off the PVDD_LDO.

The PVDD_LDO has a low-power mode, which is used automatically when the chip is in standby mode or suspend mode. It facilitates supply to HOST pads and GPIOs, and to detect wake-up signals coming from these interfaces.

Following are the PVDD_LDO features:

- Low-Drop-Out voltage regulator powered by $V_{DDP(VBUS)}$ (external supply)
- Supports soft-start mode to limit inrush current during the initial charge of the external capacitance when the LDO is powered up
- Current limiter to avoid damaging the output transistors

Note: When PVDD_LDO is used, there must not be any load current drawn from PVDD_LDO during the soft start of the PVDD_LDO.

8.15.3.3 TXLDO

The PN7462 family consists of an internal transmitter supply LDO. The TXLDO can be used to maintain a constant output voltage for the NFC interface.

The TXLDO is designed to protect the chip from voltage ripple introduced by the power supply on the pin VUP_TX. It is powered through the pin VUP_TX.

The programmable output voltages are: 3.0 V, 3.3 V, 3.6 V, 4.5 V, and 4.75 V.

For a given output voltage, VUP_TX shall always be higher than 0.3 V. In other words, to supply a 3 V output, the minimum voltage to be applied on VUP_TX is 3.3 V. If the voltage is not sufficient, then the voltage at the pin TVDD_OUT follows the voltage at the pin VUP_TX, lowered of 0.3 V.

When it is not used, TVDD_OUT shall be connected to TVDD_IN and VUP_TX, and TX_LDO shall be turned off. It must be ensured, that TVDD_IN and TVDD_OUT are never higher than VUP_TX.

Following are the TXLDO features:

- Low-Drop-Out (TXLDO) voltage regulator
- Supports soft-start mode to limit inrush current during the initial charge of the external capacitance
- Current limiter to avoid damaging the output transistors

8.15.4 Power-up sequence

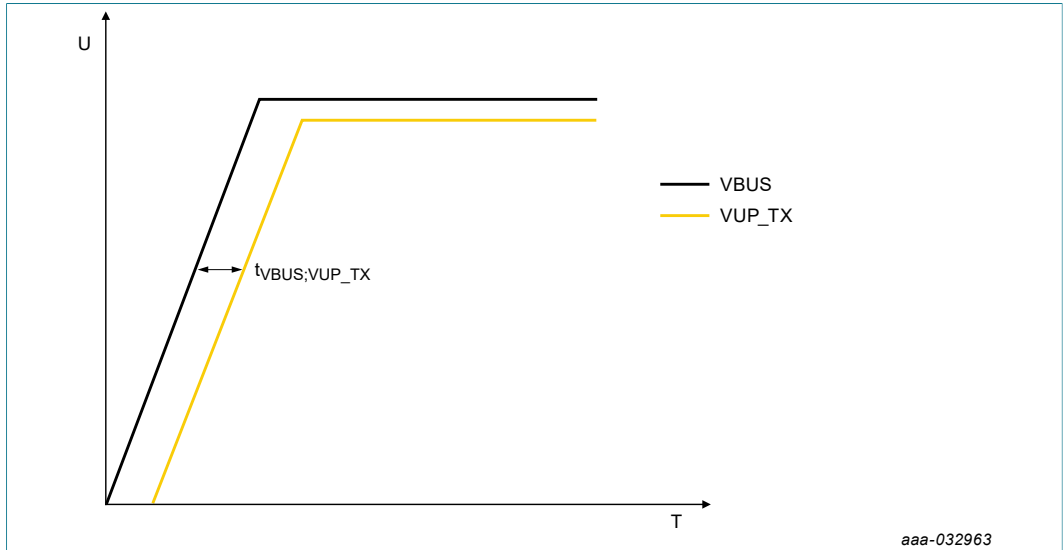


Figure 35. TX_LDO used

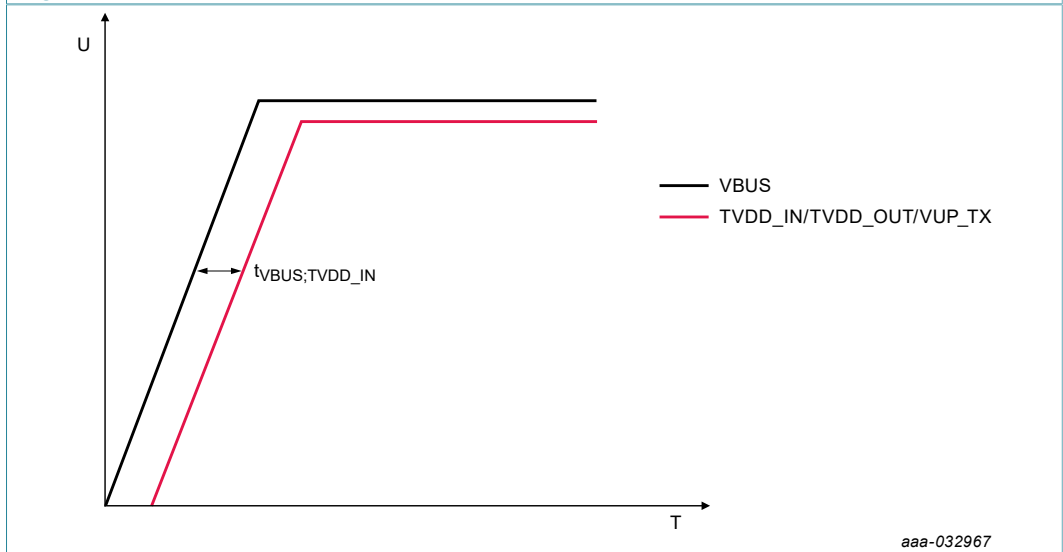


Figure 36. TX_LDO not used

Table 23. Power-up sequence

| Symbol | Min | Max | Description |
|---------------------|-----------|-----|--|
| $t_{VBUS;VUP_TX}$ | 0 μ s | - | VUP_TX must not be supplied before VBUS |
| $t_{VBUS;TVDD_IN}$ | 0 μ s | - | TVDD_IN must not be supplied before VBUS |

VUP_TX, TVDD_IN must never rise before VBUS at any time.

TVDD_IN shall be lower or equal to VUP_TX.

8.15.5 Power modes

The PN7462 family offers four different power modes, that enable the user to optimize its energy consumption. They are:

- Hard power-down mode
- Standby mode
- USB suspend mode
- Active mode

8.15.5.1 Active mode

In active mode, all functionalities are available and all IPs can be accessed. It is possible to configure the various clocks (IP clock, system clock) using register settings so that chip consumption is reduced. If IPs are not used, they can be disabled.

8.15.5.2 Standby mode

In standby mode, only a reduced part of the digital and the analog is active. It reduces the chip power consumption. The possible wake-up sources are still powered.

The LFO clock is used to lower the energy needs.

Active part in standby mode: Main LDO is active, in a low-power mode, plus all configured wake-up sources.

Depending on the application requirements, it is possible to configure PVDD_LDO in active mode, low-power mode or shut down mode when PN7462 family is going to standby mode. PVDD_LDO is active in a low-power mode by default.

Entering in standby mode: The application code triggers standby mode. Before entering in standby mode, the PN7462 manages the deactivation of the contact card.

The PN7462 family has two internal temperature sensors. If these sensors detect an overheat, the chip is put into standby mode by the application firmware. It leaves the standby mode when both temperature sensors indicate that the temperature has come below the configured limit.

Limitations: Standby mode is not possible in the following cases:

- A host communication is in progress.
- A wake-up condition is fulfilled. For example, external NFC field presence is a wake-up source, and a field is detected.
- The NFC field detector is a possible wake-up source, and the NFC field detector is disabled.
- PVDD is **not** present.

8.15.5.3 Suspend mode

In suspend mode, clock sources are stopped except LFO. It reduces the chip power consumption.

Entering in suspend mode: An interrupt indicates to the application firmware when no activity has been detected on the USB port for more than 3 ms. The application code triggers the suspend mode.

Before entering in suspend mode, the PN7462 manages automatically, the deactivation of the contact card.

Limitations: Suspend mode is prevented in the following cases:

- A host communication is in progress.
- A wake-up condition is fulfilled. For example, external RF field presence is a wake-up source, and a field is detected.

- The RF field detector is a possible wake-up source, and the RF field detector is disabled.
- No voltage at pin PVDD.

8.15.5.4 Wake-up from standby mode and suspend mode

PN7462 family can be woken-up from standby mode, and suspend mode, using the following means:

- Host Interface: SPI, HSUART, I²C, and USB if already selected before standby mode (SPI, HSUART, and I²C) or suspend mode (USB).
- RF field detection (presence of a reader or an NFC device in reader mode or P2P initiator)
- GPIO
- Contact card insertion, contact card removal (PN7462AUHN only)
- Interrupt generated on the auxiliary UART interface, through the interrupt pin (PN7462AUHN and PN7462AUEV only)
- Wake-up counter, for example to timely check for the presence of any contact or contactless card
- Current overconsumption on the PVDD_OUT, voltage above 5 V on TVDD_IN
- Temperature sensor: When the chip goes in to standby mode because of over-heating, and when the temperature goes below the sensor configured value, it wakes-up automatically. Each temperature sensor can be configured separately.

It is possible to configure the sources as enabled or disabled.

8.15.5.5 Hard Power-Down (HPD) mode

The Hard Power-Down (HPD) reduces the chip power consumption, by powering down most of its blocks. All clocks and LDOs are turned off, except the main LDO which is set in low-power mode.

Entering in HPD mode: If the RST_N pin is set to low, the NFC controller enters in to Hard Power Down (HPD) mode. It also enters in to HPD mode if the V_{DDP(VBUS)} goes below the critical voltage necessary for the chip to work (2.3 V) and the auto HPD feature is enabled.

Exiting the HPD mode: The NFC controller leaves the HPD mode, when both RST_N pin is set to high level and the V_{DDP(VBUS)} voltage is above 2.3 V.

8.15.6 Voltage monitoring

The voltage monitoring mode detects whether the voltage is within the operational conditions to enable a proper operation of the RF interface or the contact interface. The following power supplies are monitored: VBUS (two voltage monitors), VBUS_P (one voltage monitor).

[Section 9.1.2](#) discusses about the minimum voltages necessary for NFC interface operation and [Section 9.1.3](#) for the contact interface operation.

Table 24. Threshold configuration for voltage monitor

| Voltage monitor | Threshold 1 | Threshold 2 | Threshold 3 |
|-----------------|-------------|-------------|---------------------|
| VBUSMON1 | 2.3 V | 2.7 V | n.a. ^[1] |
| VBUSMON2 | 2.7 V | 4.0 V | n.a. ^[1] |

| Voltage monitor | Threshold 1 | Threshold 2 | Threshold 3 |
|-----------------|-------------|-------------|-------------|
| VBUSP | 2.7 V | 3.0 V | 3.9 V |

[1] n.a. means not applicable.

8.15.6.1 VBUS monitor

The PN7462 family includes up to two levels (2.3 V or 2.7 V) for monitoring the voltage on the VBUS pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the PCR. This signal may be enabled for interrupt in the interrupt enable register in the PCR, to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels (2.3 V or 2.7 V) can be selected to cause a forced Hard Power-Down (HPD) of chip.

8.15.6.2 VBUSP monitor

The PN7462 family includes three levels (2.7 V, 3.0 V, and 3.9 V) for monitoring the voltage on the VBUSP pin.

In addition to the above, the following applies to products with contact interface: When the voltage falls below the selected threshold value, and CT automatic deactivation is enabled in the PCR system register, hardware automatically de-activates the CT interface. An interrupt signal is also asserted to the PCR. This signal can be enabled for interrupt in the interrupt enable register in the PCR, to cause a CPU interrupt. Software must check VBUSP monitor levels by reading dedicated status registers before starting card activation sequence.

8.15.6.3 PVDD LDO supply monitor

The PN7462 family includes up to two levels (VBUSMON2: 2.7 V or 4.0 V) for monitoring the voltage on the PVDD LDO input supply. If supply voltage is 4.0 V or above, PVDD LDO can be enabled. The software has to check whether the voltage is sufficient before enabling the LDO.

8.15.7 Temperature sensor

The PN7462 family power management unit provides temperature sensors, associated to the TX_LDO. It detects problems that would result in high power consumption and heating, which could damage the chip and the user device.

Triggering levels are configurable. Following temperatures can be chosen: 135 °C, 130 °C, 125 °C, and 120 °C. By default, the temperature sensor is set to 120 °C.

Once the configured threshold is reached, an interrupt is generated. The application decides whether to enter standby or suspend mode. The triggering temperature sensor is indicated in the interrupt register.

Once the temperature goes below the configured threshold temperature, the NFC controller wakes up automatically.

8.16 System control

8.16.1 Reset

PN7462 family has six possible sources for reset. The list of sources is described in [Table 21](#).

Table 25. Reset sources

| Source | Description |
|----------------------------|---|
| software - PCR | soft reset from the PCR peripheral |
| software - Arm | software reset from the Arm processor |
| I ² C interface | I ² C Standard 3.0 defines a method to reset the chip via an I ² C command ^[1] |
| watchdog | reset the chip if the watchdog threshold is not periodically reloaded |
| VBUS voltage | power-on reset sequence; if the voltage is above 2.3 V, reset the chip |

[1] This feature can be disabled.

The watchdog reset, I²C reset and soft resets from PCR and Arm processor resets the chip except the PCR and the Arm debug interface. The Power-On Reset (POR) resets the complete chip including the PCR and Arm debug interface.

Upon reset, the processor executes the first instruction at address 0, which is initially the reset vector mapped from the boot block. At that point, all the processor and peripheral registers are initialized to predetermined values.

8.16.2 Brown-Out Detection (BOD)

The PN7462 family includes up to two levels for monitoring the voltage on the VBUS pin. If this voltage falls below one of the selected voltages (2.3 V or 2.7 V), the BOD asserts an interrupt signal to the PCR. This signal can be enabled for interrupt in the interrupt enable register in the PCR, to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Two threshold levels (2.3 V and 2.7 V) can be selected to cause a forced Hard Power-Down (HPD) of the chip.

8.16.3 APB interface and AHB-Lite

All APB peripherals are connected to one APB bus.

The AHB-Lite connects the AHB masters. The AHB masters include the CPU bus of the Arm Cortex-M0, host interface, NFC interface, SPI interface to the flash memory. It also includes EEPROM memory, SRAM, ROM, and AHB to APB bridge.

8.16.4 External interrupts

PN7462 family enables the use of 12 GPIOs as edge or level sensitive inputs (GPIO1 to GPIO12).

8.17 SWD debug interface

The Cortex-M0 processor-based devices use serial wire Arm CoreSight™ Debug technology. The PN7462 family is configured to support four break points and two watch points.

The SWD interface can be disabled for having code (or data) read/write access protection. A dedicated SWD disable bit is available in the protected area of the

EEPROM memory. Once the SWD interface is disabled, it is not possible to enable it anymore.

8.17.1 SWD interface features

- Run control of the processor allowing to start and stop programs
- Single step one source or assembler line
- Set breakpoints while the processor is running
- Read/write memory contents and peripheral registers on-the-fly
- "printf" like debug messages through the SWD interface

9 Application design-in information

9.1 Power supply connection

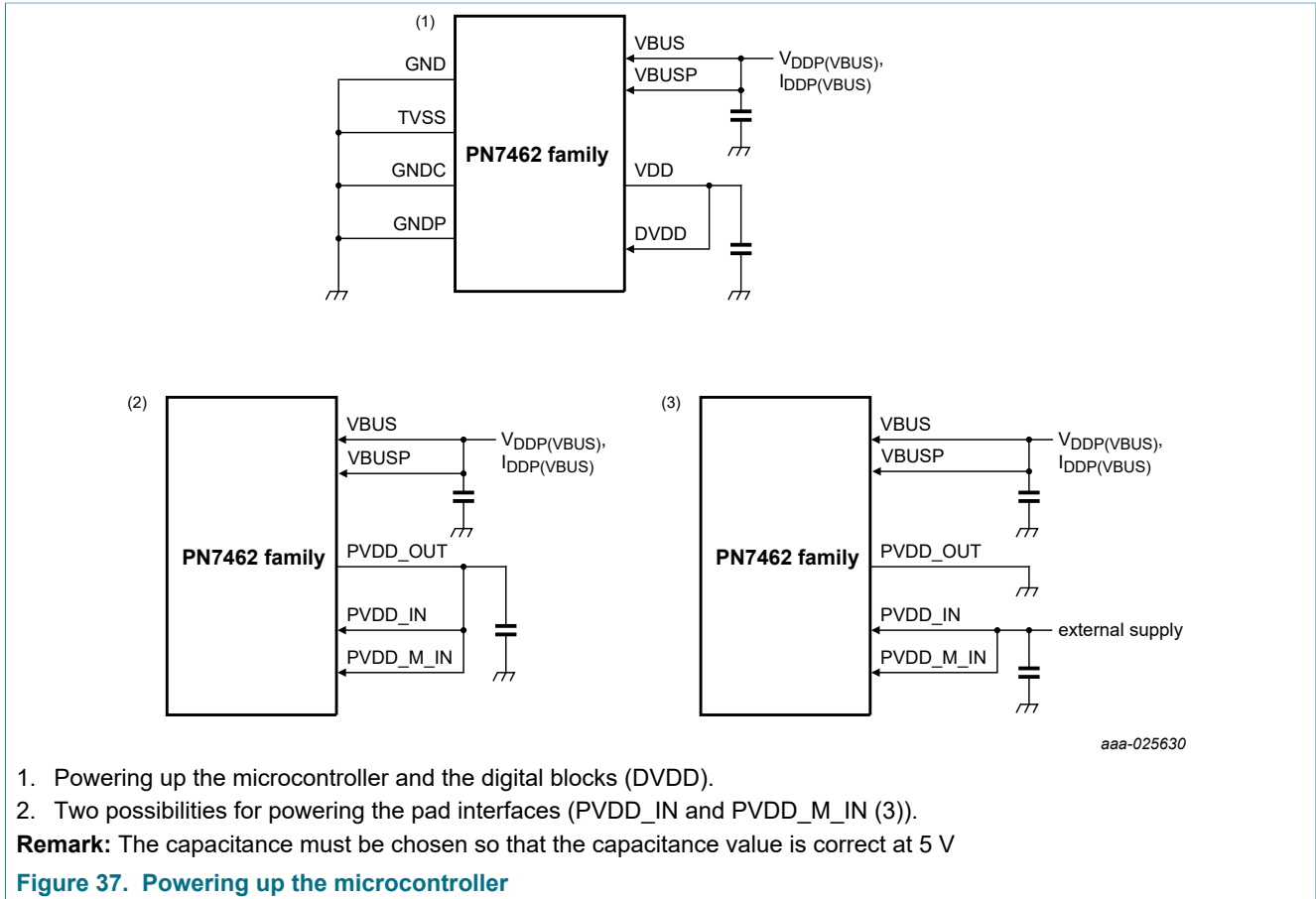
The following table indicates the power sources for all the PN7462 family power inputs.

Table 26. Power supply connection

| Power inputs | Power sources | Comment |
|--------------|---------------------------------------|---|
| VBUS | external source | |
| VBUSP | external source; connected to VBUS | VBUSP is connected to VBUS, with the addition of a decoupling capacitor |
| TVDD_IN | external supply or using the TX_LDO | |
| PVDD_IN | external supply or using PVDD_LDO | PVDD_LDO can be used, when $V_{DDP(VBUS)} > 4$ V. It makes a regulated 3.3 V supply available to GPIO and host interface pads, without the addition of an external LDO for 1.8 V, external supply has to be used |
| PVDD_M_IN | external supply or using PVDD_LDO | PVDD_LDO can be used, when $V_{DDP(VBUS)} > 4$ V. It makes a regulated 3.3 V supply available to GPIO and host interface pads, without the addition of an external LDO for 1.8 V, external supply has to be used |
| DVDD | connected to the VDD output | VDD provides 1.8 V stabilized supply, out of the MAIN_LDO |

Note: When PVDD_IN and PVDD_M_IN are externally supplied, PVDD_OUT must be connected to ground, with a ground resistance of less than 10 Ω .

9.1.1 Powering up the microcontroller



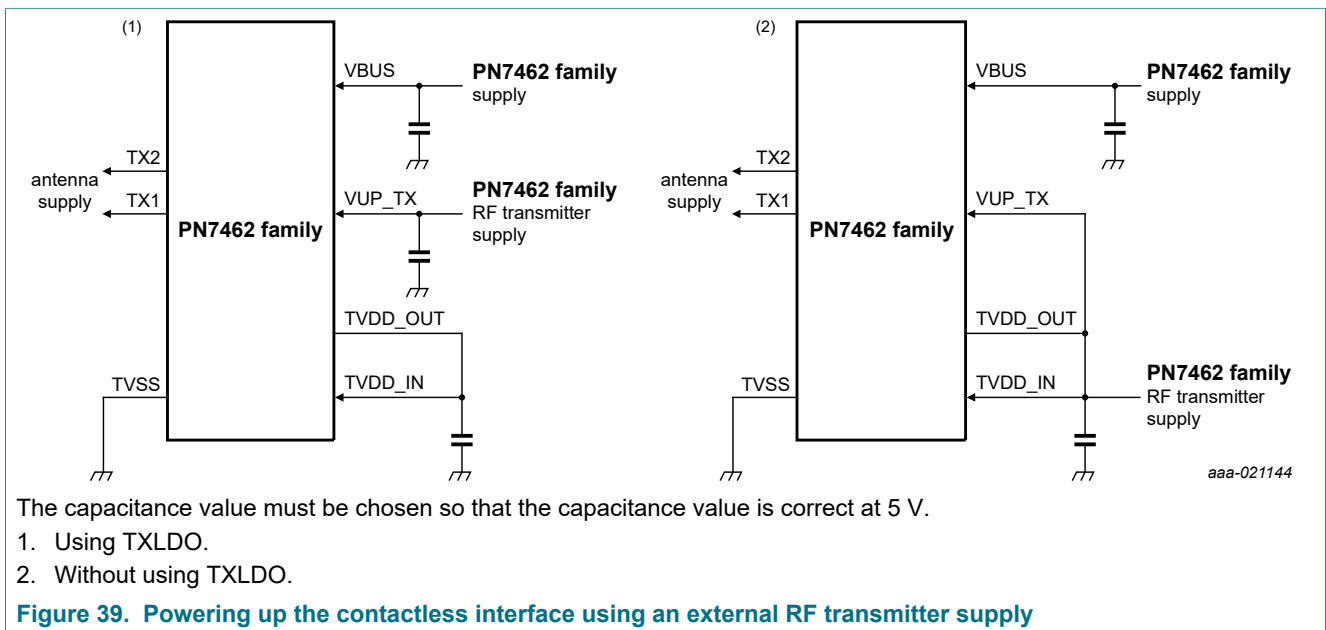
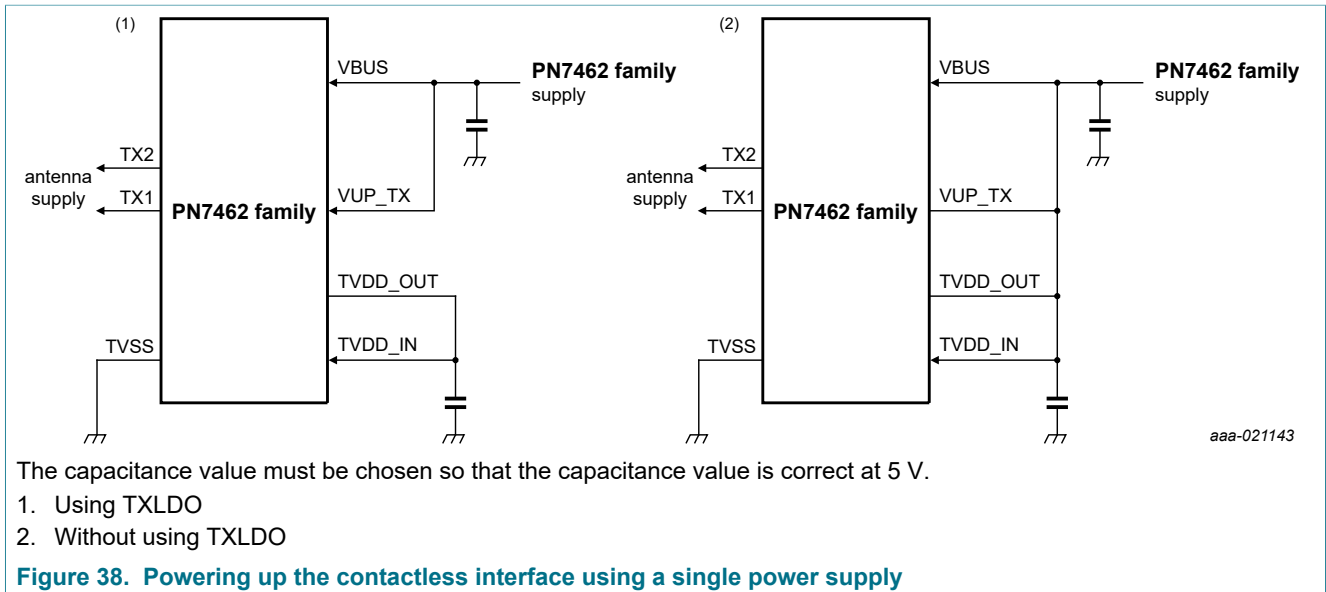
The schematics in [Figure 37](#) describe the power supply of the chip ($V_{DDP(VBUS)}$), including the digital blocks supply (DVDD). It indicates two possibilities to supply the pads, using the internal LDO, or using an external supply. The internal LDO requires that $V_{DDP(VBUS)} > 4\text{ V}$. It avoids the requirement of a separate LDO when $V_{DDP(VBUS)}$ has a sufficient voltage.

Power supply is available to pads through PVDD_IN (host interface). Similarly, power supply is available to master interface pads through PVDD_M_IN. When PVDD_LDO is used, maximum total current available from PVDD_OUT for the pads supply is 30 mA.

When an external source is used for PVDD_IN and PVDD_M_IN, PVDD_OUT must be connected to the ground, with a ground resistance of less than 10 Ω.

9.1.2 Powering up the contactless interface

Powering of contactless interface is done though TVDD_IN. Internal LDO (TXLDO) or external supply can be used.



Note: The TVDD_OUT pin must not be left floating. It should be at the same voltage as the TVDD_IN pin.

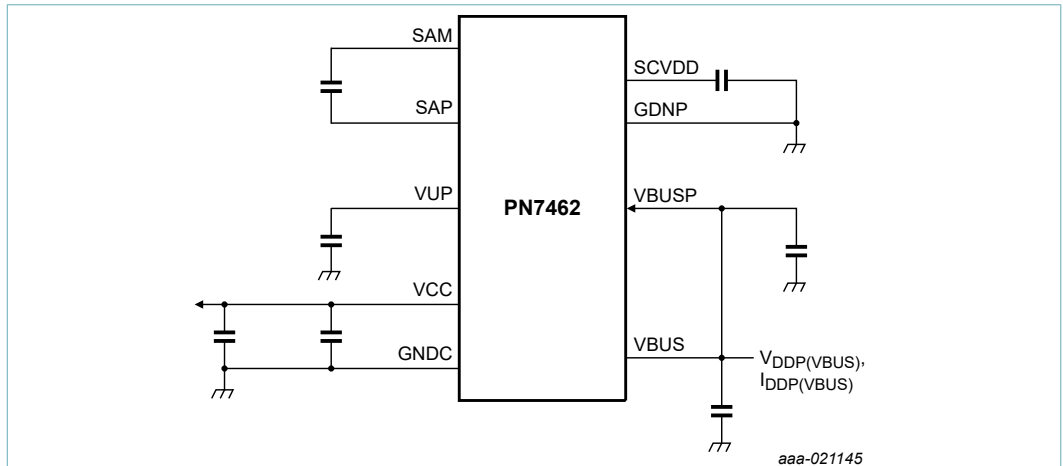
The power design must be designed properly to be able to deliver a clean power supply voltage.

In any case (external TVDD or internal TX_LDO internal supply), TVDD_IN supply must be stable before turning on the RF field. The capacitor shall be 6.8 μF or higher (up to 10 μF)

Every noise level on top of the supply voltage can disturb the RF communication performance of the PN7462 family. Therefore, special attention must be paid to the filtering circuit.

When powering up the device through the USB interface, TVDD capacitor value shall be chosen so that the maximum capacitance on VBUS remains as per the USB specification.

9.1.3 Powering up the contact interface



1. The capacitances values must be chosen so that the capacitance values are correct at 5.6 V.

Figure 40. Powering up the contact interface

Contact interface is powered through VBUSP. VBUSP must be connected to VBUS, as per the schematic in Figure 40.

In order to provide the right voltage needed for the various ISO/IEC 7816 contact card classes (A, B, or C), the following voltages are needed:

- $V_{DDP(VBUSP)} > 2.7\text{ V}$: Support of class B and class C contact cards
- $V_{DDP(VBUSP)} > 3\text{ V}$: Support of class A contact cards

Remark: To support class A cards, DC-to-DC converter is used. To support class B cards with $V_{DDP(VBUSP)} < 3.9\text{ V}$, DC-to-DC converter is used.

Figure 41 indicates the method to connect the pins related to contact interfaces, when no contact interface is used.

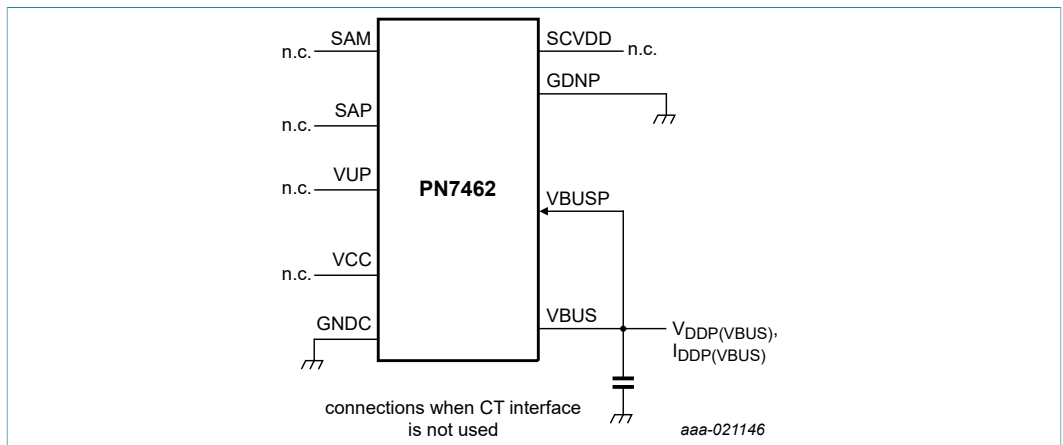


Figure 41. Contact interface power supply connection when contact interface is not used

9.2 Connecting the USB interface

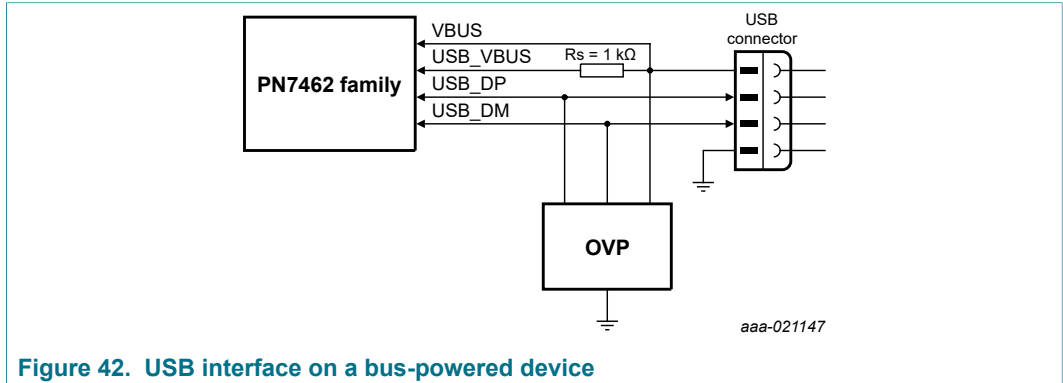
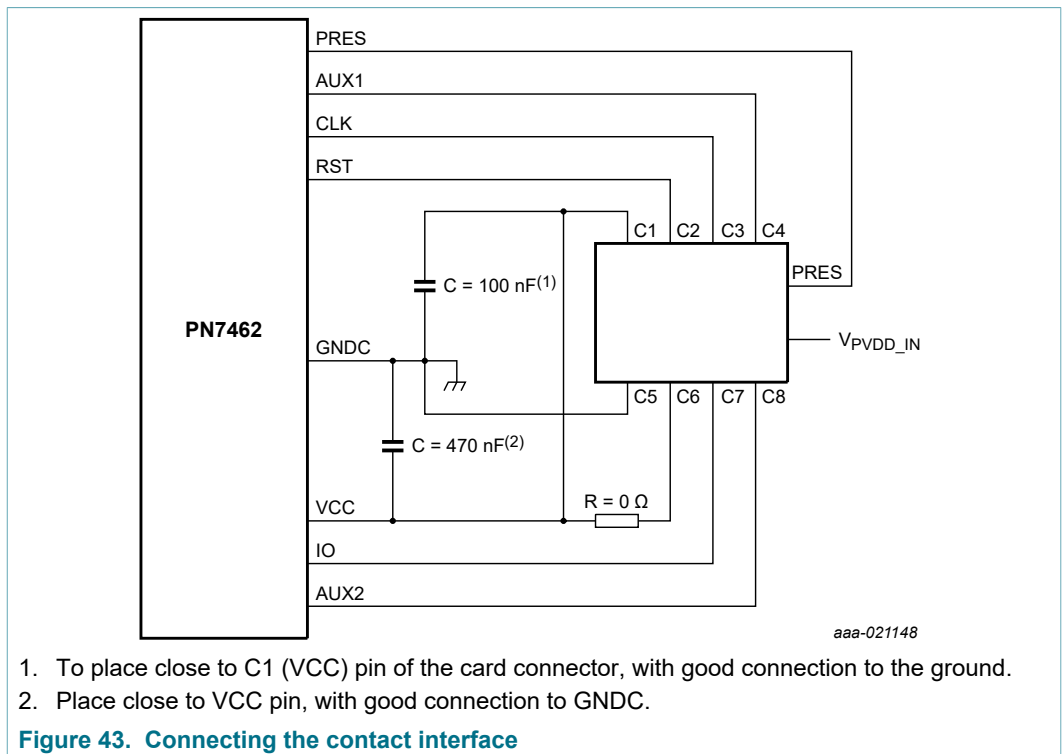


Figure 42. USB interface on a bus-powered device

The resistor R_s is used to minimize the impact of transient responses on the USB line. When the USB interface is not used, the USB_VBUS pin shall be connected to the ground.

9.3 Connecting the contact interface

The following diagrams indicate the method to connect the contact interface, when the contact interface is used, and when it is not used.



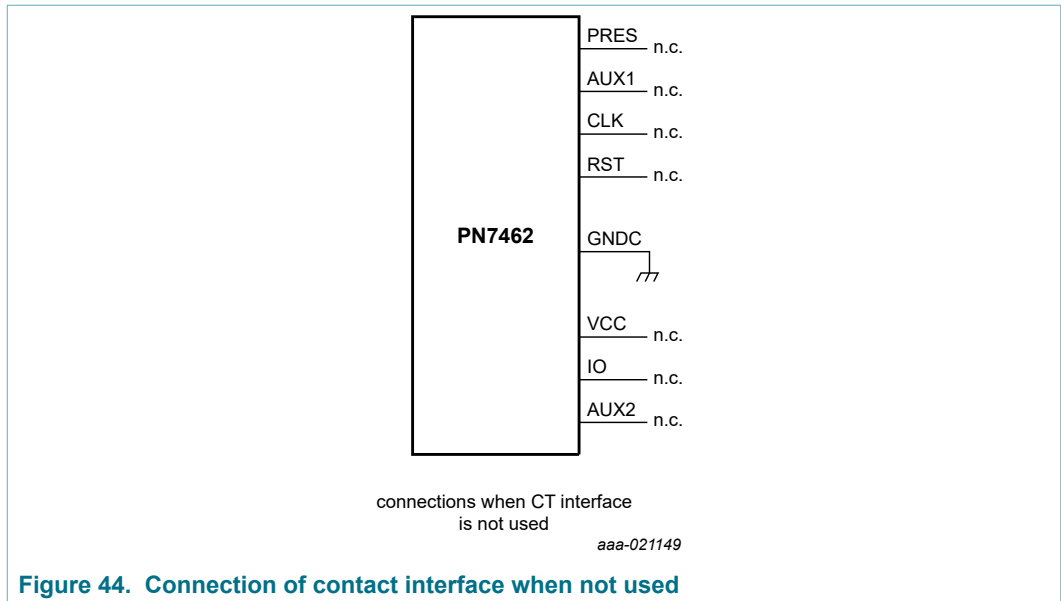


Figure 44. Connection of contact interface when not used

9.4 Connecting the RF interface

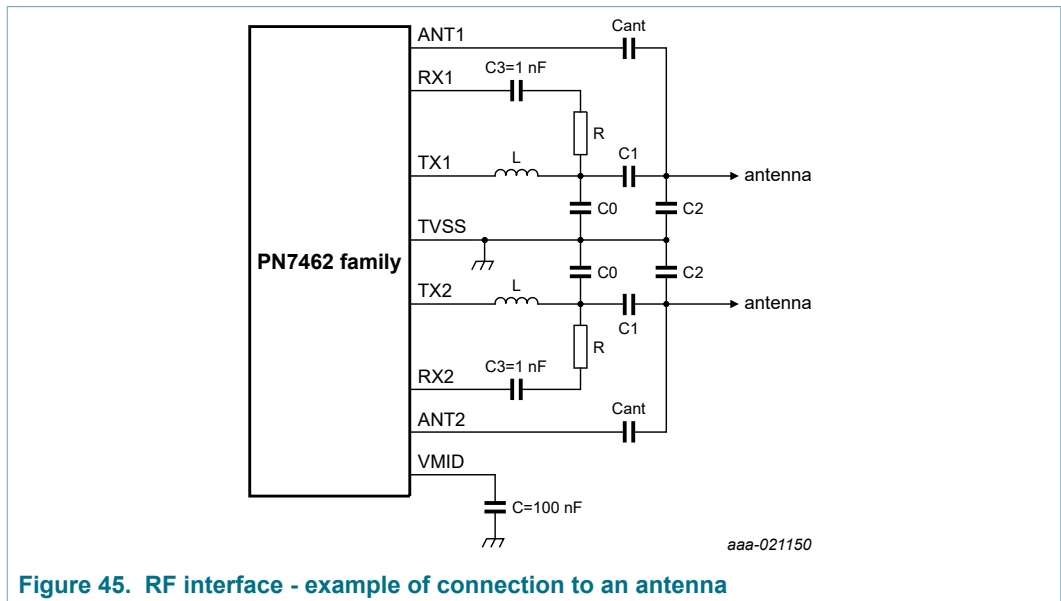


Figure 45. RF interface - example of connection to an antenna

9.5 Unconnected I/Os

When not used, the following pins need to be "not connected":

- I2C Master interface: I2CM_SDA, I2CM_SCL
- SPI Master interface: SPIM_SSN, SPIM_SCLK, SPIM_MOSI, SPIM_MISO
- AUX interface: INT_AUX, IO_AUX, CLK_AUX (PN7462 only)

Pads have to be configured in GPIO mode, pad input and output driver need to be disabled.

10 Limiting values

Table 27. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit | |
|---------------------|---------------------------------|---|-----|------|------|----|
| V _{ESD} | electrostatic discharge voltage | Human Body Model (HBM) | | | | |
| | | on card pins IO, RST, VCC, AUX1, CLK, AUX2, PRESN | [1] | -12 | +12 | kV |
| | | on all pins except contact interface pins | [1] | -2 | +2 | kV |
| | | Charged Device Model (CDM) | | | | |
| | | on all pins | [2] | -1 | +1 | kV |
| T _{stg} | storage temperature | non-operating | -55 | +150 | °C | |
| T _{j(max)} | maximum junction temperature | | - | +125 | °C | |
| P _{tot} | total power dissipation | reader mode; V _{DDP(VBUS)} = 5.5 V | - | 1050 | mW | |

[1] ANSI/ESDA/JEDEC JS-001

[2] ANSI/ESDA/JEDEC JS-002

Table 28. Limiting values for GPIO1 to GPIO12

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|---------------|------------|------|-----|------|
| V _i | input voltage | | -0.3 | 4.2 | V |

Table 29. Limiting values for I²C master pins (i2cm_sda, i2cm_scl)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|---------------|------------|------|-----|------|
| V _i | input voltage | | -0.3 | 4.2 | V |

Table 30. Limiting values for SPI master pins (spim_nss, spim_miso, spim_mosi and spi_clk)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|---------------|------------|------|-----|------|
| V _i | input voltage | | -0.3 | 4.2 | V |

Table 31. Limiting values for host interfaces atx_a, atx_b, atx_c, atx_d in all configurations (USB, HUART, SPI and I²C)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------|---------------|------------|------|-----|------|
| V _i | input voltage | | -0.3 | 4.2 | V |

Table 32. Limiting values for crystal oscillator

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|--------------------------|--------------|-----|-----|------|
| V _{IH} | high-level input voltage | XTAL1, XTAL2 | 0 | 2.2 | V |

Table 33. Limiting values for power supply

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|-----------------------------------|--|---------------------|-----|------|
| V _{DDP(VBUS)} | power supply voltage on pin VBUS | | ^[1] -0.3 | 7 | V |
| V _{DDP(VBUSP)} | power supply voltage on pin VBUSP | | ^[1] -0.3 | 7 | V |
| pin supply voltage for host interface and GPIOs (on pin PVDD_IN) | | | | | |
| V _{DD(PVDD)} | PVDD supply voltage | on pin PVDD_IN; power supply for host interfaces and GPIOs | ^[1] -0.3 | 4.2 | V |
| pin supply voltage for master interfaces (on pin PVDD_M_IN) | | | | | |
| V _{DD(PVDD)} | PVDD supply voltage | on pin PVDD_M_IN; power supply for master interfaces | ^[1] -0.3 | 4.2 | V |
| RF interface LDO (pin VUP_TX) | | | | | |
| V _{I(LDO)} | LDO input voltage | for RF interface LDO | ^[1] -0.3 | 7 | V |
| RF transmitter (pin TVDD_IN) | | | | | |
| V _{DD(TVDD)} | TVDD supply voltage | for RF interface transmitter | ^[1] -0.3 | 6 | V |

[1] Maximum/minimum voltage above the maximum operating range and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter life time of the device.

Table 34. Limiting values for contact interface

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|--------------------------|---------------------------------------|------|------|------|
| V _{IH} | high-level input voltage | on card pins IO, RST, AUX1, AUX2, CLK | -0.3 | 5.75 | V |

Table 35. Protection and limitations for contact interface

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|------------------------------------|--|-----|-----|-----|------|
| I _{Olim} | output current limit on IO, C4, C8 | class A, B, C | 5 | 8 | 15 | mA |
| I _{sd} | shutdown current | on pin V _{CC} = 5 V | 70 | 85 | 110 | mA |
| | | on pin V _{CC} = 3 V (doubler mode) | 75 | 90 | 110 | mA |
| | | on pin V _{CC} = 3 V (follower mode) | 75 | 90 | 110 | mA |
| | | on pin V _{CC} = 1.8 V | 60 | 70 | 90 | mA |

Table 36. Limiting values for RF interface

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|---------------|---------------------|-----|-----|------|
| V_i | input voltage | on pins RXN and RXP | 0 | 2.2 | V |

1. Maximum/minimum voltage above the maximum operating range and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter life time of the device.

Table 37. Limiting values for USB interface

| Symbol | Parameter | Conditions | Min | Max | Unit |
|----------------------|-------------------------|------------|------|-----|------|
| $V_{DDP(USB_VBUS)}$ | Voltage on pin USB_VBUS | [1] | -0.3 | 7 | V |

- [1] Maximum/minimum voltage above the maximum operating range and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter life time of the device.

11 Recommended operating conditions

Table 38. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|-----------------------------------|---|------|-----|------|------|
| T_{amb} | ambient temperature | JDEC PCB - 0.5 | -40 | 25 | 85 | °C |
| $V_{DDP}(VBUS)$ | power supply voltage on pin VBUS | external PVDD supply, card emulation and passive target (PLM) | 2.3 | - | 5.5 | V |
| | | external PVDD supply, reader mode, NFC initiator and passive/active target mode (ALM and PLM) | 2.7 | - | 5.5 | V |
| | | internal PVDD_LDO supply, reader mode, NFC initiator and passive/active target mode (ALM and PLM) | 4 | - | 5.5 | V |
| $V_{DDP}(VBUSP)$ | power supply voltage on pin VBUSP | class B and class C contact card | 2.7 | - | 5.5 | V |
| | | class A, class B, and class C contact card | 3 | - | 5.5 | V |
| host interface and GPIOs pin power supply (pin PVDD_IN) | | | | | | |
| $V_{DD}(PVDD)$ | PVDD supply voltage | for digital pins | | | | |
| | | 1.8 V pin supply | 1.65 | 1.8 | 1.95 | V |
| | | 3.3 V pin supply | 3 | 3.3 | 3.6 | V |
| SPI master and I²C master interfaces pin power supply (on pin PVDD_M_IN) | | | | | | |
| $V_{DD}(PVDD)$ | PVDD supply voltage | for master pins | | | | |
| | | 1.8 V pin supply | 1.65 | 1.8 | 1.95 | V |
| | | 3.3 V pin supply | 3 | 3.3 | 3.6 | V |
| RF interface LDO (pin VUP_TX) | | | | | | |
| $V_{I(LDO)}$ | LDO input voltage | TX_LDO supply for powering up RF interface | 3 | 5 | 5.5 | V |
| RF interface transmitter | | | | | | |
| $I_{DD}(TVDD)$ | TVDD supply current | on pin TVDD_IN | - | - | 250 | mA |

12 Thermal characteristics

Table 39. Thermal characteristics

| Symbol | Parameter | Conditions | Typical VFPGA64 package | Typical HVQFN64 package | Unit |
|----------------|---|---|-------------------------|-------------------------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air with exposed pad soldered on a four-layer JEDEC PCB | 53.4 | 40.0 | °K/W |
| Ψ_{j-top} | thermal characterization parameter from junction to top | not dependent on PCB | 11.2 | 5.75 | °K/W |

13 Characteristics

13.1 Static characteristics

Table 40. Static characteristics for RST_N input pin

Data are given for $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|-----------------------|-----|-----|-----------------|---------------|
| V_{IH} | high-level input voltage | | 1.1 | - | $V_{DDP(VBUS)}$ | V |
| V_{IL} | low-level input voltage | | 0 | - | 0.4 | V |
| I_{IH} | high-level input current | $V_i = V_{DDP(VBUS)}$ | - | - | 1 | μA |
| I_{IL} | low-level input current | $V_i = 0\text{ V}$ | -1 | - | - | μA |
| C_{in} | input capacitance | | - | 5 | - | pF |

Table 41. Static characteristics for IRQ output pin

Data are given for $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|-------------------------------------|----------------------|-----|----------------|------------|
| V_{OH} | high-level output voltage | $I_{OH} < 3\text{ mA}$ | $V_{PVDD_IN} - 0.4$ | - | V_{PVDD_IN} | V |
| V_{OL} | low-level output voltage | $I_{OL} < 3\text{ mA}$ | 0 | - | 0.4 | V |
| C_L | load capacitance | | - | - | 20 | pF |
| $R_{pull-down}$ | extra pull-down | extra pull-down is activated in HDP | 0.45 | - | 0.8 | M Ω |

Table 42. Static characteristics for DWL_REQ

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|-------------------------------|----------------------------|-----|----------------------------|---------------|
| V_{IH} | high-level input voltage | $V_{PVDD_IN} = 1.8\text{ V}$ | $0.65 \times V_{PVDD_IN}$ | - | - | V |
| V_{IL} | high-level input voltage | $V_{PVDD_IN} = 1.8\text{ V}$ | - | - | $0.35 \times V_{PVDD_IN}$ | V |
| V_{IH} | high-level input voltage | $V_{PVDD_IN} = 3.3\text{ V}$ | 2 | - | - | V |
| V_{IL} | high-level input voltage | $V_{PVDD_IN} = 3.3\text{ V}$ | - | - | 0.8 | V |
| I_{IH} | high-level input current | $V_i = PVDD_IN$ | - | - | 1 | μA |
| I_{IL} | low-level input current | $V_i = 0\text{ V}$ | -1 | - | - | μA |
| C_L | load capacitance | | - | 5 | - | pF |

13.1.1 GPIO static characteristics

Table 43. Static characteristics for GPIO1 to GPIO21

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|-----------------------------------|---|----------------------------|-----|----------------------------|---------------|
| V_{OH} | high-level output voltage | $I_{OH} < 3 \text{ mA}$ | $V_{PVDD_IN} - 0.4$ | - | V_{PVDD_IN} | V |
| V_{OL} | low-level output voltage | $I_{OH} < 3 \text{ mA}$ | 0 | - | 0.4 | V |
| V_{IH} | high-level input voltage | $V_{PVDD_IN} = 3.3 \text{ V}$ | 2 | - | - | V |
| | | $V_{PVDD_IN} = 1.8 \text{ V}$ | $0.65 \times V_{PVDD_IN}$ | - | - | V |
| V_{IL} | low-level input voltage | $V_{PVDD_IN} = 3.3 \text{ V}$ | - | - | 0.8 | V |
| | | $V_{PVDD_IN} = 1.8 \text{ V}$ | - | - | $0.35 \times V_{PVDD_IN}$ | V |
| V_{hys} | hysteresis voltage | $V_{PVDD_IN} = 1.8 \text{ V}$ and $V_{PVDD_IN} = 3.3 \text{ V}$ | $0.1 \times V_{PVDD_IN}$ | - | - | V |
| I_{OZ} | OFF-state output current | $V_O = 0 \text{ V}$; $V_O = V_{PVDD_IN}$; on-chip pull-up/pull-down resistors disabled | - | - | 1000 | nA |
| R_{pd} | pull-down resistance | $V_{PVDD_IN} = 3.3 \text{ V}$ | 65 | 90 | 120 | k Ω |
| | | $V_{PVDD_IN} = 1.8 \text{ V}$ | 65 | 90 | 120 | k Ω |
| R_{pu} | pull-up resistance | $V_{PVDD_IN} = 3.3 \text{ V}$ | 65 | 90 | 120 | k Ω |
| | | $V_{PVDD_IN} = 1.8 \text{ V}$ | 65 | 90 | 120 | k Ω |
| I_{OSH} | short circuit current output high | Drive high; cell connected to ground; $V_{PVDD_IN} = 3.3 \text{ V}$ | - | - | 58 | mA |
| | | Drive low; cell connected to $PVDD_IN$; $V_{PVDD_IN} = 1.8 \text{ V}$ | - | - | 30 | mA |
| I_{OSL} | short circuit current output low | $V_{OH} = V_{PVDD_IN} = 3.3 \text{ V}$ | - | - | 54 | mA |
| | | $V_{OH} = V_{PVDD_IN} = 1.8 \text{ V}$ | - | - | 37 | mA |
| I_{IL} | low-level input current | $V_I = 0 \text{ V}$ | -1 | - | - | μA |
| I_{IH} | high-level input current | $V_I = V_{PVDD_IN}$ | - | - | 1 | μA |
| I_{OH} | high-level output current | $V_{OH} = V_{PVDD_IN}$ | - | - | 3 | mA |
| I_{OL} | low-level output current | $V_{OL} = 0 \text{ V}$ | - | - | 3 | mA |

13.1.2 Static characteristics for I²C master

Table 44. Static characteristics for I²CM_SDA, I²CM_SCL - S

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|---|------------------------------|-----|------------------------------|------|
| V _{OH} | high-level output voltage | I _{OH} < 3 mA | 0.7 × V _{PVDD_M_IN} | - | V _{PVDD_M_IN} | V |
| V _{OL} | low-level output voltage | I _{OL} < 3 mA | 0 | - | 0.4 | V |
| C _L | load capacitance | | - | - | 10 | pF |
| V _{IH} | High-level input voltage | | 0.7 × V _{PVDD_M_IN} | - | - | V |
| V _{IL} | low-level input voltage | | - | - | 0.3 × V _{PVDD_M_IN} | V |
| I _{IH} | high-level input current | V _i = V _{PVDD_M_IN} | - | - | 1 | μA |
| I _{IL} | low-level input current | V _i = 0 V | -1 | - | - | μA |
| C _{in} | input capacitance | | - | 5 | - | pF |

13.1.3 Static characteristics for SPI master

Table 45. Static characteristics for SPIM_MOSI

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|------------------------|------------------------------|-----|------------------------|------|
| V _{OH} | high-level output voltage | I _{OH} < 3 mA | V _{PVDD_M_IN} - 0.4 | - | V _{PVDD_M_IN} | V |
| V _{OL} | low-level output voltage | I _{OL} < 3 mA | 0 | - | 0.4 | V |
| C _L | load Capacitance | | - | - | 20 | pF |

Table 46. Static characteristics for SPIM_NSS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|------------------------|------------------------------|-----|------------------------|------|
| V _{OH} | high-level output voltage | I _{OH} < 3 mA | V _{PVDD_M_IN} - 0.4 | - | V _{PVDD_M_IN} | V |
| V _{OL} | low-level output voltage | I _{OL} < 3 mA | 0 | - | 0.4 | V |
| C _L | load Capacitance | | - | - | 20 | pF |

Table 47. Static characteristics for SPIM_MISO

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------------|---|-------------------------------|-----|-------------------------------|------|
| V _{IH} | high-level input voltage | V _{PVDD_M_IN} = 1.8 V | 0.65 × V _{PVDD_M_IN} | - | - | V |
| V _{IL} | low-level input voltage | V _{PVDD_M_IN} = 1.8 V | - | - | 0.35 × V _{PVDD_M_IN} | V |
| V _{IH} | high-level input voltage | V _{PVDD_M_IN} = 3.3 V | 2 | - | - | V |
| V _{IL} | low-level input voltage | V _{PVDD_M_IN} = 3.3 V | - | - | 0.8 | V |
| I _{IH} | high-level input current | V _i = V _{PVDD_M_IN} | - | - | 1 | μA |
| I _{IL} | low-level input current | V _i = 0 V | -1 | - | - | μA |
| C _{in} | input capacitance | | - | 5 | - | pF |

Table 48. Static characteristics for SPI_SCLK

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|------------------------|------------------------------|-----|------------------------|------|
| V _{OH} | high-level output voltage | I _{OH} < 3 mA | V _{PVDD_M_IN} - 0.4 | - | V _{PVDD_M_IN} | V |
| V _{OL} | low-level output voltage | I _{OL} < 3 mA | 0 | - | 0.4 | V |
| C _L | load capacitance | | - | - | 20 | pF |

13.1.4 Static characteristics for host interface

Table 49. Static characteristics for ATX_ used as SPI_NSS, ATX_ used as I²CADR0, ATX_ used as SPI_SCK, ATX_ used as SPI_MOSI

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------------|---------------------------------------|-------------------------------|-----|-------------------------------|------|
| V _{IH} | high-level input voltage | V _{PVDD_IN} = 1.8 V | 0.65 × V _{PVDD_M_IN} | - | - | V |
| V _{IL} | low-level input voltage | V _{PVDD_IN} = 1.8 V | - | - | 0.35 × V _{PVDD_M_IN} | V |
| V _{IH} | high-level input voltage | V _{PVDD_IN} = 3.3 V | 2 | - | - | V |
| V _{IL} | low-level input voltage | V _{PVDD_IN} = 3.3 V | - | - | 0.8 | V |
| I _{IH} | high-level input current | V _i = V _{PVDD_IN} | - | - | 1 | μA |
| I _{IL} | low-level input current | V _i = 0 V | -1 | - | - | μA |
| C _{in} | input capacitance | | - | 5 | - | pF |

Table 50. Static characteristics of ATX_ used as I²CSDA, ATX_ used as I²CSCL

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|---------------------------------------|----------------------------|-----|----------------------------|------|
| V _{OH} | high-level output voltage | I _{OH} < 3 mA | 0.7 × V _{PVDD_IN} | - | V _{PVDD_IN} | V |
| V _{OL} | low-level output voltage | I _{OL} < 3 mA | 0 | - | 0.4 | V |
| C _L | load capacitance | | - | - | 10 | pF |
| V _{IH} | high-level input voltage | | 0.7 × V _{PVDD_IN} | - | - | V |
| V _{IL} | low-level input voltage | | - | - | 0.3 × V _{PVDD_IN} | V |
| I _{IH} | high-level input current | V _i = V _{PVDD_IN} | - | - | 1 | μA |
| I _{IL} | low-level input current | V _i = 0 V | -1 | - | - | μA |
| C _{in} | Input capacitance | | - | 5 | - | pF |

Table 51. Static characteristics of ATX_ used as SPIMISO

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---------------------------|------------------------|----------------------------|-----|----------------------|------|
| V _{OH} | high-level output voltage | I _{OH} < 3 mA | V _{PVDD_IN} - 0.4 | - | V _{PVDD_IN} | V |
| V _{OL} | low-level output voltage | I _{OL} < 3 mA | 0 | - | 0.4 | V |
| C _L | load capacitance | | - | - | 20 | pF |

Table 52. USB characteristics

Data are given for $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--|--|-----|-----|----------------|---------------|
| I_{OZ} | OFF-state output current | $0\text{ V} < V_i < 3.3\text{ V}$ | -10 | - | 10 | μA |
| $V_{DDP(VBUS)}$ | power supply voltage on pin VBUS | | 4 | - | 5.5 | V |
| V_{DI} | differential input sensitivity voltage | (D+) - (D-) | 0.2 | - | - | V |
| V_{CM} | differential common mode voltage range | includes V_{DI} range | 0.8 | - | 2.5 | V |
| $V_{th(rs)se}$ | single-ended receiver switching threshold voltage | | 0.8 | - | 2 | V |
| V_{OL} | low-level output voltage | for low-speed or full-speed; R_L of 1.5 k Ω to 3.6 V | - | - | 0.3 | V |
| V_{OH} | high-level output voltage | driven; for low-speed or full-speed; R_L of 15 k Ω to GND | 2.8 | - | V_{PVDD_IN} | V |
| C_{trans} | transceiver capacitance | pin to GND | - | 15 | - | pF |
| Z_{DRV} | driver output impedance for driver which is not high-speed capable | with 33 Ω series resistor; steady state drive | 28 | - | 44 | Ω |
| V_{CRS} | output signal crossover voltage | | 1.3 | - | 2 | V |

Table 53. Static characteristics of HSU_TX and HSU RTS pin

Data are given for $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|---------------------------|------------------------|----------------------|-----|----------------|------|
| V_{OH} | high-level output voltage | $I_{OH} < 3\text{ mA}$ | $V_{PVDD_IN} - 0.4$ | - | V_{PVDD_IN} | V |
| V_{OL} | low-level output voltage | $I_{OL} < 3\text{ mA}$ | 0 | - | 0.4 | V |
| C_L | load capacitance | | - | - | 20 | pF |

Table 54. Static characteristics of HSU_RX, HSU_CTS

Data are given for $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|----------------------------------|----------------------------|-----|----------------------------|---------------|
| V_{IH} | high-level input voltage | $V_{PVDD_M_IN} = 1.8\text{ V}$ | $0.65 \times V_{PVDD_IN}$ | - | - | V |
| V_{IL} | low-level input voltage | $V_{PVDD_M_IN} = 1.8\text{ V}$ | - | - | $0.35 \times V_{PVDD_IN}$ | V |
| V_{IH} | high-level input voltage | $V_{PVDD_M_IN} = 3.3\text{ V}$ | 2 | - | - | V |
| V_{IL} | low-level input voltage | $V_{PVDD_M_IN} = 3.3\text{ V}$ | - | - | 0.8 | V |
| I_{IH} | high-level input current | | - | - | 1 | μA |
| I_{IL} | low-level input current | | -1 | - | - | μA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|------------------|------------|-----|-----|-----|------|
| C _L | load capacitance | | - | 5 | - | pF |

13.1.5 Clock static characteristics

Table 55. Static characteristics of XTAL pin (XTAL1, XTAL2)

$T_{amb} = -40\text{ °C to }+85\text{ °C}$

| Symbol | Parameter ^[1] | Conditions | Min | Typ ^[2] | Max | Unit |
|---|----------------------------|----------------------------------|-----|--------------------|-----------------|------|
| Input clock characteristics on XTAL1 when using PLL | | | | | | |
| V _{i(p-p)} | peak-to-peak input voltage | | 0.2 | - | 1.65 | V |
| XTAL pin characteristics XTAL PLL input | | | | | | |
| I _{IH} | high-level input current | V _i = V _{DD} | - | - | 1 | μA |
| I _{IL} | low-level input current | V _i = 0 V | -1 | - | - | μA |
| V _i | input voltage | | - | - | V _{DD} | V |
| V _{AL} | input voltage amplitude | | 200 | - | - | mV |
| C _{in} | input capacitance | all power modes | - | 2 | - | pF |
| Pin characteristics for 27.12 MHz crystal oscillator | | | | | | |
| C _{in} | input capacitance | pin XTAL1 | - | 2 | - | pF |
| C _{in} | input capacitance | pin XTAL2 | - | 2 | - | pF |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C) with nominal supply voltages.

13.1.6 Static characteristics - power supply

Table 56. Static characteristics for power supply

Data are given for $T_{amb} = -40\text{ °C to }+85\text{ °C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-----------------------------------|--|-----|-----|-----|------|
| I _{DDP(VBUSP)} | power supply current on pin VBUSP | external supply current for contact interface, in operating mode | - | - | 200 | mA |
| pin supply: PVDD_LDO | | | | | | |
| V _{O(LDO)} | LDO output voltage | V _{DDP(VBUS)} ≥ 4.0 V, I _{PVDDOUT} ≤ 30 mA | 3 | 3.3 | 3.6 | V |
| I _{DD(PVDD_OUT)} | maximum supply current | for pin PVDD_OUT | - | - | 30 | mA |
| pin supply for host interface and GPIOs (on pin PVDD_IN) | | | | | | |
| I _{DD(PVDD)} | PVDD supply current | | - | - | 25 | mA |
| pin supply for master interfaces (on pin PVDD_M_IN) | | | | | | |
| I _{DD(PVDD)} | PVDD supply current | | - | - | 25 | mA |
| NFC interface: TX_LDO (pins VUP_TX, TVDD_OUT) | | | | | | |
| V _{I(LDO)} | LDO input voltage | | 3 | - | 5.5 | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|---|--------|---------------------------|-------|------|
| V _{O(LDO)} | LDO output voltage | DC output voltage (target: 3.0 V) 5.5 V > V _{I(LDO)} > 3.3 V | 2.8 | 3 | 3.25 | V |
| | | DC output voltage (target: 3.0 V) 3.3 V > V _{I(LDO)} > 2.7 V | - | V _{I(LDO)} - 0.3 | - | V |
| | | DC output voltage (target: 3.3 V) 5.5 V > V _{I(LDO)} > 3.6 V | 3.1 | 3.3 | 3.55 | V |
| | | DC output voltage (target: 3.3 V) 3.6 V > V _{I(LDO)} > 2.7 V | - | V _{I(LDO)} - 0.3 | - | V |
| | | DC output voltage (target: 3.6 V) 5.5 V > V _{I(LDO)} > 3.9 V | 3.4 | 3.6 | 3.95 | V |
| | | DC output voltage (target: 3.6 V) 3.9 V > V _{I(LDO)} > 2.7 V | - | V _{I(LDO)} - 0.3 | - | V |
| | | DC output voltage (target: 4.5 V) 5.5 V > V _{I(LDO)} > 5.0 V | 4.3 | 4.5 | 4.9 | V |
| | | DC output voltage (target: 4.75 V) 5.5 V > V _{I(LDO)} > 5.0 V | 4.55 | 4.75 | 5.2 | V |
| I _{O(LDO)} | LDO output current | V _{I(LDO)} = 5.5 V | - | - | 225 | mA |
| I _{O(LDO)} | LDO peak output current | V _{I(LDO)} = 5.5 V | - | - | 275 | mA |
| NFC interface: RF transmitter (on pin TVDD_IN) | | | | | | |
| I _{DD(TVDD)} | maximum continuous TVDD supply current | | - | - | 250 | mA |
| I _{DD(TVDD)} | maximum peak TVDD supply current | | - | - | 275 | mA |
| Contact Interface: smart card power supply (pin VCC) | | | | | | |
| C _{dec} | decoupling capacitance | connected on pin VCC (220 nF + 220 nF 10 %) | 396 | 570 | 1000 | nF |
| V _{CC} | supply voltage | class A; I _{CC} < 60 mA | 4.75 | 5 | 5.25 | V |
| | | class B; I _{CC} < 50 mA | 2.85 | 3 | 3.15 | V |
| | | class C; I _{CC} < 30 mA | 1.71 | 1.8 | 1.89 | V |
| | | class A; current pulses of 40 nA with I _{CC} < 200 mA, t _w < 400 ns | 4.6 | - | 5.4 | V |
| | | class B; current pulses of 40 nA with I _{CC} < 200 mA, t _w < 400 ns | 2.76 | - | 3.24 | V |
| | | class C; current pulses of 12 nA with I _{CC} < 200 mA, t _w < 400 ns | 1.66 | - | 1.94 | V |
| V _{ripple(p-p)} | peak-to-peak ripple voltage | from 20 kHz to 200 MHz | - | - | 350 | mV |
| SR | slew rate on pin VCC | 5 V, class A cards | 0.02 | - | 0.025 | V/μs |
| | | 3 V, class B cards | 0.012 | - | 0.015 | V/μs |
| | | 1.8 V, class C cards | 0.0072 | - | 0.009 | V/μs |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|--|-------|-----|-----|------|
| I _{CC} | supply current | class A | - | - | 60 | mA |
| | | class B | - | - | 55 | mA |
| | | class C | - | - | 35 | mA |
| | | Pin VCC shorted to ground | - | - | 110 | mA |
| Contact interface: DC-to-DC converter | | | | | | |
| V _{SAP} | SAP (DC-to-DC converter) - high-level output voltage | V _{DDP(VBUSP)} = 5 V, V _{CC} = 5 V; I _{CC} < 60 mA DC | - | - | 9 | V |
| | | V _{DDP(VBUSP)} = 5 V, V _{CC} = 3 V; I _{CC} < 55 mA DC | - | - | 5 | V |
| | | V _{DDP(VBUSP)} = 5 V, V _{CC} = 1.8 V; I _{CC} < 35 mA DC | - | - | 5 | V |
| | | V _{DDP(VBUSP)} = 3.3 V, V _{CC} = 5 V; I _{CC} < 60 mA DC | - | - | 9 | V |
| | | V _{DDP(VBUSP)} = 3.3 V, V _{CC} = 3 V; I _{CC} < 55 mA DC | - | - | 9 | V |
| | | V _{DDP(VBUSP)} = 3.3 V, V _{CC} = 1.8 V; I _{CC} < 35 mA DC | - | - | 3.3 | V |
| V _{UP} | V _{UP} - high-level output voltage | Class A; V _{DDP(VBUSP)} = 3 V to 5 V, I _{CC} < 60 mA | 5.35 | - | 5.9 | V |
| | | Class B; I _{CC} < 55 mA | 3.53 | - | 5.5 | V |
| | | Class C, V _{DDP(VBUSP)} = 2.7 V to 5.5 V, I _{CC} < 35 mA DC | 2.4 | - | 5.5 | V |
| C _{SAPSAM} | DC-to-DC converter capacitance | connected between SAP and SAM with V _{DDP(VBUSP)} = 3 V | 300 | 470 | 600 | nF |
| C _{VUP} | DC-to-DC converter capacitance | connected on pin VUP | 1.5 | 2.7 | 4.7 | μF |
| Voltage detector for the DC-to-DC converter | | | | | | |
| V _{det} | detection voltage | on pin VBUSP for doubler selection, follower/doubler for class B card | 3.775 | 3.9 | 4.2 | V |

Table 57. Static characteristics for voltage monitors

T_{amb} = -40 °C to +85 °C

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|----------------------------------|--------------|------|------|------|------|
| V _{(th)HL} | negative-going threshold voltage | VBUS monitor | | | | |
| | | set to 2.3 V | 2.15 | 2.3 | 2.45 | V |
| | | set to 2.7 V | 2.6 | 2.75 | 2.95 | V |
| | | set to 4.0 V | 3.6 | 3.8 | 3.9 | V |
| V _{hys} | hysteresis voltage | VBUS monitor | | | | |
| | | set to 2.3 V | 100 | 150 | 200 | mV |
| | | set to 2.7 V | 100 | 150 | 200 | mV |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|----------------------------------|---------------|------|-------|------|------|
| | | set to 4.0 V | 40 | 80 | 100 | mV |
| V _{(th)HL} | negative-going threshold voltage | VBUSP monitor | | | | |
| | | set to 2.7 V | 2.45 | 2.56 | 2.65 | V |
| | | set to 3.0 V | 2.68 | 2.825 | 2.95 | V |
| | | set to 3.9 V | 3.7 | 3.9 | 4.1 | V |
| V _{hys} | hysteresis voltage | VBUSP monitor | | | | |
| | | set to 2.7 V | 12 | 25 | 35 | mV |
| | | set to 3.0 V | 14 | 30 | 40 | mV |
| | | set to 3.9 V | 20 | 35 | 55 | mV |

13.1.7 Static characteristics for power modes

Table 58. Static characteristics for power modes

T_{amb} = -40 °C to +85 °C; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|----------------------------------|---|-----|-----|-----|------|
| I _{DDP(VBUS)} | power supply current on pin VBUS | active mode; V _{DDP(VBUS)} = 5.5 V, external PVDD, external TVDD, all IP clocks disabled code while(1){} executed from flash; | - | 6.5 | - | mA |
| | | active mode; V _{DDP(VBUS)} = 5.5 V, external PVDD, external TVDD, all IP clocks enabled code while(1){} executed from flash; | - | 8.5 | - | mA |
| | | suspend mode; V _{DDP(VBUS)} = 5.5 V, external PVDD, T = 25 °C | - | 120 | 250 | µA |
| | | V _{BUS} = 5.5 V, T = 25 °C, internal PVDD LDO, including D+ and D-pull-up | - | 360 | 440 | µA |
| | | standby mode; V _{DDP(VBUS)} = 3.3 V; external PVDD supply; T _{amb} = 25 °C | - | 18 | - | µA |
| | | standby mode; V _{DDP(VBUS)} = 5.5 V; V _{internal} PVDD supply; T _{amb} = 25 °C | - | 55 | - | µA |
| | | hard power down; V _{DDP(VBUS)} = 5.5 V; RST_N = 0 V; T _{amb} = 25 °C | - | 12 | 18 | µA |

13.1.8 Static characteristics for contact interface

Table 59. Static characteristics for contact interface

T_{amb} = -40 °C to +80 °C

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|----------------------------|---|-----------------------|-----|---------------------------------------|------|
| Data lines (pins IO, AUX1, AUX2) | | | | | | |
| V _o | output voltage on pin IO | inactive mode, no load | 0 | - | 0.1 | V |
| | | inactive mode, I _{I/O} = 1 mA | 0 | - | 0.3 | V |
| V _{OL} | low-level output voltage | pin IO Configured as output I _{OL} = 1 mA (class A,B), 500 μA (class C) | 0 | - | 0.15 × V _{CC} | V |
| | | pin IO configure as output, I _{OL} < 15 mA | 0 | - | 0.4 | V |
| V _{OH} | high-level output voltage | pin IO configure as output, I _{OH} < -200 μA, V _{CC} = 5 V, 3 V and 1.8 V; active pull-up | 0.9 × V _{CC} | - | V _{CC} | V |
| | | pin IO configure as output, I _{OH} < -20 μA; V _{CC} = 1.8 V | 0.8 × V _{CC} | - | V _{CC} | V |
| | | pin IO configure as output, I _{OH} < 15 mA | 0 | - | 0.4 | V |
| V _{IL} | low-level input voltage | pin IO configure as input | 0 | - | 0.2 × V _{CC} | V |
| V _{IH} | high-level input voltage | | 0.6 × V _{CC} | - | V _{CC} | V |
| V _{hys} | hysteresis voltage | on pin IO | 20 | 75 | 120 | mV |
| I _{IL} | low-level input current | on pin IO; V _{IL} = 0 V | - | - | 750 | μA |
| I _{LH} | high-level leakage current | on pin IO; V _{IH} = V _{CC} | - | - | 10 | μA |
| R _{pu} | pull-up resistance | connected to V _{CC} | 7 | 10 | 13 | kΩ |
| Reset output to the card | | | | | | |
| V _o | output voltage | inactive mode; no load | 0 | - | 0.1 | V |
| | | inactive mode; I _o = 1 mA | 0 | - | 0.3 | V |
| V _{OL} | low-level output voltage | I _{OL} = 200 μA, V _{CC} = 5 V and V _{CC} = 3 V | 0 | - | 0.3 | V |
| | | I _{OL} = 200 μA, V _{CC} = 1.8 V | 0 | - | 0.1 × V _{CC} | V |
| V _{OH} | high-level output voltage | I _{OH} = -200 μA | 0.9 × V _{CC} | - | V _{CC} | V |
| Clock output to the card | | | | | | |
| V _o | output voltage | inactive mode; no load | 0 | - | 0.1 | V |
| | | inactive mode; I _o = 1 mA | 0 | - | 0.3 | V |
| V _{OL} | low-level output voltage | I _{OL} = 200 μA | 0 | - | minimum (0.1 × V _{CC} ; 0.3) | V |
| V _{OH} | high-level output voltage | I _{OH} = -200 μA | 0.9 × V _{CC} | - | V _{CC} | V |
| Card presence input | | | | | | |
| V _{IL} | low-level input voltage | | -0.3 | - | 0.3 × V _{PVDD_IN} | V |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------|--|-----------------------------|-----|----------------------------|------|
| V _{IH} | high-level input voltage | | 0.7 × V _{PVDD_IN} | - | V _{PVDD_IN} + 0.3 | V |
| V _{hys} | hysteresis voltage | | 0.03 × V _{PVDD_IN} | - | - | V |
| I _{LL} | low-level leakage current | V _{IL} = 0 | - | - | 1 | μA |
| I _{LH} | high-level leakage current | V _{IH} = V _{PVDD_IN} | - | - | 5 | μA |

13.1.9 Static characteristics NFC interface

Table 60. Static characteristics for NFC interface

Data are given for $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|---------------------------------|--|-------------------------------|-----|------------------------|---------------------|
| pins ANT1 and ANT2 | | | | | | |
| Z | impedance | between ANT1 and ANT2; low impedance | - | 10 | 17 | Ω |
| pins RXN and RXP | | | | | | |
| V _{i(dyn)} | dynamic input voltage | on pins RXN and RXP | - | - | V _{DD} - 0.05 | V |
| C _{in} | input pin capacitance | on pins RXN and RXP | - | 12 | - | pF |
| Z | impedance | between pins RX to VMID; reader, card emulation and P2P modes | 0 | - | 15 | kΩ |
| V _{det} | detection voltage | card emulation and target modes; configuration for 19 mV threshold | - | - | 30 | mV _(p-p) |
| pins TX1 and TX2 | | | | | | |
| V _{OH} | high-level output voltage | pins TX1 and TX2; T _{VDD_IN} = 3.1 V and I _{OH} = 30 mA | V _{TVDD_IN} - 150 | - | - | mV |
| V _{OL} | low-level output voltage | pins TX1 and TX2; T _{VDD_IN} = 3.1; I _{TX} = 30 mA | - | - | 200 | mV |
| R _{OL} | low-level output resistance | V _{TX} = V _{TVDD} - 100 mV; CWGsN = 01h | - | - | 80 | Ω |
| | | V _{TX} = V _{TVDD} - 100 mV; CWGsN = 0Fh | - | - | 10 | Ω |
| R _{OH} | high-level output resistance | V _{TX} = V _{TVDD} - 100 mV | - | - | 10 | Ω |

13.2 Dynamic characteristics

Table 61. Dynamic characteristics for IRQ output pin

Data are given for $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|-----------|---|-----|-----|-----|------|
| t _f | fall time | high speed; C _L = 12 pF; V _{PVDD_IN} = 3.3 V | 1 | - | 3.5 | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|---|-----|-----|-----|------|
| | | high speed; $C_L = 12\text{ pF}$; $V_{PVDD_IN} = 1.8\text{ V}$ | 1 | - | 3.5 | ns |
| t_f | fall time | slow speed; $C_L = 12\text{ pF}$; $V_{PVDD_IN} = 3.3\text{ V}$ | 3 | - | 10 | ns |
| | | slow speed; $C_L = 12\text{ pF}$; $V_{PVDD_IN} = 1.8\text{ V}$ | 2 | - | 10 | ns |
| t_r | rise time | high speed; $C_L = 12\text{ pF}$; $V_{PVDD_IN} = 3.3\text{ V}$ | 1 | - | 3.5 | ns |
| | | high speed; $C_L = 12\text{ pF}$; $V_{PVDD_IN} = 1.8\text{ V}$ | 1 | - | 3.5 | ns |
| t_r | rise time | slow speed; $C_L = 12\text{ pF}$; $V_{PVDD_IN} = 3.3\text{ V}$ | 3 | - | 10 | ns |
| | | slow speed; $C_L = 12\text{ pF}$; $V_{PVDD_IN} = 1.8\text{ V}$ | 2 | - | 10 | ns |

13.2.1 Flash memory dynamic characteristics

Table 62. Dynamic characteristics for flash memory

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|------------------|-------------------------------|-----|-----|-----|--------|
| t_{prog} | programming time | 1 page (64 bytes); slow clock | - | - | 2.5 | ms |
| N_{Endu} | endurance | | 200 | 500 | - | Kcycle |
| t_{ret} | retention time | | - | 20 | - | year |

13.2.2 EEPROM dynamic characteristics

Table 63. Dynamic characteristics for EEPROM

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|------------------|-------------------|-----|-----|-----|--------|
| t_{prog} | programming time | 1 page (64 bytes) | - | 2.8 | - | ms |
| N_{Endu} | endurance | | 300 | 500 | - | Kcycle |
| t_{ret} | retention time | | - | 20 | - | year |

13.2.3 GPIO dynamic characteristics

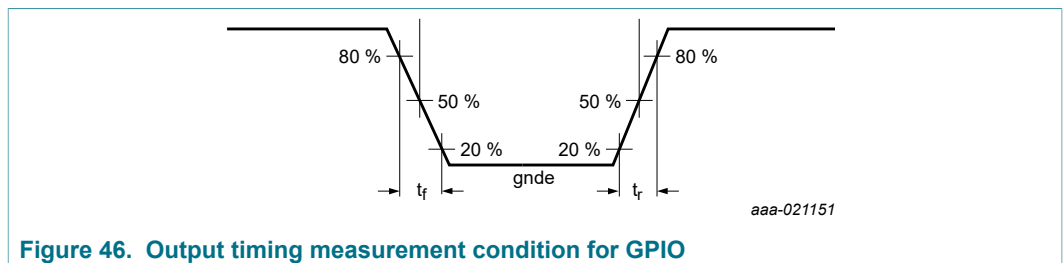


Figure 46. Output timing measurement condition for GPIO

Table 64. Dynamic characteristics for GPIO1 to GPIO21

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|---|-----|------|------|
| t_r | rise time | $C_L = 12\text{ pF}$; PVDD = 1.8 V; slow speed | 2.0 | 10.0 | ns |
| | | $C_L = 12\text{ pF}$; PVDD = 1.8 V; fast speed | 1.0 | 3.5 | ns |
| | | $C_L = 12\text{ pF}$; PVDD = 3.3 V; slow speed | 3.0 | 10.0 | ns |
| | | $C_L = 12\text{ pF}$; PVDD = 3.3 V; fast speed | 1.0 | 3.5 | ns |
| t_f | fall time | $C_L = 12\text{ pF}$; PVDD = 1.8 V; slow speed | 2.0 | 10.0 | ns |
| | | $C_L = 12\text{ pF}$; PVDD = 1.8 V; fast speed | 1.0 | 3.5 | ns |
| | | $C_L = 12\text{ pF}$; PVDD = 3.3 V; slow speed | 3.0 | 10.0 | ns |
| | | $C_L = 12\text{ pF}$; PVDD = 3.3 V; fast speed | 1.0 | 3.5 | ns |

13.2.4 Dynamic characteristics for I²C master

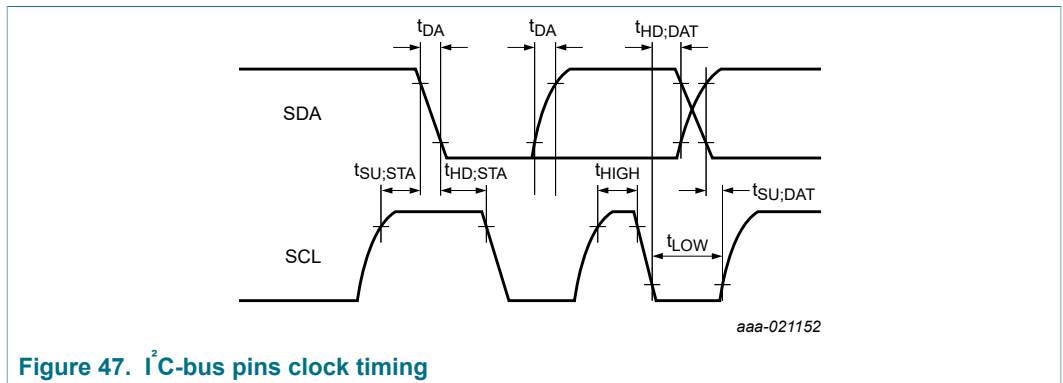


Figure 47. I²C-bus pins clock timing

Table 65. Timing specification for fast mode plus I²C

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--|---------------------------------------|-----|-----|------|
| f_{SCL} | SCL clock frequency | fast mode plus; $C_b < 100\text{ pF}$ | 0 | 1 | MHz |
| $t_{SU:STA}$ | set-up time for a (repeated) START condition | fast mode plus; $C_b < 100\text{ pF}$ | 260 | - | ns |
| $t_{HD:STA}$ | hold time (repeated) START condition | fast mode plus; $C_b < 100\text{ pF}$ | 260 | - | ns |
| t_{LOW} | low period of the SCL clock | fast mode plus; $C_b < 100\text{ pF}$ | 500 | - | ns |
| t_{HIGH} | high period of the SCL clock | fast mode plus; $C_b < 100\text{ pF}$ | 260 | - | ns |
| $t_{SU:DAT}$ | data set-up time | fast mode plus; $C_b < 100\text{ pF}$ | 50 | - | ns |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--------------------------------------|---|------------------------------|-----|------|
| t _{HD,DAT} | data hold time | fast mode plus; C _b < 100 pF | 0 | - | ns |
| t _{r(SDA)} | SDA rise time | fast mode plus; C _b < 100 pF | - | 120 | ns |
| t _{f(SDA)} | SDA fall time | fast mode plus; C _b < 100 pF | - | 120 | ns |
| V _{hys} | hysteresis of Schmitt trigger inputs | fast mode plus; C _b < 100 pF | 0.1 × V _{PVDD_M_IN} | - | V |

Table 66. Timing specification for fast mode I²C

T_{amb} = -40 °C to +85 °C

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|--|---|----------------------------|-----|------|
| f _{SCL} | SCL clock frequency | fast mode; C _b < 400 pF | 0 | 400 | kHz |
| t _{SU,STA} | set-up time for a (repeated) START condition | fast mode; C _b < 400 pF | 600 | - | ns |
| t _{HD,STA} | hold time (repeated) START condition | fast mode; C _b < 400 pF | 600 | - | ns |
| t _{LOW} | low period of the SCL clock | fast mode; C _b < 400 pF | 1.3 | - | µs |
| t _{HIGH} | high period of the SCL clock | fast mode; C _b < 400 pF | 600 | - | ns |
| t _{SU,DAT} | data set-up time | fast mode; C _b < 400 pF | 100 | - | ns |
| t _{HD,DAT} | data hold time | fast mode; C _b < 400 pF | 0 | 900 | ns |
| t _{r(SDA)} | SDA rise time | fast mode plus; C _b < 100 pF | 30 | 250 | ns |
| t _{f(SDA)} | SDA fall time | fast mode plus; C _b < 100 pF | 30 | 250 | ns |
| V _{hys} | hysteresis of Schmitt trigger inputs | fast mode; C _b < 400 pF | 0.1 × V _{PVDD_IN} | - | V |

13.2.5 Dynamic characteristics for SPI

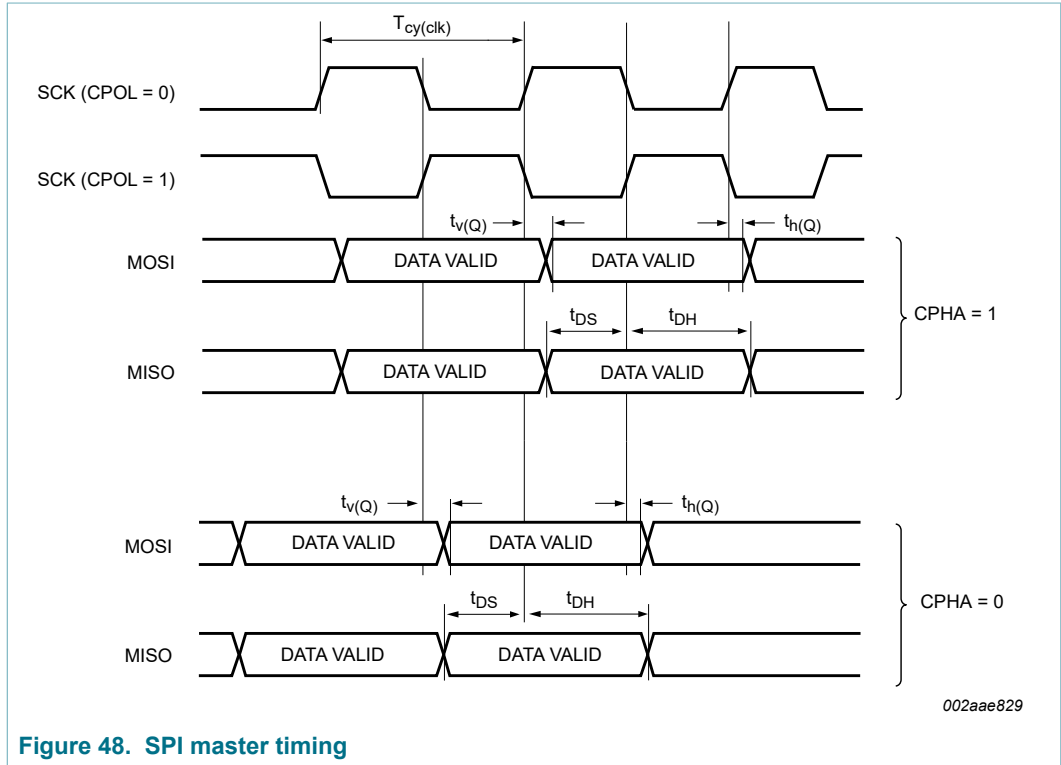


Figure 48. SPI master timing

Table 67. Dynamic characteristics and Timing specification for SPI master interface

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--|------------------------|--|-----|------|------|
| f_{SCK} | SCK frequency | controlled by the host | 0 | 6.78 | MHz |
| t_{DS} | data set-up time | | 25 | - | ns |
| t_{DH} | data hold time | | 25 | - | ns |
| $t_{V(Q)}$ | data output valid time | | - | 25 | ns |
| $t_{H(Q)}$ | data output hold time | | - | 25 | ns |
| Dynamic characteristics for SPI_SCLK, SPIM_NSS, SPIM_MOSI | | | | | |
| t_f | fall time | $C_L = 12\text{ pF}$; high speed; $V_{PVDD_IN} = 3.3\text{ V}$ | 1 | 3.5 | ns |
| | | $C_L = 12\text{ pF}$; slow speed; $V_{PVDD_IN} = 3.3\text{ V}$ | 3 | 10 | ns |
| t_r | rise time | $C_L = 12\text{ pF}$; high speed; $V_{PVDD_IN} = 3.3\text{ V}$ | 1 | 3.5 | ns |
| | | $C_L = 12\text{ pF}$; slow speed; $V_{PVDD_IN} = 3.3\text{ V}$ | 3 | 10 | ns |
| t_f | fall time | $C_L = 12\text{ pF}$; high speed; $V_{PVDD_IN} = 1.8\text{ V}$ | 1 | 3.5 | ns |
| | | $C_L = 12\text{ pF}$; slow speed; $V_{PVDD_IN} = 1.8\text{ V}$ | 2 | 10 | ns |
| t_r | rise time | $C_L = 12\text{ pF}$; high speed; $V_{PVDD_IN} = 1.8\text{ V}$ | 1 | 3.5 | ns |

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------|-----------|--|-----|-----|------|
| | | $C_L = 12 \text{ pF}$; slow speed; $V_{PVDD_IN} = 1.8 \text{ V}$ | 2 | 10 | ns |

13.2.6 Dynamic characteristics of host interface

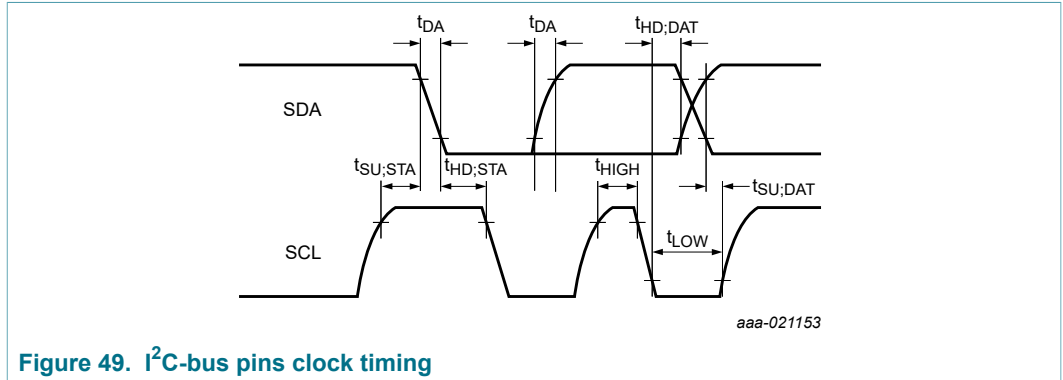


Figure 49. I²C-bus pins clock timing

Table 68. Timing specification for I2C high speed

$T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--|------------------------------------|---------------------------|-----|---------------|
| f_{scl} | clock frequency | high speed; $C_b < 100 \text{ pF}$ | 0 | 3.4 | MHz |
| $t_{SU,STA}$ | set-up time for a (repeated) START condition | high speed; $C_b < 100 \text{ pF}$ | 160 | - | ns |
| $t_{HD,STA}$ | hold time (repeated) START condition | high speed; $C_b < 100 \text{ pF}$ | 160 | - | ns |
| t_{LOW} | low period of the SCL clock | high speed; $C_b < 100 \text{ pF}$ | 160 | - | ns |
| t_{HIGH} | high period of the SCL clock | high speed; $C_b < 100 \text{ pF}$ | 60 | - | ns |
| $t_{SU,DAT}$ | data set-up time | high speed; $C_b < 100 \text{ pF}$ | 10 | - | ns |
| $t_{HD,DAT}$ | data hold time | high speed; $C_b < 100 \text{ pF}$ | 0 | - | μs |
| $t_{r(SDA)}$ | SDA rise time | high speed; $C_b < 100 \text{ pF}$ | 10 | 80 | ns |
| $t_{f(SDA)}$ | SDA fall time | high speed; $C_b < 100 \text{ pF}$ | 10 | 80 | ns |
| V_{hys} | hysteresis of Schmitt trigger inputs | high speed; $C_b < 100 \text{ pF}$ | $0.1 \times V_{PVDD_IN}$ | - | V |

Table 69. Dynamic characteristics for the I²C slave interface: ATX_B used as I²C_SDA, ATX_A used as I²C_SCL

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|---|-----|-----|-----|------|
| t_f | fall time | $C_L = 100 \text{ pF}$, $R_{pull-up} = 2 \text{ K}$, standard and fast mode | 30 | - | 250 | ns |
| | | $C_L = 100 \text{ pF}$, $R_{pull-up} = 1 \text{ K}$, high speed | 10 | - | 80 | ns |
| t_r | rise time | $C_L = 100 \text{ pF}$, $R_{pull-up} = 2 \text{ K}$, standard and fast mode | 30 | - | 250 | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|--|-----|-----|-----|------|
| | | $C_L = 100 \text{ pF}$, $R_{\text{pull-up}} = 1 \text{ K}$, high speed | 10 | - | 100 | ns |

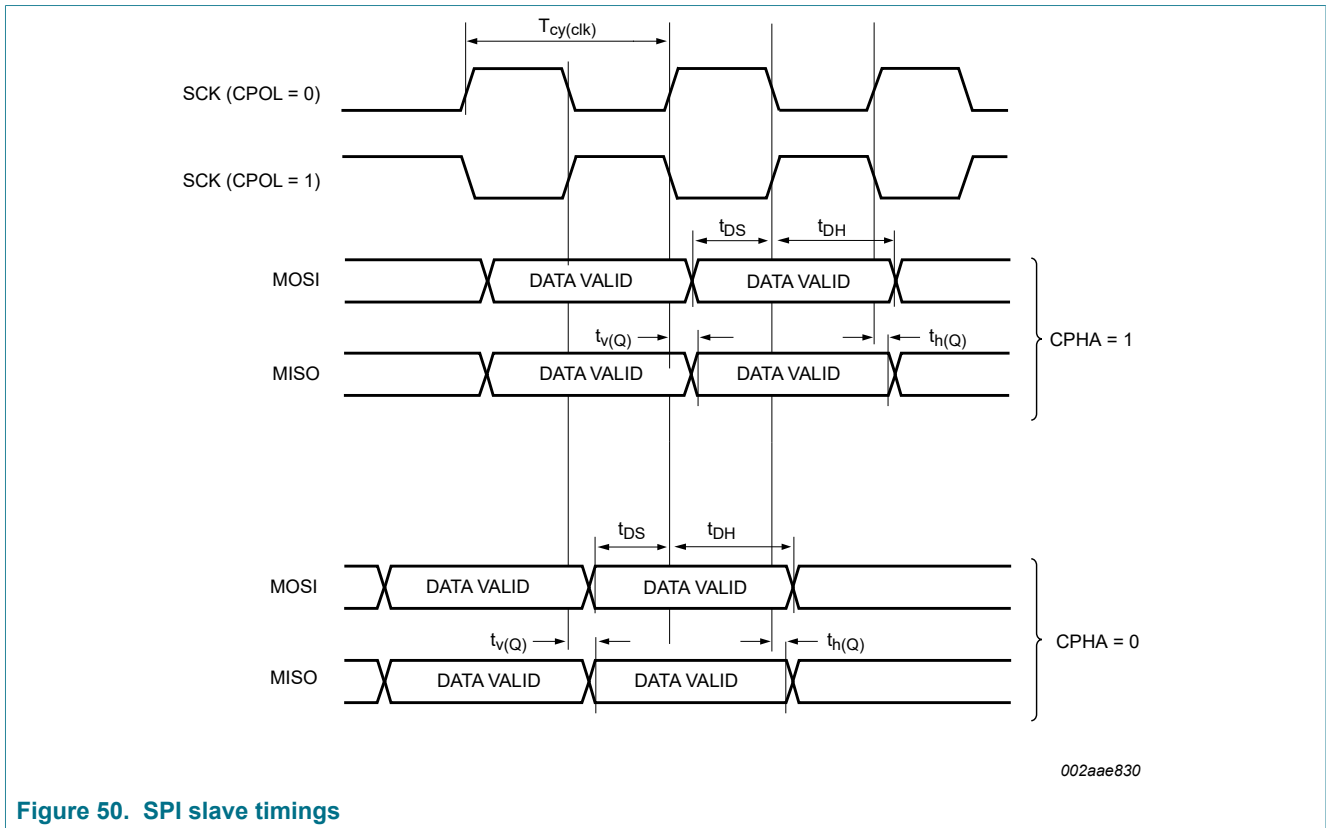


Figure 50. SPI slave timings

Table 70. Dynamic characteristics for SPI slave interface

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|------------------------|------------------------|-----|-----|------|
| f_{SCK} | SCK frequency | controlled by the host | 0 | 7 | MHz |
| t_{DS} | data set-up time | | 25 | - | ns |
| t_{DH} | data hold time | | 25 | - | ns |
| $t_{V(Q)}$ | data output valid time | | - | 25 | ns |
| $t_{H(Q)}$ | data output hold time | | - | 25 | ns |

Table 71. Dynamic characteristics for SPI slave interface: ATX_C as SPI_MISO

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|---|-----|-----|-----|------|
| t_f | fall time | $C_L = 12 \text{ pF}$; high speed; $V_{PVDD_IN} = 3.3 \text{ V}$ | 1 | - | 3.5 | ns |
| | | $C_L = 12 \text{ pF}$; slow speed; $V_{PVDD_IN} = 3.3 \text{ V}$ | 3 | - | 10 | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|-----------|--|-----|-----|-----|------|
| t _r | rise time | C _L = 12 pF; high speed; V _{PVDD_IN} = 3.3 V | 1 | - | 3.5 | ns |
| | | C _L = 12 pF; slow speed; V _{PVDD_IN} = 3.3 V | 3 | - | 10 | ns |
| t _f | fall time | C _L = 12 pF; high speed; V _{PVDD_IN} = 1.8 V | 1 | - | 3.5 | ns |
| | | C _L = 12 pF; slow speed; V _{PVDD_IN} = 1.8 V | 2 | - | 10 | ns |
| t _r | rise time | C _L = 12 pF; high speed; V _{PVDD_IN} = 1.8 V | 1 | - | 3.5 | ns |
| | | C _L = 12 pF; slow speed; V _{PVDD_IN} = 1.8 V | 2 | - | 10 | ns |

Table 72. Dynamic characteristics for HSUART ATX_ as HSU_TX, ATX_ as HSU_RTS

| Symbol | Parameter | Conditions ^[1] | Min | Typ | Max | Unit |
|----------------|-----------|--|-----|-----|-----|------|
| t _f | fall time | high speed; V _{PVDD_IN} = 3.3 V | 1 | - | 3.5 | ns |
| | | slow speed; V _{PVDD_IN} = 3.3 V | 3 | - | 10 | ns |
| t _r | rise time | high speed; V _{PVDD_IN} = 3.3 V | 1 | - | 3.5 | ns |
| | | slow speed; V _{PVDD_IN} = 3.3 V | 3 | - | 10 | ns |
| t _f | fall time | high speed; V _{PVDD_IN} = 1.8 V | 1 | - | 3.5 | ns |
| | | slow speed; V _{PVDD_IN} = 1.8 V | 2 | - | 10 | ns |
| t _r | rise time | high speed; V _{PVDD_IN} = 1.8 V | 1 | - | 3.5 | ns |
| | | slow speed; V _{PVDD_IN} = 1.8 V | 2 | - | 10 | ns |

[1] C_L=12 pF maximum.

Table 73. Dynamic characteristics for USB interface

C_L = 50 pF; R_{pu} = 1.5 kΩ on D+ to VBUS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|---|--|-------|-----|-------|------|
| t _r | rise time | 10 % to 90 % | 4 | - | 20 | ns |
| t _f | fall time | 10 % to 90 % | 4 | - | 20 | ns |
| t _{FRFM} | differential rise and fall time matching | t _r / t _f | - | - | 109 | % |
| V _{CRS} | output signal crossover voltage | | 1.3 | - | 2 | V |
| t _{FEOPT} | source SE0 interval of EOP | T = 25 °C; see Figure 51 | 160 | - | 175 | ns |
| t _{FDEOP} | source jitter for differential transition to SE0 transition | T = 25 °C; see Figure 51 | -2 | - | +5 | ns |
| t _{JR1} | receiver jitter to next transition | T = 25 °C | -18.5 | - | +18.5 | ns |
| t _{JR2} | receiver jitter for paired transitions | 10 % to 90 %; T = 25 °C | -9 | - | +9 | ns |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|------------------------------|---|-----|-----|-----|------|
| t _{FEOPR} | receiver SE0 interval of EOP | must accept as EOP; see Figure 51 | 82 | - | - | ns |

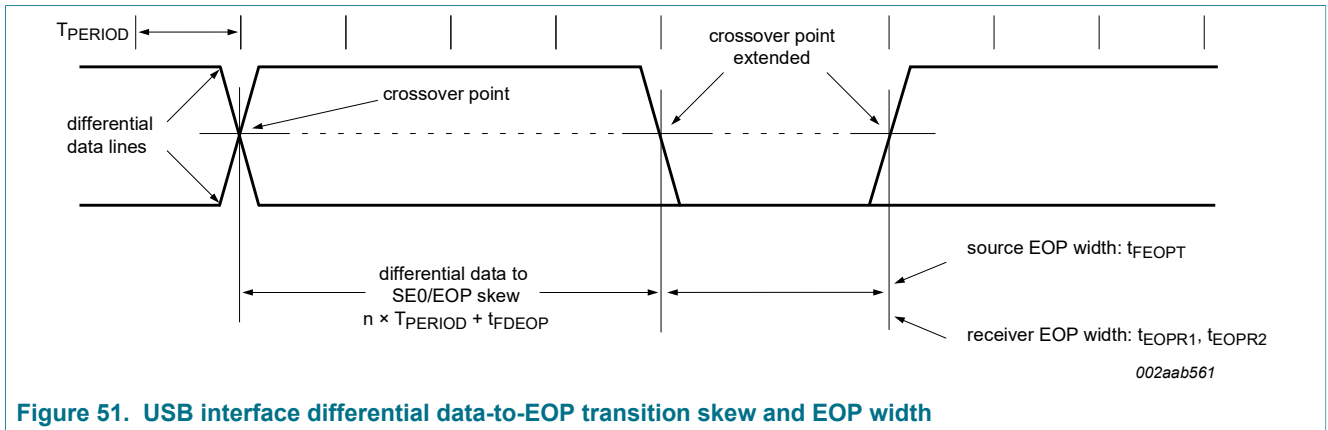


Figure 51. USB interface differential data-to-EOP transition skew and EOP width

13.2.7 Clock dynamic characteristics

Table 74. Dynamic characteristics for internal oscillators

T_{amb} = -40 °C to +85 °C

| Symbol | Parameter ^[1] | Conditions | Min | Typ ^[2] | Max | Unit |
|----------------------------------|-------------------------------|--------------------------------|-----|--------------------|-----|------|
| low frequency oscillator | | | | | | |
| f _{osc(int)} | internal oscillator frequency | V _{DDP(VBUS)} = 3.3 V | 300 | 365 | 400 | kHz |
| high frequency oscillator | | | | | | |
| f _{osc(int)} | internal oscillator frequency | V _{DDP(VBUS)} = 3.3 V | 18 | 20 | 22 | MHz |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C) with nominal supply voltages.

Table 75. Dynamic characteristics for PLL

T_{amb} = -40 °C to +85 °C

| Symbol | Parameter ^[1] | Conditions | Min | Typ ^[2] | Max | Unit |
|--------|--------------------------|---|-----|--------------------|-----|------|
| Δf | frequency deviation | deviation added to CLK_XTAL1 frequency on transmitter frequency generated using PLL | -50 | - | 50 | ppm |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C) with nominal supply voltages.

13.2.8 Dynamic characteristics for power supply

Table 76. Dynamic characteristics for power supply

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|-----------|------------|-----|-----|-----|------|
| DC-to-DC internal oscillator | | | | | | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-------------------------------|--------------------|-----|------|------|------|
| f _{osc(int)} | internal oscillator frequency | DC-to-DC converter | - | 3.39 | - | MHz |
| Main supply (pin VBUS) | | | | | | |
| SR | slew rate | rise and fall | - | - | 2.75 | V/μs |
| RF interface LDO supply (pin VUP_TX) | | | | | | |
| SR | slew rate | rise and fall | - | - | 2.75 | V/μs |
| Supply contact interface (pin VBUSP) | | | | | | |
| SR | slew rate | rise and fall | - | - | 2.75 | V/μs |

13.2.9 Dynamic characteristics for boot and reset

Table 77. Dynamic characteristics for boot and reset

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|----------------------------|---|-----|-----|-----|------|
| t _{wL(RST_N)} | RST_N Low pulse width time | | 10 | - | - | μs |
| t _{boot} | boot time | external PVDD supply; supply is stable at reset | - | - | 320 | μs |
| | | internal PVDD_LDO supply; supply is stable at reset | - | - | 2.2 | ms |

13.2.10 Dynamics characteristics for power mode

Table 78. Power modes - wake-up timings

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------|--------------|--------------|-----|-----|-----|------|
| t _{wake} | wake-up time | standby mode | [1] | - | 500 | μs |
| | | suspend mode | [1] | - | 150 | μs |

[1] Wake-up timings are measured from the wake-up event to the point in which the user application code reads the first instruction.

13.2.11 Dynamic characteristics for contact interface

Table 79. Dynamic characteristics for contact interface

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---------------------|--|-----|-----|-----|------|
| Data lines (pins IO, AUX1, AUX2) | | | | | | |
| f _{data} | data rate | on data lines | - | - | 1.5 | Mbps |
| t _{r(i)} | input rise time | from V _{IL} maximum to V _{IH} minimum | - | - | 1.2 | μs |
| t _{f(i)} | input fall time | from V _{IL} maximum to V _{IH} minimum | - | - | 1.2 | μs |
| t _{r(o)} | output rise time | C _L < = 80 pF; 10 % to 90 % from 0 to V _{CC} | - | - | 0.1 | μs |
| t _{f(o)} | output fall time | C _L < = 80 pF; 10 % to 90 % from 0 to V _{CC} | - | - | 0.1 | μs |
| t _{w(pu)} | pull-up pulse width | | - | 295 | - | ns |
| Reset output to the card | | | | | | |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------------------|----------------------|--|-------|-----|-------|---------------|
| t_r | rise time | $C_L = 100 \text{ pF}$ | - | - | 0.1 | μs |
| t_f | fall time | $C_L = 100 \text{ pF}$ | - | - | 0.1 | μs |
| Clock output to the card (CLK) | | | | | | |
| t_r | rise time | $C_L = 30 \text{ pF}; f_{\text{CLK}} = 10 \text{ MHz}$ | [1] | - | 8 | ns |
| t_r | rise time | $C_L = 30 \text{ pF}; f_{\text{CLK}} = 5 \text{ MHz}$ | [1] | - | 16 | ns |
| t_f | fall time | $C_L = 30 \text{ pF}; f_{\text{CLK}} = 10 \text{ MHz}$ | [1] | - | 8 | ns |
| t_f | fall time | $C_L = 30 \text{ pF}; f_{\text{CLK}} = 5 \text{ MHz}$ | [1] | - | 16 | ns |
| f_{CLK} | frequency on pin CLK | operational | 0 | - | 13.56 | MHz |
| δ | duty cycle | $C_L = 30 \text{ pF}$ | [1] | 45 | 55 | % |
| SR | slew rate | rise and fall; $C_L = 30 \text{ pF}; V_{\text{CC}} = +5 \text{ V}$ | 0.2 | - | - | V/ns |
| | | rise and fall; $C_L = 30 \text{ pF}; V_{\text{CC}} = +3 \text{ V}$ | 0.12 | - | - | V/ns |
| | | rise and fall; $C_L = 30 \text{ pF}; V_{\text{CC}} = +1.8 \text{ V}$ | 0.072 | - | - | V/ns |
| PRESN | | | | | | |
| t_{deb} | debounce time | on pin PRESN | - | 6 | - | ms |
| Timings | | | | | | |
| t_{act} | activation time | see figure below; $T = 25 \text{ }^\circ\text{C}$ | 11 | - | 22 | ms |
| t_{deact} | deactivation time | see figure below; $T = 25 \text{ }^\circ\text{C}$ | 60 | 100 | 250 | μs |

[1] The transition time and duty factor definitions are shown in Figure below.

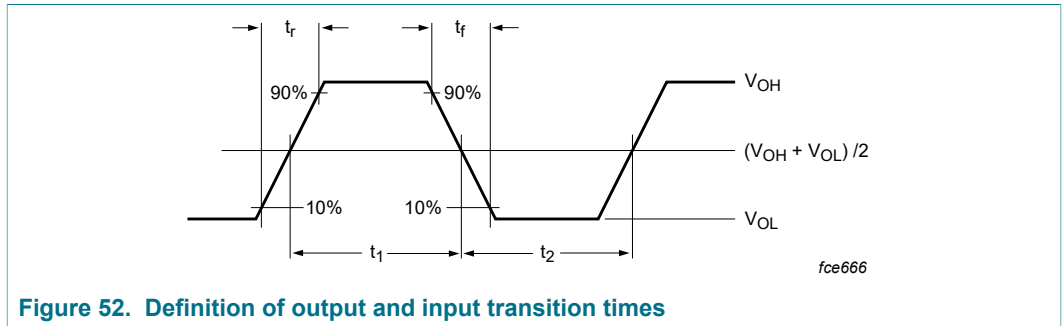


Figure 52. Definition of output and input transition times

14 Marking

14.1 Marking HVQFN64

Table 80. Marking codes

| Type number | Line | Marking code |
|-------------|--------|--|
| PN7462AUHN | Line A | 7462AU-00 |
| PN7362AUHN | | 7362AU-00 |
| PN7360AUHN | | 7360AU-00 |
| PN7412AUHN | | 7412AU-00 |
| Common | Line B | Diffusion Batch ID, Assembly Sequence ID |
| | Line C | Characters: Diffusion and assembly location, date code, product version (indicated by mask version), product life cycle status. This line includes the following elements at 8 positions: 1. Diffusion center code: Z 2. Assembly center code: S 3. RHF-2006 indicator: D "Dark Green" 4. Year code (Y) 1 5. Year code (Y) 2 6. Week code (W) 1 7. Week code (W) 2 8. HW version |
| | Line D | Empty |
| | Line E | Empty |
| | | |

14.1.1 Package marking drawing

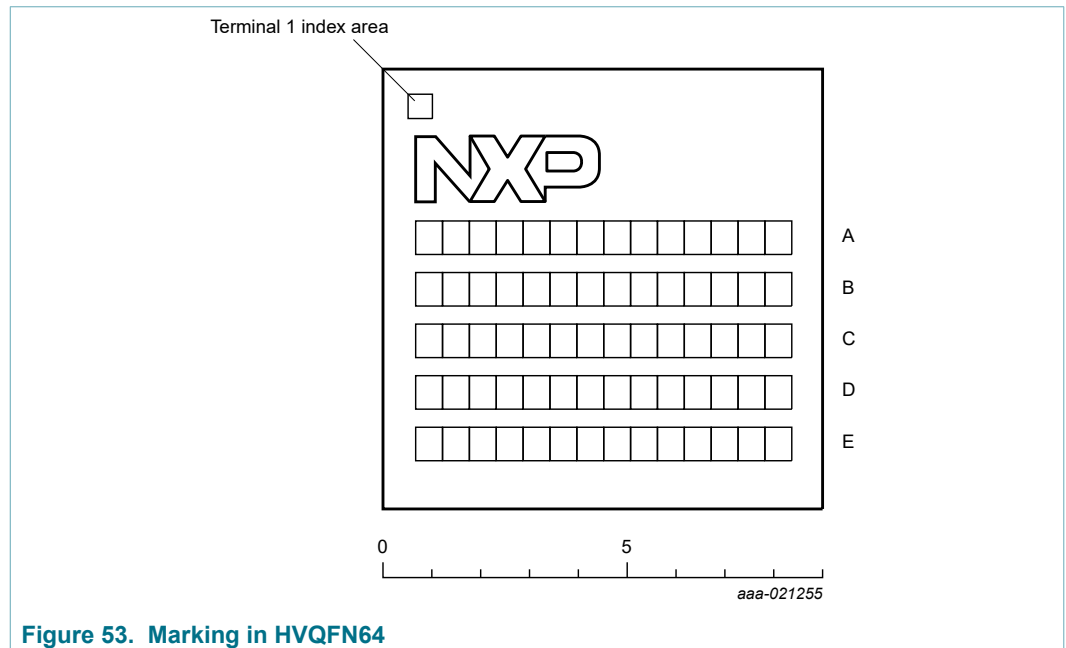


Figure 53. Marking in HVQFN64

14.2 Marking VFBGA64

Table 81. Marking codes

| Type number | Line | Marking code |
|-------------|--------|--|
| PN7462AUEV | Line A | 7462x x: means version number |
| PN7362AUEV | | 7362x x: means version number |
| PN7360AUEV | | 7360x x: means version number |
| Common | Line B | DBID+ASID Diffusion batch, 2 digits + Assembly batch, 2digits |
| | Line C | ZSDyywwX Manufacturing code including: <ul style="list-style-type: none"> • Diffusion center code, 1 digit (Z for SSMC) • Assembly center code, 1 digit (S for ATKH) • RoHS compliancy indicator, 1 digit (D: Dark Green; fully compliant RoHS and no halogen and antimony) • Manufacturing year and week, digits: <ul style="list-style-type: none"> – YY: production year – WW: production week code • Product life cycle status code, 1 digit: <ul style="list-style-type: none"> – X: means not qualified product – nothing means released product |

14.2.1 Package marking drawing

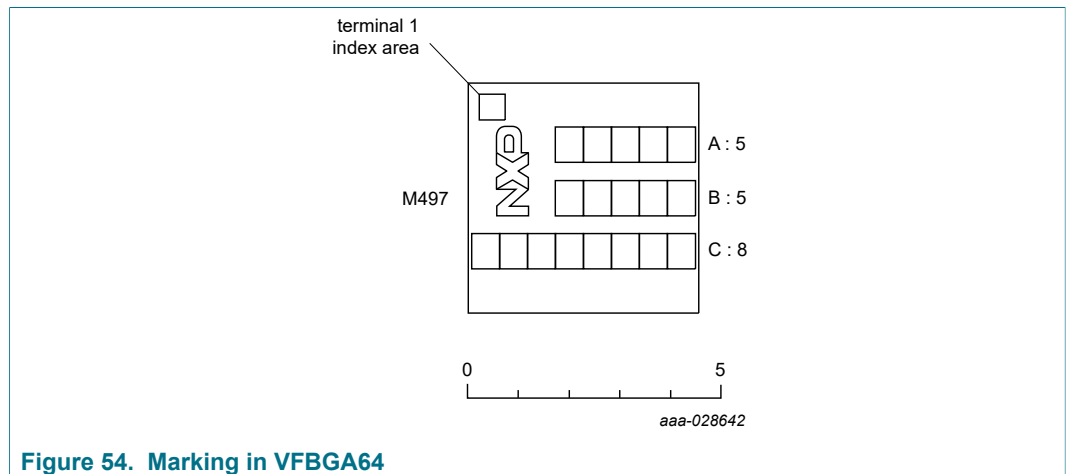


Figure 54. Marking in VFBGA64

15 Package outline HVQFN64

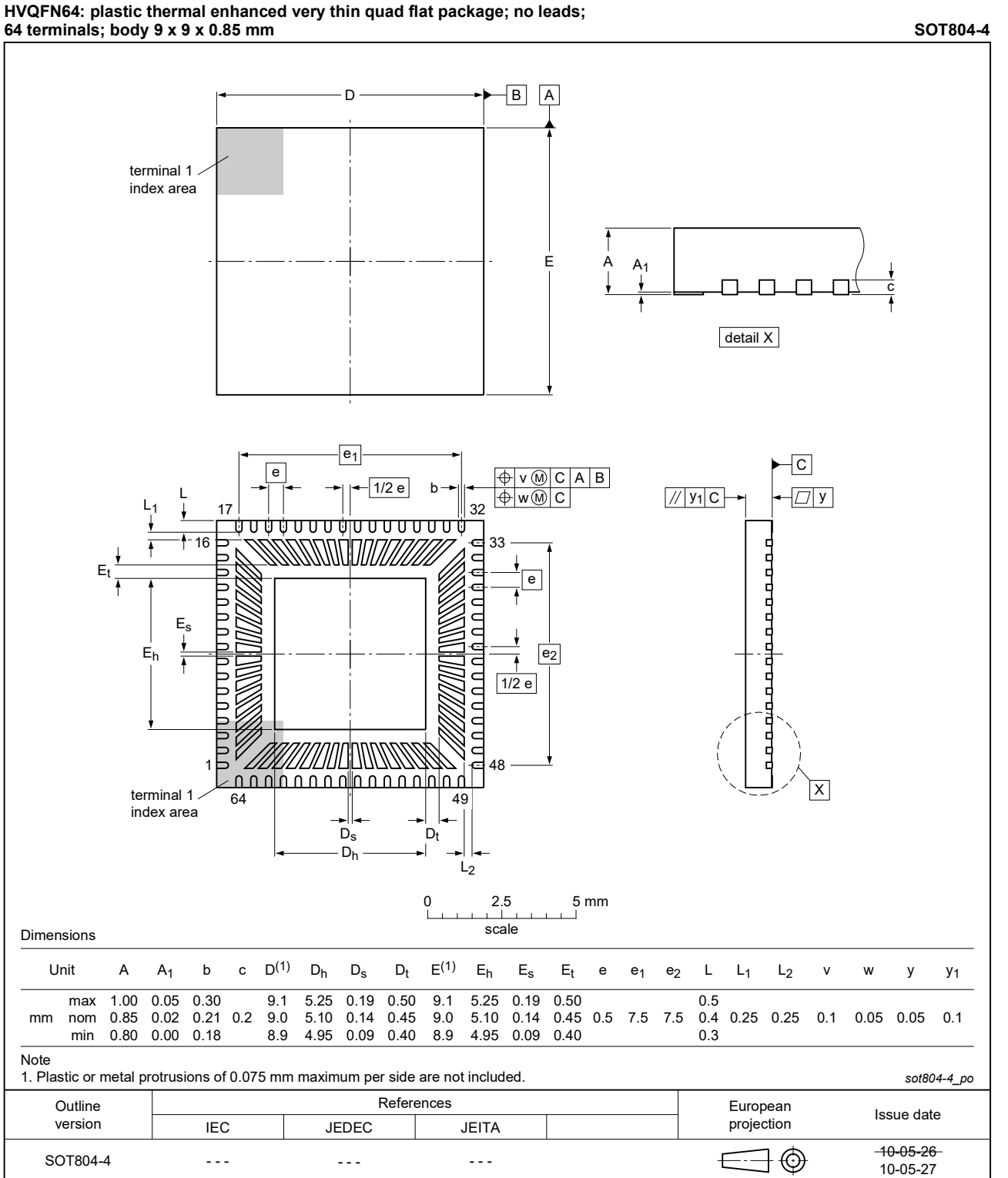


Figure 55. Package outline HVQFN64

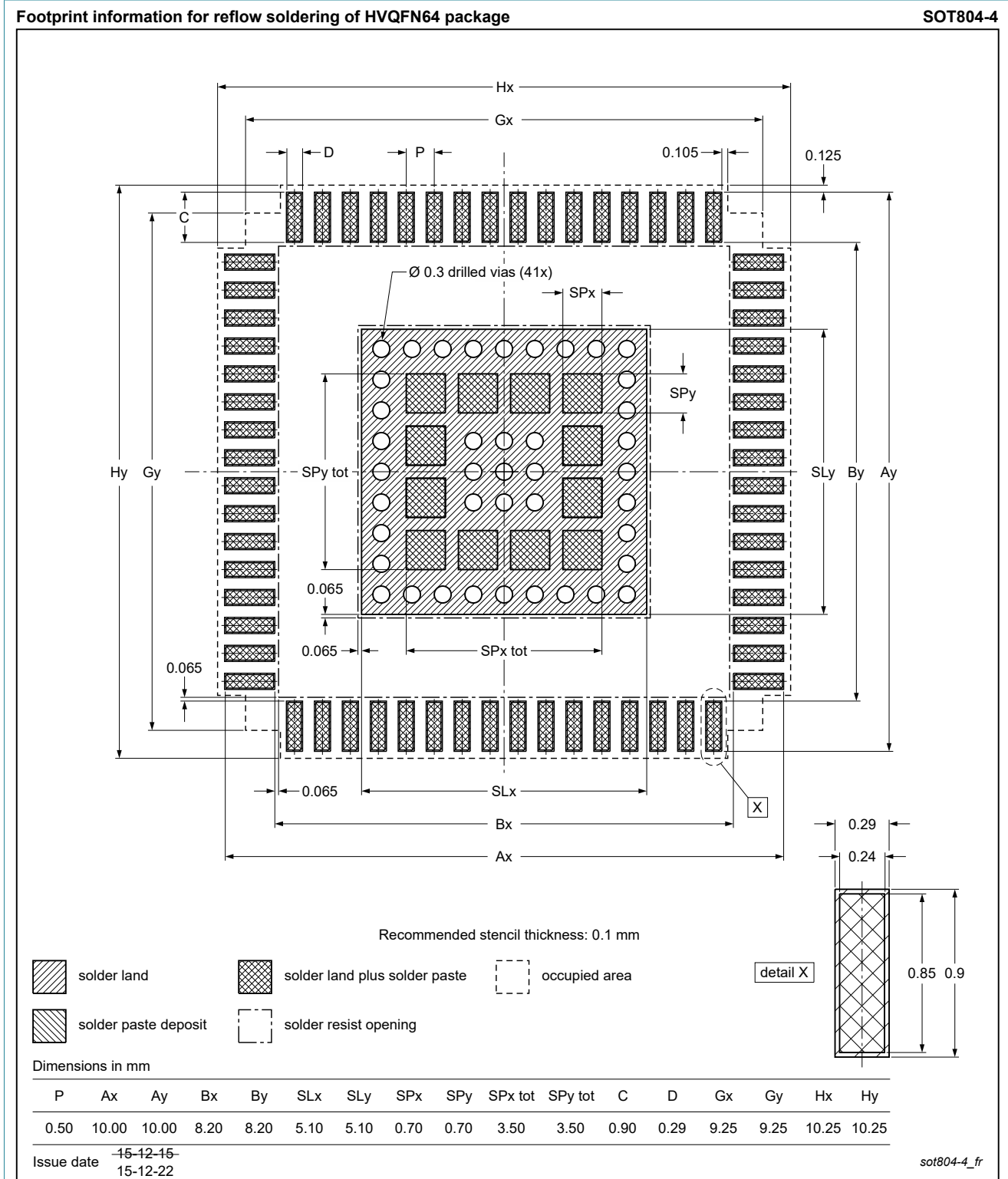


Figure 56. Footprint information for reflow soldering of HVQFN64

16 Package outline VFBGA64

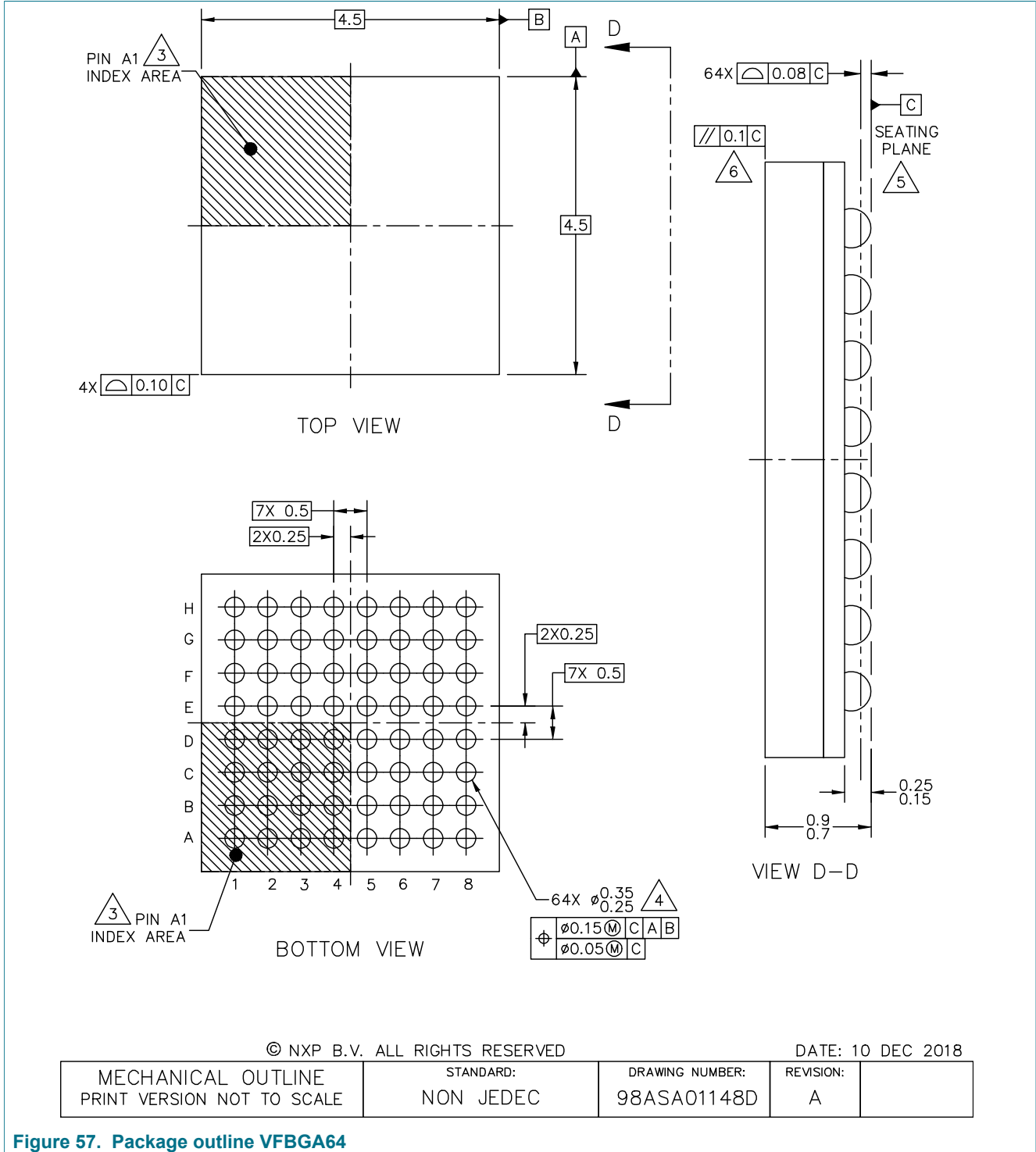


Figure 57. Package outline VFBGA64

17 Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

18 Packing information

18.1 Packing information HVQFN64

Moisture Sensitivity Level (MSL) evaluation has been performed according to JEDEC J-STD-020C. MSL for this package is level 3 which means 260 °C Pb-free convection reflow maximum temperature peak.

Dry packing is required with following floor conditions: 168 hours out of bag floor life at maximum ambient temperature 30 °C/60 % RH.

For information on packing, refer to the PIP relating to this product at <http://www.nxp.com>.

18.2 Packing information VFBGA64

Moisture Sensitivity Level (MSL) evaluation has been performed according to JEDEC J-STD-020C. MSL for this package is level 3 which means 260 °C Pb-free convection reflow maximum temperature peak.

Dry packing is required with following floor conditions: 168 hours out of bag floor life at maximum ambient temperature 30°C/60 % RH.

For information on packing, refer to the PIP relating to this product at <http://www.nxp.com>.

19 Abbreviations

Table 82. Abbreviations

| Acronym | Description |
|------------------|---|
| ADC | Analog to Digital Convertor |
| ALM | Active Load Modulation |
| ASK | Amplitude Shift Keying |
| BPSK | Binary Phase Shift Keying |
| CLIF | Contactless Interface |
| CRC | Cyclic Redundancy Check |
| DPC | Dynamic Power Control |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| GPIO | General-Purpose Input Output |
| I ² C | Inter-Interchanged Circuit |
| IC | Integrated Circuit |
| IAP | In-Application Programming |
| ISP | In-System Programming |
| LDO | Low DropOut |
| LPCD | Low-Power Card Detection |
| MSL | Moisture Sensitivity Level |
| NFC | Near Field Communication |
| NRZ | Non-Return to Zero |
| NVIC | Nested Vectored Interrupt Controller |
| P2P | Peer-to-Peer |
| PLL | Phase-Locked Loop |
| PLM | Passive Load Modulation |
| SPI | Serial Peripheral Interface |
| SWD | Serial Wire Debug |
| UART | Universal Asynchronous Receiver Transmitter |
| USB | Universal Serial Bus |

20 Revision history

Table 83. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-------------------|--|--------------------|---------------|--|
| PN7462_FAM v. 4.5 | 20200414 | Product data sheet | - | PN7462_FAM v. 4.4 |
| Modifications: | <ul style="list-style-type: none"> • Section 8.15.1: Notes added • Figure 35, Figure 36 and Figure 45: updated • Table 23: PVDD_IN removed | | | |
| PN7462_FAM v. 4.4 | 20190611 | Product data sheet | - | PN7462_FAM v. 4.3 |
| Modifications: | <ul style="list-style-type: none"> • Clarified chapter about system tick timer. • Added information about peak current at Transmitter LDO and RF Transmitter. • Added thermal characteristics for Ψ_{j-top}. | | | |
| PN7462_FAM v. 4.3 | 20190124 | Product data sheet | - | PN7462_FAM v. 4.2 |
| Modifications: | <ul style="list-style-type: none"> • Corrected AMR values for: VBUS, VBUSP, VUP_TX and USB_VBUS • Added Slew Rates for: VBUS, VUP_TX and VBUSP • Added OVP to USB supply example • Added diagrams for Power-up sequences • Corrected drawing Figure 39, showing the use case where TX_LDO is not used | | | |
| PN7462_FAM v. 4.2 | 20180910 | Product data sheet | - | PN7462_FAM v. 4.1 |
| Modifications: | <ul style="list-style-type: none"> • Marking code of HVQFN64 package in Section 14.1 corrected | | | |
| PN7462_FAM v. 4.1 | 20180628 | Product data sheet | - | PN7462_FAM v. 4.0 and PN7462_FAM incl PN7412 v.3.0 |
| Modifications: | <ul style="list-style-type: none"> • New type PN7412AUHN added • Combined data sheets PN7462_FAM and PN7462_FAM incl PN7412 | | | |
| PN7462_FAM v. 4.0 | 20180201 | Product data sheet | - | PN7462 v. 3.2 and PN736X v. 3.3 |
| Modifications: | <ul style="list-style-type: none"> • Combined data sheets PN736X and PN7462. • Added description about VFBGA64 package versions. | | | |
| PN736X v. 3.3 | 20170907 | Product data sheet | - | PN736X v.3.2 |
| Modifications: | <ul style="list-style-type: none"> • Removed chapter 8.9 "I/O auxiliary - ISO/IEC 7816 UART" which is not available on the product. • Updated Pin description, removed pin functionality INT_AUX, CLK_AUX and IO_AUX • Updated Section 9.5 "Unconnected I/O's", removed description of AUX interface INT_AUX, IO_AUX, CLK_AUX which is not available on the product | | | |
| PN736X v. 3.2 | 20161213 | Product data sheet | - | PN746X_736X v.3.1 |
| Modifications: | <ul style="list-style-type: none"> • Product name title and Descriptive title updated • Editorial changes | | | |
| PN746X_736X v.3.1 | 20160405 | Product data sheet | - | PN746X_736X v.3.0 |
| Modifications: | <ul style="list-style-type: none"> • Descriptive title updated • Section 1 "General description": updated | | | |
| PN746X_736X v.3.0 | 20160330 | Product data sheet | - | - |

21 Legal information

21.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
 [2] The term 'short data sheet' is explained in section "Definitions".
 [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

21.2 Definitions

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- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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