



**SPECIFICATIONS<sup>1</sup>****Absolute Maximum Ratings<sup>2,3</sup>**

Positive Supply Voltage ( $V_{CC}$ )	+20 V	Lead Temp. ( $T_{LEAD}$ ) (Soldering 10 sec)	260 °C
Negative Supply Voltage ( $V_{EE}$ )	-20 V	Operating Temperature Range ( $T_{OP}$ )	-40 to +85°C
Input Voltage ( $V_{IN\ MAX}$ )	$V_{CC} + 0.5V, V_{EE} - 0.5V$	Storage Temperature Range ( $T_{ST}$ )	-40 to +125°C
Output Short-Circuit Duration ( $t_{SH}$ )	Continuous	Junction Temperature ( $T_J$ )	150°C

**Recommended Operating Conditions**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Positive Supply Voltage	$V_{CC}$		+5		+20	V
Negative Supply Voltage	$V_{EE}$		-5		-20	V

**Electrical Characteristics<sup>2</sup>**

Parameter	Symbol	Conditions	1510			1512			Units
			Min	Typ	Max	Min	Typ	Max	
Supply Current	$I_{CC}, -I_{EE}$	No signal	—	6.0	7.9	—	6.0	7.9	mA
		$V_{CC} = -V_{EE} = 20V$	—	—	8.0	—	—	8.0	mA
Input Bias Current	$I_B$	No signal; Either input connected to GND	—	4.8	14	—	4.8	14	µA
Input Offset Current	$I_{B-OFF}$	No signal	-1.4	—	+1.4	-1.4	—	+1.4	µA
Offset Voltage									
Output Stage Output Offset	$V_{OSOO}$	No Signal, $V_{CM}=0$	-5	—	+5	-5	—	+5	mV
Input Stage Input Offset	$V_{OSII}$		-250	—	+250	-250	—	+250	µV
Total Output Offset		G=voltage gain	-5-0.25G		5+0.25G	-5-0.25G		5+0.25G	mV
Input Voltage Range	$V_{IN-CM}$	Common mode, all gains	—	± 13	—	—	± 13	—	V
Differential Mode	$V_{IN-UNBAL}$	Unbalanced One input to GND, 0dB gain	-13	—	+13	-13	—	+13	V
Differential Gain	$G_{diff}$		0	—	70	-6	—	64	dB
Ref Input Voltage Range			—	± 8	—	—	± 8	—	V
Ref Input Impedance			—	10	—	—	15	—	kΩ
Ref Input Gain to Output			—	0	—	—	0	—	dB
Input Impedance	$Z_{IN-DIFF}$	Differential							
		0dB gain	—	32  1.9	—	—	37  1.9	—	MΩ  pF
		20dB gain	—	32  2.0	—	—	37  2.0	—	MΩ  pF
		40dB gain	—	32  2.5	—	—	36  3.1	—	MΩ  pF
	60dB gain	—	29  8.0	—	—	31  13.9	—	MΩ  pF	
	$Z_{IN-CM}$	Common mode all gains	—	8  7.7	—	—	9  7.7	—	MΩ  pF

1. All specifications are subject to change without notice.

2. Unless otherwise noted,  $T_A=25^\circ\text{C}$ ,  $V_{CC}=+15V$ ,  $V_{EE}=-15V$ .

3. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<b>Electrical Characteristics (con't)<sup>2</sup></b>										
Parameter	Symbol	Conditions	1510			1512			Units	
			Min	Typ	Max	Min	Typ	Max		
Common Mode Rejection	CMR	$V_{CM} = \pm 10V$ ; DC to 60 Hz	0 dB gain	45	60	—	45	60	—	dB
			20 dB gain	65	80	—	65	80	—	dB
			40 dB gain	85	100	—	85	100	—	dB
			60 dB gain	105	120	—	105	120	—	dB
Power Supply Rejection	PSR	$V_{CC} = -V_{EE}$ ; $\pm 5V$ to $\pm 20V$ ; DC to 60 Hz	0 dB gain	—	85	—	—	60	—	dB
			20 dB gain	—	105	—	—	105	—	dB
			40 dB gain	—	120	—	—	120	—	dB
			60 dB gain	—	124	—	—	124	—	dB
Total Harmonic Distortion	THD+N	$V_{OUT} = 7V_{rms}$ ; $R_L = 5 k\Omega$ $f = 1kHz$ ; $BW = 20 kHz$	0 dB gain	—	0.0005	—	—	0.001	—	%
			20 dB gain	—	0.0012	—	—	0.004	—	%
			40 dB gain	—	0.0016	—	—	0.005	—	%
			60 dB gain	—	0.005	—	—	0.008	—	%
Equivalent Input Noise	$e_{n(IN)}$	$f = 1kHz$ , 0 dB gain	0 dB gain	—	57	—	—	34	—	nV/ $\sqrt{Hz}$
			20 dB gain	—	7	—	—	4.6	—	nV/ $\sqrt{Hz}$
			40 dB gain	—	1.7	—	—	1.4	—	nV/ $\sqrt{Hz}$
			60 dB gain	—	1	—	—	1	—	nV/ $\sqrt{Hz}$
Input Current Noise	$i_{n(IN)}$	60 dB gain	—	2.0	—	—	2.0	—	pA/ $\sqrt{Hz}$	
Noise Figure	NF	60 dB gain	—	1.6	—	—	1.6	—	dB	
		$R_S = 150 \Omega$ $R_S = 200 \Omega$	—	1.3	—	—	1.3	—	dB	
Slew Rate	SR	$R_L = 2 k\Omega$ $C_L = 50 pF$	13	19	—	13	19	—	V/ $\mu s$	
Bandwidth -3dB	$BW_{-3dB}$	$R_L = 2 k\Omega$ ; $C_L = 10 pF$	0 dB gain	—	15	—	—	11	—	MHz
			20 dB gain	—	8	—	—	9	—	MHz
			40 dB gain	—	7	—	—	7	—	MHz
			60 dB gain	—	3	—	—	1.6	—	MHz
Output Gain Error	$G_{ER (OUT)}$	$f = 1kHz$ ; $R_L = 2 k\Omega$	$R_G = \infty$ , $G=0 dB$	-0.5	—	+0.5	—	—	—	dB
			$R_G = 1.1 k\Omega$ , $G=20 dB$	-0.5	—	+0.5	—	—	—	dB
			$R_G = 101 \Omega$ , $G=40 dB$	-0.5	—	+0.5	—	—	—	dB
			$R_G = 10 \Omega$ , $G=60 dB$	-0.5	—	+0.5	—	—	—	dB
			$R_G = 10 k\Omega$ , $G=0 dB$	—	—	—	-0.5	—	+0.5	dB
			$R_G = 526.3 \Omega$ , $G=20 dB$	—	—	—	-0.5	—	+0.5	dB
			$R_G = 50.3 \Omega$ , $G=40 dB$	—	—	—	-0.5	—	+0.5	dB
			$R_G = 5 \Omega$ , $G=60 dB$	—	—	—	-0.5	—	+0.5	dB
Output Voltage Swing	$V_O$	$R_L = 2 k\Omega$ all gains	$\pm 13$	$\pm 13.3$	—	$\pm 13$	$\pm 13.3$	—	V	
Output Short Circuit Current	$I_{SC}$	$R_L = 0 \Omega$	—	$\pm 17$	—	—	$\pm 17$	—	mA	
Minimum Resistive Load	$R_{Lmin}$		2	—	—	2	—	—	k $\Omega$	
Maximum Capacitive Load	$C_{Lmax}$		—	—	300	—	—	300	pF	
Gain Equation			$A_V = 1 + \frac{10 k\Omega}{R_G}$			$A_V = 0.5 + \frac{5 k\Omega}{R_G}$				

## Applications

### Gain Setting

A single external resistor ( $R_G$ ) between the  $R_{G1}$  and  $R_{G2}$  pins is all that is needed to set the gain of the THAT 1510/1512, according to the formulae:

$$\text{for the 1510: } A_V = 1 + \frac{10k\Omega}{R_G} \quad \text{or}$$

$$\text{for the 1512: } A_V = 0.5 + \frac{5k\Omega}{R_G} \quad \text{where}$$

$A_V$  is the voltage gain of the part.

Either part may reach unity gain, but the value of  $R_G$  required varies significantly between the two parts. For the 1510, gain is 0dB when  $R_G$  is infinite (open); this is the minimum gain for the 1510. At infinite  $R_G$ , the 1512 reaches -6dB gain; this is the minimum gain for the 1512. With  $R_G=10k\Omega$ , the 1512 reaches 0dB gain.

Overall gain accuracy depends on the tolerance of  $R_G$  and the accuracy of the internal thin-film resistors connected to pins  $R_{G1}$  and  $R_{G2}$  in the 1510/1512 ( $R_A$  &  $R_B$  in Figure 1). These internal resistors have a typical initial accuracy (at room temperature) of  $\pm 0.5\%$ , and are typically stable with temperature to within  $\pm 100$  ppm/ $^{\circ}\text{C}$ . Gain will drift with temperature based on the mismatch between the temperature coefficient of the external  $R_G$  and that of the internal resistors  $R_A$  &  $R_B$ .

For variable-gain applications where gain accuracy is important, THAT recommends using discrete, switched resistors for  $R_G$ . Where continuous control is required, or where gain accuracy is less

critical, a potentiometer may be used. In such applications, designers should take care in specifying the element construction to avoid excess noise. The potentiometer taper will set the circuit's characteristic of gain vs. pot rotation. Typically, reverse log (reverse audio) taper elements offer the desired behavior in which gain increases with clockwise rotation (and lower values for  $R_G$ ). See THAT Design Note 138 for a discussion of potentiometer taper and gain for the 1510 and 1512 compared to similar parts from other manufacturers.

### Noise Performance

Both parts exhibit excellent voltage noise performance of  $\sim 1$  nV/ $\sqrt{\text{Hz}}$  at high gains. With  $\sim 2$  pA/ $\sqrt{\text{Hz}}$  current noise, they are optimized for relatively low source impedance applications, such as dynamic microphones with typically a few hundred ohm output impedances. But, because they have different internal gain structures, the 1510 has higher equivalent input noise at 0dB gain ( $\sim 57$  nV/ $\sqrt{\text{Hz}}$ ) than the 1512, which runs 4.5 dB lower at  $\sim 34$  nV/ $\sqrt{\text{Hz}}$ . The unusual and superior topology of the THAT 1512 makes its noise performance comparable to some of the better discrete designs currently available.

### Inputs

#### Simple Configurations

As shown in Figure 2, the 1510/1512 includes protection diodes at all pins except  $V+$  and  $V-$ .



Figure 2. THAT 1510 / 1512 Equivalent Circuit with Protection Diodes



Figure 3. Basic 1510 / 1512 Circuit

These diodes reduce the likelihood that accidental electrostatic discharge (ESD) or electrical over stress (EOS) will damage the ICs. Other diodes across the base-emitter junctions of the input transistors prevent excessive reverse biasing of these junctions (which would degrade the noise performance of the input devices).

Other than the protection diodes, the 1510/1512 input pins are connected only to the bases of their respective input devices. For proper operation, the bases must be provided a source of dc bias that will maintain the inputs within the IC's input common-mode range. Figure 3 shows the simplest approach; dc bias is supplied via  $R_1$  and  $R_2$ . At 1 k $\Omega$  each, they will minimize pickup of unwanted noise and interference, as well as generate relatively little noise due to input current noise in the 1510/1512. However, at high gains, their inherent voltage noise, plus the 1510/1512's input current noise drawn across these resistors, adds significantly to the noise at the 1510/1512's output.

Because  $R_G$  is dc coupled in the circuit of Figure 3, the dc level at the output of the 1510/1512 will vary with gain. In most applications, the output should be ac-coupled to the next stage. For applications where  $R_G$  is variable (via a pot or switched

resistors) to allow gain adjustment,  $R_G$  should be ac-coupled as shown in Figure 4. By adding  $C_G$  in series with  $R_G$ , dc gain is fixed (at unity for the 1510, and  $\frac{1}{2}$  for the 1512). This constrains the output dc offset to just over  $\pm 5$  mV, and prevents it from varying with gain. With this low offset, ac coupling of the output is usually unnecessary.

$C_G$  must be large enough not to interfere with low-frequency response at the smallest values of  $R_G$ . For 60 dB gain,  $R_G=10 \Omega$  (1510) or  $R_G=5 \Omega$  (1512). For a -3 dB point of approximately 5 Hz,  $C_G=3,300 \mu\text{F}$  (1510), or  $C_G=6,800 \mu\text{F}$  (1512). For other maximum gains or minimum frequencies, scale  $C_G$  accordingly.

### Phantom Power

Phantom power is required for many condenser microphones. THAT recommends the circuit of Figure 5 when phantom power is included<sup>4</sup>.  $R_3$ ,  $R_4$ , and  $D_1 - D_6$  are used to limit the current that flows through the 1510/1512 inputs when the circuit inputs (-In and +In) are shorted to ground while phantom power is turned on. This causes  $C_4$  and/or  $C_5$  to discharge through other circuit components, often generating transient currents of several amps.  $R_3$  and  $R_4$  should be at least 10  $\Omega$  to limit destructive

4. In revisions 0 and 1 of this data sheet, we recommended using Schottky diodes (1N5819 types) at  $D_1 - D_4$  to protect the 1510/1512 inputs against overloads. Subsequently, we discovered that the leakage of these diodes could cause problems with DC fluctuations (hence noise) at the 1510/1512 output. Upon further investigation, we concluded that conventional rectifier diodes like the 1N4004 (the glass-passivated GP version) provide adequate protection and do not introduce unacceptable leakage. Additionally, 1N4004 diodes are much cheaper and more readily available than the Schottky types.

Since publishing revision 4, we determined that the internal reverse-bias diodes between the pins +In/ $R_2$  and -In/ $R_1$  may be damaged by phantom power faults under certain conditions. Small-signal diodes ( $D_5$  and  $D_6$ ) avoid this problem by appearing in parallel with the internal diodes, diverting excess current around the 1510/1512.

currents. (Higher values further limit current flow, but introduce additional source impedance and noise.)  $D_1$  through  $D_4$  prevent the IC's inputs from significantly exceeding the supply rails.  $D_5$  and  $D_6$  steer currents around the input stage in the 1510/1512, preventing damage.

The series combination of  $C_4$  and  $C_5$  should be made large to minimize high-pass filtering of the signal based upon the sum of the values of  $R_1+R_2$ . As well, keeping their reactance low relative to the external microphone's source impedance will avoid increasing the effects of low-frequency current noise in the 1510/1512 input stage.

Other manufacturers have recommended, and many pro audio products include, a zener diode arrangement connected to the bridge rectifier instead of the connection to  $V+$  and  $V-$  as shown in Figure 5. THAT does not recommend this approach, because we find that  $R_3$  and  $R_4$  must be made much larger (e.g.,  $\geq 51 \Omega$ ) in order to limit peak currents enough to protect reasonably sized zener diodes (eg. 1/2 W). Such large series input resistors will limit the noise performance of the preamp. The ultimate floor is set by the impedance of the microphone, but any additional series resistance further degrades performance.

For further insights into this subject, see the Audio Engineering Society preprints "The 48 Volt Phantom Menace," by Gary K. Hebert and Frank W.

Thomas, presented at the 110th AES Convention and "The 48 Volt Phantom Menace Returns", by Rosalfonso Bortoni and Wayne Kirkwood presented at the 127th AES Convention.

### Impedance and Line Input Configurations

A higher common-mode input impedance is desirable (compared with that of Figures 3 and 4) when input coupling capacitors ( $C_4$  and  $C_5$ ) are used to block phantom power. At low frequencies where the reactance of  $C_4$  and  $C_5$  become significant (compared to the common-mode input impedances), the two capacitors interact with the common-mode input impedance (seen looking to the right-side of both capacitors) to form voltage dividers for common-mode signals. Differences in the two capacitors' values leads to different voltage dividers, spoiling the low-frequency common-mode rejection of the stage. Since  $C_4$  and  $C_5$  are generally large, electrolytic types, precise matching is difficult and expensive to achieve. High common-mode input impedance reduces the matching requirement by decreasing the frequency at which the capacitive reactance becomes significant inversely with the common-mode input impedance.

The "T-bias" circuit ( $R_1$ ,  $R_2$ , and  $R_7$ ) shown in Figure 5 accommodates this objective. In this circuit,  $R_1$  and  $R_2$  are connected to a third resistor  $R_7$ , boosting the low-frequency common mode input

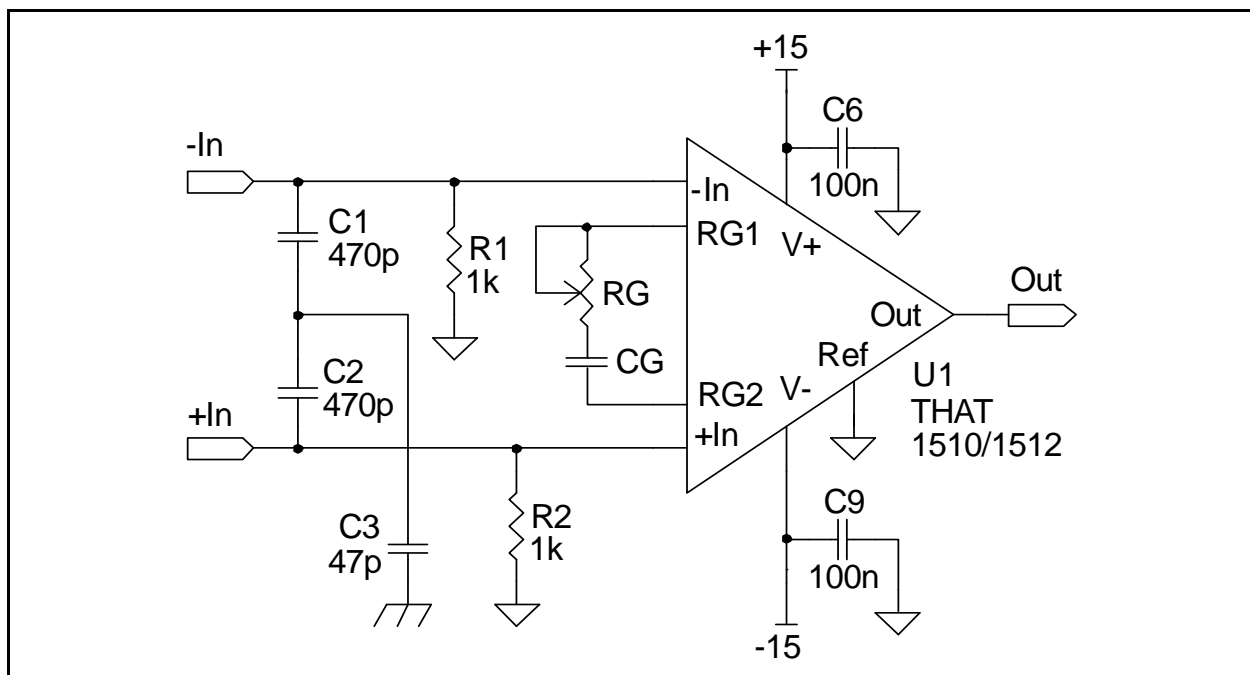


Figure 4. Basic 1510 / 1512 Circuit with Variable Gain

impedance (as "seen looking in" from the coupling capacitors) to the value of  $R_1 + (2 \cdot R_7)$  -- approximately 45 k $\Omega$  with the values shown. The increased common mode impedance from T-bias improves LF common mode rejection by reducing capacitor matching requirements by more than a factor of ten over the simpler circuit wherein  $R_7=0 \Omega$ . The circuit works well with the values shown.

Note also that the overall common-mode input impedance of the circuit is dominated by the phantom-power resistors ( $R_5$  and  $R_6$ ). For the circuit of Figure 5, this is approximately 5.9 k $\Omega$  per leg.

The 1510/1512 can be used as a line input receiver by adding attenuation to the preamplifier inputs and changing the circuit topology to allow

switching of input, fixed attenuation, and gain adjustment. The optimum circuit depends on the specific requirements of the application. For more details and specific applications advice, please consult THAT's application notes, or our applications engineers at the address and telephone below or via email at [apps\\_support@thatcorp.com](mailto:apps_support@thatcorp.com).

### Reference Terminal

The "Ref" pin provides a reference for the output signal, and is normally connected to analog ground. If necessary, the "Ref" pin can be used for offset correction or DC level shifting. However, in order to prevent spoiling the excellent common-mode rejection of the 1510/1512, the source impedance driving the "Ref" pin should be under 1 $\Omega$ .



Figure 5. Recommended 1510 / 1512 Circuit with Phantom Power

## Package Information

Both the THAT 1510 and 1512 are available in 8-pin SOIC, 8-pin DIP, and 14-pin SOIC packages. The 1510 is also available in a 16-pin (widebody) SOIC package. Other version/package combinations will be considered based on customer demand.

The package dimensions are shown in Figures 6, 7, 8, & 9, while pinouts are given in Table 1.

All versions of the 1510 and 1512 are lead free and RoHS compliant. Material Declaration Data Sheets on the parts are available at our web site, [www.thatcorp.com](http://www.thatcorp.com) or upon request.



Figure 6. 8-pin DIP package outline



Figure 7. 16-pin SO Wide package outline



Figure 8. 8-pin SOIC package outline



Figure 9. 14-pin SOIC package outline

### Revision History

Revision	ECO	Date	Changes	Page
07	2322	9/16/09	Added Max. Input Voltage specification.	2
08	2829	10/02/13	Corrected typographical error in specification table.	3



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