



Device Overview

The 89HPES32H8G2 is a member of the IDT PRECISE™ family of PCI Express® switching solutions. The PES32H8G2 is a 32-lane, 8-port system interconnect switch optimized for PCI Express Gen2 packet switching in high-performance applications, supporting multiple simultaneous peer-to-peer traffic flows. Target applications include servers, storage, communications, embedded systems, and multi-host or intelligent I/O based systems with inter-domain communication.

Features

◆ High Performance Non-Blocking Switch Architecture

- 32-lane 8-port PCIe switch
 - *Four x8 switch ports each of which can bifurcate to two x4 ports (total of eight x4 ports)*
- Integrated SerDes supports 5.0 GT/s Gen2 and 2.5 GT/s Gen1 operation
- Delivers up to 32 GBps (256 Gbps) of switching capacity
- Supports 128 Bytes to 2 KB maximum payload size
- Low latency cut-through architecture
- Supports one virtual channel and eight traffic classes

◆ Standards and Compatibility

- PCI Express Base Specification 2.0 compliant
- Implements the following optional PCI Express features
 - *Advanced Error Reporting (AER) on all ports*
 - *End-to-End CRC (ECRC)*
 - *Access Control Services (ACS)*
 - *Power Budgeting Enhanced Capability*
 - *Device Serial Number Enhanced Capability*
 - *Sub-System ID and Sub-System Vendor ID Capability*
 - *Internal Error Reporting ECN*
 - *Multicast ECN*
 - *VGA and ISA enable*
 - *L0s and L1 ASPM*
 - *ARI ECN*

◆ Port Configurability

- x4 and x8 ports
 - *Ability to merge adjacent x4 ports to create a x8 port*
- Automatic per port link width negotiation (x8 → x4 → x2 → x1)
- Crosslink support
- Automatic lane reversal
- Autonomous and software managed link width and speed control
- Per lane SerDes configuration
 - *De-emphasis*

- *Receive equalization*
- *Drive strength*

◆ Switch Partitioning

- IDT proprietary feature that creates logically independent switches in the device
- Supports up to 8 fully independent switch partitions
- Configurable downstream port device numbering
- Supports dynamic reconfiguration of switch partitions
 - *Dynamic port reconfiguration (downstream, and upstream)*
 - *Dynamic migration of ports between partitions*
 - *Movable upstream port within and between switch partitions*

◆ Initialization / Configuration

- Supports Root (BIOS, OS, or driver), Serial EEPROM, or SMBus switch initialization
- Common switch configurations are supported with pin strapping (no external components)
- Supports in-system Serial EEPROM initialization/programming

◆ Quality of Service (QoS)

- Port arbitration
 - *Round robin*
- Request metering
 - *IDT proprietary feature that balances bandwidth among switch ports for maximum system throughput*
- High performance switch core architecture
 - *Combined Input Output Queued (CIOQ) switch architecture with large buffers*

◆ Multicast

- Compliant to the PCI-SIG multicast ECN
- Supports arbitrary multicasting of Posted transactions
- Supports 64 multicast groups
- Multicast overlay mechanism support
- ECRC regeneration support

◆ Clocking

- Supports 100 MHz and 125 MHz reference clock frequencies
- Flexible port clocking modes
 - *Common clock*
 - *Non-common clock*
 - *Local port clock with SSC and port reference clock input*

◆ Hot-Plug and Hot Swap

- Hot-plug controller on all ports
 - *Hot-plug supported on all downstream switch ports*
- All ports support hot-plug using low-cost external I²C I/O expanders

- Configurable presence detect supports card and cable applications
- GPE output pin for hot-plug event notification
 - *Enables SCI/SMI generation for legacy operating system support*
- Hot-swap capable I/O
- ◆ **Power Management**
 - Supports D0, D3hot and D3 power management states
 - Active State Power Management (ASPM)
 - *Supports L0, L0s, L1, L2/L3 Ready and L3 link states*
 - *Configurable L0s and L1 entry timers allow performance/power-savings tuning*
 - Supports PCI Express Power Budgeting Capability
 - SerDes power savings
 - *Supports low swing / half-swing SerDes operation*
 - *SerDes optionally turned-off in D3hot*
 - *SerDes associated with unused ports are turned-off*
 - *SerDes associated with unused lanes are placed in a low power state*
- ◆ **9 General Purpose I/O**
- ◆ **Reliability, Availability and Serviceability (RAS)**
 - ECRC support
 - AER on all ports
 - SECDED ECC protection on all internal RAMs
 - End-to-end data path parity protection
 - Checksum Serial EEPROM content protected
 - Autonomous link reliability (preserves system operation in the presence of faulty links)
 - Ability to generate an interrupt (INTx or MSI) on link up/down transitions
- ◆ **Test and Debug**
 - On-chip link activity and status outputs available for Port 0 (upstream port)
 - Per port link activity and status outputs available using external I²C I/O expander for all other ports
 - SerDes test modes
 - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
- ◆ **Power Supplies**
 - Requires only two power supply voltages (1.0 V and 2.5 V)
Note that a 3.3V is preferred for V_{DD}I/O
 - No power sequencing requirements
- ◆ **Packaged in a 23mm x 23mm 484-ball Flip Chip BGA with 1mm ball spacing**

Product Description

Utilizing standard PCI Express interconnect, the PES32H8G2 provides the most efficient fan-out solution for applications requiring high throughput, low latency, and simple board layout with a minimum number of board layers. It provides 32 GBps (256 Gbps) of aggregated, full-duplex switching capacity through 32 integrated serial lanes, using proven and robust IDT technology. Each lane provides 5 GT/s of bandwidth in both directions and is fully compliant with PCI Express Base Specification, Revision 2.0.

The PES32H8G2 is based on a flexible and efficient layered architecture. The PCI Express layer consists of SerDes, Physical, Data Link and Transaction layers in compliance with PCI Express Base specification Revision 2.0. The PES32H8G2 can operate either as a store and forward or cut-through switch. It supports eight Traffic Classes (TCs) and one Virtual Channel (VC) with sophisticated resource management to enable efficient switching and I/O connectivity for servers, storage, and embedded processors with limited connectivity.

The PES32H8G2 is a *partitionable* PCIe switch. This means that in addition to operating as a standard PCI express switch, the PES32H8G2 ports may be partitioned into groups that logically operate as completely independent PCIe switches. Figure 2 illustrates a three partition PES32H8G2 configuration.

Block Diagram

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Figure 1 Internal Block Diagram



Figure 2 Example of Usage of Switch Partitioning

SMBus Interface

The PES32H8G2 contains two SMBus interfaces. The slave interface provides full access to the configuration registers in the PES32H8G2, allowing every configuration register in the device to be read or written by an external agent. The master interface allows the default configuration register values of the PES32H8G2 to be overridden following a reset with values programmed in an external serial EEPROM. The master interface is also used by an external Hot-Plug I/O expander.

Each of the two SMBus interfaces contain an SMBus clock pin and an SMBus data pin. In addition, the slave SMBus has SSMBADDR1 and SSMBADDR2 pins. As shown in Figure 3, the master and slave SMBuses may only be used in a split configuration.

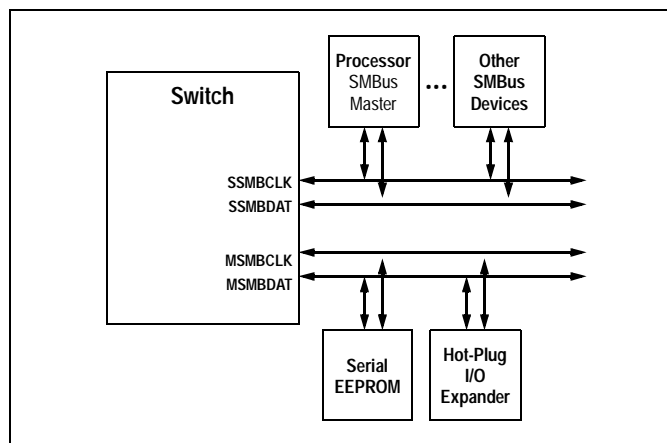


Figure 3 Split SMBus Interface Configuration

The switch's SMBus master interface does not support SMBus arbitration. As a result, the switch's SMBus master must be the only master in the SMBus lines that connect to the serial EEPROM and I/O expander slaves. In the split configuration, the master and slave SMBuses operate as two independent buses; thus, multi-master arbitration is not required.

Hot-Plug Interface

The PES32H8G2 supports PCI Express Hot-Plug on each downstream port. To reduce the number of pins required on the device, the PES32H8G2 utilizes an external I/O expander, such as that used on PC motherboards, connected to the SMBus master interface. Following reset and configuration, whenever the state of a Hot-Plug output needs to be modified, the PES32H8G2 generates an SMBus transaction to the I/O expander with the new value of all of the outputs. Whenever a Hot-Plug input changes, the I/O expander generates an interrupt which is received on the IOEX-PINTN input pin (alternate function of GPIO) of the PES32H8G2. In response to an I/O expander interrupt, the PES32H8G2 generates an SMBus transaction to read the state of all of the Hot-Plug inputs from the I/O expander.

General Purpose Input/Output

The PES32H8G2 provides 9 General Purpose Input/Output (GPIO) pins that may be used by the system designer as bit I/O ports. Each GPIO pin may be configured independently as an input or output through software control. Some GPIO pins are shared with other on-chip functions. These alternate functions may be enabled via software, SMBus slave interface, or serial configuration EEPROM.

Pin Description

The following tables list the functions of the pins provided on the PES32H8G2. Some of the functions listed may be multiplexed onto the same pin. The active polarity of a signal is defined using a suffix. Signals ending with an "N" are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

| Signal | Type | Name/Description |
|----------------------------|------|--|
| PE00RP[3:0] PE00RN[3:0] | I | PCI Express Port 0 Serial Data Receive. Differential PCI Express receive pairs for port 0. |
| PE00TP[3:0] PE00TN[3:0] | O | PCI Express Port 0 Serial Data Transmit. Differential PCI Express transmit pairs for port 0. |
| PE01RP[3:0] PE01RN[3:0] | I | PCI Express Port 1 Serial Data Receive. Differential PCI Express receive pairs for port 1. When port 0 is merged with port 1, these signals become port 0 receive pairs for lanes 4 through 7. |
| PE01TP[3:0] PE01TN[3:0] | O | PCI Express Port 1 Serial Data Transmit. Differential PCI Express transmit pairs for port 1. When port 0 is merged with port 1, these signals become port 0 transmit pairs for lanes 4 through 7. |
| PE02RP[3:0] PE02RN[3:0] | I | PCI Express Port 2 Serial Data Receive. Differential PCI Express receive pairs for port 2. |
| PE02TP[3:0] PE02TN[3:0] | O | PCI Express Port 2 Serial Data Transmit. Differential PCI Express transmit pairs for port 2. |
| PE03RP[3:0] PE03RN[3:0] | I | PCI Express Port 3 Serial Data Receive. Differential PCI Express receive pairs for port 3. When port 2 is merged with port 3, these signals become port 2 receive pairs for lanes 4 through 7. |
| PE03TP[3:0] PE03TN[3:0] | O | PCI Express Port 3 Serial Data Transmit. Differential PCI Express transmit pairs for port 3. When port 2 is merged with port 3, these signals become port 2 transmit pairs for lanes 4 through 7. |
| PE04RP[3:0] PE04RN[3:0] | I | PCI Express Port 4 Serial Data Receive. Differential PCI Express receive pairs for port 4. |
| PE04TP[3:0] PE04TN[3:0] | O | PCI Express Port 4 Serial Data Transmit. Differential PCI Express transmit pairs for port 4. |
| PE05RP[3:0] PE05RN[3:0] | I | PCI Express Port 5 Serial Data Receive. Differential PCI Express receive pairs for port 5. When port 4 is merged with port 5, these signals become port 4 receive pairs for lanes 4 through 7. |
| PE05TP[3:0] PE05TN[3:0] | O | PCI Express Port 5 Serial Data Transmit. Differential PCI Express transmit pairs for port 5. When port 4 is merged with port 5, these signals become port 4 transmit pairs for lanes 4 through 7. |
| PE06RP[3:0] PE06RN[3:0] | I | PCI Express Port 6 Serial Data Receive. Differential PCI Express receive pairs for port 6. |
| PE06TP[3:0] PE06TN[3:0] | O | PCI Express Port 6 Serial Data Transmit. Differential PCI Express transmit pairs for port 6. |
| PE07RP[3:0] PE07RN[3:0] | I | PCI Express Port 7 Serial Data Receive. Differential PCI Express receive pairs for port 7. When port 6 is merged with port 7, these signals become port 6 receive pairs for lanes 4 through 7. |
| PE07TP[3:0] PE07TN[3:0] | O | PCI Express Port 7 Serial Data Transmit. Differential PCI Express transmit pairs for port 7. When port 6 is merged with port 7, these signals become port 6 transmit pairs for lanes 4 through 7. |

Table 1 PCI Express Interface Pins

| Signal | Type | Name/Description |
|--------------------------|------|---|
| GCLKN[1:0] GCLKP[1:0] | I | Global Reference Clock. Differential reference clock input pair. This clock is used as the reference clock by on-chip PLLs to generate the clocks required for the system logic. The frequency of the differential reference clock is determined by the GCLKFSEL signal. |
| P[2:0]CLKN P[2:0]CLKP | I | Port Reference Clock. Differential reference clock pair associated with ports 0, 1, and 2. ¹ |

Table 2 Reference Clock Pins

¹. Unused port clock pins should be connected to Vss on the board.

| Signal | Type | Name/Description |
|---------------|------|---|
| MSMBCLK | I/O | Master SMBus Clock. This bidirectional signal is used to synchronize transfers on the master SMBus. |
| MSMBDAT | I/O | Master SMBus Data. This bidirectional signal is used for data on the master SMBus. |
| SSMBADDR[2,1] | I | Slave SMBus Address. These pins determine the SMBus address to which the slave SMBus interface responds. |
| SSMBCLK | I/O | Slave SMBus Clock. This bidirectional signal is used to synchronize transfers on the slave SMBus. |
| SSMBDAT | I/O | Slave SMBus Data. This bidirectional signal is used for data on the slave SMBus. |

Table 3 SMBus Interface Pins

| Signal | Type | Name/Description |
|---------|------|---|
| GPIO[0] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART0PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition. |
| GPIO[1] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART1PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition. |
| GPIO[2] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART2PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition. |

Table 4 General Purpose I/O Pins (Part 1 of 2)

| Signal | Type | Name/Description |
|---------|------|---|
| GPIO[3] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: PART3PERSTN Alternate function pin type: Input/Output Alternate function: Assertion of this signal initiated a partition fundamental reset in the corresponding partition. |
| GPIO[4] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function — Reserved 2nd Alternate function pin name: P0LINKUPN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Up Status output. |
| GPIO[5] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. 1st Alternate function pin name: GPEN 1st Alternate function pin type: Output 1st Alternate function: Hot-plug general purpose even output. 2nd Alternate function pin name: P0ACTIVEN 2nd Alternate function pin type: Output 2nd Alternate function: Port 0 Link Active Status Output. |
| GPIO[6] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. |
| GPIO[7] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. |
| GPIO[8] | I/O | General Purpose I/O. This pin can be configured as a general purpose I/O pin. Alternate function pin name: IOEXPINTN Alternate function pin type: Input Alternate function: IO expander interrupt. |

Table 4 General Purpose I/O Pins (Part 2 of 2)

| Signal | Type | Name/Description |
|--------------|------|---|
| CLKMODE[2:0] | | Clock Mode. These signals determine the port clocking mode used by ports of the device. |
| GCLKFSEL | I | Global Clock Frequency Select. These signals select the frequency of the GCLKP and GCLKN signals. 0x0 100 MHz 0x1 125 MHz |
| P01MERGEN | I | Port 0 and 1 Merge. P01MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 0 is merged with port 1 to form a single x8 port. The Serdes lanes associated with port 1 become lanes 4 through 7 of port 0. When this pin is high, port 0 and port 1 are not merged, and each operates as a single x4 port. |
| P23MERGEN | I | Port 2 and 3 Merge. P23MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 2 is merged with port 3 to form a single x8 port. The Serdes lanes associated with port 3 become lanes 4 through 7 of port 2. When this pin is high, port 2 and port 3 are not merged, and each operates as a single x4 port. |

Table 5 System Pins (Part 1 of 2)

| Signal | Type | Name/Description |
|-------------|------|---|
| P45MERGEN | I | Port 4 and 5 Merge. P45MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 4 is merged with port 5 to form a single x8 port. The Serdes lanes associated with port 5 become lanes 4 through 7 of port 4. When this pin is high, port 4 and port 5 are not merged, and each operates as a single x4 port. |
| P67MERGEN | I | Port 6 and 7 Merge. P67MERGEN is an active low signal. It is pulled low internally. When this pin is low, port 6 is merged with port 7 to form a single x8 port. The Serdes lanes associated with port 7 become lanes 4 through 7 of port 6. When this pin is high, port 6 and port 7 are not merged, and each operates as a single x4 port. |
| PERSTN | I | Global Reset. Assertion of this signal resets all logic inside PES32H8G2. |
| RSTHALT | I | Reset Halt. When this signal is asserted during a PCI Express fundamental reset, PES32H8G2 executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master. |
| SWMODE[3:0] | I | Switch Mode. These configuration pins determine the PES32H8G2 switch operating mode. Note: These pins should be static and not change following the negation of PERSTN. 0x0 - Single partition 0x1 - Single partition with Serial EEPROM initialization 0x2 through 0x7 - Reserved 0x8 - Single partition with port 0 selected as the upstream port (port 2 disabled) 0x9 - Single partition with port 2 selected as the upstream port (port 0 disabled) 0xA - Single partition with Serial EEPROM initialization and port 0 selected as the upstream port (port 2 disabled) 0xB - Single partition with Serial EEPROM initialization and port 2 selected as the upstream port (port 0 disabled) 0xC - Multi-partition 0xD - Multi-partition with Serial EEPROM initialization 0xE - Reserved 0xF - Reserved |

Table 5 System Pins (Part 2 of 2)

| Signal | Type | Name/Description |
|----------|------|---|
| JTAG_TCK | I | JTAG Clock. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic or JTAG Controller. JTAG_TCK is independent of the system clock with a nominal 50% duty cycle. |
| JTAG_TDI | I | JTAG Data Input. This is the serial data input to the boundary scan logic or JTAG Controller. |

Table 6 Test Pins (Part 1 of 2)

| Signal | Type | Name/Description |
|-------------|------|---|
| JTAG_TDO | O | JTAG Data Output. This is the serial data shifted out from the boundary scan logic or JTAG Controller. When no data is being shifted out, this signal is tri-stated. |
| JTAG_TMS | I | JTAG Mode. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. |
| JTAG_TRST_N | I | JTAG Reset. This active low signal asynchronously resets the boundary scan logic and JTAG TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: <ul style="list-style-type: none"> 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board |

Table 6 Test Pins (Part 2 of 2)

| Signal | Type | Name/Description |
|----------------------|------|--|
| REFRES00 | I/O | Port 0 External Reference Resistor. Provides a reference for the Port 0 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground. |
| REFRES01 | I/O | Port 1 External Reference Resistor. Provides a reference for the Port 1 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground. |
| REFRES02 | I/O | Port 2 External Reference Resistor. Provides a reference for the Port 2 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground. |
| REFRES03 | I/O | Port 3 External Reference Resistor. Provides a reference for the Port 3 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground. |
| REFRES04 | I/O | Port 4 External Reference Resistor. Provides a reference for the Port 4 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground. |
| REFRES05 | I/O | Port 5 External Reference Resistor. Provides a reference for the Port 5 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground. |
| REFRES06 | I/O | Port 6 External Reference Resistor. Provides a reference for the Port 6 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground. |
| REFRES07 | I/O | Port 7 External Reference Resistor. Provides a reference for the Port 7 SerDes bias currents and PLL calibration circuitry. A 3 kOhm +/- 1% resistor should be connected from this pin to ground. |
| REFRESPLL | I/O | PLL External Reference Resistor. Provides a reference for the PLL bias currents and PLL calibration circuitry. A 3K Ohm +/- 1% resistor should be connected from this pin to ground. |
| V _{DD} CORE | I | Core V_{DD}. Power supply for core logic (1.0V). |
| V _{DD} I/O | I | I/O V_{DD}. LVTTTL I/O buffer power supply (2.5V or preferred 3.3V). |

Table 7 Power, Ground, and SerDes Resistor Pins (Part 1 of 2)

| Signal | Type | Name/Description |
|----------------------|------|---|
| V _{DD} PEA | I | PCI Express Analog Power. Serdes analog power supply (1.0V). |
| V _{DD} PEHA | I | PCI Express Analog High Power. Serdes analog power supply (2.5V). |
| V _{DD} PETA | I | PCI Express Transmitter Analog Voltage. Serdes transmitter analog power supply (1.0V). |
| V _{SS} | I | Ground. |

Table 7 Power, Ground, and SerDes Resistor Pins (Part 2 of 2)

Pin Characteristics

Note: Some input pads of the switch do not contain internal pull-ups or pull-downs. Unused SMBus and System inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs which, if left floating, could adversely affect operation. Also, floating pins can cause a slight increase in power consumption. Unused Serdes (Rx and Tx) pins should be left floating. Finally, No Connection pins should not be connected.

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor ¹ | Notes |
|-----------------------|-------------|------|--------------------------------|-------------|--------------------------------|-------|
| PCI Express Interface | PE00RN[3:0] | I | PCIe differential ² | Serial Link | | |
| | PE00RP[3:0] | I | | | | |
| | PE00TN[3:0] | O | | | | |
| | PE00TP[3:0] | O | | | | |
| | PE01RN[3:0] | I | | | | |
| | PE01RP[3:0] | I | | | | |
| | PE01TN[3:0] | O | | | | |
| | PE01TP[3:0] | O | | | | |
| | PE02RN[3:0] | I | | | | |
| | PE02RP[3:0] | I | | | | |
| | PE02TN[3:0] | O | | | | |
| | PE02TP[3:0] | O | | | | |
| | PE03RN[3:0] | I | | | | |
| | PE03RP[3:0] | I | | | | |
| | PE03TN[3:0] | O | | | | |
| | PE03TP[3:0] | O | | | | |
| | PE04RN[3:0] | I | | | | |
| | PE04RP[3:0] | I | | | | |
| | PE04TN[3:0] | O | | | | |
| | PE04TP[3:0] | O | | | | |
| | PE05RN[3:0] | I | | | | |
| | PE05RP[3:0] | I | | | | |
| | PE05TN[3:0] | O | | | | |
| | PE05TP[3:0] | O | | | | |
| | PE06RN[3:0] | I | | | | |
| | PE06RP[3:0] | I | | | | |
| | PE06TN[3:0] | O | | | | |
| | PE06TP[3:0] | O | | | | |
| PE07RN[3:0] | I | | | | | |
| PE07RP[3:0] | I | | | | | |
| PE07TN[3:0] | O | | | | | |
| PE07TP[3:0] | O | | | | | |

Table 8 Pin Characteristics (Part 1 of 2)

| Function | Pin Name | Type | Buffer | I/O Type | Internal Resistor ¹ | Notes |
|-------------------------------|---------------|------|--------|-------------------|--------------------------------|------------------|
| PCI Express Interface (cont.) | GCLKN[1:0] | I | HCSL | Diff. Clock Input | | Refer to Table 9 |
| | GCLKP[1:0] | I | | | | |
| | P[2:0]CLKN | I | | | | |
| | P[2:0]CLKP | I | | | | |
| SMBus | MSMBCLK | I/O | LVTTTL | STI ³ | | pull-up on board |
| | MSMBDAT | I/O | | STI | | pull-up on board |
| | SSMBADDR[2,1] | I | | Input | pull-up | |
| | SSMBCLK | I/O | | STI | | pull-up on board |
| | SSMBDAT | I/O | | STI | | pull-up on board |
| General Purpose I/O | GPIO[8:0] | I/O | LVTTTL | STI, High Drive | pull-up | |
| System Pins | CLKMODE[1:0] | I | LVTTTL | Input | pull-up | |
| | CLKMODE[2] | I | | | pull-down | |
| | GCLKFSEL | I | | | pull-down | |
| | P01MERGEN | I | | | pull-down | |
| | P23MERGEN | I | | | pull-down | |
| | P45MERGEN | I | | | pull-down | |
| | P67MERGEN | I | | | pull-down | |
| | PERSTN | I | | STI | | |
| | RSTHALT | I | | Input | pull-down | |
| | SWMODE[3:0] | I | | | pull-down | |
| EJTAG / JTAG | JTAG_TCK | I | LVTTTL | STI | pull-up | |
| | JTAG_TDI | I | | STI | pull-up | |
| | JTAG_TDO | O | | | | |
| | JTAG_TMS | I | | STI | pull-up | |
| | JTAG_TRST_N | I | | STI | pull-up | |
| SerDes Reference Resistors | REFRES0 | I/O | Analog | | | |
| | REFRES1 | I/O | | | | |
| | REFRES2 | I/O | | | | |
| | REFRES3 | I/O | | | | |
| | REFRES4 | I/O | | | | |
| | REFRES5 | I/O | | | | |
| | REFRES6 | I/O | | | | |
| | REFRES7 | I/O | | | | |
| REFRESPLL | I/O | | | | | |

Table 8 Pin Characteristics (Part 2 of 2)

- ¹. Internal resistor values under typical operating conditions are 92K Ω for pull-up and 91K Ω for pull-down.
- ². All receiver pins set the DC common mode voltage to ground. All transmitters must be AC coupled to the media.
- ³. Schmitt Trigger Input (STI).

Logic Diagram — PES32H8G2



Figure 4 PES32H8G2 Logic Diagram

System Clock Parameters

Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 13 and 14.

| Parameter | Description | Condition | Min | Typical | Max | Unit |
|--------------------------|--|--------------|-------|---------|------------------|------|
| Refclk _{FREQ} | Input reference clock frequency range | | 100 | | 125 ¹ | MHz |
| T _{C-RISE} | Rising edge rate | Differential | 0.6 | | 4 | V/ns |
| T _{C-FALL} | Falling edge rate | Differential | 0.6 | | 4 | V/ns |
| V _{IH} | Differential input high voltage | Differential | +150 | | | mV |
| V _{IL} | Differential input low voltage | Differential | | | -150 | mV |
| V _{CROSS} | Absolute single-ended crossing point voltage | Single-ended | +250 | | +550 | mV |
| V _{CROSS-DELTA} | Variation of V _{CROSS} over all rising clock edges | Single-ended | | | +140 | mV |
| V _{RB} | Ring back voltage margin | Differential | -100 | | +100 | mV |
| T _{STABLE} | Time before V _{RB} is allowed | Differential | 500 | | | ps |
| T _{PERIOD-AVG} | Average clock period accuracy | | -300 | | 2800 | ppm |
| T _{PERIOD-ABS} | Absolute period, including spread-spectrum and jitter | | 9.847 | | 10.203 | ns |
| T _{CC-JITTER} | Cycle to cycle jitter | | | | 150 | ps |
| V _{MAX} | Absolute maximum input voltage | | | | +1.15 | V |
| V _{MIN} | Absolute minimum input voltage | | -0.3 | | | V |
| Duty Cycle | Duty cycle | | 40 | | 60 | % |
| Rise/Fall Matching | Single ended rising Refclk edge rate versus falling Refclk edge rate | | | 20 | | % |
| Z _{C-DC} | Clock source output DC impedance | | 40 | | 60 | Ω |

Table 9 Input Clock Requirements

¹ The input clock frequency will be either 100 or 125 MHz depending on signal GCLKFSEL.

AC Timing Characteristics

| Parameter | Description | Gen 1 | | | Gen 2 | | | Units |
|---|--|------------------|------------------|------------------|------------------|------------------|------------------|-------|
| | | Min ¹ | Typ ¹ | Max ¹ | Min ¹ | Typ ¹ | Max ¹ | |
| PCIe Transmit | | | | | | | | |
| UI | Unit Interval | 399.88 | 400 | 400.12 | 199.94 | 200 | 200.06 | ps |
| T _{TX-EYE} | Minimum Tx Eye Width | 0.75 | | | 0.75 | | | UI |
| T _{TX-EYE-MEDIAN-to-MAX-JITTER} | Maximum time between the jitter median and maximum deviation from the median | | | 0.125 | | | | UI |
| T _{TX-RISE} , T _{TX-FALL} | TX Rise/Fall Time: 20% - 80% | 0.125 | | | 0.15 | | | UI |
| T _{TX-IDLE-MIN} | Minimum time in idle | 20 | | | 20 | | | UI |

Table 10 PCIe AC Timing Characteristics (Part 1 of 2)

| Parameter | Description | Gen 1 | | | Gen 2 | | | Units |
|--|--|------------------|------------------|------------------|------------------|------------------|------------------|-------|
| | | Min ¹ | Typ ¹ | Max ¹ | Min ¹ | Typ ¹ | Max ¹ | |
| T _{TX-IDLE-SET-TO-IDLE} | Maximum time to transition to a valid Idle after sending an Idle ordered set | | | 8 | | | 8 | ns |
| T _{TX-IDLE-TO-DIFF-DATA} | Maximum time to transition from valid idle to diff data | | | 8 | | | 8 | ns |
| T _{TX-SKEW} | Transmitter data skew between any 2 lanes | | | 1.3 | | | 1.3 | ns |
| T _{MIN-PULSED} | Minimum Instantaneous Lone Pulse Width | NA | | | 0.9 | | | UI |
| T _{TX-HF-DJ-DD} | Transmitter Deterministic Jitter > 1.5MHz Bandwidth | NA | | | | | 0.15 | UI |
| T _{RF-MISMATCH} | Rise/Fall Time Differential Mismatch | NA | | | | | 0.1 | UI |
| PCIe Receive | | | | | | | | |
| UI | Unit Interval | 399.88 | 400 | 400.12 | 199.94 | | 200.06 | ps |
| T _{RX-EYE (with jitter)} | Minimum Receiver Eye Width (jitter tolerance) | 0.4 | | | 0.4 | | | UI |
| T _{RX-EYE-MEDIUM TO MAX JITTER} | Max time between jitter median & max deviation | | | 0.3 | | | | UI |
| T _{RX-SKEW} | Lane to lane input skew | | | 20 | | | 8 | ns |
| T _{RX-HF-RMS} | 1.5 — 100 MHz RMS jitter (common clock) | NA | | | | | 3.4 | ps |
| T _{RX-HF-DJ-DD} | Maximum tolerable DJ by the receiver (common clock) | NA | | | | | 88 | ps |
| T _{RX-LF-RMS} | 10 KHz to 1.5 MHz RMS jitter (common clock) | NA | | | | | 4.2 | ps |
| T _{RX-MIN-PULSE} | Minimum receiver instantaneous eye width | NA | | | 0.6 | | | UI |

Table 10 PCIe AC Timing Characteristics (Part 2 of 2)

¹ Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0

| Signal | Symbol | Reference Edge | Min | Max | Unit | Timing Diagram Reference |
|------------------------|------------------------------|----------------|-----|-----|------|--------------------------|
| GPIO | | | | | | |
| GPIO[8:0] ¹ | T _{pw} ² | None | 50 | — | ns | |

Table 11 GPIO AC Timing Characteristics

¹ GPIO signals must meet the setup and hold times if they are synchronous or the minimum pulse width if they are asynchronous.

² The values for this symbol were determined by calculation, not by testing.

| Signal | Symbol | Reference Edge | Min | Max | Unit | Timing Diagram Reference |
|----------------------------------|----------------------|------------------|------|------|------|--------------------------|
| JTAG | | | | | | |
| JTAG_TCK | Tper_16a | none | 50.0 | — | ns | See Figure 5. |
| | Thigh_16a, Tlow_16a | | 10.0 | 25.0 | ns | |
| JTAG_TMS ¹ , JTAG_TDI | Tsu_16b | JTAG_TCK rising | 2.4 | — | ns | |
| | Thld_16b | | 1.0 | — | ns | |
| JTAG_TDO | Tdo_16c | JTAG_TCK falling | — | 20 | ns | |
| | Tdz_16c ² | | — | 20 | ns | |
| JTAG_TRST_N | Tpw_16d ² | none | 25.0 | — | ns | |

Table 12 JTAG AC Timing Characteristics

¹ The JTAG specification, IEEE 1149.1, recommends that JTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when JTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

² The values for this symbol were determined by calculation, not by testing.



Figure 5 JTAG AC Timing Waveform

Recommended Operating Supply Voltages

| Symbol | Parameter | Minimum | Typical | Maximum | Unit |
|----------------|--|---------|---------|---------|------|
| V_{DDCORE} | Internal logic supply | 0.9 | 1.0 | 1.1 | V |
| $V_{DDI/O}$ | I/O supply except for SerDes | 2.25 | 2.5 | 2.75 | V |
| | | 3.125 | 3.3 | 3.465 | V |
| V_{DDPEA}^1 | PCI Express Analog Power | 0.95 | 1.0 | 1.1 | V |
| V_{DDPEHA}^2 | PCI Express Analog High Power | 2.25 | 2.5 | 2.75 | V |
| V_{DDPETA}^1 | PCI Express Transmitter Analog Voltage | 0.95 | 1.0 | 1.1 | V |
| V_{SS} | Common ground | 0 | 0 | 0 | V |

Table 13 PES32H8G2 Operating Voltages

¹ V_{DDPEA} and V_{DDPETA} should have no more than 25mV_{peak-peak} AC power supply noise superimposed on the 1.0V nominal DC value.

² V_{DDPEHA} should have no more than 50mV_{peak-peak} AC power supply noise superimposed on the 2.5V nominal DC value.

Power-Up/Power-Down Sequence

During power supply ramp-up, V_{DDCORE} must remain at least 1.0V below $V_{DDI/O}$ at all times. There are no other power-up sequence requirements for the various operating supply voltages.

The power-down sequence can occur in any order.

Recommended Operating Temperature

| Grade | Temperature |
|------------|------------------------|
| Commercial | 0°C to +70°C Ambient |
| Industrial | -40°C to +85°C Ambient |

Table 14 PES32H8G2 Operating Temperatures

Power Consumption

Typical power is measured under the following conditions: 25°C Ambient, 35% total link usage on all ports, typical voltages defined in Table 13 (and also listed below).

Maximum power is measured under the following conditions: 70°C Ambient, 85% total link usage on all ports, maximum voltages defined in Table 13 (and also listed below).

| Number of Active Lanes per Port | | Core Supply | | PCIe Analog Supply | | PCIe Analog High Supply | | PCIe Transmitter Supply | | I/O Supply | | Total | |
|---------------------------------|-------|-------------|----------|--------------------|----------|-------------------------|-----------|-------------------------|----------|------------|-----------|-----------|-----------|
| | | Typ 1.0V | Max 1.1V | Typ 1.0V | Max 1.1V | Typ 2.5V | Max 2.75V | Typ 1.0V | Max 1.1V | Typ 2.5V | Max 2.75V | Typ Power | Max Power |
| 8/8/8/8 (Full Swing) | mA | 2920 | 5336 | 1514 | 1826 | 507 | 514 | 561 | 603 | 24 | 29 | | |
| | Watts | 2.92 | 5.87 | 1.51 | 2.01 | 1.27 | 1.41 | 0.56 | 0.66 | 0.06 | 0.08 | 6.32 | 10.04 |
| 8/8/8/8 (Half Swing) | mA | 2920 | 5336 | 1302 | 1571 | 507 | 514 | 292 | 313 | 24 | 29 | | |
| | Watts | 2.92 | 5.87 | 1.30 | 1.73 | 1.27 | 1.41 | 0.29 | 0.34 | 0.06 | 0.08 | 5.84 | 9.44 |

Table 15 PES32H8G2 Power Consumption — 2.5V I/O

| Number of Active Lanes per Port | | Core Supply | | PCIe Analog Supply | | PCIe Analog High Supply | | PCIe Transmitter Supply | | I/O Supply | | Total | |
|---------------------------------|-------|-------------|----------|--------------------|----------|-------------------------|-----------|-------------------------|----------|------------|-----------|-----------|-----------|
| | | Typ 1.0V | Max 1.1V | Typ 1.0V | Max 1.1V | Typ 2.5V | Max 2.75V | Typ 1.0V | Max 1.1V | Typ 3.3V | Max 3.465 | Typ Power | Max Power |
| 8/8/8/8 (Full Swing) | mA | 2920 | 5336 | 1514 | 1826 | 507 | 514 | 561 | 603 | 30 | 35 | | |
| | Watts | 2.92 | 5.87 | 1.51 | 2.01 | 1.27 | 1.41 | 0.56 | 0.66 | 0.10 | 0.12 | 6.36 | 10.08 |
| 8/8/8/8 (Half Swing) | mA | 2920 | 5336 | 1302 | 1571 | 507 | 514 | 292 | 313 | 30 | 35 | | |
| | Watts | 2.92 | 5.87 | 1.30 | 1.73 | 1.27 | 1.41 | 0.29 | 0.34 | 0.10 | 0.12 | 5.88 | 9.48 |

Table 16 PES32H8G2 Power Consumption — 3.3V I/O

Note 1: I/O supply of 3.3V is preferred.

Note 2: The above power consumption assumes that all ports are functioning at Gen2 (5.0 GT/S) speeds. Power consumption can be reduced by turning off unused ports through software or through boot EEPROM. Power savings will occur in V_{DDPEA} , V_{DDPEHA} , and V_{DDPETA} . Power savings can be estimated as directly proportional to the number of unused ports, since the power consumption of a turned-off port is close to zero. For example, if 2 ports out of 8 are turned off, then the power savings for each of the above three power rails can be calculated quite simply as 2/8 multiplied by the power consumption indicated in the above table.

Note 3: Using a port in Gen1 mode (2.5GT/S) results in approximately 18% power savings for each power rail: V_{DDPEA} , V_{DDPEHA} , and V_{DDPETA} .

Thermal Considerations

This section describes thermal considerations for the PES32H8G2 (23mm² FCBGA484 package). The data in Table 17 below contains information that is relevant to the thermal performance of the PES32H8G2 switch.

| Symbol | Parameter | Value | Units | Conditions |
|--------------------------|---|-------|-------|---------------------------------------|
| $T_{J(max)}$ | Junction Temperature | 125 | °C | Maximum |
| $T_{A(max)}$ | Ambient Temperature | 70 | °C | Maximum for commercial-rated products |
| | | 85 | °C | Maximum for industrial-rated products |
| $\theta_{JA(effective)}$ | Effective Thermal Resistance, Junction-to-Ambient | 15.2 | °C/W | Zero air flow |
| | | 8.5 | °C/W | 1 m/S air flow |
| | | 7.1 | °C/W | 2 m/S air flow |
| θ_{JB} | Thermal Resistance, Junction-to-Board | 3.1 | °C/W | |
| θ_{JC} | Thermal Resistance, Junction-to-Case | 0.15 | °C/W | |
| P | Power Dissipation of the Device | 10.08 | Watts | Maximum |

Table 17 Thermal Specifications for PES32H8G2, 23x23 mm FCBGA484 Package

Note: It is important for the reliability of this device in any user environment that the junction temperature not exceed the $T_{J(max)}$ value specified in Table 17. Consequently, the effective junction to ambient thermal resistance (θ_{JA}) for the worst case scenario must be maintained below the value determined by the formula:

$$\theta_{JA} = (T_{J(max)} - T_{A(max)})/P$$

Given that the values of $T_{J(max)}$, $T_{A(max)}$, and P are known, the value of desired θ_{JA} becomes a known entity to the system designer. How to achieve the desired θ_{JA} is left up to the board or system designer, but in general, it can be achieved by adding the effects of θ_{JC} (value provided in Table 17), thermal resistance of the chosen adhesive (θ_{CS}), that of the heat sink (θ_{SA}), amount of airflow, and properties of the circuit board (number of layers and size of the board). It is strongly recommended that users perform their own thermal analysis for their own board and system design scenarios.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 13.

Note: See Table 8, Pin Characteristics, for a complete I/O listing.

| I/O Type | Parameter | Description | Gen1 | | | Gen2 | | | Unit | Condi- tions |
|---------------------|--|---|------------------|------------------|------------------|------------------|------------------|------------------|----------|-----------------|
| | | | Min ¹ | Typ ¹ | Max ¹ | Min ¹ | Typ ¹ | Max ¹ | | |
| Serial Link | PCIe Transmit | | | | | | | | | |
| | $V_{TX-DIFFp-p}$ | Differential peak-to-peak output voltage | 800 | | 1200 | 800 | | 1200 | mV | |
| | $V_{TX-DIFFp-p-LOW}$ | Low-Drive Differential Peak to Peak Output Voltage | 400 | | 1200 | 400 | | 1200 | mV | |
| | $V_{TX-DE-RATIO-3.5dB}$ | De-emphasized differential output voltage | -3 | | -4 | -3.0 | -3.5 | -4.0 | dB | |
| | $V_{TX-DE-RATIO-6.0dB}$ | De-emphasized differential output voltage | NA | | | -5.5 | -6.0 | -6.5 | dB | |
| | $V_{TX-DC-CM}$ | DC Common mode voltage | 0 | | 3.6 | 0 | | 3.6 | V | |
| | $V_{TX-CM-ACP}$ | RMS AC peak common mode output voltage | | | 20 | | | | mV | |
| | $V_{TX-CM-DC-active-idle-delta}$ | Abs delta of DC common mode voltage between LO and idle | | | 100 | | | 100 | mV | |
| | $V_{TX-CM-DC-line-delta}$ | Abs delta of DC common mode voltage between D+ and D- | | | 25 | | | 25 | mV | |
| | $V_{TX-Idle-DiffP}$ | Electrical idle diff peak output | | | 20 | | | 20 | mV | |
| | $RL_{TX-DIFF}$ | Transmitter Differential Return loss | 10 | | | | | 10 | dB | 0.05 - 1.25GHz |
| | | | | | | | | | 8 | dB |
| | RL_{TX-CM} | Transmitter Common Mode Return loss | 6 | | | | | 6 | dB | |
| | $Z_{TX-DIFF-DC}$ | DC Differential TX impedance | 80 | 100 | 120 | | | 120 | Ω | |
| | $V_{TX-CM-ACpp}$ | Peak-Peak AC Common | NA | | | | | 100 | mV | |
| | $V_{TX-DC-CM}$ | Transmit Driver DC Common Mode Voltage | 0 | | 3.6 | 0 | | 3.6 | V | |
| $V_{TX-RCV-DETECT}$ | The amount of voltage change allowed during Receiver Detection | | | 600 | | | 600 | mV | | |
| $I_{TX-SHORT}$ | Transmitter Short Circuit Current Limit | 0 | | 90 | | | | 90 | mA | |

Table 18 DC Electrical Characteristics (Part 1 of 2)

| I/O Type | Parameter | Description | Gen1 | | | Gen2 | | | Unit | Conditions |
|-----------------------------|--------------------------------------|--|------------------|------------------|------------------|---------------------------|------------------|------------------|-----------------|------------------|
| | | | Min ¹ | Typ ¹ | Max ¹ | Min ¹ | Typ ¹ | Max ¹ | | |
| Serial Link (cont.) | PCIe Receive | | | | | | | | | |
| | $V_{RX-DIFFp-p}$ | Differential input voltage (peak-to-peak) | 175 | | 1200 | 120 | | 1200 | mV | |
| | $RL_{RX-DIFF}$ | Receiver Differential Return Loss | 10 | | | | | 10 | dB | 0.05 - 1.25GHz |
| | | | | | | | | 8 | | 1.25 - 2.5GHz |
| | RL_{RX-CM} | Receiver Common Mode Return Loss | 6 | | | | | 6 | dB | |
| | $Z_{RX-DIFF-DC}$ | Differential input impedance (DC) | 80 | 100 | 120 | Refer to return loss spec | | | Ω | |
| | Z_{RX--DC} | DC common mode impedance | 40 | 50 | 60 | 40 | | 60 | Ω | |
| | $Z_{RX-COMM-DC}$ | Powered down input common mode impedance (DC) | 200k | 350k | | | | 50k | Ω | |
| | $Z_{RX-HIGH-IMP-DC-POS}$ | DC input CM input impedance for $V > 0$ during reset or power down | | | 50k | | | 50k | Ω | |
| | $Z_{RX-HIGH-IMP-DC-NEG}$ | DC input CM input impedance for $V < 0$ during reset or power down | | | 1.0k | | | 1.0k | Ω | |
| $V_{RX-IDLE-DET-DIFFp-p}$ | Electrical idle detect threshold | 65 | | 175 | 65 | | 175 | mV | | |
| $V_{RX-CM-ACp}$ | Receiver AC common-mode peak voltage | | | 150 | | | 150 | mV | $V_{RX-CM-ACp}$ | |
| PCIe REFCLK | | | | | | | | | | |
| | C_{IN} | Input Capacitance | 1.5 | — | | 1.5 | — | | pF | |
| Other I/Os | | | | | | | | | | |
| LOW Drive Output | I_{OL} | | — | 2.5 | — | — | 2.5 | — | mA | $V_{OL} = 0.4v$ |
| | I_{OH} | | — | -5.5 | — | — | -5.5 | — | mA | $V_{OH} = 1.5V$ |
| High Drive Output | I_{OL} | | — | 12.0 | — | — | 12.0 | — | mA | $V_{OL} = 0.4v$ |
| | I_{OH} | | — | -20.0 | — | — | -20.0 | — | mA | $V_{OH} = 1.5V$ |
| Schmitt Trigger Input (STI) | V_{IL} | | -0.3 | — | 0.8 | -0.3 | — | 0.8 | V | — |
| | V_{IH} | | 2.0 | — | $V_{DD}/O + 0.5$ | 2.0 | — | $V_{DD}/O + 0.5$ | V | — |
| Input | V_{IL} | | -0.3 | — | 0.8 | -0.3 | — | 0.8 | V | — |
| | V_{IH} | | 2.0 | — | $V_{DD}/O + 0.5$ | 2.0 | — | $V_{DD}/O + 0.5$ | V | — |
| Capacitance | C_{IN} | | — | — | 8.5 | — | — | 8.5 | pF | — |
| Leakage | Inputs | | — | — | ± 10 | — | — | ± 10 | μA | V_{DD}/O (max) |
| | I/O_{LEAK} W/O Pull-ups/downs | | — | — | ± 10 | — | — | ± 10 | μA | V_{DD}/O (max) |
| | I/O_{LEAK} WITH Pull-ups/downs | | — | — | ± 80 | — | — | ± 80 | μA | V_{DD}/O (max) |

Table 18 DC Electrical Characteristics (Part 2 of 2)

¹ Minimum, Typical, and Maximum values meet the requirements under PCI Specification 2.0.

Absolute Maximum Voltage Rating

| Core Supply | PCIe Analog Supply | PCIe Analog High Supply | PCIe Transmitter Supply | I/O Supply |
|-------------|--------------------|-------------------------|-------------------------|------------|
| 1.5V | 1.5V | 4.6V | 1.5V | 4.6V |

Table 19 PES32H8G2 Absolute Maximum Voltage Rating

Warning: For proper and reliable operation in adherence with this data sheet, the device should not exceed the recommended operating voltages in Table 13. The absolute maximum operating voltages in Table 19 are offered to provide guidelines for voltage excursions outside the recommended voltage ranges. Device functionality is not guaranteed at these conditions and sustained operation at these values or any exposure to voltages outside the maximum range may adversely affect device functionality and reliability.

SMBus Characterization

| Symbol | Parameter | SMBus 2.0 Char. Data ¹ | | | Unit |
|---------------------------------|--------------------|-----------------------------------|------|------|------|
| | | 3V | 3.3V | 3.6V | |
| DC Parameter for SDA Pin | | | | | |
| V _{IL} | Input Low | 1.16 | 1.26 | 1.35 | V |
| V _{IH} | Input High | 1.56 | 1.67 | 1.78 | V |
| V _{OL@350uA} | Output Low | 15 | 15 | 15 | mV |
| I _{OL@0.4V} | | 23 | 24 | 25 | mA |
| I _{Pullup} | Current Source | — | — | — | μA |
| I _{IL_Leak} | Input Low Leakage | 0 | 0 | 0 | μA |
| I _{IH_Leak} | Input High Leakage | 0 | 0 | 0 | μA |
| DC Parameter for SCL Pin | | | | | |
| V _{IL (V)} | Input Low | 1.11 | 1.2 | 1.31 | V |
| V _{IH (V)} | Input High | 1.54 | 1.65 | 1.76 | V |
| I _{IL_Leak} | Input Low Leakage | 0 | 0 | 0 | μA |
| I _{IH_Leak} | Input High Leakage | 0 | 0 | 0 | μA |

Table 20 SMBus DC Characterization Data

¹. Data at room and hot temperature.

| Symbol | Parameter | SMBus @3.3V \pm 10% ¹ | | Unit |
|------------------------|--|------------------------------------|------|---------|
| | | Min | Max | |
| F _{SCL} | Clock frequency | 5 | 600 | KHz |
| T _{BUF} | Bus free time between Stop and Start | 3.5 | — | μ s |
| T _{HD:STA} | Start condition hold time | 1 | — | μ s |
| T _{SU:STA} | Start condition setup time | 1 | — | μ s |
| T _{SU:STO} | Stop condition setup time | 1 | — | μ s |
| T _{HD:DAT} | Data hold time | 1 | — | ns |
| T _{SU:DAT} | Data setup time | 1 | — | ns |
| T _{TIMEOUT} | Detect clock low time out | — | 74.7 | ms |
| T _{LOW} | Clock low period | 3.7 | — | μ s |
| T _{HIGH} | Clock high period | 3.7 | — | μ s |
| T _F | Clock/Data fall time | — | 72.2 | ns |
| T _R | Clock/Data rise time | — | 68.3 | ns |
| T _{POR@10kHz} | Time which a device must be operational after power-on reset | 20 | — | ms |

Table 21 SMBus AC Timing Data

¹. Data at room and hot temperature.

Package Pinout — 484-BGA Signal Pinout

The following table lists the pin numbers and signal names for the PES32H8G2 device.

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|---------------------|-----|-----|---------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| A1 | V _{SS} | | B13 | V _{SS} | | D3 | V _{SS} | | E15 | V _{DD} PEA | |
| A2 | V _{DD} I/O | | B14 | P02CLKN | | D4 | V _{SS} | | E16 | V _{SS} | |
| A3 | PE03TP3 | | B15 | V _{SS} | | D5 | PE03RP3 | | E17 | PE02RP1 | |
| A4 | PE03TP2 | | B16 | PE02TN1 | | D6 | PE03RN2 | | E18 | V _{DD} PEHA | |
| A5 | V _{SS} | | B17 | PE02TN0 | | D7 | V _{SS} | | E19 | V _{SS} | |
| A6 | PE03TP1 | | B18 | V _{DD} I/O | | D8 | PE03RP1 | | E20 | V _{SS} | |
| A7 | PE03TP0 | | B19 | MSMBCLK | | D9 | V _{SS} | | E21 | PE00TN0 | |
| A8 | V _{SS} | | B20 | JTAG_TMS | | D10 | PE03RP0 | | E22 | PE00TP0 | |
| A9 | GCLKP0 | | B21 | SSMBCLK | | D11 | REFRESPLL | | F1 | V _{SS} | |
| A10 | V _{SS} | | B22 | JTAG_TCK | | D12 | V _{SS} | | F2 | V _{SS} | |
| A11 | PE02TP3 | | C1 | V _{SS} | | D13 | PE02RP3 | | F3 | PE05RN3 | |
| A12 | PE02TP2 | | C2 | V _{DD} I/O | | D14 | V _{SS} | | F4 | PE05RP3 | |
| A13 | V _{SS} | | C3 | V _{SS} | | D15 | PE02RP2 | | F5 | V _{DD} PEHA | |
| A14 | P02CLKP | | C4 | V _{SS} | | D16 | V _{SS} | | F6 | V _{DD} PEHA | |
| A15 | V _{SS} | | C5 | PE03RN3 | | D17 | PE02RN1 | | F7 | V _{DD} PEHA | |
| A16 | PE02TP1 | | C6 | V _{SS} | | D18 | PE02RP0 | | F8 | V _{DD} PEA | |
| A17 | PE02TP0 | | C7 | V _{SS} | | D19 | V _{SS} | | F9 | V _{DD} PETA | |
| A18 | V _{DD} I/O | | C8 | PE03RN1 | | D20 | JTAG_TDI | | F10 | V _{DD} PEA | |
| A19 | MSMBDAT | | C9 | V _{SS} | | D21 | V _{DD} I/O | | F11 | V _{DD} PEA | |
| A20 | JTAG_TDO | | C10 | PE03RN0 | | D22 | V _{DD} I/O | | F12 | V _{DD} PETA | |
| A21 | CLKMODE1 | | C11 | V _{SS} | | E1 | V _{SS} | | F13 | V _{DD} PETA | |
| A22 | SSMBADDR2 | | C12 | V _{SS} | | E2 | V _{SS} | | F14 | V _{DD} PEA | |
| B1 | V _{SS} | | C13 | PE02RN3 | | E3 | V _{SS} | | F15 | V _{DD} PEA | |
| B2 | V _{DD} I/O | | C14 | V _{SS} | | E4 | V _{SS} | | F16 | V _{DD} PEA | |
| B3 | PE03TN3 | | C15 | PE02RN2 | | E5 | V _{DD} PEHA | | F17 | V _{DD} PEHA | |
| B4 | PE03TN2 | | C16 | REFRES02 | | E6 | PE03RP2 | | F18 | V _{DD} PEHA | |
| B5 | V _{SS} | | C17 | V _{SS} | | E7 | V _{DD} PEA | | F19 | V _{DD} PEHA | |
| B6 | PE03TN1 | | C18 | PE02RN0 | | E8 | V _{DD} PEA | | F20 | V _{SS} | |
| B7 | PE03TN0 | | C19 | PERSTN | | E9 | V _{DD} PETA | | F21 | PE00TN1 | |
| B8 | V _{SS} | | C20 | JTAG_TRST_N | | E10 | V _{DD} PEA | | F22 | PE00TP1 | |
| B9 | GCLKN0 | | C21 | SSMBDAT | | E11 | REFRES03 | | G1 | PE05TP3 | |
| B10 | V _{SS} | | C22 | SSMBADDR1 | | E12 | V _{DD} PETA | | G2 | PE05TN3 | |
| B11 | PE02TN3 | | D1 | V _{SS} | | E13 | NC | | G3 | V _{SS} | |
| B12 | PE02TN2 | | D2 | V _{SS} | | E14 | V _{SS} | | G4 | PE05RN2 | |

Table 22 PES32H8G2 Signal Pin-Out (Part 1 of 4)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| G5 | PE05RP2 | | H20 | V _{SS} | | K13 | V _{SS} | | M6 | V _{DD} PEA | |
| G6 | V _{DD} PEA | | H21 | P01CLKN | | K14 | V _{DD} CORE | | M7 | V _{SS} | |
| G7 | V _{SS} | | H22 | P01CLKP | | K15 | V _{DD} CORE | | M8 | V _{DD} CORE | |
| G8 | V _{DD} CORE | | J1 | V _{SS} | | K16 | V _{SS} | | M9 | V _{DD} CORE | |
| G9 | V _{DD} CORE | | J2 | V _{SS} | | K17 | V _{DD} PETA | | M10 | V _{SS} | |
| G10 | V _{SS} | | J3 | PE05RN1 | | K18 | REFRES01 | | M11 | V _{DD} CORE | |
| G11 | V _{DD} CORE | | J4 | PE05RP1 | | K19 | PE00RP2 | | M12 | V _{DD} CORE | |
| G12 | V _{DD} CORE | | J5 | V _{DD} PETA | | K20 | PE00RN2 | | M13 | V _{SS} | |
| G13 | V _{SS} | | J6 | V _{DD} PETA | | K21 | V _{SS} | | M14 | V _{DD} CORE | |
| G14 | V _{DD} CORE | | J7 | V _{SS} | | K22 | V _{SS} | | M15 | V _{DD} CORE | |
| G15 | V _{DD} CORE | | J8 | V _{DD} CORE | | L1 | PE05TP0 | | M16 | V _{SS} | |
| G16 | V _{SS} | | J9 | V _{DD} CORE | | L2 | PE05TN0 | | M17 | V _{DD} PEA | |
| G17 | V _{DD} PEA | | J10 | V _{SS} | | L3 | V _{SS} | | M18 | V _{DD} PEA | |
| G18 | V _{DD} PEA | | J11 | V _{DD} CORE | | L4 | V _{SS} | | M19 | V _{SS} | |
| G19 | PE00RP0 | | J12 | V _{DD} CORE | | L5 | V _{DD} PEA | | M20 | V _{SS} | |
| G20 | PE00RN0 | | J13 | V _{SS} | | L6 | V _{DD} PEA | | M21 | PE00TN3 | |
| G21 | V _{SS} | | J14 | V _{DD} CORE | | L7 | V _{SS} | | M22 | PE00TP3 | |
| G22 | V _{SS} | | J15 | V _{DD} CORE | | L8 | V _{DD} CORE | | N1 | PE04TP3 | |
| H1 | PE05TP2 | | J16 | V _{SS} | | L9 | V _{DD} CORE | | N2 | PE04TN3 | |
| H2 | PE05TN2 | | J17 | V _{DD} PETA | | L10 | V _{SS} | | N3 | REFRES04 | |
| H3 | REFRES05 | | J18 | V _{DD} PETA | | L11 | V _{DD} CORE | | N4 | PE04RN2 | |
| H4 | V _{SS} | | J19 | REFRES00 | | L12 | V _{DD} CORE | | N5 | PE04RP2 | |
| H5 | V _{DD} PEA | | J20 | NC | | L13 | V _{SS} | | N6 | V _{DD} PEA | |
| H6 | V _{DD} PEA | | J21 | P00CLKN | | L14 | V _{DD} CORE | | N7 | V _{SS} | |
| H7 | V _{SS} | | J22 | P00CLKP | | L15 | V _{DD} CORE | | N8 | V _{DD} CORE | |
| H8 | V _{DD} CORE | | K1 | PE05TP1 | | L16 | V _{SS} | | N9 | V _{DD} CORE | |
| H9 | V _{DD} CORE | | K2 | PE05TN1 | | L17 | V _{DD} PEA | | N10 | V _{SS} | |
| H10 | V _{SS} | | K3 | V _{SS} | | L18 | PE00RP3 | | N11 | V _{DD} CORE | |
| H11 | V _{DD} CORE | | K4 | PE05RN0 | | L19 | PE00RN3 | | N12 | V _{DD} CORE | |
| H12 | V _{DD} CORE | | K5 | PE05RP0 | | L20 | V _{SS} | | N13 | V _{SS} | |
| H13 | V _{SS} | | K6 | V _{DD} PETA | | L21 | PE00TN2 | | N14 | V _{DD} CORE | |
| H14 | V _{DD} CORE | | K7 | V _{SS} | | L22 | PE00TP2 | | N15 | V _{DD} CORE | |
| H15 | V _{DD} CORE | | K8 | V _{DD} CORE | | M1 | V _{SS} | | N16 | V _{SS} | |
| H16 | V _{SS} | | K9 | V _{DD} CORE | | M2 | V _{SS} | | N17 | V _{DD} PEA | |
| H17 | V _{DD} PEA | | K10 | V _{SS} | | M3 | PE04RN3 | | N18 | V _{DD} PEA | |
| H18 | PE00RP1 | | K11 | V _{DD} CORE | | M4 | PE04RP3 | | N19 | PE01RP0 | |
| H19 | PE00RN1 | | K12 | V _{DD} CORE | | M5 | V _{DD} PEA | | N20 | PE01RN0 | |

Table 22 PES32H8G2 Signal Pin-Out (Part 2 of 4)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|-----|----------------------|-----|
| N21 | V _{SS} | | R14 | V _{DD} CORE | | U7 | V _{DD} PEA | | V22 | PE01TP3 | |
| N22 | V _{SS} | | R15 | V _{DD} CORE | | U8 | V _{DD} PEA | | W1 | V _{SS} | |
| P1 | PE04TP2 | | R16 | V _{SS} | | U9 | V _{DD} PEA | | W2 | P23MERGEN | |
| P2 | PE04TN2 | | R17 | V _{DD} PETA | | U10 | V _{DD} PETA | | W3 | P45MERGEN | |
| P3 | V _{SS} | | R18 | V _{DD} PETA | | U11 | V _{DD} PETA | | W4 | V _{DD} I/O | |
| P4 | V _{SS} | | R19 | V _{SS} | | U12 | V _{DD} PEA | | W5 | PE06RP0 | |
| P5 | V _{DD} PETA | | R20 | V _{SS} | | U13 | V _{DD} PEA | | W6 | PE06RN1 | |
| P6 | V _{DD} PETA | | R21 | PE01TN1 | | U14 | V _{DD} PEA | | W7 | REFRES06 | |
| P7 | V _{SS} | | R22 | PE01TP1 | | U15 | V _{DD} PETA | | W8 | PE06RP2 | |
| P8 | V _{DD} CORE | | T1 | PE04TP1 | | U16 | V _{DD} PEA | | W9 | V _{SS} | |
| P9 | V _{DD} CORE | | T2 | PE04TN1 | | U17 | V _{DD} PEHA | | W10 | V _{SS} | |
| P10 | V _{SS} | | T3 | V _{SS} | | U18 | PE01RP3 | | W11 | PE06RP3 | |
| P11 | V _{DD} CORE | | T4 | V _{SS} | | U19 | PE01RN3 | | W12 | V _{SS} | |
| P12 | V _{DD} CORE | | T5 | V _{DD} PEHA | | U20 | V _{SS} | | W13 | PE07RP0 | |
| P13 | V _{SS} | | T6 | V _{DD} PEHA | | U21 | PE01TN2 | | W14 | PE07RN1 | |
| P14 | V _{DD} CORE | | T7 | V _{SS} | | U22 | PE01TP2 | | W15 | V _{SS} | |
| P15 | V _{DD} CORE | | T8 | V _{DD} CORE | | V1 | V _{DD} I/O | | W16 | PE07RP2 | |
| P16 | V _{SS} | | T9 | V _{DD} CORE | | V2 | V _{DD} I/O | | W17 | V _{SS} | |
| P17 | V _{DD} PEA | | T10 | V _{SS} | | V3 | PE04RN0 | | W18 | V _{DD} PEHA | |
| P18 | PE01RP1 | | T11 | V _{DD} CORE | | V4 | PE04RP0 | | W19 | PE07RP3 | |
| P19 | PE01RN1 | | T12 | V _{DD} CORE | | V5 | V _{SS} | | W20 | V _{DD} I/O | |
| P20 | V _{SS} | | T13 | V _{SS} | | V6 | PE06RP1 | | W21 | V _{DD} I/O | |
| P21 | PE01TN0 | | T14 | V _{DD} CORE | | V7 | V _{SS} | | W22 | V _{DD} I/O | |
| P22 | PE01TP0 | | T15 | V _{DD} CORE | | V8 | V _{DD} PEA | | Y1 | P01MERGEN | |
| R1 | V _{SS} | | T16 | V _{SS} | | V9 | V _{DD} PEA | | Y2 | P67MERGEN | |
| R2 | V _{SS} | | T17 | V _{DD} PETA | | V10 | V _{SS} | | Y3 | CLKMODE2 | |
| R3 | PE04RN1 | | T18 | V _{DD} PETA | | V11 | V _{DD} PETA | | Y4 | V _{DD} I/O | |
| R4 | PE04RP1 | | T19 | PE01RP2 | | V12 | V _{SS} | | Y5 | PE06RN0 | |
| R5 | V _{DD} PETA | | T20 | PE01RN2 | | V13 | V _{DD} PEA | | Y6 | V _{SS} | |
| R6 | V _{DD} PETA | | T21 | V _{SS} | | V14 | PE07RP1 | | Y7 | V _{SS} | |
| R7 | V _{SS} | | T22 | V _{SS} | | V15 | V _{DD} PETA | | Y8 | PE06RN2 | |
| R8 | V _{DD} CORE | | U1 | PE04TP0 | | V16 | V _{DD} PEA | | Y9 | V _{SS} | |
| R9 | V _{DD} CORE | | U2 | PE04TN0 | | V17 | V _{DD} PEHA | | Y10 | V _{SS} | |
| R10 | V _{SS} | | U3 | V _{SS} | | V18 | V _{DD} PEHA | | Y11 | PE06RN3 | |
| R11 | V _{DD} CORE | | U4 | V _{SS} | | V19 | V _{SS} | | Y12 | V _{SS} | |
| R12 | V _{DD} CORE | | U5 | V _{DD} PEHA | | V20 | V _{SS} | | Y13 | PE07RN0 | |
| R13 | V _{SS} | | U6 | V _{DD} PEHA | | V21 | PE01TN3 | | Y14 | V _{SS} | |

Table 22 PES32H8G2 Signal Pin-Out (Part 3 of 4)

| Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt | Pin | Function | Alt |
|-----|---------------------|-----|------|-----------------|-----|------|---------------------|-----|------|-----------------|-----|
| Y15 | REFRES07 | | AA6 | PE06TN0 | | AA19 | V _{SS} | | AB10 | PE06TP3 | |
| Y16 | PE07RN2 | | AA7 | PE06TN1 | | AA20 | GPIO_03 | 1 | AB11 | V _{SS} | |
| Y17 | V _{SS} | | AA8 | V _{SS} | | AA21 | GPIO_04 | 1 | AB12 | GCLKP1 | |
| Y18 | V _{SS} | | AA9 | PE06TN2 | | AA22 | GPIO_05 | 2 | AB13 | V _{SS} | |
| Y19 | PE07RN3 | | AA10 | PE06TN3 | | AB1 | SWMODE1 | | AB14 | PE07TP0 | |
| Y20 | GPIO_06 | | AA11 | V _{SS} | | AB2 | RSTHALT | | AB15 | PE07TP1 | |
| Y21 | GPIO_07 | | AA12 | GCLKN1 | | AB3 | SWMODE2 | | AB16 | V _{SS} | |
| Y22 | GPIO_08 | 1 | AA13 | V _{SS} | | AB4 | SWMODE3 | | AB17 | PE07TP2 | |
| AA1 | CLKMODE0 | | AA14 | PE07TN0 | | AB5 | V _{DD} I/O | | AB18 | PE07TP3 | |
| AA2 | GCLKFSEL | | AA15 | PE07TN1 | | AB6 | PE06TP0 | | AB19 | V _{SS} | |
| AA3 | SWMODE0 | | AA16 | V _{SS} | | AB7 | PE06TP1 | | AB20 | GPIO_00 | 1 |
| AA4 | V _{SS} | | AA17 | PE07TN2 | | AB8 | V _{SS} | | AB21 | GPIO_01 | 1 |
| AA5 | V _{DD} I/O | | AA18 | PE07TN3 | | AB9 | PE06TP2 | | AB22 | GPIO_02 | 1 |

Table 22 PES32H8G2 Signal Pin-Out (Part 4 of 4)

Alternate Signal Functions

| Pin | GPIO | 1st Alternate | 2nd Alternate |
|------|---------|---------------|---------------|
| AB20 | GPIO_00 | PART0PERSTN | — |
| AB21 | GPIO_01 | PART1PERSTN | — |
| AB22 | GPIO_02 | PART2PERSTN | — |
| AA20 | GPIO_03 | PART3PERSTN | |
| AA21 | GPIO_04 | — | POLINKUPN |
| AA22 | GPIO_05 | GPEN | POACTIVEN |
| Y22 | GPIO_08 | IOEXPINTN | — |

Table 23 PES32H8G2 Alternate Signal Functions

No Connection Pins

| | |
|-----|-----|
| NC | |
| E13 | J20 |

Table 24 PES32H8G2 No Connection

Power Pins

| V _{DD} Core | V _{DD} Core | V _{DD} Core | V _{DD} I/O | V _{DD} PEA | V _{DD} PEA | V _{DD} PEHA | V _{DD} PETA |
|----------------------|----------------------|----------------------|---------------------|---------------------|---------------------|----------------------|----------------------|
| G8 | K11 | N14 | A2 | E7 | M5 | E5 | E9 |
| G9 | K12 | N15 | A18 | E8 | M6 | E18 | E12 |
| G11 | K14 | P8 | B2 | E10 | M17 | F5 | F9 |
| G12 | K15 | P9 | B18 | E15 | M18 | F6 | F12 |
| G14 | L8 | P11 | C2 | F8 | N6 | F7 | F13 |
| G15 | L9 | P12 | D21 | F10 | N17 | F17 | J5 |
| H8 | L11 | P14 | D22 | F11 | N18 | F18 | J6 |
| H9 | L12 | P15 | V1 | F14 | P17 | F19 | J17 |
| H11 | L14 | R8 | V2 | F15 | U7 | T5 | J18 |
| H12 | L15 | R9 | W4 | F16 | U8 | T6 | K6 |
| H14 | M8 | R11 | W20 | G6 | U9 | U5 | K17 |
| H15 | M9 | R12 | W21 | G17 | U12 | U6 | P5 |
| J8 | M11 | R14 | W22 | G18 | U13 | U17 | P6 |
| J9 | M12 | R15 | Y4 | H5 | U14 | V17 | R5 |
| J11 | M14 | T8 | AA5 | H6 | U16 | V18 | R6 |
| J12 | M15 | T9 | AB5 | H17 | V8 | W18 | R17 |
| J14 | N8 | T11 | | L5 | V9 | | R18 |
| J15 | N9 | T12 | | L6 | V13 | | T17 |
| K8 | N11 | T14 | | L17 | V16 | | T18 |
| K9 | N12 | T15 | | | | | U10 |
| | | | | | | | U11 |
| | | | | | | | U15 |
| | | | | | | | V11 |
| | | | | | V15 | | |

Table 25 PES32H8G2 Power Pins

Ground Pins

| V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} | V _{SS} |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| A1 | D4 | H4 | L20 | R10 | W12 |
| A5 | D7 | H7 | M1 | R13 | W15 |
| A8 | D9 | H10 | M2 | R16 | W17 |
| A10 | D12 | H13 | M7 | R19 | Y6 |
| A13 | D14 | H16 | M10 | R20 | Y7 |
| A15 | D16 | H20 | M13 | T3 | Y9 |
| B1 | D19 | J1 | M16 | T4 | Y10 |
| B5 | E1 | J2 | M19 | T7 | Y12 |
| B8 | E2 | J7 | M20 | T10 | Y14 |
| B10 | E3 | J10 | N7 | T13 | Y17 |
| B13 | E4 | J13 | N10 | T16 | Y18 |
| B15 | E14 | J16 | N13 | T21 | AA4 |
| C1 | E16 | K3 | N16 | T22 | AA8 |
| C3 | E19 | K7 | N21 | U3 | AA11 |
| C4 | E20 | K10 | N22 | U4 | AA13 |
| C6 | F1 | K13 | P3 | U20 | AA16 |
| C7 | F2 | K16 | P4 | V5 | AA19 |
| C9 | F20 | K21 | P7 | V7 | AB8 |
| C11 | G3 | K22 | P10 | V10 | AB11 |
| C12 | G7 | L3 | P13 | V12 | AB13 |
| C14 | G10 | L4 | P16 | V19 | AB16 |
| C17 | G13 | L7 | P20 | V20 | AB19 |
| D1 | G16 | L10 | R1 | W1 | |
| D2 | G21 | L13 | R2 | W9 | |
| D3 | G22 | L16 | R7 | W10 | |

Table 26 PES32H8G2 Ground Pins

Signals Listed Alphabetically

| Signal Name | I/O Type | Location | Signal Category |
|---------------|---|----------|------------------------------|
| CLKMODE0 | I | AA1 | System |
| CLKMODE1 | I | A21 | |
| CLKMODE2 | I | Y3 | |
| GCLKFSEL | I | AA2 | |
| GCLKN0 | I | B9 | PCI Express |
| GCLKN1 | I | AA12 | |
| GCLKP0 | I | A9 | |
| GCLKP1 | I | AB12 | |
| GPIO_00 | I/O | AB20 | General Purpose Input/Output |
| GPIO_01 | I/O | AB21 | |
| GPIO_02 | I/O | AB22 | |
| GPIO_03 | I/O | AA20 | |
| GPIO_04 | I/O | AA21 | |
| GPIO_05 | I/O | AA22 | |
| GPIO_06 | I/O | Y20 | |
| GPIO_07 | I/O | Y21 | |
| GPIO_08 | I/O | Y22 | |
| JTAG_TCK | I | B22 | JTAG |
| JTAG_TDI | I | D20 | |
| JTAG_TDO | O | A20 | |
| JTAG_TMS | I | B20 | |
| JTAG_TRST_N | I | C20 | |
| MSMBCLK | I/O | B19 | SMBus |
| MSMBDAT | I/O | A19 | |
| NO CONNECTION | Refer to Table 24 for a listing of No Connect pins. | | |
| P00CLKN | I | J21 | PCI Express |
| P00CLKP | I | J22 | |
| P01CLKN | I | H21 | |
| P01CLKP | I | H22 | |
| P02CLKN | I | B14 | |
| P02CLKP | I | A14 | |

Table 27 PES32H8G2 Alphabetical Signal List (Part 1 of 6)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|-----------------|
| P01MERGEN | I | Y1 | System |
| P23MERGEN | I | W2 | |
| P45MERGEN | I | W3 | |
| P67MERGEN | I | Y2 | |
| PE00RN0 | I | G20 | PCI Express |
| PE00RN1 | I | H19 | |
| PE00RN2 | I | K20 | |
| PE00RN3 | I | L19 | |
| PE00RP0 | I | G19 | |
| PE00RP1 | I | H18 | |
| PE00RP2 | I | K19 | |
| PE00RP3 | I | L18 | |
| PE00TN0 | O | E21 | |
| PE00TN1 | O | F21 | |
| PE00TN2 | O | L21 | |
| PE00TN3 | O | M21 | |
| PE00TP0 | O | E22 | |
| PE00TP1 | O | F22 | |
| PE00TP2 | O | L22 | |
| PE00TP3 | O | M22 | |
| PE01RN0 | I | N20 | |
| PE01RN1 | I | P19 | |
| PE01RN2 | I | T20 | |
| PE01RN3 | I | U19 | |
| PE01RP0 | I | N19 | |
| PE01RP1 | I | P18 | |
| PE01RP2 | I | T19 | |
| PE01RP3 | I | U18 | |
| PE01TN0 | O | P21 | |
| PE01TN1 | O | R21 | |
| PE01TN2 | O | U21 | |
| PE01TN3 | O | V21 | |
| PE01TP0 | O | P22 | |
| PE01TP1 | O | R22 | |
| PE01TP2 | O | U22 | |
| PE01TP3 | O | V22 | |

Table 27 PES32H8G2 Alphabetical Signal List (Part 2 of 6)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|---------------------|
| PE02RN0 | I | C18 | PCI Express (Cont.) |
| PE02RN1 | I | D17 | |
| PE02RN2 | I | C15 | |
| PE02RN3 | I | C13 | |
| PE02RP0 | I | D18 | |
| PE02RP1 | I | E17 | |
| PE02RP2 | I | D15 | |
| PE02RP3 | I | D13 | |
| PE02TN0 | O | B17 | |
| PE02TN1 | O | B16 | |
| PE02TN2 | O | B12 | |
| PE02TN3 | O | B11 | |
| PE02TP0 | O | A17 | |
| PE02TP1 | O | A16 | |
| PE02TP2 | O | A12 | |
| PE02TP3 | O | A11 | |
| PE03RN0 | I | C10 | |
| PE03RN1 | I | C8 | |
| PE03RN2 | I | D6 | |
| PE03RN3 | I | C5 | |
| PE03RP0 | I | D10 | |
| PE03RP1 | I | D8 | |
| PE03RP2 | I | E6 | |
| PE03RP3 | I | D5 | |
| PE03TN0 | O | B7 | |
| PE03TN1 | O | B6 | |
| PE03TN2 | O | B4 | |
| PE03TN3 | O | B3 | |
| PE03TP0 | O | A7 | |
| PE03TP1 | O | A6 | |
| PE03TP2 | O | A4 | |
| PE03TP3 | O | A3 | |
| PE04RN0 | I | V3 | |
| PE04RN1 | I | R3 | |
| PE04RN2 | I | N4 | |
| PE04RN3 | I | M3 | |

Table 27 PES32H8G2 Alphabetical Signal List (Part 3 of 6)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|---------------------|
| PE04RP0 | I | V4 | PCI Express (Cont.) |
| PE04RP1 | I | R4 | |
| PE04RP2 | I | N5 | |
| PE04RP3 | I | M4 | |
| PE04TN0 | O | U2 | |
| PE04TN1 | O | T2 | |
| PE04TN2 | O | P2 | |
| PE04TN3 | O | N2 | |
| PE04TP0 | O | U1 | |
| PE04TP1 | O | T1 | |
| PE04TP2 | O | P1 | |
| PE04TP3 | O | N1 | |
| PE05RN0 | I | K4 | |
| PE05RN1 | I | J3 | |
| PE05RN2 | I | G4 | |
| PE05RN3 | I | F3 | |
| PE05RP0 | I | K5 | |
| PE05RP1 | I | J4 | |
| PE05RP2 | I | G5 | |
| PE05RP3 | I | F4 | |
| PE05TN0 | O | L2 | |
| PE05TN1 | O | K2 | |
| PE05TN2 | O | H2 | |
| PE05TN3 | O | G2 | |
| PE05TP0 | O | L1 | |
| PE05TP1 | O | K1 | |
| PE05TP2 | O | H1 | |
| PE05TP3 | O | G1 | |
| PE06RN0 | I | Y5 | |
| PE06RN1 | I | W6 | |
| PE06RN2 | I | Y8 | |
| PE06RN3 | I | Y11 | |
| PE06RP0 | I | W5 | |
| PE06RP1 | I | V6 | |
| PE06RP2 | I | W8 | |
| PE06RP3 | I | W11 | |

Table 27 PES32H8G2 Alphabetical Signal List (Part 4 of 6)

| Signal Name | I/O Type | Location | Signal Category |
|-------------|----------|----------|----------------------------|
| PE06TN0 | O | AA6 | PCI Express (Cont.) |
| PE06TN1 | O | AA7 | |
| PE06TN2 | O | AA9 | |
| PE06TN3 | O | AA10 | |
| PE06TP0 | O | AB6 | |
| PE06TP1 | O | AB7 | |
| PE06TP2 | O | AB9 | |
| PE06TP3 | O | AB10 | |
| PE07RN0 | I | Y13 | |
| PE07RN1 | I | W14 | |
| PE07RN2 | I | Y16 | |
| PE07RN3 | I | Y19 | |
| PE07RP0 | I | W13 | |
| PE07RP1 | I | V14 | |
| PE07RP2 | I | W16 | |
| PE07RP3 | I | W19 | |
| PE07TN0 | O | AA14 | |
| PE07TN1 | O | AA15 | |
| PE07TN2 | O | AA17 | |
| PE07TN3 | O | AA18 | |
| PE07TP0 | O | AB14 | |
| PE07TP1 | O | AB15 | |
| PE07TP2 | O | AB17 | |
| PE07TP3 | O | AB18 | |
| PERSTN | I | C19 | System |
| REFRES00 | I/O | J19 | SerDes Reference Resistors |
| REFRES01 | I/O | K18 | |
| REFRES02 | I/O | C16 | |
| REFRES03 | I/O | E11 | |
| REFRES04 | I/O | N3 | |
| REFRES05 | I/O | H3 | |
| REFRES06 | I/O | W7 | |
| REFRES07 | I/O | Y15 | |
| REFRESPLL | I/O | D11 | |
| RSTHALT | I | AB2 | System |

Table 27 PES32H8G2 Alphabetical Signal List (Part 5 of 6)

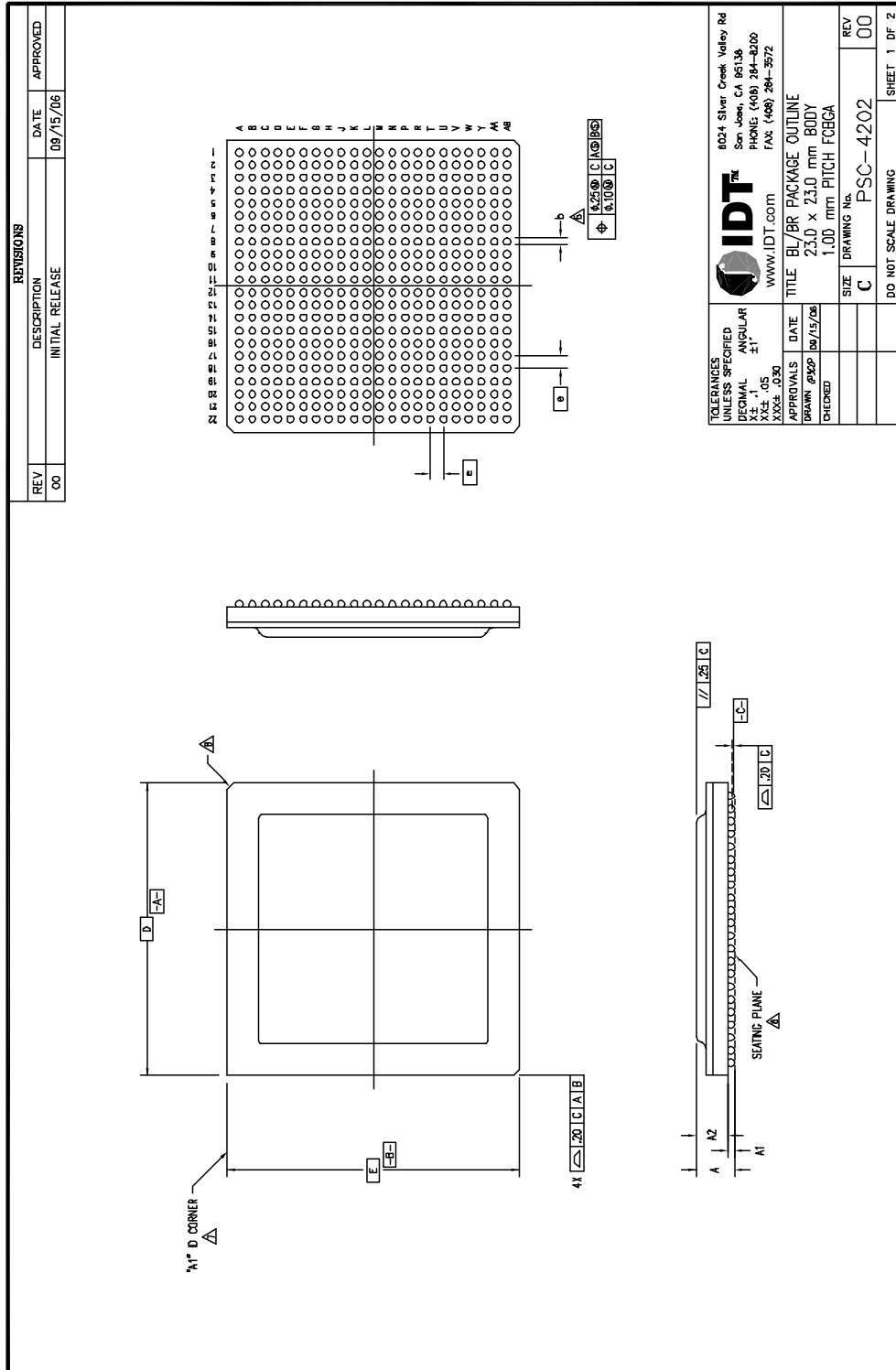
| Signal Name | I/O Type | Location | Signal Category |
|--|---|----------|-----------------|
| SSMBADDR1 | I | C22 | SMBus |
| SSMBADDR2 | I | A22 | |
| SSMBCLK | I/O | B21 | |
| SSMBDAT | I/O | C21 | |
| SWMODE0 | I | AA3 | System |
| SWMODE1 | I | AB1 | |
| SWMODE2 | I | AB3 | |
| SWMODE3 | I | AB4 | |
| V _{DD} CORE, V _{DD} -PEA, V _{DD} IO, V _{DD} PE, V _{TT} PE | Refer to Table 25 for a listing of No Connect pins. | | |
| V _{SS} | Refer to Table 26 for a listing of No Connect pins. | | |

Table 27 PES32H8G2 Alphabetical Signal List (Part 6 of 6)

PES32H8G2 Pinout — Top View



PES32H8G2 Package Drawing — 484-Pin BL484/BR484



| REVISIONS | | DATE | APPROVED |
|-----------|-----------------|----------|----------|
| REV | DESCRIPTION | | |
| 00 | INITIAL RELEASE | 09/15/06 | |

| | | |
|--|---|---|
| IDT 8024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-4200 FAX: (408) 284-3972 www.IDT.com | | TITLE: BL/BR PACKAGE OUTLINE 23.0 x 23.0 mm BODY 1.00 mm PITCH FBGA |
| TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X.2, .1 ±1° X.25, .05 X.05, .020 | APPROVALS DATE DRAWN PWS/DW/15/06 CHECKED | DRAWING No. PSC-4202 REV 00 DO NOT SCALE DRAWING SHEET 1 OF 2 |

| REV | DESCRIPTION | DATE | APPROVED |
|-----|-----------------|----------|----------|
| 00 | INITIAL RELEASE | 09/15/06 | |

NOTES:

- 1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- 2 "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
- 3 "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
- 4 "N" REPRESENTS THE BALLCOUNT NUMBER

△ DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-

△ SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

△ "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY

△ EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 ALL DIMENSIONS ARE IN MILLIMETERS

484 BALLS

| SYMBOL | JEDEC VARIATION | | | NOTE |
|--------------------|-----------------|-----|------|------|
| | MIN | NOM | MAX | |
| A | - | - | 3.32 | |
| A1 | - | .50 | - | |
| A2 | 2.36 | - | 2.72 | |
| D | 23.00 BSC | | | |
| E | 23.00 BSC | | | |
| M | 22 | | | 3 |
| N | 484 | | | 4 |
| e | 1.00 BSC | | | |
| b | .50 | .64 | .70 | 5 |
| CENTER BALL MATRIX | N/A | | | |

| TOLERANCES UNLESS SPECIFIED | DATE | DRAWING No. | REV | TITLE |
|-----------------------------|----------|-------------|-----|-----------------------|
| DECIMAL ANGULAR ±1° | 09/15/06 | PSC-4202 | 00 | BL/BR PACKAGE OUTLINE |
| X±.1 | | | | 23.0 x 23.0 mm BODY |
| X±.05 | | | | 1.00 mm PITCH FCBGA |
| X±.025 | | | | |
| APPROVALS | | | | |
| DRAWN PVP/P | | | | |
| CHECKED | | | | |

| | |
|---|---|
| <p style="font-size: small;">4024 Silver Creek Valley Rd San Jose, CA 95136 PHONE: (408) 284-6200 FAX: (408) 284-3572 www.IDT.com</p> | <p style="font-size: x-small;">DO NOT SCALE DRAWING</p> <p style="font-size: x-small;">SHEET 2 OF 2</p> |
|---|---|

Revision History

January 21, 2010: Publication of Final data sheet.

March 30, 2011: In Table 13, added $V_{DD}PETA$ to footnote #1.

November 28, 2011: Added new Tables 20 and 21, SMBus Characterization and Timing.

Ordering Information



Legend
 A = Alpha Character
 N = Numeric Character

Valid Combinations

- 89H32H8G2ZBBL 484-ball FCBGA package, Commercial Temperature
- 89H32H8G2ZBBLG 484-ball Green FCBGA package, Commercial Temperature
- 89H32H8G2ZBBLI 484-ball FCBGA package, Industrial Temperature
- 89H32H8G2ZBBLGI 484-ball Green FCBGA package, Industrial Temperature
- 89H32H8G2ZCBL 484-ball FCBGA package, Commercial Temperature
- 89H32H8G2ZCBLG 484-ball Green FCBGA package, Commercial Temperature
- 89H32H8G2ZCBLI 484-ball FCBGA package, Industrial Temperature
- 89H32H8G2ZCBLGI 484-ball Green FCBGA package, Industrial Temperature



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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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