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FAIRCHILD SEMICONDUCTOR®

February 2013

FAN4931
Ultra-Low Cost, Rail-to-Rail I/O, CMOS Amplifier

Features

- 200 µA Supply Current per Amplifier
- 3.7 MHz Bandwidth
- Output Swing to within 10 mV of Either Rail
- Input Voltage Range Exceeds the Rails
- 3 V/µs Slew Rate
- 25 nV/√Hz Input Voltage Noise
- FAN4931 Competes with LMV931; Available in SC70-5 Package
- Fully Specified at +2.7 V and +5 V Supplies

Applications

- Motor Control
- Portable / Battery-Powered Applications
- PCMCIA, USB
- Mobile Communications, Cellular Phones, Pagers
- Notebooks and PDAs
- Sensor Interface
- A/D Buffer
- Active Filters
- Signal Conditioning
- Portable Test Instruments

Description

FAN4931 is an ultra-low cost voltage feedback amplifier with CMOS inputs that consumes only 200 µA of supply current, while providing ±33 mA of output short-circuit current. This amplifier is designed to operate from 2.5 V to 5 V supplies. The common-mode voltage range extends beyond the negative and positive rails.

The FAN4931 is designed on a CMOS process and provides 3.7 MHz of bandwidth and 3 V / µs of slew rate at a supply voltage of 5 V. This amplifier operates and is reliable over a wide temperature range -40°C to +125°C. The combination of extended temperature operation, low power, rail-to-rail performance, low voltage operation,and tiny package optimizes this amplifier for use in many industrial, general purpose and battery powered applications.

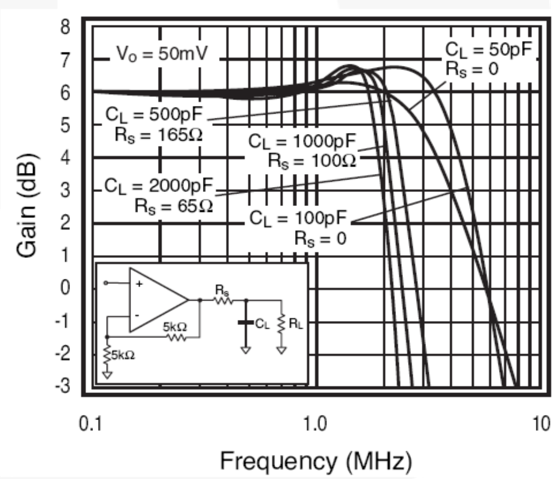

Figure 1. Frequency vs. Gain

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN4931IP5X	-40 to +125°C	5-Lead SC70 Package	Tape and Reel (3000)

Typical Application

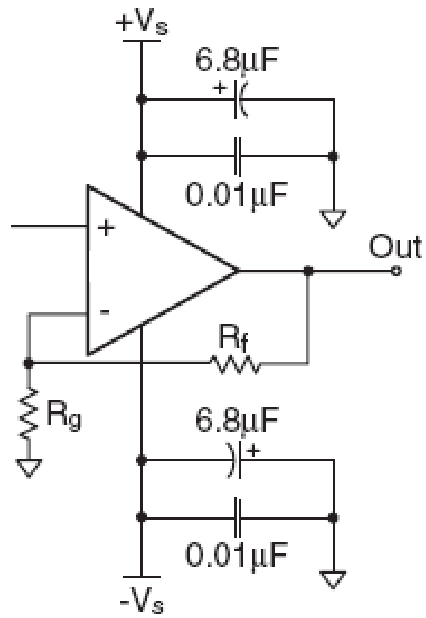

Figure 2. Typical Application

Pin Configurations

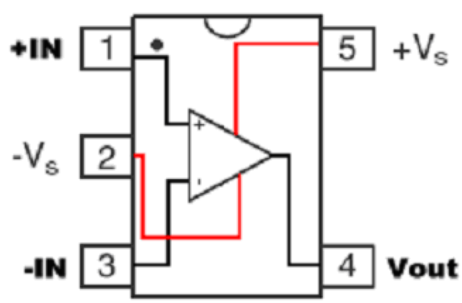

Figure 3. Pin Assignments

Pin Assignments

Pin #	Name	Description
1	+IN	Positive Input
2	$-V_S$	Negative Supply
3	-IN	Negative Input
4	V_{OUT}	Output
5	$+V_S$	Positive Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if operating conditions are not exceeded.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		0	6	V
V_{IN}	Input Voltage Range		$-V_S$-0.5	$+V_S$+0.5	V
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature		-65	+150	°C
T_L	Lead Soldering, 10 Seconds			+300	°C
Θ_{JA}	Thermal Resistance(1)			331	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		5	kV
		Charged Device Model, JESD22-C101		2	

Note:

1. Package thermal resistance JEDEC standard, multi-layer test boards, still air.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
$+V_S$	Supply Voltage	2.30	5.25	V
T_A	Operating Temperature Range	-40	+125	°C

Electrical Specifications at +2.7V

V_S=+2.7 V, G=2, R_L=10 kΩ to V_S/2, R_F=5 kΩ; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G=+1		4.0		MHz
BW_{SS}	-3dB Bandwidth			2.5		MHz
GBWP	Gain Bandwidth Product			4		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_O=1.0 V Step		300		ns
OS	Overshoot	V_O=1.0 V Step		5		%
SR	Slew Rate	V_O=3 V Step, G=-1		3		V/µs
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_O=1 V_{PP}, 10 kHz		-66		dBc
HD3	3rd Harmonic Distortion	V_O=1 V_{PP}, 10 kHz		-67		dBc
THD	Total Harmonic Distortion	V_O=1 V_{PP}, 10 kHz		0.1		%
e_n	Input Voltage Noise			26		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage(2)		-6	0	+6	mV
dV_{IO}	Average Drift			2.1		µV/°C
I_{bn}	Input Bias Current			5		pA
PSRR	Power Supply Rejection Ratio(2)	DC	50	73		dB
A_{OL}	Open-Loop Gain	DC		98		dB
I_S	Supply Current per Amplifier(2)			200	300	µA
Input Characteristics						
R_{IN}	Input Resistance			10		GΩ
C_{IN}	Input Capacitance			1.4		pF
CMIR	Input Common Mode Voltage Range			-0.3 to 2.8		V
CMRR	Common Mode Rejection Ratio(2)	DC, V_{CM}=OV to 2.2 V	50	65		dB
Output Characteristics						
V_O	Output Voltage Swing(2)	R_L=10 kΩ to V_S/2	0.03	0.01 to 2.69	2.65	V
		R_L=1 kΩ to V_S/2		0.05 to 2.55		V
I_{SC}	Short-Circuit Output Current			+34/-12		mA
V_S	Power Supply Operating Range			2.5 to 5.5		V

Note:
2. 100% tested at T_A=25°C.

Electrical Specifications at +5V

V_S=+5 V, G=2, R_L=10 kΩ to V_S/2, R_F= 5 kΩ; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Frequency Domain Response						
UGBW	-3dB Bandwidth	G=+1		3.7		MHz
BW_{SS}	-3dB Bandwidth			2.3		MHz
GBWP	Gain Bandwidth Product			3.7		MHz
Time Domain Response						
t_R, f_F	Rise and Fall Time	V_O=1.0 V Step		300		ns
OS	Overshoot	V_O=1.0 V Step		5		%
SR	Slew Rate	V_O=3 V Step, G=-1		3		V/µs
Distortion and Noise Response						
HD2	2nd Harmonic Distortion	V_O=1 V_{PP}, 10 kHz		-80		dBc
HD3	3rd Harmonic Distortion	V_O=1 V_{PP}, 10 kHz		-80		dBc
THD	Total Harmonic Distortion	V_O=1 V_{PP}, 10 kHz		0.02		%
e_n	Input Voltage Noise			25		nV/√Hz
DC Performance						
V_{IO}	Input Offset Voltage(3)		-8	0	+8	mV
dV_{IO}	Average Drift			2.9		µV/°C
I_{bn}	Input Bias Current			5		pA
PSRR	Power Supply Rejection Ratio(3)	DC	50	73		dB
A_{OL}	Open-Loop Gain	DC		102		dB
I_S	Supply Current per Amplifier(3)			200	300	µA
Input Characteristics						
R_{IN}	Input Resistance			10		GΩ
C_{IN}	Input Capacitance			1.2		pF
CMIR	Input Common Mode Voltage Range	Typical		-0.3 to 5.1		V
CMRR	Common Mode Rejection Ratio(3)	DC, V_{CM}=0 V to V_S	58	73		dB
Output Characteristics						
V_O	Output Voltage Swing(3)	R_L=10 kΩ to V_S/2	0.03	0.01 to 4.99	4.95	V
		R_L=1 kΩ to V_S/2		0.1 to 4.9		V
I_{SC}	Short-Circuit Output Current			±33		mA
V_S	Power Supply Operating Range			2.5 to 5.5		V

Note:

3. 100% tested at T_A=25°C.

Typical Performance Characteristics

V_S=+2.7, G=2, R_L=10 kΩ to V_S/2, R_F=5 kΩ; unless otherwise noted.

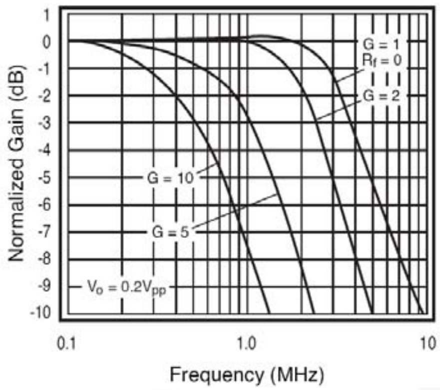

Figure 4. Non-Inverting Frequency Response (+5)

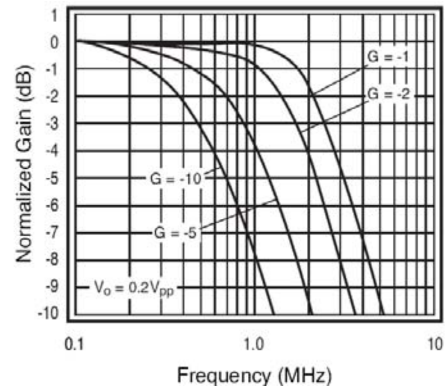

Figure 5. Inverting Frequency Response (+5 V)

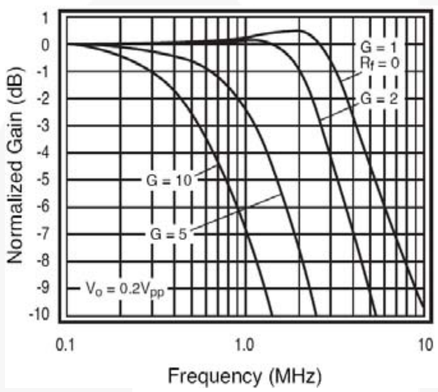

Figure 6. Non-Inverting Frequency Response

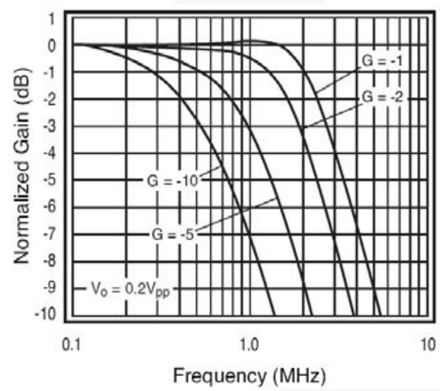

Figure 7. Inverting Frequency Response

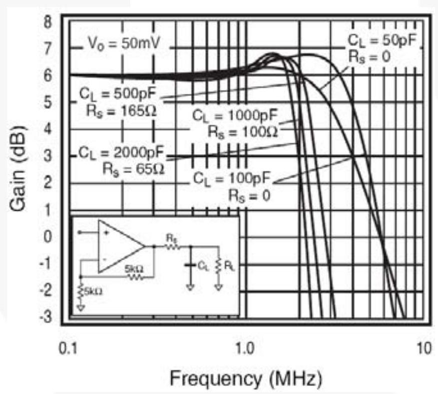

Figure 8. Frequency Response vs. C_L

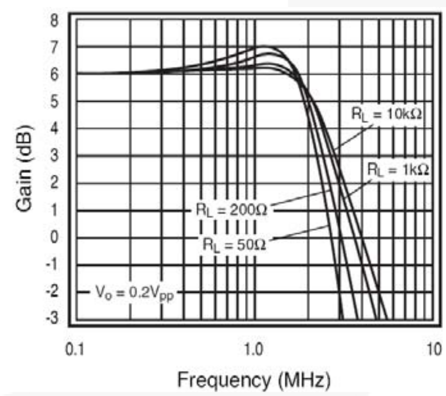

Figure 9. Frequency Response vs. R_L

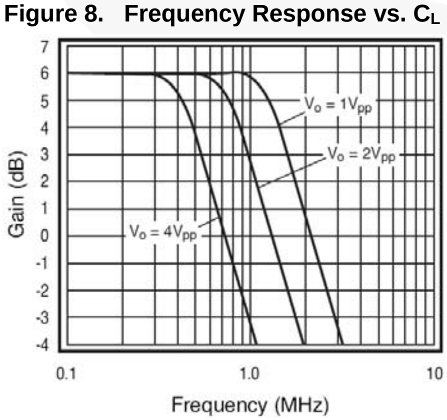

Figure 10. Large Signal Frequency Response (+5 V)

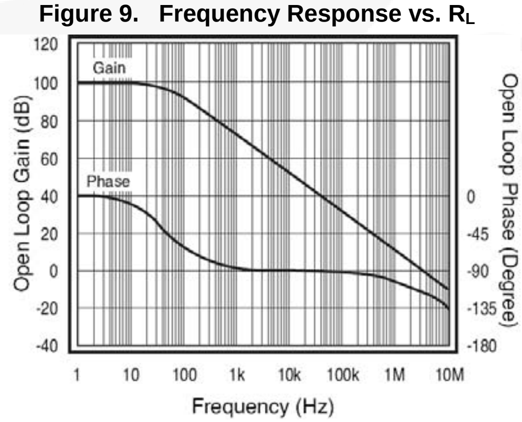

Figure 11. Open-Loop Gain and Phase vs. Frequency

Typical Performance Characteristic

V_S=+2.7, G=2, R_L=10 kΩ to V_S/2, R_F=5 kΩ; unless otherwise noted.

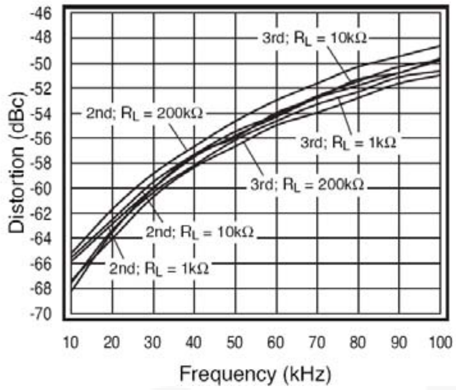

Figure 12. 2nd and 3rd Harmonic Distortion

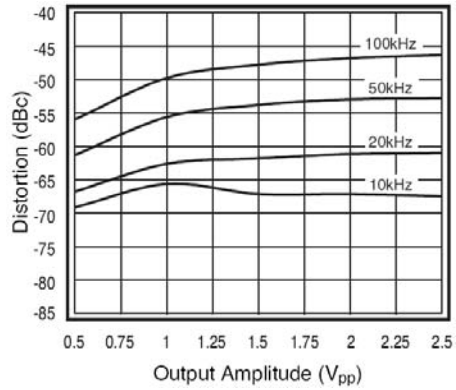

Figure 13. 2nd Harmonic Distortion vs. V_O

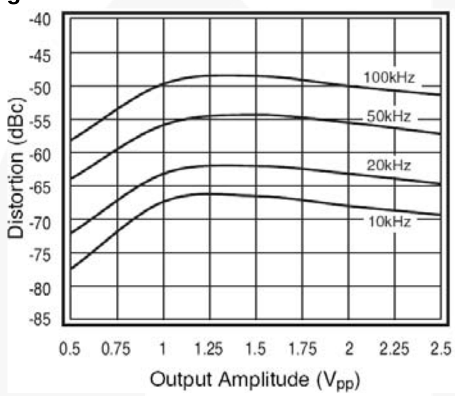

Figure 14. 3rd Harmonic Distortion vs. V_O

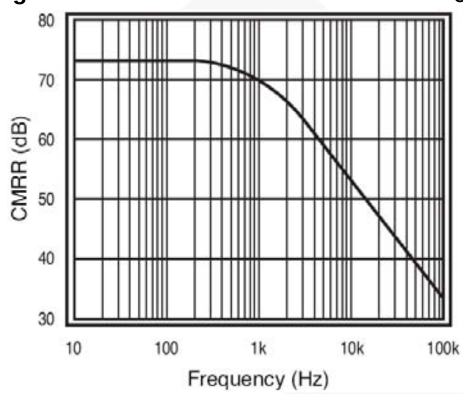

Figure 15. CMRR V_S=5 V

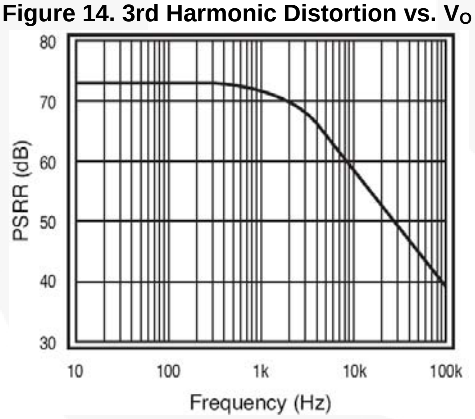

Figure 16. PSRR V_S=5 V

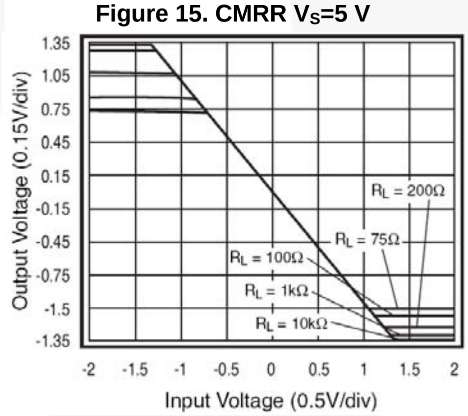

Figure 17. Output Swing vs. Load

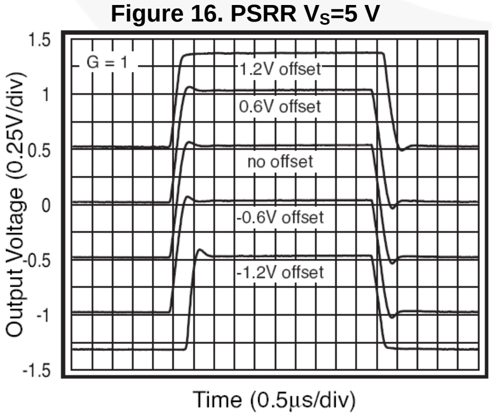

Figure 18. Pulse Response vs. Common-Mode Voltage

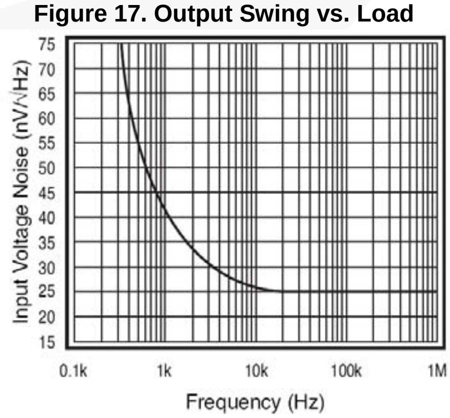

Figure 19. Input Voltage Noise

Application Information

General Description

The FAN4931 amplifier is a single-supply, general-purpose, voltage-feedback amplifier, fabricated on a bi-CMOS process. It features a rail-to-rail input and output and is unity gain stable. The typical non-inverting circuit schematic is shown in Figure 20.

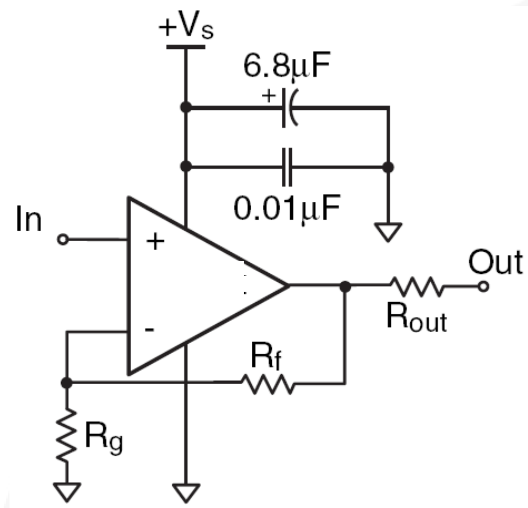

Figure 20. Typical Non-Inverting Configuration

Input Common-Mode Voltage

The common-mode input range extends to 300 mV below ground and to 100 mV above V_S in single-supply operation. Exceeding these values does not cause phase reversal; however, if the input voltage exceeds the rails by more than 0.5 V, the input ESD devices begin to conduct. The output stays at the rail during this overdrive condition. If the absolute maximum input V_{IN} (700 mV beyond either rail) is exceeded, externally limit the input current to ±5 mA, as shown in Figure 21.

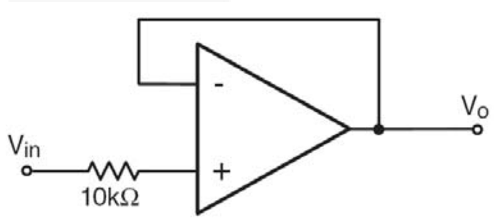

Figure 21. Circuit for Input Current Protection

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, performance degradation occurs. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur.

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the range is exceeded. The FAN4931 typically recovers in less than 500 ns from an overdrive condition. Figure 22 shows the FAN4931 amplifier in an overdriven condition.

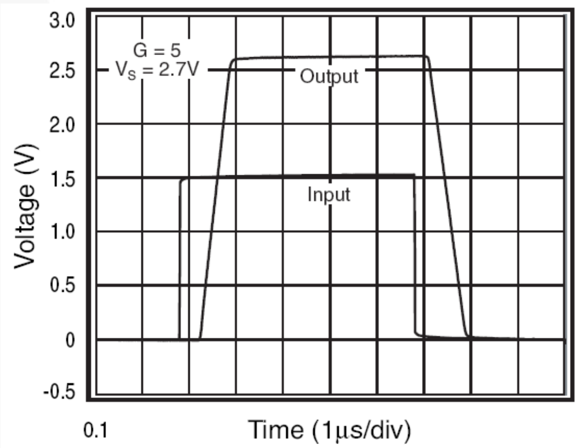

Figure 22. Overdrive Recovery

Driving Capacitive Loads

Figure 8 illustrates the response of the amplifier. A small series resistance (R_S) at the output, illustrated in Figure 23, improves stability and settling performance. R_S values in Figure 8 were chosen to achieve maximum bandwidth with less than 2 dB of peaking. For maximum flatness, use a larger R_S. Capacitive loads larger than 500 pF require the use of R_S.

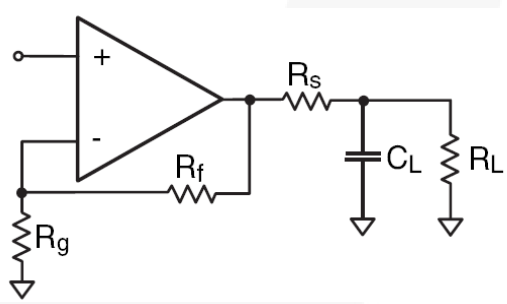

Figure 23. Typical Topology for Driving a Capacitive Load

Driving a capacitive load introduces phase-lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the amplifier requires a 300 Ω–series resistor to drive a 100 pF load.

Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance. Fairchild evaluation boards help guide high-frequency layout and aid in device testing and characterization. Follow the steps below as a basis for high-frequency layout:

Include 6.8 µF and 0.01 µF ceramic capacitors.

Place the 6.8 µF capacitor within 0.75 inches of the power pin.

Place the 0.01 µF capacitor within 0.1 inches of the power pin.

Remove the ground plane under and around the part, especially near the input and output pins, to reduce parasitic capacitance.

Minimize all trace lengths to reduce series inductances.

Refer to the evaluation board layouts shown in Figure 24-Figure 26 for more information.

When evaluating only one channel, complete the following on the unused channel:

Ground the non-inverting input.

Short the output to the inverting input.

Evaluation Board Information

The following evaluation board is available to aid in the testing and layout of this device.

Evaluation Board	Description	Products
FAN4931-011	Single-Channel, Dual-Supply, 5 -Lead SC70	FAN4931IP5X

Evaluation board schematics are shown in Figure 24; layouts are shown in Figure 25-Figure 26.

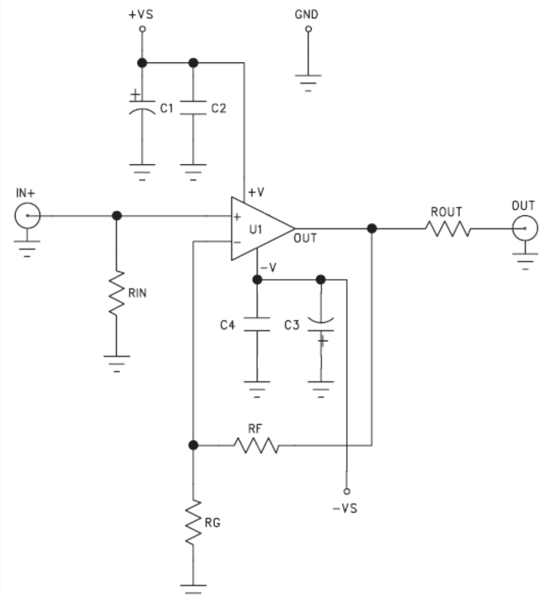

Figure 24. Evaluation Board Schematic

Board Layout Information

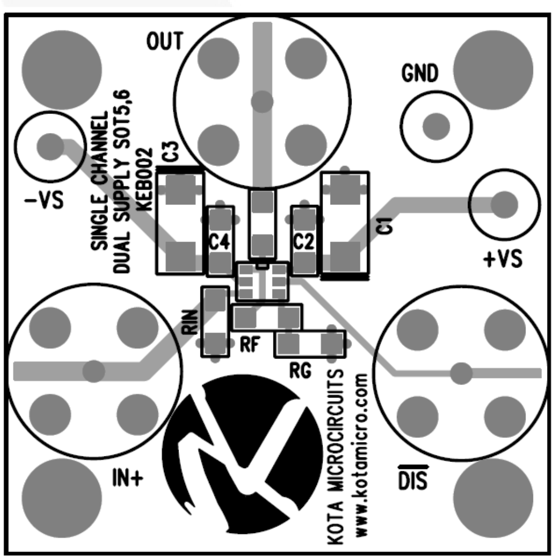

Figure 25. Top Side

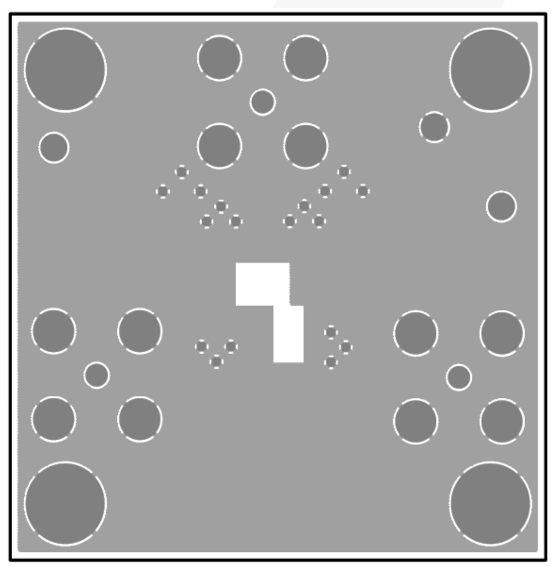

Figure 26. Bottom Side

Physical Dimensions

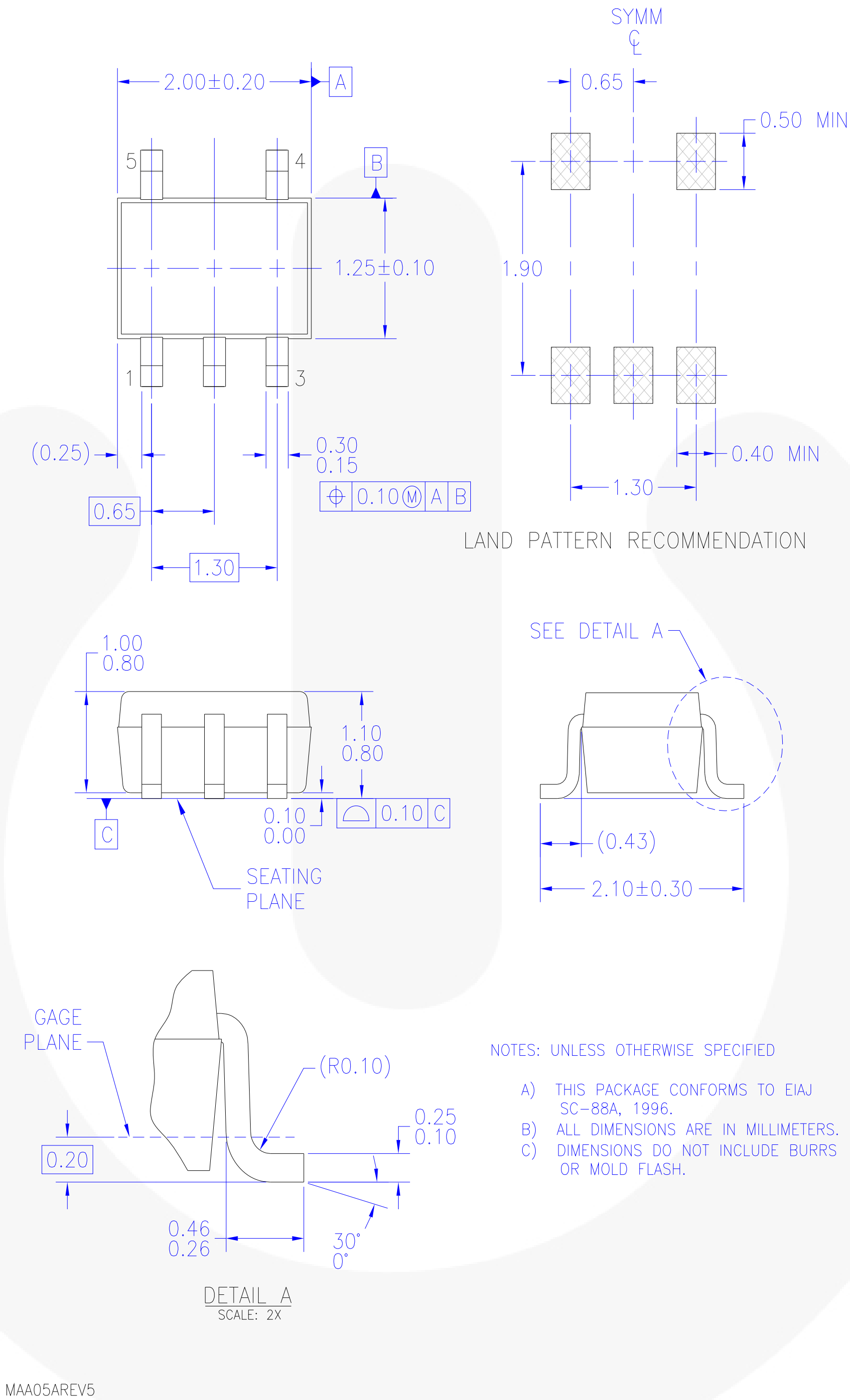

Figure 27. 5-Lead SC70 Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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SuperFET®
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SuperSOT™-6
SuperSOT™-8
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
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