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DS28C40

DeepCover Automotive I²C Authenticator

General Description

The DS28C40 is a secure authenticator that provides a core set of cryptographic tools derived from integrated asymmetric (ECC-P256) and symmetric (SHA-256) security functions. In addition to the security services provided by the hardware implemented crypto engines, the device integrates a FIPS/NIST true random number generator (TRNG), 6kb of one-time programmable (OTP) memory for user data, keys and certificates, one configurable GPIO, and a unique 64-bit ROM identification number (ROM ID).

The ECC public/private key capabilities operate from the NIST defined P-256 curve and include FIPS 186-4 compliant ECDSA signature generation and verification to support a bidirectional asymmetric key authentication model. The SHA-256 secret-key capabilities are compliant with FIPS 180 and are flexibly used either in conjunction with ECDSA operations or independently for multiple HMAC functions.

The GPIO pin can be operated under command control and include configurability supporting authenticated and nonauthenticated operation including an ECDSA-based crypto-robust mode to support secure boot of a host processor.

DeepCover® embedded security solutions cloak sensitive data under multiple layers of advanced security to provide the most secure key storage possible. To protect against device-level security attacks, invasive and noninvasive countermeasures are implemented including active die shield, encrypted storage of keys, and algorithmic methods.

Applications

- Automotive Secure Authentication
- Identification and Calibration Automotive Parts/Tools/Accessories
- IoT Node Crypto-Protection
- Secure Authentication of Accessories and Peripherals
- Secure Storage of Cryptographic Keys for a Host Controller
- Secure Boot or Download of Firmware and/or System Parameters

Benefits and Features

- ECC-P256 Compute Engine
 - FIPS 186 ECDSA P256 Signature Generation and Verification
 - ECDH Key Exchange for Session Key Establishment
 - ECDSA Authenticated R/W of Configurable Memory
- SHA-256 Compute Engine
 - FIPS 198 HMAC for Bidirectional Authentication
- SHA-256 One-Time Pad Encrypted R/W of Configurable Memory Using an ECDH Established Key
- One GPIO Pin with Optional Authentication Control
 - Open-Drain, 4mA/0.4V
 - Optional SHA-256 or ECDSA Authenticated On/Off and State Read
 - Optional ECDSA Certificate Verification to Set On/Off after Multiblock Hash for Secure Boot
- TRNG with NIST SP 800-90B Compliant Entropy Source with Function to Read Out
- Optional Chip Generated Private/Public (Pr/Pu) Key Pairs for ECC Operations
- 6Kb of One-Time Programmable (OTP) for User Data, Keys, and Certificates
- Unique and Unalterable Factory Programmed 64-Bit Identification Number (ROM ID)
 - Optional Input Data Component to Crypto and Key Operations
- I²C Communication Up to 1MHz
- 3.3V ±10%, -40°C to +125°C Operating Range
- 10-Pin, 3mm x 4mm TDFN Package
- AEC-Q100 Grade 1

Ordering Information appears at end of data sheet.

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Simplified Block Diagram

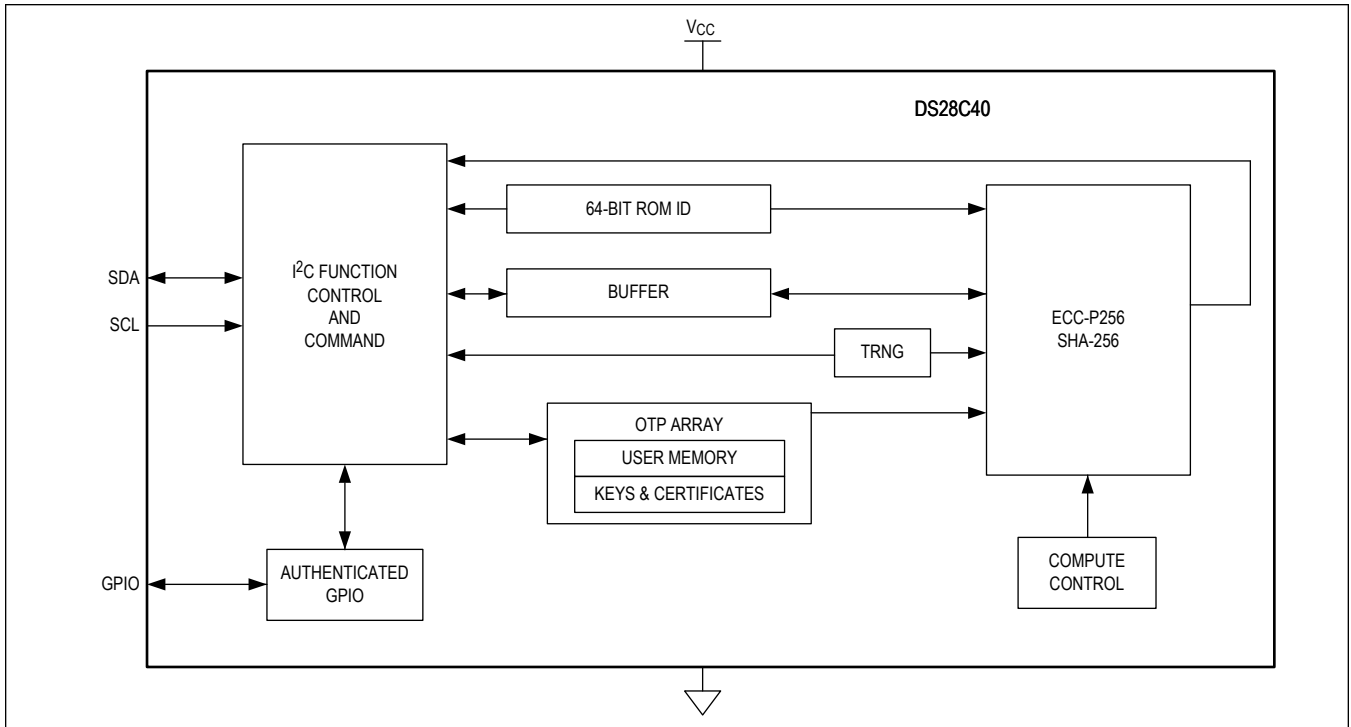


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Absolute Maximum Ratings

Voltage Range on Any Pin Relative to GND -0.5V to 4.0V
 Maximum Current into Any Pin -20mA to 20mA
 Operating Temperature Range -40°C to +125°C
 Junction Temperature +150°C
 Storage Temperature Range -40°C to +150°C

Lead Temperature (soldering, 10s) +300°C
 Soldering Temperature (reflow) +260°C

Package Information

10 TDFN

| | |
|---|-------------------------|
| Package Code | T1034+2 |
| Outline Number | 21-0268 |
| Land Pattern Number | 90-0247 |
| Thermal Resistance, Four Layer Board: | |
| Junction-to-Ambient (θ_{JA}) | 60°C/W |
| Junction-to-Case Thermal Resistance (θ_{JC}) | 30°C/W |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(Limits are 100% tested at $T_A = +25^\circ\text{C}$. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------|---|---------------------|----------------------|---------------------|-------|
| Supply Voltage | V_{CC} | (Note 1) | 2.97 | 3.3 | 3.63 | V |
| Supply Current | I_{CC} | Standby | | 0.5 | 2 | mA |
| | | Communicating (Note 12) | | | 16.5 | |
| I²C SCL AND SDA PINS (Note 2) | | | | | | |
| Low-Level Input Voltage | V_{IL} | | -0.3 | | $0.3 \times V_{CC}$ | V |
| High-Level Input Voltage | V_{IH} | | $0.7 \times V_{CC}$ | | $V_{CC} + 0.3$ | V |
| Hysteresis of Schmitt Trigger Inputs | V_{HYS} | (Note 3) | | $0.05 \times V_{CC}$ | | V |
| Low-Level Output Voltage at 4mA Sink Current | V_{OL} | (Note 4) | | | 0.4 | V |

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|---------------------|--|------------------------|-----|-----------------------|-------|
| Output Fall Time from V _{IH(MIN)} to V _{IL(MAX)} with a Bus Capacitance from 10pF to 400pF | t _{OF} | (Note 3) | | 30 | | ns |
| Pulse Width of Spikes that are Suppressed by the Input Filter | t _{SP} | (Note 3) | | | 50 | ns |
| Input Current with an Input Voltage Between 0.1V _{CCmax} and 0.9V _{CCmax} | I _I | (Note 3 , Note 5) | -1 | | +1 | μA |
| Input Capacitance | C _I | (Note 3) | | 10 | | pF |
| SCL Clock Frequency | f _{SCL} | (Note 1) | | | 1 | MHz |
| Hold Time (Repeated) START Condition | t _{HD:STA} | | 0.45 | | | μs |
| Low Period of the SCL Clock | t _{LOW} | (Note 6) | 0.65 | | | μs |
| High Period of the SCL Clock | t _{HIGH} | (Note 3) | 0.35 | | | μs |
| Setup Time for a Repeated START Condition | t _{SU:STA} | (Note 3) | 0.35 | | | μs |
| Data Hold Time | t _{HD:DAT} | (Note 3 , Note 6 , Note 7) | | | 0.35 | μs |
| Data Setup Time | t _{SU:DAT} | (Note 3 , Note 6 , Note 8) | 100 | | | ns |
| Setup Time for STOP Condition | t _{SU:STO} | (Note 3) | 0.35 | | | μs |
| Bus Free Time Between a STOP and START Condition | t _{BUF} | (Note 3) | 0.6 | | | μs |
| Capacitive Load for Each Bus Line | C _B | (Note 1 , Note 9) | | | 400 | pF |
| Warm-Up Time | t _{OSCWUP} | (Note 1 , Note 10) | | | 1 | ms |
| GPIO PIN | | | | | | |
| GPIO Output Low | PIOV _{OL} | PIOI _{OL} = 4mA (Note 4) | | | 0.4 | V |
| GPIO Input Low | PIOV _{IL} | | -0.3 | | 0.3 x V _{CC} | V |
| GPIO Master Sample | PIOV _{IH} | | 0.70 x V _{CC} | | V _{CC} + 0.3 | V |
| GPIO Switching Hysteresis | PIOV _{HY} | | | 0.3 | | V |
| GPIO Leakage Current | PIOI _L | | -1 | | +1 | μA |

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum and maximum operating temperature are guaranteed by design and are not production tested.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|---|-----|-----|------|-------|
| CRYPTO FUNCTIONS | | | | | | |
| Computation Current | I _{CMP} | Note 12 | | 11 | 16.5 | mA |
| Read Memory | t _{RM} | | | | 2 | ms |
| Write Memory | t _{WM} | | | | 150 | ms |
| Write State | t _{WS} | | | | 15 | ms |
| Computation Time (HMAC) | t _{CMP} | | | | 4 | ms |
| Generate ECC Key Pair | t _{GKP} | | | | 500 | ms |
| Generate ECDSA Signature | t _{GES} | | | | 50 | ms |
| Verify ECDSA Signature or Compute ECDH Time | t _{VES} | | | | 160 | ms |
| TRNG Generation | t _{RNG} | | | | 50 | ms |
| TRNG On-Demand Check | t _{ODC} | | | | 50 | ms |
| OTP | | | | | | |
| OTP Write Temperature | T _{OPTW} | | 0 | | 50 | °C |
| Data Retention | t _{DR} | T _A = +125°C (Note 11) | 10 | | | Years |

Note 1: System requirement.

Note 2: All I²C timing values are referred to V_{IH(MIN)} and V_{IL(MAX)} levels.

Note 3: Guaranteed by design and/or characterization only. Not production tested.

Note 4: The I-V characteristic is linear for voltages less than 1V.

Note 5: I/O pins of the DS28C40 do not obstruct the SDA and SCL lines if V_{CC} is switched off.

Note 6: t_{LOW} min = t_{HD:DAT} max + 200ns for rise or fall time + t_{SU:DAT} min. Values greater than these can be accommodated by extending t_{LOW} accordingly.

Note 7: The DS28C40 provides a hold time of at least 100ns for the SDA signal (referenced to the V_{IH(MIN)} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 8: The DS28C40 can be used in a standard-mode I²C-bus system, but the requirement t_{SU:DAT} ≥ 250ns must then be met. Also, the acknowledge timing must meet this setup time (I²C bus specification Rev. 03, 19 June 2007).

Note 9: C_B = Total capacitance of one bus line in pF. The maximum bus capacitance allowable may vary from this value depending on the actual operating voltage and frequency of the application (I²C bus specification Rev. 03, 19 June 2007).

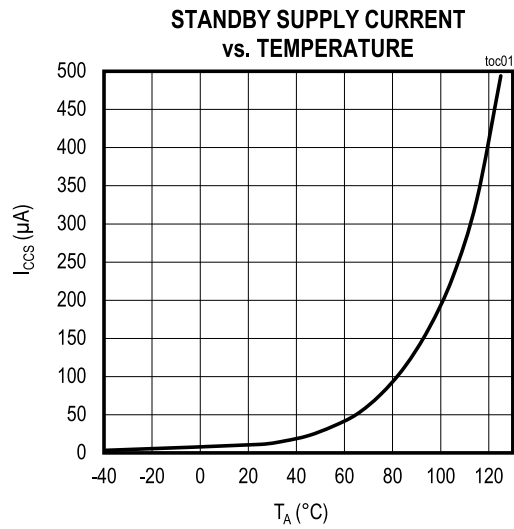
Note 10: I²C communication should not take place for the max t_{OSCWUP} time following a power-on reset.

Note 11: Data retention is tested in compliance with JESD47G.

Note 12: OTP programming current production tested at 25°C.

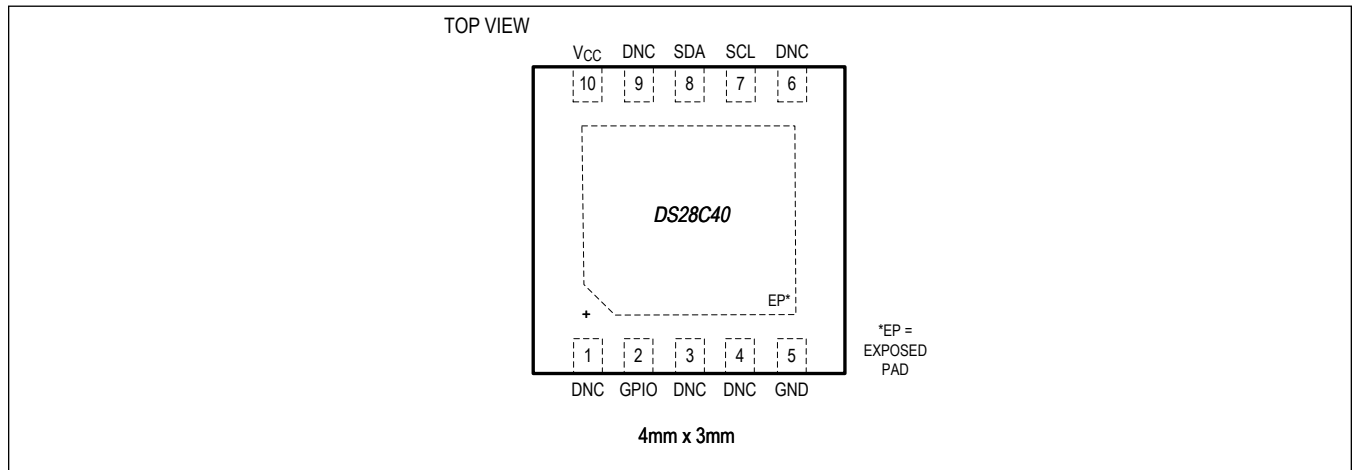
Typical Operating Characteristics

(V_{CC} = +3.63V.)



Pin Configuration

10 TDFN



Pin Description

| PIN | NAME | FUNCTION |
|---------------|------|--------------------|
| 1, 3, 4, 6, 9 | DNC | Do Not Connect |
| 2 | GPIO | General-Purpose IO |

Pin Description (continued)

| PIN | NAME | FUNCTION |
|------------|-----------------|---|
| 5 | GND | Ground |
| 7 | SCL | I ² C Clock (Connect to V _{CC} with pullup resistor) |
| 8 | SDA | I ² C Data (Connect to V _{CC} with pullup resistor) |
| 10 | V _{CC} | Supply Voltage |
| — | EP | Exposed Pad. Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: Exposed Pads: A Brief Introduction for additional information. |

Detailed Description

The DS28C40 secure authenticator for automotive applications provides a core set of cryptographic tools derived from integrated asymmetric (ECC-P256) and symmetric (SHA-256) security functions. In addition to the security services provided by the hardware implemented crypto engines, the device integrates a FIPS/NIST true random number generator (TRNG), 6Kb of secured OTP (3Kb User, 3Kb Keys/Secrets), one configurable GPIO pin, and a unique 64-bit ROM identification number (ROM ID).

I²C

General Characteristics

The I²C bus uses a data line (SDA) plus a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are high. The output stages of devices connected to the bus must have an open drain or open collector to perform the wired-AND function. Data on the I²C bus can be transferred at rates up to 100kbps in standard mode and up to 400kbps in fast mode. The DS28C40 works in both modes or up to a clock rate of 1MHz. A device that sends data on the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The device that controls communication is called a master. Devices controlled by the master are slaves. To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus. Data transfers can be initiated only when the bus is not busy. The master generates the serial clock (SCL), controls the bus access, generates the START and STOP conditions, and determines the number of data bytes transferred between START and STOP [Figure 1](#). Data is transferred in bytes with the most significant bit being transmitted first. After each byte follows an acknowledge bit to allow synchronization between master and slave.

Slave Address

The slave address to which the DS28C40 responds is shown in [Figure 2](#). The slave address is part of the slave address/control byte. The last bit of the slave address/control byte (R/W) defines the data direction. When set to 0, subsequent data flows from master to slave (write access); when set to 1, data flows from slave to master (read access).

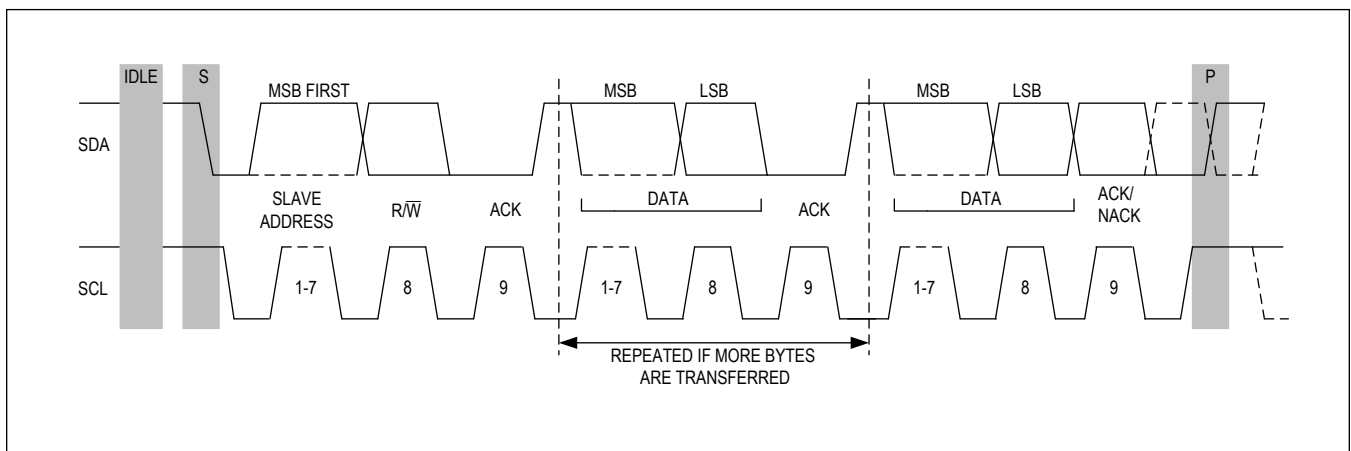


Figure 1. I²C Protocol Overview

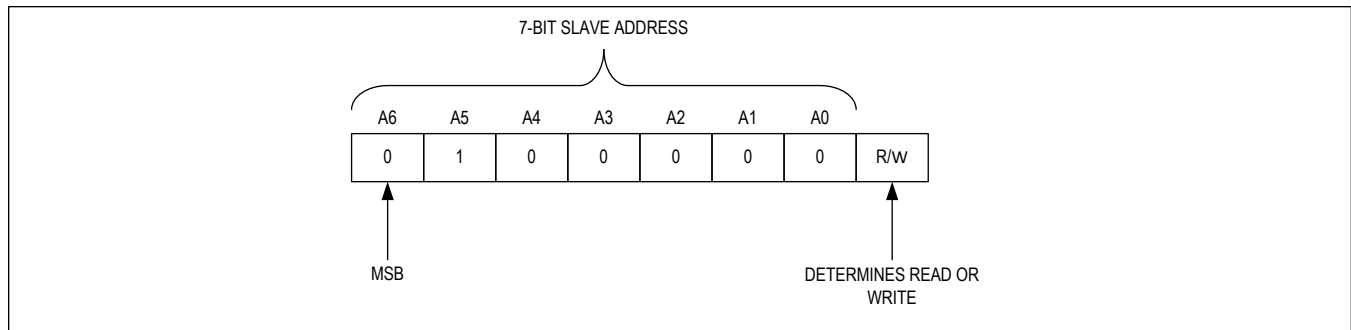


Figure 2. I²C Slave Address

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. The timing references are defined in [Figure 3](#).

Bus Idle or Not Busy

Both SDA and SCL are inactive and in their logic-high states.

START Condition

To initiate communication with a slave, the master must generate a START condition. A START condition is defined as a change in state of SDA from high to low while SCL remains high.

STOP Condition

To end communication with a slave, the master must generate a STOP condition. A STOP condition is defined as a change in state of SDA from low to high while SCL remains high.

Repeated START Condition

Repeated STARTs are commonly used for read accesses after having specified a memory address to read from in a preceding write access. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without leaving the bus idle after a STOP condition.

Data Valid

With the exception of the START and STOP condition, transitions of SDA can occur only during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL; see [Figure 3](#)). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of the SCL pulse.

When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum $t_{SU:DAT}$, + t_R in [Figure 3](#)) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

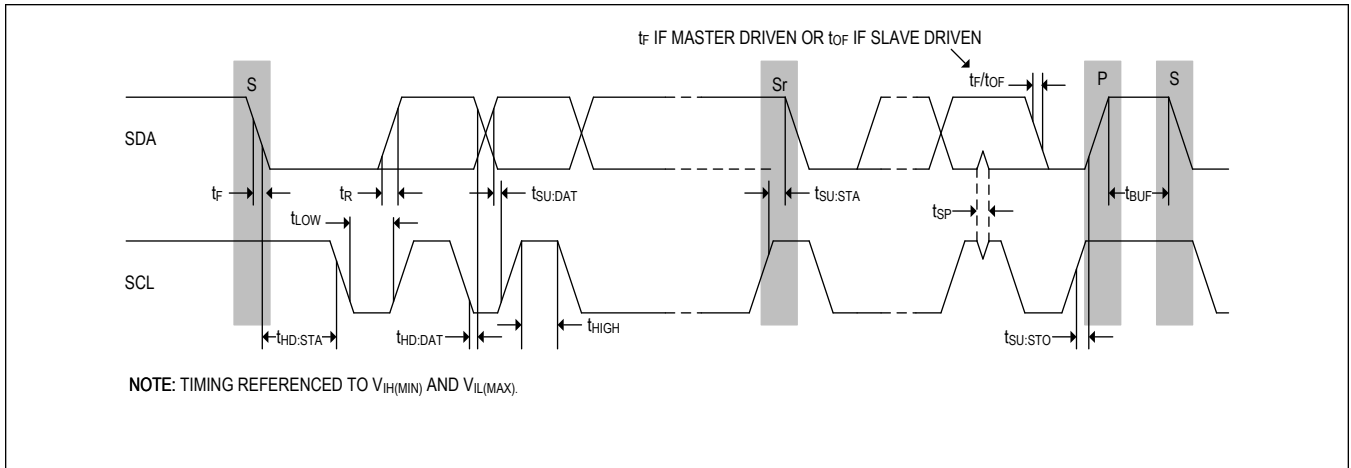
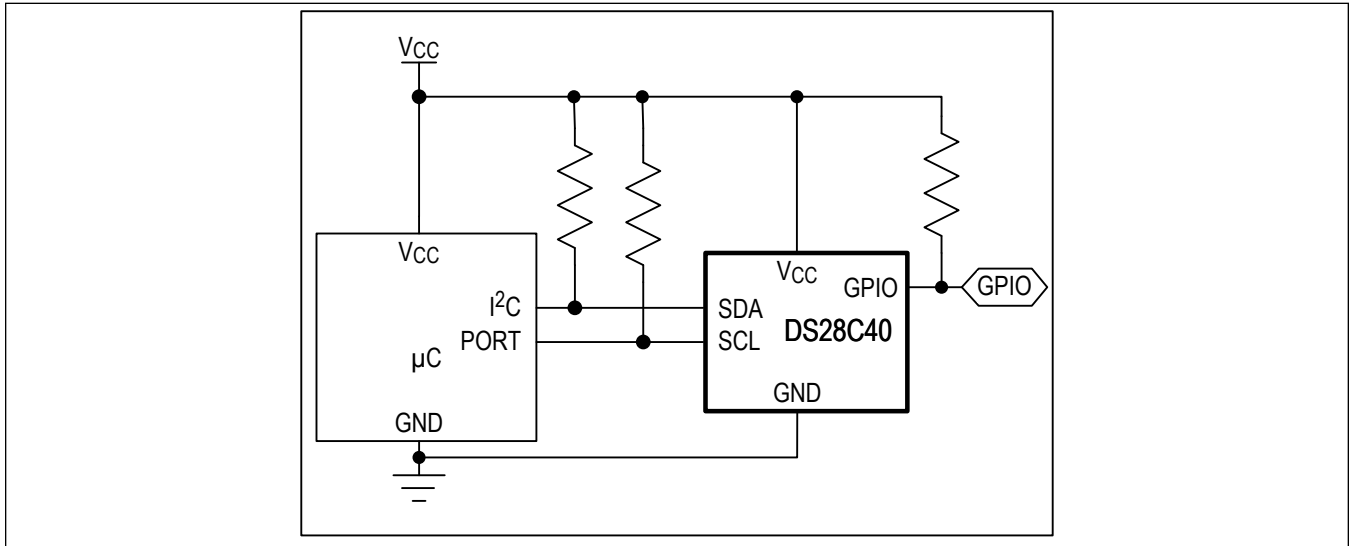


Figure 3. I²C Timing Diagram

Typical Application Circuit



Ordering Information

| PART NUMBER | TEMP RANGE | PIN-PACKAGE |
|--------------|-----------------|---------------------------------|
| DS28C40G/V+T | -40°C to +125°C | 10 TDFN T1034+2 (2.5k pcs reel) |
| DS28C40G/V+U | -40°C to +125°C | 10 TDFN T1034+2 |

+Denotes a lead(Pb)-free/RoHS-compliant package.

/V = Denotes an automotive qualified part.

T = Tape and reel.

U = Cut tape.

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|-----------------|---------------|
| 0 | 5/19 | Initial release | — |

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