# 0.5 AND 2.5 AMP ISODRIVERS WITH OPTO INPUT (2.5, 3.75, AND 5.0 $kV_{RMS}$)

## Features

- Functional upgrade for HCPL-0302, HCPL-3120, TLP350, and similar opto-drivers
- 60 ns propagation delay max (independent of input drive current)
- 14x tighter part-to-part matching versus opto-drivers
- 2.5, 3.75, and 5.0 $kV_{RMS}$ isolation
- Transient Immunity
  - 30 kV/µs
- Under-voltage lockout protection with hysteresis
- Resistant to temperature and aging effects
- Gate driver supply voltage
  - 6.5 V to 24 V
- AEC-Q100 qualification
- Wide operating range
  - –40 to +125 °C
- RoHS-compliant packages
  - SOIC-8 narrow body
  - SOIC-16 wide body

## Applications

- IGBT/ MOSFET gate drives
- Industrial control systems
- Switch mode power supplies
- UPS systems
- Motor control drives
- Inverters

## Safety Regulatory Approvals

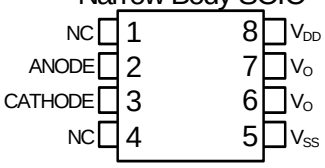
- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
  - IEC 60747-5-5 (VDE 0884 Part 5)
  - EN 60950-1 (reinforced insulation)
- CQC certification approval
  - GB4943.1

## Description

The Si8220/21 is a high-performance functional upgrade for opto-coupled drivers, such as the HCPL-3120 and the HPCL-0302 providing 2.5 A of peak output current. It utilizes Silicon Laboratories' proprietary silicon isolation technology, which provides a choice of 2.5, 3.75, or 5.0 $kV_{RMS}$ withstand voltages per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to opto-isolated drivers. While the input circuit mimics the characteristics of an LED, less drive current is required, resulting in increased efficiency. Propagation delay time is independent of input drive current, resulting in consistently short propagation time, tighter unit-to-unit variation, and greater input circuit design flexibility.

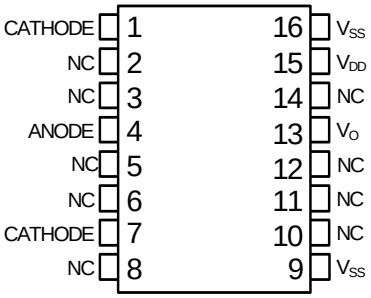
**Pin Assignments:**
**See page 20**

Narrow Body SOIC




Top View

Wide Body SOIC




Top View

Patent pending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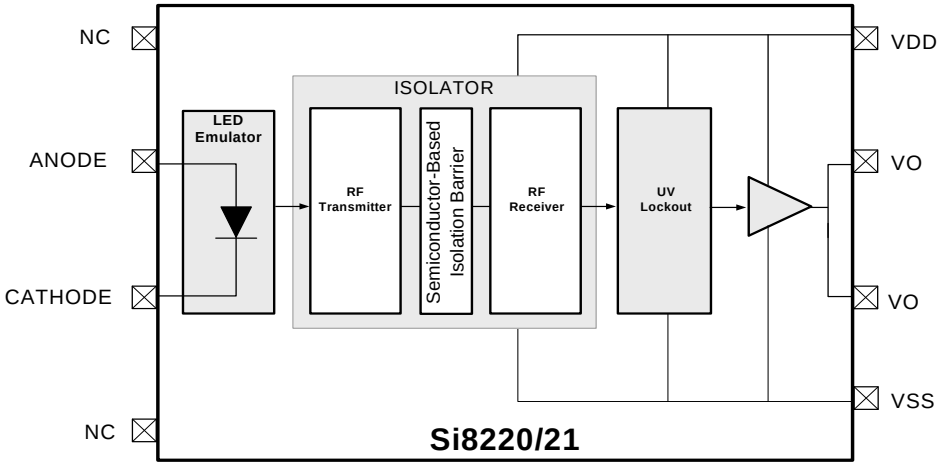
## Functional Block Diagram



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# 1. Electrical Specifications

### Table 1. Electrical Characteristics [1]

$V_{DD}$ = 12 V or 15 V, $V_{SS}$ = GND, $T_A$ = –40 to +125 °C; typical specs at 25 °C.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DC Specifications** | | | | | | |
| Power Supply Voltage | $V_{DD}$ | ($V_{DD}$ – $V_{SS}$) | 6.5 | — | 24 | V |
| Input Current (ON) | $I_{F(ON)}$ | | 5.0 | — | 20 | mA |
| Input Current Rising Edge Hysteresis | $I_{HYS}$ | | — | 0.5 | — | mA |
| Input Voltage (OFF) | $V_{F(OFF)}$ | Measured at ANODE with respect to CATHODE. | –0.6 | — | 1.6 | V |
| Input Forward Voltage | $V_F$ | Measured at ANODE with respect to CATHODE. $I_F$ = 5 mA. | 1.7 | — | 2.5 | V |
| Output Resistance High (Source) | $R_{OH}$ | 0.5 A devices | — | 15 | — | Ω |
| | | 2.5 A devices | — | 2.7 | — | |
| Output Resistance Low (Sink) | $R_{OL}$ | 0.5 A devices | — | 5.0 | — | |
| | | 2.5 A devices | — | 1.0 | — | |
| Output High Current (Source) | $I_{OH}$ | (0.5 A), $I_F$ = 0 (see Figure 2) | — | 0.3 | — | A |
| | | (2.5 A), $I_F$ = 0 (see Figure 2) | — | 1.5 | — | |
| Output Low Current (Sink) | $I_{OL}$ | (0.5 A), $I_F$ = 10 mA, (see Figure 1) | — | 0.5 | — | A |
| | | (2.5 A), $I_F$ = 10 mA, (see Figure 1) | — | 2.5 | — | |
| High-Level Output Voltage | $V_{OH}$ | (0.5 A), $I_{OUT}$ = –50 mA | — | $V_{DD}$– 0.5 | — | V |
| | | (2.5 A), $I_{OUT}$ = –50 mA | | $V_{DD}$– 0.1 | | |
| Low-Level Output Voltage | $V_{OL}$ | (0.5 A), $I_{OUT}$ = 50 mA | — | 200 | — | mV |
| | | (2.5 A), $I_{OUT}$ = 50 mA | | 50 | | |
| High-Level Supply Current | | Output open $I_F$ = 10 mA | — | 1.2 | — | mA |
| Low-Level Supply Current | | Output open $V_F$ = –0.6 to +1.6 V | — | 1.4 | — | mA |

**Notes:**
1. VDD = 12 V for 5, 8, and 10 V UVLO devices; VDD = 15 V for 12.5 V UVLO devices.
2. See "9.Ordering Guide" on page 22 for more information.

**Table 1. Electrical Characteristics (Continued)[1]**

$V_{DD}$ = 12 V or 15 V, $V_{SS}$ = GND, $T_A$ = –40 to +125 °C; typical specs at 25 °C.

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Input Reverse Voltage | $BV_R$ | $I_R$ = 10 mA. Measured at ANODE with respect to CATHODE. | 0.5 | — | — | V |
| Input Capacitance | $C_{IN}$ | | — | 10 | — | pF |
| VDD Undervoltage Threshold[2] | $VDD_{UV+}$ | $V_{DD}$ rising | | | | |
| 5 V Threshold | | See Figure 9 on page 15. | 5.20 | 5.80 | 6.30 | V |
| 8 V Threshold | | See Figure 10 on page 15. | 7.50 | 8.60 | 9.40 | V |
| 10 V Threshold | | See Figure 11 on page 15. | 9.60 | 11.1 | 12.2 | V |
| 12.5 V Threshold | | See Figure 12 on page 15. | 12.4 | 13.8 | 14.8 | |
| VDD Undervoltage Threshold[2] | $VDD_{UV-}$ | $V_{DD}$ falling | | | | |
| 5 V Threshold | | See Figure 9 on page 15. | 4.90 | 5.52 | 6.0 | V |
| 8 V Threshold | | See Figure 10 on page 15. | 7.20 | 8.10 | 8.70 | V |
| 10 V Threshold | | See Figure 11 on page 15. | 9.40 | 10.1 | 10.9 | V |
| 12.5 V Threshold | | See Figure 12 on page 15. | 11.6 | 12.8 | 13.8 | |
| VDD Lockout Hysteresis | $VDD_{HYS}$ | UVLO voltage = 5 V | — | 280 | — | mV |
| VDD Lockout Hysteresis | $VDD_{HYS}$ | UVLO voltage = 8 V | — | 600 | — | mV |
| VDD Lockout Hysteresis | $VDD_{HYS}$ | UVLO voltage = 10 V or 12.5 V | — | 1000 | — | mV |
| **AC Specifications** | | | | | | |
| Propagation Delay Time to High Output Level | $t_{PLH}$ | $C_L$ = 200 pF | — | — | 60 | ns |
| Propagation Delay Time to Low Output Level | $t_{PHL}$ | $C_L$ = 200 pF | — | — | 40 | ns |
| Output Rise and Fall Time | $t_R$, $t_F$ | (0.5 A), $C_L$ = 200 pF | — | — | 30 | ns |
| | | (2.5 A), $C_L$ = 200 pF | — | — | 20 | |
| Device Startup Time | $t_{START}$ | Time from $V_{DD}$ = $V_{DD_UV+}$ to $V_O$ | — | — | 40 | µs |
| Common Mode Transient Immunity | CMTI | Input ON or OFF $V_{CM}$ = 1500 V (see Figure 3) | — | 30 | — | kV/µs |

**Notes:**
1. VDD = 12 V for 5, 8, and 10 V UVLO devices; VDD = 15 V for 12.5 V UVLO devices.
2. See "9.Ordering Guide" on page 22 for more information.

## 2. Test Circuits

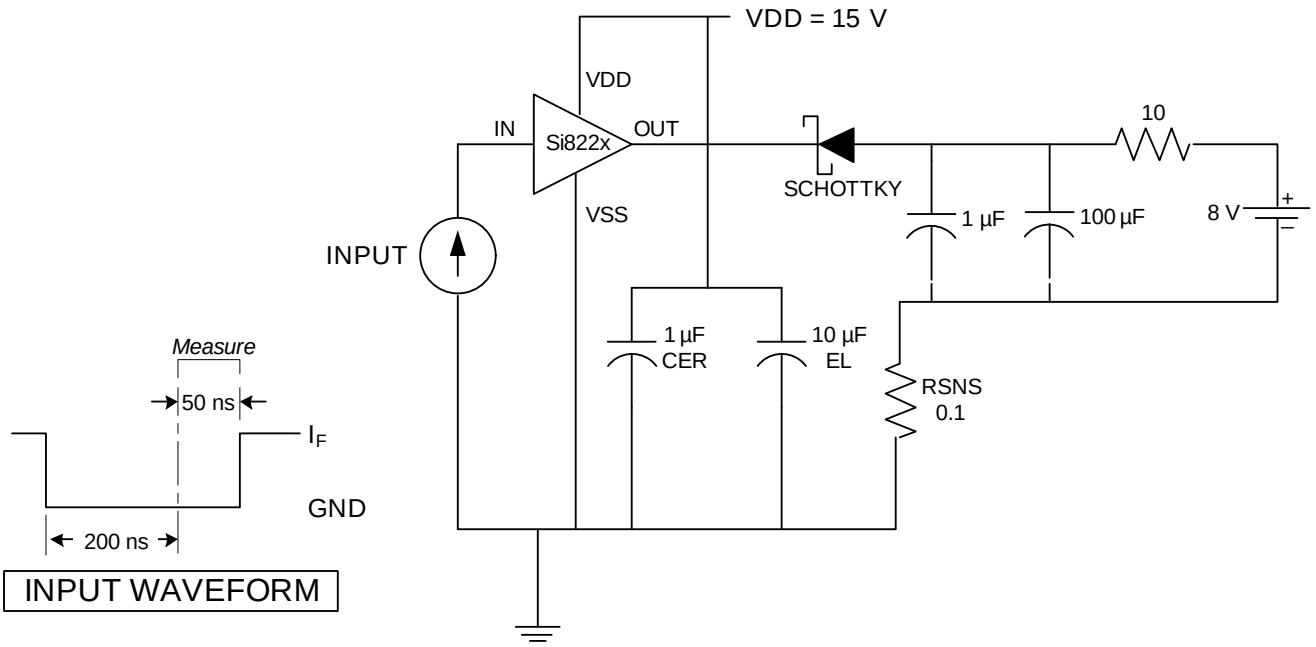



**Figure 1. IOL Sink Current Test Circuit**

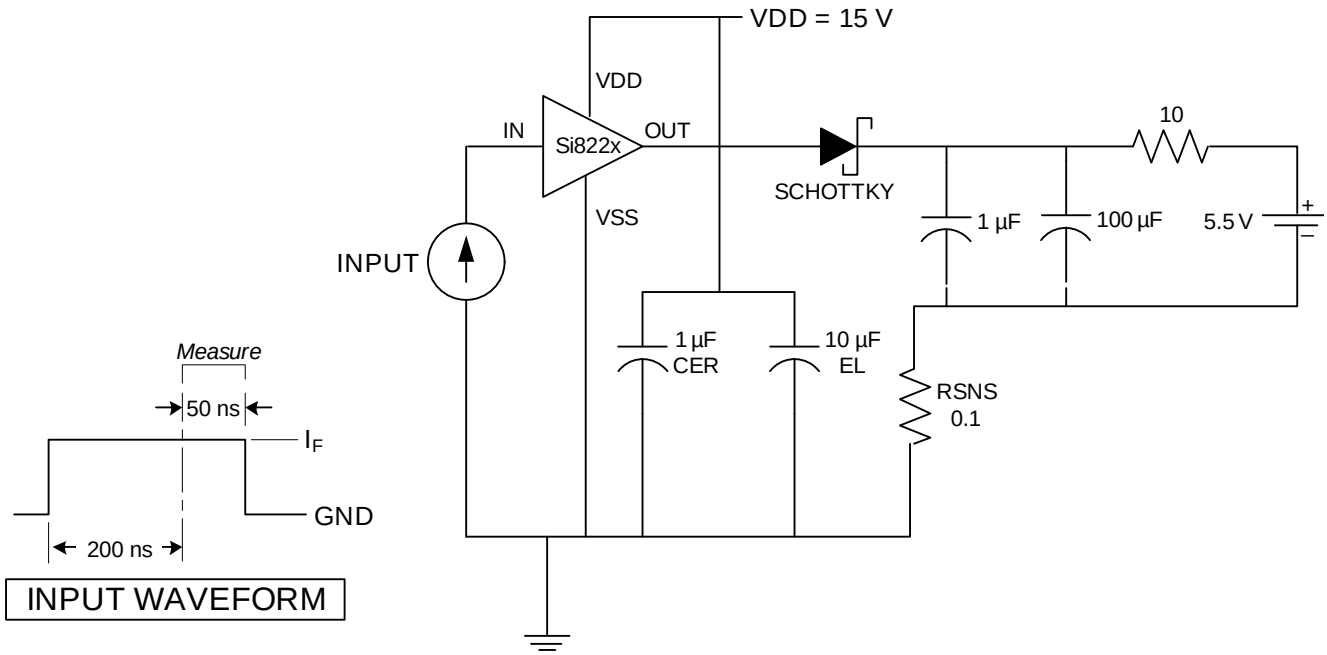



**Figure 2. IOH Source Current Test Circuit**

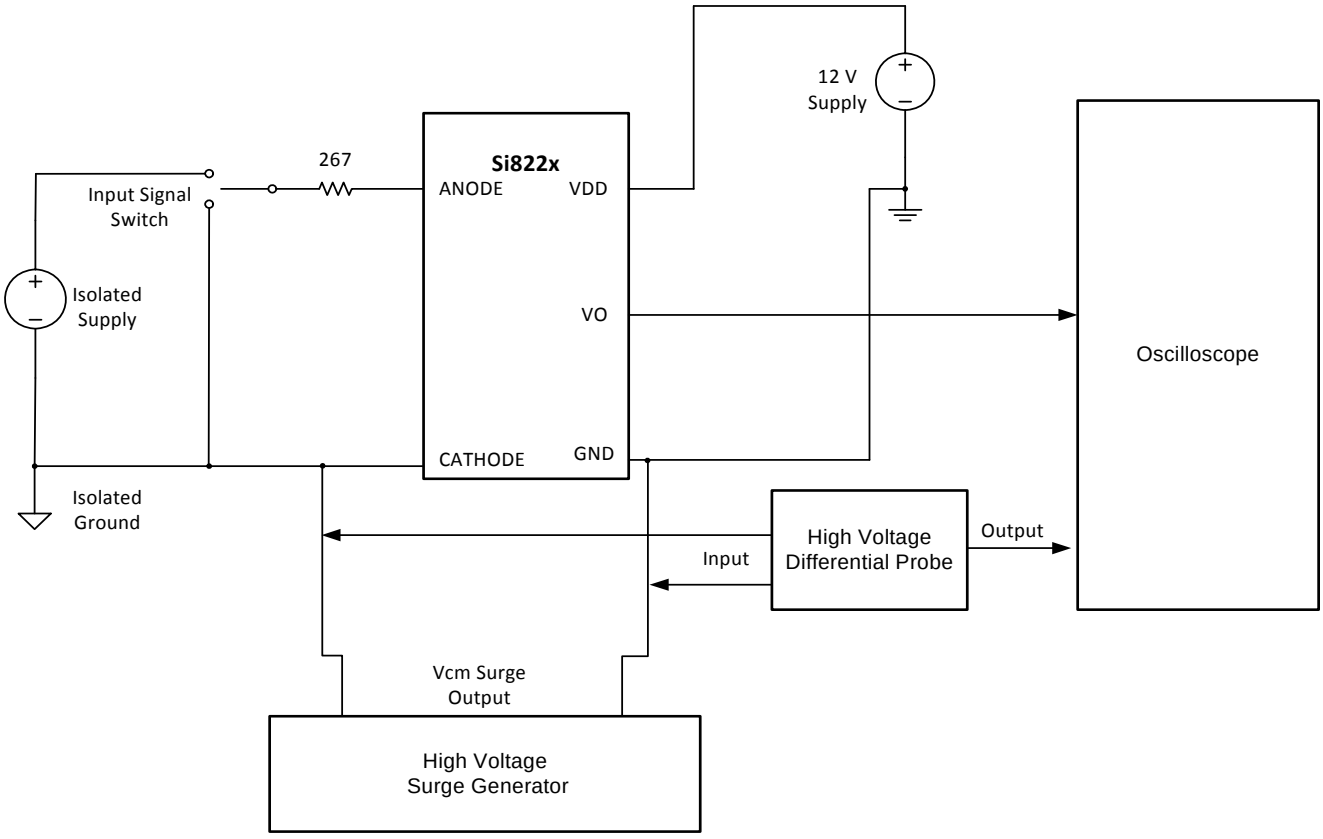



**Figure 3. Common Mode Transient Immunity Test Circuit**

## 3. Regulatory Information

**Table 2. Regulatory Information***

| |
|---|
| **CSA** |
| The Si822x is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873. |
| 61010-1: Up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 600 $V_{RMS}$ basic insulation working voltage. |
| 60950-1: Up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| 60601-1: Up to 125 $V_{RMS}$ reinforced insulation working voltage; up to 380 $V_{RMS}$ basic insulation working voltage. |
| **VDE** |
| The Si822x is certified according to IEC 60747-5-5. For more details, see File 5006301-4880-0001. |
| 60747-5-5: Up to 891 $V_{peak}$ for basic insulation working voltage. |
| 60950-1: Up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| **UL** |
| The Si822x is certified under UL1577 component recognition program. For more details, see File E257455. |
| Rated up to 5000 $V_{RMS}$ isolation voltage for basic protection. |
| **CQC** |
| The Si822x is certified under GB4943.1-2011. For more details, see certificates CQC13001096107 and CQC13001096109. |
| Rated up to 600 $V_{RMS}$ reinforced insulation working voltage; up to 1000 $V_{RMS}$ basic insulation working voltage. |
| ***Note:** Regulatory Certifications apply to 2.5 $kV_{RMS}$ rated devices which are production tested to 3.0 $kV_{RMS}$ for 1 sec. Regulatory Certifications apply to 3.75 $kV_{RMS}$ rated devices which are production tested to 4.5 $kV_{RMS}$ for 1 sec. Regulatory Certifications apply to 5.0 $kV_{RMS}$ rated devices which are production tested to 6.0 $kV_{RMS}$ for 1 sec. For more information, see "9.Ordering Guide" on page 22. |

**Table 3. Insulation and Safety-Related Specifications**

| Parameter | Symbol | Test Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | WB SOIC-16 | NB SOIC-8 | |
| Nominal Air Gap (Clearance)[1] | L(IO1) | | 8.0 min | 4.9 min | mm |
| Nominal External Tracking (Creepage)[1] | L(IO2) | | 8.0 min | 4.01 min | mm |
| Minimum Internal Gap (Internal Clearance) | | | 0.014 | 0.014 | mm |
| Tracking Resistance (Proof Tracking Index) | PTI | IEC60112 | 600 | 600 | V |
| Erosion Depth | ED | | 0.019 | 0.019 | mm |
| Resistance (Input-Output)[2] | $R_{IO}$ | | $10^{12}$ | $10^{12}$ | Ω |
| Capacitance (Input-Output)[2] | $C_{IO}$ | f = 1 MHz | 2.0 | 1.0 | pF |
| Input Capacitance[3] | $C_I$ | | 4.0 | 4.0 | pF |

**Notes:**

1. The values in this table correspond to the nominal creepage and clearance values as detailed in "12.Package Outline: 16-Pin Wide Body SOIC" on page 25, "10.Package Outline: 8-Pin Narrow Body SOIC" on page 23. VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC-16 package and 4.7 mm minimum for the NB SOIC-8 package. UL does not impose a clearance and creepage minimum for component level certifications. CSA certifies the clearance and creepage limits as 3.9 mm minimum for the NB SOIC-8 and 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si822x is converted into a 2-terminal device. Pins 1–8 (1–4, NB SOIC-8) are shorted together to form the first terminal and pins 9–16 (5–8, NB SOIC-8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.
3. Measured from input pin to ground.

**Table 4. IEC 60664-1 (VDE 0844 Part 5) Ratings**

| Parameter | Test Conditions | Specification | |
|---|---|---|---|
| | | NB SOIC8 | WB SOIC 16 |
| Basic Isolation Group | Material Group | I | I |
| Installation Classification | Rated Mains Voltages ≤ 150 $V_{RMS}$ | I-IV | I-IV |
| | Rated Mains Voltages ≤ 300 $V_{RMS}$ | I-III | I-IV |
| | Rated Mains Voltages ≤ 400 $V_{RMS}$ | I-II | I-III |
| | Rated Mains Voltages ≤ 600 $V_{RMS}$ | I-II | I-III |

**Table 5. IEC 60747-5-5 Insulation Characteristics for Si822xxC***

| Parameter | Symbol | Test Condition | Characteristic | | Unit |
|---|---|---|---|---|---|
| | | | WB SOIC-16 | NB SOIC-8 | |
| Maximum Working Insulation Voltage | $V_{IORM}$ | | 891 | 560 | V peak |
| Input to Output Test Voltage | $V_{PR}$ | Method b1 ($V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test, $t_m$ = 1 sec, Partial Discharge < 5 pC) | 1671 | 1050 | V peak |
| Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR}$ = 60 sec) | $V_{TR}$ | | 6000 | 4000 | V peak |
| Pollution Degree (DIN VDE 0110, Table 1) | | | 2 | 2 | |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | $R_S$ | | >$10^9$ | >$10^9$ | Ω |

***Note:** This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si822x provides a climate classification of 40/125/21.

**Table 6. IEC Safety Limiting Values[1]**

| Parameter | Symbol | Test Condition | Max | | Unit |
|---|---|---|---|---|---|
| | | | WB SOIC-16 | NB SOIC-8 | |
| Case Temperature | $T_S$ | | 150 | 150 | °C |
| Safety Input, Output, or Supply Current | $I_S$ | $\theta_{JA}$ = 140 °C/W (NB SOIC-8), 100 °C (WB SOIC-16), $V_I$ = 5.5 V, $T_J$ = 150 °C, $T_A$ = 25 °C | 50 | 40 | mA |
| Device Power Dissipation[2] | $P_D$ | | 1.2 | 1.2 | W |

**Notes:**
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 5 and 6.
2. The Si822x is tested with $V_O$ = 24 V, $T_J$ = 150 ºC, $C_L$ = 200 pF, input a 2 MHz 50% duty cycle square wave.

**Table 7. Thermal Characteristics**

| Parameter | Symbol | Typ | | Unit |
|---|---|---|---|---|
| | | WB SOIC-16 | NB SOIC-8 | |
| IC Junction-to-Air Thermal Resistance | $\theta_{JA}$ | 100 | 140 | ºC/W |

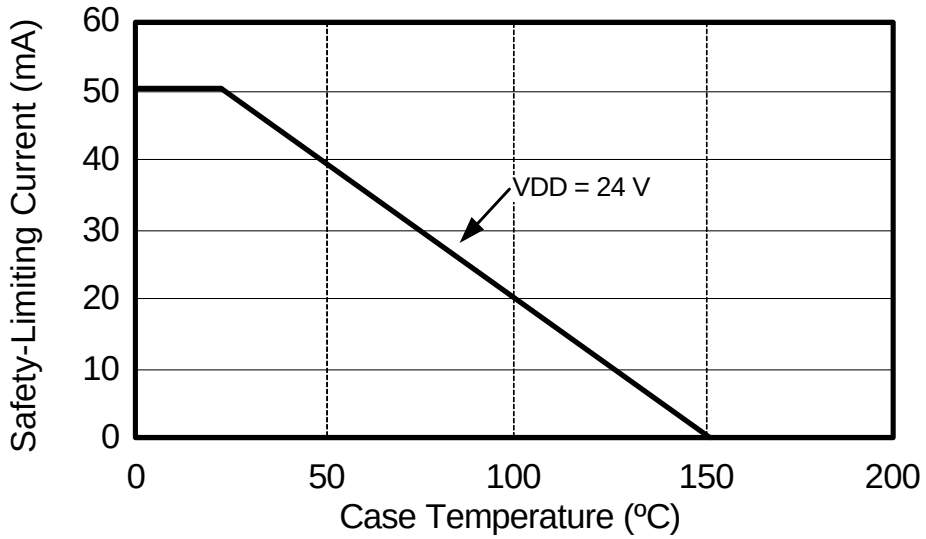



**Figure 4. (WB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-5**

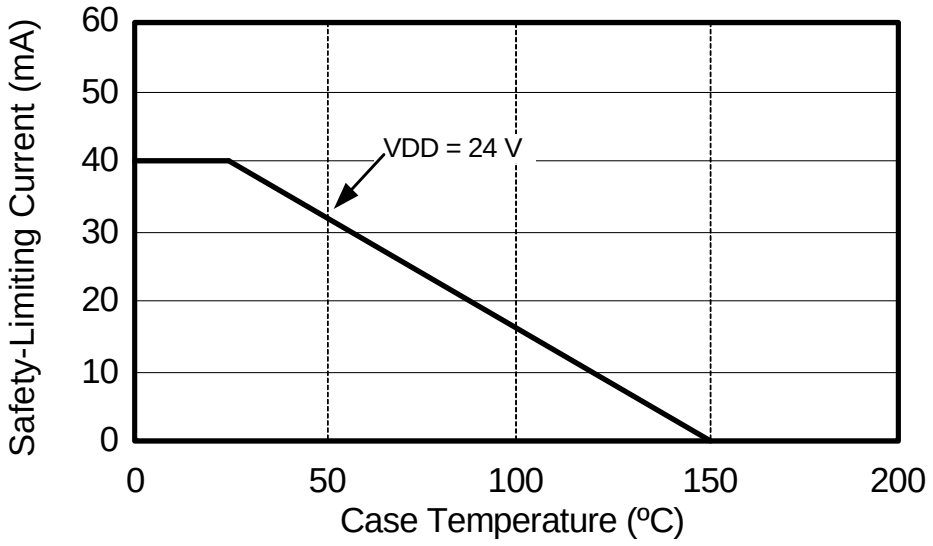



**Figure 5. (NB SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-5**

**Table 8. Absolute Maximum Ratings[1]**

| Parameter | Conditions | Min | Max | Units |
|---|---|---|---|---|
| Storage Temperature[2] | $T_{STG}$ | –65 | +150 | °C |
| Ambient Temperature under Bias | $T_A$ | –40 | +125 | °C |
| Junction Temperature | $T_J$ | — | 150 | °C |
| Input Current | $IF_{(AVG)}$ | –100 | 30 | mA |
| Driver-side Supply Voltage | $V_{DD}$ | –0.6 | 30 | V |
| Voltage on any output Pin with respect to Ground | $V_O$ | –0.5 | $V_{DD}$ + 0.5 | V |
| Peak Output Current ($t_{PW}$ = 10 µs, duty cycle = 0.2%) (0.5 Amp versions) | $I_{OPK}$ | — | 0.5 | A |
| Peak Output Current ($t_{PW}$ = 10 µs, duty cycle = 0.2%) (4.0 Amp versions) | $I_{OPK}$ | — | 4.0 | A |
| Lead Solder Temperature (10 s) | | — | 260 | °C |
| Maximum Isolation Voltage (1 s) NB SOIC-8 | | — | 4250 | $V_{RMS}$ |
| Maximum Isolation Voltage (1 s) WB SOIC-16 | | — | 6500 | $V_{RMS}$ |

**Notes:**
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.
2. VDE certifies storage temperature from –40 to 150 °C.

# 4. Functional Description

## 4.1. Theory of Operation

The Si8220/21 is a functional upgrade for popular opto-isolated drivers, such as the Avago HPCL-3120, HPCL-0302, Toshiba TLP350, and others. The operation of an Si8220/21 channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for the Si8220/21 is shown in Figure 6.

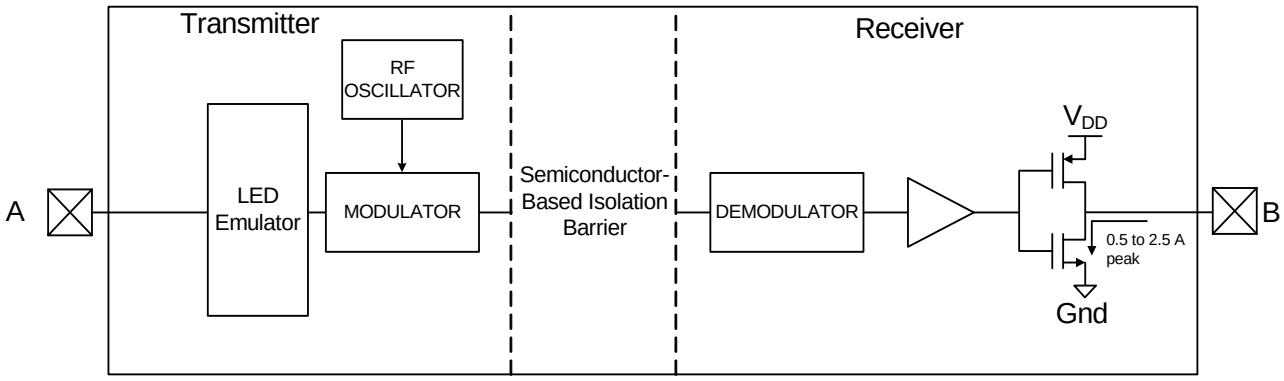



**Figure 6. Simplified Channel Diagram**

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 7 for more details.

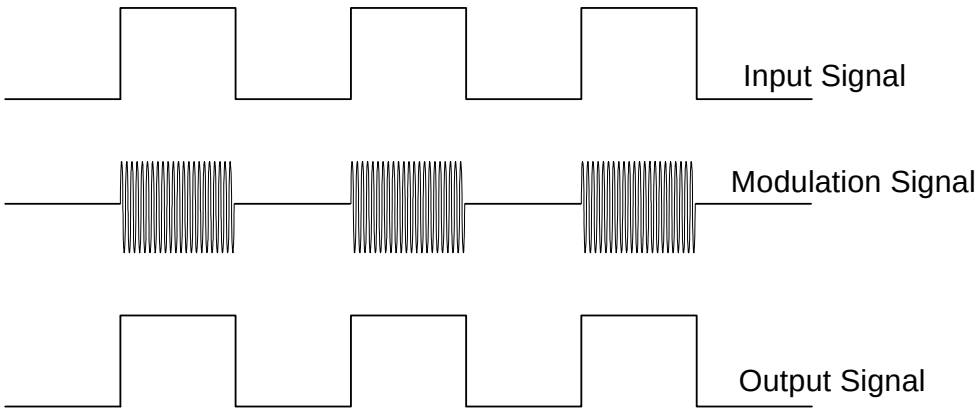



**Figure 7. Modulation Scheme**

# 5. Technical Description

## 5.1. Device Behavior

Truth tables for the Si8220/21 are summarized in Table 9.

**Table 9. Si8220/21 Truth Table Summary**

| Cathode | Anode | Diode Current ($I_F$) | $V_{DD}$ | VO | Comments |
|---|---|---|---|---|---|
| X | X | X | < UVLO | L | Device turned off |
| Hi-Z | X | 0 | > UVLO | L | Logic low state |
| X | Hi-Z | 0 | > UVLO | L | Logic low state |
| GND | GND | 0 | > UVLO | L | Logic low state |
| VF | VF | 0 | > UVLO | L | Logic low state |
| GND1 | VF | < $I_{F(OFF}$ | > UVLO | L | Logic low state |
| GND1 | VF | ≥ $I_{F(OFF)}$ | > UVLO | H | Logic high state |

**Note:** "X" = don't care. This truth table assumes VDD is powered. If VDD is below UVLO, see "5.3.Under Voltage Lockout (UVLO)" on page 15 for more information.

## 5.2. Device Startup

Output $V_O$ is held low during power-up until $V_{DD}$ rises above the UVLO+ threshold for a minimum time period of $t_{START}$. Following this, the output is high when the current flowing from anode to cathode is > $I_{F(ON)}$. Device startup, normal operation, and shutdown behavior is shown in Figure 8.

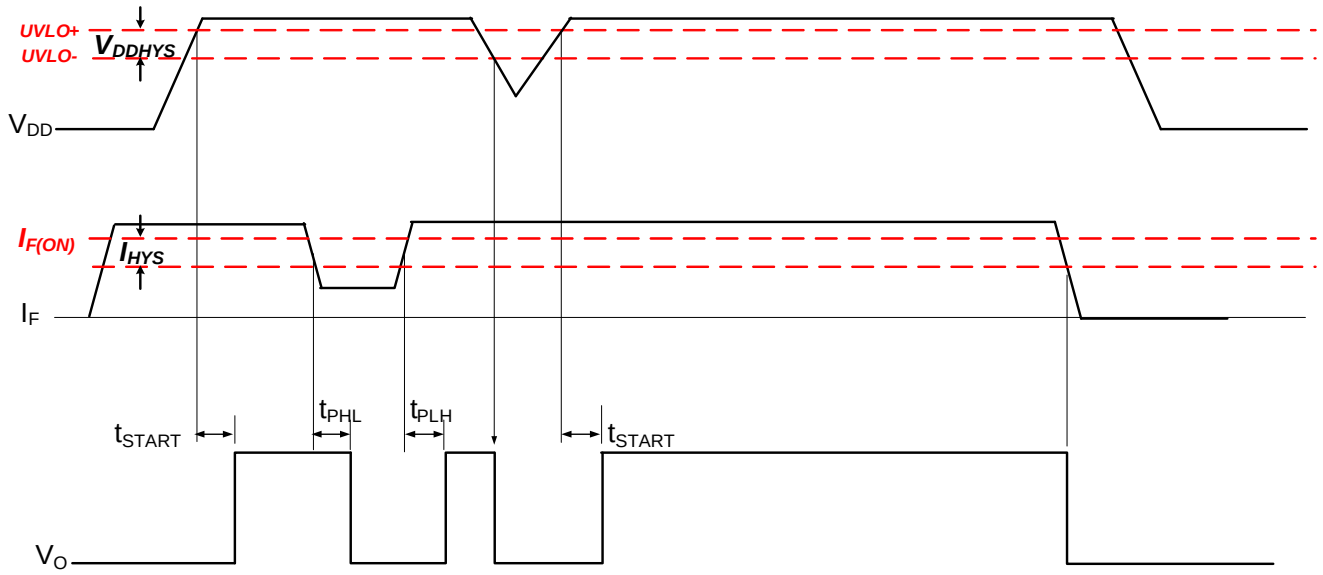



**Figure 8. Si8220/21 Operating Behavior ($I_F \geq I_{F(MIN)}$ when $V_F \geq V_{F(MIN)}$)**

## 5.3. Under Voltage Lockout (UVLO)

The UVLO circuit unconditionally drives $V_O$ low when $V_{DD}$ is below the lockout threshold. Referring to Figures 9 through 12, upon power up, the Si8220/21 is maintained in UVLO until VDD rises above $VDD_{UV+}$. During power down, the Si8220/21 enters UVLO when VDD falls below the UVLO threshold plus hysteresis (i.e., VDD $\leq$ $VDD_{UV+}$ – $VDD_{HYS}$).

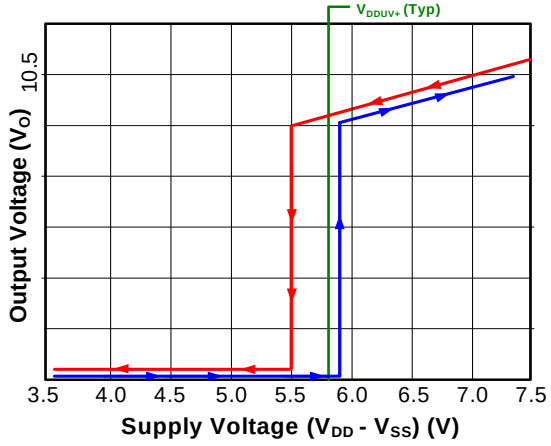



**Figure 9. Si8220/21 UVLO Response (5 V)**

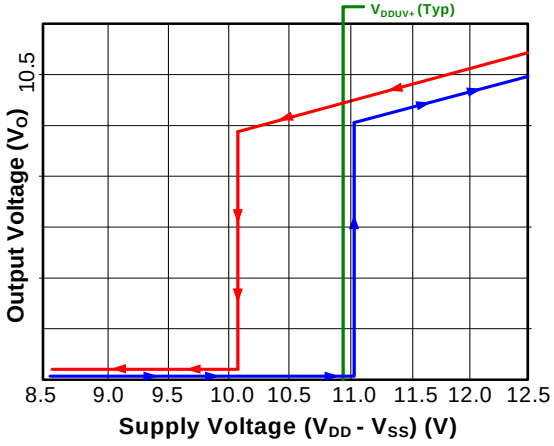



**Figure 11. Si8220/21 UVLO Response (10 V)**

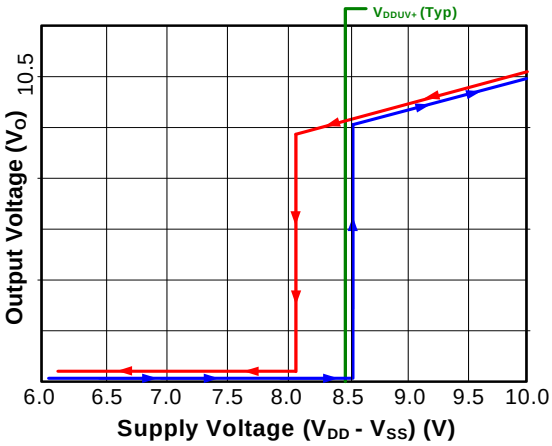



**Figure 10. Si8220/21 UVLO Response (8 V)**

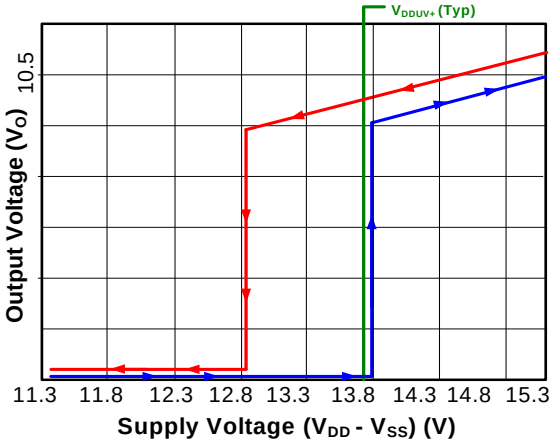



**Figure 12. Si8220/21 UVLO Response (12.5 V)**

# 6. Applications

## 6.1. Power Supply Connections

$V_{SS}$ can be biased at, above, or below ground as long as the voltage on $V_{DD}$ with respect to $V_{SS}$ is a maximum of 24 V. $V_{DD}$ decoupling capacitors should be placed as close to the package pins as possible. The optimum values for these capacitors depend on load current and the distance between the chip and its power source. It is recommended that 0.1 and 10 µF bypass capacitors be used to reduce high-frequency noise and maximize performance.

## 6.2. Layout Considerations

It is most important to minimize ringing in the drive path and noise on the $V_{DD}$ lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si8220/21 as close to the device it is driving as possible. In addition, the $V_{DD}$ supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and $V_{DD}$ planes for power devices and small signal components provides the best overall noise performance.

## 6.3. Power Dissipation Considerations

Proper system design must assure that the Si8220/21 operates within safe thermal limits across the entire load range. The Si8220/21 total power dissipation is the sum of the power dissipated by bias supply current, internal switching losses, and power delivered to the load, as shown in Equation 1.

$$P_D = (V_F)(I_F)(\text{Duty Cycle}) + (V_{DD})(I_{QOUT}) + (C_{int})(V_{DD}{}^2)(F) + (C_L)(V_{DD}{}^2)(F)$$

where:

$P_D$ is the total Si8220 device power dissipation (W)

$I_F$ is the diode current (20 mA max)

$V_F$ is the diode anode voltage (2.8 V max)

$I_{QOUT}$ is the driver maximum bias curent (5 mA)

$C_{int}$ is the internal parasitic capacitance (370 pF)

$V_{DD}$ is the driver-side supply voltage (24 V max)

F is the switching frequency (Hz)

**Equation 1.**

The maximum allowable power dissipation for the Si8220/21 is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2.

$$P_{Dmax} \leq \frac{T_{jmax} - T_A}{\theta_{ja}}$$

where:

$P_{Dmax}$ is the maximum allowable Si8220/21 power dissipation (W)

$T_{jmax}$ is the Si8220/21 maximum junction temperature (150 °C)

$T_A$ is the ambient temperature (°C)

$\theta_{ja}$ is the Si8220/21 package junction-to-air thermal resistance (125 °C/W)

**Equation 2.**

Substituting values for $P_{Dmax}$ $T_{jmax}$, $T_A$, and $\theta_{ja}$ into Equation 2 results in a maximum allowable total power dissipation of 1.0 W. The maximum allowable load is found by substituting this limit and the appropriate datasheet values from Table 1 on page 4 into Equation 1 and simplifying. The result is Equation 3, where $V_F$ = 2.8 V, $I_F$ = 10 mA, and $V_{DD}$ = 18 V.

$$C_{L(max)} = \frac{1.35 \times 10^{-3}}{F} - 1.85 \times 10^{-10}$$

where:

$C_{L(max)}$ is the maximum load (pF) allowable at switching frequency F

**Equation 3.**

A graph of Equation 3 is shown in Figure 13. Each point along the load line in this graph represents the package dissipation-limited value of $C_L$ for the corresponding switching frequency.

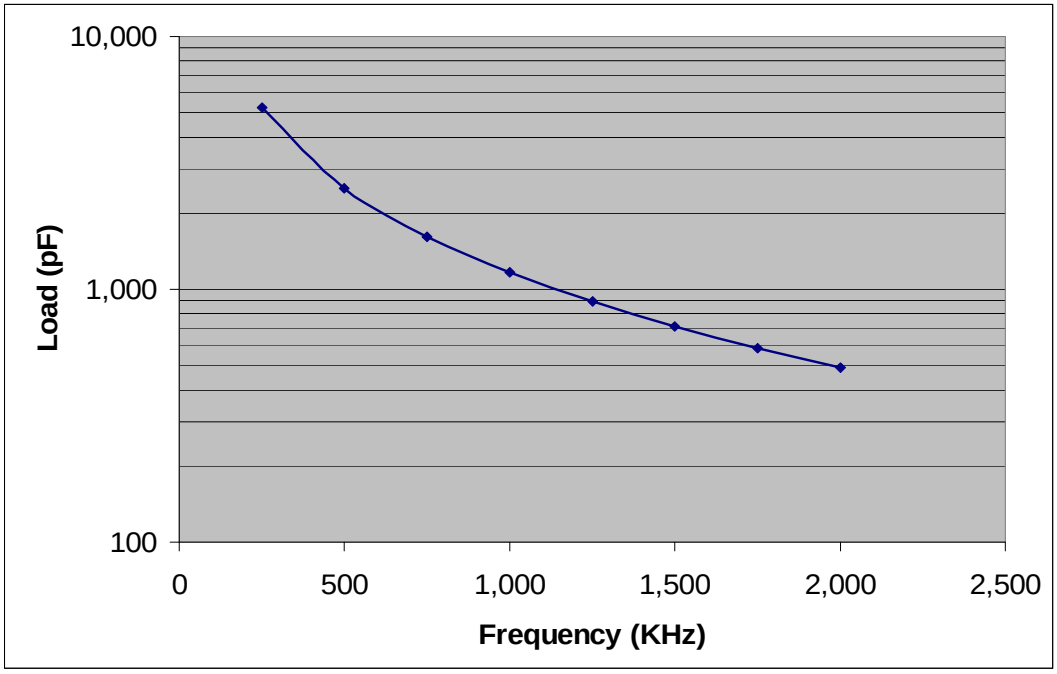



**Figure 13. Maximum Load vs. Switching Frequency**

## 6.4. Input Circuit Design

Opto driver manufacturers typically recommend the circuits shown in Figures 14 and 15. These circuits are specifically designed to improve opto-coupler input common-mode rejection and increase noise immunity.

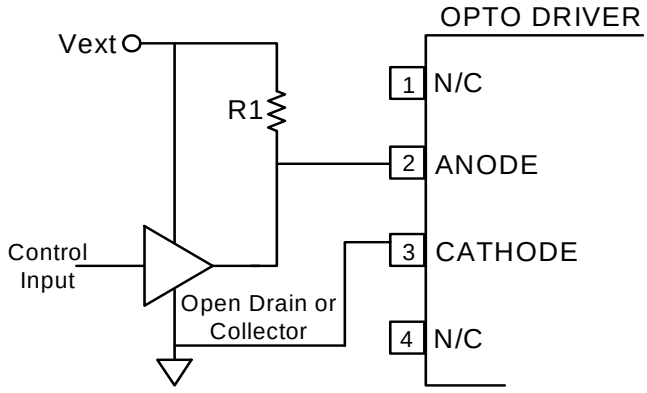



**Figure 14. Opto Driver Input Circuit**

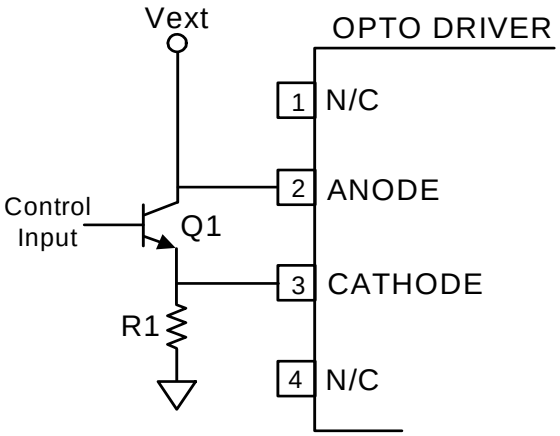



**Figure 15. High CMR Opto Driver Input Circuit**

The optically-coupled driver circuit of Figure 14 turns the LED on when the control input is high. However, internal capacitive coupling from the LED to the power and ground conductors can momentarily force the LED into its off state when the anode and cathode inputs are subjected to a high common-mode transient. The circuit shown in Figure 15 addresses this issue by using a value of R1 sufficiently low to overdrive the LED, ensuring it remains on during an input common-mode transient. Q1 shorts the LED off in the low output state, again increasing common-mode transient immunity. Some opto driver applications also recommend reverse-biasing the LED when the control input is off to prevent coupled noise from energizing the LED.

The Si8220/21 can be used with the input circuits shown in Figures 14 and 15; however, some applications will require increasing the value of R1 in order to limit $I_F$ to a maximum of 20 mA. The Si8220/21 propagation delay and output drive do not change for values of $I_F$ between $I_{F(MIN)}$ and $I_{F(MAX)}$. New designs should consider the input circuit configurations of Figure 16, which are more efficient than those of Figures 14 and 15. As shown, S1 represents any suitable switch, such as a BJT or MOSFET, analog transmission gate, processor I/O, etc. Also, note that the Si8220/21 input can be driven from the I/O port of any MCU or FPGA capable of sourcing a minimum of 5 mA (see Figure 16C).

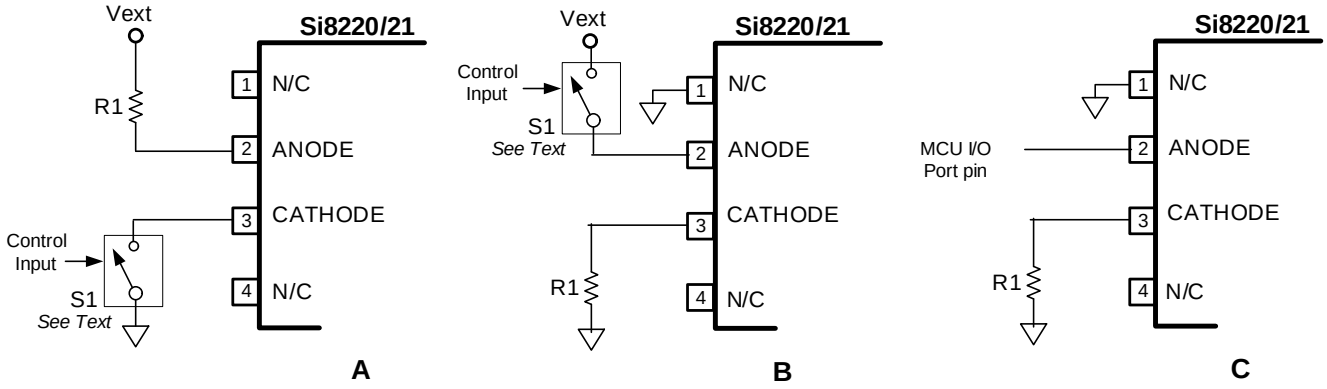



**Figure 16. Si8220/21 Other Input Circuit Configurations**

## 6.5. Parametric Differences between Si8220/21 and HCPL-0302 and HCPL-3120 Opto Drivers

The Si8220/21 is designed to directly replace HCPL-3120 and similar opto drivers. Parametric differences are summarized in Table 10 below.

**Table 10. Parametric Differences of Si8220 vs. HCPL-3120**

| Parameter | Si8220 | HCPL-3120 | Units |
|---|---|---|---|
| Max supply voltage | 24 | 30 | V |
| ON state forward input current | 5 to 20 | 7 to 16 | mA |
| OFF state input voltage | –0.6 to +1.6 | –0.3 to +0.8 | V |
| Max reverse input voltage | 0.5 | –5 | V |
| UVLO threshold (rising) | 5.8 to 13.8 | 11.0 to 13.5 | V |
| UVLO threshold (falling) | 5.5 to 12.8 | 9.7 to 12.0 | V |
| UVLO hysteresis | 0.28 to 1 | 1.6 | V |
| Rise/fall time into 10 Ω in series with 10 nF | 20 | 100 | ns |

**Table 11. Parametric Differences of Si8221 vs. HCPL-0302**

| Parameter | Si8221 | HCPL-0302 | Units |
|---|---|---|---|
| Max supply voltage | 24 | 30 | V |
| ON state forward input current | 5 to 20 | 7 to 16 | mA |
| OFF state input voltage | –0.6 to +1.6 | –0.3 to +0.8 | V |
| Max reverse input voltage | 0.5 | –5 | V |
| UVLO threshold (rising) | 5.8 to 13.8 | 11.0 to 13.5 | V |
| UVLO threshold (falling) | 5.5 to 12.8 | 9.7 to 12.0 | V |
| UVLO hysteresis | 0.28 to 1 | 1.6 | V |
| Rise/fall time into 10 Ω in series with 10 nF | 20 | 100 | ns |

### 6.5.1. Supply Voltage and UVLO

The supply voltage of the Si8220/21 is limited to 24 V, and the UVLO voltage thresholds are scaled accordingly. Opto replacement applications should limit their supply voltages to 24 V or less.

### 6.5.2. Input Diode Differences

The Si8220/21 input circuit requires less current and has twice the off-state noise margin compared to opto drivers. However, high CMR opto driver designs that overdrive the LED (see Figure 15) may require increasing the value of R1 to limit input current to 20 mA max. In addition, there is no benefit in driving the Si8220/21 input diode into reverse bias when in the off state. Consequently, opto driver circuits using this technique should either leave the negative bias circuitry unpopulated or modify the circuitry (e.g. add a clamp diode) to ensure that the anode pin of the Si8220/21 is no more than –0.8 V with respect to the cathode when reverse-biased.

## 7. Pin Descriptions (Narrow-Body SOIC)

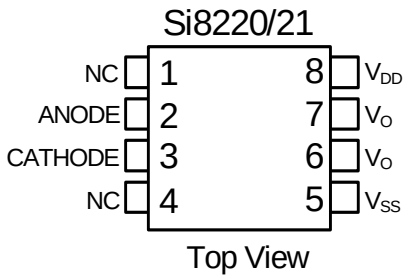



**Figure 17. Pin Configuration**

**Table 12. Pin Descriptions (Narrow-Body SOIC)**

| Pin | Name | Description |
|---|---|---|
| 1 | NC | No connect. |
| 2 | ANODE | Anode of LED emulator. $V_O$ follows the signal applied to this input with respect to the CATHODE input. |
| 3 | CATHODE | Cathode of LED emulator. $V_O$ follows the signal applied to ANODE with respect to this input. |
| 4 | NC | No connect. |
| 5 | $V_{SS}$ | External MOSFET source connection and ground reference for $V_{DD}$. This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 6 | $V_O$ | Output signal. Pins 6 and 7 are connected together internally. |
| 7 | $V_O$ | Output signal. Pins 6 and 7 are connected together internally. |
| 8 | $V_{DD}$ | Output-side power supply input referenced to $V_{SS}$ (24 V max). |
| ***Note:** No Connect. These pins are not internally connected. | | |

## 8. Pin Descriptions (Wide-Body SOIC)

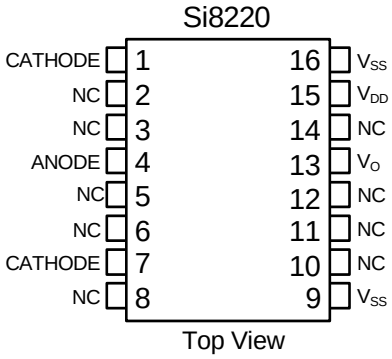



**Table 13. Pin Descriptions (Wide-Body SOIC)**

| Pin | Name | Description |
|---|---|---|
| 1,7 | CATHODE | Cathode of LED emulator. $V_O$ follows the signal applied to ANODE with respect to this input. |
| 2,3,5,6,8, 10,11,12, 14 | NC* | No connect. |
| 4 | ANODE | Anode of LED emulator. $V_O$ follows the signal applied to this input with respect to the CATHODE input. |
| 9,16 | $V_{SS}$ | External MOSFET source connection and ground reference for $V_{DD}$. This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 13 | $V_O$ | Output signal. |
| 15 | $V_{DD}$ | Output-side power supply input referenced to $V_{SS}$ (24 V max). |
| ***Note:** No Connect. These pins are not internally connected. | | |

## 9. Ordering Guide

**Table 14. Si8220/21 Ordering Guide***

| New Ordering Part Number (OPN) | Ordering Options | | | | | |
|---|---|---|---|---|---|---|
| | Input Configuration | Peak Output Current (Cross Reference) | UVLO Voltage | Insulation Rating | Temp Range | Pkg Type |
| Si8220BB-D-IS | Opto input | 2.5 A (HCPL-3120) | 8 V default | 2.5 kVrms | –40 to +125 °C | SOIC-8 |
| Si8220CB-D-IS | Opto input | 2.5 A (HCPL-3120) | 10 V | 2.5 kVrms | –40 to +125 °C | SOIC-8 |
| Si8220DB-D-IS | Opto input | 2.5 A (HCPL-3120) | 12.5 V | 2.5 kVrms | –40 to +125 °C | SOIC-8 |
| Si8220BD-D-IS | Opto input | 2.5 A (HCPL-3120) | 8 V default | 5.0 kVrms | –40 to +125 °C | WB SOIC-16 |
| Si8220CD-D-IS | Opto input | 2.5 A (HCPL-3120) | 10 V | 5.0 kVrms | –40 to +125 °C | WB SOIC-16 |
| Si8220DD-D-IS | Opto input | 2.5 A (HCPL-3120) | 12.5 V | 5.0 kVrms | –40 to +125 °C | WB SOIC-16 |
| Si8221CC-D-IS | Opto input | 0.5 A (HCPL-0302) | 10 V | 3.75 kVrms | –40 to +125 °C | SOIC-8 |
| Si8221DC-D-IS | Opto input | 0.5 A (HCPL-0302) | 12.5 V | 3.75 kVrms | –40 to +125 °C | SOIC-8 |

***Note:** All packages are RoHS-compliant with peak reflow temperatures of 260 °C according to the JEDEC industry standard classifications and peak solder temperatures.
All devices are AEC-Q100 qualified.
“Si” and “SI” are used interchangeably.

## 10. Package Outline: 8-Pin Narrow Body SOIC

Figure 18 illustrates the package details for the Si822x. Table 15 lists the values for the dimensions shown in the illustration.

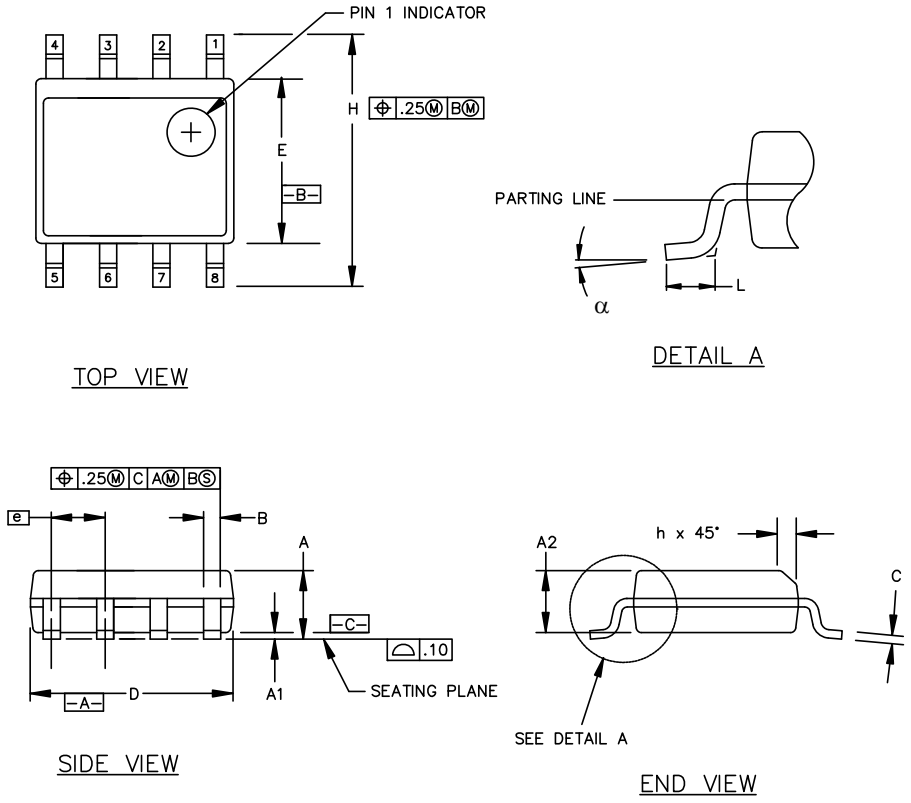



**Figure 18. 8-pin Small Outline Integrated Circuit (SOIC) Package**

**Table 15. Package Diagram Dimensions**

| Symbol | Millimeters | |
|---|---|---|
| | Min | Max |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.40 REF | 1.55 REF |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| ∝ | 0° | 8° |

## 11. Land Pattern: 8-Pin Narrow Body SOIC

Figure 19 illustrates the recommended land pattern details for the Si822x in an 8-pin narrow-body SOIC. Table 16 lists the values for the dimensions shown in the illustration.

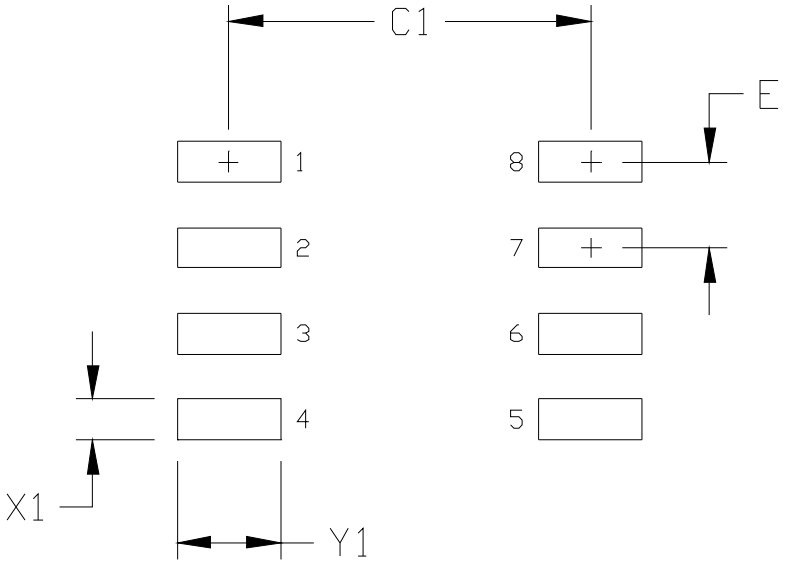



**Figure 19. PCB Land Pattern: 8-Pin Narrow Body SOIC**

**Table 16. PCM Land Pattern Dimensions (8-Pin Narrow Body SOIC)**

| Dimension | Feature | (mm) |
|---|---|---|
| C1 | Pad Column Spacing | 5.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.55 |

**Notes:**
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 12. Package Outline: 16-Pin Wide Body SOIC

Figure 20 illustrates the package details for the Si822x Digital Isolator. Table 17 lists the values for the dimensions shown in the illustration.

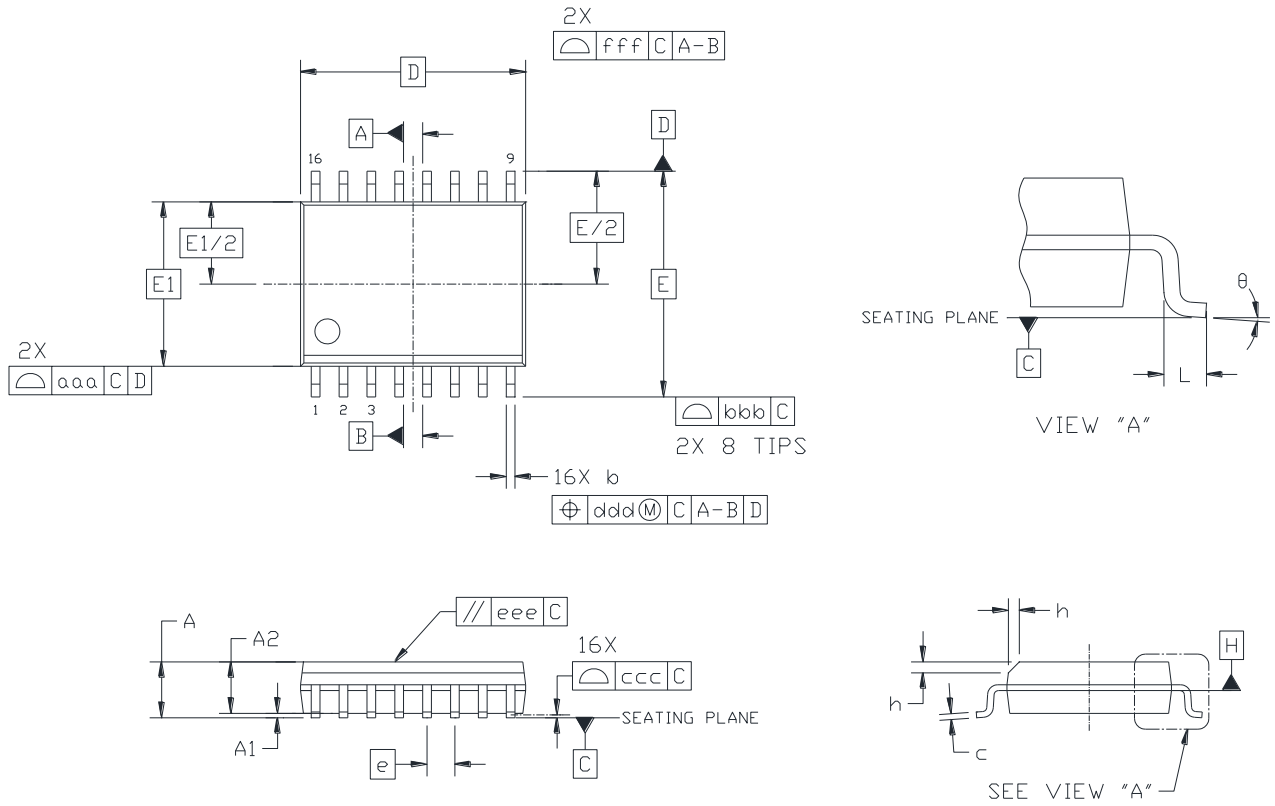



**Figure 20. 16-Pin Wide Body SOIC**

**Table 17. Package Diagram Dimensions**

| Dimension | Min | Max |
|---|---|---|
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| A2 | 2.05 | — |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 10.30 BSC | |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| h | 0.25 | 0.75 |
| θ | 0° | 8° |
| aaa | — | 0.10 |
| bbb | — | 0.33 |
| ccc | — | 0.10 |
| ddd | — | 0.25 |
| eee | — | 0.10 |
| fff | — | 0.20 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

## 13. Land Pattern: 16-Pin Wide-Body SOIC

Figure 21 illustrates the recommended land pattern details for the Si822x in a 16-pin wide-body SOIC. Table 18 lists the values for the dimensions shown in the illustration.

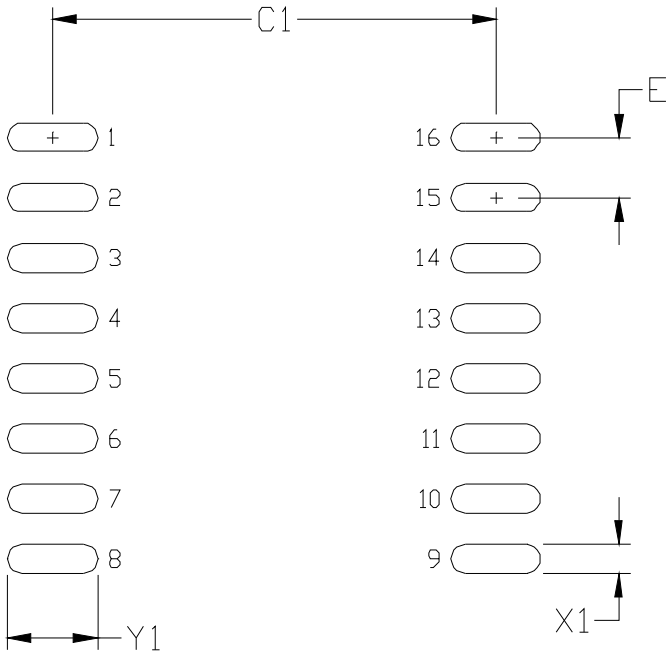



**Figure 21. 16-Pin SOIC Land Pattern**

**Table 18. 16-Pin Wide Body SOIC Land Pattern Dimensions**

| Dimension | Feature | (mm) |
|---|---|---|
| C1 | Pad Column Spacing | 9.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.90 |

**Notes:**
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

## 14. Top Marking: 16-Pin Wide Body SOIC

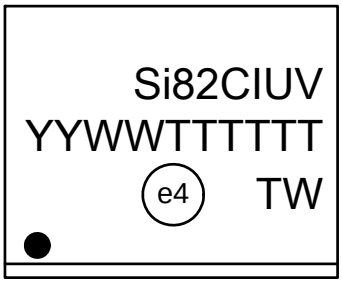



**Figure 22. 16-Pin Wide Body SOIC Top Marking**

**Table 19. 16-Pin Wide Body SOIC Top Marking Explanation**

| | | |
|---|---|---|
| **Line 1 Marking:** | Base Part Number<br>Ordering Options<br>See Ordering Guide for more information. | Si82 = ISOdriver product series<br>C = Input configuration<br>2 = Opto input type<br>I = Peak output current<br>0 = 2.5A; 1 = 0.5A<br>U = UVLO level<br>A = 5 V; B = 8 V; C = 10 V; D = 12.5 V<br>V = Isolation rating<br>A = 1 kV; B = 2.5 kV; C = 3.75 kV<br>D = 5.0 kV |
| **Line 2 Marking:** | YY = Year<br>WW = Workweek | Assigned by the Assembly House. Corresponds to the year and workweek of the mold date. |
| | TTTTTT = Mfg Code | Manufacturing Code from Assembly Purchase Order form. |
| **Line 3 Marking:** | Circle = 1.5 mm Diameter (Center Justified) | "e4" Pb-Free Symbol |
| | Country of Origin<br>ISO Code Abbreviation | TW = Taiwan |

## 15. Top Marking: 8-Pin Narrow Body SOIC

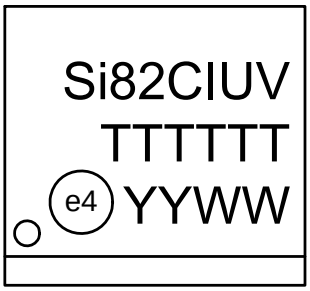



**Figure 23. 8-Pin Narrow Body SOIC Top Marking**

**Table 20. 8-Pin Narrow Body SOIC Top Marking Explanations**

| | | |
|---|---|---|
| **Line 1 Marking:** | Base Part Number<br>Ordering Options<br>(See Ordering Guide for more information) | Si82 = ISOdriver product series<br>C = Input configuration<br>2 = Opto input type<br>I = Peak output current<br>0 = 2.5 A; 1 = 0.5 A<br>U = UVLO level<br>A = 5 V; B = 8 V; C = 10 V; D = 12.5 V<br>V = Isolation rating<br>A = 1 = kV; B = 2.5 = kV; C = 3.75 kV<br>D = 5.0 kV |
| **Line 2 Marking:** | TTTTTT | Manufacturing date code assigned by assembly contractor. |
| **Line 3 Marking:** | Circle = 1.1 mm Diameter<br>Left-Justified | "e4" Pb-Free Symbol |

# Document Change List

## Revision 0.22 to Revision 1.0

- Updated Tables 2, 3, 4, and 5.
- Updated “9. Ordering Guide” .
- Added Device Marking sections.

## Revision 1.0 to Revision 1.1

- Updated Table 5 on page 10.
- Updated Table 8 on page 12.
- Removed introductory text and Figure 17.
- Changed all packages to MSL2A in "9.Ordering Guide" on page 22.
- Updated "12.Package Outline: 16-Pin Wide Body SOIC" on page 25.

## Revision 1.1 to Revision 1.2

- Updated CMTI spec in Table 1 on page 4.
- Updated Figure 1 on page 6.
- Updated Figure 2 on page 6.
- Added Figure 3 on page 7.
- Updated Table 5 on page 10.
- Added note to Table 14 on page 22.

## Revision 1.2 to Revision 1.3

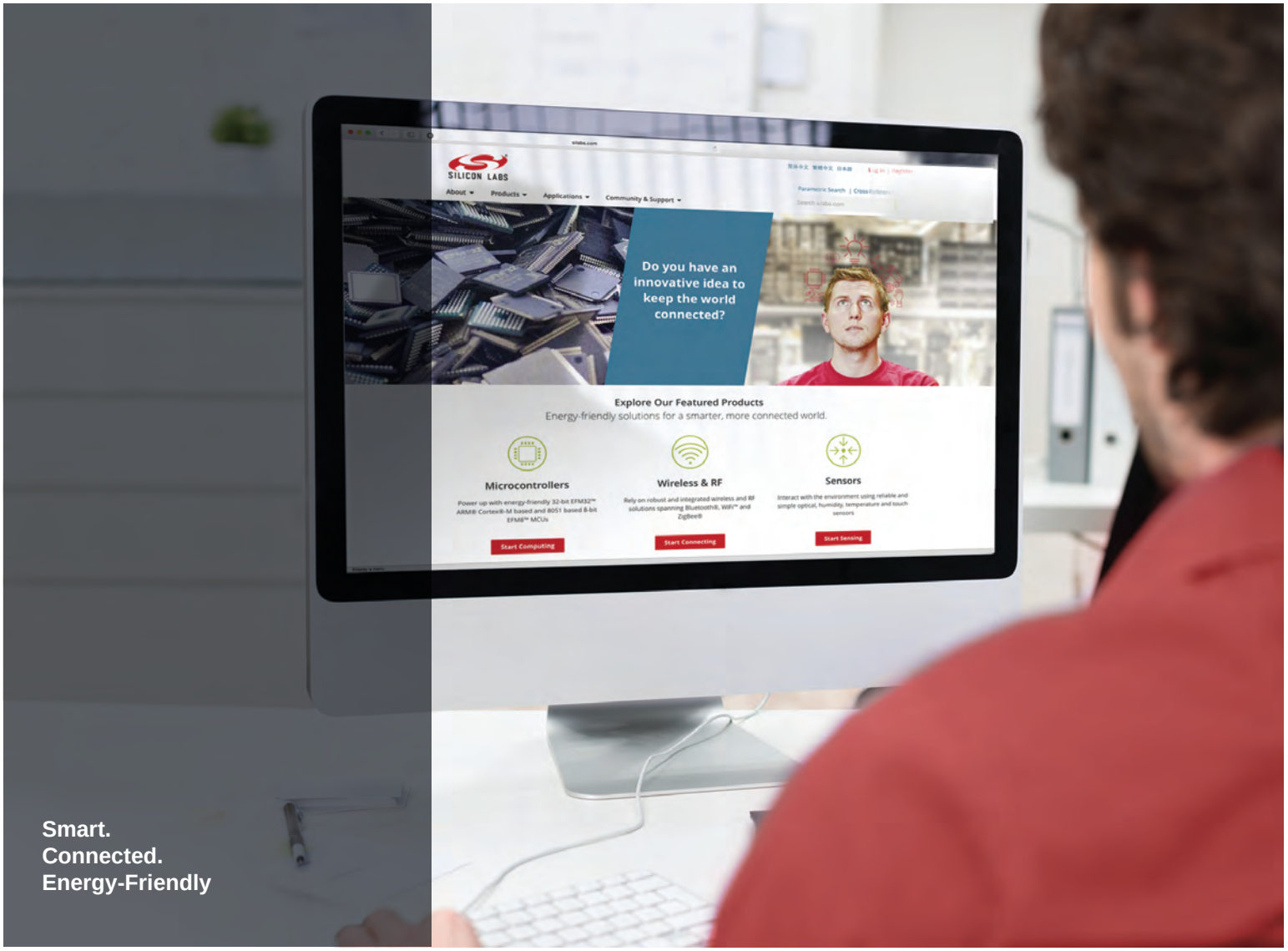
- Added references to AEC-Q100 throughout.
- Changed all 60747-5-2 references to 60747-5-5.
- Added references to CQC throughout.
- Removed all references to moisture sensitivity level.

## Revision 1.3 to Revision 1.4

- Updated Table 14, Ordering Part Numbers.
  - Added Revision D Ordering Part Numbers.
  - Removed all Ordering Part Numbers of previous revisions.

## Revision 1.4 to Revision 1.5

- Updated Table 2 on page 8.
  - Added CQC certificate numbers.
- Updated Table 3 on page 9.
  - Updated Erosion Depth specification.
- Updated Table 8 on page 12.
  - Replaced $I_O$ with Peak Output Current $I_{OPK}$.
  - Added $T_J$ specification in Table 8 on page 12.
- Updated Figure 14 on page 17.
- Updated Figure 15 on page 18.
- Updated Figure 16 on page 18.
- Updated "9.Ordering Guide" on page 22.
  - Updated AEC-Q100 note.

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