# PCM1865-Q1 110 dB 4ch Audio ADCs With Universal Front End

## 1 Features

- Universal Analog Mic Input, 2.1 $V_{RMS}$ Full Scale
  - 8 Analog Input Pins With MUX and PGA
  - Analog Pre-Mix Function Before PGA/MUX
  - Single-Ended, Pseudo-Differential or Differential Inputs With Mic Bias
  - 4x Digital Microphone Inputs
- Up to 4 Mono ADC Channels (PCM1865-Q1)
- $I^2C$ or SPI Control (PCM1865-Q1)
- H/W Programmable Gain Amplifier
  - Fixed Mic Pregain Select: 20, 32 dB (Analog)
- S/W Programmable Gain Amplifier
- Integrated High Performance Audio PLL
- Single 3.3 V Supply for Analog and Digital
  - Additional 1.8 V Core and Interface for Lower Power Consumption
- Power Dissipation at 3.3 V: <145 mW
- 'Energysense' Audio Content Detector - for Auto System Wakeup and Sleep
- Master or Slave Audio Interface
- Mixer Functionality:
  - Digital Mixer to Mix ADC Outputs and $I^2S$ Synchronous Inputs
  - Zero Crossing PGA Gain Changes
- Automatic PGA Clipping Suppression Control
- PCB-Footprint Compatibility Across All Devices
- Qualified in Accordance With AEC-Q100 for Automotive Applications

## 2 Applications

- Home Theater and TV
- Automotive Head Units
- Bluetooth® Speaker
- Microphone Array Processors

## 3 Description

The PCM1865-Q1 audio front-end device takes a new approach to audio-function integration to ease compliance with European Ecodesign legislation while enabling high-performance end products. With no need for a 5-V supply or an external programmable-gain amplifier, smaller, smarter products are feasible at reduced cost.

The PCM1865-Q1's highly flexible audio front end supports input levels from small-mV microphone inputs to 2.1 $V_{RMS}$ line Inputs without external resistor dividers. The PCM1865-Q1 integrates many system-level functions that assist or replace some DSP functions.

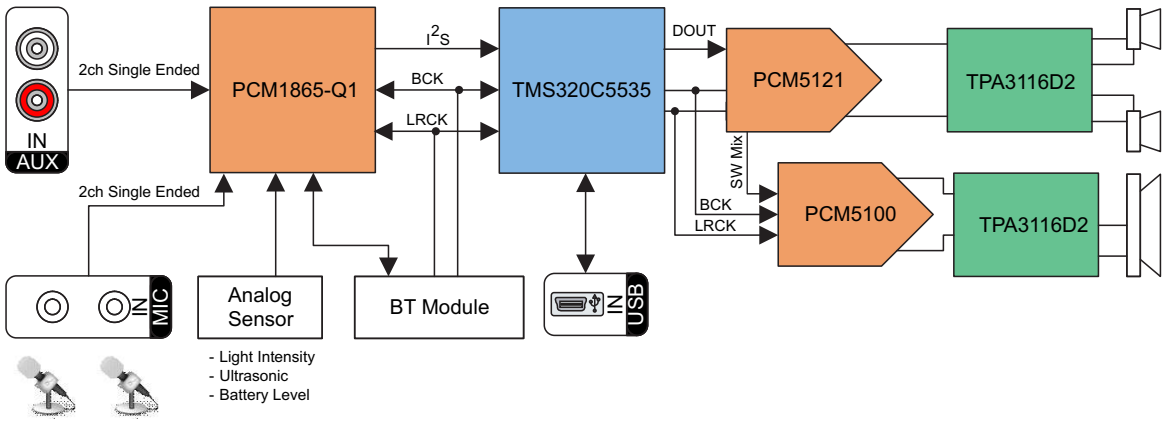
All these features are available using a single 3.3-V power supply. An integrated bandgap voltage reference provides excellent PSRR, so that a dedicated analog 3.3-V rail may not be required.

**Device Information**(1)

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| PCM1865-Q1 | TSSOP (30) | 7.80 mm × 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the document.

## 4 Simplified Application Diagram




An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

# Table of Contents

**1 Features** ... 1
**2 Applications** ... 1
**3 Description** ... 1
**4 Simplified Application Diagram** ... 1
**5 Revision History** ... 2
**6 Device Comparison Table** ... 3
**7 Pin Configuration and Functions** ... 4
7.1 Pin Assignments ... 4
**8 Specifications** ... 6
8.1 Absolute Maximum Ratings ... 6
8.2 ESD Ratings ... 6
8.3 Recommended Operating Conditions ... 6
8.4 Thermal Information ... 6
8.5 Electrical Characteristics, DC ... 7
8.6 Electrical Characteristics, Primary PGA and ADC AC Performance ... 8
8.7 Electrical Characteristics, Secondary ADC Performance ... 9
8.8 Digital Filter Characteristics ... 9
8.9 Timing Requirements, External Clock ... 9
8.10 $I^2C$ Control Interface Timing Requirements ... 10
8.11 SPI Control Interface Timing Requirements ... 11
8.12 Typical Characteristics ... 12
**9 Parameter Measurement Information** ... 14
**10 Detailed Description** ... 15
10.1 Overview ... 15
10.2 Functional Block Diagram ... 16
10.3 Device Functional Modes ... 17
10.4 Analog Front End ... 18
10.5 Microphone Support ... 19
10.6 PCM1865-Q1 Mixers and Multiplexers ... 19
10.7 Programmable Gain Amplifier ... 21
10.8 Automatic Clipping Suppression ... 21
10.9 Zero Crossing Detect ... 23
10.10 Digital Inputs ... 23
10.11 Clocks ... 25
10.12 ADCs ... 33
10.13 Energysense ... 35
10.14 Audio Processing ... 38
10.15 Fade-In and Fade-Out Functions ... 40
10.16 Mappable GPIO Pins ... 40
10.17 Current Status Registers ... 40
10.18 Control ... 40
10.19 Interrupt Controller ... 43
10.20 Audio Format Selection and Timing Details ... 46
**11 Application and Implementation** ... 49
11.1 Application Information ... 49
11.2 Typical Application ... 52
**12 Power Supply Recommendations** ... 53
12.1 Power Supply Distribution and Requirements ... 53
12.2 1.8V Support ... 53
12.3 Power Up Sequence ... 53
12.4 Lowest Power Down Modes ... 53
12.5 Power-On Reset Sequencing Timing Diagram ... 55
12.6 Power Connection Examples ... 55
12.7 Fade In ... 56
**13 Layout** ... 58
13.1 Layout Guidelines ... 58
13.2 Layout Example ... 60
**14 Programming and Registers Reference** ... 61
14.1 Coefficient Data Formats ... 61
14.2 Register Map ... 61
14.3 Programming DSP Coefficients ... 100
**15 Device and Documentation Support** ... 102
15.1 Development Support ... 102
15.2 Trademarks ... 102
15.3 Electrostatic Discharge Caution ... 102
15.4 Glossary ... 102
**16 Mechanical, Packaging, and Orderable Information** ... 102

## 5 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| December 2014 | * | Initial release. |


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# 6 Device Comparison Table

| PART NUMBER | CONTROL METHOD | DIFFERENTIAL SNR PERFORMANCE (1) | ANALOG FRONT END | Simultaneous Channel Capability |
|---|---|---|---|---|
| PCM1860 | Hardware | 103 dB | 1 or $2V_{RMS}$ MUX with fixed PGA gains | 2 |
| PCM1861 | Hardware | 110 dB | 1 or $2V_{RMS}$ MUX with fixed PGA gains | 2 |
| PCM1862 | $I^2C$ or SPI | 103 dB | 1 or $2V_{RMS}$ MUX, Mix, PGA and Aux ADC | 2 |
| PCM1863 | $I^2C$ or SPI | 110 dB | 1 or $2V_{RMS}$ MUX, Mix, PGA and Aux ADC | 2 |
| PCM1864 | $I^2C$ or SPI | 103 dB | 1 or $2V_{RMS}$ MUX, Mix, PGA and Aux ADC, 4 mono ADCs | 4 |
| PCM1865 | $I^2C$ or SPI | 110 dB | 1 or $2V_{RMS}$ MUX, Mix, PGA and Aux ADC, 4 mono ADCs | 4 |

(1) A weighted data.

**Table 1. Typical Performance (3.3-V Supply, –1 dB FS Input)**

| Parameter | Performance |
|---|---|
| SNR | 110 dB |
| Single Ended Input Dynamic Range | 103 dB |
| Differential Input Dynamic Range | 110 dB |
| Differential Input THD+N at - 1dBFS | –93 dB |
| Full Scale Input | $2.1V_{RMS}$ |
| Normal Group Delay: | $30/f_S$ |
| Low Latency - Group Delay Latency: | $10/f_S$ |
| Sampling Frequency | 32 kHz to 192 kHz |

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# 7 Pin Configuration and Functions

## 7.1 Pin Assignments

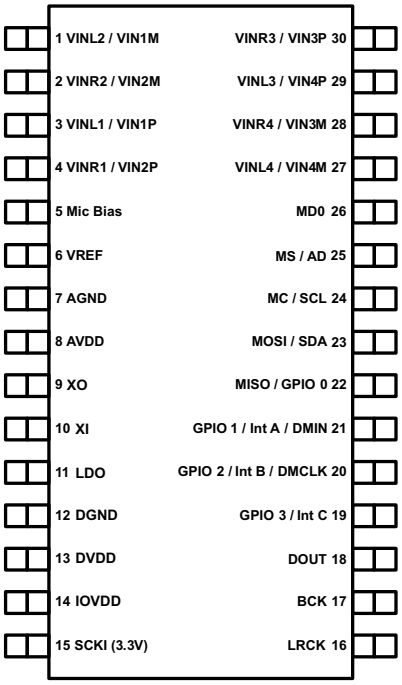



**Figure 1. Device Pin Assignments**

**Pin Functions**

| PIN | | I/O | DESCRIPTIONS |
|---|---|---|---|
| NAME | NO. | | |
| VINL2/VIN1M | 1 | I | Analog input 2, L-channel (or Differential M input for input 1) |
| VINR2/VIN2M | 2 | I | Analog input 2, R-channel (or Differential M input for input 2) |
| VINL1/VIN1P | 3 | I | Analog input 1, L-channel (or Differential P input for input 1) |
| VINR1/VIN2P | 4 | I | Analog input 1, R-channel (or Differential P input for input 2) |
| Mic Bias | 5 | — | Mic Bias |
| VREF | 6 | — | Reference voltage decoupling (= 0.5 AVDD) |
| AGND | 7 | — | Analog GND |
| AVDD | 8 | — | Analog power supply, +3.3 V |
| XO | 9 | — | Oscillation amplifier output (Connect External Crystal if needed here) |
| XI | 10 | I | Oscillation amplifier input (Connect External Crystal if needed here) |
| LDO | 11 | — | LDO output (or +1.8V input to bypass LDO) |
| DGND | 12 | — | Digital GND |
| DVDD | 13 | — | Digital power supply, +3.3 V |
| IOVDD | 14 | — | Power Supply for I/O Voltages (for example, +3.3 V or +1.8 V) |
| SCKI | 15 | I | CMOS Level (+3.3 V) Master Clock Input |
| LRCK | 16 | I/O | Audio data world clock (Left Right Clock) input/output(1) |
| BCK | 17 | I/O | Audio data bit clock input/output(1) |
| DOUT | 18 | O | Audio data digital output |
| GPIO 3 / INT C | 19 | I/O | GPIO 3 or Interrupt C |
| GPIO2 / INT B / DMCLK | 20 | I/O | GPIO 2, Interrupt B or Digital Microphone Clock Output |

(1) Schmitt trigger input with internal pull-down (50kΩ typically).


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## Pin Assignments (continued)

**Pin Functions (continued)**

| PIN | | I/O | DESCRIPTIONS |
|---|---|---|---|
| NAME | NO. | | |
| GPIO1 / INT A / DMIN | 21 | I/O | GPIO 1, Interrupt A or Digital Microphone Input |
| MISO / GPIO0 / DMIN2 | 22 | I/O | **SPI-Mode** Master In, Slave Out OR **I2C-Mode** GPIO0, OR DMIN2 |
| MOSI / SDA | 23 | I/O | **SPI-Mode** Master Out, Slave IN OR **I2C-Mode** SDA |
| MC / SCL | 24 | I | **SPI-Mode**Serial Bit Clock **I2C-Mode** Serial Bit Clock |
| MS / AD | 25 | I | **SPI-Mode** Chip Select OR **I2C-Mode** Address Pin |
| MD0 | 26 | I | Control Method Select Pin: $I^2C$ (tied low or not connected) or SPI (tied high) |
| VINL4/VIN4M | 27 | I | Analog input 4, L-channel (or Differential M input for input 4) |
| VINR4/VIN3M | 28 | I | Analog input 4, R-channel (or Differential M input for input 3) |
| VINL3/VIN4P | 29 | I | Analog input 3, L-channel (or Differential P input for input 4) |
| VINR3/VIN3P | 30 | I | Analog input 3, R-channel (or Differential P input for input 3) |

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# 8 Specifications

## 8.1 Absolute Maximum Ratings

over operating temperature (unless otherwise noted) (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | AVDD to AGND | –0.3 | 3.9 | V |
| | DVDD to DGND | –0.3 | 3.9 | |
| | IOVDD to DGND | –0.3 | 3.9 | |
| Ground voltage differences | AGND, DGND | –0.3 | 0.3 | |
| Digital input voltage | to DGND | –0.3 | IOVDD + 0.3 | |
| XI | to DGND | –0.3 | 2.1 | |
| Analog input voltage | $V_{IN}$xx | –1.7 | 5.0 | |
| $T_{stg}$ | Storage Temperature | –40 | 125 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 8.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins | ±1500 | |

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

## 8.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog supply voltage | AVDD to AGND | 3.0 | 3.3 | 3.6 | V |
| Digital supply voltage | DVDD to DGND | 3.0 | 3.3 | 3.6 | V |
| IO supply voltage to DGND | IOVDD at 1.8V to DGND | 1.62 | 1.8 | 1.98 | V |
| IO supply voltage to DGND | IOVDD at 3.3V to DGND | 3.0 | 3.3 | 3.6 | V |
| LDO to DGND | LDO is an input when using external 1.8V power supply | IOVDD – 0.3 | IOVDD | IOVDD + 0.3 | V |
| Operating junction temperature range | | –40 | | 125 | °C |

## 8.4 Thermal Information

over operating temperature range (unless otherwise noted)

| THERMAL METRIC(1) | | DBT (30 PINS) | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance (2) | 91.2 | ºC/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.0 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 41.5 | |
| $R_{\theta JC}$ | Junction-to-case (top) thermal resistance | 25.3 | |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 42.0 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) High K (High Thermal Conductivity, Multilayer Circuit Board)


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## 8.5 Electrical Characteristics, DC

all specifications at $T_A$ = 25°C, AVDD = 3.3V, DVDD = 3.3V, IOVDD = 3.3V, Master Mode, Single Speed Mode, $f_S$ = 48kHz, system clock = 256×$f_S$, 24-bit data (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power** | | | | | | |
| | 3.3V AVDD Current | 2 ch 48 kHz, XTAL Master Mode | | 16 | | mA |
| | 3.3V AVDD Current | 4 ch, 48 kHz, Slave mode | | 31 | | mA |
| | 3.3V DVDD Current | 2 ch 48 kHz, XTAL Master Mode | | 10 | | µA |
| | 3.3V DVDD Current | 4 ch 48 kHz, XTAL Master Mode | | 10 | | µA |
| | 1.8V DVDD Current | DVDD=1.8 V, 2 ch, 48k Hz, XTAL | | 10 | | µA |
| | PSRR | Valid with recommended values on Analog Rails (AVDD, VREF etc) | | 80 | | dB |
| | Power Consumption | 48 kHz 2 ch Active 3.3 V source for all | | 80 | | mW |
| | Power Consumption | 48 kHz Sleep (Energysense) 3.3 V source for all | | 24 | | mW |
| | Power Consumption | 48 kHz Standby 3.3 V source for all | | 0.59 | | mW |
| | Power Consumption | 48 kHz 4ch Active 3.3 V source for all | | 145 | | mW |
| | 3.3V AVDD Current | 2 ch 48 kHz with XTAL - Sleep Mode | | 2.7 | | mA |
| | 3.3V AVDD Current | 2 ch 48 kHz with XTAL - Standby Mode | | 17.1 | | mA |
| | 3.3V AVDD Current | 2 ch 48 kHz with XTAL - Powerdown Mode | | 1.2 | | mA |
| | 3.3V DVDD Current | 3.3 V DVDD 2 ch Mode, 48 kHz, Master Mode - Sleep Mode | | 353 | | µA |
| | 3.3V DVDD Current | 3.3 V DVDD 2 ch Mode, 48 kHz, Master Mode - Standby Mode | | 353 | | µA |
| | 3.3V DVDD Current | 3.3 V DVDD 2 ch Mode, 48 kHz, master mode - Powerdown | | 353 | | µA |
| | 1.8V DVDD Current | DVDD=1.8 V, 2 ch, 48 kHz, XTAL.- Sleep Mode | | 384 | | µA |
| | 1.8V DVDD Current | DVDD=1.8 V, 2 ch, 48 kHz, XTAL.- Powerdown | | 384 | | µA |
| | 1.8V DVDD Current | DVDD=1.8 V, 2 ch, 48 kHz, XTAL. Powerdown | | 384 | | µA |
| | Power Consumption (3.3V AVDD, 1.8V DVDD) | 48 kHz 2 ch Active 3.3 V analog, 1.8 V digital | | 68 | | mW |
| | Power Consumption (3.3V AVDD, 1.8V DVDD) | 48 kHz 4 ch Active 3.3 V analog, 1.8 V digital | | 128 | | mW |
| | 3.3V AVDD Current | 4 ch, 48 kHz, Master mode | | 31 | | mA |
| **Mic Bias** | | | | | | |
| | Mic Bias Noise | | | 5 | | µVRMS |
| | Mic Bias Current Capability | | | 4 | | mA |
| | Mic Bias Voltage | | | 2.6 | | V |
| **Digital IO** | | | | | | |
| $V_{OH}$ | Output Logic "High" Voltage Level | IOH = 2 mA | | 75 | | %IOVDD |
| $V_{OL}$ | Output Logic "Low" Voltage Level | IOL = –2mA | | 25 | | %IOVDD |
| $\|I_{IH}\|$1 | Input Logic "High" Current Level | All digital pins | | | 10 | µA |
| $\|I_{IL}\|$1 | Input Logic "Low" Current Level | All digital pins | | | –10 | µA |

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## 8.6 Electrical Characteristics, Primary PGA and ADC AC Performance

all specifications at $T_A$ = 25°C, AVDD = 3.3V, DVDD = 3.3V, IOVDD = 3.3V, Master Mode, Single Speed Mode, $f_S$ = 48kHz, system clock = 256×$f_S$, 24-bit data (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Input Channel Signal to Noise ratio | 0 dB PGA Gain, –60dB input signal, Master Mode. at DIFF Input | 97 | 110 | | dB |
| | Input Channel Signal to Noise ratio at 32 dB | 32 dB PGA Gain, –86dB input signal, Master Mode at DIFF Input | | 90 | | dB |
| | Input Channel THD+N | 0 dB PGA Gain, –1dB input signal, Master Mode at DIFF Input | –85 | –93 | | dB |
| | Input Channel THD+N at 32 dB | 32 dB PGA Gain, –33dB input signal, Master Mode at DIFF Input | | –84 | | dB |
| | L channel to R channel separation line input | 0 dB PGA Gain, –1dB input signal, Master Mode | | –105 | | dB |
| | L channel to R channel separation mic input | 20 dB PGA Gain, –1dB input signal, Master Mode | | –105 | | dB |
| | L1 channel to L2 channel separation line input | 0 dB PGA Gain, –1dB input signal, Master Mode | | –105 | | dB |
| | R1 channel to R2 channel separation line input | 0 dB PGA Gain, –1dB input signal, Master Mode | | –105 | | dB |
| | L1 channel to L2 channel separation mic input | 20 dB PGA Gain, –1dB input signal, Master Mode | | –105 | | dB |
| | R1 channel to R2 channel separation mic input | 20 dB PGA Gain, –1dB input signal, Master Mode | | –105 | | dB |
| | Range of the analog PGA | –12 to +12 dB (1 dB STEP) , 20 dB and 32 dB | –12 (1) | | 32 | dB |
| | Accuracy of the PGA + ADC | | | 0.5 | | dB |
| | Matching between PGA + ADCs onchip | | | 0.05 | | dB |
| | Full Scale Voltage Input per input pin | Single Ended Mode | | | 2.1 | $V_{RMS}$ |
| | Full Scale Voltage Input per input pin | Differential Input Mode (2.1 $V_{RMS}$ Per Pin, Out Of phase) | | | 4.2 | $V_{RMS}$ |
| | Input Channel Signal to Noise ratio | 0 dB PGA Gain, –60 dB input signal, Master Mode. at SE input | | 110 | | dB |
| | Input Channel Signal to Noise ratio at 32dB | 32 dB PGA Gain, –92 dB input signal, Master Mode at SE input | | 75 | | dB |
| | Input Channel THD+N | 0 dB PGA Gain, –1 dB input signal, Master Mode at SE input | | 87 | | dB |
| | Input Channel THD+N at 32dB | 32 dB PGA Gain, –33 dB input signal, Master Mode at SE input | | 68 | | dB |
| | Input Impedance per analog input pin | | | 10 | | kΩ |
| CMRR | Common Mode Rejection Ratio | Differential Input, 1 kHz signal on both pins and measure level at output. | | 56 | | dB |

(1) Specified by design.


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## 8.7 Electrical Characteristics, Secondary ADC Performance

all specifications at $T_A$ = 25°C, AVDD = 3.3V, DVDD = 3.3V, IOVDD = 3.3V, Master Mode, Single Speed Mode, $f_S$ = 48kHz, system clock = 256×$f_S$, 24-bit data (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Energysense Detection Threshold | | | –57 | | dBFS |
| Energysense Signal Bandwidth | | | 10 | | kHz |
| Energysense Accuracy(1) | | | 3 | | dB |
| Secondary ADC Accuracy | | | 12 | | bits |
| Secondary ADC Sampling Rate | | | same as audio sampling rate | | |

(1) Specified by design.

## 8.8 Digital Filter Characteristics

all specifications at $T_A$ = 25°C, AVDD = 3.3V, DVDD = 3.3V, IOVDD = 3.3V, Master Mode, Single Speed Mode, $f_S$ = 48kHz, system clock = 256×$f_S$, 24-bit data (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **Classic FIR** | | | | | |
| Pass Band | | | 0.454 | | $f_S$ |
| Stop Band | | | 0.583 | | $f_S$ |
| Pass Band Ripple | | | ±0.05 | | dB |
| Stop Band Attenuation | | | –65 | | dB |
| Group Delay / Latency | | | 30 | | Samples |
| HPF Frequency Response | | | 1 | | Hz |
| **Low Latency IIR** | | | | | |
| Pass Band | | | 0.454 | | $f_S$ |
| Stop Band | | | 0.546 | | $f_S$ |
| Pass Band Ripple | | | ±0.02 | | dB |
| Stop Band Attenuation | | | –75 | | dB |
| Group Delay / Latency | | | 10 | | Samples |
| HPF Frequency Response | | | 1 | | Hz |

## 8.9 Timing Requirements, External Clock

all specifications at $T_A$ = 25°C, AVDD = 3.3V, DVDD = 3.3V, IOVDD = 3.3V, Master Mode, Single Speed Mode, $f_S$ = 48kHz, system clock = 256×$f_S$, 24-bit data (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| XTAL Support | | 15 | | 35 | MHz |
| MCLK Frequency | 3.3 V on MCLK Pin | 1 | | 50 | MHz |
| MCLK | 1.8 V MCLK Input on XI pin. | 1 | | 50 | MHz |
| MCLK Input Duty Cycle | 1.8 V | 48% | | 52% | |

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## 8.10 I²C Control Interface Timing Requirements

| | | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | Standard | | 100 | kHz |
| | | Fast | | 400 | kHz |
| $t_{BUF}$ | Bus free time between a STOP and START condition | Standard | 4.7 | | µs |
| | | Fast | 1.3 | | |
| $t_{LOW}$ | Low period of the SCL clock | Standard | 4.7 | | µs |
| | | Fast | 1.3 | | |
| $t_{HI}$ | High period of the SCL clock | Standard | 4.0 | | µs |
| | | Fast | 600 | | ns |
| $t_{RS-SU}$ | Setup time for (repeated) START condition | Standard | 4.7 | | µs |
| | | Fast | 600 | | ns |
| $t_{S-HD}$ | Hold time for (repeated) START condition | Standard | 4.0 | | µs |
| $t_{RS-HD}$ | | Fast | 600 | | ns |
| $t_{D-SU}$ | Data setup time | Standard | 250 | | ns |
| | | Fast | 100 | | |
| $t_{D-HD}$ | Data hold time | Standard | 0 | 900 | ns |
| | | Fast | 0 | 900 | |
| $t_{SCL-R}$ | Rise time of SCL signal | Standard | $20 + 0.1C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1C_B$ | 300 | |
| $t_{SCL-R1}$ | Rise time of SCL signal after a repeated START condition and after an acknowledge bit | Standard | $20 + 0.1C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1C_B$ | 300 | |
| $t_{SCL-F}$ | Fall time of SCL signal | Standard | $20 + 0.1C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1C_B$ | 300 | |
| $t_{SDA-R}$ | Rise time of SDA signal | Standard | $20 + 0.1C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1C_B$ | 300 | |
| $t_{SDA-F}$ | Fall time of SDA signal | Standard | $20 + 0.1C_B$ | 1000 | ns |
| | | Fast | $20 + 0.1C_B$ | 300 | |
| $t_{P-SU}$ | Setup time for STOP condition | Standard | 4.0 | | µs |
| | | Fast | 600 | | ns |
| $C_B$ | Capacitive load for SDA and SCL line | | | 400 | pF |
| $t_{SP}$ | Pulse width of spike suppressed | Fast | | 50 | ns |
| $V_{NH}$ | Noise margin at High level for each connected device (including hysteresis) | | $0.2V_{DD}$ | | V |

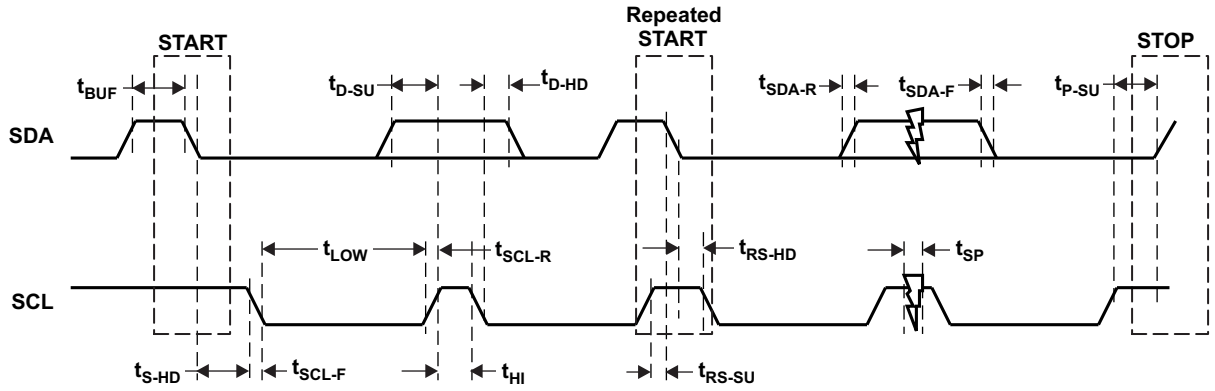



**Figure 2. I²C Control Interface Timing**


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## 8.11 SPI Control Interface Timing Requirements

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{MCY}$ | MC Pulse Cycle Time | 100 | | ns |
| $t_{MCL}$ | MC Low Level Time | 40 | | ns |
| $t_{MCH}$ | MC High Level Time | 40 | | ns |
| $t_{MHH}$ | High Level Time | 20 | | ns |
| $t_{MSS}$ | Fall Edge to MC Rise Edge | 30 | | ns |
| $t_{MSH}$ | Hold Time(1) | 30 | | ns |
| $t_{MDH}$ | MOSI Hold Time | 15 | | ns |
| $t_{MDS}$ | MOSI Set-up Time | 15 | | ns |
| $t_{MOS}$ | MC Rise Edge to MDO Stable | | 20 | ns |

(1) MC fall edge for LSB to MS rise edge.

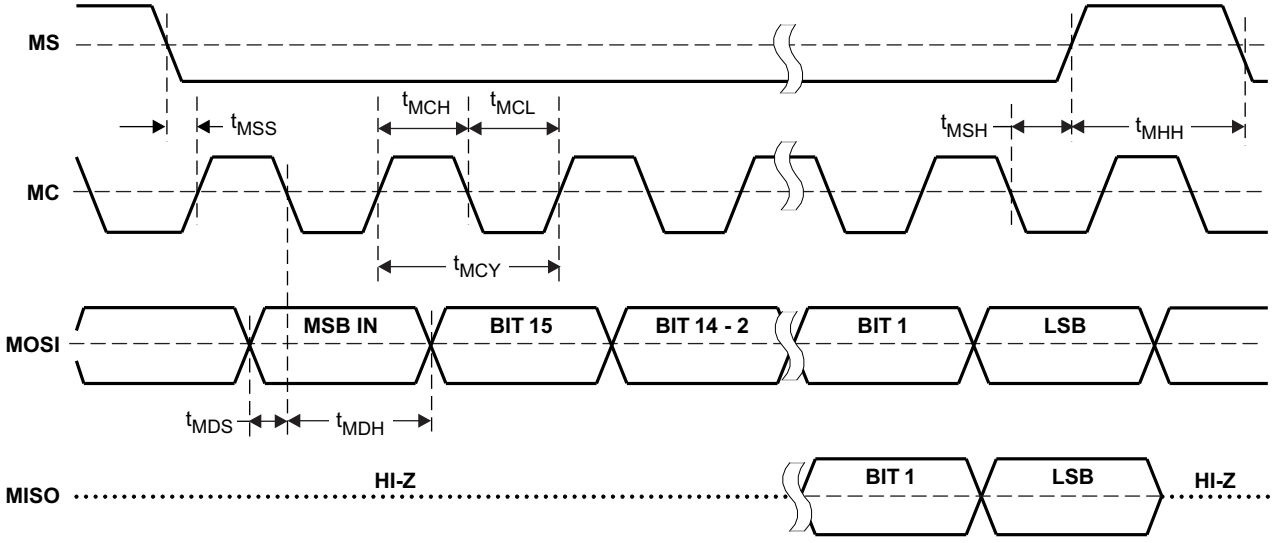



**Figure 3. SPI Control Interface Timing**

## 8.12 Typical Characteristics

all specifications at $T_A$ = 25°C, AVDD = 3.3V, DVDD = 3.3V, IOVDD = 3.3V, Master Mode, Single Speed Mode, $f_S$ = 48kHz, system clock = 256×$f_S$, 24-bit data (unless otherwise noted)

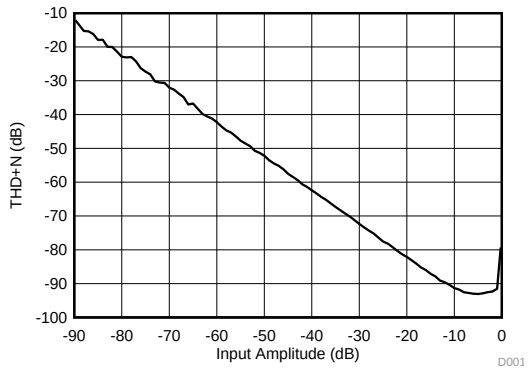



**Figure 4. THD+N vs Input Level**

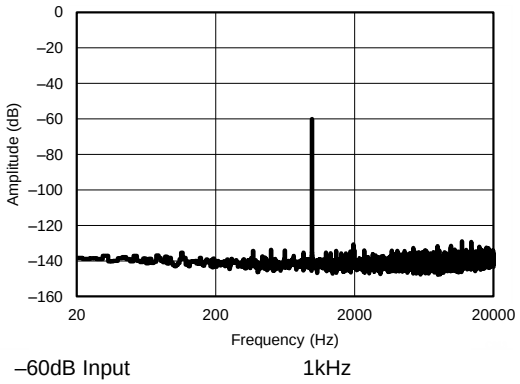



**Figure 5. Frequency Response**

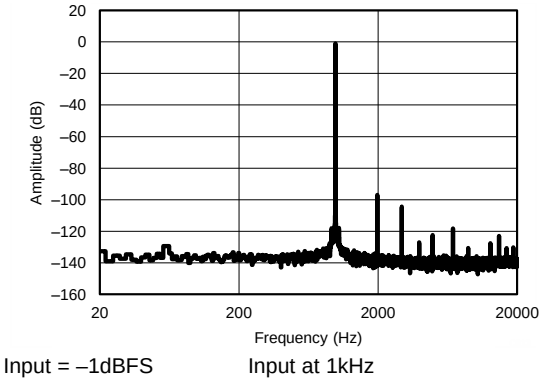



**Figure 6. Frequency Response**

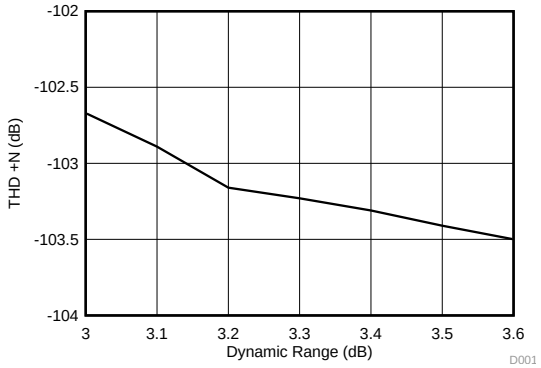



**Figure 7. Dynamic Range vs Supply Voltage**

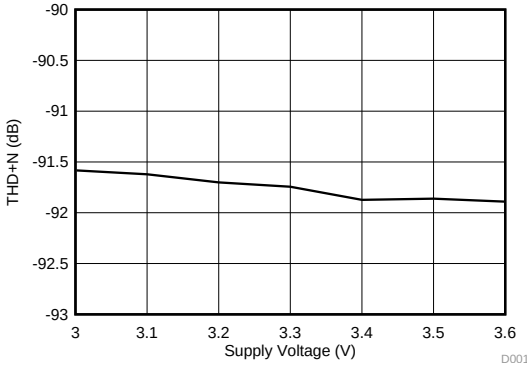



**Figure 8. THD+N vs Supply Voltage**

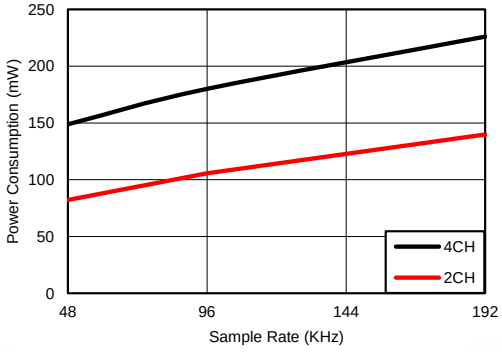
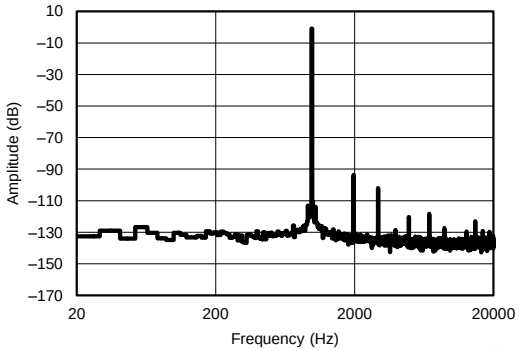



**Figure 9. Power Consumption vs Sample Rate**


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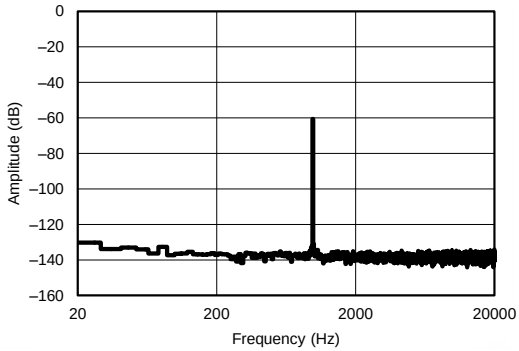
## Typical Characteristics (continued)

all specifications at $T_A$ = 25°C, AVDD = 3.3V, DVDD = 3.3V, IOVDD = 3.3V, Master Mode, Single Speed Mode, $f_S$ = 48kHz, system clock = 256×$f_S$, 24-bit data (unless otherwise noted)



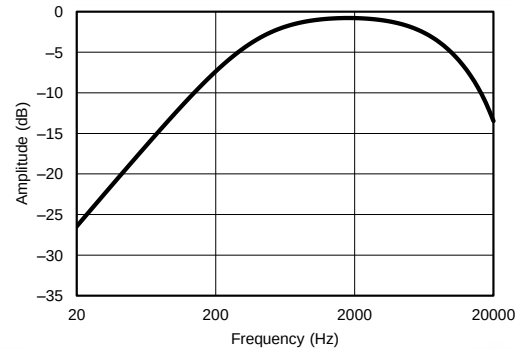

$f_S$ = 192kHz Input = –1dBFS Input at 1kHz

**Figure 10. FFT with -1dBFS input**



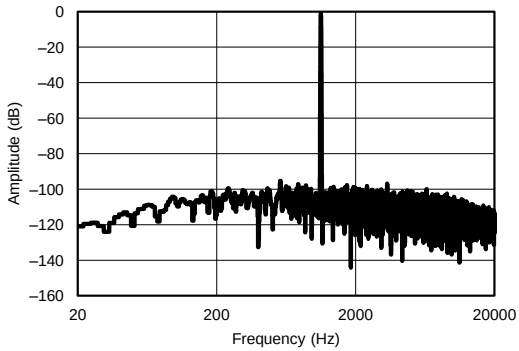

$f_S$ = 192kHz Input = –60dBFS Input at 1kHz

**Figure 11. FFT with -60dBFS input**



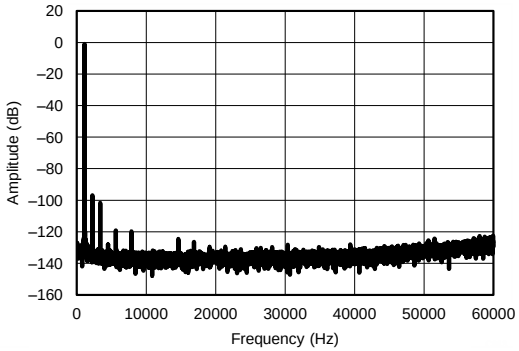

$f_S$ = 48kHz

**Figure 12. Seconday ADC Frequency Response**




$f_S$ = 48kHz

**Figure 13. Secondary ADC FFT**




$f_S$ = 192kHz BW = 60kHz Input = –1dBFS

**Figure 14. High Bandwidth FFT of THD Components**

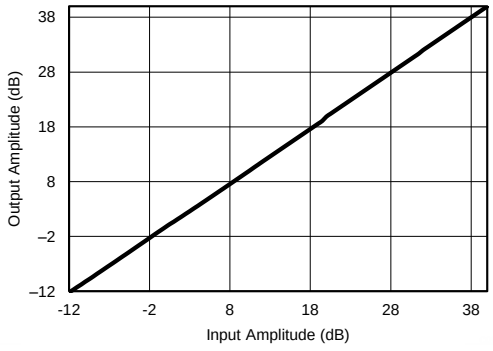



**Figure 15. PGA ADC Gain**

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## Typical Characteristics (continued)

all specifications at $T_A$ = 25°C, AVDD = 3.3V, DVDD = 3.3V, IOVDD = 3.3V, Master Mode, Single Speed Mode, $f_S$ = 48kHz, system clock = 256×$f_S$, 24-bit data (unless otherwise noted)

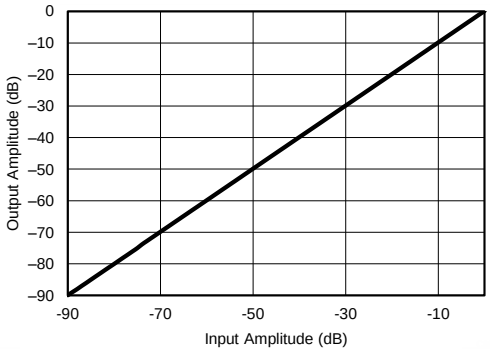



**Figure 16. Linearity, Input vs Output**

# 9 Parameter Measurement Information

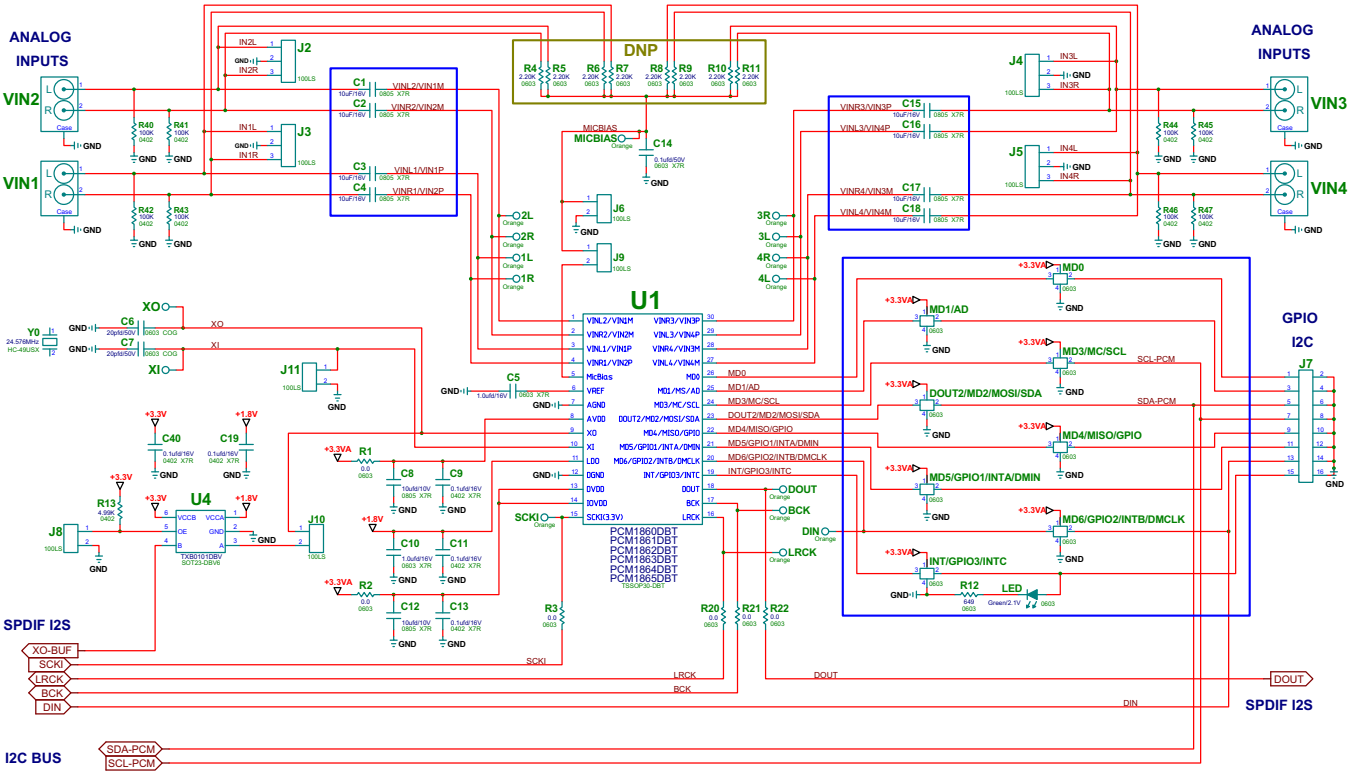



**Figure 17. PCM1865-Q1 Test Circuit**

All typical characteristics for the devices are measured using the EVM and an Audio Precision SYS-2722 Audio Analyzer. A PSIA interface is used to allow the I2S interface to be driven directly into the SYS-2722.


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# 10 Detailed Description

## 10.1 Overview

The PCM1865-Q1 supports advanced clocking support with the aid of an integrated oscillator circuit and an onchip analog PLL. The integrated oscillator circuit allows the capability to use an external crystal or an external Master clock as the clock source in Master mode. In addition, the PLL can be used to generate an onchip master clock that can be shared with the rest of the system, all from a bit clock input. This is especially useful in systems where the audio source has no master clock to drive DACs and amplifiers. The onchip clock monitoring system can also be used to generate interrupts for the system microcontroller, should clocks be lost.

The secondary ADC is a lower power, non-audio ADC that is used in sleep mode to monitor the analog inputs. It can also be used in ControlSense mode to measure DC voltages in a system, such as battery voltage, control potentiometers. Additional Controlsense features are the ability to generate interrupts once detected voltages cross specific thresholds, allowing the microcontroller to be in a lower power sleep mode while control voltages being measured are stable.

Control registers in this datasheet are given by **REGISTER BIT/BYTE NAME (Page.x HEX ADDRESS).** SE refers to "Single Ended" analog inputs, DIFF refers to "Differential" analog inputs. SCK (System Clock) and MCLK (Master Clock) are used interchangeably. Sampling frequency is symbolized by "$f_S$". Full scale is symbolized by "FS". Sample time as a unit is symbolized by "$t_S$".

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## 10.2 Functional Block Diagram

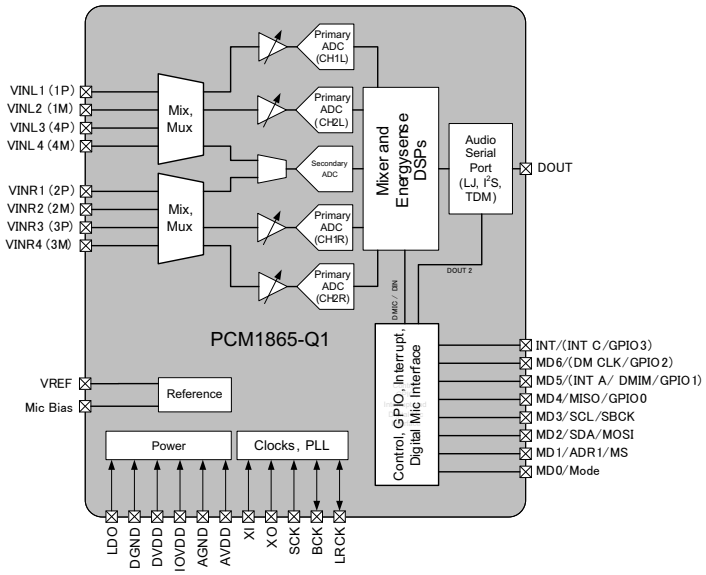



**Figure 18. Simplified Block Diagram**

An internal block diagram of the PCM1865-Q1 is shown below. Note that power supplies and references have been omitted from this diagram to aid simplicity. Dotted lines (for the PGA and the additional ADC's) are for the 4ch devices only. Greyed out pins are the multifunction pins only.


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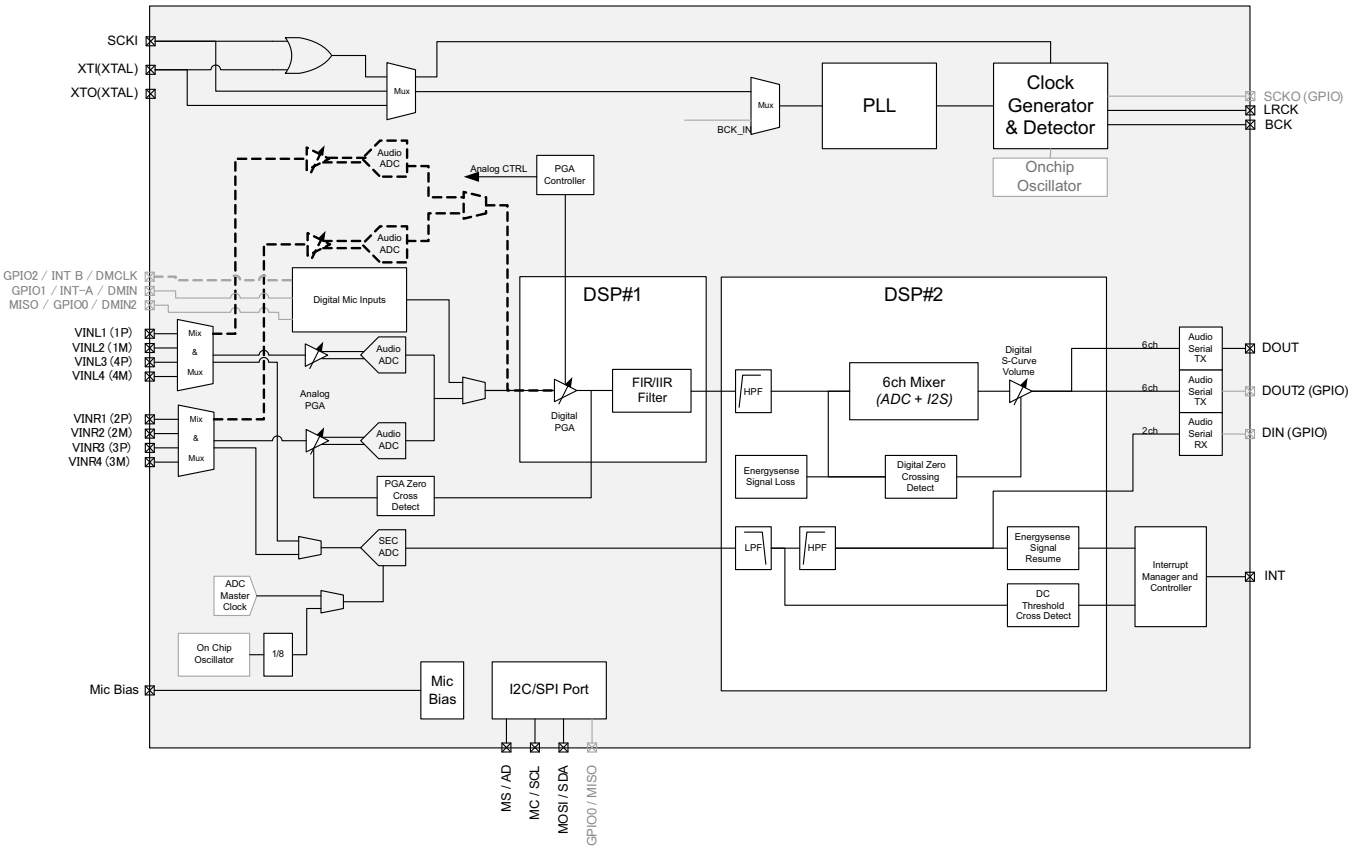



**Figure 19. Internal Block Diagram of the PCM1865-Q1**

## 10.3 Device Functional Modes

### 10.3.1 Power Mode Descriptions

The PCM1865-Q1 has multiple power states. They are Active, Sleep, Idle, and Standby.

**Active Mode** describes the active mode where the device is targeting full performance and functionality.

**Sleep Mode** describes a mode where the main ADCs are not in use, but the device continues to do Energysense input level detection.

**Idle Mode** describes a mode where the digital output is muted and the analog side (such as PGAs) are still powered up.

**Standby / Shutdown** drops the power into an ultra-low power mode where only the control port is available.

**Table 2. Power Modes**

| Analog Functions | Active or Idle (Mute) | Sleep (Energysense) | Standby / Shutdown |
|---|---|---|---|
| Programmable Gain Amps | ON | OFF | OFF |
| ADC | ON | OFF | OFF |
| ADC Reference | ON | OFF | OFF |
| CMBF | ON | ON | ON |
| Reference | ON | ON | ON |
| Mic Bias | ON | ON | OFF |
| Secondary ADC PGA | ON | ON | OFF |
| Secondary PGA | ON | ON | OFF |

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**Table 2. Power Modes (continued)**

| Analog Functions | Active or Idle (Mute) | Sleep (Energysense) | Standby / Shutdown |
|---|---|---|---|
| **Accessory Functions** | | | |
| LDO | ON | ON | ON |
| Oscillator | ON | ON | ON |
| Clock Halt Detection | ON | ON | ON |
| PLL | ON | ON | OFF |
| **Digital Cores** | ON | 20% ON | 5% ON (Control Port Only) |

#### *10.3.1.1 PCM1865-Q1 Software Device Power Down Functions*

**Enter or Exit Stand-by mode for Software Controlled Device**

Enter standby mode: Send power down command by writing register **PWRDN_CTRL (Page.0 0x70)**

Exit standby mode: Send power up command by writing register **PWRDN_CTRL (Page.0 0x70)**

**Enter or Exit Sleep mode for Software Device:**

(1) Send sleep command by writing register **PWRDN_CTRL (Page.0 0x70)** or

(2) Halt BCK and LRCK when $I^2S$ is configured as $I^2S$ Slave mode

**Exit Sleep mode:**

(1) Send resume from (exit) sleep command by writing register PWRDN_CTRL or

(2) Resume BCK and LRCK when $I^2S$ is configured as $I^2S$ master mode

#### *10.3.1.2 Bypassing the Internal LDO To Reduce Power Consumption*

The PCM1865-Q1 has an integrated LDO allowing single 3.3-V supply operation. However, developers desiring to minimize power consumption can bypass the on-chip LDO and provide 1.8V to DVDD under the following conditions:

- TDM Mode is not possible (the I/O or other function requires 3.3V)
- IOVDD MUST be 1.8V along with LDO, if an external 1.8V supply is used to bypass the internal LDO.

## 10.4 Analog Front End

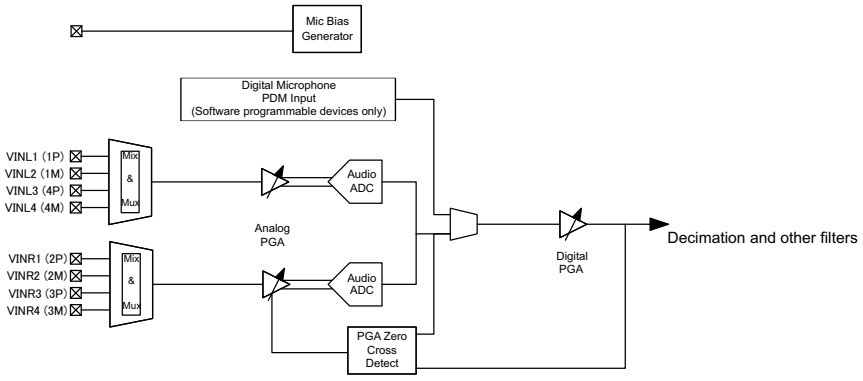



**Figure 20. High Level View of PCM1865-Q1 Front End Circuitry**

The PCM1865-Q1 has a universal front end that accepts differential or single-ended inputs, from microphone level to $2.1V_{RMS}$. The highest performance (up to 110 dB SNR) can be achieved using differential inputs. In differential mode, the full scale voltage is defined as 4.2VRMS, where each pin is 2.1VRMS, out of phase.


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## Analog Front End (continued)

The front-end Mix and MUX circuit allows both differential and single-ended inputs to be used in the products, as well as direct Input mixing. This feature is mainly enabled on the software-controlled devices, while the hardware-controlled devices support single-ended or differential inputs. The Mix and MUX circuits are summing circuits, done pre-PGA. No individual volume controls are available before the PGA.

DC blocking capacitors are required on the inputs, to ensure that the DC bias conditions are known (assumed to be GND, but **not** certain). Also, the value of the output short-circuit protection resistor in the source product is not known, which could cause issues such as gain error and DC shift.

## 10.5 Microphone Support

The PCM1865-Q1 supports analog and digital microphones. Analog signals are treated in much the same way as line-level signals, except for the requirement for mic bias. Digital microphone Inputs (PDM inputs) use GPIOs on the device. Two-channel ADC variants of the PCM1865-Q1 can support two digital microphones using a single data pin and a single clock pin. The 4-channel variants can support up to 4 digital microphones (2 data pins).

The PCM1865-Q1 software programmable devices support electret condenser mics through a mic bias circuit and a PGA input providing up to 32 dB of gain.

Digital microphones typically have a PDM output that can be brought into an ADC digital decimation filter. PDM microphones require power and a clock. Power should be handled from an external source.

Digital microphone mode Gain can be added in the digital PGA and in the mixer. The Maximum gain is 30 dB (18 dB in the mixer + 12 dB in the digital PGA).

On the PCM1865-Q1, a 2-channel digital mic + 2-channel ADC mode is possible.

### 10.5.1 Mic Bias

The PCM1865-Q1 can provide a microphone bias to power and bias microphones at 2.6V on pin 5. Mic Bias should be decoupled/filtered with an external capacitor. Mic Bias is typically used with a electret microphone. An on-chip series resistor can be bypassed using register **MIC_BIAS_CTRL (Page.3, 0x15).** By default, the device is configured to bypass the on-chip resistor.

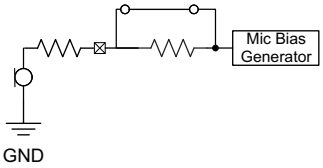



**Figure 21. On-Chip Mic Bias Resistor Bypassed (Default)**

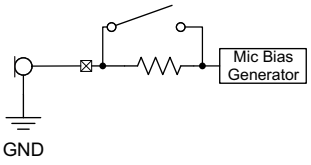



**Figure 22. On-Chip Mic Bias Resistor In Use**

## 10.6 PCM1865-Q1 Mixers and Multiplexers

The PCM1865-Q1 software programmable devices offer a mix/multiplex level of functionality on the front end as shown in Figure 20. The switches integrated into the multiplexer can also be switched on in parallel, offering a direct mix of inputs. This function can be selected by register for each ADC input selection, **ADCX1_INPUT_SEL_X (Page.0, 0x06 → 0x09)**. In single ended mode, each Audio ADC is tightly coupled to a dedicated PGA and MUX. ADC1L (and ADC2L on the PCM1865-Q1) is connected a mux that has input pins VINLx, (x = 1 to 4). ADC1R (and ADC2R on the PCM1865-Q1) is connected to a mux that has input pins VINRx (x = 1 to 4).

Mixing between the left channels of stereo pairs is possible in the mux dedicated to ADC1L and right channels of stereo pairs in the mux dedicated to ADC1R. In addition, polarity of the inputs can be inverted using the MSB of the select register. Mixing left and right sources to create mono mixes can only be done in the digital mixer, post ADC conversion, or alternatively, other analog inputs can be connected for mixing.

The examples available are below - where [SE] is single ended, and [DIFF] is a differential input. Bold items are the single channel selects.

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## PCM1865-Q1 Mixers and Multiplexers (continued)

**Table 3. MUX, Mix, and Polarity Input Selection**

| Register Code | ADC1L and ADC2L | ADC1R and ADC2R |
|---|---|---|
| 0x00 | No Selection (Mute) | No Selection (Mute) |
| **0x01** | **VINL1[SE] (Default)** | **VINR1[SE] (Default)** |
| **0x02** | **VINL2[SE]** | **VINR2[SE]** |
| 0x03 | VINL2[SE] + VINL1[SE] | VINR2[SE] + VINR1[SE] |
| **0x04** | **VINL3[SE]** | **VINR3[SE]** |
| 0x05 | VINL3[SE] + VINL1[SE] | VINR3[SE] + VINR1[SE] |
| 0x06 | VINL3[SE] + VINL2[SE] | VINR3[SE] + VINR2[SE] |
| 0x07 | VINL3[SE] + VINL2[SE] + VINL1[SE] | VINR3[SE] + VINR2[SE] + VINR1[SE] |
| **0x08** | **VINL4[SE]** | **VINR4[SE]** |
| 0x09 | VINL4[SE] + VINL1[SE] | VINR4[SE] + VINR1[SE] |
| 0x0A | VINL4[SE] + VINL2[SE] | VINR4[SE] + VINR2[SE] |
| 0x0B | VINL4[SE] + VINL2[SE] + VINL1[SE] | VINR4[SE] + VINR2[SE] + VINR1[SE] |
| 0x0C | VINL4[SE] + VINL3[SE] | VINR4[SE] + VINR3[SE] |
| 0x0D | VINL4[SE] + VINL3[SE] + VINL1[SE] | VINR4[SE] + VINR3[SE] + VINR1[SE] |
| 0x0E | VINL4[SE] + VINL3[SE] + VINL2[SE] | VINR4[SE] + VINR3[SE] + VINR2[SE] |
| 0x0F | VINL4[SE] + VINL3[SE] + VINL2[SE] + VINL1[SE] | VINR4[SE] + VINR3[SE] + VINR2[SE] + VINR1[SE] |
| **0x10** | **{VIN1P, VIN1M}[DIFF]** | **{VIN2P, VIN2M}[DIFF]** |
| **0x20** | **{VIN4P, VIN4M}[DIFF]** | **{VIN3P, VIN3M}[DIFF]** |
| 0x30 | {VIN1P, VIN1M}[DIFF] + {VIN4P, VIN4M}[DIFF] | {VIN2P, VIN2M}[DIFF] + {VIN3P, VIN3M}[DIFF] |


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## 10.7 Programmable Gain Amplifier

The PCM1865-Q1 has a two-stage programmable gain amplifier (PGA). Coarse gain adjustment is done in the analog domain, whilst fine gain adjustment is done in the digital domain. The ±12 dB Analog gain steps are designed for varying line level inputs, whilst the +20 dB and +32 dB are primarily designed for microphone inputs, which will likely need additional gain that can be done in the digital domain. The analog gain steps between -12 dB and +12 dB are in 1 dB steps. Half dB steps between those points are done in the digital PGA. Gain steps between 12 dB and 20 dB are all done in the digital domain. (for example, 18 dB gain = 12 dB analog + 6 dB Digital). The gain structure in the PCM1865-Q1 is shown below.

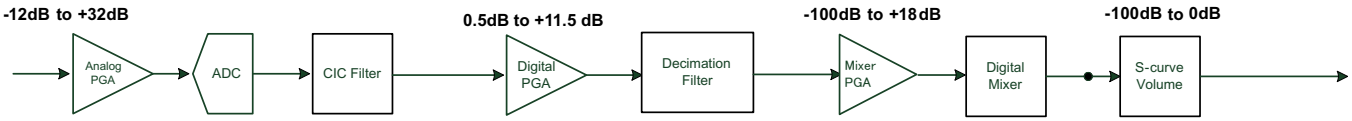



**Figure 23. PCM1865-Q1 Complete Gain Structure (PGAs and Attenuator)**

The analog gain steps within the analog PGA are shown below. Again, from -12 dB to +12 dB, the steps are 1 dB each. The digital PGA has granularity down to 0.5 dB.

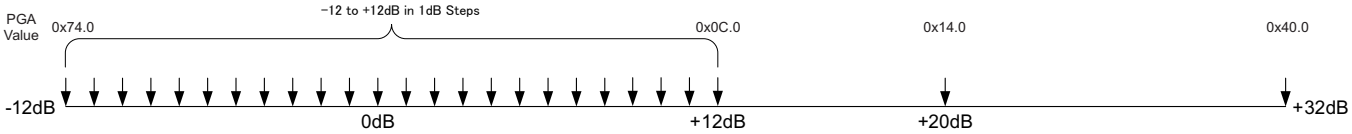



**Figure 24. Analog Gain Steps with PCM1865-Q1 Software Programmable Devices**

The PGA in the PCM1865-Q1 is a hybrid analog and digital programmable gain amplifier. The devices integrate a lookup table with the optimal gain balance between analog and digital gain, allowing the gain to be set in a single register per channel. For example, set 18dB Gain, and the system will allocate 12dB to the analog PGA and 6dB to the digital.

The PGA is a zero crossing detect type, and has the ability to set target gain, and have the device work towards it (with a timeout if there is no zero crossing). Any changes in the Analog PGA and Digital PGA are designed to step towards the final level. However, any changes in the Mixer PGA are immediate. Care should be taken when changing gain levels in the digital mixer PGA. Alternatively, multiple writes can be made of small enough values that will not cause significant pops/clicks.

For example, Current level 0dB, set target as 3.5 dB – PGA increases gain in 0.5dB steps towards 3.5dB.

The Auto Gain Mapping function can by bypassed if required, using Manual Gain Mapping. Manual Gain Mapping is particularly useful when using digital microphones, as the PDM input signal bypasses the analog PGA and must be amplified using the digital PGA. (**PGA_MODE Register(Page.0, 0x19)**

**NOTE**

Using the device with a differential inputs increases the full scale voltage to 4.2VRMS (that's 2.1VRMS per pin, out of phase).

## 10.8 Automatic Clipping Suppression

The PCM1865-Q1 software controlled devices have the ability to automatically lower the gain in 0.5 dB steps under the following conditions if the ADC is clipping.

The device detects clipping after the decimation filter in the signal chain (shown in Figure 25), and counts the number of successive clips before responding.

The device can also generate an internal interrupt that can be mapped to a GPIO or interrupt pin, allowing the system microcontroller to make the decision to increase the gain and consider the clipping an isolated event, or make the decision that the new gain setting is appropriate.

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## Automatic Clipping Suppression (continued)

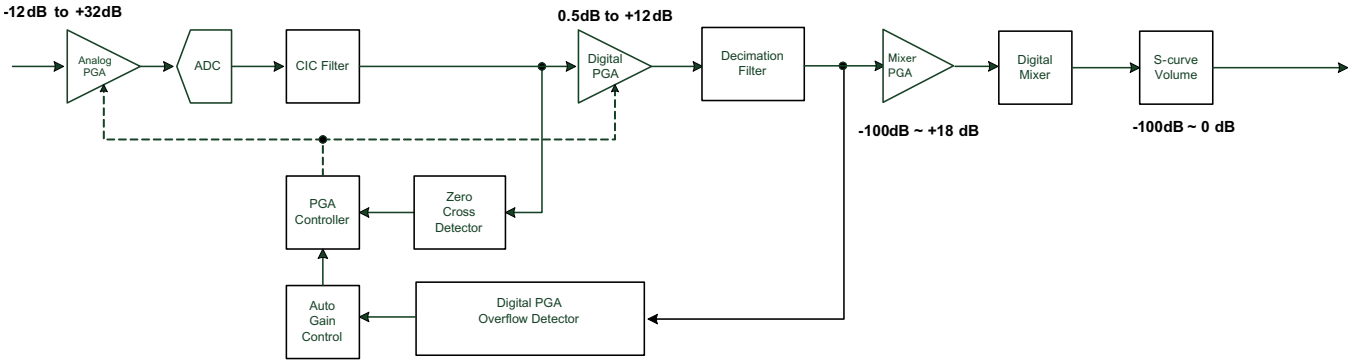



**Figure 25. Sampling points within the PCM1865-Q1 for Auto Clipping Suppression**

### Maximum Attenuation Level

This feature is not designed to be a complete analog gain control. This feature was defined to avoid clipping, and to inform the system microcontroller of a clipping event, to allow the microcontroller (or the end user) to decide if the gain should be increased again.

The maximum attenuation is programmable to be -3 / -4 / -5 / -6 dB.

### Channel Linking

Depending on the application, users may not want to link input channels, however, for the majority of Stereo input applications, its strongly recommended to set the system to track gain across inputs, to maintain balance.

The Auto PGA Clipping Suppression Control has the following settings:

**Table 4. Auto Clipping Suppression Control Registers**

| Register Name | Register Location | Usage | Values |
|---|---|---|---|
| AGC_EN | Pg0 0x05 | Enable Auto Gain Control. | 0: Disable (Default)<br>1: Enable |
| CLIP_NUM[1:0] | Pg0 0x05 | Start auto gain control after detects CLIP_NUM times of ADC sample clips | 0: 80<br>1: 40<br>2: 20<br>3: 10 (Default) |
| MAX_ATT[1:0] | Pg0 0x05 | Maximum automatic attenuation | 0: -3dB (Default)<br>1: -4dB<br>2: -5dB<br>3: -6dB |
| DPGA_CLIP_EN | Pg0 0x05 | Enable Clipping detection after the digital PGA. Note, digital PGA is post ADC, meaning that there will be a short delay before clipping is detected. | 0: Disable (Default)<br>1: Enable |
| LINK | Pg0 0x05 | Link all channels together. Should be linked if dealing with stereo sources to maintain balance. | 0: Independent control (Default)<br>1: Ch1[R]/Ch2[L]/Ch2[R] follow Ch1[L] PGA value. |
| SMOOTH | Pg0 0x05 | Enable Smooth transition from step to step. (zero crossing) | 0: Immediate Change<br>1: Smooth Change (Default) |


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## 10.9 Zero Crossing Detect

The PCM1865-Q1 uses a zero crossing detector to make gain changes only when the incoming signal crosses its halfway point between negative and positive swing, reducing "zipper noise".

There are two sources for the controller, the output of the ADC Modulator and the output from the digital PGA. The Analog PGA is sampled at 4× the audio sampling rate to detect the zero crossing. The digital PGA is sampled at a similar rate.

The process for changing gain in the PCM1865-Q1 is as follows:

1. Detect a zero crossing of the oversampled analog input channel.
2. Increment or Decrement the gain toward the target PGA value step by 0.5dB.
3. Repeat from (1) until arrival at the target PGA value.
4. If zero crossing does not occur for 8192 sample times (= time out), change the gain per sample.

This process does not require intervention by the user. This data serves as information only.

## 10.10 Digital Inputs

### 10.10.1 Stereo PCM Sources

The PCM1865-Q1 can support Stereo PCM data on GPIO pins so that $I^2S$ sources, such as wireless modules can have their data mixed with the incoming analog content. The clock rate of the incoming data (known as DIN) must be synchronous with the PCM1865-Q1 software programmable device main clocks. There is no integrated sample rate converter on-chip. The DIN signal can be received on GPIO0,1,2,3. configured on **GPIO_FUNC_X (Page.0 0x10 and 0x11)**. The incoming data is then driven to the digital mixer running on DSP2.

The audio format can be configured separately from the output serial port using register **RX_TDM_OFFSET (P0, 0x0E).**

Inputs can be mixed and volume-controlled before routing to a digital amplifier. Typical uses could be the connection to a *Bluetooth* module. The mixing and crossfading could be done all in the PCM1865-Q1, rather than a hard switch in external logic. The on-chip PLL can also help create the system master clock (SCKOUT) for poorly designed $I^2S$ *Bluetooth* modules that don't provide an system clock to drive the system DACs.

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## Digital Inputs (continued)

### 10.10.2 Digital PDM Microphones

Up to four digital microphones are supported on the PCM1865-Q1, using a shared output clock (configured from GPIO2) and two data lines, GPIO0 or GPIO1.

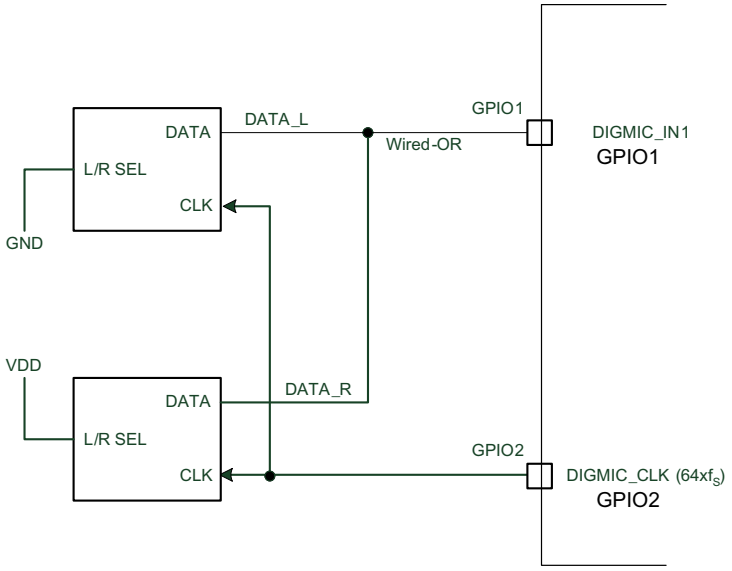



**Figure 26. Digital Microphone Example Connection**

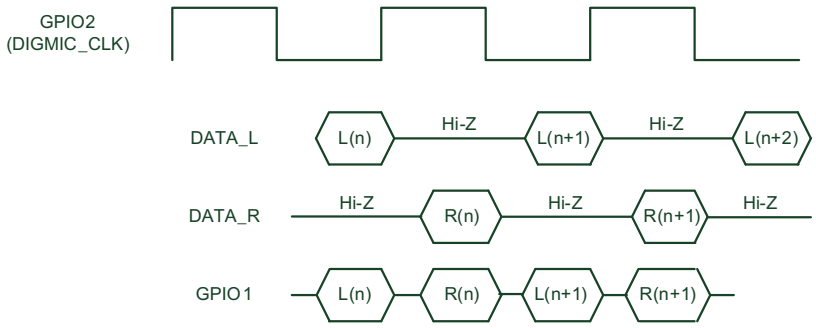



**Figure 27. Digital Microphone Protocol**

Supported Digital Microphone clock frequency is as follows, and the frequency depends on required operating sampling frequency as follows:

- 2.0480 MHz (32 kHz × 64)
- 2.8224 MHz (44.1 kHz × 64)
- 3.072 MHz (48 kHz × 64)
- 3.072 MHz (96 kHz × 32 )

The recommended operating conditions for the Digital MIC to get good performance are:

- Sampling frequency is 32 kHz or 44.1 kHz
- SCK is 256 × $f_S$.
- Enable Auto Clock Detector (Default)


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## 10.11 Clocks

### 10.11.1 Description

The PCM1865-Q1 has an extremely flexible clocking architecture. All converters require a Master Clock (typically a $2^n$ power of the sampling rate, known as MCK), a bit clock (BCK) which is used to clock the data bit by bit out of the device (typically running at 64-$f_S$ - to allow up to 32 bits per channel output) and finally a Wordclock/Left-Right Clock (LRCK) that is used to set the exact sampling point for the ADC.

The PCM1865-Q1 can be a clock master (where BCK and LRCK can be internally divided from a provided master clock) or can be a clock slave, where all clocks (MCK, BCK and LRCK) must be provided by an external source.

Unlike many competing devices, the PCM1865-Q1 can source its master clock from two different sources, either an external crystal, or a CMOS level (3.3 V or 1.8 V) clock, eliminating the usual external crystal oscillator circuit required to source a CMOS clock signal.

The PCM1865-Q1 also differentiates itself by integrating an on-chip Phase Locked Loop (PLL) that can generate real audio-rate clocks from any clock source between 1 MHz and 50 MHz. Software Controlled devices, such as the PCM1865-Q1 can have their PLL programmed to generate audio clocks based on any incoming clock rate. For example, a 12-MHz clock in the system can be used to generate clocks for a 44.1 kHz system.

### 10.11.2 External Clock-Source Limits

The 3 different clock sources for the device each have some limits in terms of their input circuitry. These limits are separate from the internal PLL capability.

**Table 5. External Clock-Source Limitations and notes**

| Clock Source | Limits | Notes |
|---|---|---|
| XTAL | 15 MHz → 35 MHz | |
| 3.3 V CMOS MCLK | 1 MHz → 50 MHz | Should be input to SCKI pin. 3.3 V CMOS can be input, even when IOVDD is 1.8 V |
| 1.8 V CMOS MCLK | 1 MHz → 50 MHz | Should be input to XI pin. |

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### 10.11.3 Device Clock Distribution and Generation

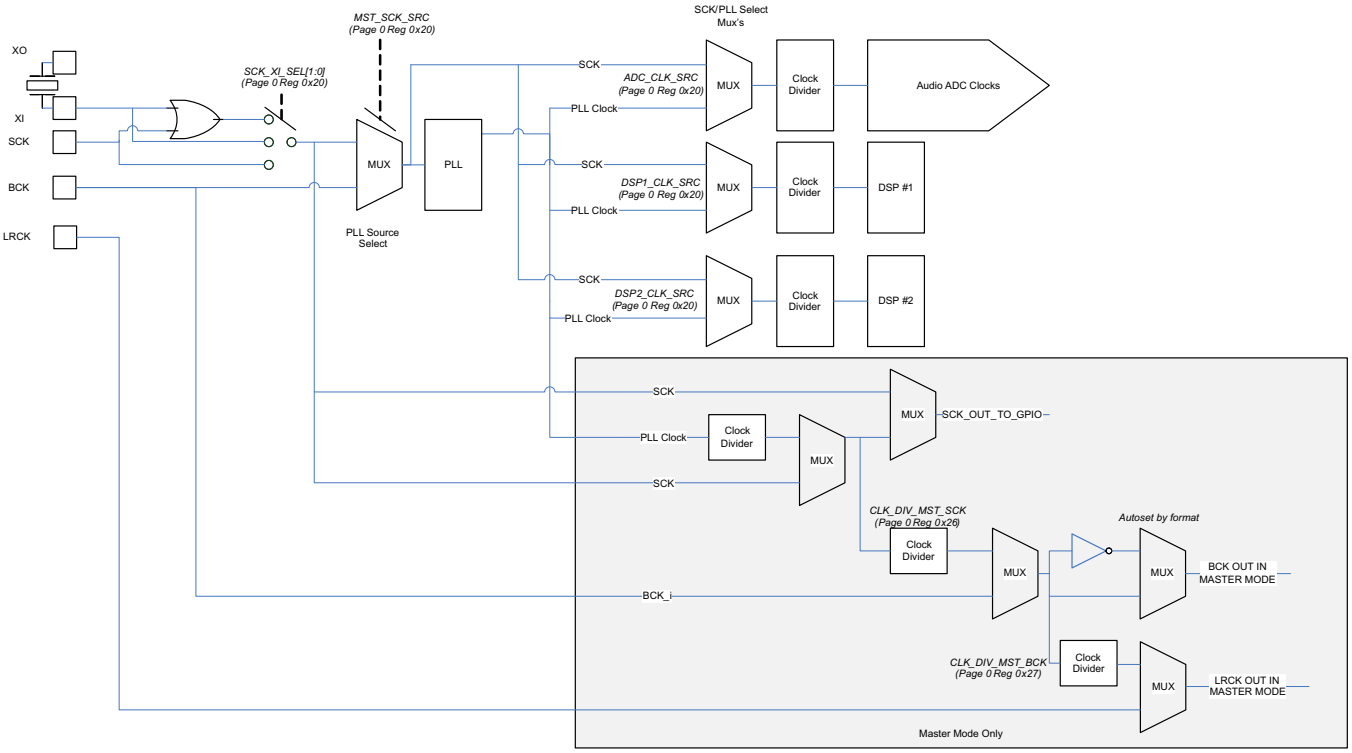



**Figure 28. PCM1865-Q1 Main Audio Clock Tree and Clock Generation**

PLLs are used in all modes to generate the clocks required to run both fixed-function DSPs. The dividers are automatically configured based on the clock rate detection. The clock architecture above allows non-audio clock sources to be used as clock sources and the PCM1865-Q1 to continue to run in a Master mode, providing all PCM/$I^2S$ Clocks for other converters in the system.

### 10.11.4 PCM1865-Q1 Clocking Modes

There are four different clocking modes available on the device which can take advantage of the onboard PLL and clock detection. Advanced clock detection and a smart internal state engine in the PCM1865-Q1 can automatically configure the various dividers in the device (shown in *Device Clock Distribution and Generation*) with optimized values. Automatic clock configuration is enabled by default, using the register **CLKDET_EN (Page.0, 0x20)**.

| NAME | Device | External XTAL/MCK INPUT | BCK, LRCK Direction | PLL Configuration |
|---|---|---|---|---|
| ADC Master Mode | PCM1865-Q1 | YES | OUT | Not Required |
| ADC Slave Mode | PCM1865-Q1 | YES | IN | Not Required |
| ADC Slave PLL Mode | PCM1865-Q1 | NO | IN | Automatic for standard audio rates |
| ADC Non-Audio MCK | PCM1865-Q1 | YES | OUT | Manual |


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#### 10.11.4.1 PCM1865-Q1 Clock Configuration and selection

The PCM1865-Q1 offers both Master and Slave functionality. In master mode, a source master clock (of 256, 384 or 512× the sampling rate) can be sourced from either an external crystal (XI/XO) or on an incoming SCK. (see *External Clock-Source Limits* for input rate limitations on SCK sources) The clock from XI and SCK are OR'd internally, allowing either to be used.

The device can generate the other $I^2S$ clocks (BCK and LRCK) in master mode (with dividers set in MD0 and MD1) or be a clock slave to MCK,BCK and LRCK. In this scenario, the device auto-detects the clock divider ratio.

In master mode, BCK per LRCK is fixed at 64. This allows up to 32 bits per channel.

Selection of the appropriate master/slave and clock ratio between MCK and $f_S$ can be done using MD0 and MD1.

Table 6 shows the suggested master clock rates for each of the sample rates supported.

**Table 6. External Master Clock Rate versus Sampling Frequency**

| SAMPLING RATE FREQUENCY | SYSTEM CLOCK FREQUENCY (MHz) | | |
|---|---|---|---|
| (kHz) | $256f_S$ | $384f_S$ | $512f_S$ |
| 8.0 | 2.048 | 3.072 | 4.096 |
| 16.0 | 4.096 | 6.144 | 8.192 |
| 32.0 | 8.1920 | 12.2880 | 16.3840 |
| 44.1 | 11.2896 | 16.9344 | 22.5792 |
| 48.0 | 12.2880 | 18.4320 | 24.5760 |
| 64.0 | 16.3840 | 24.5760 | 32.7680 |
| 88.2 | 22.5792 | 33.8688 | 45.1584 |
| 96.0 | 24.5760 | 36.8640 | 49.1520 |
| 176.4 | 45.1584 | | |
| 192.0 | 49.1520 | | |

For slave mode, BCK per LRCK should be set to 64.

#### 10.11.4.2 Clock Sources (PCM1865-Q1 Software Programmable Devices)

The PCM1865-Q1 devices support a wide range of options for generating the clocks required to operate the ADC section, as well as interface and other control blocks as shown in Figure 29.

The clocks for the PLL require a source reference clock. This clock source can be configured on software devices as the XTAL, SCK or BCK.

The PCM1865-Q1 software programmable devices share a similar clock tree for the generation and distribution of clocks Figure 28.

**CLK_MODE (Page.0 0x20)** is used to configure the clock configuration. Bits [5:7] configure the OR and MUX for the incoming MCLK.

Register **MST_MODE (Page.0 0x20)** is used to set the device in Master or Slave Mode. Bits [1:3] set clock sources for the ADC, DSP1 and DSP2. These can mostly be ignored for the most common applications, but are provided for advanced users.

The **CLKDET_EN (Page.0, 0x20)** register bit (Auto Clock Detector) is important; the clock detector is mainly functional for slave modes, and for master modes where the master clock is a 256/384/512× multiple of the incoming data rate.

**NOTE**

Non audio related master clock sources can be used with the PCM1865-Q1 software programmable devices providing the PLL is programmed manually. CLKDET_EN should be set to 0.

The result of configurations can be checked by reading registers **FS_INFO / CURRENT_BCK_RATIO (Page.0 0x73 and 0x74)**.

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**Table 7. PLL Configuration Registers**

| CLOCK MULTIPLEXER | FUNCTION | BITS |
|---|---|---|
| MST_SCK_SRC | PLL Reference | Page 0, Register 0x20 |
| **DIVIDER** | **FUNCTION** | **BITS** |
| CLK_DIV_PLL_SCK | Clock Divider of PLL to emulate SCK | Pg0, Reg 0x25, b[0:6] |
| CLK_DIV_MST_SCK | Master Mode SCK to SCKOUT Ratio | Pg0, Reg 0x26, b[0:6] |
| CLK_DIV_MST_BCK | Master Mode SCK to BCK Ratio | Pg0, Reg 0x27, b[0:6] |

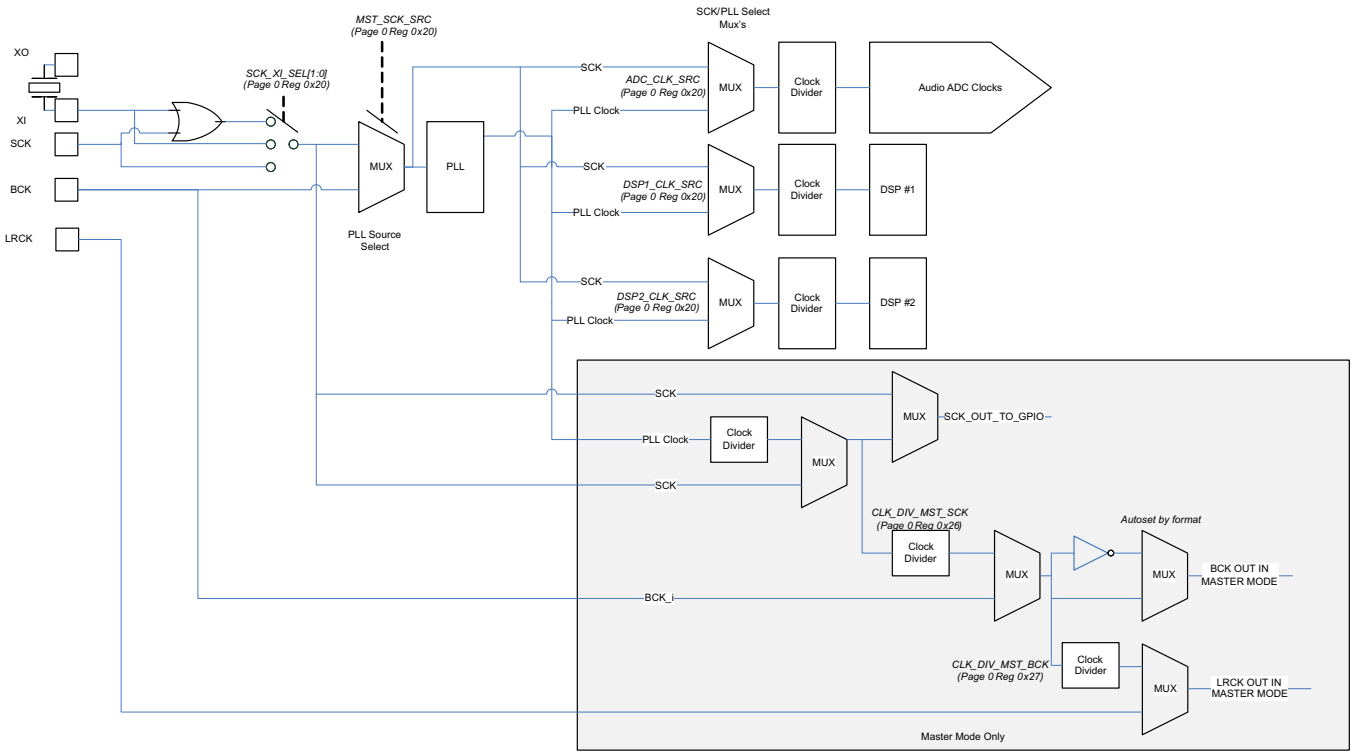



**Figure 29. PLL Clock Source and Clock Distribution**

### *10.11.4.3 PCM1865-Q1 Software Programmable Device Clocking Configuration and Selection*

#### 10.11.4.3.1 Configuration of Master Mode

If an external, high quality MCLK is available (either on the SCK pin or XTAL), then the PCM1865-Q1 should be configured to run in Master Mode where possible, with the ADC and serial ports being driven from the MCLK/SCK source. The on-chip DSPs will continue to require clocks from the PLL, as they run from a much higher clock rate.

Clock MUXs and overall configuration can be done in register Page0, 0x20. For the best performance in master mode, where possible, the automatic clock configuration circuitry will configure the clocks as shown in , depending on if the device is a PCM1865-Q1 software programmable device. The tables below show data at 48kHz multiples, the ratios for multiples of 44.1kHz are identical, while the absolute MHz values will be multiples of 44.1kHz instead of 48kHz.

This automatic configuration can be bypassed using registers, starting from **CLKDET_EN (Page.0, 0x20).**


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## Table 8. Clock Divider and Source Control with External SCK

| $f_S$ | SCK Ratio | SCK Frequency (MHz) | PLL Ratio | PLL Frequency (MHz) | PLL Configuration | DSP1 Clock (MHz) | DSP1 Clock | | DSP 2 Clock (MHz) | DSP2 Clock | | ADC Clock (MHz) | ADC Clock | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Source | Divider | | Source | Divider | | Source | Divider |
| 8 kHz | 128 | 1.024 | 12288 | 98.304 | P=0,R=1, J=48, D=0 | 2.048 | PLL | 48 | 2.048 | PLL | 48 | 1.024 | PLL | 96 |
| | 256 | 2.048 | 12288 | 98.304 | P=0,R=1, J=24, D=0 | 2.048 | SCK | 1 | 2.048 | SCK | 1 | 1.024 | SCK | 2 |
| | 384 | 3.072 | 12288 | 98.304 | P=0,R=1, J=16, D=0 | 2.048 | SCK | 1 | 2.048 | SCK | 1 | 1.024 | SCK | 3 |
| | 512 | 4.096 | | off | | 2.048 | SCK | 2 | 2.048 | SCK | 2 | 1.024 | SCK | 4 |
| | 768 | 6.144 | | off | | 3.072 | SCK | 2 | 3.072 | SCK | 2 | 1.024 | SCK | 6 |
| 16 kHz | 128 | 2.048 | 6144 | 98.304 | P=0,R=1, J=24, D=0 | 4.096 | PLL | 24 | 4.096 | PLL | 24 | 2.048 | PLL | 48 |
| | 256 | 4.096 | 6144 | 98.304 | P=0,R=1, J=12, D=0 | 4.096 | SCK | 1 | 4.096 | SCK | 1 | 2.048 | SCK | 2 |
| | 384 | 6.144 | 6144 | 98.304 | P=0,R=1, J=8, D=0 | 6.144 | SCK | 1 | 6.144 | SCK | 1 | 2.048 | SCK | 3 |
| | 512 | 8.192 | | off | | 4.096 | SCK | 2 | 4.096 | SCK | 2 | 2.048 | SCK | 4 |
| | 768 | 12.288 | | off | | 6.144 | SCK | 2 | 6.144 | SCK | 2 | 2.048 | SCK | 6 |
| 48 kHz | 128 | 6.144 | 2048 | 98.304 | P=0,R=1, J=8, D=0 | 12.288 | PLL | 8 | 12.288 | PLL | 8 | 6.144 | PLL | 16 |
| | 256 | 12.288 | 2048 | 98.304 | P=1,R=1, J=8, D=0 | 12.288 | SCK | 1 | 12.288 | SCK | 1 | 6.144 | SCK | 2 |
| | 384 | 18.432 | 2048 | 98.304 | P=2,R=1, J=8, D=0 | 18.432 | SCK | 1 | 18.432 | SCK | 1 | 6.144 | SCK | 3 |
| | 512 | 24.576 | | off | | 12.288 | SCK | 2 | 12.288 | SCK | 2 | 6.144 | SCK | 4 |
| | 768 | 36.864 | | off | | 18.432 | SCK | 2 | 18.432 | SCK | 2 | 6.144 | SCK | 6 |
| 96 kHz | 128 | 12.288 | 1024 | 98.304 | P=3,R=1, J=16, D=0 | 24.756 | PLL | 4 | 24.756 | PLL | 4 | 6.144 | SCK | 2 |
| | 256 | 24.576 | 1024 | 98.304 | P=7,R=1, J=16, D=0 | 24.756 | SCK | 1 | 24.756 | SCK | 1 | 6.144 | SCK | 4 |
| | 384 | 36.864 | 1024 | 98.304 | P=11,R=1, J=16, D=0 | 24.756 | SCK | 1 | 24.756 | SCK | 1 | 6.144 | SCK | 6 |
| | 512 | 49.152 | | off | | 24.756 | SCK | 2 | 24.756 | SCK | 2 | 6.144 | SCK | 8 |
| 192 kHz | 128 | 24.576 | 512 | 98.304 | P=3,R=1, J=8, D=0 | 49.152 | PLL | 2 | 49.152 | PLL | 2 | 6.144 | SCK | 4 |
| | 256 | 49.152 | 512 | 98.304 | P=7,R=1, J=8, D=0 | 49.152 | SCK | 1 | 49.152 | SCK | 1 | 6.144 | SCK | 8 |

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### 10.11.4.4 PCM1865-Q1 BCK Input Slave PLL Mode

The PCM1865-Q1 software programmable devices can generate an internal MCLK system clock using it's PLL (referenced from an external input BCK) in slave mode. BCK must be 64$f_S$. Supported sampling frequencies are listed in Table 9. Whilst the PCM1865-Q1 can support down to 8 kHz, analog performance is not tested at this rate.

**Table 9. Auto PLL BCK Requirements**

| Sampling Frequency | BCK Ratio to LRCK | BCK Frequency |
|---|---|---|
| 8 kHz | 256 | 2.048 |
| 16 kHz | 64 | 1.024 |
| | 256 | 4.096 |
| 48 kHz | 32 | 1.536 |
| | 48 | 2.304 |
| | 64 | 3.072 |
| | 256 | 12.288 |
| 96 kHz | 32 | 3.072 |
| | 48 | 4.608 |
| | 64 | 6.144 |
| | 256 | 24.576 |
| 192 kHz | 32 | 6.144 |
| | 48 | 9.216 |
| | 64 | 12.288 |
| | 256 | 49.152 |

In software SPI/$I^2C$ mode, a PCM1865-Q1 software programmable device can use its on-chip crystal oscillator, if a CMOS clock source is not available. Audio Clocks can be generated through the PLL from the non-audio standard CMOS/Crystal frequency (and then can be divided down as described above). This function is not available in hardware mode.

8 kHz is only supported if an external MCK is provided. The Autodetect and PLL system support frequencies as low as 32 kHz. Analog performance is not tested in this mode.

The clock tree can also be programmed manually, with the settings shown in Table 10.

| $f_S$ | BCK Ratio | BCK Freq. (MHz) | PLL Ratio | PLL Frequency (MHz) | PLL Configuration | DSP1 Clock (MHz) 2CH | DSP1 Clock Divider 2 CH Mode | | DSP 2 Clock (MHz) | DSP2 Clock Divider | | ADC Clock (MHz) | ADC Clock Divider | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Source | Divider | | Source | Divider | | Source | Divider |
| 8 kHz | 256 | 2.048 | 12288 | 98.304 | P=0,R=1, J=24, D=0 | 2.048 | PLL | 48 | 2.048 | PLL | 48 | 1.024 | PLL | 96 |
| 16 kHz | 64 | 1.024 | 6144 | 98.304 | P=0,R=1, J=48, D=0 | 4.096 | PLL | 24 | 4.096 | PLL | 24 | 2.048 | PLL | 48 |
| | 256 | 4.096 | 6144 | 98.304 | P=1,R=1, J=24, D=0 | 4.096 | PLL | 24 | 4.096 | PLL | 24 | 2.048 | PLL | 48 |
| 48 kHz | 32 | 1.536 | 2048 | 98.304 | P=0,R=1, J=32, D=0 | 12.288 | PLL | 8 | 12.288 | PLL | 8 | 6.144 | PLL | 16 |
| | 48 | 2.304 | 2048 | 92.16 | P=0,R=1, J=20, D=0 | 15.36 | PLL | 6 | 15.36 | PLL | 6 | 6.144 | PLL | 15 |
| | 64 | 3.072 | 2048 | 98.304 | P=0,R=1, J=16, D=0 | 12.288 | PLL | 8 | 12.288 | PLL | 8 | 6.144 | PLL | 16 |
| | 256 | 12.288 | 2048 | 98.304 | P=3,R=1, J=16, D=0 | 12.288 | PLL | 8 | 12.288 | PLL | 8 | 6.144 | PLL | 16 |
| 96 kHz | 32 | 3.072 | 1024 | 98.304 | P=0,R=1, J=16, D=0 | 24.576 | PLL | 4 | 24.576 | PLL | 4 | 6.144 | PLL | 16 |


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| $f_S$ | BCK Ratio | BCK Freq. (MHz) | PLL Ratio | PLL Frequency (MHz) | PLL Configuration | DSP1 Clock (MHz) 2CH | DSP1 Clock Divider 2 CH Mode | | DSP 2 Clock (MHz) | DSP2 Clock Divider | | ADC Clock (MHz) | ADC Clock Divider | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Source | Divider | | Source | Divider | | Source | Divider |
| | 48 | 4.608 | 1024 | 98.304 | P=2,R=1, J=32, D=0 | 24.576 | PLL | 4 | 24.576 | PLL | 4 | 6.144 | PLL | 16 |
| | 64 | 6.144 | 1024 | 98.304 | P=1,R=1, J=16, D=0 | 24.576 | PLL | 4 | 24.576 | PLL | 4 | 6.144 | PLL | 16 |
| | 256 | 24.576 | 1024 | 98.304 | P=7,R=1, J=16, D=0 | 24.576 | PLL | 4 | 24.576 | PLL | 4 | 6.144 | PLL | 16 |
| 192 kHz | 32 | 6.144 | 512 | 98.304 | P=1,R=1, J=16, D=0 | 49.152 | PLL | 2 | 49.152 | PLL | 2 | 6.144 | PLL | 16 |
| | 48 | 9.216 | 512 | 98.304 | P=2,R=1, J=16, D=0 | 49.152 | PLL | 2 | 49.152 | PLL | 2 | 6.144 | PLL | 16 |
| | 64 | 12.288 | 512 | 98.304 | P=3,R=1, J=16, D=0 | 49.152 | PLL | 2 | 49.152 | PLL | 2 | 6.144 | PLL | 16 |
| | 256 | 49.152 | 512 | 98.304 | P=15,R=1, J=16, D=0 | 49.152 | PLL | 2 | 49.152 | PLL | 2 | 6.144 | PLL | 16 |

## Table 10. PCM1865-Q1 (4-Channel) PLL BCK Settings

| $f_S$ | BCK Ratio | BCK Freq. (MHz) | PLL Ratio | PLL Frequency (MHz) | PLL Configuration | DSP1 Clock (MHz) 4ch | DSP1 Clock Divider 4 CH Mode | | DSP1 Clock (MHz) 2CH | DSP2 Clock Divider | | ADC Clock (MHz) | ADC Clock Divider | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Source | Divider | | Source | Divider | | Source | Divider |
| 8 kHz | 256 | 2.048 | 12288 | 98.304 | P=0,R=1, J=24, D=0 | 4.096 | PLL | 24 | 2.048 | PLL | 48 | 1.024 | PLL | 96 |
| 16 kHz | 64 | 1.024 | 6144 | 98.304 | P=0,R=1, J=48, D=0 | 8.192 | PLL | 12 | 4.096 | PLL | 24 | 2.048 | PLL | 48 |
| | 256 | 4.096 | 6144 | 98.304 | P=1,R=1, J=24, D=0 | 8.192 | PLL | 12 | 4.096 | PLL | 24 | 2.048 | PLL | 48 |
| 48 kHz | 32 | 1.536 | 2048 | 98.304 | P=0,R=1, J=32, D=0 | 24.576 | PLL | 4 | 12.288 | PLL | 8 | 6.144 | PLL | 16 |
| | 48 | 2.304 | 2048 | 92.16 | P=0,R=1, J=20, D=0 | 30.72 | PLL | 3 | 15.36 | PLL | 6 | 6.144 | PLL | 15 |
| | 64 | 3.072 | 2048 | 98.304 | P=0,R=1, J=16, D=0 | 24.576 | PLL | 4 | 12.288 | PLL | 8 | 6.144 | PLL | 16 |
| | 256 | 12.288 | 2048 | 98.304 | P=3,R=1, J=16, D=0 | 24.576 | PLL | 4 | 12.288 | PLL | 8 | 6.144 | PLL | 16 |
| 96 kHz | 32 | 3.072 | 1024 | 98.304 | P=0,R=1, J=16, D=0 | 49.152 | PLL | 2 | 24.576 | PLL | 4 | 6.144 | PLL | 16 |
| | 48 | 4.608 | 1024 | 98.304 | P=2,R=1, J=32, D=0 | 49.152 | PLL | 2 | 24.576 | PLL | 4 | 6.144 | PLL | 16 |
| | 64 | 6.144 | 1024 | 98.304 | P=1,R=1, J=16, D=0 | 49.152 | PLL | 2 | 24.576 | PLL | 4 | 6.144 | PLL | 16 |
| | 256 | 24.576 | 1024 | 98.304 | P=7,R=1, J=16, D=0 | 49.152 | PLL | 2 | 24.576 | PLL | 4 | 6.144 | PLL | 16 |
| 192 kHz | 32 | 6.144 | 512 | 98.304 | P=1,R=1, J=16, D=0 | 98.304 | PLL | 1 | 49.152 | PLL | 2 | 6.144 | PLL | 16 |
| | 48 | 9.216 | 512 | 98.304 | P=2,R=1, J=16, D=0 | 98.304 | PLL | 1 | 49.152 | PLL | 2 | 6.144 | PLL | 16 |
| | 64 | 12.288 | 512 | 98.304 | P=3,R=1, J=16, D=0 | 98.304 | PLL | 1 | 49.152 | PLL | 2 | 6.144 | PLL | 16 |
| | 256 | 49.152 | 512 | 98.304 | P=15,R=1, J=16, D=0 | 98.304 | PLL | 1 | 49.152 | PLL | 2 | 6.144 | PLL | 16 |

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#### *10.11.4.5 PCM1865-Q1 Software Programmable Devices ADC Non-Audio MCK PLL Mode*

This mode is mainly used for systems driving TDM ports or systems where the MCK is not related to the audio sampling rate. Examples may be where the Audio ADC needs to share a clock source with the central processor. (This is commonly 12 MHz, 24 MHz or 27 MHz.)

Under these conditions, the automatic configuration register **CLKDET_EN (Page 0, 0x20)** should be set to 0, and the PLL manually configured, using registers **(Page 0, 0x28 - 0x2D)**. See *PCM1865-Q1 Software Programmable Devices Manual PLL Calculation*.

### 10.11.5 PCM1865-Q1 Software Programmable Devices Manual PLL Calculation

The PCM1865-Q1 has an on-chip PLL with fractional multiplication to generate the clock frequency required by the audio ADC, Modulator and Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input supports clocks varying from 1MHz to 50MHz and is register programmable to enable generation of required sampling rates with fine precision.

The PLL by default is enabled because the on-chip fixed function DSPs require high clock rates to complete all various decimation, mixing and level-detection functions. The PLL output clock PLLCK is given by Equation 1: PLL Rate Calculation:

$$PLLCK = \frac{PLLCKIN \times R \times J.D}{P} \text{ or } PLLCK = \frac{PLLCKIN \times R \times K}{P} \quad (1)$$

R = 1, 2, 3, 4, ….. 15, 16
J = 1, 2, 3, 4,...63, and D = 0000, 0001, 0002...9999
K = J.D
P = 1, 2, 3...15

R, J, D, and P are register programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

**Examples:**

If K = 8.5, then J = 8, D = 5000
If K = 7.12, then J = 7, D = 1200
If K = 14.03, then J = 14, D = 0300
If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, *the following conditions must be satisfied:*

1 MHz = (PLLCKIN / P) = 20 MHz
64 MHz < (PLLCK IN × K × R / P) < 100 MHz
1 = J = 63

When the PLL is enabled and D /= 0000, *the following conditions must be satisfied:*

6.667MHz = PLLCLK _IN / P = 20 MHz
64MHz < (PLLCK IN x K x R / P) < 100 MHz
4 = J = 11
R = 1

When the PLL is enabled,

$f_S$ref = (PLLCLK_IN × K × R) / (N × P) :
N is selected so that $f_S$ref × N = PLLCLK_IN × K × R / P is in the allowable range.

**Example:**

MCLK = 12 MHz and $f_S$ref = 44.1 kHz, (N=2048)
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

**Example:**

MCLK = 12 MHz and $f_S$ref = 48.0 kHz, (N=2048)
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920


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The PLL can be programmed via Page 0, Registers 20 thru 24. The PLL can be turned on via Page 0, Register 4, D(0). The variable P can be programmed via Page 0, Register 20, D(3:0). The variable R can be programmed via Page 0, Register 24, D(3:0). The variable J can be programmed via Page 0, Register 21, D(5:0). The variable D is 14-bits and is programmed into two registers. The MSB portion can be programmed via Page 0, Register 22, D(5:0), and the LSB portion is programmed via Page 0, Register 23, D(7:0). The variable D is set when the LSB portion is programmed.

Values are programmed in the registers in Table 11.

**Table 11. PLL Coefficient Registers**

| Register | FUNCTION | BITS |
|---|---|---|
| PLL_EN | PLL enable, Lock Status and PLL Reference | Page 0, Register 0x28 |
| PLL_P | PLL P | Page 0, Register 0x29 |
| PLL_J | PLL J | Page 0, Register 0x2B |
| PLL_Dx | PLL D | Page 0, Register 0x2C (least significant bits) |
| | | Page 0, Register 0x2D (most significant bits) |
| PLL_R | PLL R | Page 0, Register 0x2A |

### 10.11.6 Clock Halt and Error

The PCM1865-Q1 has a clock error detection block inside that continues to monitor the ratio of BCK to LRCK.

If a clock error is detected - such as an unexpected number of BCKs per LRCK, then the device will go into Standby mode, and an interrupt can be configured (software programmable devices) to inform the host.

Should all clocks be stopped going into the device, then the device will shift into Sleep state and begin Energysense Signal Detect Mode.

The status of the halt and error detector can be read from register: **CLK_ERR_STAT (Page.0, 0x75).**

## 10.12 ADCs

### 10.12.1 Main Audio ADCs

The main ADCs in the PCM1865-Q1 are 110dB, 40 kHz bandwidth ADCs that are tightly coupled to dedicated PGAs and input multiplexers. Often in this document, references are made to ADC1L and ADC1R (or CH1_L and CH1_R), the main Left/Right ADCs present in PCM1865-Q1. References to ADC2L and ADC2R are the other pair of L/R ADCs also present.

### 10.12.2 Secondary ADC - Energysense and Analog Control

The PCM1865-Q1 has a secondary ADC which is used for signal level detection or DC level change detection.

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## ADCs (continued)

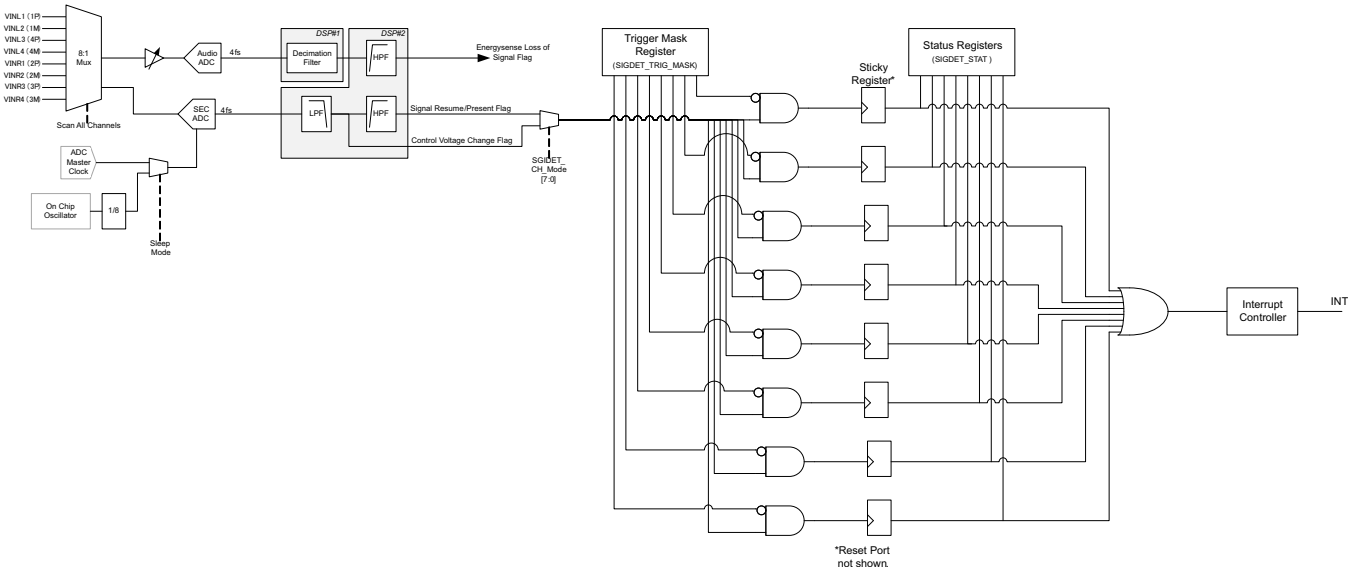



**Figure 30. Secondary ADC Architecture**

The secondary ADC has two main purposes in the PCM1865-Q1. The primary purpose is to act as a low power signal detection system, to aid with system wakeup from sleep. TI calls this functionality "Energysense". Other functionality includes the ability to use any spare analog inputs as "generic" ADC inputs, for connection to simple analog sources, such as voltages from control potentiometers. TI calls this functionality "Controlsense".

The secondary ADC is a one-bit delta-sigma type ADC. The sampling rate is directly connected to the main ADC audio sampling clocks during ACTIVE functionality. When the device is in SLEEP state, then the secondary ADC will switch clock source to an on-chip oscillator. (If there are no other clock sources.)

In sleep mode, the inputs are all treated as single ended inputs. Differential inputs are not supported in this mode, as the PGA would need to be powered up, which would consume more power.

To make the secondary ADC as flexible as possible in both Energysense and Controlsense modes, the following controls and coefficients are available in the register map. More details on each are in the relevant following sections.

- Coefficients for the Low Pass Filter
- Coefficients for the High Pass Filter
- Reference Voltage and Interrupt Voltage Delta for each input in Controlsense mode
- Signal Loss Conditions (Time and Threshold)
- Signal Resume Conditions (Time and Threshold)
- Interrupt behavior (Ping every X ms if host does not clear, for example.)
- Scan time for each single ended input.

#### *10.12.2.1 Secondary ADC Analog Input Range*

To match the dynamic range of the secondary ADC to an incoming line level signal, an overall attenuation is applied to the incoming signal. This attenuation is also present in Controlsense mode. The impact of this is that the secondary ADC in Controlsense mode can only detect control signals up to 1.65 V. Control signals should be appropriately attenuated external to the PCM1865-Q1. This could be easily done by putting a resistor of the same value as a control potentiometer in series.

#### *10.12.2.2 Frequency Response of the Secondary ADC*

The natural response of the secondary ADC is not flat by frequency. However, the frequency response can be flattened, so that all frequencies are equally sensitive to the energystar detector by modifying the LPF/HPF biquads in the DSP.


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## ADCs (continued)

An example of the code required is shown in Table 13.

### 10.12.3 Secondary ADC DC Level Change Detection

This function is used for external analog controls, such as potentiometers to set volume, tone control, or a sensor.

There are two parameters for the DC level change detection. Reference level (REF_LEVEL) and Difference level (DIFF_LEVEL). Each input pin (input 1 through 8) has a different reference and difference level.

Users set a reference point, and a difference point. If the voltage at the control point crosses the difference point then an interrupt is driven from the device. This is useful for filtering out noise, as well as reducing the load on the host processor for controls that tend to be "set and forget" (such as volume).

The data from the secondary ADC can also be streamed out of the device in TDM form and directly from the $I^2C$ register map. **AUXADC_DATA_CTRL (Page.0 0x58)** is used to configure and check the status of the DC detector.

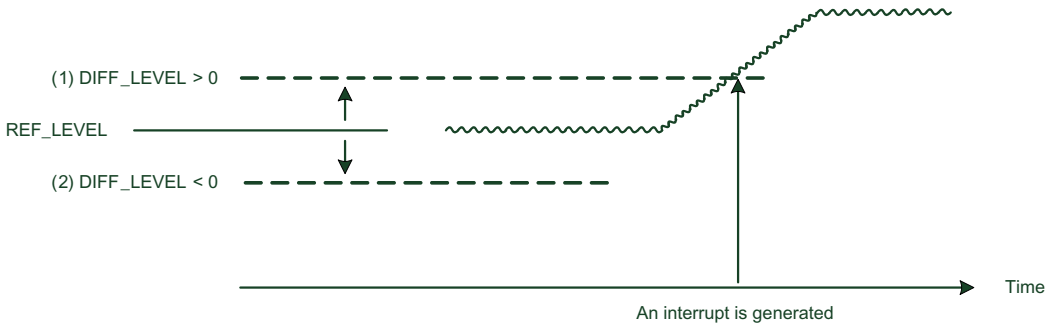



**Figure 31. DC Detection function**

## 10.13 Energysense

Energysense functionality has been added to the PCM1865-Q1 to aid with auto-sleep and auto-wakeup for audio systems that are expected to be sold within the European Union. The latest EcoDesign legislation in Europe has demanded that products consume less than 500 mW in standby. Most off-the-shelf external power adaptors can consume 300mW when idling, leaving the system with only 200 mW available. In many systems that requires that almost everything be powered down in sleep mode, to be powered back up when signal enterers the system again.

Energysense is split into two functions: Signal Loss Flag and Signal Resume Flag. Both are available on the PCM1865-Q1 software controlled devices. Usage is shown below. By default, the Signal Resume Threshold is set at –57 dBFS.

**Table 12. Energysense States**

| MODE | PURPOSE | CONDITIONS | POSITIVE OUTCOME | WORST CASE |
|---|---|---|---|---|
| SLEEP (Signal Detect Mode) | Detect Input Signal and Wake up from SLEEP | BCK and LRCK stopped (not locked) or Register Set. | Host Wakes and services interrupt (reads register) | Host Doesn't respond or start clocks. |
| | | Trigger Interrupt when input crosses above (threshold) | Host Starts BCK/LRCK. (Moving system to ACTIVE mode) or writes to register. | PCM1865-Q1 keeps triggering interrupts until host responds. |
| | | Trigger for 1ms every X seconds until clocks start (x=1 by default) | | |
| ACTIVE (Signal Loss Mode) | Detect content below (threshold) over time | BCK and LRCK are currently running | System can choose to go to sleep or not. If not, reset interrupt | If system does not sleep, remain in Mode 2, and prompt every Y. |
| | Assist system to sleep after audio inactivity (for example, Source is off, but speaker still on) | If no content above -(threshold) dB for Y minutes, drive interrupt. | If System decides to sleep, stop BCK/LRCK. This will move PCM1865-Q1 to SLEEP mode. | MCU will need to mask that interrupt. |

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### 10.13.1 Energysense Signal Loss Flag

The main ADC constantly monitors the input signal level while in ACTIVE mode. Should the input level remain below a register defined threshold (for example –60dB) for a register defined amount of time (for example 1 minute), an interrupt will be generated.

Should the system MCU decide to move to SLEEP mode, the PCM1865-Q1 can be moved to SLEEP by stopping BCK/LRCK or using a register. See Table 12 for detail. If BCK and LRCK are stopped by the Host after the interrupt, the device goes to the sleep state as shown in Figure 32. Otherwise, the device repeats the interrupt every Y minutes as shown in Figure 33. The interrupt can be cleared by reading the status register.

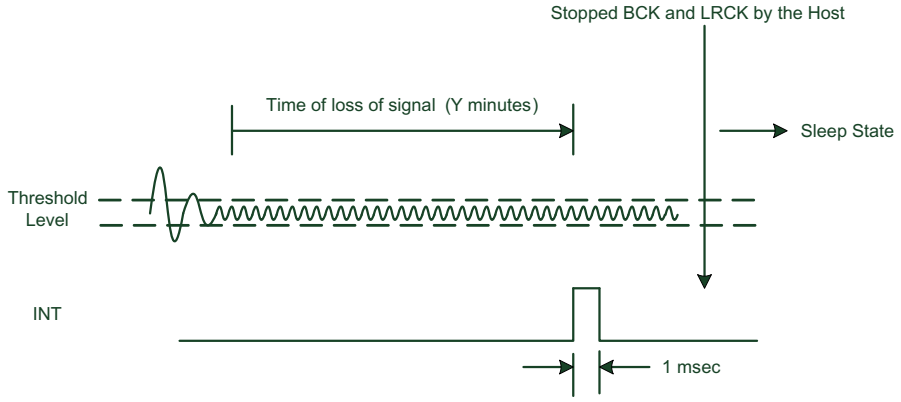



**Figure 32. Energysense Signal Loss**

In a typical application, the host MCU will note and reset this register multiple times until a system sleep number is hit. For example, a 5-minute signal loss could be implemented by using the default 1-minute timeout on the PCM1865-Q1, and counting 5 interrupts. An example can be seen in the diagram below.

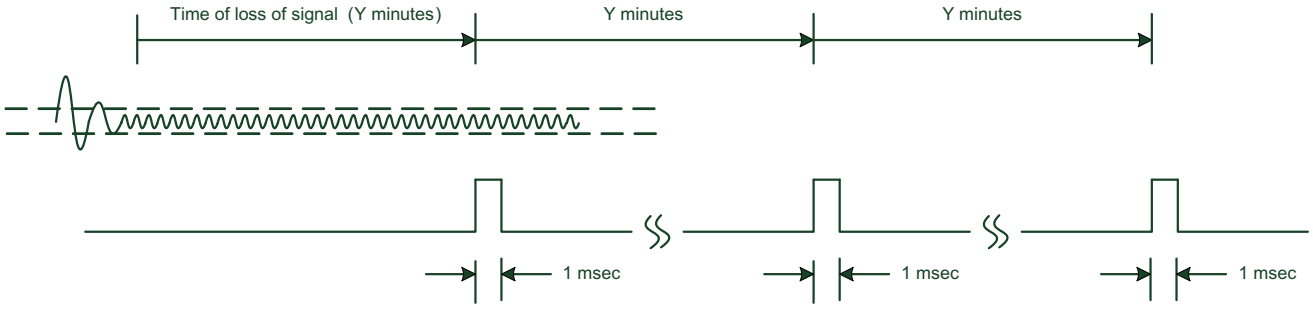



**Figure 33. Interrupt Behavior for Signal Loss.**

Alternatively, the **SIGDET_LOSS_TIME (Page.0, 0x34)** register in the device can be changed from 1 minute (Default) to 5 minutes.

The duration of the interrupt can also be modified using **INT_PLS (Page.0 0x62)** to be pulses or to be a sticky flag until cleared.

### 10.13.2 Energysense Signal Detect Circuitry

In SLEEP mode (BCK and LRCK stop, or by register), the PCM1865-Q1 monitors the signal level or DC level change using the secondary ADC. All 8 channels are converted one after the other in a circular manner. The scan time can be specified with a register SIGDET_SCAN_TIME. All 8 channels will be measured, even if some have their interrupt outputs muted. Accuracy and frequency response are a function of scan time. A long scan time allows detection of lower frequency content.


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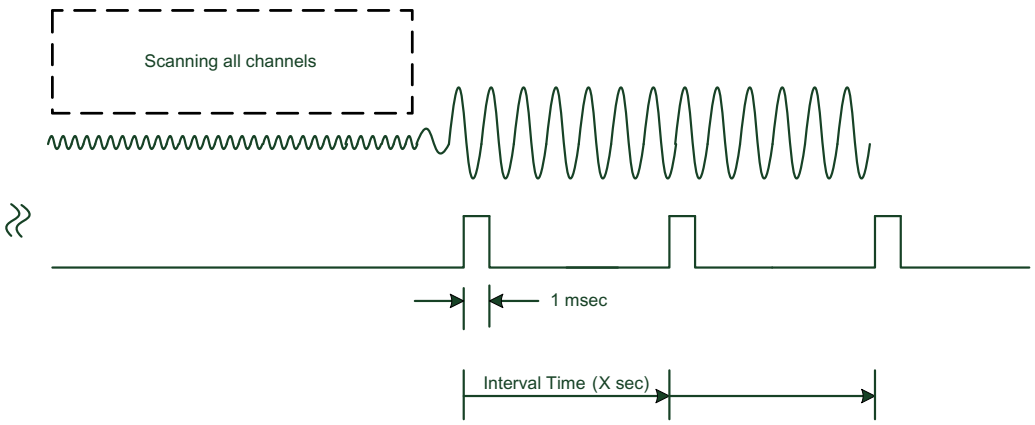



**Figure 34. Energysense Signal Wakeup Logic**

There is a balance between lowest frequency detectable, and time on that particular channel. There are three options in register **SIGDET_INT_INTVL (Page.0 0x36):**

- 50 Hz detect (160 ms per channel)
- 100 Hz detect (80 ms per channel)
- 200 Hz detect (40 ms per channel)

#### *10.13.2.1 Energysense Threshold Levels for both Signal Loss and Signal Detect*

There are two threshold levels used for Energysense. One is the loss of signal level, another one is the resume of signal level.

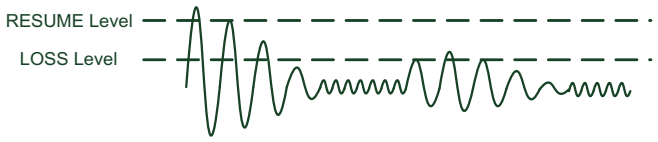



**Figure 35. Dual Thresholds for Energysense**

As both thresholds are DSP based, their coefficients are stored in virtual coefficient space that is programmed through the device register map.

For example, to change the resume threshold value to –30dB (0x040C37):

Write 0x00 0x01 ; # change to register page 1

Write 0x02 0x2D ; # write the memory address of resume threshold

Write 0x04 0x04 ; # bit[23:15]

Write 0x05 0x0C ; # bit[15:8]

Write 0x06 0x37 ; # bit[7:0]

Write 0x01 0x01 ; # execute write operation

### 10.13.3 Programming Various Coefficients for Energysense

Programming the DSP coefficients for the Energysense secondary ADC is done through the indirect virtual programming registers in Page1. The Low Pass Filter (LPF) and High Pass filter (HPF) coefficients can be written to flatten out the frequency response, as well as the Energysense Loss and Resume thresholds. Visually, one can imagine the DSP flow as shown in Figure 36.

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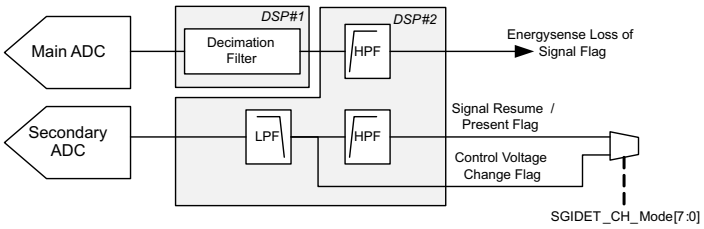



**Figure 36. Energysense Process Flow**

To flatten out the response of the secondary ADC, so that all frequencies are detected evenly, the following biquads should be written to the virtual DSP memory, using the techniques discussed in *Programming DSP Coefficients*.

**Table 13. Secondary ADC Biquad Coefficients at 48kHz Sampling**

| Coefficient | Virtual RAM Address |
|---|---|
| LPF_B0: | 0x20 |
| LPF_B1: | 0x21 |
| LPF_B2: | 0x22 |
| LPF_A1: | 0x23 |
| LPF_A2: | 0x24 |
| HPF_B0: | 0x25 |
| HPF_B1: | 0x26 |
| HPF_B2: | 0x27 |
| HPF_A1: | 0x28 |
| HPF_A2: | 0x29 |

## 10.14 Audio Processing

Both DSP1 and DSP2 are fixed function processors that are not custom-programmable. They are used in this device to perform multiple filtering and mixing functions. Programming the DSP coefficients is done indirectly using registers on Page1. The data and target DSP memory address are stored in registers, and once the DSPs are ready for the data (that is done by request) the data is then latched into the DSP memory.

This indirect method of programming the DSP allows multiple registers to be written, without consuming valuable register map space. More details can be found in the *Programming DSP Coefficients* section.

### 10.14.1 DSP1 Processing Features

#### *10.14.1.1 Digital Decimation Filters*

The decimation filter used to convert the high-data-rate modulator to $I^2S$ rates is selectable between a Classic FIR response and a low-latency IIR response. A high pass filter is also available to remove any DC bias that may be present in the signal.

Details can be found in the **DSP_CTRL** register **(Page.0, 0x71)**.

#### *10.14.1.2 Digital PGA Gain*

As discussed in the *Programmable Gain Amplifier* section, the digital PGA gain can be controlled by the auto gain mapping function, that will use the analog gain settings in register **PGA_VAL_CH1_L (Page.0 0x01)** and related registers to achieve the target gain with a combination of digital and analog gain. However, digital gain can be also controlled directly by disabling the auto gain mapping function using register **PGA_CONTROL_MAPPING (Page.0 0x19)**.


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## Audio Processing (continued)

### 10.14.2 DSP2 Processing Features

#### *10.14.2.1 Digital Mixing Function*

This function allows post ADC mixing, as well as ADC + incoming $I^2S$ mix. Volume control functionality can be performed prior to outputting the signal to an $I^2S$ DAC or Amplifier.

Gain range is from –120 dB to + 18 dB (4.20 format). Phase Inversion can be done by performing the 2's compliment of the positive gain coefficient. 2's compliment can be performed by inverting all bits in the binary coefficient, and adding 1 to the LSB.

As the DSP coefficients are directly written, no soft ramping is available. Use of $I^2S$ receive sacrifices 2 digital mic channels due to pin limitations.

Coefficients are written indirectly to virtual memory addresses using the registers on Page 1. Details of the registers are shown in the *Register Map* section.

A diagram of the digital mixing functionality is shown in Figure 37.

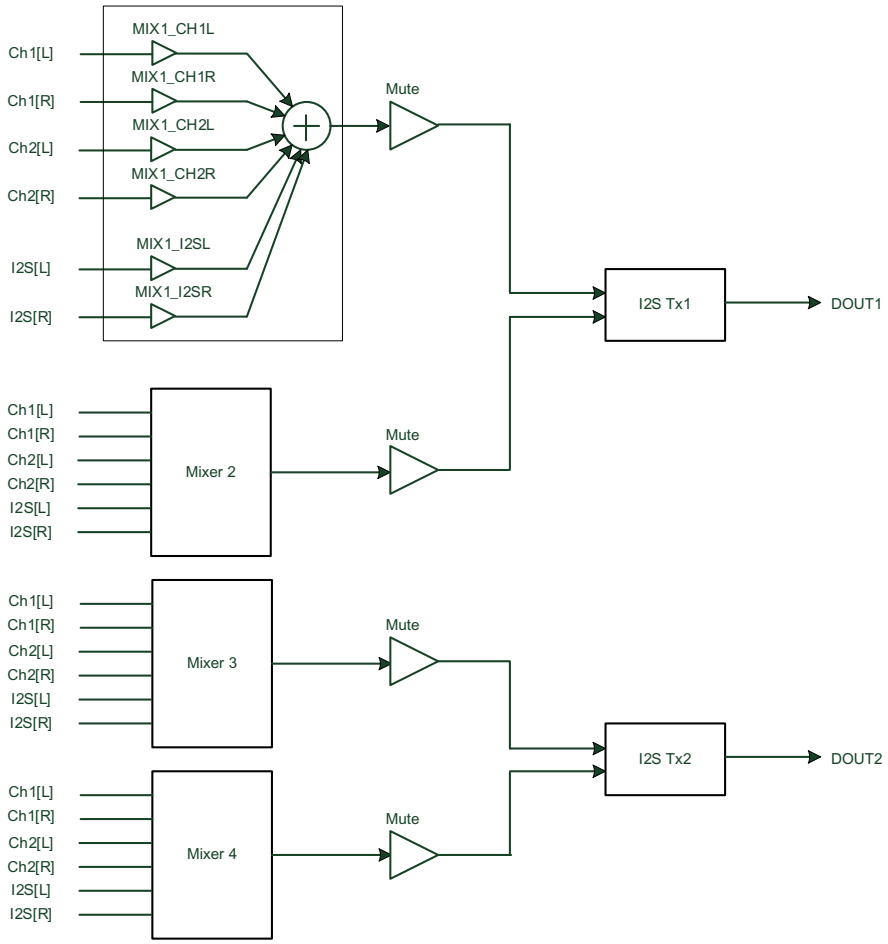



**Figure 37. Digital Mixer Functionality**

## 10.15 Fade-In and Fade-Out Functions

The PCM1865-Q1 has Fade-In and Fade-Out functions on DOUT to avoid pop noise. This function is engaged on device power up/down and mute/unmute. The level changes from 0 dB to mute or mute to 0 dB are performed using pseudo S-shaped characteristics calculation with zero cross detection. Because of the zero cross detection, the time needed for the Fade-In and Fade-Out depends upon the analog input frequency ($f_{IN}$). Fade takes 48 / $f_{IN}$ until processing is completed. If there is no zero cross during 8192 / $f_S$, DOUT is faded in or out by force during 48/$f_S$ (TIME OUT). Figure 38 illustrates the Fade-In and Fade-Out operation processing.

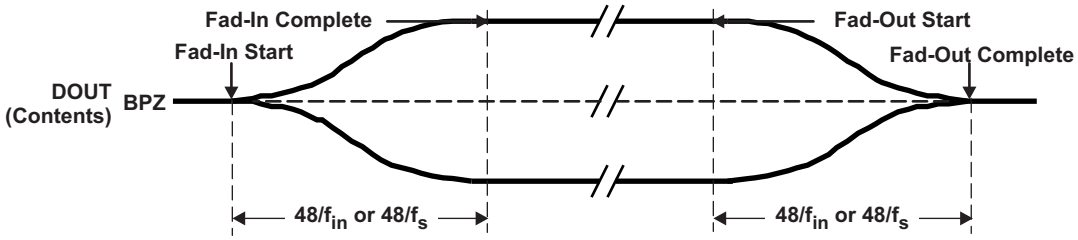



**Figure 38. Fade-In and Fade-Out Operations**

## 10.16 Mappable GPIO Pins

All the GPIO pins on thePCM1865-Q1 software programmable devices can be configured for various functions. They can each have their polarity inverted to make control of following circuits easier. See the control registers for each GPIO for a better explanation of mapping. (such as **GPIO1_FUNC at Page.0 0x10**)

The type of function can also be controlled, including such behavior as regular inputs, inputs with toggle detection, or sticky bits. The device can also be configured as an open drain output, so that multiple interrupt outputs from different devices in the system can be connected together.

## 10.17 Current Status Registers

**Page.0, Registers 0x72 through 0x75 and 0x78** can be used to read the device status at any time. Sample Rate, Power Rail status, Clock Error and Clock Ratios can all be read from these registers.

## 10.18 Control

### 10.18.1 Hardware Control Configuration

PCM1865-Q1 devices require the following functions to be configured on startup. Hardware Programmable devices require a subset of these configurations.

1. Control Interface type and address for PCM1865-Q1 software programmable devices
2. The Clock Mode and Rate (Automatic in Slave Mode, or divider ratio in Master Mode) (For more details see the *Clocks* section.)
3. The Interface Audio Data Format
4. Digital Filter Selection (FIR or IIR) (requires a power cycle to change)
5. Analog Input Channels and PGA Gain

### 10.18.2 Software Controlled Device Configuration

PCM1865-Q1 software programmable devices are configured and controlled by using either $I^2C$ or SPI using MD0.

**Table 14. MD0 - Control Protocol Select**

| MD0 | Control Protocol |
|---|---|
| Low (or floating) | $I^2C$ Mode |
| High | SPI Mode |


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**Table 15. MD1 - I²C Address or SPI Chip Select**

| Mode | MD1 Usage | Static MD1 Value | Configuration |
|---|---|---|---|
| I²C | Address pin | Low | I²C Address: 0x94 |
| I²C | Address pin | High | I²C Address: 0x96 |
| SPI | MS (SPI Chip Select) | N/A | N/A |

### 10.18.3 SPI Interface

The SPI interface is a 4-wire synchronous serial port which operates asynchronously to the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers.

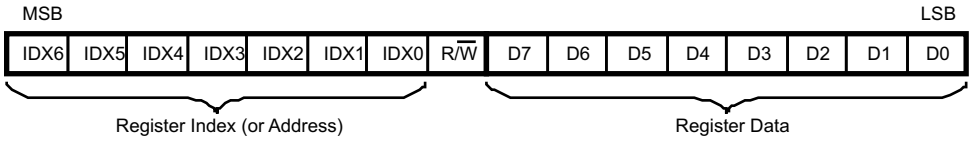
The control interface includes MISO, MOSI , MC, and MS. MISO (Master In Slave Out) is the serial data output, used to read back the values of the mode registers; MOSI (Master Out Slave In) is the serial data input, used to program the mode registers.

MC is the serial bit clock, used to shift data in and out of the control port on the MC falling edge. MS is the active-low mode control enable, used to enable the internal mode register access. If data from the device is not required, the MISO pin can be assigned to GPIO1 by register control.

#### *10.18.3.1 Register Read/Write Operation*

All read/write operations for the serial control port use 16-bit data words. Figure 39 shows the control data word format. The most significant bit is the read/write (R/W) bit. For write operations, the bit must be set to 0. For read operations, the bit must be set to 1. There are seven bits, labeled IDX[6:0], that hold the register index (or address) for the read and write operations. The least significant eight bits, D[7:0], contain the data to be written to, or the data that was read from, the register specified by IDX[6:0].

Figure 40 and Figure 41 show the functional timing diagram for writing or reading through the serial control port. MS should be held at logic 1 state until a register needs to be written or read. To start the register write or read cycle, MS should be set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MOSI and readback data on MISO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MISO during the read operation. After the sixteenth clock cycle has completed, the data is latched into the indexed-mode control register during the write operation. To write or read subsequent data, MS should be set to logic 1 once.




NOTE: B8 is used for selection of “Write” or “Read”. Setting = 0 indicates a “Write”, while = 1 indicates a ”Read”. Bits 15–9 are used for register address. Bits 7–0 are used for register data.

**Figure 39. Control Data Word Format for MDI**

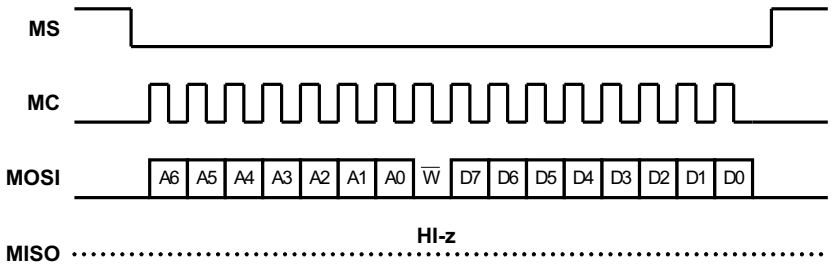



**Figure 40. Serial Control Format for Write**

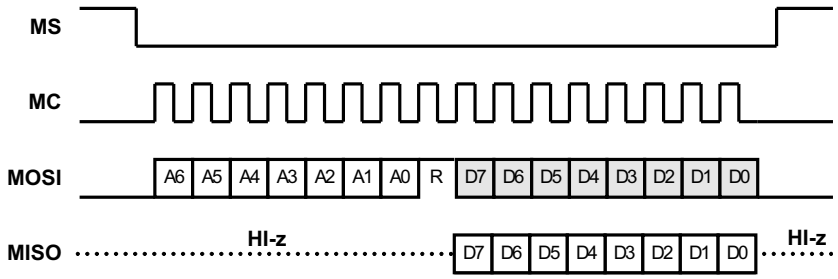



**Figure 41. Serial Control Format for Read**


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### 10.18.4 I²C Interface

The PCM1865-Q1 software programmable devices support the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device. This protocol is explained in I²C specification 2.0.

In I²C mode, the control pins are changed as follows:

**Table 16. I²C Pins and Functions**

| PIN NAME | PIN NUMBER | PROPERTY | DESCRIPTION |
|---|---|---|---|
| SDA | 15 | Input / Output | I²C Data |
| SCL | 16 | Input | I²C Clock |
| AD | 14 | Input | I²C Address 1 |

#### *10.18.4.1 Slave Address*

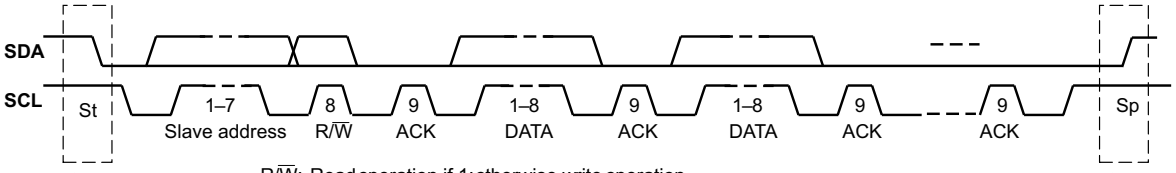
**Table 17. I²C Slave Address**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 1 | AD | R/$\overline{W}$ |

The PCM1865-Q1 software programmable devices have a 7-bit slave address. The first six bits (MSBs) of the slave address are factory preset to 1001 01. The next bit of the address byte is the device select bit, which can be user-defined by the AD pin. A maximum of two PCM1865-Q1 devices can be connected on the same bus at one time. Each device responds when it receives its own slave address.

#### *10.18.4.2 Packet Protocol*

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The PCM1865-Q1 software programmable devices support only slave receivers and slave transmitters.




**write operation**

| Transmitter | *M* | *M* | *M* | *S* | *M* | *S* | *M* | *S* | | *S* | *M* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Data Type | St | slave address | R/$\overline{W}$ | ACK | DATA | ACK | DATA | ACK | ---------- | ACK | Sp |

**read operation**

| Transmitter | *M* | *M* | *M* | *S* | *M* | *S* | *M* | *S* | | *S* | *M* |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Data Type | St | slave address | R/$\overline{W}$ | ACK | DATA | ACK | DATA | ACK | ---------- | ACK | Sp |

*M: Master Device* *S: Slave Device*
St: Start Condition Sp: Stop Conditiion

**Figure 42. Basic I²C Framework**

## 10.19 Interrupt Controller

The Software controlled devices have multiple signals that can be mapped to the interrupt outputs. These include:

- Energysense (DEFAULT)
- Secondary ADC Controlsense Interrupt

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## Interrupt Controller (continued)

- Clock Error
- DIN Toggle

The Interrupt controller has the following features

- The Interrupt sources can be filtered by the enable register (INT_EN).
- The Interrupt flags can be monitored by reading the status register (INT_STAT).
- The interrupt flags can be cleared by writing the status register.
- The polarity of the interrupt signal can be changed between active high, active low and Open Collector (High Impedance is pulled to GND) (INT_PLS).
- The pulse width of the interrupt signal can be changed between 1ms, 2ms, 3ms and Infinity (until the flag is cleared).

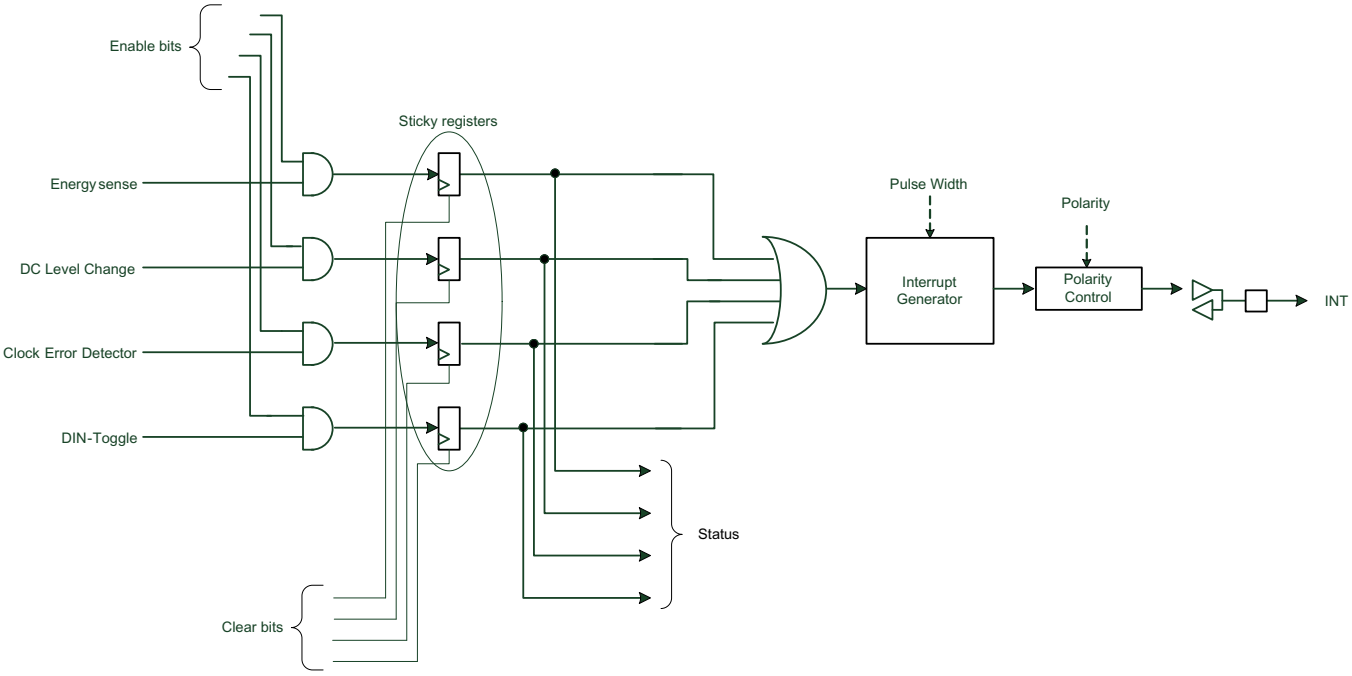



**Figure 43. Interrupt Logic**

Using a combination of these features, as well as the interrupt sources, allows the PCM1865-Q1 to alert a host microcontroller of an event, using whichever polarity signal required (Pull High, Pull Low, Hiz-Open Collector). The Host controller can then communicate with the device to poll the interrupt flag register to find out "what happened". Additional registers can then be read for more details. (For instance, which input triggered an Energysense event.)

### 10.19.1 Clock Error Detect

When a clock error occurs, the PCM1865-Q1 starts the following sequence:

1. Mute audio output immediately (without volume ramp down)
2. Generate an interrupt if the clock error interrupt is enabled
3. Wait until proper clock is supplied (Known as "Clock Waiting State")
4. Restart the clock detection. The PLL and all clock dividers are reconfigured with the result of the detection.
5. Start Fade-IN

The clock error status can be read in register **CLK_ERR_STAT (Page.0 0x20)**. The clock detection logic is shown below:


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## Interrupt Controller (continued)

**Table 18. Summary of Clock Detection Logic**

| SCK | BCK | LRCK | Result | Action |
|---|---|---|---|---|
| ACTIVE | ACTIVE | ACTIVE | No Error | Normal Operation |
| ACTIVE | ACTIVE | HALT | Clock Error | Enter Clock Waiting State |
| ACTIVE | HALT | ACTIVE | Clock Error | Enter Clock Waiting State |
| ACTIVE | HALT | HALT | Clock Error | Enter SLEEP |
| HALT | ACTIVE | ACTIVE | No Error | Enter BCK PLL Mode |
| HALT | ACTIVE | HALT | Clock Error | Enter Clock Waiting State |
| HALT | HALT | ACTIVE | Clock Error | Enter Clock Waiting State |
| HALT | HALT | HALT | Clock Error | Enter SLEEP |

In addition, the device uses an on-chip oscillator to detect errors in the rate of present clocks. That logic is shown below:

**Table 19. Summary of Clock Error Logic**

| SCK/LRCK Ratio | BCK/LRCK Ratio | LRCK | Error Detect | Action |
|---|---|---|---|---|
| - | - | < 8kHz or > 192kHz | $f_S$ error | Enter Clock Waiting State |
| Not 128 / 256 / 384 / 512 / 768 | - | 8 / 16 / 32 / 44.1 / 48 kHz | SCK error | Enter the clock waiting state, tie $I^2S$ output to 0 |
| Not 128 / 256 / 384 / 512 | - | 88.2 / 96kHz | SCK error | Enter the clock waiting state, tie $I^2S$ output to 0 |
| Not 128 / 256 | - | 176.4 / 192kHz | SCK error | Enter the clock waiting state, tie $I^2S$ output to 0 |
| | Not 256 / 64 / 48 / 32 | 8 / 16 / 32 / 44.1 / 48 / 88.2 / 96 / 174.6 / 196kHz | BCK error | Enter the clock waiting state, tie $I^2S$ output to 0 |
| | | >192kHz | $f_S$ error | Enter the clock waiting state, tie $I^2S$ output to 0 |

In an application with a non-audio standard SCK coming into the product, the clock error detection on the SCK pin can be ignored by disabling the Auto Clock Detector **(CLKDET_EN Page.0 0x20)**.

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## 10.20 Audio Format Selection and Timing Details

### 10.20.1 Audio Format Selection

On the PCM1865-Q1 software programmable devices, format selection is done with the registers in **I2S_FMT (Page.0 0x0B)**, which offers additional support for Right Justified "RJ" and Time Division Multiplexed data "TDM" for multiple channels.

The PCM1865-Q1 software programmable devices also offer an additional DOUT pin that can be driven through the GPIO pins. For example, see register details at **GPIO1_FUNC (Page.0 0x10).**

### 10.20.2 Serial Audio Interface Timing Details

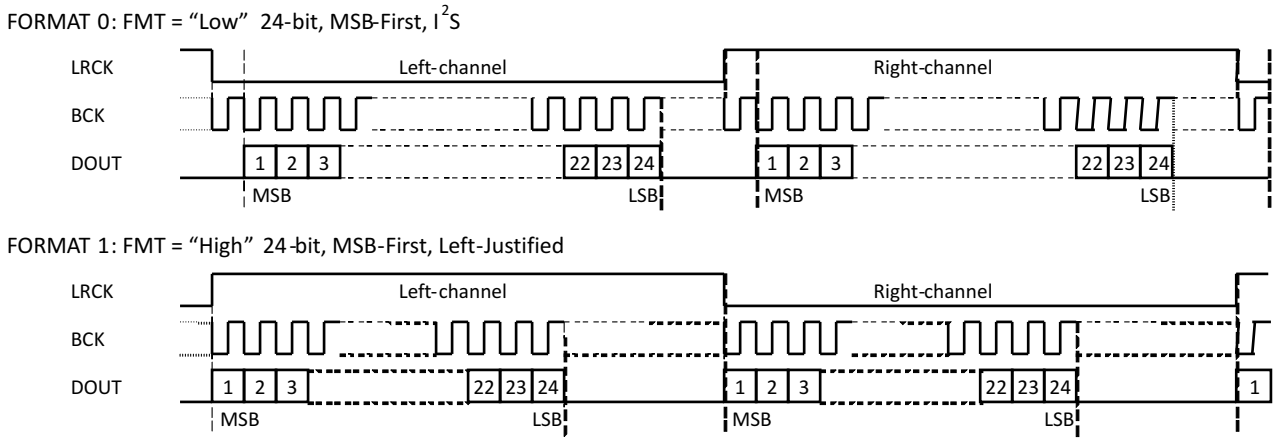



**Figure 44. Audio Data Format**
**(LRCK and BCK work as inputs in slave mode and as outputs in master mode)**

### 10.20.3 Digital Audio Output 2 Configuration

The PCM1865-Q1 software programmable devices offer an additional DOUT through the use of a GPIO that has its rate synchronized with the primary DOUT. DOUT2 is configured using the digital mixer, shown in *Digital Mixing Function*.

### 10.20.4 Decimation Filter Select

The PCM1865-Q1 offers a choice of two different digital filters, a Classic FIR response and a low latency IIR.

### 10.20.5 Serial Audio Data Interface

The PCM1865-Q1 devices interface to the audio system through LRCK, BCK and DOUT.

The PCM1865-Q1 software programmable devices are configured using register **I2S_FMT (Page.0 0x0B)**. **Register I2S_TX_OFFSET (Page.0 0x0D)** should be used when dealing with TDM systems to offset the data transmit.

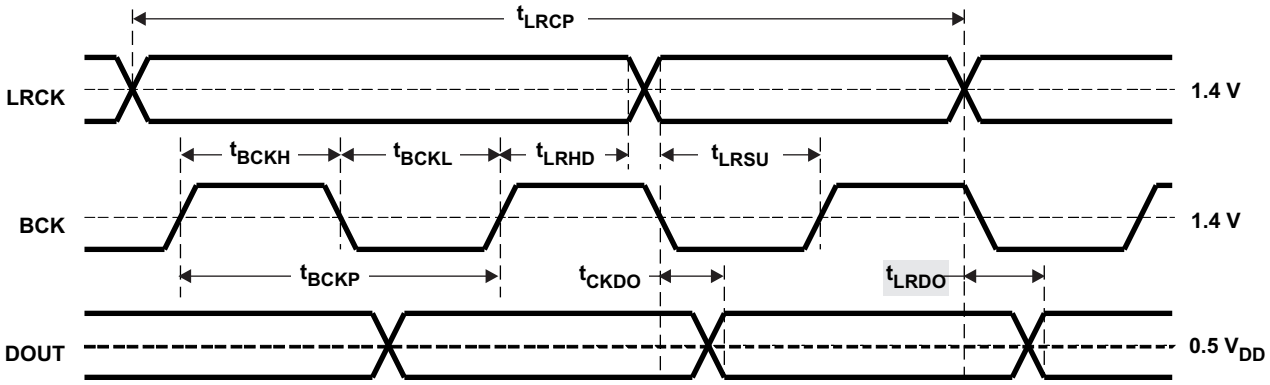
In addition, the offset required for receiving 24-bit data can be programmed using **RX_TDM_OFFSET (P0, R0x0E).**


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## Audio Format Selection and Timing Details (continued)

### *10.20.5.1 Interface Timing*

Figure 45 and Figure 46 illustrate the interface timing in slave mode, and Figure 47 shows master mode.

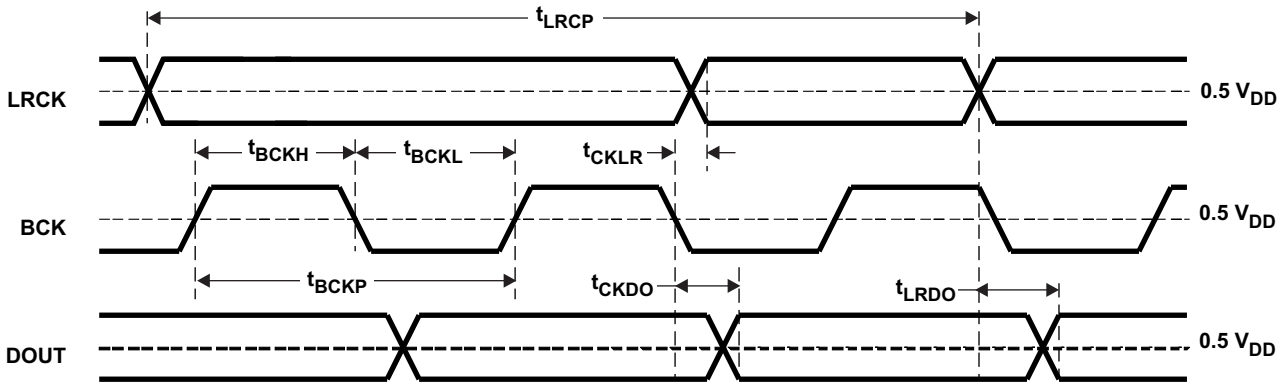



| PARAMETER(1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{BCKP}$ | BCK Period | 1/(64$f_S$) | | | ns |
| $t_{BCKH}$ | BCK Pulse Width HIGH | 1.5 × $t_{SCKI}$ | | | ns |
| $t_{BCKL}$ | BCK Pulse Width LOW | 1.5 × $t_{SCKI}$ | | | ns |
| $t_{LRSU}$ | LRCK Set Up Time to BCK Rising Edge | 50 | | | ns |
| $t_{LRHD}$ | LRCK Hold Time to BCK Rising Edge | 10 | | | ns |
| $t_{LRCP}$ | LRCK Period | 10 | | | µs |
| $t_{CKDO}$ | Delay time BCK Falling Edge to DOUT Valid | –10 | | 40 | ns |
| $t_{LRDO}$ | Delay time LRCK Edge to DOUT Valid | –10 | | 40 | ns |
| $t_R$ | Rise Time of All Signals | | | 20 | ns |
| $t_F$ | Fall Time of All Signals | | | 20 | ns |

(1) Timing measurement reference level is 1.4V for input and 0.5VDD for output. Rise and fall times are measured from 10% to 90% of the IN/OUT signals' swing. Load capacitance of DOUT is 20pF. $t_{SCKI}$ means SCKI period.

**Figure 45. Audio Data Interface Timing (Slave Mode: LRCK and BCK work as inputs)**

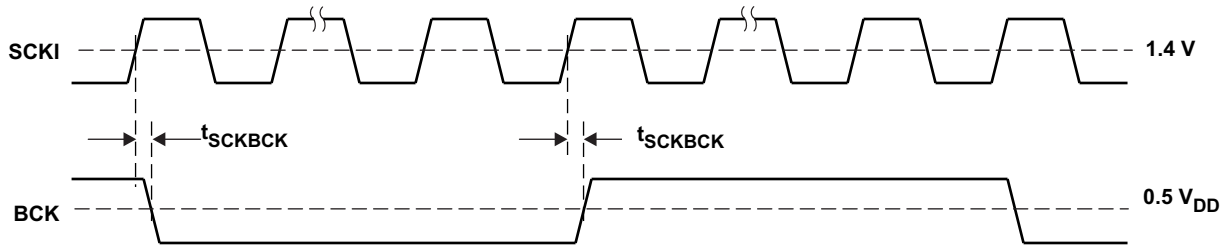
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| PARAMETER(1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{BCKP}$ | BCK Period | 150 | $1/(64f_S)$ | 2000 | ns |
| $t_{BCKH}$ | BCK Pulse Width HIGH | 65 | | 1000 | ns |
| $t_{BCKL}$ | BCK Pulse Width LOW | 65 | | 1000 | ns |
| $t_{CKLR}$ | Delay Time BCK Falling Edge to LRCK Valid | –10 | | 20 | ns |
| $t_{LRCP}$ | LRCK Period | 10 | $1/f_S$ | 125 | µs |
| $t_{CKDO}$ | Delay time BCK Falling Edge to DOUT Valid | –10 | | 20 | ns |
| $t_{LRDO}$ | Delay time LRCK Edge to DOUT Valid | –10 | | 20 | ns |
| $t_R$ | Rise Time of All Signals | | | 20 | ns |
| $t_F$ | Fall Time of All Signals | | | 20 | ns |

(1) Timing measurement reference level is $0.5V_{DD}$. Rise and fall times are measured from 10% to 90% of the IN/OUT signals' swing. Load capacitance of all signals are 20pF.

**Figure 46. Audio Data Interface Timing (Master Mode: LRCK and BCK work as outputs)**




| PARAMETER(1) | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{SCKBCK}$ | Delay Time SCKI Rising Edge to BCK Edge | 5 | | 30 | ns |

(1) Timing measurement reference level is 1.4V for input and 0.5 $V_{DD}$ for output. Load capacitance of BCK is 20pF. This timing is applied when SCKI frequency is less than 25MHz.

**Figure 47. Audio Data Interface Timing (Master Mode: BCK works as outputs)**


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# 11 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The PCM1865-Q1 is extremely flexible, and this flexibility gives rise to a number of design questions that define the design requirements for a given application.

## 11.1 Application Information

In this section, the design choices are described, followed by a typical system implementation. The simplified application diagrams below show a typical system that would require the following architecture decisions to be made.

- *Device Control Method*
  - Software Control (PCM1865-Q1)
    - SPI
    - $I^2C$
- *Power Supply Options*
  - Single supply
  - Separate analog and digital supplies
  - Separate IO supply
- *Master Clock Source*
  - External CMOS-level clock
  - External crystal with integrated oscillator
- *Analog Input Configuration*
  - Single-ended
  - Differential

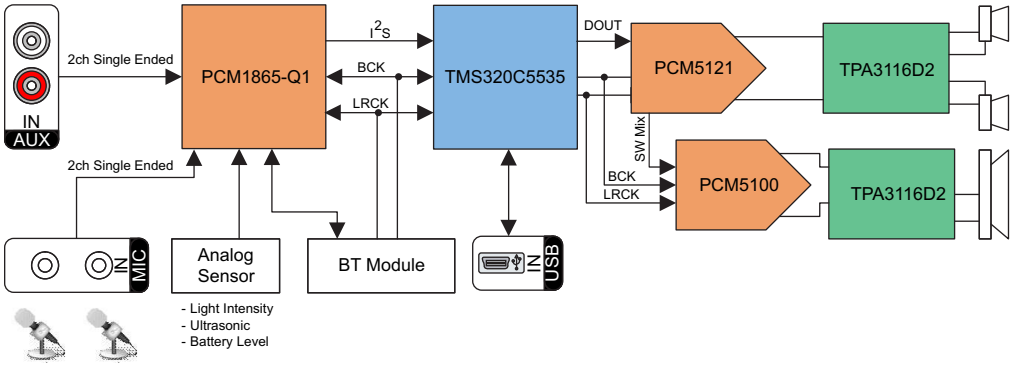



**Figure 48. Example Application Diagram**

### 11.1.1 Device Control Method

#### *11.1.1.1 Software Control*

##### 11.1.1.1.1 SPI Control

SPI control is selected by the MD0 pin; in this case, MDO connects to 3.3V, so that the device acts as an SPI slave.

## Application Information (continued)

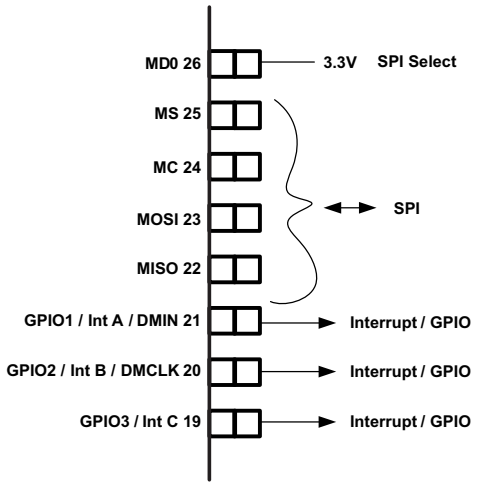



**Figure 49. SPI Control Interface Including Interrupt Signals**

#### 11.1.1.1.2 $I^2C$ Control

$I^2C$ control is selected by the MD0 pin; in this example, MDO is pulled down to ground, so that the device acts as an $I^2C$ slave. One address line is supported to select between two devices on the same bus.

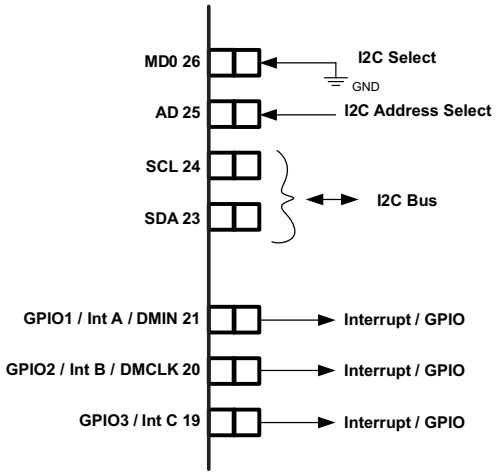



**Figure 50. $I^2C$ Control Interface Including Interrupt Signals**

### 11.1.2 Power Supply Options

#### *11.1.2.1 3.3 V AVDD, DVDD and IOVDD*

*3.3 V AVDD, DVDD and IOVDD* is the most typical power supply configuration.


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## Application Information (continued)

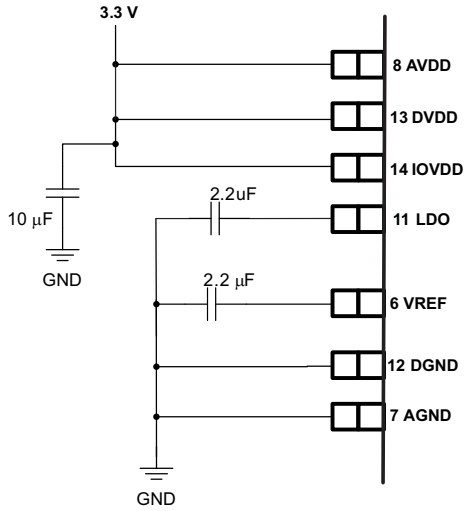



**Figure 51. Single 3.3 V Supply**

#### *11.1.2.2 3.3V AVDD, DVDD, and 1.8V IOVDD*

For details regarding lower power applications, see *3.3V AVDD, DVDD with a 1.8V IOVDD* for lower power applications.

### 11.1.3 Master Clock Source

The PCM1865-Q1 offers 3 different clock sources. For the highest performance, run the ADC in master mode from a stable, well-known SCK source, such as a CMOS SCK, or a external crystal (XTAL). The PCM1865-Q1 is easy to hook up to a crystal, simply connect to XI and XO, and add capacitors to ground, as suggested in the XTAL manufacturer's data sheet (typically 15 pF).

External CMOS clock sources can be brought directly into the SCKI pin (for 3.3 V sources) or into the XI pin (1.8 V sources).

If you have a clock source that is unrelated to the audio rate, then the PLL will need to be enabled. For instance, a 12 MHz USB crystal will require custom PLL settings to generate the 48 kHz rate clocks and the 44.1 kHz rate clocks required by many audio systems. An example with a 12-MHz clock is shown in *PCM1865-Q1 Software Programmable Devices Manual PLL Calculation*.

### 11.1.4 Analog Input Configuration

#### *11.1.4.1 Analog Front-End Circuit For Single-Ended Line-In Applications*

Most systems can simply use an input filter similar to Figure 52. However, for systems with significant out of band noise, a simple filter such as that shown in Figure 53 can be used for pre-ADC anti-aliasing filtering. The recommended resistor value is 100 Ω. Film-type capacitors of 0.01 µF should be located as close as possible to the VINLx and VINRx pins and should be terminated to GND as close as possible to the AGND pin to maximize the dynamic performance of the ADC.




**Figure 52. Analog Input Circuit for Single Ended Input Applications**

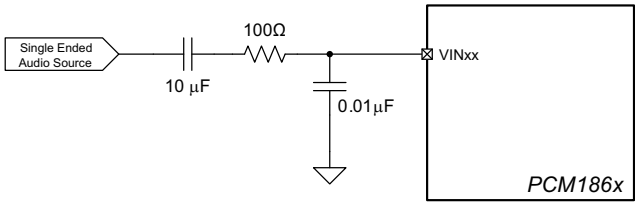



**Figure 53. Analog Input Circuit with Additional Anti Aliasing Filter for Single-Ended Applications**

## Application Information (continued)

### 11.1.4.2 Analog Front-End Circuit Differential Line In Applications

As in single-ended applications, most systems can simply use an input filter similar to Figure 54. However, for systems with significant out of band noise, a simple filter such as that shown in Figure 55 can be used for pre-ADC anti-aliasing filtering. The recommended R value is 47 Ω. Film-type capacitors of 0.01 µF should be located as close as possible to the VINLx and VINRx pins and should be terminated to GND as close as possible to the AGND pin to maximize the dynamic performance of ADC. To maintain common mode rejection, the series resistors should be matched as closely as possible.

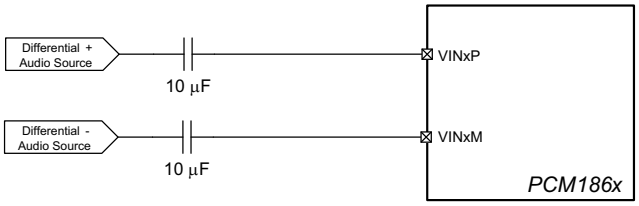



**Figure 54. Analog Input Circuit for Differential Input Applications**

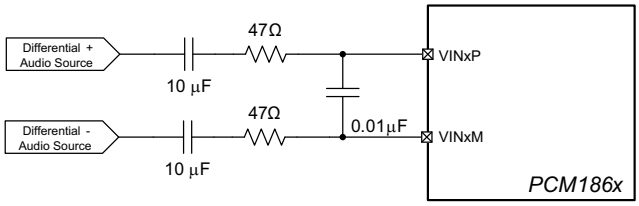



**Figure 55. Differential Input Circuit with Additional Anti Aliasing Filter for Single Ended Applications**

## 11.2 Typical Application


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# 12 Power Supply Recommendations

## 12.1 Power Supply Distribution and Requirements

The PCM1865-Q1 has the following pins used for powering the device.

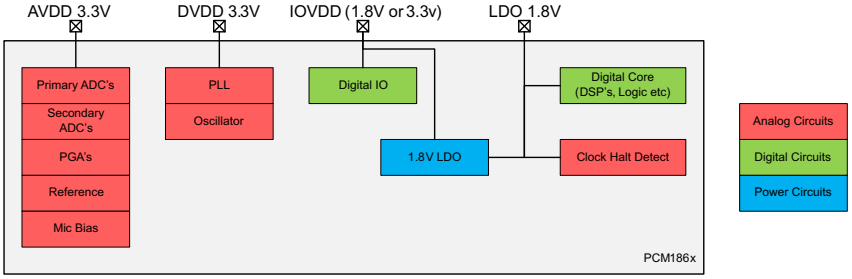



**Figure 56. PCM1865-Q1 Power Distribution Tree**

The PCM1865-Q1 uses a combination of 3.3 V functional blocks and 1.8 V functional blocks to achieve high analog performance, combined with high levels of digital integration. As such, the device has 3 internal power rails. AVDD provides the analog circuits with a clean 3.3V rail. DVDD is used for 3.3 V digital clock circuits. Externally, AVDD and DVDD can be connected together without significant impact to performance.

The PCM1865-Q1 integrates an on-chip LDO to convert an external 3.3 V to 1.8 V required by the digital core. The LDO input is derived from the IOVDD.

**Table 20. Power Supply Pin Descriptions**

| NAME | USAGE / DESCRIPTION |
|---|---|
| AVDD | Analog Voltage Supply - should be 3.3 V. Powers the ADC, PGA, Reference, and Secondary ADC |
| DVDD | Digital Voltage Supply - should be 3.3 V. Used for the PLL and the Oscillator Circuit |
| IOVDD | Input/Output Pin Voltage. Also used as a source for the internal LDO for the digital circuit. |
| LDO | Output from the on-chip LDO. Should be used with a 0.1uF decoupling capacitor. Can be driven (used as power input) with a 1.8 V supply to bypass the on-chip LDO for lower power consumption. |
| AGND | Analog ground |
| DGND | Digital ground |

## 12.2 1.8V Support

All PCM1865-Q1 devices can support external devices with 1.8 V IO. This is configured by driving IOVDD with 1.8 V.

## 12.3 Power Up Sequence

The Power up sequence consists of the following steps

1. Power On Reset
   (a) Power-up AVDD, DVDD and IOVDD
   (b) Check if LDO is being driven with an external 1.8 V, or is an output. Enable LDO if required.
   (c) Release Digital Reset
2. Wait Until Analog Voltage Reference is stable
3. Configure Clock
4. Fade-IN Audio ADC Content

## 12.4 Lowest Power Down Modes

To achieve the lowest levels of power down and sleep current, the following recommended write sequences are suggested on PCM1865-Q1 software programmable devices:

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## Lowest Power Down Modes (continued)

### 12.4.1 Lowest Power In Standby (AVDD=DVDD=IOVDD=3.3V)

Consumption as low as 0.59mW

0x00=0x00 //select page0

0x70=0x14 //power down reference

0x00=0x03 //select page3

0x12=0x41 //disable OSC

0x00=0x00 //select page0

### 12.4.2 Lowest Power In Sleep/Energysense Mode (AVDD=DVDD=IOVDD=3.3V)

Consumption as low as 14mW

Clocks must be running during this process

0x00=0x00 //select page0

0x70=0x72 //enter in sleep mode

0x00=0xfd //select page253

0x14=0x10 //change global bias current

0x00=0x00 //select page0

Now stop the clocks

### 12.4.3 Lower Power In Sleep/Energysense Mode (AVDD=DVDD 3.3V and IOVDD=1.8V)

Consumption as low as 11.15mW

Clocks must be running during this process

0x00=0x00 //select page0

0x70=0x72 //enter in sleep mode

0x00=0xfd //select page253

0x14=0x10 //change global bias current

0x00=0x00 //select page0

stop the clocks (note: make sure the clock IO is 1.8V)


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## 12.5 Power-On Reset Sequencing Timing Diagram

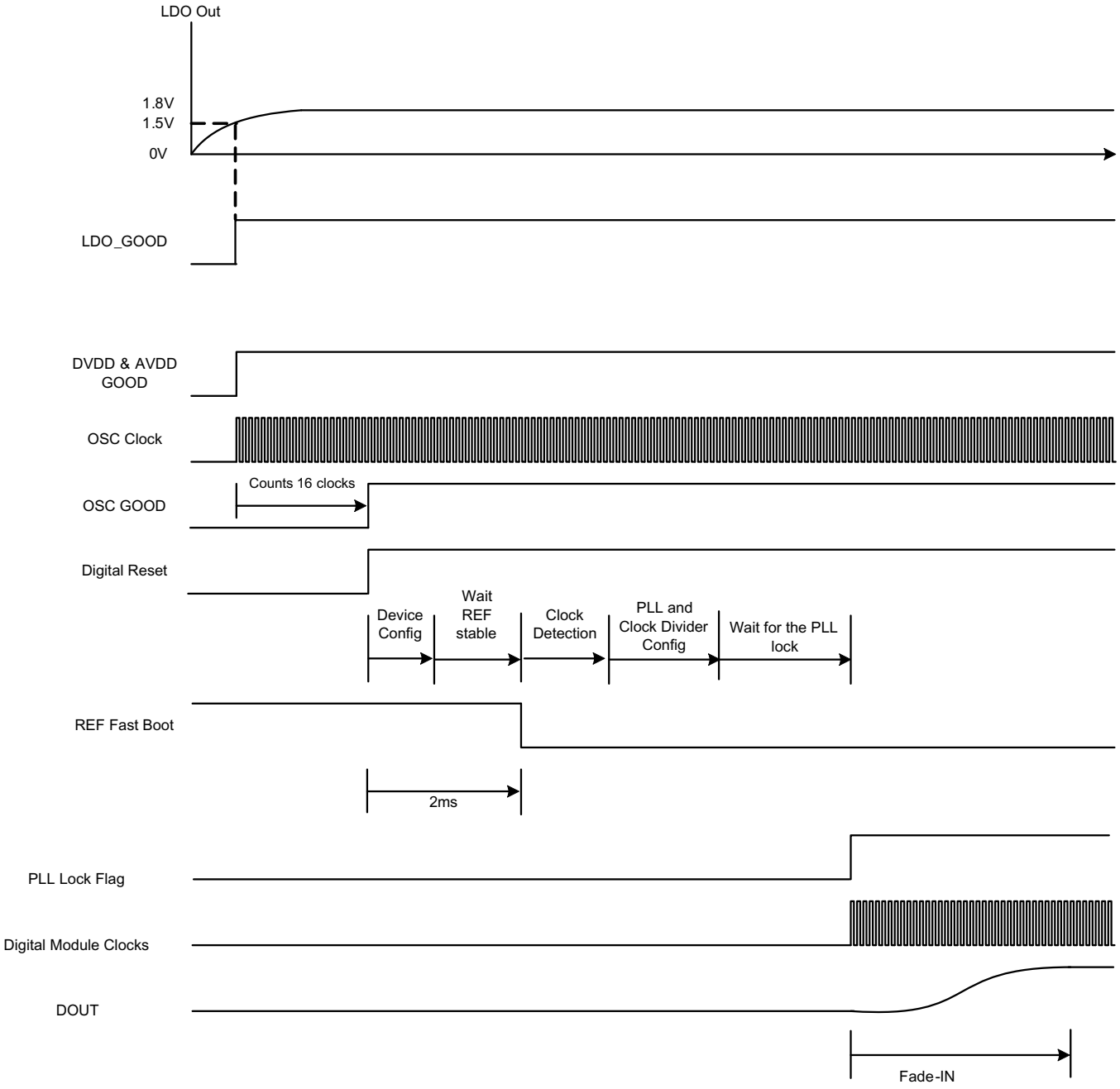



**Figure 57. Power-On Reset Timing Diagram**

## 12.6 Power Connection Examples

### 12.6.1 3.3V AVDD, DVDD, and IOVDD

This is the most typical usage. One single supply, shared between all three supply voltage inputs. Rail-connected decoupling capacitors are not shown. Note; there is no disadvantage in separating the AVDD and DVDD, as the device will wait until both are present before powering up.

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## Power Connection Examples (continued)

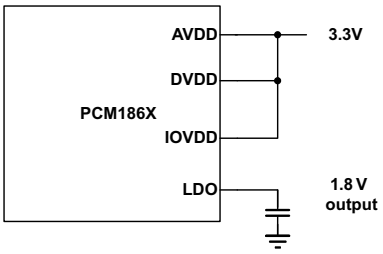



**Figure 58. 3.3 V for All supplies**

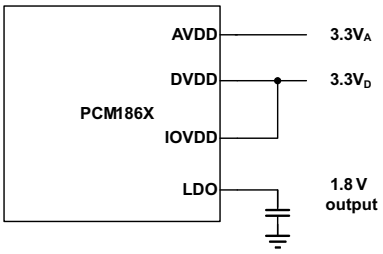



**Figure 59. Separate 3.3 V for AVDD and DVDD**

### 12.6.2 3.3V AVDD, DVDD With a 1.8V IOVDD for Lower-Power Applications

The PCM1865-Q1 also supports interfacing to lower power 1.8 V processors. In the presence of an external 1.8 V connected to LDO, the internal LDO that takes DVDD (3.3 V) and converts it to the 1.8 V core voltage is bypassed. Under such conditions, IOVDD will then be used as the 1.8 V source for the digital core of the device. In such systems, it is still important to have 3.3 V for DVDD, as specific sections of the digital core in the device run from 3.3 V.

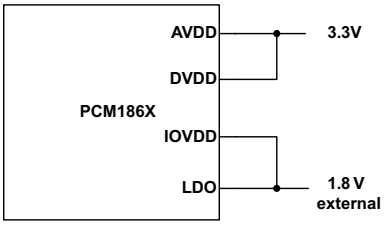



**Figure 60. 1.8V IOVDD with 3.3 V for AVDD and DVDD**

## 12.7 Fade In

This is the final stage of the Power Up Sequence. Once the PLL has locked, The ADC will start running, and the data will follow the Fade-IN sequence according to the following steps:

1. Detect a zero crossing audio input.
2. Increment the volume towards 0 dB with S-shaped volume.
3. Repeat from (1) until arrive at the 0 dB. The number of steps from mute to 0dB is 48 steps.
4. If zero crossing does not occur for 8192 sample times (= time out), change the volume per sample time.


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## Fade In (continued)

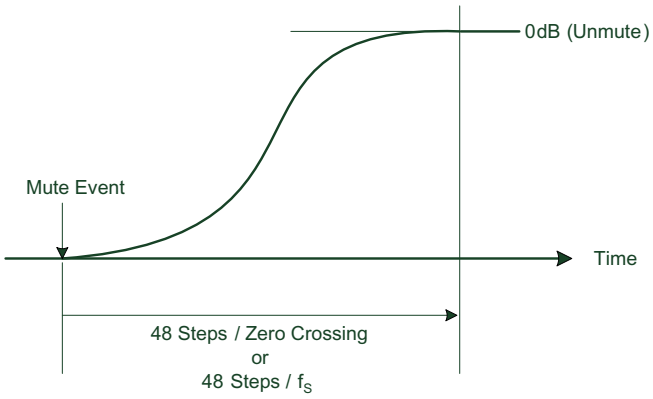



**Figure 61. S-Curve Fade-In Behavior**

# 13 Layout

## 13.1 Layout Guidelines

The PCM1865-Q1 is a relatively simple device to lay out, even on a two layer PCB. The bottom copper plane can be a shared GND, while GND flood can be used on the top plane. For the lowest crosstalk on the inputs, there should be ground planes between the signals coming into the VINxy pins. Decoupling capacitors should be kept as close to the device as possible. Separated grounds aren't needed to achieve data sheet performance, providing analog input traces are kept away from the digital control and clock traces.

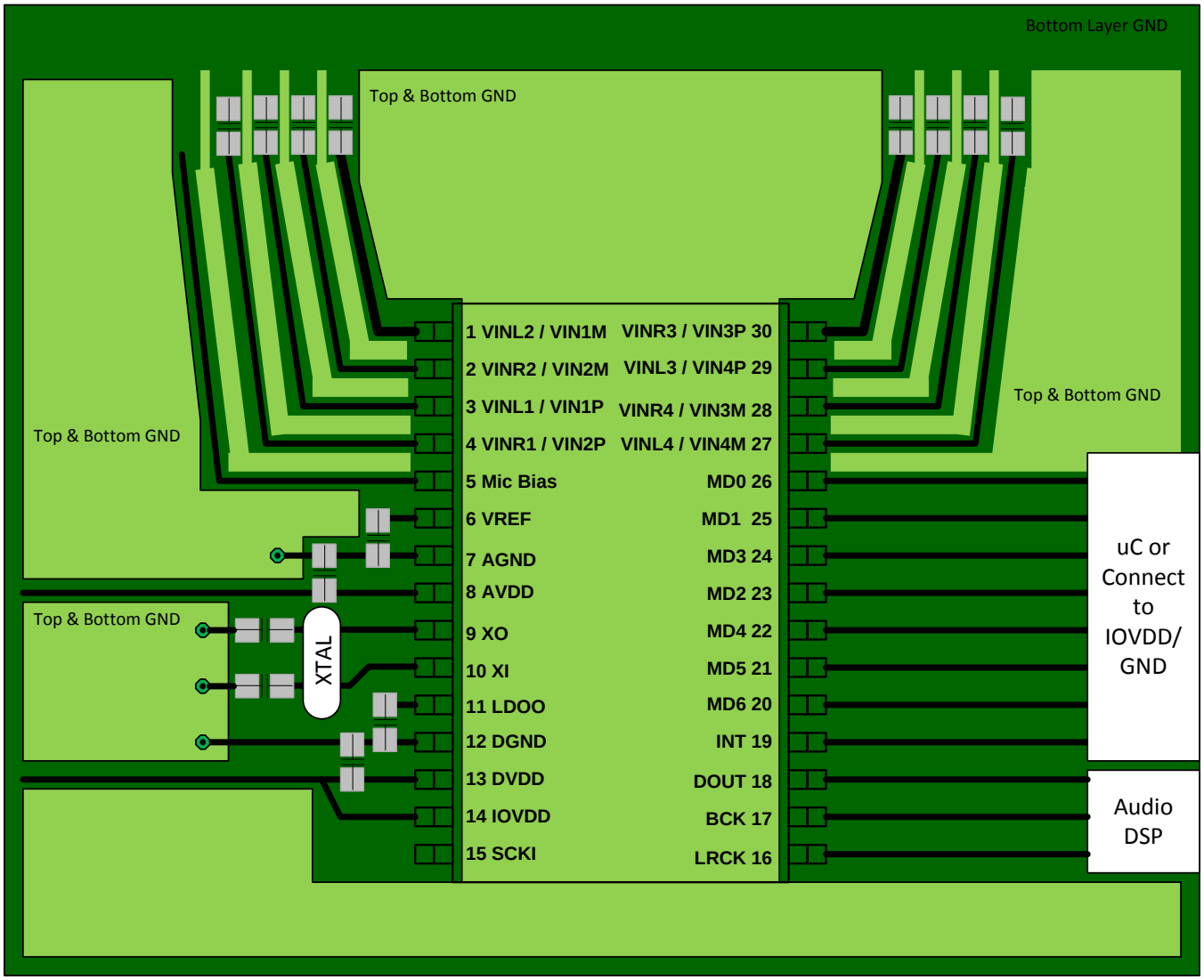



**Figure 62. Suggested Layout for PCM1865-Q1 Devices**

### 13.1.1 Grounding and System Partitioning

Designers should try to use the same ground between AGND and DGND to avoid any potential voltage difference between them. On the PCM1865-Q1 EVM, we achieve up to 110 dB SNR using a single ground plane, and ensuring that the return currents for digital signals do not go near the AGND pin or the input signals. Avoid running high frequency clock and control signals near AGND, or any of the VIN pins where possible.

The pin layout of the PCM1865-Q1 partitions into two parts - analog section and digital section. Providing the system is partitioned in such a way that digital signals are routed away from the analog sections, then no digital return currents (for example, clocks) should be generated in the analog circuitry.


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## Layout Guidelines (continued)

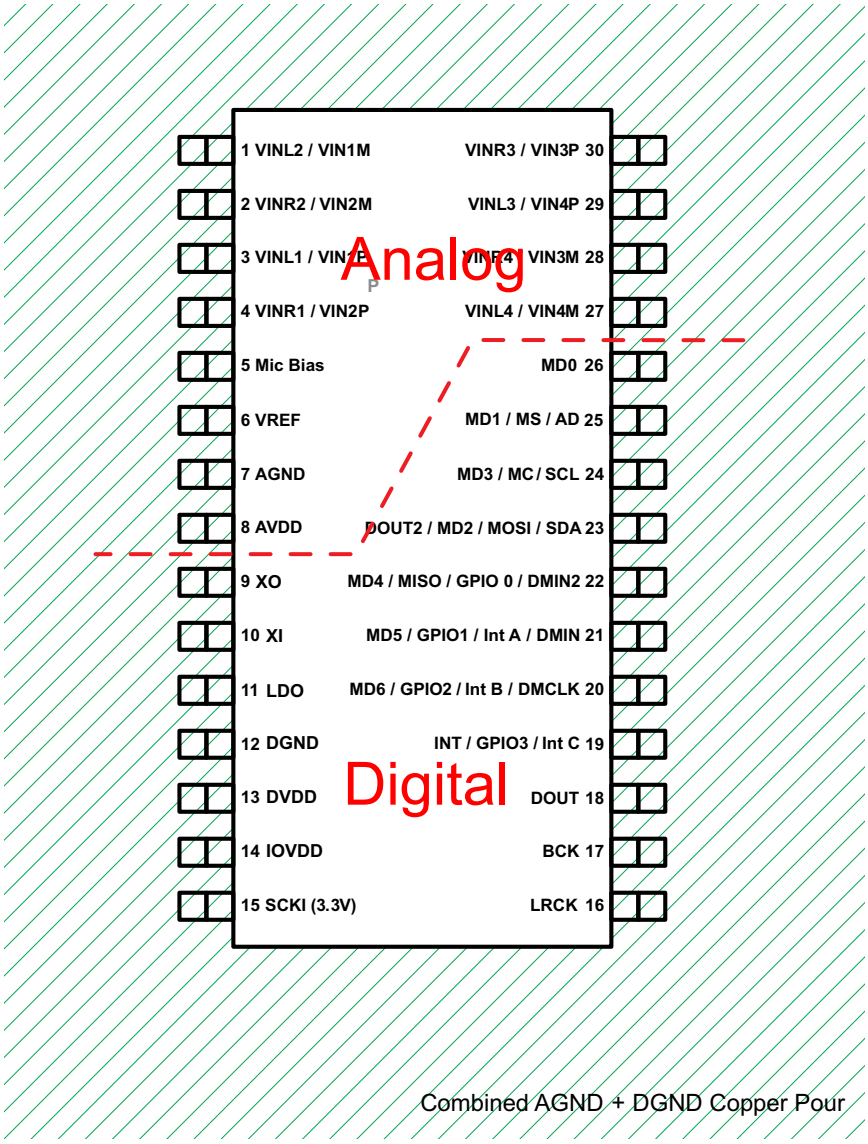



**Figure 63. Single Ground With Analog Partitioned to the Top, Digital at the Bottom**

With this in mind, when we laid out the EVM, we made sure that any digital return currents had a ground plane to their source/destination that did not require passing below any analog circuitry (see Figure 64).

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## 13.2 Layout Example

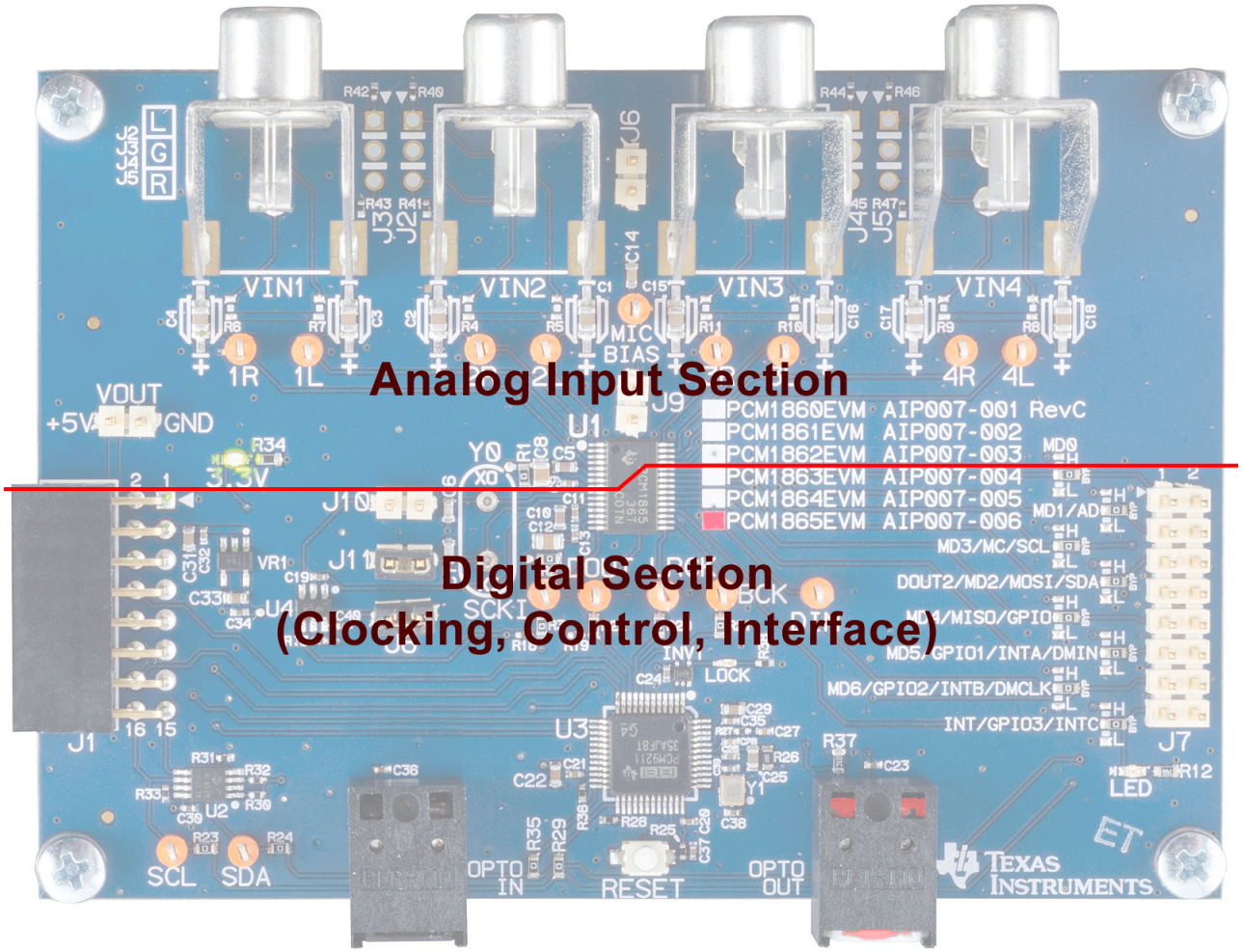



**Figure 64. PCM1865-Q1 EVM Signal Partitioning**


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# 14 Programming and Registers Reference

## 14.1 Coefficient Data Formats

All mixer gain coefficients are 24-bit coefficients using a 4.20 number format. Numbers formatted as 4.20 numbers have 4 bits to the left of the binary point and 20 bits to the right of the binary point.

The most significant bit of the 4.20 number format is the sine bit. It's used, as part of a 2's complement number to invert the phase of that mixer input.

See SLAC663 for a calculator to convert from dB's to the Hexadecimal coefficient required.

## 14.2 Register Map

The register map is the primary way to configure the PCM1865-Q1 software programmable devices. The register map is separated into four pages (Page 0,1,3 and 253). Page 0 handles all of the device configuration whilst Page 1 is used to indirectly program coefficients into the two fixed function DSPs on the IC. Page 3 contains some additional registers for lower power usage along with Page 253. All undocumented registers should be considered reserved and should not be written.

Changing between pages is done by writing to register 0x00 with the page that you want.

Resetting registers is done by writing 0xFF to register 0x00.

### 14.2.1 Register Map Summary

**Register Map Summary**

| Page 0 | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Dec** | **Hex** | **b7** | **b6** | **b5** | **b4** | **b3** | **b2** | **b1** | **b0** |
| 1 | 0x01 | PGA_VAL_CH1_L7 | PGA_VAL_CH1_L6 | PGA_VAL_CH1_L5 | PGA_VAL_CH1_L4 | PGA_VAL_CH1_L3 | PGA_VAL_CH1_L2 | PGA_VAL_CH1_L1 | PGA_VAL_CH1_L0 |
| 2 | 0x02 | PGA_VAL_CH1_R7 | PGA_VAL_CH1_R6 | PGA_VAL_CH1_R5 | PGA_VAL_CH1_R4 | PGA_VAL_CH1_R3 | PGA_VAL_CH1_R2 | PGA_VAL_CH1_R1 | PGA_VAL_CH1_R0 |
| 3 | 0x03 | PGA_VAL_CH2_L | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 4 | 0x04 | PGA_VAL_CH2_R7 | PGA_VAL_CH2_R6 | PGA_VAL_CH2_R5 | PGA_VAL_CH2_R4 | PGA_VAL_CH2_R3 | PGA_VAL_CH2_R2 | PGA_VAL_CH2_R1 | PGA_VAL_CH2_R0 |
| 5 | 0x05 | SMOOTH | LINK | DPGA_CLIP_EN | MAX_ATT1 | MAX_ATT0 | START_ATT1 | START_ATT0 | AGC_EN |
| 6 | 0x06 | POL | RSV | SEL_L5 | SEL_L4 | SEL_L3 | SEL_L2 | SEL_L1 | SEL_L0 |
| 7 | 0x07 | POL | RSV | SEL_R5 | SEL_R4 | SEL_R3 | SEL_R2 | SEL_R1 | SEL_R0 |
| 8 | 0x08 | POL | RSV | SEL_L5 | SEL_L4 | SEL_L3 | SEL_L2 | SEL_L1 | SEL_L0 |
| 9 | 0x09 | POL | RSV | SEL_R5 | SEL_R4 | SEL_R3 | SEL_R2 | SEL_R1 | SEL_R0 |
| 10 | 0x0A | RSV | RSV | RSV | RSV | SEL3 | SEL2 | SEL1 | SEL0 |
| 11 | 0x0B | RX_WLEN1 | RX_WLEN0 | RSV | TDM_LRCK_MODE | TX_WLEN1 | TX_WLEN0 | FMT1 | FMT0 |
| 12 | 0x0C | RSV | RSV | RSV | RSV | RSV | RSV | TDM_OSEL1 | TDM_OSEL0 |
| 13 | 0x0D | TX_TDM_OFFSET7 | TX_TDM_OFFSET6 | TX_TDM_OFFSET5 | TX_TDM_OFFSET4 | TX_TDM_OFFSET3 | TX_TDM_OFFSET2 | TX_TDM_OFFSET1 | TX_TDM_OFFSET0 |
| 14 | 0x0E | RX_TDM_OFFSET7 | RX_TDM_OFFSET6 | RX_TDM_OFFSET5 | RX_TDM_OFFSET4 | RX_TDM_OFFSET3 | RX_TDM_OFFSET2 | RX_TDM_OFFSET1 | RX_TDM_OFFSET0 |
| 15 | 0x0F | DPGA_VAL_CH1_L7 | DPGA_VAL_CH1_L6 | DPGA_VAL_CH1_L5 | DPGA_VAL_CH1_L4 | DPGA_VAL_CH1_L3 | DPGA_VAL_CH1_L2 | DPGA_VAL_CH1_L1 | DPGA_VAL_CH1_L0 |
| 16 | 0x10 | GPIO1_POL | GPIO1_FUNC2 | GPIO1_FUNC1 | GPIO1_FUNC0 | GPIO0_POL | GPIO0_FUNC2 | GPIO0_FUNC1 | GPIO0_FUNC0 |
| 17 | 0x11 | GPIO3_POL | GPIO3_FUNC2 | GPIO3_FUNC1 | GPIO3_FUNC0 | GPIO2_POL | GPIO2_FUNC2 | GPIO2_FUNC1 | GPIO2_FUNC0 |
| 18 | 0x12 | | GPIO1_DIR2 | GPIO1_DIR1 | GPIO1_DIR0 | RSV | GPIO0_DIR2 | GPIO0_DIR1 | GPIO0_DIR0 |
| 19 | 0x13 | | GPIO3_DIR2 | GPIO3_DIR1 | GPIO3_DIR0 | RSV | GPIO2_DIR2 | GPIO2_DIR1 | GPIO2_DIR0 |
| 20 | 0x14 | GPIO3_OUT | GPIO2_OUT | GPIO1_OUT | GPIO0_OUT | GPIO3_IN | GPIO2_IN | GPIO1_IN | GPIO0_IN |
| 21 | 0x15 | PULL_DOWN_DIS[3] | PULL_DOWN_DIS[2] | PULL_DOWN_DIS[1] | PULL_DOWN_DIS[0] | RSV | RSV | RSV | RSV |
| 22 | 0x16 | DPGA_VAL_CH1_R7 | DPGA_VAL_CH1_R6 | DPGA_VAL_CH1_R5 | DPGA_VAL_CH1_R4 | DPGA_VAL_CH1_R3 | DPGA_VAL_CH1_R2 | DPGA_VAL_CH1_R1 | DPGA_VAL_CH1_R0 |
| 23 | 0x17 | DPGA_VAL_CH2_L7 | DPGA_VAL_CH2_L6 | DPGA_VAL_CH2_L5 | DPGA_VAL_CH2_L4 | DPGA_VAL_CH2_L3 | DPGA_VAL_CH2_L2 | DPGA_VAL_CH2_L1 | DPGA_VAL_CH2_L0 |
| 24 | 0x18 | DPGA_VAL_CH2_R7 | DPGA_VAL_CH2_R6 | DPGA_VAL_CH2_R5 | DPGA_VAL_CH2_R4 | DPGA_VAL_CH2_R3 | DPGA_VAL_CH2_R2 | DPGA_VAL_CH2_R1 | DPGA_VAL_CH2_R0 |
| 25 | 0x19 | DPGA_CH2_R | DPGA_CH2_L | DPGA_CH1_R | DPGA_CH1_L | APGA_CH2_R | APGA_CH2_L | APGA_CH1_R | APGA_CH1_L |

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## Register Map (continued)

### Register Map Summary (continued)

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 26 | 0x1A | DIGMIC_IN1_SEL 1 | DIGMIC_IN1_SEL 0 | DIGMIC_IN0_SEL 1 | DIGMIC_IN0_SEL 0 | RSV | RSV | DIGMIC_4CH | DIGMIC_EN |
| 27 | 0x1B | RSV | RSV | 1 | 0 | RSV | RSV | DIN_RESAMP1 | DIN_RESAMP0 |
| 32 | 0x20 | SCK_XI_SEL1 | SCK_XI_SEL0 | MST_SCK_SRC | MST_MODE | ADC_CLK_SRC | DSP2_CLK_SRC | DSP1_CLK_SRC | CLKDET_EN |
| 33 | 0x21 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| 34 | 0x22 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| 35 | 0x23 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| 37 | 0x25 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| 38 | 0x26 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| 39 | 0x27 | DIV_NUM7 | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| 40 | 0x28 | RSV | RSV | RSV | LOCK | RSV | RSV | PLL_REF_SEL | PLL_EN |
| 41 | 0x29 | RSV | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| 42 | 0x2A | RSV | RSV | RSV | RSV | R3 | R2 | R1 | R0 |
| 43 | 0x2B | RSV | RSV | J5 | J4 | J3 | J2 | J1 | J0 |
| 44 | 0x2C | D_LSB | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 45 | 0x2D | RSV | RSV | D_MSB5 | D_MSB4 | D_MSB3 | D_MSB2 | D_MSB1 | D_MSB0 |
| 48 | 0x30 | CH4R | CH4L | CH3R | CH3L | CH2R | CH2L | CH1R | CH1L |
| 49 | 0x31 | CH4R | CH4L | CH3R | CH3L | CH2R | CH2L | CH1R | CH1L |
| 50 | 0x32 | CH4R | CH4L | CH3R | CH3L | CH2R | CH2L | CH1R | CH1L |
| 52 | 0x34 | RSV | RSV | RSV | TIME4 | TIME3 | TIME2 | TIME1 | TIME0 |
| 53 | 0x35 | RSV | RSV | RSV | RSV | RSV | TIME2 | TIME1 | TIME0 |
| 54 | 0x36 | RSV | RSV | RSV | RSV | RSV | INT_INTVL2 | INT_INTVL1 | INT_INTVL0 |
| 64 | 0x40 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 65 | 0x41 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| 66 | 0x42 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| 67 | 0x43 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 68 | 0x44 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| 69 | 0x45 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| 70 | 0x46 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 71 | 0x47 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| 72 | 0x48 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| 73 | 0x49 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 74 | 0x4A | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| 75 | 0x4B | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| 76 | 0x4C | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 77 | 0x4D | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| 78 | 0x4E | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| 79 | 0x4F | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 80 | 0x50 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| 81 | 0x51 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| 82 | 0x52 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 83 | 0x53 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| 84 | 0x54 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| 85 | 0x55 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF2 | REF0 |
| 86 | 0x56 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| 87 | 0x57 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| 88 | 0x58 | DC_NOLATCH | AUXADC_RDY | DC_RDY | AUXADC_LATCH | AUXADC_DATA_ TYPE | DC_CH2 | DC_CH1 | DC_CH0 |
| 89 | 0x59 | AUXADC_DATA_ LSB7 | AUXADC_DATA_ LSB6 | AUXADC_DATA_ LSB5 | AUXADC_DATA_ LSB4 | AUXADC_DATA_ LSB3 | AUXADC_DATA_ LSB2 | AUXADC_DATA_ LSB1 | AUXADC_DATA_ LSB0 |
| 90 | 0x5A | AUXADC_DATA_ MSB7 | AUXADC_DATA_ MSB6 | AUXADC_DATA_ MSB5 | AUXADC_DATA_ MSB4 | AUXADC_DATA_ MSB3 | AUXADC_DATA_ MSB2 | AUXADC_DATA_ MSB1 | AUXADC_DATA_ MSB0 |
| 96 | 0x60 | RSV | RSV | RSV | POSTPGA_CP | CLKERR | DC_CHANG | DIN_TOGGLE | ENGSTR |
| 97 | 0x61 | RSV | RSV | RSV | POSTPGA_CP | CLKERR | DC_CHANG | DIN_TOGGLE | ENGSTR |
| 98 | 0x62 | RSV | RSV | POL1 | POL0 | RSV | RSV | WIDTH1 | WIDTH0 |
| 112 | 0x70 | RSV | RSV | RSV | RSV | RSV | PWRDN | SLEEP | STBY |
| 113 | 0x71 | 2CH | RSV | FLT | HPF_EN | MUTE_CH2_R | MUTE_CH2_L | MUTE_CH1_R | MUTE_CH1_L |


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## Register Map (continued)

**Register Map Summary (continued)**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 114 | 0x72 | RSV | RSV | RSV | RSV | STATE3 | STATE2 | STATE1 | STATE0 |
| 115 | 0x73 | RSV | RSV | RSV | RSV | RSV | INFO2 | INFO1 | INFO0 |
| 116 | 0x74 | RSV | BCK_RATIO2 | BCK_RATIO1 | BCK_RATIO0 | RSV | SCK_RATIO2 | SCK_RATIO1 | SCK_RATIO0 |
| 117 | 0x75 | RSV | LRCKHLT | BCKHLT | SCKHTL | RSV | LRCKERR | BCKERR | SCKERR |
| 120 | 0x78 | | RSV | RSV | RSV | RSV | DVDD | AVDD | LDO |
| **Page 1** | | | | | | | | | |
| **Dec** | **Hex** | **b7** | **b6** | **b5** | **b4** | **b3** | **b2** | **b1** | **b0** |
| 1 | 0x01 | RSV | RSV | RSV | DONE | RSV | BUSY | R_REQ | W_REQ |
| 2 | 0x02 | RSV | MEM_ADDR[6:0]6 | MEM_ADDR[6:0]5 | MEM_ADDR[6:0]4 | MEM_ADDR[6:0]3 | MEM_ADDR[6:0]2 | MEM_ADDR[6:0]1 | MEM_ADDR[6:0]0 |
| 4 | 0x04 | MEM_WDATA_07 | MEM_WDATA_06 | MEM_WDATA_05 | MEM_WDATA_04 | MEM_WDATA_03 | MEM_WDATA_02 | MEM_WDATA_01 | MEM_WDATA_00 |
| 5 | 0x05 | MEM_WDATA_17 | MEM_WDATA_16 | MEM_WDATA_15 | MEM_WDATA_14 | MEM_WDATA_13 | MEM_WDATA_12 | MEM_WDATA_11 | MEM_WDATA_10 |
| 6 | 0x06 | MEM_WDATA_27 | MEM_WDATA_26 | MEM_WDATA_25 | MEM_WDATA_24 | MEM_WDATA_23 | MEM_WDATA_22 | MEM_WDATA_21 | MEM_WDATA_20 |
| 7 | 0x07 | MEM_WDATA_3 | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| 8 | 0x08 | MEM_RDATA_07 | MEM_RDATA_06 | MEM_RDATA_05 | MEM_RDATA_04 | MEM_RDATA_03 | MEM_RDATA_02 | MEM_RDATA_01 | MEM_RDATA_00 |
| 9 | 0x09 | MEM_RDATA_17 | MEM_RDATA_16 | MEM_RDATA_15 | MEM_RDATA_14 | MEM_RDATA_13 | MEM_RDATA_12 | MEM_RDATA_11 | MEM_RDATA_10 |
| 10 | 0x0A | MEM_RDATA_27 | MEM_RDATA_26 | MEM_RDATA_25 | MEM_RDATA_24 | MEM_RDATA_23 | MEM_RDATA_22 | MEM_RDATA_21 | MEM_RDATA_20 |
| 11 | 0x0B | MEM_RDATA_3 | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| **Page 3** | | | | | | | | | |
| **Dec** | **Hex** | **b7** | **b6** | **b5** | **b4** | **b3** | **b2** | **b1** | **b0** |
| 18 | 0x12 | RSV | RSV | RSV | RSV | RSV | RSV | RSV | PD |
| 21 | 0x15 | RSV | RSV | RSV | TERM | RSV | RSV | RSV | PDZ |
| **Page 253** | | | | | | | | | |
| **Dec** | **Hex** | **b7** | **b6** | **b5** | **b4** | **b3** | **b2** | **b1** | **b0** |
| 20 | 0x14 | PGA_ICI1 | PGA_ICI0 | REF_ICI1 | REF_ICI0 | RSV | RSV | RSV | RSV |

### 14.2.2 Page 0 Registers

**Page 0 / Register 1 (Hex 0x01)**

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0x01 | PGA_VAL_CH1_L7 | PGA_VAL_CH1_L6 | PGA_VAL_CH1_L5 | PGA_VAL_CH1_L4 | PGA_VAL_CH1_L3 | PGA_VAL_CH1_L2 | PGA_VAL_CH1_L1 | PGA_VAL_CH1_L0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **PGA_VAL_CH1_L [7:0]** | **PGA Value Channel 1 Left**<br>: Global Channel gain for ADC1L. (Analog + Digital). Analog gain only, if manual gain mapping is enabled. (0x19)<br>Default value: 00000000<br>Specify 2s complement value with 7.1 format.<br>1110100_0: -12.0dB (Min)<br>:<br>1111111_0: -1.0dB<br>1111111_1: 0.5dB<br>0000000_0: 0.0dB<br>0000000_1: +0.5dB<br>0000001_0: +1.0dB<br>:<br>0001100_0: +12.0dB<br>:<br>0010100_0: +20.0dB<br>: |

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| | |
|---|---|
| | 0100000_0: +32.0dB<br>:<br>0101000_0: +40.0dB (Max) |

## Page 0 / Register 2 (Hex 0x02)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 2 | 0x02 | PGA_VAL_CH1_R7 | PGA_VAL_CH1_R6 | PGA_VAL_CH1_R5 | PGA_VAL_CH1_R4 | PGA_VAL_CH1_R3 | PGA_VAL_CH1_R2 | PGA_VAL_CH1_R1 | PGA_VAL_CH1_R0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **PGA_VAL_CH1_R[7:0]** | **PGA Value Channel 1 Right**<br>Programmable Gain Value, Channel 1 Right: (See Pg0, 0x01 for complete description.)<br>Default value: 00000000<br>(See Pg0, 0x01 for complete description.) |

## Page 0 / Register 3 (Hex 0x03)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 3 | 0x03 | PGA_VAL_CH2_L7 | PGA_VAL_CH2_L6 | PGA_VAL_CH2_L5 | PGA_VAL_CH2_L4 | PGA_VAL_CH2_L3 | PGA_VAL_CH2_L2 | PGA_VAL_CH2_L1 | PGA_VAL_CH2_L0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **PGA_VAL_CH2_L** | **PGA Value Channel 2 Left**<br>Programmable Gain Value, Channel 2 Left: (See Pg0, 0x01 for complete description.)<br>Default value: 0<br>(See Pg0, 0x01 for complete description.) |

## Page 0 / Register 4 (Hex 0x04)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 4 | 0x04 | PGA_VAL_CH2_R7 | PGA_VAL_CH2_R6 | PGA_VAL_CH2_R5 | PGA_VAL_CH2_R4 | PGA_VAL_CH2_R3 | PGA_VAL_CH2_R2 | PGA_VAL_CH2_R1 | PGA_VAL_CH2_R0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **PGA_VAL_CH2_R[7:0]** | **PGA Value Channel 2 Right**<br>Programmable Gain Value, Channel 2 Right: (See Pg0, 0x01 for complete description.)<br>Default value: 00000000<br>(See Pg0, 0x01 for complete description.) |

## Page 0 / Register 5 (Hex 0x05)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 5 | 0x05 | SMOOTH | LINK | DPGA_CLIP_EN | MAX_ATT1 | MAX_ATT0 | START_ATT1 | START_ATT0 | AGC_EN |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

| | |
|---|---|
| **SMOOTH** | **PGA Control - Enable PGA Smooth Change**<br>Default value: 1<br>0: Immediate Change<br>1: Smooth Change (Default) |
| **LINK** | **Link PGA control**<br>Default value: 0 |


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| | |
|---|---|
| | 0: Independent control (Default)<br>1: ch1[R]/Ch2[L]/Ch2[R] follow Ch1[L] PGA value. |
| **DPGA_CLIP_EN** | **Enable Clipping Detection After Digital PGA**<br>Default value: 0<br>0: Disable (Default)<br>1: Enable |
| **MAX_ATT[1:0]** | **Attenuation limit of the Automatic Clipping Suppression**<br>Default value: 00<br>00: -3dB (Default)<br>01: -4dB<br>10: -5dB<br>11: -6dB |
| **START_ATT[1:0]** | **Start Automatic Clipping Suppression after clipping is detected CLIP_NUM times**<br>Default value: 11<br>00: 80<br>01: 40<br>10: 20<br>11: 10 (Default) |
| **AGC_EN** | **Enable Automatic Clipping Suppression**<br>Default value: 0<br>0: Disable (Default)<br>1: Enable |

## Page 0 / Register 6 (Hex 0x06)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 6 | 0x06 | POL | RSV | SEL_L5 | SEL_L4 | SEL_L3 | SEL_L2 | SEL_L1 | SEL_L0 |
| Reset Value | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **POL** | **ADC1_INPUT_SEL_L - Change signal polarity**<br>Default value: 0<br>0: Normal (Default)<br>1: Inverted |
| **SEL_L[5:0]** | **ADC Input Channel Select (ADC1L)**<br>Default value: 000001<br>00_0000: No Select<br>00_0001: VINL1[SE] (Default)<br>00_0010: VINL2[SE]<br>00_0011: VINL2[SE] + VINL1[SE]<br>00_0100: VINL3[SE]<br>00_0101: VINL3[SE] + VINL1[SE]<br>00_0110: VINL3[SE] + VINL2[SE]<br>00_0111: VINL3[SE] + VINL2[SE] + VINL1[SE]<br>00_1000: VINL4[SE]<br>00_1001: VINL4[SE] + VINL1[SE] |

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| | |
|---|---|
| | 00_1010: VINL4[SE] + VINL2[SE]<br>00_1011: VINL4[SE] + VINL2[SE] + VINL1[SE]<br>00_1100: VINL4[SE] + VINL3[SE]<br>00_1101: VINL4[SE] + VINL3[SE] + VINL1[SE]<br>00_1110: VINL4[SE] + VINL3[SE] + VINL2[SE]<br>00_1111: VINL4[SE] + VINL3[SE] + VINL2[SE] + VINL1[SE]<br>01_0000: {VIN1P, VIN1M}[DIFF]<br>10_0000: {VIN4P, VIN4M}[DIFF]<br>11_0000: {VIN1P, VIN1M}[DIFF] + {VIN4P, VIN4M}[DIFF] |

## Page 0 / Register 7 (Hex 0x07)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 7 | 0x07 | POL | RSV | SEL_R5 | SEL_R4 | SEL_R3 | SEL_R2 | SEL_R1 | SEL_R0 |
| Reset Value | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **POL** | **ADC1_INPUT_SEL_R - Change signal polarity**<br>Default value: 0<br>0: Normal (Default)<br>1: Inverted |
| **SEL_R[5:0]** | **ADC Input Channel Select (ADC1R)**<br>Default value: 000001<br>00_0000: No Select<br>00_0001: VINR1[SE] (Default)<br>00_0010: VINR2[SE]<br>00_0011: VINR2[SE] + VINR1[SE]<br>00_0100: VINR3[SE]<br>00_0101: VINR3[SE] + VINR1[SE]<br>00_0110: VINR3[SE] + VINR2[SE]<br>00_0111: VINR3[SE] + VINR2[SE] + VINR1[SE]<br>00_1000: VINR4[SE]<br>00_1001: VINR4[SE] + VINR1[SE]<br>00_1010: VINR4[SE] + VINR2[SE]<br>00_1011: VINR4[SE] + VINR2[SE] + VINR1[SE]<br>00_1100: VINR4[SE] + VINR3[SE]<br>00_1101: VINR4[SE] + VINR3[SE] + VINR1[SE]<br>00_1110: VINR4[SE] + VINR3[SE] + VINR2[SE]<br>00_1111: VINR4[SE] + VINR3[SE] + VINR2[SE] + VINR1[SE]<br>01_0000: {VIN2P, VIN2M}[DIFF]<br>10_0000: {VIN3P, VIN3M}[DIFF]<br>11_0000: {VIN2P, VIN2M}[DIFF] + {VIN3P, VIN3M}[DIFF] |

## Page 0 / Register 8 (Hex 0x08)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 8 | 0x08 | POL | RSV | SEL_L5 | SEL_L4 | SEL_L3 | SEL_L2 | SEL_L1 | SEL_L0 |
| Reset Value | | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |


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| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **POL** | **ADC2_INPUT_SEL_L - Change signal polarity**<br>Default value: 0<br>0: Normal (Default)<br>1: Inverted |
| **SEL_L[5:0]** | **ADC 2 Input Channel Select (ADC2L)**<br>Default value: 000010<br>00_0000: No Select<br>00_0001: VINL1[SE]<br>00_0010: VINL2[SE] (Default)<br>00_0011: VINL2[SE] + VINL1[SE]<br>00_0100: VINL3[SE]<br>00_0101: VINL3[SE] + VINL1[SE]<br>00_0110: VINL3[SE] + VINL2[SE]<br>00_0111: VINL3[SE] + VINL2[SE] + VINL1[SE]<br>00_1000: VINL4[SE]<br>00_1001: VINL4[SE] + VINL1[SE]<br>00_1010: VINL4[SE] + VINL2[SE]<br>00_1011: VINL4[SE] + VINL2[SE] + VINL1[SE]<br>00_1100: VINL4[SE] + VINL3[SE]<br>00_1101: VINL4[SE] + VINL3[SE] + VINL1[SE]<br>00_1110: VINL4[SE] + VINL3[SE] + VINL2[SE]<br>00_1111: VINL4[SE] + VINL3[SE] + VINL2[SE] + VINL1[SE]<br>01_0000: {VIN1P, VIN1M}[DIFF]<br>10_0000: {VIN4P, VIN4M}[DIFF]<br>11_0000: {VIN1P, VIN1M}[DIFF] + {VIN4P, VIN4M}[DIFF] |

## Page 0 / Register 9 (Hex 0x09)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 9 | 0x09 | POL | RSV | SEL_R5 | SEL_R4 | SEL_R3 | SEL_R2 | SEL_R1 | SEL_R0 |
| Reset Value | | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **POL** | **ADC2_INPUT_SEL_R - Change signal polarity**<br>Default value: 0<br>0: Normal (Default)<br>1: Inverted |
| **SEL_R[5:0]** | **ADC 2 Input Channel Select (ADC2R)**<br>Default value: 000010<br>00_0000: No Select<br>00_0001: VINR1[SE]<br>00_0010: VINR2[SE] (Default )<br>00_0011: VINR2[SE] + VINR1[SE]<br>00_0100: VINR3[SE] |

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| | |
|---|---|
| | 00_0101: VINR3[SE] + VINR1[SE]<br>00_0110: VINR3[SE] + VINR2[SE]<br>00_0111: VINR3[SE] + VINR2[SE] + VINR1[SE]<br>00_1000: VINR4[SE]<br>00_1001: VINR4[SE] + VINR1[SE]<br>00_1010: VINR4[SE] + VINR2[SE]<br>00_1011: VINR4[SE] + VINR2[SE] + VINR1[SE]<br>00_1100: VINR4[SE] + VINR3[SE]<br>00_1101: VINR4[SE] + VINR3[SE] + VINR1[SE]<br>00_1110: VINR4[SE] + VINR3[SE] + VINR2[SE]<br>00_1111: VINR4[SE] + VINR3[SE] + VINR2[SE] + VINR1[SE]<br>01_0000: {VIN2P, VIN2M}[DIFF]<br>10_0000: {VIN3P, VIN3M}[DIFF]<br>11_0000: {VIN2P, VIN2M}[DIFF] + {VIN3P, VIN3M}[DIFF] |

## Page 0 / Register 10 (Hex 0x0A)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 10 | 0x0A | RSV | RSV | RSV | RSV | SEL3 | SEL2 | SEL1 | SEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **SEL[3:0]** | **Secondary ADC Input Channel (Note, Do not select the same channel that is already in use by an audio ADC)**<br>Default value: 0000<br>0: No Select (Default)<br>1: ch1(L)<br>2: ch1(R)<br>3: ch2(L)<br>4: ch2(R)<br>5: ch3(L)<br>6: ch3(R)<br>7: ch4(L)<br>8: ch4(R) |

## Page 0 / Register 11 (Hex 0x0B)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 11 | 0x0B | RX_WLEN1 | RX_WLEN0 | RSV | TDM_LRCK_MODE | TX_WLEN1 | TX_WLEN0 | FMT1 | FMT0 |
| Reset Value | | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **RX_WLEN[1:0]** | **Receive PCM Word length**<br>Default value: 01<br>00: Reserved<br>01: 24bit (Default)<br>10: 20bit<br>11: 16bit |


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| | |
|---|---|
| **TDM_LRCK_MODE** | **Notes: 1. TDM format can support 2 channels / 4 channels / 6 channels with one device 2. When BCK to LRCK ratio is 256, FMT must be configured as TDM format.**<br>Default value: 0<br>Configure the duty cycle of LRCK when I2S is configured as TDM mode<br>0: duty cycle of LRCK is 50%<br>1: duty cycle of LRCK is 1/256 (similar DSP mode) |
| **TX_WLEN[1:0]** | **Stereo PCM Word length**<br>Default value: 01<br>00: Reserved<br>01: 24bit (Default)<br>10: 20bit<br>11: 16bit |
| **FMT[1:0]** | **Serial Audio Interface Format (TDM/DSP Mode)**<br>Default value: 00<br>0: I2S (Default)<br>1: Left Justified<br>2: Right Justified<br>3: TDM/DSP (256Fs BCK is required) |

## Page 0 / Register 12 (Hex 0x0C)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 12 | 0x0C | RSV | RSV | RSV | RSV | RSV | RSV | TDM_OSEL1 | TDM_OSEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **TDM_OSEL[1:0]** | **Select TDM transmission data. Ch2 data only available on 4ch devices.**<br>Default value: 00<br>00: 2ch TDM (Default)<br>DOUT1: ch1[L], ch1[R]<br>DOUT2: ch2[L], ch2[R]<br>01: 4ch TDM<br>DOUT1: ch1[L], ch1[R], ch2[L], ch2[R]<br>DOUT2: ch1[L], ch1[R], ch2[L], ch2[R]<br>10: 6ch TDM<br>DOUT1: ch1[L], ch1[R], ch2[L], ch2[R], sec_ADC_LPF, sec_ADC_HPF<br>DOUT2: ch1[L], ch1[R], ch2[L], ch2[R], sec_ADC_LPF, sec_ADC_HPF<br>11: RESERVED |

## Page 0 / Register 13 (Hex 0x0D)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 13 | 0x0D | TX_TDM_OFFSET7 | TX_TDM_OFFSET6 | TX_TDM_OFFSET5 | TX_TDM_OFFSET4 | TX_TDM_OFFSET3 | TX_TDM_OFFSET2 | TX_TDM_OFFSET1 | TX_TDM_OFFSET0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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| | |
|---|---|
| **TX_TDM_OFFSET[7:0]** | **Set offset position in a serial audio data frame. This setting is enabled when 0x0B FMT[1:0] is set to DSP format.**<br>Default value: 00000000<br>0: 0 (Default)<br>1: 1 BCK (Same as I2S)<br>2: 2 BCK<br>3: 3 BCK<br>:<br>:<br>255: 255 BCK |

### Page 0 / Register 14 (Hex 0x0E)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 14 | 0x0E | RX_TDM_OFFSET7 | RX_TDM_OFFSET6 | RX_TDM_OFFSET5 | RX_TDM_OFFSET4 | RX_TDM_OFFSET3 | RX_TDM_OFFSET2 | RX_TDM_OFFSET1 | RX_TDM_OFFSET0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RX_TDM_OFFSET[7:0]** | **Set offset position in a serial audio data frame. This setting is enabled when I2S_RX_FMT is set to DSP format.**<br>Default value: 00000000<br>Offset position in a serial audio data frame.<br>0: 0 (Default)<br>1: 1 BCK (Same as I2S, only if LRCK is configured as 50/50 duty cycle)<br>2: 2 BCK<br>3: 3 BCK<br>:<br>:<br>255: 255 BCK |

### Page 0 / Register 15 (Hex 0x0F)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 15 | 0x0F | DPGA_VAL_CH1_L7 | DPGA_VAL_CH1_L6 | DPGA_VAL_CH1_L5 | DPGA_VAL_CH1_L4 | DPGA_VAL_CH1_L3 | DPGA_VAL_CH1_L2 | DPGA_VAL_CH1_L1 | DPGA_VAL_CH1_L0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **DPGA_VAL_CH1_L[7:0]** | **Gain setting for digital PGA when the device is used in the following scenarios:**<br>i. Analog PGA gain and digital PGA are set separately. ii. Digital Microphone Interface is used (4-channel device only, when Manual Gain Mapping is enabled in register 0x19)<br>Default value: 00000000<br>Specify 2s complement value with 7.1 format.<br>0x28 - 0x3F in 0.5 dB steps<br>Others: Reserved |

### Page 0 / Register 16 (Hex 0x10)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 16 | 0x10 | GPIO1_POL | GPIO1_FUNC2 | GPIO1_FUNC1 | GPIO1_FUNC0 | GPIO0_POL | GPIO0_FUNC2 | GPIO0_FUNC1 | GPIO0_FUNC0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |


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| | |
|---|---|
| **GPIO1_POL** | **GPIO1 Polarity Control**<br>Default value: 0<br>0: Normal (Default)<br>1: Invert |
| **GPIO1_FUNC[2:0]** | **Function select, GPIO1**<br>Default value: 000<br>000: GPIO1(Default)<br>001: Digital MIC Input 1(In)<br>010: INT<br>011: Internal SCK (Out)<br>100: Digital Mute (In)<br>101: DOUT2 (Out)<br>110: DIN (In)<br>111: Reserved |
| **GPIO0_POL** | **GPIO0 Polarity Control**<br>Default value: 0<br>0: Normal (Default)<br>1: Invert |
| **GPIO0_FUNC[2:0]** | **Function select, GPIO0**<br>Default value: 001<br>000: GPIO0<br>001: SPI MISO (Out:Default)<br>010: RESERVED<br>011: Internal SCK (Out)<br>100: Digital Mute (In)<br>101: DOUT2 (Out)<br>110: DIN (In)<br>111: Reserved |

## Page 0 / Register 17 (Hex 0x11)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 17 | 0x11 | GPIO3_POL | GPIO3_FUNC2 | GPIO3_FUNC1 | GPIO3_FUNC0 | GPIO2_POL | GPIO2_FUNC2 | GPIO2_FUNC1 | GPIO2_FUNC0 |
| Reset Value | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **GPIO3_POL** | **GPIO3 Polarity Control**<br>Default value: 0<br>0: Normal (Default)<br>1: Invert |
| **GPIO3_FUNC[2:0]** | **Function select, GPIO3**<br>Default value: 010<br>000: GPIO3<br>001: (Reserved)<br>010: INT (Default)<br>011: Internal SCK (Out)<br>100: Digital Mute (In) |

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| | |
|---|---|
| | 101: DOUT2 (Out)<br>110: DIN (In)<br>111: Reserved |
| **GPIO2_POL** | **GPIO2 Polarity Control**<br>Default value: 0<br>0: Normal (Default)<br>1: Invert |
| **GPIO2_FUNC[2:0]** | **Function select, GPIO2**<br>Default value: 000<br>000: GPIO2(Default)<br>001: Digital MIC Clock Output (Out)<br>010: INT<br>011: Internal SCK (Out)<br>100: Digital Mute (In)<br>101: DOUT2 (Out)<br>110: DIN (In)<br>111: Reserved |

## Page 0 / Register 18 (Hex 0x12)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 18 | 0x12 | | GPIO1_DIR2 | GPIO1_DIR1 | GPIO1_DIR0 | RSV | GPIO0_DIR2 | GPIO0_DIR1 | GPIO0_DIR0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **GPIO1_DIR[2:0]** | **Direction control of GPIO1 when it is configured as GPIO function**<br>Default value: 000<br>000: Input (Default)<br>001: Input with 'sticky bit'<br>010: Input with toggle detection<br>011: Raw input (not deglictched)<br>100: Output<br>101: Open Drain<br>110: (Reserved)<br>111: (Reserved) |
| **GPIO0_DIR[2:0]** | **Direction control of GPIO0 when it is configured as GPIO function**<br>Default value: 000<br>000: Input (Default)<br>001: Input with 'sticky bit'<br>010: Input with toggle detection<br>011: Raw input (not deglictched)<br>100: Output<br>101: Open Drain<br>110: (Reserved)<br>111: (Reserved) |


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## Page 0 / Register 19 (Hex 0x13)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 19 | 0x13 | | GPIO3_DIR2 | GPIO3_DIR1 | GPIO3_DIR0 | RSV | GPIO2_DIR2 | GPIO2_DIR1 | GPIO2_DIR0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **GPIO3_DIR[2:0]** | Direction control of GPIO3 when it is configured as GPIO function<br>Default value: 000<br>000: Input (Default)<br>001: Input with 'sticky bit'<br>010: Input with toggle detection<br>011: Raw input (not deglictched)<br>100: Output<br>101: Open Drain<br>110: (Reserved)<br>111: (Reserved) |
| **GPIO2_DIR[2:0]** | Direction control of GPIO2 when it is configured as GPIO function<br>Default value: 000<br>000: Input (Default)<br>001: Input with 'sticky bit'<br>010: Input with toggle detection<br>011: Raw input (not deglictched)<br>100: Output<br>101: Open Drain<br>110: (Reserved)<br>111: (Reserved) |

## Page 0 / Register 20 (Hex 0x14)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 20 | 0x14 | GPIO3_OUT | GPIO2_OUT | GPIO1_OUT | GPIO0_OUT | GPIO3_IN | GPIO2_IN | GPIO1_IN | GPIO0_IN |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **GPIO3_OUT** | **GPIO_STATE - Output status**<br>Default value: 0 |
| **GPIO2_OUT** | Default value: 0 |
| **GPIO1_OUT** | Default value: 0 |
| **GPIO0_OUT** | Default value: 0 |
| **GPIO3_IN** | **Input status (or toggle status) of the GPIOs**<br>The sticky flag is cleared when this register is read.<br>Default value: 0 |
| **GPIO2_IN** | |

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| | |
|---|---|
| | Default value: 0 |
| **GPIO1_IN** | Default value: 0 |
| **GPIO0_IN** | Default value: 0 |

## Page 0 / Register 21 (Hex 0x15)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 21 | 0x15 | PULL_DOWN_DIS[3] | PULL_DOWN_DIS[2] | PULL_DOWN_DIS[1] | PULL_DOWN_DIS[0] | RSV | RSV | RSV | RSV |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **PULL_DOWN_DIS[3]** | **Enable or disable the pull down resistor of IO pins**<br>Default value: 0<br>0: Enable the pull down of GPIO3/IntC (pin 19)<br>1: Disable the pull down |
| **PULL_DOWN_DIS[2]** | Default value: 0<br>0: Enable the pull down of GPIO2/IntB (pin 20)<br>1: Disable the pull down |
| **PULL_DOWN_DIS[1]** | Default value: 0<br>0: Enable the pull down of GPIO1 (pin 21)<br>1: Disable the pull down |
| **PULL_DOWN_DIS[0]** | Default value: 0<br>0: Enable the pull down of GPIO0 (pin 22)<br>1: Disable the pull down |

## Page 0 / Register 22 (Hex 0x16)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 22 | 0x16 | DPGA_VAL_CH1_R7 | DPGA_VAL_CH1_R6 | DPGA_VAL_CH1_R5 | DPGA_VAL_CH1_R4 | DPGA_VAL_CH1_R3 | DPGA_VAL_CH1_R2 | DPGA_VAL_CH1_R1 | DPGA_VAL_CH1_R0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **DPGA_VAL_CH1_R[7:0]** | **Gain setting for digital PGA channel 1 right when the device is used in the following two scenarios (4 channel device only, values from 0x28 to 0x37):**<br>i. Analog PGA gain and digital PGA are set separately ii. Digital Microphone Interface is used (4-channel device only, when Manual Gain Mapping is enabled in register 0x19)<br>Default value: 00000000<br>Specify 2s complement value with 7.1 format.<br>0010100_0: 0.0 dB<br>0010100_1: 0.5 dB<br>0010101_0: 1.0 dB<br>0010101_1: 1.5 dB |


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| | |
|---|---|
| | . . .<br>0011111_1: 7.5 dB ( Max)<br>Others: Reserved |

## Page 0 / Register 23 (Hex 0x17)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 23 | 0x17 | DPGA_VAL_CH2_L7 | DPGA_VAL_CH2_L6 | DPGA_VAL_CH2_L5 | DPGA_VAL_CH2_L4 | DPGA_VAL_CH2_L3 | DPGA_VAL_CH2_L2 | DPGA_VAL_CH2_L1 | DPGA_VAL_CH2_L0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **DPGA_VAL_CH2_L[7:0]** | **Gain setting for digital PGA channel 2 left (4-channel device only)**<br>See Pg0, Reg 0x16 description<br>Default value: 00000000<br>See Pg0, Reg 0x16 description |

## Page 0 / Register 24 (Hex 0x18)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 24 | 0x18 | DPGA_VAL_CH2_R7 | DPGA_VAL_CH2_R6 | DPGA_VAL_CH2_R5 | DPGA_VAL_CH2_R4 | DPGA_VAL_CH2_R3 | DPGA_VAL_CH2_R2 | DPGA_VAL_CH2_R1 | DPGA_VAL_CH2_R0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **DPGA_VAL_CH2_R[7:0]** | **Gain setting for digital PGA channel 2 right (4-channel device only)**<br>See Pg0, Reg 0x16 description<br>Default value: 00000000<br>See Pg0, Reg 0x16 description |

## Page 0 / Register 25 (Hex 0x19)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 25 | 0x19 | DPGA_CH2_R | DPGA_CH2_L | DPGA_CH1_R | DPGA_CH1_L | APGA_CH2_R | APGA_CH2_L | APGA_CH1_R | APGA_CH1_L |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **DPGA_CH2_R** | **DPGA Control Mapping (4-channel device only)**<br>CH2_R channel (Note: Using manual gain mapping in the 2ch devices sets the digital gain to 0dB.)<br>Default value: 0<br>0: Auto gain mapping (Default)<br>1: Manual gain mapping |
| **DPGA_CH2_L** | **DPGA Control Mapping (4-channel devices only)**<br>Gain control mode for digital PGA of CH2_L channel<br>Default value: 0<br>0: Auto gain mapping (Default)<br>1: Manual gain mapping |
| **DPGA_CH1_R** | **DPGA Control Mapping (4-channel device only)**<br>Gain control mode for digital PGA of CH1_R channel<br>Default value: 0<br>0: Auto gain mapping (Default)<br>1: Manual gain mapping |
| **DPGA_CH1_L** | **DPGA Control Mapping (4-channel device only)**<br>Gain control mode for digital PGA of CH1_L channel<br>Default value: 0<br>0: Auto gain mapping (Default) |

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| | |
|---|---|
| | 1: Manual gain mapping |
| **APGA_CH2_R** | **DPGA Control Mapping (4-channel device only)**<br>Gain control mode for analog PGA of CH2_R channel<br>Default value: 0<br>0: Auto gain mapping (Default)<br>1: Manual gain mapping |
| **APGA_CH2_L** | **DPGA Control Mapping (4-channel device only)**<br>Gain control mode for analog PGA of CH2_L channel<br>Default value: 0<br>0: Auto gain mapping (Default)<br>1: Manual gain mapping |
| **APGA_CH1_R** | **DPGA Control Mapping (4-channel device only)**<br>Gain control mode for analog PGA of CH1_R channel<br>Default value: 0<br>0: Auto gain mapping (Default)<br>1: Manual gain mapping |
| **APGA_CH1_L** | **DPGA Control Mapping (4-channel device only)**<br>Gain control mode for analogPGA of CH1_L channel<br>Default value: 0<br>0: Auto gain mapping (Default)<br>1: Manual gain mapping |

## Page 0 / Register 26 (Hex 0x1A)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 26 | 0x1A | DIGMIC_IN1_SEL 1 | DIGMIC_IN1_SEL 0 | DIGMIC_IN0_SEL 1 | DIGMIC_IN0_SEL 0 | RSV | RSV | DIGMIC_4CH | DIGMIC_EN |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DIGMIC_IN1_SEL[1:0]** | **Select which pin is used for digital mic data input for MIC1 interface (4CH device Only)**<br>Default value: 00<br>00: GPIO0 (Default)<br>01: GPIO1<br>10: Invalid<br>11: Invalid |
| **DIGMIC_IN0_SEL[1:0]** | **Select which pin is used for digital mic data input for MIC0 interface**<br>Default value: 00<br>00: GPIO0 (Default)<br>01: GPIO1<br>10: Invalid<br>11: Invalid |
| **DIGMIC_4CH** | **(4ch device only) Select if the second pair of filters will be used for digital Microphone as signal processing**<br>Default value: 0<br>0: configured for analog ADC signal processing (Default)<br>1: configured for digital MIC signal processing |
| **DIGMIC_EN** | **Select if the first pair of filters will be used for digital Microphone as signal processing** |


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| | |
|---|---|
| | Default value: 0<br>0: configured as analog ADC signal processing (Default)<br>1: configured as digital MIC signal processing |

## Page 0 / Register 27 (Hex 0x1B)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 27 | 0x1B | RSV | RSV | 1 | 0 | RSV | RSV | DIN_RESAMP1 | DIN_RESAMP0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DIN_RESAMP[1:0]** | **Resample DIN with internal BCK to avoid internal timing issue**<br>Default value: 00<br>00: No resample (Default)<br>01: resample DIN with rising edge of BCK<br>10: resample DIN with falling edge of BCK<br>11: Not supported |

## Page 0 / Register 32 (Hex 0x20)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 32 | 0x20 | SCK_XI_SEL1 | SCK_XI_SEL0 | MST_SCK_SRC | MST_MODE | ADC_CLK_SRC | DSP2_CLK_SRC | DSP1_CLK_SRC | CLKDET_EN |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **SCK_XI_SEL[1:0]** | **SCK/Xtal selection**<br>SCK/Xtal selection<br>Default value: 00<br>00: SCK or Xtal (Default)<br>01: SCK<br>10: Xtal<br>11: (Reserved) |
| **MST_SCK_SRC** | **Master-Mode SCK source select**<br>Default value: 0<br>0: SCK or XI (Default)<br>1: BCK |
| **MST_MODE** | **Master/Slave selection**<br>Default value: 0<br>0: Slave (Default)<br>1: Master |
| **ADC_CLK_SRC** | **ADC Clock Source selection. Ignored if CLKDET_EN = 1**<br>Default value: 0<br>0: SCK (Default)<br>1: PLL |
| **DSP2_CLK_SRC** | **DSP2 Clock Source selection. Ignored if CLKDET_EN = 1**<br>Default value: 0<br>0: SCK (Default)<br>1: PLL |
| **DSP1_CLK_SRC** | **DSP1 Clock Source selection. Ignored if CLKDET_EN = 1**<br>Default value: 0 |

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| | |
|---|---|
| | 0: SCK (Default)<br>1: PLL |
| **CLKDET_EN** | **Enable Auto Clock Detector Configuration**<br>Default value: 1<br>0: Disable<br>1: Enable (Default) |

## Page 0 / Register 33 (Hex 0x21)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 33 | 0x21 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DIV_NUM[6:0]** | **Set the DSP1 Clock Divider Value**<br>Ignored if CLKDET_EN = 1<br>Default value: 0000001<br>0: 1<br>1: 1/2<br>2: 1/3<br>3: 1/4<br>:<br>:<br>127: 1/128 |

## Page 0 / Register 34 (Hex 0x22)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 34 | 0x22 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DIV_NUM[6:0]** | **Set the DSP2 Clock Divider Value**<br>Ignored if CLKDET_EN = 1<br>Default value: 0000001<br>0: 1<br>1: 1/2<br>2: 1/3<br>3: 1/4<br>:<br>:<br>127: 1/128 |

## Page 0 / Register 35 (Hex 0x23)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 35 | 0x23 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |


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| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DIV_NUM[6:0]** | **Set the ADC Clock Divider Value**<br>Ignored if CLKDET_EN = 1<br>Default value: 0000011<br>0: 1<br>1: 1/2<br>2: 1/3<br>3: 1/4<br>:<br>:<br>127: 1/128 |

## Page 0 / Register 37 (Hex 0x25)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 37 | 0x25 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DIV_NUM[6:0]** | **Set the PLL SCK Clock Divider value**<br>Default value: 0000111<br>Divider value.<br>0: 1<br>1: 1/2<br>2: 1/3<br>3: 1/4<br>:<br>:<br>7: 1/8 (Default)<br>:<br>:<br>127: 1/128 |

## Page 0 / Register 38 (Hex 0x26)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 38 | 0x26 | RSV | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DIV_NUM[6:0]** | **Set the Master Clock (SCK) Divider value**<br>Ratio of Master clock (SCK) to Bit Clock (BCK)<br>Default value: 0000011<br>Divider value.<br>0: 1<br>1: 1/2<br>2: 1/3<br>3: 1/4 |

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| | |
|---|---|
| | :<br>:<br>7: 1/8 (Default)<br>:<br>:<br>127: 1/128 |

## Page 0 / Register 39 (Hex 0x27)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 39 | 0x27 | DIV_NUM7 | DIV_NUM6 | DIV_NUM5 | DIV_NUM4 | DIV_NUM3 | DIV_NUM2 | DIV_NUM1 | DIV_NUM0 |
| Reset Value | | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| **DIV_NUM[7:0]** | **Set the Master SCK Clock Divider value**<br>SCK to LRCK ratio in master mode<br>Default value: 00111111<br>Divider value<br>0: 1<br>1: 1/2<br>2: 1/3<br>3: 1/4<br>:<br>:<br>63: 1/64 (Default)<br>:<br>:<br>127: 1/128<br>. . .<br>255: 1/256 |

## Page 0 / Register 40 (Hex 0x28)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 40 | 0x28 | RSV | RSV | RSV | LOCK | RSV | RSV | PLL_REF_SEL | PLL_EN |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **LOCK** | **PLL Lock Status**<br>Default value: 0<br>0: Not locked<br>1: Locked |
| **PLL_REF_SEL** | **PLL Reference clock selection**<br>Ignored if CLKDET_EN = 1<br>Default value: 0<br>0: SCK (Default)<br>1: BCK |
| **PLL_EN** | **Enable the PLL**<br>Ignored if CLKDET_EN = 1<br>Default value: 1<br>0: Disable |


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| | |
|---|---|
| | 1: Enable (Default) |

### Page 0 / Register 41 (Hex 0x29)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 41 | 0x29 | RSV | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **P[6:0]** | **PLL P-Divider value**<br>Ignored if CLKDET_EN = 1<br>Default value: 0000000<br>0: 1<br>1: 1/2<br>2: 1/3<br>3: 1/4<br>:<br>127: 1/128 |

### Page 0 / Register 42 (Hex 0x2A)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 42 | 0x2A | RSV | RSV | RSV | RSV | R3 | R2 | R1 | R0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **R[3:0]** | **PLL R-Divider value**<br>Ignored if CLKDET_EN = 1<br>Default value: 0000<br>0: 1<br>1: 1/2<br>2: 1/3<br>3: 1/4<br>:<br>:<br>15: 1/16 |

### Page 0 / Register 43 (Hex 0x2B)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 43 | 0x2B | RSV | RSV | J5 | J4 | J3 | J2 | J1 | J0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **J[5:0]** | **Integer part of the PLL J.D-Divider value**<br>Ignored if CLKDET_EN = 1<br>Default value: 000001<br>0: (Prohibit)<br>1: 1<br>2: 2 |

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| | |
|---|---|
| | :<br>:<br>63: 63 |

## Page 0 / Register 44 (Hex 0x2C)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 44 | 0x2C | D_LSB7 | D_LSB6 | D_LSB5 | D_LSB4 | D_LSB3 | D_LSB2 | D_LSB1 | D_LSB0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **D_LSB** | **Fractional part of the PLL J.D-Divider value. (Least Significant Bits)**<br>Ignored if CLKDET_EN = 1<br>Default value: 0<br>0: 0<br>1: 1<br>2: 2<br>3: 3<br>:<br>:<br>:<br>9999: 9999 |

## Page 0 / Register 45 (Hex 0x2D)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 45 | 0x2D | RSV | RSV | D_MSB5 | D_MSB4 | D_MSB3 | D_MSB2 | D_MSB1 | D_MSB0 |
| Reset Value | | | | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **D_MSB[5:0]** | **Fractional part of the PLL J.D-Divider value. (Most Significant Bits, [13:8])**<br>Ignored if CLKDET_EN = 1<br>Default value: 000000<br>0: 0<br>1: 1<br>2: 2<br>3: 3<br>:<br>:<br>:<br>9999: 9999 |

## Page 0 / Register 48 (Hex 0x30)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 48 | 0x30 | CH4R | CH4L | CH3R | CH3L | CH2R | CH2L | CH1R | CH1L |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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| | |
|---|---|
| **CH4R** | **SIGDET_CH_MODE**<br>Select the signal detection mode for each channel in SLEEP Mode<br>Default value: 0<br>0: Audio signal detection (Default)<br>1: DC level-change detection |
| **CH4L** | Default value: 0 |
| **CH3R** | Default value: 0 |
| **CH3L** | Default value: 0 |
| **CH2R** | Default value: 0 |
| **CH2L** | Default value: 0 |
| **CH1R** | Default value: 0 |
| **CH1L** | Default value: 0 |

## Page 0 / Register 49 (Hex 0x31)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 49 | 0x31 | CH4R | CH4L | CH3R | CH3L | CH2R | CH2L | CH1R | CH1L |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **CH4R** | **SIGDET_TRIG_MASK**<br>Mask bits of the interrupt trigger. All channels are scanned, even if they are masked. Developers can ignore specific channels and prevent them from generating interrupts using this register.<br>Default value: 0<br>0: No mask (Default)<br>1: Mask |
| **CH4L** | Default value: 0 |
| **CH3R** | Default value: 0 |
| **CH3L** | Default value: 0 |
| **CH2R** | Default value: 0 |
| **CH2L** | Default value: 0 |

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| | |
|---|---|
| **CH1R** | Default value: 0 |
| **CH1L** | Default value: 0 |

## Page 0 / Register 50 (Hex 0x32)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 50 | 0x32 | CH4R | CH4L | CH3R | CH3L | CH2R | CH2L | CH1R | CH1L |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **CH4R** | **SIGDET_STAT**<br>Status of the signal level detection In both Energysense and Controlsense modes (Read only)<br>Default value: 0<br>[In the Audio Signal Detection Mode]<br>a) In the Active/Run state<br>0: Signal active<br>1: Signal lost<br>b) In the Sleep mode<br>0: Signal lost<br>1: Signal active<br>[In Automatic Clipping Suppresion Mode]<br>0: No change.<br>1: changed DC level |
| **CH4L** | Default value: 0 |
| **CH3R** | Default value: 0 |
| **CH3L** | Default value: 0 |
| **CH2R** | Default value: 0 |
| **CH2L** | Default value: 0 |
| **CH1R** | Default value: 0 |
| **CH1L** | Default value: 0 |

## Page 0 / Register 52 (Hex 0x34)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 52 | 0x34 | RSV | RSV | RSV | TIME4 | TIME3 | TIME2 | TIME1 | TIME0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **TIME[4:0]** | **SIGDET_LOSS_TIME**<br>If the signal drops below the threshold on the current audio input for this set amount of time, the device generates an interrupt.<br>Default value: 00000<br>0: Prohibit<br>1: 1 minute (Default)<br>2: 2 minutes<br>3: 3 minutes<br>:<br>30: 30 minutes (Max) |

## Page 0 / Register 53 (Hex 0x35)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 53 | 0x35 | RSV | RSV | RSV | RSV | RSV | TIME2 | TIME1 | TIME0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **TIME[2:0]** | **SIGDET_SCAN_TIME**<br>Configures the scan time for each channel in the SLEEP state<br>Default value: 000<br>000: 160[msec] (Default)<br>001: 80[msec]<br>010: 40[msec]<br>011: 20[msec]<br>100: 10[msec]<br>Others: Invalid |

## Page 0 / Register 54 (Hex 0x36)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 54 | 0x36 | RSV | RSV | RSV | RSV | RSV | INT_INTVL2 | INT_INTVL1 | INT_INTVL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **INT_INTVL[2:0]** | **SIGDET_INT_INTVL**<br>Interval time of the signal detector interrupt when there is signal detection. This time value is used for Energysense wakeup from sleep interrupt and from Controlsense interrupts<br>Default value: 001<br>Interval time of the signal-resume interrupt<br>000: No repeat<br>001: 1 sec (Default)<br>010: 2 sec<br>011: 3 sec<br>100: 4 sec<br>Others: Invalid |

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### Page 0 / Register 64 (Hex 0x40)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 64 | 0x40 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **REF[7:0]** | **SIGDET_DC_REF_CH1_L**<br>Reference level of Controlsense detection<br>Default value: 10000000<br>0x80: Default |

### Page 0 / Register 65 (Hex 0x41)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 65 | 0x41 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| Reset Value | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| **DIFF[7:0]** | **SIGDET_DC_DIFF_CH1_L**<br>Difference level of Controlsense detection<br>Default value: 01111111<br>0x7F: Default |

### Page 0 / Register 66 (Hex 0x42)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 66 | 0x42 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **LEVEL[7:0]** | **10.7.3 SIGDET_DC_LEVEL_CH1_L**<br>Current DC level<br>Default value: 00000000 |

### Page 0 / Register 67 (Hex 0x43)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 67 | 0x43 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **REF[7:0]** | **SIGDET_DC_REF_CH1_R**<br>Reference level of Controlsense detection<br>Default value: 10000000<br>0x80: Default |

### Page 0 / Register 68 (Hex 0x44)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 68 | 0x44 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| Reset Value | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| **DIFF[7:0]** | **SIGDET_DC_DIFF_CH1_R**<br>Difference level of Controlsense detection<br>Default value: 01111111<br>0x7F: Default |

### Page 0 / Register 69 (Hex 0x45)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 69 | 0x45 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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| | |
|---|---|
| **LEVEL[7:0]** | **10.7.3 SIGDET_DC_LEVEL_CH1_R**<br>Current DC level<br>Default value: 00000000 |

### Page 0 / Register 70 (Hex 0x46)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 70 | 0x46 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **REF[7:0]** | **SIGDET_DC_REF_CH2_L**<br>Reference level of Controlsense detection<br>Default value: 10000000<br>0x80: Default |

### Page 0 / Register 71 (Hex 0x47)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 71 | 0x47 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| Reset Value | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| **DIFF[7:0]** | **SIGDET_DC_DIFF_CH2_L**<br>Difference level of Controlsense detection<br>Default value: 01111111<br>0x7F: Default |

### Page 0 / Register 72 (Hex 0x48)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 72 | 0x48 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **LEVEL[7:0]** | **10.7.3 SIGDET_DC_LEVEL_CH2_L**<br>Current DC level<br>Default value: 00000000 |

### Page 0 / Register 73 (Hex 0x49)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 73 | 0x49 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **REF[7:0]** | **SIGDET_DC_REF_CH2_R**<br>Reference level of Controlsense detection<br>Default value: 10000000<br>0x80: Default |

### Page 0 / Register 74 (Hex 0x4A)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 74 | 0x4A | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| Reset Value | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| **DIFF[7:0]** | **SIGDET_DC_DIFF_CH2_R**<br>Difference level of Controlsense detection<br>Default value: 01111111<br>0x7F: Default |

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### Page 0 / Register 75 (Hex 0x4B)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 75 | 0x4B | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **LEVEL[7:0]** | **10.7.3 SIGDET_DC_LEVEL_CH2_R**<br>Current DC level<br>Default value: 00000000 |

### Page 0 / Register 76 (Hex 0x4C)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 76 | 0x4C | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **REF[7:0]** | **SIGDET_DC_REF_CH3_L**<br>Reference level of Controlsense detection<br>Default value: 10000000<br>0x80: Default |

### Page 0 / Register 77 (Hex 0x4D)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 77 | 0x4D | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| Reset Value | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| **DIFF[7:0]** | **SIGDET_DC_DIFF_CH3_L**<br>Difference level of Controlsense detection<br>Default value: 01111111<br>0x7F: Default |

### Page 0 / Register 78 (Hex 0x4E)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 78 | 0x4E | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **LEVEL[7:0]** | **10.7.3 SIGDET_DC_LEVEL_CH3_L**<br>Current DC level<br>Default value: 00000000 |

### Page 0 / Register 79 (Hex 0x4F)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 79 | 0x4F | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **REF[7:0]** | **SIGDET_DC_REF_CH3_R**<br>Reference level of Controlsense detection<br>Default value: 10000000<br>0x80: Default |

### Page 0 / Register 80 (Hex 0x50)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 80 | 0x50 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| Reset Value | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |


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| | |
|---|---|
| **DIFF[7:0]** | **SIGDET_DC_DIFF_CH3_R**<br>Difference level of Controlsense detection<br>Default value: 01111111<br>0x7F: Default |

### Page 0 / Register 81 (Hex 0x51)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 81 | 0x51 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **LEVEL[7:0]** | **10.7.3 SIGDET_DC_LEVEL_CH3_R**<br>Current DC level<br>Default value: 00000000 |

### Page 0 / Register 82 (Hex 0x52)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 82 | 0x52 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **REF[7:0]** | **SIGDET_DC_REF_CH4_L**<br>Reference level of Controlsense detection<br>Default value: 10000000<br>0x80: Default |

### Page 0 / Register 83 (Hex 0x53)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 83 | 0x53 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| Reset Value | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| **DIFF[7:0]** | **SIGDET_DC_DIFF_CH4_L**<br>Difference level of Controlsense detection<br>Default value: 01111111<br>0x7F: Default |

### Page 0 / Register 84 (Hex 0x54)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 84 | 0x54 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **LEVEL[7:0]** | **10.7.3 SIGDET_DC_LEVEL_CH4_L**<br>Current DC level<br>Default value: 00000000 |

### Page 0 / Register 85 (Hex 0x55)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 85 | 0x55 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF2 | REF0 |
| Reset Value | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **REF[7:0]** | **SIGDET_DC_REF_CH4_R**<br>Reference level of Controlsense detection<br>Default value: 10000000<br>0x80: Default |

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## Page 0 / Register 86 (Hex 0x56)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 86 | 0x56 | DIFF7 | DIFF6 | DIFF5 | DIFF4 | DIFF3 | DIFF2 | DIFF1 | DIFF0 |
| Reset Value | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

| | |
|---|---|
| **DIFF[7:0]** | **SIGDET_DC_DIFF_CH4_R**<br>Difference level of Controlsense detection<br>Default value: 01111111<br>0x7F: Default |

## Page 0 / Register 87 (Hex 0x57)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 87 | 0x57 | LEVEL7 | LEVEL6 | LEVEL5 | LEVEL4 | LEVEL3 | LEVEL2 | LEVEL1 | LEVEL0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **LEVEL[7:0]** | **10.7.3 SIGDET_DC_LEVEL_CH4_R**<br>Current DC level<br>Default value: 00000000 |

## Page 0 / Register 88 (Hex 0x58)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 88 | 0x58 | DC_NOLATCH | AUXADC_RDY | DC_RDY | AUXADC_LATCH | AUXADC_DATA_TYPE | DC_CH2 | DC_CH1 | DC_CH0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **DC_NOLATCH** | **AUXADC_DATA_CTRL**<br>Read Directly without latch operation (from secondary ADC)<br>Default value: 0<br>0: With latch operation<br>1: Without latch operation when read DC value |
| **AUXADC_RDY** | **Indicate the latch operation is finished and AUXADC value is ready for read operation**<br>Default value: 0<br>0: Latch operation is running<br>1: AUXADC value is ready for read operation |
| **DC_RDY** | **Indicate the latch operation is finished and DC value is ready**<br>Default value: 0<br>0: Latch operation is running<br>1: DC value is ready for read operation |
| **AUXADC_LATCH** | **Trigger to latch 16-bit AUXADC value for read operation: Rising edge is the trigger signal**<br>Default value: 0<br>0: Idle<br>1: Latch the value for read operation |
| **AUXADC_DATA_TYPE** | **Data to be read from Control Interface**<br>Default value: 0<br>0: read LPF data<br>1: read HPF data |
| **DC_CH[2:0]** | **Select DC-value channel to be latched for control-interface read operation**<br>Default value: 000<br>000: CH1_L |


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| | |
|---|---|
| | 001: CH1_R<br>010: CH2_L<br>011: CH2_R<br>100: CH3_L<br>101: CH3_R<br>110: CH4_L<br>111: CH4_R |

## Page 0 / Register 89 (Hex 0x59)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 89 | 0x59 | AUXADC_DATA_LSB7 | AUXADC_DATA_LSB6 | AUXADC_DATA_LSB5 | AUXADC_DATA_LSB4 | AUXADC_DATA_LSB3 | AUXADC_DATA_LSB2 | AUXADC_DATA_LSB1 | AUXADC_DATA_LSB0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **AUXADC_DATA_LSB[7:0]** | **Low byte of Secondary ADC output [7:0]**<br>The data depends on AUXADC_DATA_TYPE setting AUXADC_DATA_TYPE = 0: reading LPF of secondary ADC AUXADC_DATA_TYPE = 1: reading HPF of secondary ADC<br>Default value: 00000000 |

## Page 0 / Register 90 (Hex 0x5A)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 90 | 0x5A | AUXADC_DATA_MSB7 | AUXADC_DATA_MSB6 | AUXADC_DATA_MSB5 | AUXADC_DATA_MSB4 | AUXADC_DATA_MSB3 | AUXADC_DATA_MSB2 | AUXADC_DATA_MSB1 | AUXADC_DATA_MSB0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **AUXADC_DATA_MSB[7:0]** | **High byte of Secondary ADC output [15:8]**<br>The data depends on AUXADC_DATA_TYPE setting AUXADC_DATA_TYPE = 0: reading LPF of secondary ADC AUXADC_DATA_TYPE = 1: reading HPF of secondary ADC<br>Default value: 00000000 |

## Page 0 / Register 96 (Hex 0x60)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 96 | 0x60 | RSV | RSV | RSV | POSTPGA_CP | CLKERR | DC_CHANG | DIN_TOGGLE | ENGSTR |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **POSTPGA_CP** | **Write 0 to clear interrupts, all bits in this register**<br>Enable the Post-PGA Clipping Interrupt<br>Default value: 0<br>0: Disable (Default)<br>1: Enable |
| **CLKERR** | **Enable the Clock Error Interrupt**<br>Default value: 0<br>0: Disable (Default)<br>1: Enable |
| **DC_CHANG** | **Enable the DC Level Change Interrupt**<br>Default value: 0<br>0: Disable (Default)<br>1: Enable |

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| | |
|---|---|
| **DIN_TOGGLE** | **Enable I2S RX DIN toggle Interrupt**<br>Default value: 0<br>0: Disable (Default)<br>1: Enable |
| **ENGSTR** | **Enable the Energysense Interrupt**<br>Default value: 1<br>0: Disable<br>1: Enable (Default) |

## Page 0 / Register 97 (Hex 0x61)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 97 | 0x61 | RSV | RSV | RSV | POSTPGA_CP | CLKERR | DC_CHANG | DIN_TOGGLE | ENGSTR |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **POSTPGA_CP** | **Write 0 to register 0x60 clear interrupts, all bits in this register**<br>Status of Post-PGA Clipping Interrupt<br>Default value: 0<br>0: None<br>1: Interrupt Occurred<br>Status is cleared by writing a 0 to register 0x60 - all bits in this register |
| **CLKERR** | **Status of the Clock Error Interrupt**<br>Default value: 0<br>0: None<br>1: Interrupt Occurred |
| **DC_CHANG** | **Status of the DC Level Change Interrupt**<br>Default value: 0<br>0: None<br>1: Interrupt Occurred |
| **DIN_TOGGLE** | **Status of I2S RX DIN toggle Interrupt**<br>Default value: 0<br>0: None<br>1: Interrupt Occurred |
| **ENGSTR** | **Status of the Energysense Interrupt**<br>Default value: 0<br>0: None<br>1: Interrupt Occurred |

## Page 0 / Register 98 (Hex 0x62)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 98 | 0x62 | RSV | RSV | POL1 | POL0 | RSV | RSV | WIDTH1 | WIDTH0 |
| Reset Value | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |


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| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **POL[1:0]** | **Polarity of the interrupt pulse**<br>Default value: 01<br>00: Low Active<br>01: High Active (Default)<br>10: Open Drain (L-Active)<br>11: Reserved |
| **WIDTH[1:0]** | **Width of the interrupt pulse**<br>Default value: 00<br>00: 1 msec(Default)<br>01: 2 msec<br>10: 3 msec<br>11: Infinity for level sense |

## Page 0 / Register 112 (Hex 0x70)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 112 | 0x70 | RSV | RSV | RSV | RSV | RSV | PWRDN | SLEEP | STBY |
| Reset Value | | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **PWRDN** | **Enter Analog Power Down state**<br>Default value: 0<br>0: Power Up (Default)<br>1: Power Down |
| **SLEEP** | **Enter the Device Sleep state, once the chip goes into SLEEP state, Energysense application will be triggered.**<br>Default value: 0<br>0: Power Up (Default)<br>1: Sleep |
| **STBY** | **Enter Digital Stand-by state**<br>Default value: 0<br>0: Run (Default)<br>1: Stand-by |

## Page 0 / Register 113 (Hex 0x71)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 113 | 0x71 | 2CH | RSV | FLT | HPF_EN | MUTE_CH2_R | MUTE_CH2_L | MUTE_CH1_R | MUTE_CH1_L |
| Reset Value | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **2CH** | **DSP_CTRL**<br>Select the processing mode for 4 channel device only. This configuration CANNOT be changed 'on the fly' in RUN state.<br>Default value: 0<br>0: 4 channels (Default) |

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| | |
|---|---|
| | 1: 2 channels |
| **FLT** | **Select the decimation filter type**<br>Default value: 0<br>0: Normal (Default)<br>1: Short Latency |
| **HPF_EN** | **Enable high-pass filter**<br>Default value: 1<br>0: Disable<br>1: Enable (Default) |
| **MUTE_CH2_R** | **Mute Ch2(R)**<br>Default value: 0<br>0: Unmute (Default)<br>1: Mute |
| **MUTE_CH2_L** | **Mute Ch2(L)**<br>Default value: 0<br>0: Unmute (Default)<br>1: Mute |
| **MUTE_CH1_R** | **Mute Ch1(R)**<br>Default value: 0<br>0: Unmute (Default)<br>1: Mute |
| **MUTE_CH1_L** | **Mute Ch1(L)**<br>Default value: 0<br>0: Unmute (Default)<br>1: Mute |

## Page 0 / Register 114 (Hex 0x72)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 114 | 0x72 | RSV | RSV | RSV | RSV | STATE3 | STATE2 | STATE1 | STATE0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **STATE[3:0]** | **Device Current Status**<br>Current Power State of the device<br>Default value: 0000<br>0000: Power Down<br>0001: Wait clock stable<br>0010: Release reset<br>0011: Stand-by<br>0100: Fade IN<br>0101: Fade OUT<br>0110: (Reserved)<br>0111: (Reserved)<br>1000: (Reserved)<br>1001: (Sleep) |


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| | |
|---|---|
| | 1010: (Reserved))<br>1011: (Reserved)<br>1100: (Reserved)<br>1101: (Reserved)<br>1110: (Reserved)<br>1111: Run |

## Page 0 / Register 115 (Hex 0x73)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 115 | 0x73 | RSV | RSV | RSV | RSV | RSV | INFO2 | INFO1 | INFO0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **INFO[2:0]** | **Current Sampling Frequency**<br>Default value: 000<br>000: Out of range (Low) or LRCK Halt<br>001: 8kHz<br>010: 16kHz<br>011: 32-48kHz<br>100: 88.2-96kHz<br>101: 176.4-192kHz<br>110: Out of range (High)<br>111: Invalid Fs |

## Page 0 / Register 116 (Hex 0x74)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 116 | 0x74 | RSV | BCK_RATIO2 | BCK_RATIO1 | BCK_RATIO0 | RSV | SCK_RATIO2 | SCK_RATIO1 | SCK_RATIO0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **BCK_RATIO[2:0]** | **Current receiving BCK ratio**<br>Default value: 000<br>000: Out of range (L) or BCK Halt<br>001: 32<br>010: 48<br>011: 64<br>100: 256<br>101: (Not assigned)<br>110: Out of range (H)<br>111: Invalid BCK ratio or LRCK Halt |
| **SCK_RATIO[2:0]** | **Current SCK Ratio**<br>Default value: 000<br>000: Out of range (L) or SCK Halt<br>001: 128<br>010: 256<br>011: 384<br>100: 512<br>101: 768 |

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| | |
|---|---|
| | 110: Out of range (H)<br>111: Invalid SCK ratio or LRCK Halt |

## Page 0 / Register 117 (Hex 0x75)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 117 | 0x75 | RSV | LRCKHLT | BCKHLT | SCKHTL | RSV | LRCKERR | BCKERR | SCKERR |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **LRCKHLT** | **CLK_ERR_STAT**<br>LRCK Halt Status<br>Default value: 0<br>0: No Error<br>1: Halt |
| **BCKHLT** | **BCK Halt Status**<br>Default value: 0<br>0: No Error<br>1: Halt |
| **SCKHTL** | **SCK Halt Status**<br>Default value: 0<br>0: No Error<br>1: Halt |
| **LRCKERR** | **LRCK Error Status**<br>Default value: 0<br>0: No Error<br>1: Error |
| **BCKERR** | **BCK Error Status**<br>Default value: 0<br>0: No Error<br>1: Error |
| **SCKERR** | **SCK Error Status**<br>Default value: 0<br>0: No Error<br>1: Error |

## Page 0 / Register 120 (Hex 0x78)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 120 | 0x78 | RSV | RSV | RSV | RSV | RSV | DVDD | AVDD | LDO |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DVDD** | **DVDD Status**<br>Default value: 0<br>0:Bad/Missing<br>1:Good |


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| | |
|---|---|
| **AVDD** | **AVDD Status**<br>Default value: 0<br>0:Bad/Missing<br>1:Good |
| **LDO** | **Digital LDO Status**<br>Default value: 0<br>0:Bad/Missing<br>1:Good |

### 14.2.3 Page 1 Registers

**Page 1 / Register 1 (Hex 0x01)**

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 0x01 | RSV | RSV | RSV | DONE | RSV | BUSY | R_REQ | W_REQ |
| Reset Value | | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **DONE** | Default value: 1<br>1: Access done<br>0: Accessing now |
| **BUSY** | Default value: 1<br>1: Access ready<br>0: Busy |
| **R_REQ** | **Memory Mapper Register Access to DSP-2 - READ**<br>Default value: 1<br>1: Access ready<br>0: Busy |
| **W_REQ** | **Memory Mapper Register Access to DSP-2 - WRITE**<br>Default value: 1<br>1: Access ready<br>0: Busy |

**Page 1 / Register 2 (Hex 0x02)**

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 2 | 0x02 | RSV | MEM_ADDR[6:0]6 | MEM_ADDR[6:0]5 | MEM_ADDR[6:0]4 | MEM_ADDR[6:0]3 | MEM_ADDR[6:0]2 | MEM_ADDR[6:0]1 | MEM_ADDR[6:0]0 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **MEM_ADDR[6:0][6:0]** | **Memory Mapped Register Address**<br>Status of the memory mapped register access<br>Default value: 0000000 |

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### Page 1 / Register 4 (Hex 0x04)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 4 | 0x04 | MEM_WDATA_07 | MEM_WDATA_06 | MEM_WDATA_05 | MEM_WDATA_04 | MEM_WDATA_03 | MEM_WDATA_02 | MEM_WDATA_01 | MEM_WDATA_00 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **MEM_WDATA_0 [7:0]** | **Write Data to 24bit memory[23:16]**<br>COEFFICIENT [23:16]<br>Default value: 00000000 |

### Page 1 / Register 5 (Hex 0x05)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 5 | 0x05 | MEM_WDATA_17 | MEM_WDATA_16 | MEM_WDATA_15 | MEM_WDATA_14 | MEM_WDATA_13 | MEM_WDATA_12 | MEM_WDATA_11 | MEM_WDATA_10 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **MEM_WDATA_1[7:0]** | **Write Data to 24bit memory - [15:8]**<br>COEFFICIENT [15:8]<br>Default value: 00000000 |

### Page 1 / Register 6 (Hex 0x06)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 6 | 0x06 | MEM_WDATA_27 | MEM_WDATA_26 | MEM_WDATA_25 | MEM_WDATA_24 | MEM_WDATA_23 | MEM_WDATA_22 | MEM_WDATA_21 | MEM_WDATA_20 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **MEM_WDATA_2[7:0]** | **Write Data to 24bit memory - [7:0]**<br>COEFFICIENT [7:0]<br>Default value: 00000000 |

### Page 1 / Register 7 (Hex 0x07)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 7 | 0x07 | MEM_WDATA_3 | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **MEM_WDATA_3** | **Write Data to 24bit memory - Reserved**<br>RESERVED |

### Page 1 / Register 8 (Hex 0x08)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 8 | 0x08 | MEM_RDATA_07 | MEM_RDATA_06 | MEM_RDATA_05 | MEM_RDATA_04 | MEM_RDATA_03 | MEM_RDATA_02 | MEM_RDATA_01 | MEM_RDATA_00 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **MEM_RDATA_0 [7:0]** | **Read Data from 24bit memory[23:16]**<br>COEFFICIENT [23:16]<br>Default value: 00000000 |

### Page 1 / Register 9 (Hex 0x09)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 9 | 0x09 | MEM_RDATA_17 | MEM_RDATA_16 | MEM_RDATA_15 | MEM_RDATA_14 | MEM_RDATA_13 | MEM_RDATA_12 | MEM_RDATA_11 | MEM_RDATA_10 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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| | |
|---|---|
| **MEM_RDATA_1[7:0]** | **Read Data from 24bit memory - [15:8]**<br>COEFFICIENT [15:8]<br>Default value: 00000000 |

### Page 1 / Register 10 (Hex 0x0A)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 10 | 0x0A | MEM_RDATA_27 | MEM_RDATA_26 | MEM_RDATA_25 | MEM_RDATA_24 | MEM_RDATA_23 | MEM_RDATA_22 | MEM_RDATA_21 | MEM_RDATA_20 |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **MEM_RDATA_2[7:0]** | **Read Data from 24bit memory - [7:0]**<br>COEFFICIENT [7:0]<br>Default value: 00000000 |

### Page 1 / Register 11 (Hex 0x0B)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 11 | 0x0B | MEM_RDATA_3 | RSV | RSV | RSV | RSV | RSV | RSV | RSV |
| Reset Value | | | | | | | | | |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **MEM_RDATA_3** | **Read Data from 24bit memory - Reserved**<br>RESERVED |

## 14.2.4 Page 3 Registers

### Page 3 / Register 18 (Hex 0x12)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 18 | 0x12 | RSV | RSV | RSV | RSV | RSV | RSV | RSV | PD |
| Reset Value | | | | | | | | | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **PD** | Oscillator Power Down Control<br>Default value: 0<br>0: Power up (Default)<br>1: Power down |

### Page 3 / Register 21 (Hex 0x15)

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 21 | 0x15 | RSV | RSV | RSV | TERM | RSV | RSV | RSV | PDZ |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **TERM** | **Mic Bias Control**<br>Mic bias resistor bypass (Write only)<br>Default value: 0<br>0: Disable (Default)<br>1: Enable |
| **PDZ** | **Mic Bias Control** |

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| | |
|---|---|
| | Mic bias control (Write only)<br>Default value: 1<br>0: Power down<br>1: Power up (Default) |

### 14.2.5 Page 253 Registers

**Page 253 / Register 20 (Hex 0x14)**

| Dec | Hex | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 20 | 0x14 | PGA_ICI1 | PGA_ICI0 | REF_ICI1 | REF_ICI0 | RSV | RSV | RSV | RSV |
| Reset Value | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | |
|---|---|
| **RSV** | **Reserved**<br>Reserved. Do not access. |
| **PGA_ICI[1:0]** | **PGA_ICI**<br>PGA bias current trim<br>Default value: 00<br>00: 100% (default)<br>01: Reserved<br>10: 75%<br>11: Reserved |
| **REF_ICI[1:0]** | <br>Global bias current trim<br>Default value: 00<br>00: 100% (default)<br>01: 75%<br>10: Reserved<br>11: Reserved |

## 14.3 Programming DSP Coefficients

The two fixed function DSPs on chip can have coefficients for filters and mixers programmed to them. This is done indirectly using specific registers on Page 1 (see Register map). See SLAC663 for more details.

The internal DSP coefficient memory space is mapped as follows:

**Table 21. Virtual 24bit DSP Coefficient Registers**

| | Coefficient | Address | Description |
|---|---|---|---|
| Mixer-1 | MIX1_CH1L | 0x00 | 4.20 Format |
| | MIX1_CH1R | 0x01 | |
| | MIX1_CH2L | 0x02 | |
| | MIX1_CH2R | 0x03 | |
| | MIX1_I2SL | 0x04 | |
| | MIX1_I2SR | 0x05 | |
| Mixer-2 | MIX2_CH1L | 0x06 | |
| | MIX2_CH1R | 0x07 | |
| | MIX2_CH2L | 0x08 | |
| | MIX2_CH2R | 0x09 | |
| | MIX2_I2SL | 0x0A | |
| | MIX2_I2SR | 0x0B | |
| Mixer-3 | MIX3_CH1L | 0x0C | |
| | MIX3_CH1R | 0x0D | |


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## Programming DSP Coefficients (continued)

**Table 21. Virtual 24bit DSP Coefficient Registers (continued)**

| | Coefficient | Address | Description |
|---|---|---|---|
| | MIX3_CH2L | 0x0E | |
| | MIX3_CH2R | 0x0F | |
| | MIX3_I2SL | 0x10 | |
| | MIX3_I2SR | 0x11 | |
| Mixer-4 | MIX4_CH1L | 0x12 | |
| | MIX4_CH1R | 0x13 | |
| | MIX4_CH2L | 0x14 | |
| | MIX4_CH2R | 0x15 | |
| | MIX4_I2SL | 0x16 | |
| | MIX4_I2SR | 0x17 | |
| Secondary ADCLPF/HPF | LPF_B0 | 0x20 | 1.23 Format |
| Coefficients | LPF_B1 | 0x21 | |
| | LPF_B2 | 0x22 | |
| | LPF_A1 | 0x23 | |
| | LPF_A2 | 0x24 | |
| | HPF_B0 | 0x25 | |
| | HPF_B1 | 0x26 | |
| | HPF_B2 | 0x27 | |
| | HPF_A1 | 0x28 | |
| | HPF_A2 | 0x29 | |
| Energysense | Loss_threshold | 0x2C | 1.23 Format |
| Energysense | Resume_threshold | 0x2D | |

An example of how to write to these registers is shown below

For example, change the Energysense resume threshold value to -30 dB (0x040C37)

Write 0x00 0x01 ; # change to register bank 1

Read 0x01 # if value is 0x17 then continue (check if system is still writing/reading)

Write 0x02 0x2D ; # write the memory address of resume threshold

Write 0x04 0x04 ; # bit[23:15]

Write 0x05 0x0C ; # bit[15:8]

Write 0x06 0x37 ; # bit[7:0]

Write 0x01 0x01 ; # execute write operation

Write 0x00 0x01 ; # Dummy write to latch data from register space to internal DSP memory space

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# 15 Device and Documentation Support

## 15.1 Development Support

See the PCM1865-Q1 EVM User's Guide, SLAU559

## 15.2 Trademarks

Bluetooth is a registered trademark of Bluetooth SIG, Inc..
All other trademarks are the property of their respective owners.

## 15.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 15.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 16 Mechanical, Packaging, and Orderable Information

The following packaging information and addendum reflect the most current data available for the designated devices. This data is subject to change without notice and revision of this document.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM1865QDBTRQ1 | ACTIVE | TSSOP | DBT | 30 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | PCM1865Q1 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF PCM1865-Q1 :**

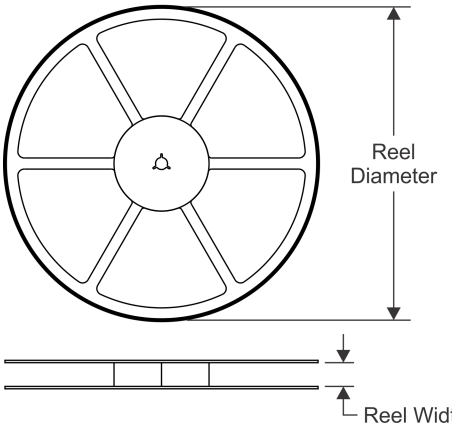
- Catalog: PCM1865

NOTE: Qualified Version Definitions:

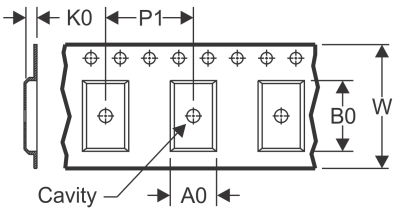
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

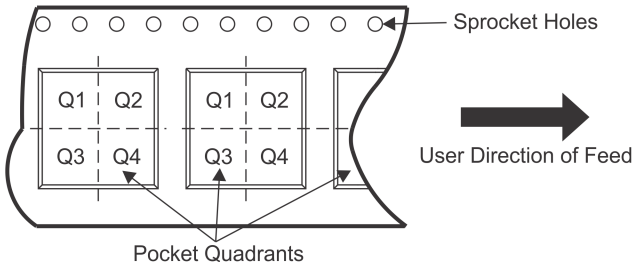



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

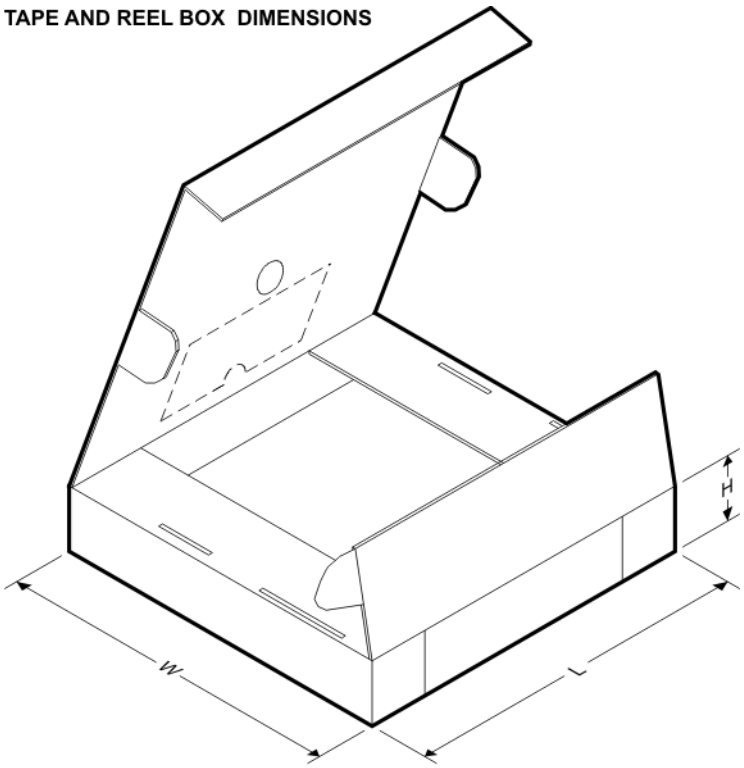
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PCM1865QDBTRQ1 | TSSOP | DBT | 30 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

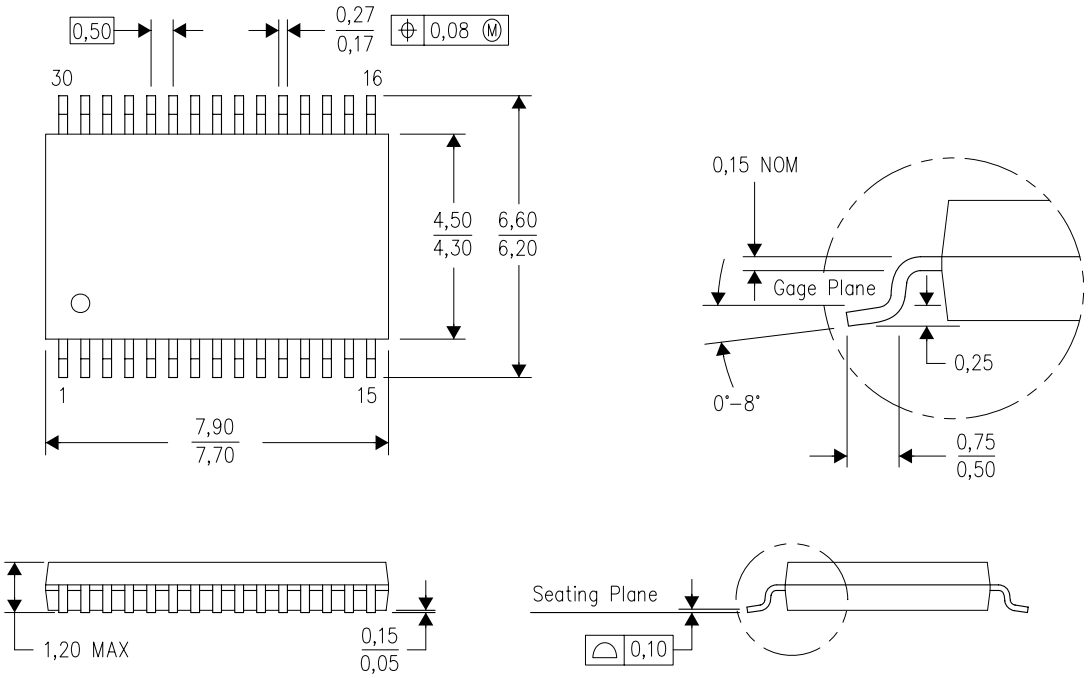
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| PCM1865QDBTRQ1 | TSSOP | DBT | 30 | 2000 | 367.0 | 367.0 | 38.0 |

DBT (R–PDSO–G30) PLASTIC SMALL OUTLINE




4073252–5/I 03/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153.

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