Adjustable Output 1-/2-/3-Phase Synchronous Buck Controller

Preliminary Technical Data

ADP3182

FEATURES

- **Selectable 1-, 2-, or 3-phase operation at up to 1 MHz per phase**
- **±2% Worst-case differential sensing error over temperature**
- **Externally adjustable 0.8 V to 5 V output from a 12 V supply**
- **Logic-level PWM outputs for interface to external high-power drivers**
- **Active current balancing between all output phases**
- **Built-in power good/crowbar functions**
- **Programmable short circuit protection with programmable latch-off delay**

APPLICATIONS

- **Auxiliary supplies**
- **DDR memory supplies**
- **Point-of-load modules**

GENERAL DESCRIPTION

The ADP3182 is a highly efficient multi-phase synchronous buck switching regulator controller optimized for converting a 12 V main supply into a high-current low voltage supply for use in point-of-load (POL) applications. It uses a multi-mode PWM architecture to drive the logic-level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The phase relationship of the output signals can be programmed to provide 1-, 2-, or 3-phase operation, allowing for the construction of up to three complementary buck switching stages.

The ADP3182 also provides accurate and reliable short circuit protection and adjustable current limiting.

ADP3182 is specified over the commercial temperature range of 0°C to +85°C and is available in a 20-lead QSOP package.

FUNCTIONAL BLOCK DIAGRAM

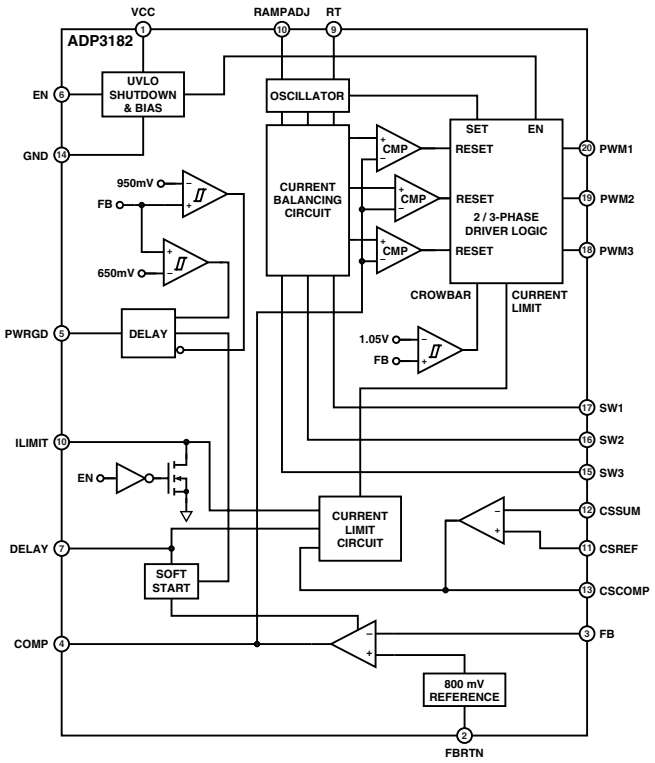


Figure 1.

Rev. PrB

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REVISION HISTORY

Revision PrA: Initial Version

Revision PrB: Updated electrical table, added theory of operation section and typical application circuit

SPECIFICATIONS

VCC = 12 V, FBRTN = GND, T_A = 0°C to 85°C, unless otherwise noted.[1]

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
OSCILLATOR						
Frequency Range	f_{OSC}		0.25		3	MHz
Frequency Variation	f_{PHASE}	T_A = 25°C, R_T = 332 kΩ, 3-phase	155	200	245	kHz
		T_A = 25°C, R_T = 154 kΩ, 3-phase		400		kHz
		T_A = 25°C, R_T = 100 kΩ, 3-phase		600		kHz
Output Voltage	V_{RT}	R_T = 100 kΩ to GND	1.9	2.0	2.1	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ – FB	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		0		100	µA
VOLTAGE ERROR AMPLIFIER						
Output Voltage Range[2]	V_{COMP}		0.3		3.1	V
Accuracy	V_{FB}	Referenced to FBRTN	784	800	816	mV
Line Regulation	ΔV_{FB}	VCC = 10 V to 14 V		0.05		%
Input Bias Current	I_{FB}	FB = 800 mV	-4		+4	µA
FBRTN Current	I_{FBRTN}			100	140	µA
Output Current	$I_{O(ERR)}$	FB forced to V_{OUT} – 3%		500		µA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		C_{COMP} = 10 pF		25		V/µs
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM – CSREF, Figure 2	−5.5		+5.5	mV
Input Bias Current	$I_{BIAS(CSSUM)}$		−50		+50	nA
Gain Bandwidth Product	$GBW_{(CSA)}$			10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/µs
Input Common-Mode Range		CSSUM and CSREF	0		VCC–2.5	V
Output Voltage Range			0.05		VCC–2.5	V
Output Current	I_{CSCOMP}			500		µA
CURRENT BALANCE CIRCUIT						
Common-Mode Range	$V_{SW(X)CM}$		−600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0 V	20	30	40	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0 V	4	7	10	µA
Input Current Matching	$\Delta I_{SW(X)}$	SW(X) = 0 V	−7		+7	%
CURRENT LIMIT COMPARATOR						
Output Voltage						
Normal Mode	$V_{ILIMIT(NM)}$	EN > 2 V, R_{ILIMIT} = 250 kΩ	2.9	3	3.1	V
In Shutdown Mode	$V_{ILIMIT(SD)}$	EN < 0.8 V, I_{ILIMIT} = -100 µA			400	mV
Output Current, Normal Mode	$I_{ILIMIT(NM)}$	EN > 2 V, R_{ILIMIT} = 250 kΩ		12		µA
Maximum Output Current			60			µA
Current Limit Threshold Voltage	V_{CL}	$V_{CSREF} – V_{CSCOMP}$, R_{ILIMIT} = 250 kΩ	105	125	145	mV
Current Limit Setting Ratio		V_{CL}/I_{ILIMIT}		10.4		mV/µA
DELAY Normal Mode Voltage	$V_{DELAY(NM)}$	R_{DELAY} = 250 kΩ	2.9	3	3.1	V
DELAY Overcurrent Threshold	$V_{DELAY(OC)}$	R_{DELAY} = 250 kΩ	1.7	1.8	1.9	V
Latch-Off Delay Time	t_{DELAY}	R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF		1.5		ms
SOFT START						
Output Current, Soft-Start Mode	$I_{DELAY(SS)}$	During startup, DELAY < 2.4 V	15	20	25	µA
Soft-Start Delay Time	$t_{DELAY(SS)}$	R_{DELAY} = 250 kΩ, C_{DELAY} = 12 nF		500		µs

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ENABLE INPUT						
Input Low Voltage	$V_{IL(EN)}$				0.8	V
Input High Voltage	$V_{IH(EN)}$		2.0			V
Input Current	$I_{IN(EN)}$		-1		+1	μA
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to FBRTN	600	660	720	mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to FBRTN	880	940	1000	mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 4 mA		225	400	mV
Power Good Delay Time				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to FBRTN	0.975	1.05	1.1	V
Crowbar Reset Point		Relative to FBRTN	550	650	750	mV
Crowbar Delay Time	$t_{CROWBAR}$	Overvoltage to PWM going low		400		ns
PWM OUTPUTS						
Output Low Voltage	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = −400 μA		160	500	mV
Output High Voltage	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400 μA	4.0	5		V
SUPPLY						
DC Supply Current				5	10	mA
UVLO Threshold Voltage	V_{UVLO}	VCC rising	6.5	6.9	7.3	V
UVLO Hysteresis			0.7	0.9	1.1	V

[1] All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC).
[2] Guaranteed by design or bench characterization, not tested in production.

TEST CIRCUITS

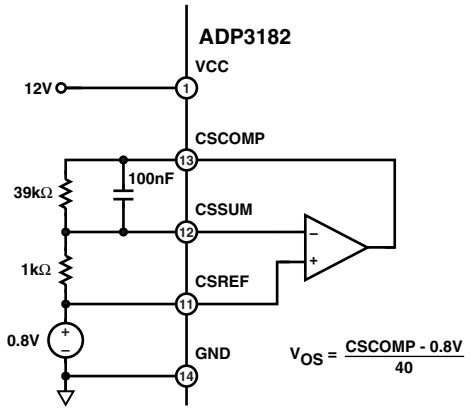


Figure 2. Current Sense Amplifier V_{OS}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC	−0.3 V to +15 V
FBRTN	−0.3 V to +0.3 V
EN, DELAY, ILIMIT, CSCOMP, RT, PWM1 – PWM3, COMP	−0.3 V to 5.5 V
SW1 – SW3	−5 V to +25 V
All Other Inputs and Outputs	−0.3 V to VCC + 0.3 V
Storage Temperature	−65°C to +150°C
Operating Ambient Temperature Range	0°C to 85°C
Operating Junction Temperature	125°C
Thermal Impedance (θ_{JA})	100°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Infrared (15 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified all other voltages re referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTION

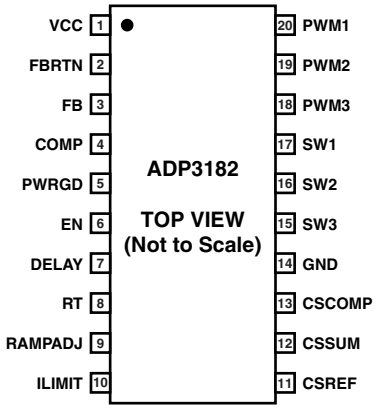


Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC	Supply Voltage for the Device.
2	FBRTN	Feedback Return. Voltage error amplifier reference for remote sensing of the output voltage.
3	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor divider between the output and FBRTN connected to this pin sets the output voltage point. This pin is also the reference point for the power good and crowbar comparators.
4	COMP	Error Amplifier Output and Compensation Point.
5	PWRGD	Power Good Output. Open-drain output that signals when the output voltage is outside the proper operating range.
6	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
7	DELAY	Soft-Start Delay and Current Limit Latch-Off Delay Setting Input. An external resistor and capacitor connected between this pin and GND sets the soft-start ramp-up time and the overcurrent latch-off delay time.
8	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
9	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
10	ILIMIT	Current Limit Setpoint/Enable Output. An external resistor from this pin to GND sets the current limit threshold of the converter. This pin is actively pulled low when the ADP3182 EN input is low, or when VCC is below its UVLO threshold, to signal to the driver IC that the driver high-side and low-side outputs should go low.
11	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier. This pin should be connected to the common point of the output inductors.
12	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
13	CSCOMP	Current Sense Compensation Point. A resistor and a capacitor from this pin to CSSUM determines the gain of the current sense amplifier.
14	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
15 to 17	SW3 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
18 to 20	PWM3 to PMW1	Logic-Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3418. Connecting the PWM3 output to GND causes that phase to turn off, allowing the ADP3182 to operate as a 1- or 2-phase controller.

TYPICAL PERFORMANCE CHARACTERISTICS

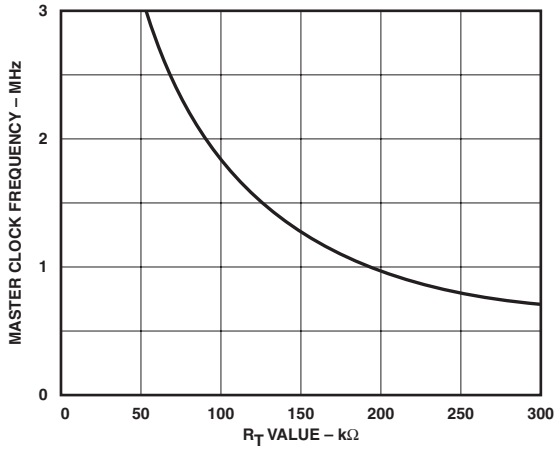


Figure 4. Master Clock Frequency vs. R_T

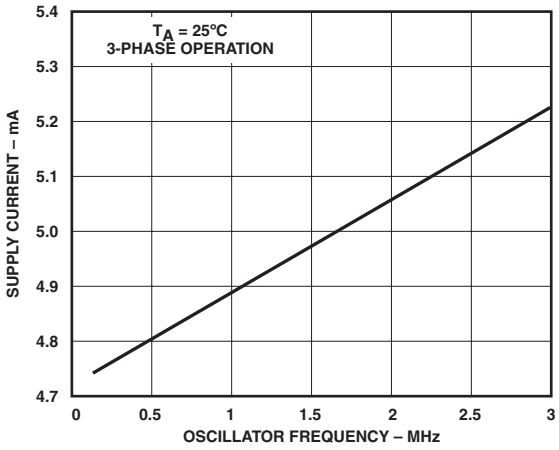


Figure 5. Supply Current vs. Oscillator Frequency

THEORY OF OPERATION

The ADP3182 combines a multi-mode, fixed frequency PWM control with multi-phase logic outputs for use in 1-, 2-, and 3-phase synchronous buck point-of-load supply power converters. Multiphase operation is important for producing the high currents and low voltages demanded by auxiliary supplies in desktop computers, workstations, and servers. Handling the high currents in a single-phase converter would place high thermal demands on the components in the system such as the inductors and MOSFETs.

The multimode control of the ADP3182 ensures a stable, high performance topology for

- Balancing currents and thermals between phases
- High speed response at the lowest possible switching frequency and output decoupling
- Minimizing thermal switching losses due to lower frequency operation
- Tight load line regulation and accuracy
- Reduced output ripple due to multiphase cancellation
- PC board layout noise immunity
- Ease of use and design due to independent component selection
- Flexibility in operation for tailoring design to low cost or high performance

START-UP SEQUENCE

During start-up, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the ADP3182 operates as a 3-phase PWM controller. Grounding the PWM3 pin programs 1/2-phase operation.

When the ADP3182 is enabled, the controller outputs a voltage on PWM3 which is approximately 675 mV. An internal comparator checks the pin's voltage versus a threshold of 300 mV. If the pin is grounded, it is below the threshold and the phase is disabled. The output resistance of the PWM pin is approximately 5 kΩ during this detection time. Any external pull-down resistance connected to the PWM pin should not be less than 25 kΩ to ensure proper operation. PWM1 and PWM2 are disabled during the phase detection interval, which occurs during the first two clock cycles of the internal oscillator. After this time, if the PWM output is not grounded, the 5 kΩ resistance is removed. and it switches between 0 V and 5 V. If the PWM output was grounded, it remains off.

The PWM outputs are logic-level devices intended for driving external gate drivers such as the ADP3418. Since each phase is monitored independently, operation approaching 100% duty cycle is possible. Also, more than one output can be on at the same time for overlapping phases.

MASTER CLOCK FREQUENCY

The clock frequency of the ADP3182 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 4. To determine the frequency per phase, the clock is divided by the number of phases in use. If PWM3 is grounded, then divide the master clock by 2 for the frequency of the remaining two phases.

It is important to note that if only one phase is used, the clock will still be switching as if two phases were operating. This means that the oscillator frequency needs to be set at twice the expected value to program the desired PWM frequency.

OUTPUT VOLTAGE DIFFERENTIAL SENSING

The ADP3182 uses a differential sensing low offset voltage error amplifier. This maintains a worst-case specification of ±2% differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB and FBRTN pins. FB should be connected through a resistor to the regulation point, usually the local bypass capacitor for the load. FBRTN should be connected directly to the remote sense ground point. The internal precision reference is referenced to FBRTN, which has a minimal current of 100 μA to allow accurate remote sensing. The internal error amplifier compares the output of the reference to the FB pin to regulate the output voltage.

OUTPUT CURRENT SENSING

The ADP3182 provides a dedicated current sense amplifier (CSA) to monitor the total output current for current limit detection. Sensing the load current at the output gives the total average current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low-side MOSFET. This amplifier can be configured several ways depending on the objectives of the system:

- Output inductor DCR sensing without a thermistor for lowest cost
- Output inductor DCR sensing with a thermistor for improved accuracy with tracking of inductor temperature
- Sense resistors for highest accuracy measurements

The positive input of the CSA is connected to the CSREF pin, which is connected to the output voltage. The inputs to the amplifier are summed together through resistors from the sensing element (such as the switch node side of the output inductors) to the inverting input, CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier, and a filter capacitor is placed in parallel with this resistor. The

gain of the amplifier is programmable by adjusting the feedback resistor. The current information is then given as the difference of CSREF – CSCOMP. This difference signal is used as a differential input for the current limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors so that it can be made extremely accurate.

CURRENT CONTROL MODE AND THERMAL BALANCE

The ADP3182 has individual inputs for each phase, which are used for monitoring the current in each phase. This information is combined with an internal ramp to create a current balancing feedback system, which has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning described previously.

The magnitude of the internal ramp can be set to optimize the transient response of the system. It is also monitors the supply voltage for feed-forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp. External resistors can be placed in series with individual phases to create, if desired, an intentional current imbalance such as when one phase may have better cooling and can support higher currents. Resistors R_{SW1} through R_{SW3} (see the typical application circuit in Figure 8) can be used for adjusting thermal balance. It is best to have the ability to add these resistors during the initial design, so make sure that placeholders are provided in the layout.

To increase the current in any given phase, make R_{SW} for that phase larger (make R_{SW} = 0 for the hottest phase and do not change during balancing). Increasing R_{SW} to only 500 Ω makes a substantial increase in phase current. Increase each R_{SW} value by small amounts to achieve balance, starting with the coolest phase first.

VOLTAGE CONTROL MODE

A high gain-bandwidth voltage mode error amplifier is used for the voltage-mode control loop. The control input voltage to the positive input is derived from the internal 800 mV reference. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.

The negative input (FB) is tied to the center point of a resistor divider from the output sense location. The main loop compensation is incorporated into the feedback network between FB and COMP.

SOFT START

The power-on ramp-up time of the output voltage is set with a capacitor and resistor in parallel from the DELAY pin to ground. The RC time constant also determines the current limit latch off time as explained in the following section. In UVLO or when EN is a logic low, the DELAY pin is held at ground. After the UVLO threshold is reached and EN is a logic high, the DELAY capacitor is charged with an internal 20 μA current source. The output voltage follows the ramping voltage on the DELAY pin, limiting the inrush current. The soft-start time depends on the value of C_{DLY}, with a secondary effect from R_{DLY}.

If either EN is taken low or VCC drops below UVLO, the DELAY capacitor is reset to ground to be ready for another soft-start cycle. Figure 6 shows a typical soft-start sequence for the ADP3182.

TO BE ADDED

Figure 6. Typical Start-Up Waveforms
Channel 1: PWRGD, Channel 2: CSREF,
Channel 3: DELAY, Channel 4: COMP

CURRENT LIMIT, SHORT CIRCUIT, AND LATCH-OFF PROTECTION

The ADP3182 compares a programmable current limit set point to the voltage from the output of the current sense amplifier. The level of current limit is set with the resistor from the ILIMIT pin to ground. During normal operation, the voltage on ILIMIT is 3 V. The current through the external resistor is internally scaled to give a current limit threshold of 10.4 mV/μA. If the difference in voltage between CSREF and CSCOMP rises above the current limit threshold, the internal current limit amplifier controls the internal COMP voltage to maintain the average output current at the limit.

After the limit is reached, the 3 V pull-up on the DELAY pin is disconnected, and the external delay capacitor is discharged through the external resistor. A comparator monitors the DELAY voltage and shuts off the controller when the voltage drops below 1.8 V. The current limit latch-off delay time is therefore set by the RC time constant discharging from 3 V to 1.8 V.

Because the controller continues to cycle the phases during the latch-off delay time, if the short is removed before the 1.8 V threshold is reached, the controller returns to normal operation. The recovery characteristic depends on the state of PWRGD. If

the output voltage is within the PWRGD window, the controller resumes normal operation. However, if short circuit has caused the output voltage to drop below the PWRGD threshold, a soft-start cycle is initiated.

The latch-off function can be reset by either removing and reapplying VCC to the ADP3182, or by pulling the EN pin low for a short time. To disable the short circuit latch-off function, the external resistor to ground should be left open, and a high-value (>1 MΩ) resistor should be connected from DELAY to VCC. This prevents the DELAY capacitor from discharging, so the 1.8 V threshold is never reached. The resistor has an impact on the soft-start time because the current through it adds to the internal 20 μA current source.

During start-up when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit controls the internal COMP voltage to the PWM comparators to 2 V. This limits the voltage drop across the low-side MOSFETs through the current balance circuitry.

An inherent per phase current limit protects individual phases if one or more phases stops functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

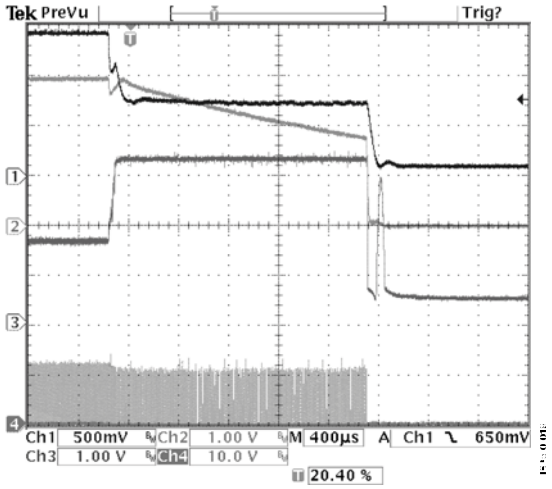


Figure 7. Overcurrent Latch-Off Waveforms
Channel 1: CSREF, Channel 2: DELAY,
Channel 3: COMP, Channel 4: Phase 1 Switch Node

POWER GOOD MONITORING

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open-drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the nominal limits specified in the electrical table. PWRGD goes low if the output voltage is outside of this specified range or whenever the EN pin is pulled low.

OUTPUT CROWBAR

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low-side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 650 mV.

Turning on the low-side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output over-voltage is due to a short in the high-side MOSFET, this action current-limits the input supply or blows its fuse, protecting the microprocessor from being destroyed.

OUTPUT ENABLE AND UVLO

For the ADP3182 to begin switching, the input supply (VCC) to the controller must be higher than the UVLO threshold, and the EN pin must be higher than its logic threshold. If UVLO is less than the threshold or the EN pin is a logic low, the ADP3182 is disabled. This holds the PWM outputs at ground, shorts the DELAY capacitor to ground, and holds the ILIMIT pin at ground.

In the application circuit, the ILIMIT pin should be connected to the $\overline{OD}$ pins of the ADP3418 drivers. The ILIMIT being grounded disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs were not disabled, a negative voltage could be generated during output due to the high current discharge of the output capacitors through the inductors.

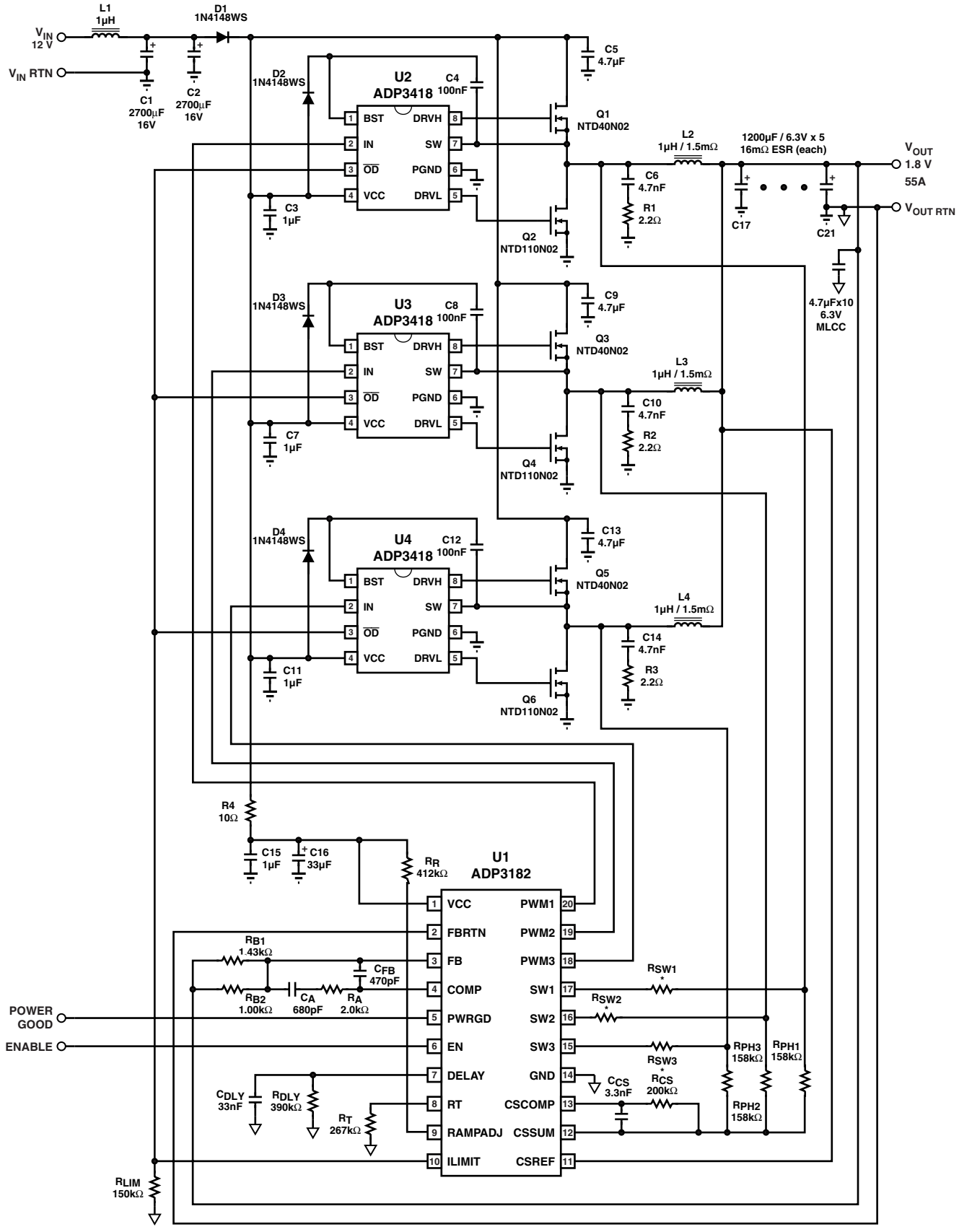


Figure 8. 1.8 V, 55 A Application Circuit

APPLICATIONS INFORMATION

LAYOUT AND COMPONENT PLACEMENT

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

General Recommendations

For good results, a PCB with at least four layers is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, power planes for ground, input and output power, and wide interconnection traces in the remainder of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~0.53 mΩ at room temperature.

Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.

If critical signal lines (including the output voltage sense lines of the ADP3182) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.

An analog ground plane should be used around and under the ADP3182 as a reference for the components associated with the controller. This plane should be tied to the nearest output decoupling capacitor ground and should not be tied to any other power circuitry to prevent power currents from flowing in it.

The components around the ADP3182 should be located close to the controller with short traces. The most important traces to keep short and away from other traces are the FB and CSSUM pins. The output capacitors should be connected as close as possible to the load or connector. If the load is distributed, the capacitors should also be distributed and generally be in proportion to where the load tends to be more dynamic.

Avoid crossing any signal lines over the switching power path loop, described in the following section.

Power Circuitry Recommendations

The switching power path should be routed on the PCB to encompass the shortest possible length in order to minimize radiated switching noise energy (i.e., EMI) and conduction losses in the board. Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors and the power MOSFETs including all interconnecting PCB traces and planes. Using short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high energy ringing, and it accommodates the high current demand with minimal voltage loss.

Whenever a power dissipating component, for example, a power MOSFET, is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are improved current rating through the vias and improved thermal performance from vias extended to the opposite side of the PCB, where a plane can more readily transfer the heat to the air. Make a mirror image of any pad being used to heatsink the MOSFETs on the opposite side of the PCB to achieve the best thermal dissipation to the air around the board. To further improve thermal performance, use the largest possible pad area.

The output power path should also be routed to encompass a short distance. The output power path is formed by the current path through the inductor, the output capacitors, and the load.

For best EMI containment, a solid power ground plane should be used as one of the inner layers extending fully under all the power components.

Signal Circuitry Recommendations

The output voltage is sensed and regulated between the FB pin and the FBRTN pin, which connect to the signal ground at the load. To avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus, the FB and FBRTN traces should be routed adjacent to each other on top of the power ground plane back to the controller.

The feedback traces from the switch nodes should be connected as close as possible to the inductor. The CSREF signal should be connected to the output voltage at the nearest inductor to the controller.

OUTLINE DIMENSIONS

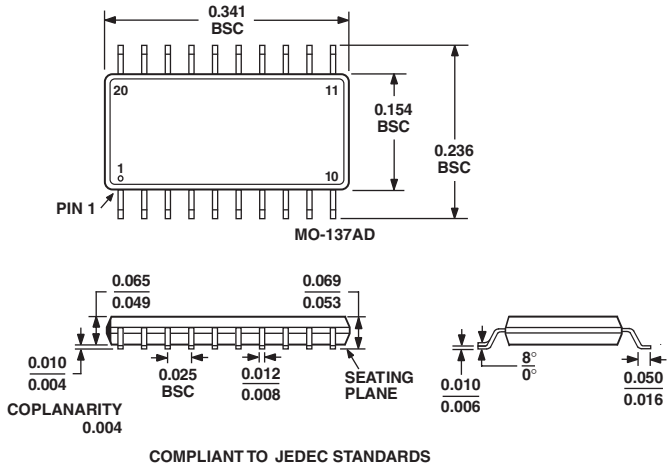


Figure 9. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Quantity per Reel
ADP3182JRQZ-REEL[1]	0°C to 85°C	Shrink SOIC 13″ Reel	RQ-20	2500

[1] Z = Pb-free part.

NOTES:

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