CN8330

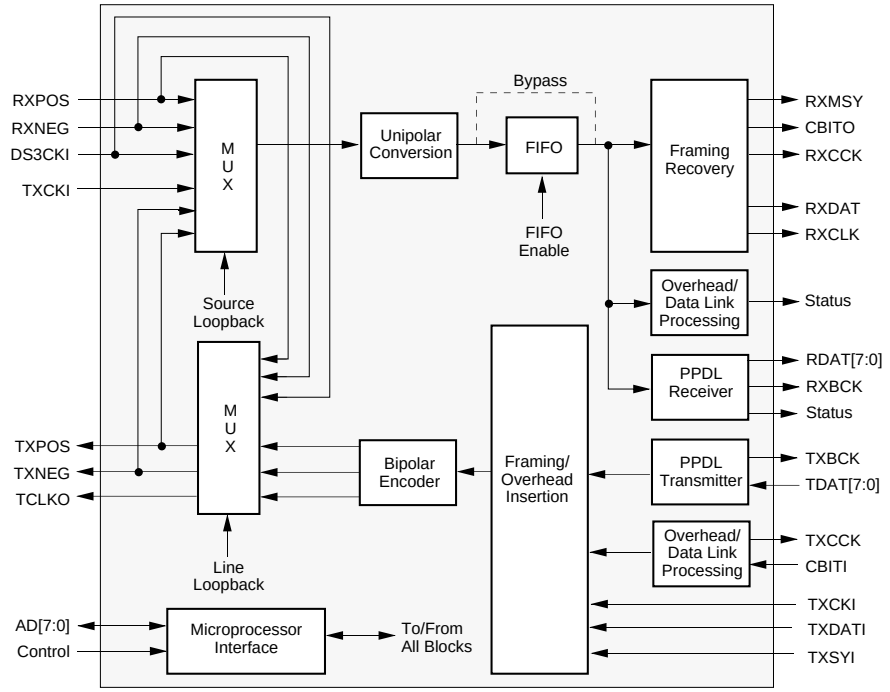
DS3/E3 Framer with 52 Mbps HDLC Controller

The CN8330 is an integral DS3/E3 framer designed to support the transmission formats defined by ANSI T1.107-1988, T1.107a-1989, T1.404, and ITU-T G.751 standards. All maintenance features required by Bellcore TR-TSY-000009 and AT&T PUB 54014 are provided. In addition, the CN8330 can be optionally configured as a High-Level Data Link Controller (HDLC) usable with or without DS3/E3 framing overhead.

The CN8330 provides framing recovery for M13, C-bit parity, Syntran, and G.751 E3 formatted signals. A First In First Out (FIFO) buffer in the receive path can be enabled to reduce jitter on the incoming data. Transmit and receive data is available to the host in either serial or parallel byte and nibble formats. Access is provided to the terminal data link and the Far End Alarm/Control (FEAC) channel, as specified in T1.107a-1989. Counters are included for frame-bit errors, Line Code Violations (LCVs), parity errors, and Far End Block Errors (FEBEs).

Two operational modes are available: microprocessor and stand-alone monitor control modes. The microprocessor control mode monitors all status conditions and provides configuration control. The stand-alone monitor mode allows the CN8330 to operate as a monitor providing status and alarm information on external pins.

Functional Block Diagram



Distinguishing Features

- Supports DS3/E3 framing modes
- Includes high-speed HDLC controller (52 MHz)
- Framing recovery for M13, C-bit parity, Syntran, and G.751 E3 signals
- Serial or parallel (octet or nibble) interface modes
- Average reframe time of less than 1 ms for DS3 and less than 250 µs for E3
- Supports the LAPD terminal data link and FEAC channel as defined in T1.107a-1989
- 68-pin PLCC or 80-pin MQFP surface-mount package
- Operates from a single +5 VDC ±5% power supply
- Low-power CMOS technology

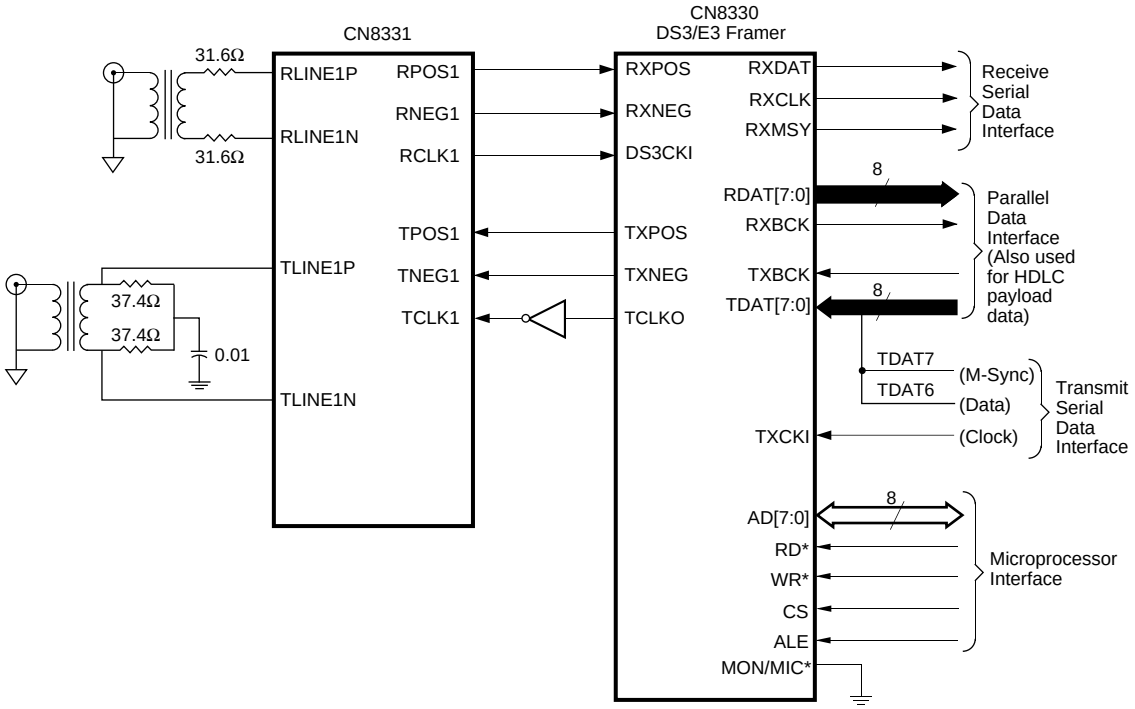
Applications

- Digital PCM switches
- Digital Cross-Connect Systems
- Channel Service Units (CSUs)
- Channel extenders
- ATM Switches/Concentrators
- PBXs
- Switched Multimegabit Digital Service (SMDS) Equipment
- Test equipment
- Routers (including HSSI ports)

Ordering Information

Model Number	Package	Ambient Temperature
CN8330EPJD	68-Pin Plastic Leaded Chip Carrier (PLCC)	–40 to 85° C
CN8330EPD	80-Pin Metric Quad Flat Pack (MQFP)	–40 to 85° C

CN8330 Typical DS3 Application



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1.0 Product Description

The CN8330 is a frame synchronization, recovery, and signal generation circuit. Applications for digital terminals include digital cross-connect systems, customer premise multiplexers, channel extenders, network managers, PBXs, Switched Multimegabit Digital Service (SMDS) equipment, and monitor or test equipment. The integrated circuit features a High-Level Data Link Control (HDLC) formatter usable with or without DS3/E3 framing. The CN8330 framer is designed to meet the requirements of DS3 and E3 transmission and reception formats as per ANSI T1.107-1988, T1.107a-1989, T1.404, and ITU-T G.751 standards. Both the LAPD terminal data link and the Far End Alarm Control (FEAC) channel, as defined in T1.107a-1989, are supported. All maintenance features required by Bellcore TR-TSY-000009 and AT&T PUB 54014 are furnished. HDLC data transmission according to ITU-T standard Q.921 and ISO 3309-1984 is supported, as are SMDS standards prETS 300 214 and TR-TSV-000773.

The framer provides framing recovery for M13, C-bit parity, and G.751 E3 formatted signals. The received data stream is available serially for unchannelized applications or for external decoding of the asynchronous multiplexed formats. The framing circuit has an average reframe time of less than 1 msec for DS3 signals and less than 250 µsec for E3 signals. A First In First Out (FIFO) buffer in the receive signal path can be enabled to reduce the jitter on the incoming data. The framer circuitry is capable of operating to 52 MHz, making it compatible with High-Speed Serial Interface (HSSI) signals or DS3 and E3 signals that are embedded in SONET STS-1 or SDH STM-1 carriers.

The transmitter can process serial data from an external pin, or in byte- or nibble-oriented data format from the Payload Parallel Data Link (PPDL) data port. DS3 overhead bits or E3 Frame Alignment Signal (FAS) bits are automatically inserted. The parallel data can be formatted with idle flags, zero stuffing for transparency, and a selectable 16- or 32-bit Frame Check Sequence (FCS). Bytes or nibbles without HDLC formatting can also be transmitted. The transmitter also generates an Alarm Indication Signal (AIS), idle code, yellow alarm, and all-ones signals. DS3 C-bits (or E3 N-bits) can be inserted into the data stream from an external source.

The circuit can be configured as a high-speed data formatter without inserting the CN8330 overhead bits. This allows the circuit to be used for data applications on communication links other than those requiring DS3 or E3 formatting. Data bytes can be formatted with HDLC flags and FCS bytes for transmission at any speed up to 52 MHz.

Configuration, control, and monitoring of the CN8330 termination circuit and framer are accomplished with a selectable microprocessor control mode that monitors all status conditions and provides configuration control. In DS3 mode a stand-alone mode of operation is featured. This allows the circuit to operate as a monitor and provide status and alarm indications to external processing or counting circuitry including:

- AIS, all-ones
- Yellow alarm
- Loss of signal
- Idle code detection
- Out-of-frame and frame-bit error counting
- Parity error
- LCV (Line Code Violation)
- Path parity
- X-bit disagreement
- FEBE event counting

The received DS3 C-bits (or E3 N-bits) are directed to an external pin to provide visibility for external processing, as required.

1.1 Pin Descriptions

The CN8330 Framer is packaged in a 68-pin Plastic Leaded Chip Carrier (PLCC) and an 80-pin Metric Quad Flat Pack (MQFP) and shown in Figure 1-1 and Figure 1-2 respectively. Pin assignments are listed in numerical order in Table 1-1. Figure 1-3 and Figure 1-4 illustrate functionally partitioned logic diagrams of the CN8330. Pin descriptions, labels, and I/O assignments are detailed in Table 1-2.

Figure 1-1. CN8330 Pinout Diagram - 68-Pin PLCC

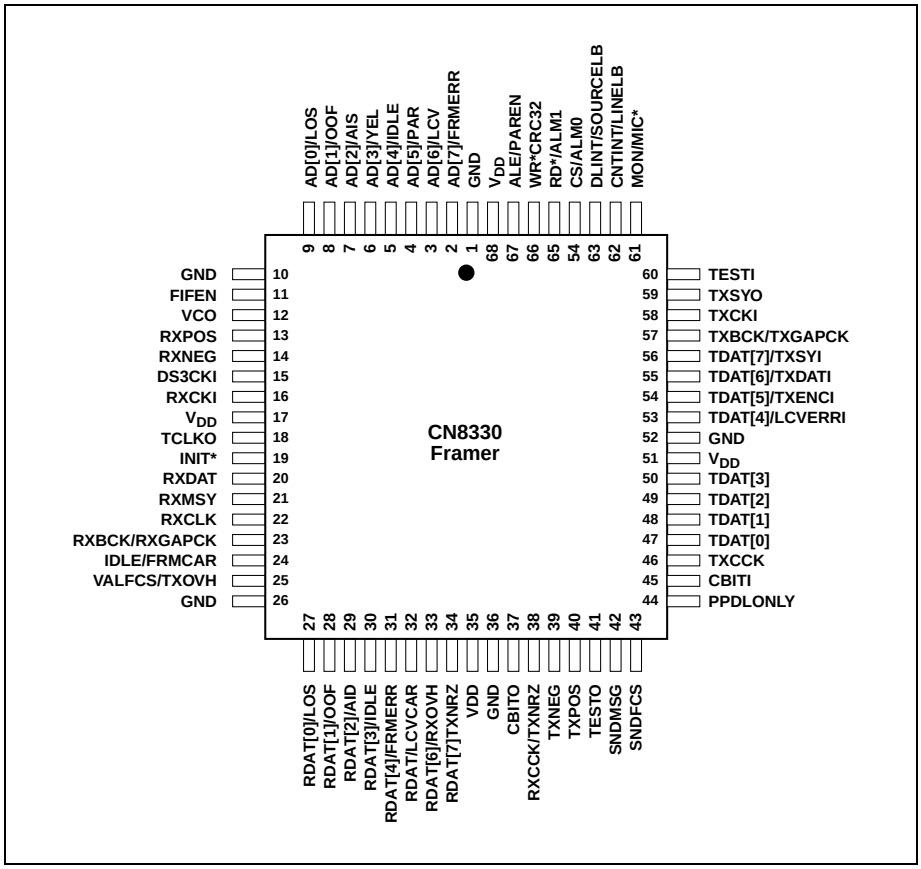


Figure 1-2. CN8330 Pinout Diagram - 80-Pin MQFP

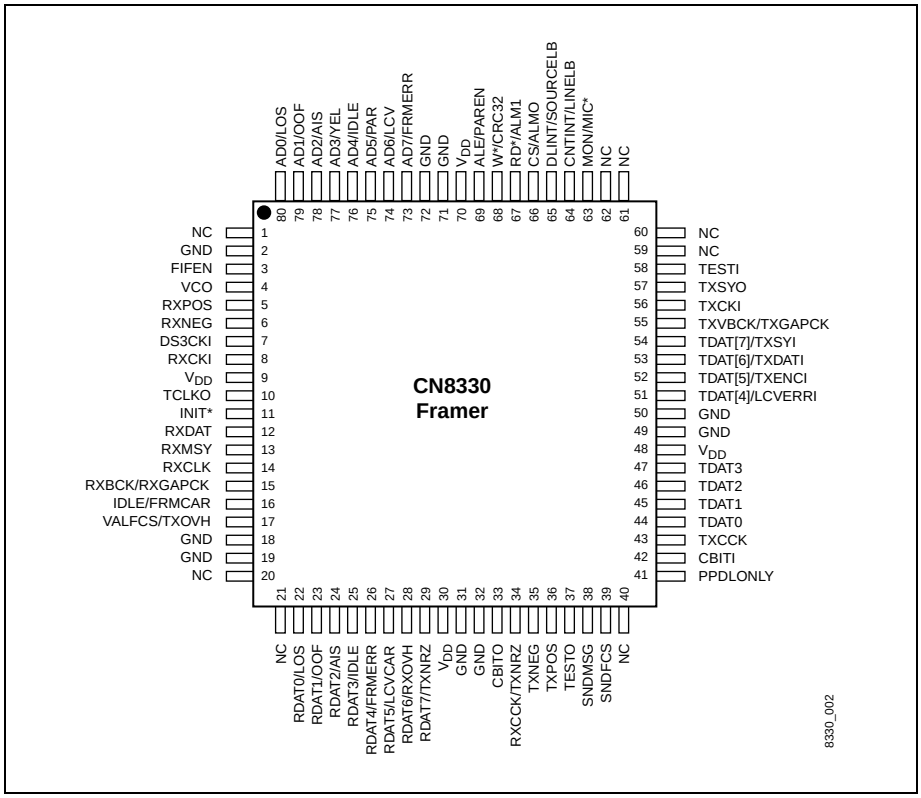


Table 1-1. Pin Descriptions

Pin (68-Pin PLCC)	Pin (80-Pin MQFP)	Pin Label	I/O
1	72	GND	I
2	73	AD[7]/FRMERR	B/O
3	74	AD[6]/LCV	B/O
4	75	AD[5]/PAR	B/O
5	76	AD[4]/IDLE	B/O
6	77	AD[3]YEL	B/O
7	78	AD[2]/AIS	B/O
8	79	AD[1]/OOF	B/O
9	80	AD[0]/LOS	B/O
10	2	GND	I
11	3	FIFEN	I
12	4	VCO	O
13	5	RXPOS	I
14	6	RXNEG	I
15	7	DS3CKI	I
16	8	RXCKI	I
17	9	V_{DD}	I
18	10	TCLKO	O
19	11	INIT*	I
20	12	RXDAT	O
21	13	RXMSY	O
22	14	RXCLK	O
23	15	RXBCK/RXGAPCK	O
24	16	IDLE/FRMCAR	O
25	17	VALFCS/TXOVH	O
26	18	GND	I
27	22	RDAT[0]/LOS	O
28	23	RDAT[1]/OOF	O
29	24	RDAT[2]/AIS	O
30	25	RDAT[3]/IDLE	O
31	26	RDAT[4]/FRMERR	O
32	27	RDAT[5]/LCVCAR	O
33	28	RDAT[6]/RXOVH	O
34	29	RDAT[7]/TXNRZ	O
35	30	V_{DD}	I
36	31	GND	I
37	33	CBITO	O
38	34	RXCCK/TXNRZ	O
39	35	TXNEG	O
40	36	TXPOS	O
41	37	TESTO	O
42	38	SNDMSG	I
43	39	SNDFCS	I
44	41	PPDLONLY	I
45	42	CBITI	I
46	43	TXCCK	O
47	44	TDAT[0]	I
48	45	TDAT[1]	I
49	46	TDAT[2]	I
50	47	TDAT[3]	I
51	48	V_{DD}	I
52	49	GND	I
53	51	TDAT[4]/LCVERRI	I
54	52	TDAT[5]/TXENCI	I
55	53	TDAT[6]/TXDATI	I
56	54	TDAT[7]/TXSYI	I
57	55	TXBCK/TXGAPCK	O
58	56	TXCKI	I
59	57	TXSYO	O
60	58	TESTI	I
61	63	MON/MIC*	I
62	64	CNTINT/LINELB	O/I
63	65	DLINT/SOURCELB	O/I
64	66	CS/ALM0	I
65	67	RD*/ALM1	I
66	68	WR*/CRC32	I
67	69	ALE/PAREN	I
68	70	V_{DD}	I
	1,20, 21,40, 59,60, 61,62	N/C	–
	19,32, 50,71	GND	I

Figure 1-3. CN8330 Framer Functional Logic Diagram - 68-Pin PLCC

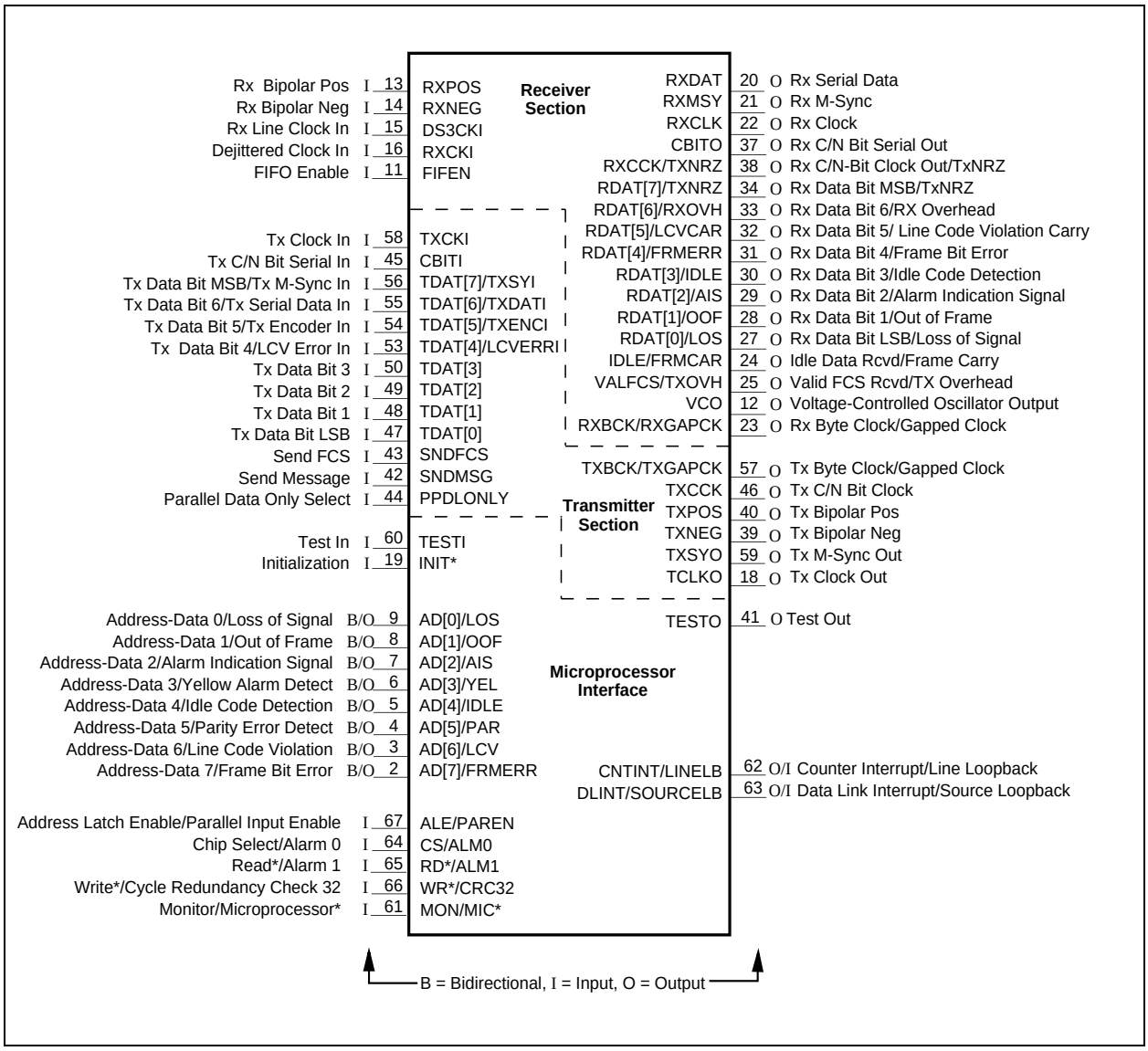


Figure 1-4. CN8330 Framer Functional Logic Diagram - 80-Pin MQFP

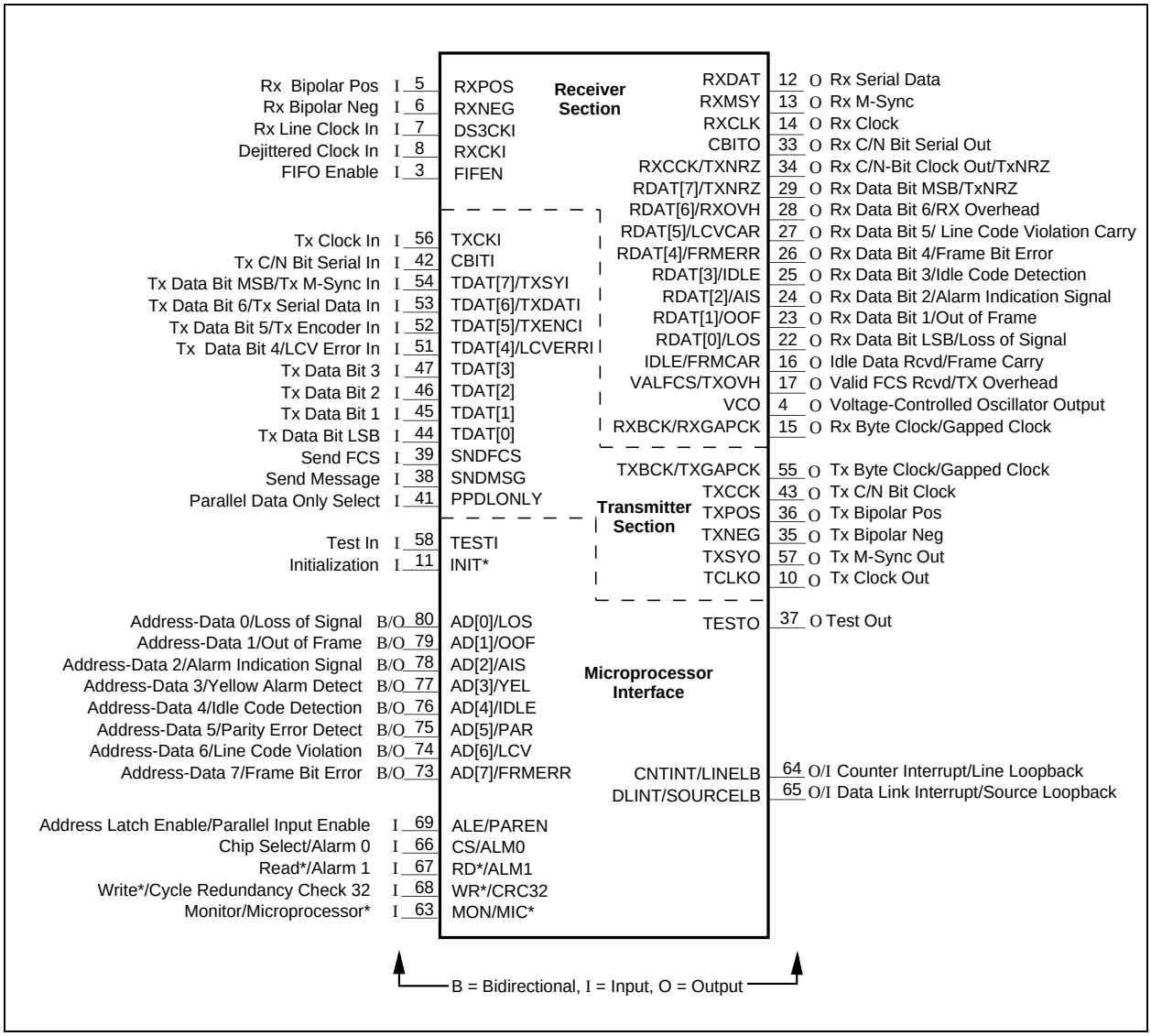


Table 1-2. Hardware Signal Definitions *(1 of 5)*

	Pin Label	Signal Name	I/O	Definition
Microprocessor Interface	ALE/PAREN	Address Latch Enable/Parallel Input Enable	I	A dual-purpose active-high signal which, when MON/MIC* is tied low, is microprocessor-generated and causes the CN8330 to latch in the address on the address-data bus. When MON/MIC* is tied high (stand-alone mode), the parallel input for the PPDL formatter is enabled. When this pin is tied low, transmit data is sourced from the serial input TDAT[6]/TXDAT.(1)
	CS/ALM0	Chip Select/Alarm 0	I	A dual-purpose signal that enables read/write functions when MON/MIC* is tied low, and controls AIS transmission in stand-alone mode when MON/MIC* is tied high. Both CS and ALM0 are active high signals.(1)
	RD*/ALM1	Read/Alarm 1	I	A dual-purpose signal that enables read data to be passed to the address-data bus when MON/MIC* is tied low, and controls idle code transmission in stand-alone mode when MON/MIC* is tied high, RD* is an active low signal and ALM1 is active-high.(1)
	WR*/CRC32	Write/Cycle Redundancy Check 32	I	A dual-purpose signal that latches write data from the address-data bus when MON/MIC* is tied low, and controls the Cycle Redundancy Check (CRC) when MON/MIC* is tied high. WR* is an active low signal. In stand-alone mode, a high-speed 32-bit CRC calculation is enabled if CRC32 is high; if low, a 16-bit calculation is performed.(1)
	MON/MIC*	Monitor/Microprocessor Mode Select	I	Selects either microprocessor mode when tied low, or stand-alone monitor mode when tied high. The state of MON/MIC* determines which function the dual-purpose pins (AD[7:0]) serve. The standalone mode is valid only in DS3 mode.(1)
	AD[0]/LOS	Address-Data 0/Loss of Signal	B/O	Part of the bidirectional 8-bit multiplexed address-data bus when MON/MIC* is tied low. When in stand-alone mode, this pin is an active-high monitor output indicating loss of signal.(1)
	AD[1]/OOF	Address-Data 1/Out of Frame	B/O	Part of the bidirectional 8-bit multiplexed address-data bus when MON/MIC* is tied low. When in stand-alone mode, this pin is an active-high monitor output indicating an out-of-frame state.(1)
	AD[2]/AIS	Address-Data 2/Alarm Indication Signal	B/O	Part of the bidirectional 8-bit multiplexed address-data bus when MON/MIC* is tied low. When in stand-alone mode, this pin is an active-high monitor output indicating alarm indication signal detection.(1)
	AD[3]/YEL	Address-Data 3/Yellow Alarm Detection	B/O	Part of the bidirectional 8-bit multiplexed address-data bus when MON/MIC* is tied low. When in stand-alone mode, this pin is an active-high monitor output indicating a yellow alarm.(1)

Table 1-2. Hardware Signal Definitions *(2 of 5)*

	Pin Label	Signal Name	I/O	Definition
Microprocessor Interface	AD[4]/IDLE	Address-Data 4/Idle Code Detection	B/O	Part of the bidirectional 8-bit multiplexed address-data bus when MON/MIC* is tied low. When in stand-alone mode, this pin is an active-high monitor output indicating an idle code detection.(1)
	AD[5]/PAR	Address-Data 5/Parity Error Detection	B/O	Part of the bidirectional 8-bit multiplexed address-data bus when MON/MIC* is tied low. When in stand-alone mode, this pin is an active-high monitor output indicating a parity error.(1)
	AD[6]/LCV	Address-Data 6/Line Code Violation	B/O	Part of the bidirectional 8-bit multiplexed address-data bus when MON/MIC* is tied low. When in stand-alone mode, this pin is an active-high monitor output indicating a line code violation.(1)
	AD[7]/FRMERR	Address-Data 7/ Frame Bit Error	B/O	Part of the bidirectional 8-bit multiplexed address-data bus when MON/MIC* is tied low. When in stand-alone mode, this pin is an active-high monitor output indicating a frame bit error.(1)
	CNTINT/LINELB	Counter Interrupt/ Line Loopback	O/I	The composite interrupt signal generated by the error counters when MON/MIC* is tied low. When MON/MIC* is tied high, this pin controls line loopback transmission in stand-alone mode. CNTINT is an active-low output; LINELB is an active-high input.
	DLINT/SOURCELB	Data Link Interrupt/Source Loopback	O/I	The composite interrupt signal generated by the data links when MON/MIC* is tied low. When MON/MIC* is tied high, this pin controls source loopback transmission in stand-alone mode. DLINT is an active-low output; SOURCELB is an active-high input.
	TESTI	Test In	I	Used for test functions only. Should be tied to ground for normal operation.
	INIT*	Initialization	I	Active low initialization control. Not all internal storage elements are affected by this signal. See Clock Interface and Initialization in the Overview section of the Functional Description chapter.
	TESTO	Test Out	O	Used for test functions only. Should be left disconnected for normal operation.

Table 1-2. Hardware Signal Definitions *(3 of 5)*

	Pin Label	Signal Name	I/O	Definition
Transmitter Section	TCLKO	Transmit Clock Out	O	Used to clock out the TXPOS and TXNEG outputs. Data is clocked out on the rising edge of TCLKO.
	TXPOS, TXNEG	Transmit Bipolar Positive, Negative	O	The positive and negative pulses generated by the B3ZS/HDB3 encoder.
	TDAT[3:0]	Transmit Data Bits 3–0 (Bit 0 is the LSB)	I	In parallel mode(2), these bits form the lower nibble of the byte-oriented data that is input to the PPDL transmitter in response to the transmit byte clock, TXBCK.
	TDAT[4]/LCVERRI	Transmit Data Bit 4/Line Code Violation Error In	I	In parallel mode, the TDAT[4] is bit 4 of the byte-oriented data that is input to the PPDL transmitter. In serial mode, LCVERRI allows test equipment to insert LCVs into the transmit stream under microprocessor control, in both DS3 and E3 modes.
	TDAT[5]/TXENCI	Transmit Data Bit 5/Transmit Encoder In	I	In parallel mode, TDAT[5] is bit 5 of the byte-oriented data that is input to the PPDL transmitter. In serial mode, TXENCI is an alternate direct input to the B3ZS/HDB3 encoder.
	TDAT[6]/TXDATI	Transmit Data Bit 6/Transmit Serial Data	I	In parallel mode, TDAT[6] is bit 6 of the byte-oriented data that is input to the PPDL transmitter. In serial mode, TXDATI is applied to the transmitter.
	TDAT[7]/TXSYI	Transmit Data Bit 7/Transmit M-Sync In	I	In parallel mode, TDAT[7] is the MSB (Bit 7)of the byte-oriented data that is input to the PPDL transmitter. In serial mode, TXSYI is applied to the transmitter.
Transmitter Section	TXSYO	Transmit M-Sync Out	O	The transmit M-frame sync output.
	TXCKI	Transmit Clock In	I	TXCKI rising edge is used to sample parallel data, while the falling edge is used to sample serial data.
	TXBCK/TXGAPCK	Transmit Byte Clock/Gapped Clock	O	In parallel mode, TXBCK clocks the byte-oriented data that is input to the PPDL transmitter. In serial mode, TXGAPCK is a transmit clock that is gapped during overhead bit intervals in either E3 or DS3 modes.
	SNDMSG	Send Message	I	In parallel mode, SNDMSG initiates message transmission in the PPDL transmitter.
	SNDFCS	Send Frame Check Sequence	I	In parallel mode, SNDFCS initiates transmission of the 16- or 32-bit frame check sequence on the PPDC transmitter.
	CBITI	Transmit C/N-Bit Serial In	I	The serial C-bit (DS3 mode) or N-bit (E3 mode) data input to be transmitted.
	TXCCK	Transmit C/N-Bit Clock	O	Used to sample the CBITI input on the falling edge of TXCCK.
	PPDLONLY	Payload Parallel Data Only Select	I	Enables the PPDL-only mode in which no DS3/E3 framing is inserted. This mode is entered by tying this pin high.

Table 1-2. Hardware Signal Definitions *(4 of 5)*

	Pin Label	Signal Name	I/O	Definition
Receiver Section	DS3CKI	DS3 Receive Line Clock In	I	Clock input DS3CKI should be connected to a 44.736 MHz source (34.368 MHz for the E3) derived from incoming receive data.
	RXPOS, RXNEG	Receive Bipolar Positive/Negative	I	The input positive and negative pulses are sampled on the rising edge of the receiver input clock (DS3CKI) and should be a full clock period wide.
	RXCKI	Receive Dejittered Clock In	I	Used to read the received data out of the internal FIFO (required only if FIFO is enabled). If unused, tie to ground.
	FIFEN	FIFO Enable	I	An active-high input which enables the internal FIFO, used to dejitter the received data by using the dejittered clock input, RXCKI. When FIFEN is low, the FIFO is bypassed and the serial data is output with respect to the incoming clock, DS3CKI.
	RXDAT	Receive Serial Data	O	RXDAT is the serial data bit stream clocked out on the rising edge of RXCLK.
	RXMSY	Receive M-Sync	O	The M-frame synchronization output recovered from the incoming serial data stream.
	RXCLK	Receive Clock	O	The receive clock used internally to clock out the serial data stream onto RXDAT.
	RXBCK/RXGAPCK	Receive Byte/Gapped Clock	O	When in serial mode, RXGAPCK provides a gapped clock signal during every overhead bit (in both DS3 and E3 modes). In parallel mode, RXBCK is used to internally clock out the receive byte-oriented data on RDAT[7:0].
	CBITO	Receive C/N-Bit Serial Out	O	The receive serial C-bit (DS3 mode) or N-bit (E3 mode) data. CBITO changes on the rising edge of RXCCK.
	RXCCK/TXNRZ	Receive C/N-Bit Clock Out/Transmit NRZ	O	A clock that indicates transitions in the CBIT0 signal. In PPDL-only mode, transmit NRZ data is available on this pin.
	RDAT[0]/LOS	Receive Data Byte 0/Loss of Signal	O	Part of the 8-bit data bus output from the PPDL receiver when parallel mode is enabled. When parallel mode is disabled, this pin is an active-high monitor output indicating loss of signal.
	RDAT[1]/OOF	Receive Data Byte 1/ Out of Frame	O	Part of the 8-bit data bus output from the PPDL receiver when parallel mode is enabled. When parallel mode is disabled, this pin is an active-high monitor output indicating out-of-frame.
	RDAT[2]/AIS	Receive Data Byte 2/Alarm Indication Signal	O	Part of the 8-bit data bus output from the PPDL receiver when parallel mode is enabled. When parallel mode is disabled, this pin is an active-high monitor output indicating alarm indication signal.

Table 1-2. Hardware Signal Definitions *(5 of 5)*

	Pin Label	Signal Name	I/O	Definition
Receiver Section	RDAT[3]/IDLE	Receive Data Byte 3/Idle Code Detection	O	Part of the 8-bit data bus output from the PPDL receiver when parallel mode is enabled. When parallel mode is disabled, this pin is an active-high monitor output indicating idle code detection.
	RDAT[4]/ FRMERR	Receive Data Byte 4/Frame Error Detection	O	Part of the 8-bit data bus output from the PPDL receiver when parallel mode is enabled. When parallel mode is disabled, this pin is an active-high monitor output indicating frame error detection.
	RDAT[5]/ LCVCAR	Receive Data Byte 5/Line Code Violation Carry	O	Part of the 8-bit data bus output from the PPDL receiver when parallel mode is enabled. When parallel mode is disabled, this pin is an active-high ripple carry output from the LCV error counter.
	RDAT[6]/RXOVH	Receive Data Byte 6/Receive Overhead Detection	O	Part of the 8-bit data bus output from the PPDL receiver when parallel mode is enabled. When parallel mode is disabled, this pin is an active-low monitor output indicating the receive overhead bit positions.
	RDAT[7]/TXNRZ	Receive Data Byte 7/ Transmit NRZ Out	O	Part of the 8-bit data bus output from the PPDL receiver when parallel mode is enabled. When parallel mode is disabled, this pin is a monitor output for the transmit NRZ data.
	IDLE/ FRMCAR	Idle/Frame Carry	O	Set if an idle flag is received after a non-idle sequence, when parallel mode is enabled. When parallel mode is disabled, this pin is an active-high ripple carry output from the frame error counter.
	VALFCS/TXOVH	Valid FCS Received/Transmit Overhead	O	Active high if a valid FCS was received, when parallel mode is enabled. When parallel mode is disabled, this pin is an active-low transmit overhead bit position indicator.
	VCO	Voltage-Controlled Oscillator Output	O	Used as the phase control for the clock recovery circuit that generates the dejittered clock, RXCKI. Valid only when FIFEN is high. FIFEN enables the internal FIFO when tied high.
VCC and GND	V_{DD}	Supply Voltage		Four pins are provided for power.
	GND	Ground		Five pins are provided for ground.
Not Connected	NC	Not Connected		These pins are not connected internally.

NOTE(S):

(1) Standalone operation is valid only in DS3 mode.

(2) Parallel mode is enabled by setting the Parallel Data Enable bit [ParaEn;CR04.3] in the Feature Control Register [CR04; 0x04] when MON/MIC* is low. When MON/MIC* is high, Parallel mode is entered by tying the ALE/PAREN pin high.

2.0 Functional Description

2.1 Overview

2.1.1 Brief Block Description

A block diagram of the circuit is illustrated in Figure 2-1. The receive B3ZS/HDB3 signal is decoded and the bipolar input is converted to a unipolar, clocked serial data stream. Frame bit content is checked and the overhead bit data links and alarms are extracted. The receive clock is provided at the receiver output (RXCLK). The data is also connected to a Payload Parallel Data Link (PPDL) receiver that decodes message blocks using the High-Level Data Link Control (HDLC) format (Refer to Appendix A in this document for a description of the HDLC formatter). The recovered data bytes are provided on a parallel output port with a byte clock. The PPDL receiver can also be programmed to operate in nibble mode or transparently without HDLC formatting.

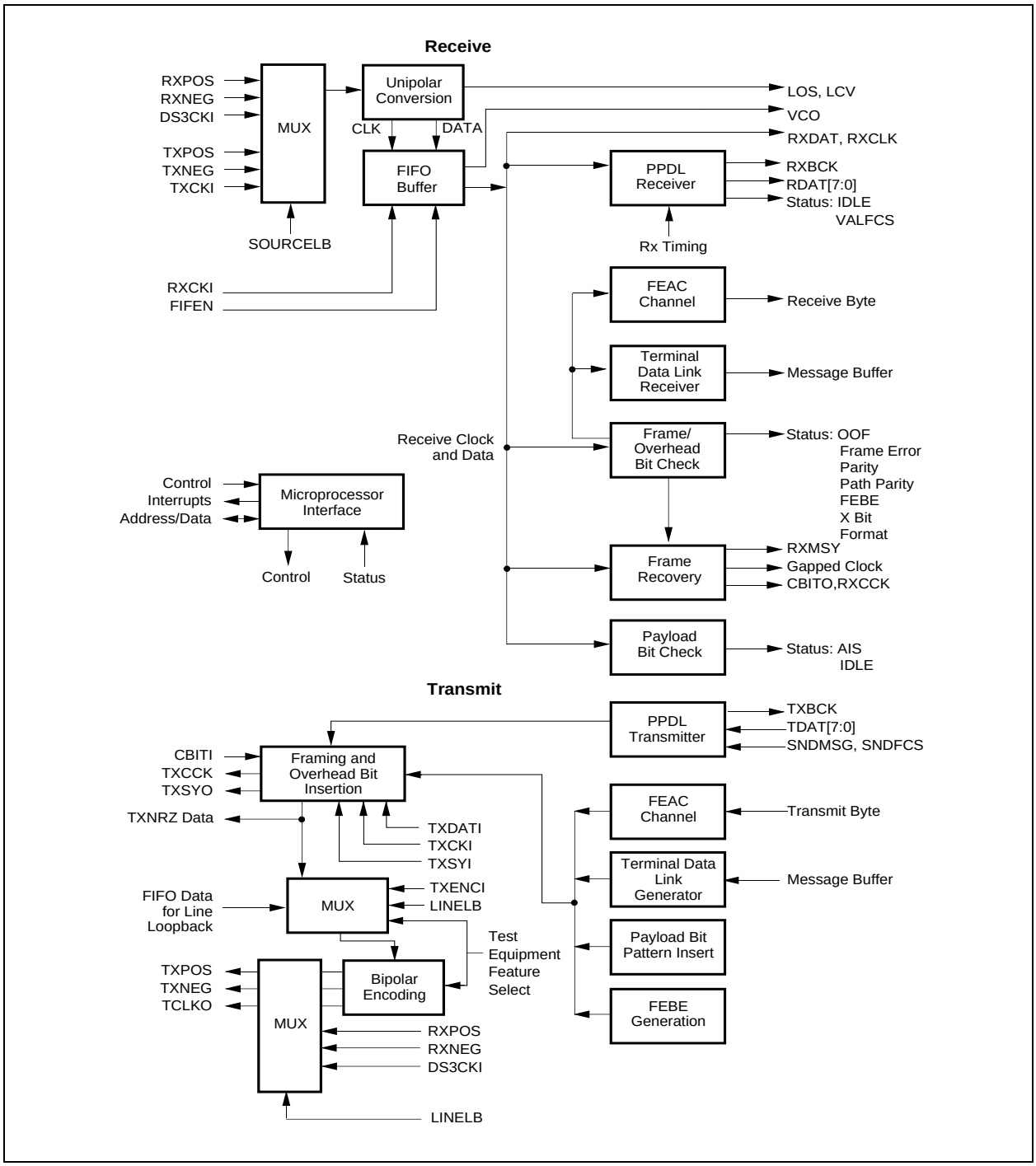
A First In First Out (FIFO) memory buffer in the receive signal path can be enabled to reduce the jitter on the incoming data. The receive data is clocked into the FIFO buffer after bipolar decoding. The FIFO buffer provides a Voltage Controlled Oscillator (VCO) control signal to an external clock recovery circuit. A dejittered clock (RXCKI) from the VCO is then used to read the data from the FIFO buffer to the remaining receiver circuitry.

The transmitter is capable of sending either serial data from an external pin, or byte- or nibble-oriented data from the PPDL data port. DS3 overhead bits or E3 Frame Alignment Signal (FAS) bits are automatically inserted. Parallel data can be formatted with idle flags, zero stuffing for transparency, and a selectable 16- or 32-bit Frame Check Sequence (FCS). Bytes or nibbles without HDLC formatting can also be transmitted. The transmitter is able to send AIS, idle code, yellow alarm, and all-ones signals. DS3 C-bits (or E3 N-bits) can be optionally inserted into the data stream from an external source.

LAPD (Link Access Procedure-D) receiver and transmitter circuitry is provided for the terminal data link in DS3 C-bit parity format and the E3 mode. In C-bit mode, the three C-bits in subframe 5 of the M-frame are used for the terminal data link. In E3 mode, the N-bit is used for the terminal data link.

The microprocessor interface or external outputs monitors all status indications in the received signal. For both DS3 and E3 modes, indications include AIS, all-ones, and yellow alarm detection; and Out-of-Frame (OOF) and frame bit error counting. In addition, loss of signal, idle code, and parity error detection; line code violation (LCV), path parity, and FEBE event counting; and parity and X-bit disagreement counting are provided for DS3 mode. The received DS3 C-bits (or E3 N-bits) are available on an external pin to provide visibility for external processing, if necessary.

Figure 2-1. Functional Block Diagram



2.1.2 Clock Interface and Initialization

The CN8330 clock input (TXCKI) controls the transmitter. This input should be supplied with a 44.736 MHz clock in DS3 mode and a 34.368 MHz clock in E3 mode. TDAT[6]/TXDATI is sampled on the falling edge of TXCKI and TDAT[7]/TXSYI is sampled on the rising edge of TXCKI. The transmit pulses TXPOS and TXNEG are clocked out on the rising edge of TCLKO.

DS3CKI is the raw data clock that accompanies the RXPOS and RXNEG data pulse inputs for the receiver. If the FIFO buffer is enabled, the data is clocked into the FIFO buffer after B3ZS/HDB3 decoding. RXCKI is the dejittered version of DS3CKI and is used to clock the receive data out of the FIFO buffer (if enabled) to the rest of the receiver circuitry. If the FIFO buffer is disabled, DS3CKI clocks the data into all of the receiver circuitry and the RXCKI input should be grounded.

Clock timing requirements are given in the Electrical and Mechanical Specifications chapter.

2.1.2.1 Initialization

The CN8330 can be initialized with an active-low input pulse of at least 200 ns duration on the INIT* pin. All error counters are initialized to zero when this input is active low if the transmit and receive clocks are present. Initialization is not required for proper operation. During initialization (active low) host cannot read or write any CN8330.

2.1.3 Microprocessor Interface

The CN8330 can be controlled by a microprocessor or a microcontroller through an 8-bit multiplexed address/data interface. An interface to an Intel 8051 family processor or equivalent, or Motorola 68HC11 family or equivalent is provided. The microprocessor interface is enabled by tying the MON/MIC* pin low. The CN8330 is connected to the microprocessor exactly like static RAM.

2.1.3.1 Using with Specific Microcontrollers

The microprocessor interface is designed to allow direct connection of Intel 8051 family, Motorola 68HC11 family, or equivalent microcontrollers. The controller interface to the CN8330 consists of 14 pins: Address Latch Enable (ALE), Read Enable (RD*), Write Enable (WR*), Chip Select (CS), eight multiplexed address/data bits (AD[7:0]), and two interrupts (DLINT/SOURCELB and CNTINT/LINELB). If a 68HC11 controller is used, then its address strobe as is connected to ALE, Enable is connected to RD*, and Read/Write* (R/W*) is connected to WR*. The chip select input (CS/ALM0) allows the control of multiple ICs from a single microprocessor. Interrupt outputs are used for data link and maintenance operations and provide active-low interrupts.

2.1.3.2 Microprocessor Interrupts

There are two separate interrupt pins that can be connected to the microprocessor (or microcontroller): Counter and Data Link. The counter interrupt pin (CNTINT/LINELB) combines seven sources of interrupts on an external pin connected to the microprocessor. This interrupt signal is active low and is a composite indication of all interrupt sources that are enabled in the Status Interrupt Control Register [CR02;0x02]. The interrupt source can be determined by reading the Counter Interrupt Status Register [SR01;0x11]. The data link interrupt pin (DLINT/SOURCELB) is a composite indication of the interrupts from four sources. The interrupt source can be determined by reading the Data Link Interrupt Status Register [SR02;0x12]. When the C-Bit Parity Mode/Enable DLINT bit [CBitP/DL;CR00.0] is not set, the DLINT/SOURCELB pin is held high (inactive). The two interrupt pins are open-drain outputs and can be connected to form a single-wire ORed interrupt, if desired.

2.1.3.3 Address Map

The register address map for the CN8330 is given in Table 3-1 through Table 3-4, Register Summary. There are three types of registers: Control Registers, which can be read or written; Status Registers and Counters which can only be read; and Data Link Message Buffers which can be read or written. The Control Registers serve as latches that are modified by a microprocessor write operation and can also be read to verify contents. They are located at addresses 0x00–0x05. Status Registers are located at addresses 0x10–0x16. Maintenance Error Counters are located at addresses 0x20–0x26. The Transmit Terminal Data Link Message Buffers are located at addresses 0x30–0x37, and the Receive Terminal Data Link Message Buffers are located at addresses 0x40–0x47. The chip select input (CS/ALM0) must be high to address the CN8330 and to enable read or write operations.

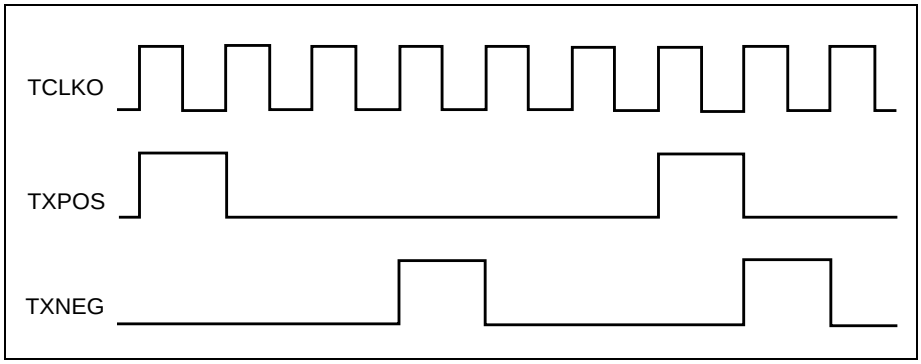
2.2 Line Interfaces

2.2.1 Transmitter Line Interface

The transmitted line signals are shown in Figure 2-2. Nine bits of a representative output sequence are shown. Separate signal pins provide the appropriate output signal for positive and negative pulses. The outputs are a full clock period wide and change on positive clock transitions of the TCLKO pin. For additional information on the TXPOS and TXNEG outputs refer to Transmitter Outputs in the Transmitter Operation section in this chapter

B3ZS/HDB3 encoding is performed automatically on the output data stream; however, this encoding can be disabled to send AMI data without any zero code suppression. Transmit NRZ data, prior to B3ZS/HDB3 encoding, is also available on the RDAT[7]/TXNRZ pin when parallel mode is not selected and on the RXCCK/TXNRZ pin when PPDLONLY mode is selected.

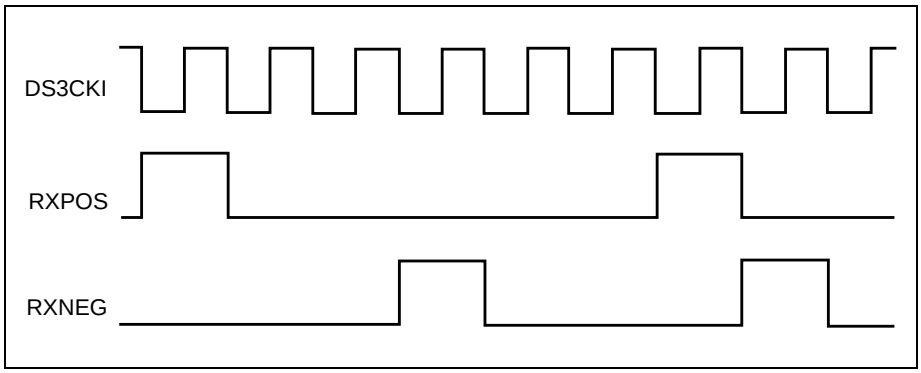
Figure 2-2. Transmitter Line Driver Outputs



2.2.2 Receiver Line Interface

The line interface for the receive bipolar signals consists of two logic-level signals that represent the positive and negative bipolar line pulses (RXPOS, RXNEG) and an input (DS3CKI) for an externally derived clock at a nominal frequency of 44.736 MHz or 34.368 MHz. The receiver line signals are shown in Figure 2-3. Nine bits of a representative input sequence are shown. The input signal is sampled on the rising edge of the clock signal. B3ZS/HDB3 decoding is provided internally. Decoding can be defeated for NRZ inputs by connecting the NRZ data input to both the RXPOS and RXNEG inputs or by selecting the AMI mode/LCV Type 2 bit [AMI/LCV2;CR04.6] in the Feature Control Register [CR04;0x04].

Figure 2-3. Clocked Receiver Input



2.3 Transmitter Operation

The transmitter circuit is synchronized to the transmit input data by an external synchronization signal. The external synchronization signal sets the M-frame reference for transmitted signals.

2.3.1 Input and Synchronization

The input to the transmitter consists of the transmit serial data input (or the PPDL transmitter data), transmit clock, and transmit M-frame sync signal. An M-frame sync signal output is available on the TXSYO pin to synchronize external circuitry, if desired. If an input sync is not provided, the CN8330 generates a sync internally whose position is indicated by TXSYO. In this case, the sync input should be grounded. The TDAT[7]/TXSYI is sampled on the rising edge of TXCKI and TDAT[6]/TXDATI is sampled by the falling edge of TXCKI.

2.3.2 DS3 Mode

The input bits are synchronized to the M-frame sync signal, which can either be externally provided or taken from the M-frame sync signal that is internally generated. Serial input data on TDAT[6]/TXDATI must contain bit positions for the overhead bits, although these are not used unless external insertion is enabled. The clock frequency is nominally 44.736 MHz and the transmit data input is sampled on the falling edge of the clock signal. The path delay of the transmitter from the serial data input to the positive and negative outputs is six cycles of the transmit clock. This delay includes B3ZS/HDB3 coding. The delay from the serial data input to the NRZ output is two clock cycles and the coding delay of the B3ZS encoder is four clock cycles.

If the TDAT[7]/TXSYI M-frame sync signal is provided, it is sampled on the rising edge of TXCKI and should have a low-to-high transition from the last bit of the M-frame (bit 680 of subframe 7) to the X1 bit (bit 1 of subframe 1). TXSYO is clocked out by the rising edge of TXCKI and may be used for synchronization of external circuitry. Serial data may alternatively be provided in response to the TXBCK/TXGAPCK pin without the need for providing frame synchronization or overhead bit slots. The gapped clock output is a gated version of TXCKI with one pulse gapped for each overhead bit position (one pulse every 85 clock cycles). A transmit overhead VALFCS/TXOVH bit position indicator pulse is available when the PPDL is not selected. This pulse is clocked out on the falling edge of TXCKI and may be of use for providing overhead bits externally. A timing diagram is presented in Figure 2-4 with propagation delays shown as negligible. Refer to the Electrical and Mechanical Specifications chapter for actual propagation delay specifications.

Figure 2-4. Transmitter Timing for Serial DS3 Mode

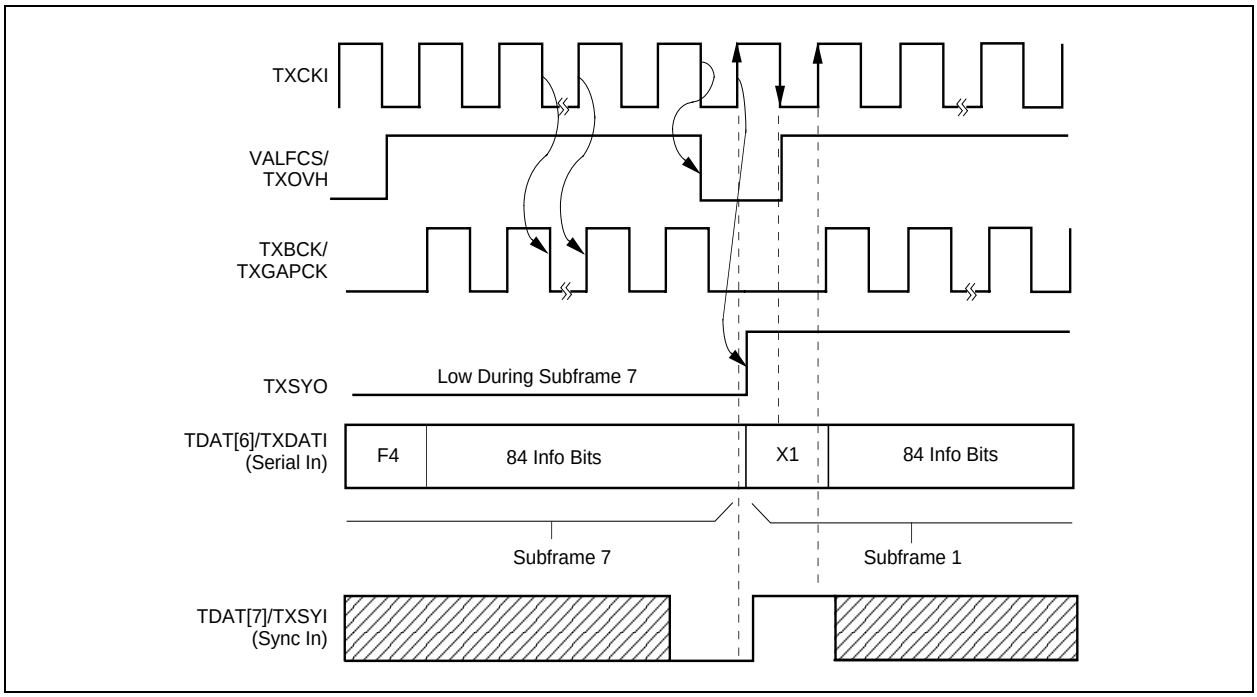
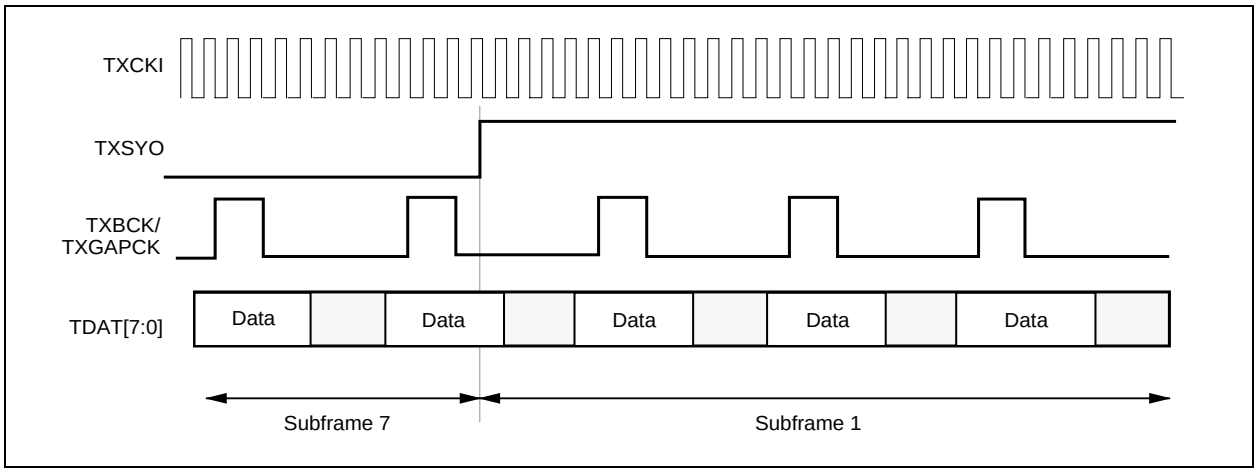


Figure 2-5 illustrates the transmitter timing for the parallel DS3 mode. This mode is enabled by setting the Parallel Data Enable bit [ParaEn;CR04.3] in the Feature Control Register and setting the Disable PPDL Transparency bit [DisPPDL;CR05.1] in the PPDL Control Register [CR05;0x05]. The SNDMSG pin should be tied high and the SNDFCS tied low to ensure that flags or FCS bytes are not transmitted.

Figure 2-5. Transmitter Timing for Parallel DS3 Mode

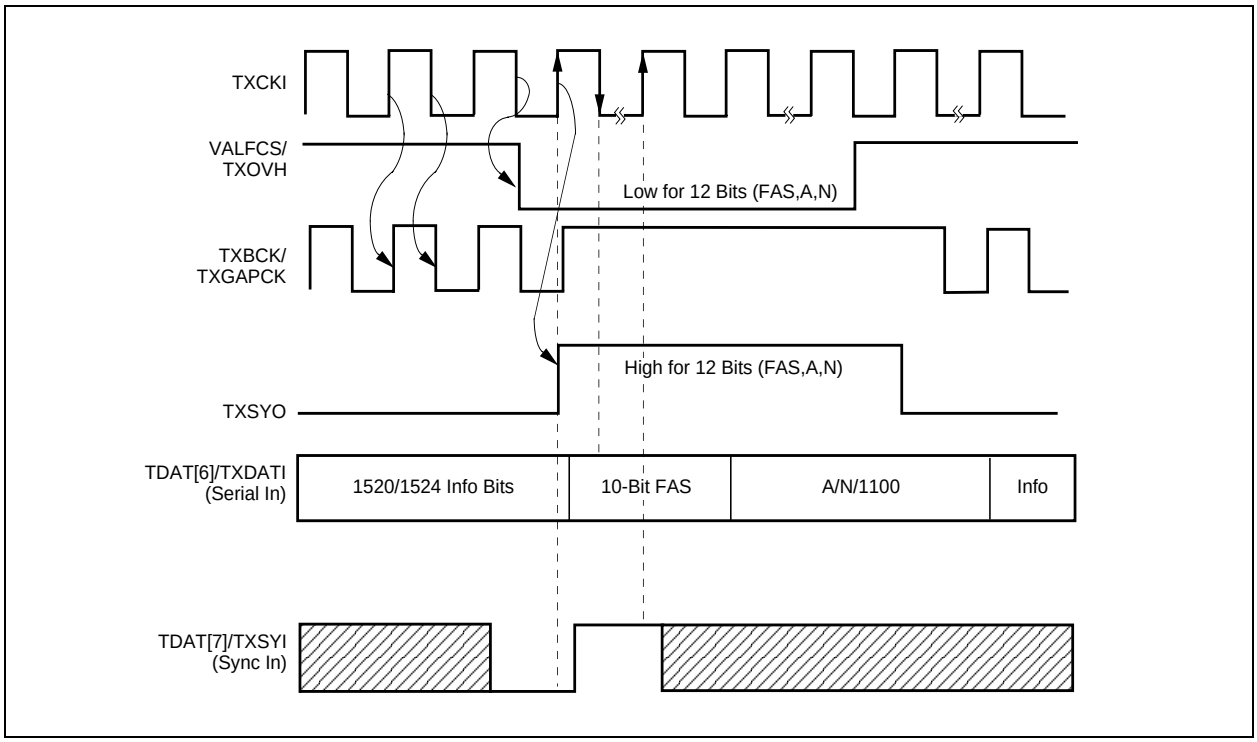


2.3.3 E3 Mode

The clock and data edges for E3 mode have the same relationship as in DS3 mode. The synchronization overhead for E3 mode is 12 contiguous bits in each frame rather than being distributed throughout the frame. The input bits are synchronized to the M-frame sync signal, which can be externally provided or internally generated from the M-frame sync signal. Serial input data must contain bit positions for the overhead bits, although these are not used unless external insertion is enabled. The clock frequency is nominally 34.368 MHz and the transmit data input is sampled on the falling edge of the clock signal. The path delay of the transmitter from the serial data input to the positive and negative line driver outputs is seven cycles of the transmit clock. This delay includes HDB3 encoding. The delay from the serial data input to the NRZ output is two clock cycles and the coding delay of the HDB3 encoder is five clock cycles.

The TDAT[7]/TXSYI signal should have a low-to-high transition from the last bit of the M-frame (bit 1536) to the first bit of the FAS (bit 1). TXSYO may be used to synchronize external circuitry. Serial data may be provided alternatively in response to the TXBCK/TXGAPCK output without providing frame synchronization or overhead bit slots. Figure 2-6 illustrates the timing with propagation delays shown as negligible. Refer to the Electrical and Mechanical Specifications chapter for actual propagation delay specifications. Note that in E3 mode gapped clock TXBCK/TXGAPCK is one clock cycle late relative to the overhead bit positions when compared to the same relationship in DS3 mode. This clock can still be used for data input to the transmitter. The last data bit clocked in external circuitry by the gapped clock output should be held during the overhead interval and will be sampled by the first falling edge of TXCKI after the overhead interval. This bit will appear as the first bit in the information field after the overhead field.

Figure 2-6. Transmitter Timing for Serial E3 Mode

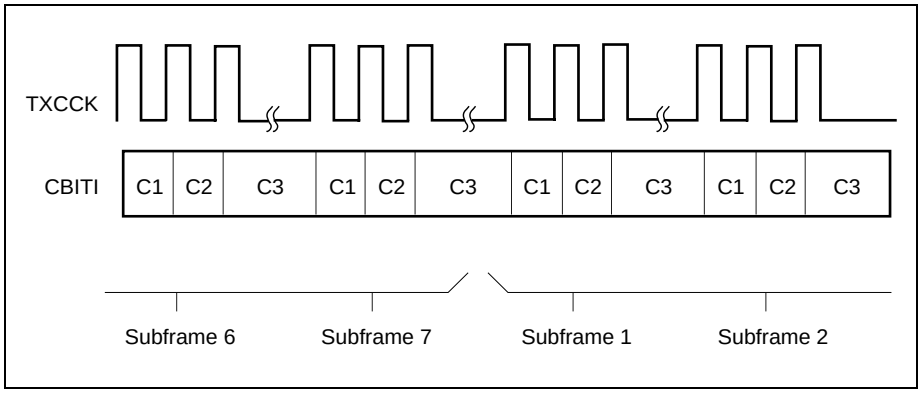


2.3.4 Framing Bit Generation

In DS3 mode, all F and M framing bits are automatically generated by the transmitter circuitry. Additionally, the transmitter calculates the parity of each M-frame and inserts this data into bits P1 and P2 of the following M-frame. Bits X1 and X2 contain ones unless the Transmit Alarm Control 0 bit [TxAlm0; CR00.4] in the Mode Control Register [CR00;0x00] is set. If set, bits X1 and X2 contain zeros. If C-bit parity mode is selected, all C-bit positions are generated automatically by the transmitter if the External C-Bit Insert bit [ExtCBit;CR00.2] is low. If high, all C-bits are generated internally except for the CP (subframe 3) an FEBE (subframe 4) bit positions. These bits must be provided on the CBITI pin at the proper time in response to TXCCK as shown in Figure 2-7. The CBITI data must be valid on the falling edge of TXCCK. This allows the chip to be used in a repeater mode with pass-through of the path parity and FEBE information. If C-bit parity mode is not selected, all C-bit positions come from either the serial data stream or the CBITI pin depending on the ExtCBit setting in the Mode Control Register. The X, P, M, and F bit positions may be inserted from the transmit serial data stream by setting External Overhead Insert bit [ExtOvh;CR00.3] high.

In E3 mode, the FAS pattern is automatically generated by the transmitter circuitry. The transmitter also inserts the A-bit as determined from the Transmit Alarm Control 1 bit [TxAlm1;CR00.5] and the N-bit from the terminal data link circuitry. If ExtCBit is high, the N-bit must be provided on the CBITI pin in response to the rising edge of TXCCK. The TXOVH/VALFCS and TXSYO signals are active during the 12 bits of overhead. If the PPDL is enabled, the transmitter also inserts a 1100 pattern after the normal 12-bit framing sequence for a total of 16 overhead bits. This 16-bit pattern is for conformance with draft standard prETS 300 214 for SMDS applications. In this mode, the VALFCS/TXOVH and TXSYO signals are active during all 16 bits of overhead. All overhead bits can be inserted via the serial data input by setting the ExtOvh bit high.

Figure 2-7. C-Bit Input Timing



2.3.5 Alarm Signal Generation

Three alarm signals, yellow, AIS, and idle, can be generated by the transmitter in DS3 mode by setting the TxAlm[1,0] bit pair in the Mode Control Register.

The yellow alarm is contained in the X1 and X2 bits. The X1 and X2 bits are normally set to 1. The yellow alarm (X1 and X2 bits = 0) can be sent by setting the TxAlm bit pair to 01.

The AIS signal is enabled by setting the bit pair to 11. The AIS signal has valid framing and parity, all C-bits set to zero regardless of framing mode, both X-bits set to one, and the payload set to a 1010... pattern starting with 10 after each overhead bit.

The idle code signal is enabled by setting the bit pair to 10. The idle code signal has valid framing and parity, both X-bits set to one, and the payload set to a 1100... pattern starting with 11 after each overhead bit. If the framing mode is M13, all C-bits are set to zero during transmission of the idle signal. If the framing mode is C-bit parity, the C-bits in subframe 3 are set to zero, and the other C-bits are from the selected source. This allows full use of the terminal data link and transmit FEAC channel during transmission of idle code.

In C-bit parity mode with internal sourcing of the C-bits, FEBE alarms are generated automatically in the transmitter when the receiver detects either a frame bit error or a C-bit parity error in an M-frame. The 3-bit FEBE pattern that is transmitted is contained in the FEBE Pattern Bit Field [FEBEC[3:1];CR04.2:0] of the Feature Control Register. Bit 2 is placed in the C1 position of subframe 4 during the alarm condition, bit 1 is placed in the C2 position, and bit 0 is placed in the C3 position. When no alarm condition is present, the FEBE channel contains all ones. Therefore, to prevent disabling proper FEBE operation, the FEBE field should be written to any combination other than 111.

An unframed, all-ones signal can be transmitted by setting both TxAlm0 and TxAlm1 to a 1 and ExtOvh cleared to a 0.

In E3 mode, the AIS (unframed all-ones) is enabled by setting TxAlm0 high. The yellow alarm is enabled by setting TxAlm1 high. This causes the transmitted A-bit to be set to a one.

2.3.6 Terminal Data Link Transmitter

The terminal data link transmitter consists of the three C-bits in subframe 5 of the M-frame in DS3 mode or the N-bit in E3 mode and uses the LAPD protocol. When the Send Message bit [TxMsg;CR01.0] of the Terminal Data Link Control Register [CR01;0x01] is low, the data link transmitter is continuously sending idle flags (01111110). When high, message transmission is initiated. Transmission of the FCS bytes is controlled by the Send Frame Check Sequence bit [TxFCS;CR01.1]. If a nonstandard FCS is required, it may be loaded into the message buffer and transmitted as part of the message. A message in progress may be abandoned by setting the Abort Message bit [TxAbort;CR01.2]. This will cause an abort flag (11111110) to be transmitted, followed by idle flags, until the Send Message bit is reactivated. Two consecutive messages may share ending and beginning idle flags. The transmitter can be disabled by setting the Disable Terminal Data Link Transmission bit [DisTxTDL;CR01.6] to a one. This causes all ones to be sent in the data link bit positions.

The terminal data link transmitter is under control of the C-Bit Parity Mode/Enable DLINT/SOURCELB (CBitP/DL;CR00.0), E3 Framing Mode [E3Frm;CR00.1], External C-Bit Insert, and Transmit Alarm Control bits in the Mode Control Register. In the Terminal Data Link Control Register, the transmitter is under the control of the TxMsg, TxFCS, TxAbort, Send Byte [TxByte[2:0];CR01.5:3], and DisTxTDL bits. An interrupt for use with data link operations is available on the DLINT/SOURCELB output pin and status bits for determining the interrupt source are located in the Data Link Interrupt Status Register [SR02;0x12].

The framer mode must be set to either C-bit parity mode or E3 mode for terminal data link transmission to take place. In C-bit parity mode, the three C-bits in subframe 5 of the M-frame will be used for transmission. In E3 mode, the N-bit will be used for transmission. When E3 mode is selected, the CBitP/DL bit must also be set to enable interrupts on the DLINT/SOURCELB pin. If neither mode is set, terminal data link transmission will not take place. If the ExtCBit bit is set in E3 mode, terminal data link transmission will be disabled. In C-bit parity mode, ExtCBit has no effect on terminal data link transmission. Setting the Transmit Alarm Control [1,0] bits for transmission of AIS or all ones in either C-bit parity mode or E3 mode will disable transmission of the terminal data link. Transmission of yellow alarms or idle codes has no effect on terminal data link transmission.

If the framer is in a mode that allows data link transmission as described previously, then the Terminal Data Link Control Register is the main control register used for transmit data link operations. The DisTxTDL bit must be set low to enable operation of the data link. If high, an all-ones signal will be transmitted in the data link bit positions in the outgoing serial stream. With the data link enabled, the TxMsg, TxFCS, and TxAbort bits control operation. The TxByte[2:0] bits form a pointer to the Transmit Terminal Data Link Message Buffer [TxTdl;0x30–0x37] used by the data link transmitter.

The transmitter implements an LAPD data link per CCITT standard Q.921. The functions provided by the data link transmitter circuitry are transparency zero stuffing, FCS generation, idle flag generation, and abort flag generation. The total length of the message has no restrictions. Q.921 requires all messages be integral numbers of 8-bit bytes. The transmitter can only transmit 8-bit bytes. Byte transmission time for the transmitter is approximately 284 microseconds in C-bit parity mode and approximately 357 microseconds in E3 mode.

The Transmit Terminal Data Link Message Buffer is an 8-byte buffer provided for the transmit data link channel to minimize processor interruptions. Filling of this buffer is accomplished by the processor in the same manner as writes to control registers. This buffer can be read as well as written to verify contents. The buffer is divided into two halves to reduce the real-time requirements on the processor. The processor loads four bytes at a time, while the data link transmitter reads from the other half of the buffer. This gives the processor at least 1 msec to assemble the next four bytes of message for transmission before the next interrupt is issued. Interrupts are issued each time the transmitter circuitry reaches a 4-byte buffer boundary.

The transmitter must initialized with bits 0 through 6 of the Terminal Data Link Control Register written to zero. This will enable the transmitter to send idle flags on the data link. No interrupts are generated when the data link is sending idle flags, thus no processor intervention is required until a message is to be sent.

2.3.6.1 Sending a Message

Beginning with an idle channel, the processor writes the first four bytes of message data to the Transmit Terminal Data Link Message Buffer. The first byte of data to be transmitted should be written to address 0x30. The message is read from the buffer in ascending order starting at address 0x30 and ending at address 0x37. The Least Significant Bit (LSB) in each byte is the first transmitted. This buffer may be written well before the message is to be sent, if desired. After the first block of data is present in the buffer memory, the processor writes to the Terminal Data Link Control Register to begin transmission (TxMsg = 1, TxByte[2:0] = 011, TxFCS = 0, TxAbort = 0). The 3-bit TxByte[2:0] field is functionally split into two parts. The Most Significant Bit (MSB) indicates to the transmitter circuitry which half of the buffer to read from next. The two LSBs indicate the stop location, i.e., where the last message byte is located. When the new controls are latched by the transmitter circuitry, the processor will be interrupted for the next set of controls. Now, the processor has up to 1 msec to write a new set of controls to the control register. The processor may now also write the next block of data to the next half of the message buffer.

When the end of a message is reached, or in the event of a short message, there may not be exactly 4 bytes remaining. In this case, the processor writes the remaining data to the message buffer as usual. The processor now must write the highest location used to the TxByte[2:0] field. Also, the TxFCS bit is set to 1. This causes the FCS to be sent after this last block of data.

When this set of controls is latched, the processor will be interrupted. At this time, a new message may be sent, or the TxMsg bit may be set to zero to send idle flags. If a new message is to be sent immediately, the next half of the transmit buffer can be written, and the Terminal Data Link Control Register optioned accordingly. This will result in only one idle flag being transmitted between messages. If there is no new message ready, the processor must write TxMsg to zero. If this is not done within 1 msec, undefined data will be transmitted.

2.3.6.2 Aborting a Message

To abort a message in progress, the controller writes the TxAbort bit to one in the Terminal Data Link Control Register. The transmitter will finish sending the message byte in progress, then transmit an abort flag (11111110). After writing the abort signal to the control register, a second write may follow immediately to cause the transmitter to go to the idle condition, or to transmit another message. In the latter case, the abort flag will be followed by one idle flag, and then the new message will begin. If the second write is not performed, the formatter will continue to transmit abort flags until instructed otherwise.

2.3.6.3 Transmitter Interrupts

The transmitter generates an interrupt when it has latched the present set of controls and is ready for a new set. There will not be any interrupts during the transmission of idle flags. Therefore, to start a message from an idle condition, the first half of the buffer and the proper control bits are written by the processor. When the circuit latches these controls internally, an interrupt will immediately be issued for the next set of control bits. The processor then has up to 1 msec (4 byte periods) to respond to the interrupt. The Data Link Interrupt Status Register [SR02;0x12] indicates the source of the interrupt but not the cause. The controller software must know from message context what response is required. The interrupt is an active low level, not a pulse. The interrupt will be cleared upon the writing of the Terminal Data Link Control Register. A write operation must be performed to clear the current interrupt and prevent missing later interrupts.

If the interrupt is a mid-message interrupt, a new data link control word must be written, with bytes equal to the ending location of the next message block. The MSB of TxByte[2:0] will inform the transmit circuitry which half of the buffer to read next.

Interrupts from the Terminal Data Link Transmitter will appear in the Transmit Terminal Data Link Interrupt bit [TxTDLItr;SR02.3]. Interrupts must be enabled to appear on DLINT/SOURCELB by setting the CBitP/DL bit to a 1 in the Mode Control Register in either C-bit parity or E3 mode.

2.3.6.4 Transmitter Control Example

This example will show the sequence necessary to transmit a 10-byte hex message starting in the low half of the transmit buffer. With the transmitter in the idle state, the processor would execute the following sequence:

write byte 1 to address 0x30
write byte 2 to address 0x31
write byte 3 to address 0x32
write byte 4 to address 0x33
write 0x19 to address 0x01 (TxByte[2:0] = 011, TxMsg = 1)
at TX Interrupt:
write byte 5 to address 0x34
write byte 6 to address 0x35
write byte 7 to address 0x36
write byte 8 to address 0x37
write 0x39 to address 0x01 (TxByte[2:0] = 111, TxMsg = 1)
at TX Interrupt:
write byte 9 to address 0x30
write byte 10 to address 0x31
write 0x0B to address 0x01 (TxByte[2:0] = 001, TxMsg = 1, TxFCS = 1)
at TX Interrupt:
write 00 to address 0x01 (TxMsg = 0, TxFCS = 0)

2.3.7 TxFEAC Channel Transmission

The third C-bit in subframe 1 of the M-frame is the Transmit Far End Alarm and Control (TxFEAC) Channel. This channel uses a bit-oriented protocol and is under control of the Transmit FEAC Channel Byte Register [CR03;0x03].

The TxFEAC Channel Transmitter is under control of the CBitP/DL, E3Frm, and TxAlm[1,0] bits in the Mode Control Register and the Transmit FEAC Channel Message Byte [TxFEAC[7:0];CR03.7:0] in the Transmit FEAC Channel Byte Register. An interrupt for use with TxFEAC channel operations is available on the DLINT/SOURCELB output pin and status bits for determining the interrupt source are located in the Data Link Interrupt Status Register.

The framer mode must be set to C-bit parity mode for TxFEAC channel transmission to take place. In C-bit parity mode, the last C-bit in subframe 1 of the M-frame will be used for transmission. There is no TxFEAC channel transmission in either E3 mode or with the CBitP/DL bit set to zero. Setting ExtCBit in C-bit parity mode has no effect on TxFEAC channel transmission. Setting the TxAlm[1,0] bits for transmission of AIS or all ones in C-bit parity mode will disable transmission of the TxFEAC channel. Transmission of yellow alarm or idle code in C-bit parity mode has no effect on TxFEAC channel transmission.

The Transmit FEAC Channel Byte Register controls the byte to be transmitted on the TxFEAC channel. All messages for transmission on this channel must be in the form “0xxxmmm011111111". The rightmost bit of this sequence is the first bit transmitted on the channel. To initiate transmission of a message byte in the TxFEAC channel, the desired byte in the form 0mmmxxx0 is written into the Transmit FEAC Channel Byte Register. Transmission of the flag (11111111) is automatic. Each time the message is sent, an interrupt will be issued on the DLINT/SOURCELB pin and will appear in the Data Link Interrupt Status Register to request a new byte from the processor. The Transmit FEAC Channel Byte Register must be written to clear the interrupt. If multiple transmissions of the same byte are desired, the processor should rewrite the desired byte on each interrupt and count the interrupts until the desired number of transmissions have taken place. Interrupts from the TxFEAC channel will occur at a rate of approximately one interrupt per 1.7 msec.

Transmit FEAC clears the internal data shift buffer after sending CR03 contents unless the host has again written to CR03. When the host writes CR03, CN8330 transfers CR03 contents to an internal data shift buffer and then immediately raises an interrupt (SR02.1) which tells the host that another codeword (or the same one) can be written. After the interrupt the host must write to CR03 within 1.7ms to keep sending codewords, else after sending the shift buffer contents CN8330 will automatically return to sending idle (all ones) FEAC codewords.

In summary, Transmit FEAC clears the internal data shift buffer after sending the transmit FEAC channel byte from the CR03 register contents unless the host has again written to this register (CR03). When the host writes to Transmit FEAC Channel byte Register (CR03), CN8330 transfers the contents to an internal data shift buffer and then immediately raises an interrupt in the Data Link Interrupt Status Register (SR02.1) which tells the host that another code word (or the same one) can be written. After the interrupt, the host must write to Transmit FEAC Channel Byte Register (CR03) within 1.7 ms to keep sending code words, or else after sending the shift buffer contents CN8330 will automatically return to sending idle (all ones) FEAC codewords.

If a one is in either the MSB or LSB position of the TxFEAC field, then continuous transmission of idle flags is enabled and no interrupts will be issued until a byte of the proper format is written to the Transmit FEAC Channel Byte Register.

Interrupts from the TxFEAC channel transmitter will appear on Transmit FEAC Channel Interrupt bit. Interrupts must be enabled to appear on DLINT/SOURCELB by setting the CBitP/DL bit in the Mode Control Register.

2.3.8 PPDL Transmitter

The payload portion of the CN8330 data stream can come from an internal PPDL formatter that provides an external byte-wide data interface and a byte clock. This source is enabled by setting the ParaEn bit in the Feature Control Register. The PPDL formatter is controlled by signals applied on the SNDMSG and SNDFCS pins. Both byte-wide and nibble-wide inputs can be provided. Optional HDLC formatting with 16-bit or 32-bit FCSs is provided.

HDLC mode is selected by setting the ParaEn bit of the Feature Control Register high and the DisPPDL bit of the PPDL Control Register low. Operation is controlled by the SNDMSG and SNDFCS pins. If no message is in progress, idle flags (01111110) are continuously transmitted in the data payload. Setting SNDMSG high initiates message transmission. Data bytes and control signals are provided in response to the rising edge of the TXBCK/TXGAPCK pin and are sampled internally after the falling edge. The data and controls should be held for a full period. The LSB of the transmitted bytes is applied to TDAT[0] and the MSB to TDAT[7]; transmission is LSB first. The transmitter performs automatic zero stuffing for transparency and FCS calculation for the data. The message must be an integral number of bytes in length. The FCS is 16 or 32 bits in length depending on the setting of the 32-bit CRC Select bit [CRC32;CR05.2] in the PPDL Control Register. If this bit is low, a 16-bit FCS is calculated with the polynomial:

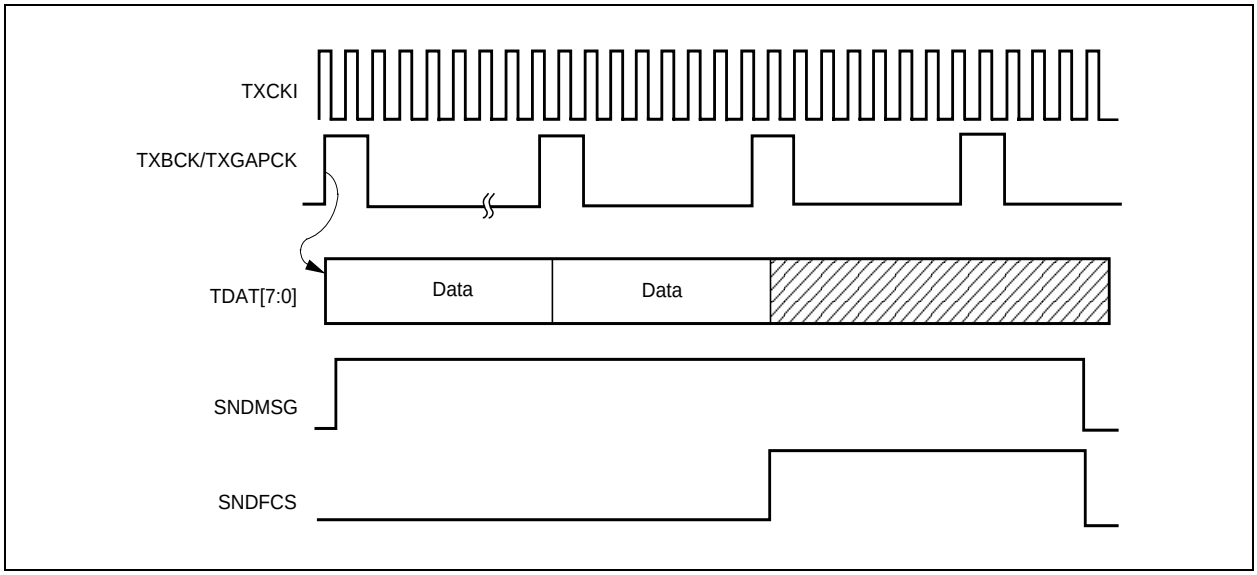
$$x^{16}+x^{12}+x^{5}+1$$

If the CRC32 bit is high, a 32-bit FCS is calculated. SNDFCS must be high for four cycles of the transmit byte clock and the FCS is calculated with the polynomial:

$$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$$

The FCS is transmitted by setting both the SNDMSG and SNDFCS pins high after the last data byte has been transmitted. An abort sequence may be transmitted by setting SNDFCS high while SNDMSG is set low. Timing for the transmit operation is shown in Figure 2-8.

Figure 2-8. PPDL Transmitter Timing

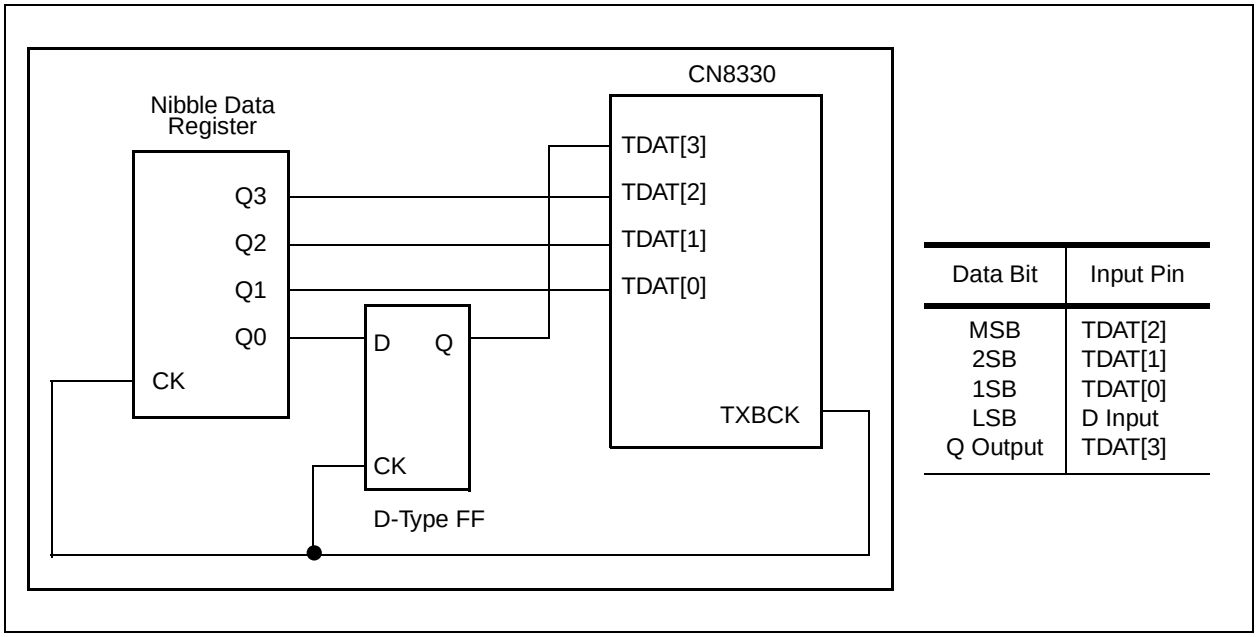


TXBCK/TXGAPCK is generated from TXCKI and has a duty cycle of 25 percent. TXBCK will nominally be one-eighth the TXCKI frequency but is influenced by HDLC transparency bit insertions and DS3/E3 overhead bits. In the absence of any transparency bit insertions or overhead bits, there will be one pulse on TXBCK for every eight clock cycles of the TXCKI input. When a transparency bit is inserted into the serial transmit data stream, the TXBCK period will be lengthened to nine clock cycles of TXCKI (or up to 11 cycles if two transparency bit insertions and a DS3 overhead bit land in the same data octet interval). TXBCK/TXGAPCK is present continuously even during the transmission of idle flags. The actual setup times on TDAT[7:0], SNDMSG, and SNDFCS relative to the rising edge of TXBCK are negative. Therefore, it is possible to read data and control from a RAM or FIFO buffer with the rising edge. The CN8330 will sample the data after the falling edge. This allows FIFOs or RAMs with access times of 35–40 nsec to be used.

The parallel interface can be used without transparency bit insertion by setting the DisPPDL bit in the PPDL Control Register to a 1. In this mode, SNDMSG is held high and SNDFCS is held low so that no flags or FCS bytes are transmitted. Byte synchronization in the transmitter and receiver is achieved from the M-frame sync alignment. This allows the byte-wide interface to be used as the data input for non-HDLC payloads rather than the serial input pin. Data is inserted on the TDAT[7:0] pins in response to TXBCK/TXGAPCK just as in the HDLC mode. Data bytes are transmitted LSB first. If E3 mode is enabled, the transmitted bytes are byte aligned after the 16 overhead bits for a total of 190 bytes per frame. To accommodate E3 SMDS applications, the input bytes should be applied to the TDAT[7:0] pins in reverse bit order so that the MSB will be transmitted first.

The PPDL transmitter can be used with a nibble-wide interface for DS3 SMDS applications if desired. To enable nibble-wide transmission, both the Nibble Mode Enable [Nibble;CR05.0] and DisPPDL bits in the PPDL Control Register should be set to one. Data should be inserted on the TDAT[3:0] pins; MSB on TDAT[2], second MSB on TDAT[1], next MSB on TDAT[0], LSB on TDAT[3] in response to TXBCK/TXGAPCK (which now occurs every 4 bits). In nibble mode, the nibbles are transmitted MSB first and are nibble-aligned after each overhead bit in the DS3 frame for a total of 21 nibbles per 85-bit data block. Nibble mode should not be used for E3 applications. In this mode (Nibble mode and PPDLONLY pin = 0), the transmit PPDL interface shifts the serial data by one bit. This anomaly (only on the transmit side) can be remedied by the circuit shown in Figure 2-9.

Figure 2-9. Nibble Mode with the PPDLONLY Control Pin Low



Data Bit	Input Pin
MSB	TDAT[2]
2SB	TDAT[1]
1SB	TDAT[0]
LSB	D Input
Q Output	TDAT[3]

FCS calculation can be limited to the first N bytes of the transmitted message by setting the Limit Frame Check Sequence Calculation [LimitFCS;CR05.3] control bit. In this mode, the FCS is calculated on the first N bytes transmitted after the opening flag and then held until the end of the message. It is then appended to the end of the message in normal fashion. The desired number N can be from 1 to 16 (a value of 0 gives N=16) and is loaded in the Frame Check Sequence Calculation Count [FCSCnt[3:0];CR05.7:4] control field. This allows FCS calculation only on the header information in a T1 packet voice format.

2.3.9 PPDLONLY Mode

The transmitter can be placed in a mode where the entire transmit stream consists of data with no DS3/E3 overhead bits inserted. This mode is enabled by providing a high input on the PPDLONLY input pin. This mode allows the CN8330 to be used as a high-speed PPDL formatter and can be used at any clock rate up to the full 52 MHz capability of the device. Data and controls are provided to the transmitter in response to the transmit byte clock. When PPDLONLY mode is set, the transmit NRZ data stream is available on the RXCCK/TXNRZ pin.

2.3.10 Transmitter Outputs

The TXPOS and TXNEG pins provide a variety of signals depending on the control bits in the Feature Control Register. Table 2-1 summarizes the available output combinations when the Test Equipment Feature Select bit [TstEqSel;CR04.7] is low.

Table 2-1. Transmit Encoding Options

DisEnc	AMI/LCV2	Transmit Output
0	0	B3ZS/HDB3 Encoded Data on TXPOS, TXNEG
0	1	AMI Encoded Data on TXPOS, TXNEG
1	0	NRZ Data on TXPOS, Transmit Clock on TXNEG
1	1	NRZ Data on TXPOS, Transmit Clock on TXNEG

2.3.11 Test Equipment Specific Features

Additional features in the transmitter are available if parallel mode is not selected (ParaEn = 0). The RDAT[7]/TXNRZ pin becomes an output of the transmit data in NRZ format before being presented to the B3ZS/HDB3 encoder. The TDAT[5]/TXENCI pin is an input directly to the B3ZS/HDB3 encoder. This input is selected if the TstEqSel bit is set high. This allows either direct insertion of data for B3ZS/HDB3 encoding or modification of the transmit data via RDAT[7] and reinsertion of this stream for encoding. The TDAT[4]/LCVERRI pin is an input that allows insertion of line code violations into the transmit data stream. This input is also enabled when the TstEqSel bit is set high. When enabled, a line code violation will be inserted at the next opportunity each time the LCVERRI pin is high. The input should be high for only one clock cycle to guarantee that only one line code violation is generated. If the AMI/LCV2 control bit in the Feature Control Register is low, a valid insertion opportunity is defined as the second 1 in a 11 sequence. If AMI/LCV2 is high, a valid insertion opportunity is defined as the next B3ZS/HDB3 substitution. The opposite polarity of substitution pattern will be inserted if an error is to be generated (a B0V/B00V instead of an 00V/000V or vice versa). This avoids the possibility of incorrectly emulating a B3ZS/HDB3 substitution pattern and causing bit errors.

NOTE: B = Legal Bipolar Pulse; V = Bipolar Violation Pulse.

2.4 Receiver Operation

2.4.1 Bipolar-to-Unipolar Conversion

The bipolar-to-unipolar recovery circuit includes the B3ZS/HDB3 decoding circuit. Decoding is done according to TR-TSY-000009 for B3ZS or G.703 for HDB3. A circuit detects the B3ZS/HDB3 signature and the substitution back to three or four zeros is made. Substitution to three or four zeros is made on every occurrence of 00V/B0V (B3ZS) or 000V/B00V (HDB3). Bipolar and line code violations (other than those associated with a valid B3ZS/HDB3 signature) are counted in the 16-bit DS3/E3 LCV Counter [SR12,SR13;0x25,0x26] that is cleared when read. In DS3 mode, a substitution pattern of improper polarity (B0V for 00V or vice versa) will be decoded to three zeros but will be counted as a bipolar violation. Occurrences of three or more zeros before B3ZS decoding will also be counted as a bipolar violation.

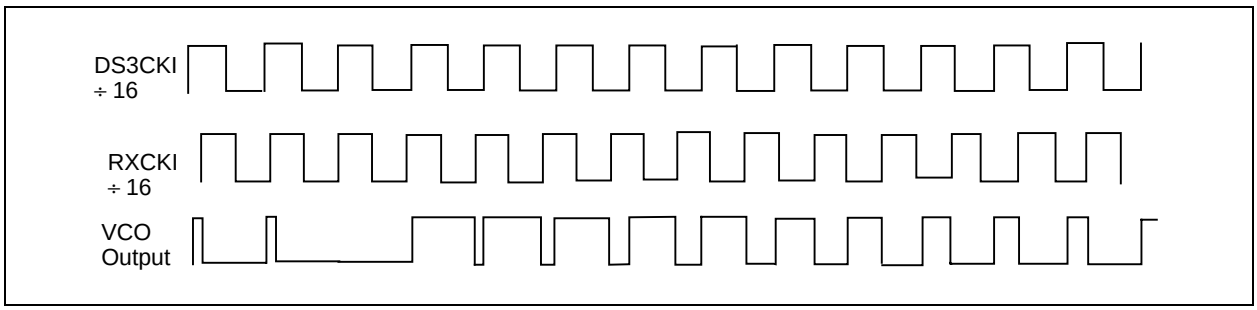
In E3 mode, Line Code Violations (LCVs) are counted in the DS3/E3 LCV Counter. An LCV is defined by ITU-T O.161 as two consecutive BPVs of the same polarity. Occurrences of four or more zeros before HDB3 decoding will *not* be counted as an LCV.

B3ZS/HDB3 decoding can be defeated by connecting the RXPOS and RXNEG inputs together and supplying NRZ input data to both pins or by setting the AMI/LCV2 control bit high and supplying a non-encoded AMI signal on RXPOS and RXNEG.

2.4.2 Receive FIFO

The receiver circuit contains a 16-bit FIFO buffer immediately following the B3ZS decoding circuit to provide jitter elasticity of up to ± 5 unit intervals. The data is clocked into the FIFO buffer with the incoming DS3CKI clock. Data is clocked out of the FIFO buffer and into the remaining receiver circuitry by the RXCKI which is a dejittered version of DS3CKI. The FIFO buffer circuit provides a VCO control signal to indicate the phase relationship of the FIFO buffer input and output clocks. Both clocks are divided by 16 internally to derive the VCO output as shown in Figure 2-10. This signal can be used to control the clock recovery circuit producing the smoothed RXCKI. The FIFO buffer circuit is bypassed and all receiver circuitry is clocked with DS3CKI if FIFEN is low. RXCKI should be tied to ground if the FIFO buffer is disabled.

Figure 2-10. VCO Output Signal Timing



2.4.3 Received Signal Output

The received unipolar signal is recovered and provided with a clock on RXDAT and RXCLK. An M-frame synchronization signal and gapped clock are also provided. Figure 2-11 shows a timing diagram for DS3 mode with negligible propagation delays for the DS3 receiver output signals. Refer to the Electrical and Mechanical Specifications section for actual propagation delay specifications. RXMSY is low during subframe 7 preceding the X1 bit in the first subframe. Outputs change on the rising edge of the receive clock except for the gapped clock on RXBCK/RXGAPCK. This clock is an inverted version of RXCLK with a gapped pulse every 85 bits. The receive clock will be nominally 44.736 MHz. Data on RXDAT can be clocked into the user's circuit with the rising edge of the RXBCK/RXGAPCK if it is desired to observe only data bits (there is no rising edge present during the overhead bit positions). The rising edge of RXBCK will be mid-bit for each payload bit in the serial stream. An overhead indicator RDAT[6]/RXOVH is available when the PPDL is not enabled. This signal is low for each bit position that is an overhead bit in the receive serial stream.

Figure 2-11. Receiver Timing for Serial DS3 Mode

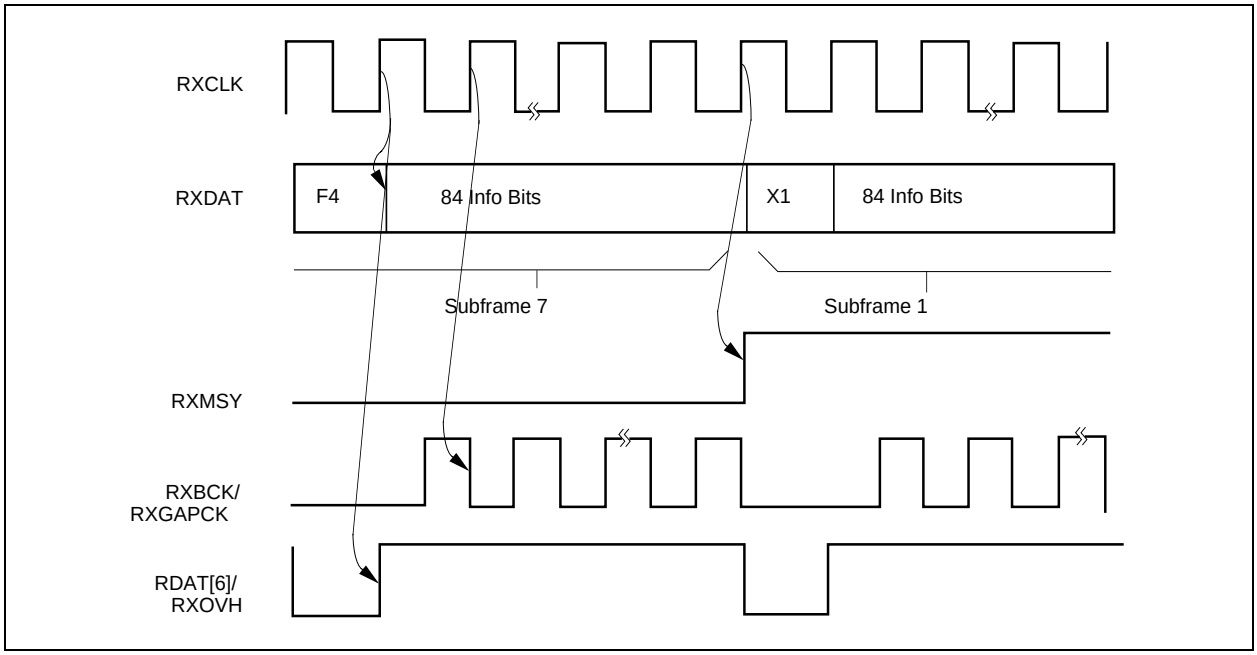


Figure 2-12 illustrates the receiver timing for the parallel DS3 mode. This mode is enabled by setting the ParaEn bit in the Feature Control Register and setting the DisPPDL bit in the PPDL Control Register. The receive data is valid on either the rising or falling edge of RXBCK.

Figure 2-12. Receiver Timing for Parallel DS3 Mode

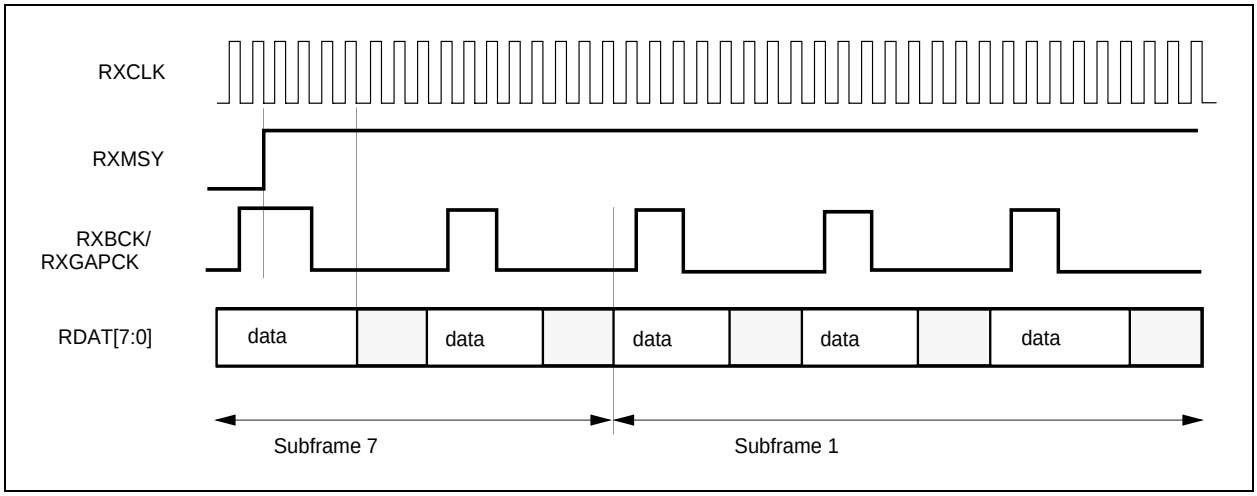
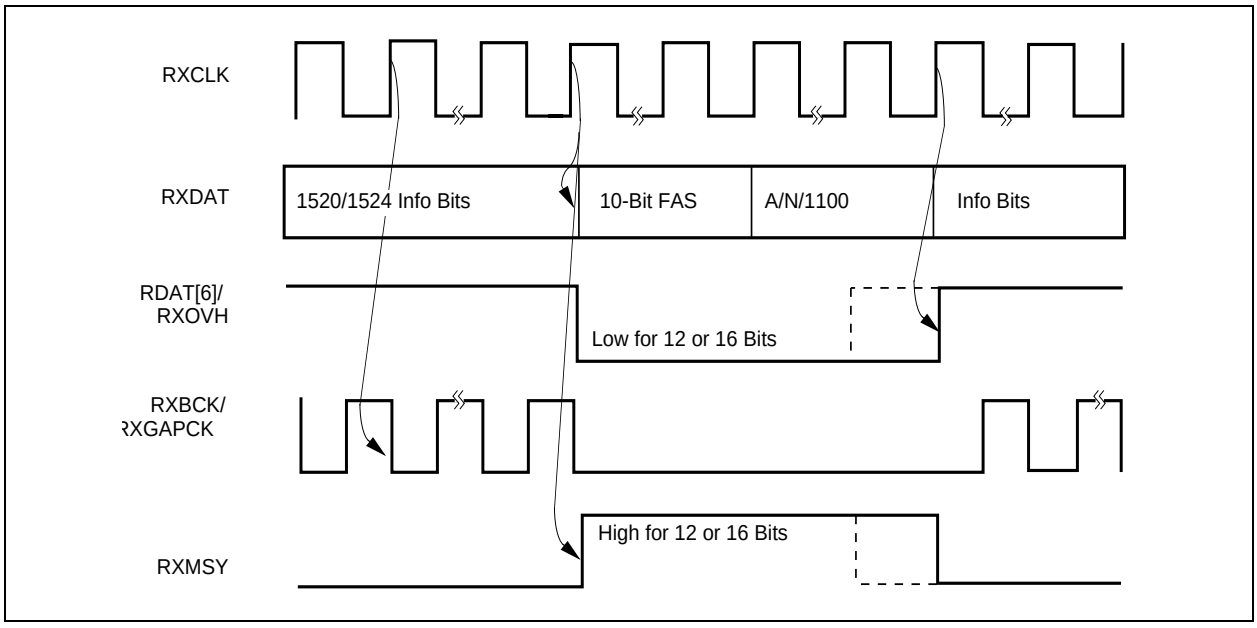


Figure 2-13 illustrates a timing diagram for the E3 receiver output signal with the PPDL enabled. The clock and data edge relationships are similar to those in DS3 mode. The M-frame synchronization signal RXMSY is high during the 12-bit block corresponding to the 10-bit FAS and the A and N bits. If the PPDL is enabled, the M-frame synchronization signal will be high for four additional bit periods corresponding to the 1100 pattern found in SMDS formatted signals. RDAT[6]/RXOVH will be low for 12 bits in serial mode and for 16 bits if the PPDL is enabled.

Figure 2-13. E3 Receiver Output Timing



2.4.4 Framing Operation

In DS3 mode, a parallel search framing circuit is used to recover the subframe and M-frame alignments in the DS3 signal. Framing is initiated by an Out-of-Frame (OOF) condition as determined by the receiver frame bit check circuitry. When 3 out of 16 consecutive subframing (F) bits are in error or when 2 out of 3 consecutive M-frames have M bit errors, an OOF condition is declared. Average reframe time is less than 1 msec.

In E3 mode, a serial search for the 10-bit FAS pattern (1111 0100 00) is conducted. When three consecutive correct patterns are found, the receiver is declared to be in frame. An OOF condition is declared when four consecutive incorrect FAS patterns are detected. Average reframe time is less than 250 µsec.

In either mode, serial data continues to be present on RXDAT and RXMSY and will continue to indicate the old framing position until the OOF condition clears. RXMSY will indicate the new framing position when the OOF condition is cleared.

2.4.5 Alarm Detection

The CN8330 receiver contains status indicators to obtain alarm information for link maintenance.

Alarm Indication Signal Detect [AISDet;SR00.2] in the DS3/E3 Maintenance Status Register [SR00;0x10] is updated each M-frame interval. It is set if AIS was detected in the previous M-frame. An AIS condition is present when there is valid framing and parity, both X-bits are equal, all C-bits are zero, and the payload bits are 1010... starting with 10 after each overhead bit. This signal can be integrated by the controller to declare a received AIS. In E3 mode, an unframed all-ones signal is detected as AIS.

Idle Code Detect [IdleDet;SR00.4] is updated each M-frame interval. It is set if the idle code condition was detected in the previous M-frame. The idle code condition is present when there is valid framing and parity, both X-bits are equal, all C-bits in subframe 3 are zero, and the payload bits are 1100... starting with 11 after each overhead bit. No idle code is defined for E3 signals; therefore, IdleDet will indicate zero in E3 mode.

Yellow Alarm Detect [YelDet;SR00.3] is updated each M-frame interval and is an active high indication that both X-bits in the previous M-frame were low. This indication will not be set if the X-bits are in disagreement or if both X-bits are high. In E3 mode, YelDet will be set if the A-bit is high.

Loss-of-Signal Alarm [LOSAlm;SR00.0] is set as soon as 175 ± 75 consecutive zeros (prior to B3ZS/HDB3 decoding) are received. This alarm condition is set as soon as the condition is detected. The indication is cleared when a one's density of more than 33 percent (25 percent for E3) is achieved for 175 ± 75 clock cycles. Note that in some systems, a loss-of-signal alarm is not cleared until the receiver is in frame. This function can be performed by the controller.

The frame bits are monitored to determine errors and OOF conditions. The OOF indicator is set whenever 3 of 16 consecutive F framing bits are in error or when 2 of 3 consecutive M-frames have M-bit errors in DS3 mode. In E3 mode, four consecutive occurrences of an incorrect FAS will result in an OOF condition. Auxiliary error indication outputs are available when the PPDL is not enabled. A 1-bit-period-wide pulse for each F- or M-bit error or each incorrect FAS is available on the RDAT[4]/FRMERR pin. Indications of LOS, OOF, AIS, and IDLE are available on RDAT[0:3], respectively. These indications are not internally latched and do not require action from the microprocessor to clear.

2.4.6 Terminal Data Link Reception

LAPD receiver logic for the terminal data link in C-bit parity format is included in the framer circuit. Data link reception is also provided for the N-bit in E3 mode. This logic manages an 8-byte message buffer for the data link receiver. Idle and abort flag detection, FCS checking, and stuffed zero removal are also included. Microprocessor interrupts are used to synchronize the passing of data to and from the message buffer.

The terminal data link receiver is under the control of the received data stream only. The receiver interrupt is under the control of Receive Data Link Interrupt Enable [RxTDLIE;CR01.7] in the Terminal Data Link Control Register and CBitP/DL in the Mode Control Register. This interrupt must be enabled by setting both of these bits for receiver interrupts to appear on the DLINT/SOURCELB output and for proper interaction with the processor. The C-bits in subframe 5 in C-bit parity mode or standard DS3 mode (the N-bit in E3 mode) are provided to the receiver circuitry at all times. Therefore, when the DS3/E3 Maintenance Status Register indicates that alarms are being received rendering the data link information useless, it may be desirable to disable the RxTDLIE bit to prevent excessive or spurious interrupts to the processor. Receiver status is monitored via Receive Terminal Data Link Interrupt [RxTDLItr;SR02.2] in the Data Link Interrupt Status Register and via the Terminal Data Link Status Register [SR04;0x14]. When a receive data link interrupt is generated on DLINT/SOURCELB, the RXTDLItr bit will be set in the Data Link Interrupt Status Register. If this bit is observed upon reading the Data Link Interrupt Status Register, then the Terminal Data Link Status Register should be read to get the receiver status that caused the interrupt.

The Terminal Data Link Status Register contains 3 status bits and a 3-bit buffer pointer. The status bits are Abort Flag Received [RxAbort;SR04.0], Bad FCS [BadFCS;SR04.1], and Idle Code Received [RxIdle;SR04.2]. The 3-bit buffer pointer, Byte Received [RxByte[2:0];SR04.5:3], is used to point to locations in the 8-byte Receive Terminal Data Link Message Buffer [RxTDL;0x40–0x47]. The buffer pointer indicates the last location written by the data link receiver.

The receiver implements a LAPD data link per CCITT standard Q.921. The functions provided by the data link receiver circuitry are transparency zero removal, FCS checking, idle flag reception, and abort flag reception. There are no restrictions on the total length of the message. Q.921 requires all messages be an integral number of 8-bit bytes. If the receiver receives a message that is not an integral number of bytes, the receiver status will indicate a message received with bad FCS. The per-byte reception time is approximately 284 microseconds in C-bit parity mode and approximately 357 microseconds in E3 mode.

The receiver powers up in an indeterminate state. It is initialized by the receipt of an idle flag (0x7E) on the link, which sets RxIdle = 1 in the Terminal Data Link Status Register. When the idle flag is removed from the link and a message starts coming in, the receiver removes stuffed zeros and writes the resulting data to the Receive Terminal Data Link Message Buffer beginning with address 0x40 and counting up to 0x47.

When the first four addresses have been written, the processor is interrupted to read the data out of the buffer. The processor has four byte intervals (at least 1 msec) to read the data before it is overwritten with new data. The interrupt is cleared when the processor reads the Terminal Data Link Register. This register will indicate a message in progress at this time (RxIdle = 0, RxByte[2:0] = 3). If the upper half of the buffer had just been filled, the status register will indicate RxByte[2:0] = 111 and locations 4 through 7 must be read during the next four byte intervals to retrieve the message.

When the last block of data has been received, the processor will again be interrupted. This time the Terminal Data Link Status Register will indicate the end of message (RxIdle = 1, RxByte[2:0] = n, BadFCS = 0 or 1). The RxByte[2:0] = n portion of the register indicates the highest numbered location that was written in the receive buffer. Locations 0 to n or 4 to m (where n = 0 to 3 and m = 4 to 7) must be read to retrieve the data depending on what has already been read at the previous interrupt. The two highest numbered locations contain the FCS that was received at the end of the message. A new incoming message will always start in the opposite buffer half from where the previous message ended to prevent overwriting of previously received bytes and allow the processor time to retrieve those bytes. For example, if a message ended in buffer address 0x44, 0x45, 0x46, or 0x47, the next message received would be stored beginning in address 0x40. If a message ended in buffer address 0x40, 0x41, 0x42, or 0x43, the next message received would be stored beginning in address 0x44.

If the received message is a multiple of 8 bytes, then when the processor is interrupted to read the last block of data, the FCS has yet to be received. In this event, the processor will again be interrupted when the FCS has been checked and an idle flag is received. The Terminal Data Link Status Register will show RxByte[2:0] = 001 (or 101), BadFCS = 0 or 1, and RxIdle = 1; and the FCS received will be in locations 0 and 1 (or 4 and 5). Again, the data must be read out during the next four byte intervals, or it may be overwritten by a new incoming message. Alternatively, the FCS data may be ignored, and the good or bad indication used directly. It is important that software strategies allow for the fact that the LAPD receiver cannot recognize the FCS as such until the closing flag is recognized. It can happen that the processor is interrupted to read four message bytes, and the next byte received is the closing flag. When the processor exits the interrupt routine, another interrupt will be pending for the end of message. The status for this interrupt will indicate the idle condition, the FCS status, and the byte count will be the same as the previous interrupt (RxByte[2:0] = 011 or 111) because no extra bytes were received. In this event, the last two bytes read from memory on the previous interrupt were not message bytes after all, but were actually the FCS bytes. If the FCS spans a 4-byte boundary, the final interrupt will indicate the idle condition, the FCS status, and that one additional byte was received (RxByte[2:0] = 000 or 100).

2.4.6.1 Receiver Interrupts

The data link receiver generates an interrupt in response to three events: the current half of the message buffer is full, the end-of-message flag was detected, or an abort flag was detected. The Terminal Data Link Status Register indicates the cause of the interrupt. The interrupt will be cleared upon the reading of this register.

If the interrupt is due to the current half of the receive buffer being full, RxIdle will be cleared, and RxByte[2:0] will indicate which half of the buffer must be read.

If the interrupt is due to the end-of-message flag being detected, RxIdle will be set, BadFCS will indicate the result of the FCS error check, and RxByte[2:0] will indicate the last location written. The processor will not be interrupted again until 4 bytes of a new message have been received.

If the interrupt is due to an abort flag being received, Abort will be set, and there is nothing to do other than discard any previously received message bytes. The processor will not be interrupted again until 4 bytes of a new message have been received.

Interrupts from the terminal data link receiver will appear on RxTDLItr in the Data Link Interrupt Status Register. Interrupts must be enabled to appear on DLINT/SOURCELB by setting the CBitP/DL bit in the Mode Control Register and RxTDLIE bit in the Terminal Data Link Control Register in either C-bit parity mode or E3 mode.

2.4.6.2 Receiver Response Example

The following example shows the sequence necessary to receive an 8-byte hex message that is stored starting in the lower half of the receive buffer. The final interrupt indicates that two more bytes are present in the buffer but these bytes are FCS bytes, not message bytes. When an interrupt is received, the processor reads the Data Link Interrupt Status Register to determine the source of the interrupt. If the source is determined to be the receive terminal data link, the processor will respond in the following manner:

At RX Interrupt:

read address 0x14 to get status (status = 0x18: RxByte[2:0] = 011, RxIdle = 0)

read address 0x40 to get 1st data byte
read address 0x41 to get 2nd data byte
read address 0x42 to get 3rd data byte
read address 0x43 to get 4th data byte

At RX Interrupt:

read address 0x14 to get status (status = 0x38: RxByte[2:0] = 111, RxIdle = 0)
read address 0x44 to get 5th data byte
read address 0x45 to get 6th data byte
read address 0x46 to get 7th data byte
read address 0x47 to get 8th data byte

At RX Interrupt:

read address 0x14 to get status (status = 0x0C or 0x0E: RxByte[2:0] = 001, RxIdle = 1, BadFCS = 0 or 1)
read address 0x40 if desired (FCS byte 1)
read address 0x41 if desired (FCS byte 2)

2.4.7 RxFEAC Channel Reception

Receiver logic is provided for reception of the Receive Far End Alarm and Control (RxFEAC) Channel which is present in C-bit parity mode. This channel uses a bit-oriented protocol and received data is provided in the Receive FEAC Channel Byte Register [SR03;0x13].

The RxFEAC channel receiver is under control only of the received data stream. The receiver interrupt is under control of Receive FEAC Interrupt Enable [RxFEACIE;CR02.6] in the Status Interrupt Control Register and the CBitP/DL bit in the Mode Control Register. This interrupt must be enabled by setting both of these bits for receiver interrupts to appear on the DLINT/SOURCELB output and for proper interaction with the processor. The last C-bit in subframe 1 in C-bit parity mode or in M13 mode is provided to the receiver circuitry at all times. There is no RxFEAC channel capability in E3 mode. Therefore, when E3 mode is selected with CBitP/DL set or when the Mode Control Register indicates that alarms are being received rendering the data link information useless, it may be desirable to disable the receive FEAC interrupt via the RxFEACIE bit to prevent excessive or spurious interrupts to the processor.

Receiver status is monitored via the Receive FEAC Channel Interrupt [RxFEACItr;SR02.0]. When an RxFEAC channel interrupt is generated on DLINT/SOURCELB, the RxFEACItr bit will be set in the Data Link Interrupt Status Register. If this bit is observed to be a 1 upon reading the Data Link Interrupt Status Register, then another byte has been received and placed in the Receive FEAC Channel Byte Register.

An idle message is all-ones and all other messages are of the form “0xxxmmm011111111” with reception of the rightmost bit first from the channel. The receiver logic recognizes the eight ones message flag followed by a message byte and interrupts the controller upon reception of a valid message byte. The “0mmmxxx0” message byte that was received is stored in the Receive FEAC Channel Byte Register. Continuous incoming messages on the RxFEAC channel will produce an interrupt rate of approximately one interrupt per 1.7 msec for this interrupt source. No interrupts are generated if the RxFEAC channel is receiving continuous idle flags, the interrupt is not enabled in the Status Interrupt Control Register, or CBitP/DL bit is not set. Reading the Receive FEAC Channel Byte Register clears the interrupt.

Interrupts from the RxFEAC channel receiver will appear on the RxFEACItr. Interrupts must be enabled to appear on DLINT/SOURCELB by setting both CBitP/DL in the Mode Control Register and the RxFEACIE bit in the Status Interrupt Control Register.

2.4.8 PPDL Receiver

The receiver circuitry contains a PPDL receiver for the payload portion of the CN8330 data that is activated when the ParaEn bit in the Feature Control Register is set. This receiver performs idle flag detection, stuffed zero deletion, and FCS checking on the incoming data stream. The recovered data bytes are presented on RDAT[7:0] and are valid on both the rising and falling edges of RXBCK/RXGAPCK. The LSB is on RDAT[0] and the MSB on RDAT[7]/TXNRZ; the LSB is the first received from the serial input. If the payload stream contains idle flags, the IDLE pin will be high and the flags will be present on RDAT[7:0]. If a valid FCS is received at the end of the message block, the VALFCS/TXOVH pin will be active high while IDLE/FRMCAR is high. At the start of the next message, both indications will go low until the end of the incoming message has been received. If a bad FCS is received, IDLE/FRMCAR will go high and VALFCS/TXOVH will remain low. If VALFCS/TXOVH goes high and IDLE/FRMCAR does not, an abort sequence was received in the data. If there is only one flag received between incoming packets, there will be only one RXBCK/RXGAPCK pulse present while IDLE/FRMCAR is high. If the 32-bit CRC Select bit (CRC32;CR05.2) is low, the FCS is checked with the polynomial:

$$x^{16}+x^{12}+x^{5}+1$$

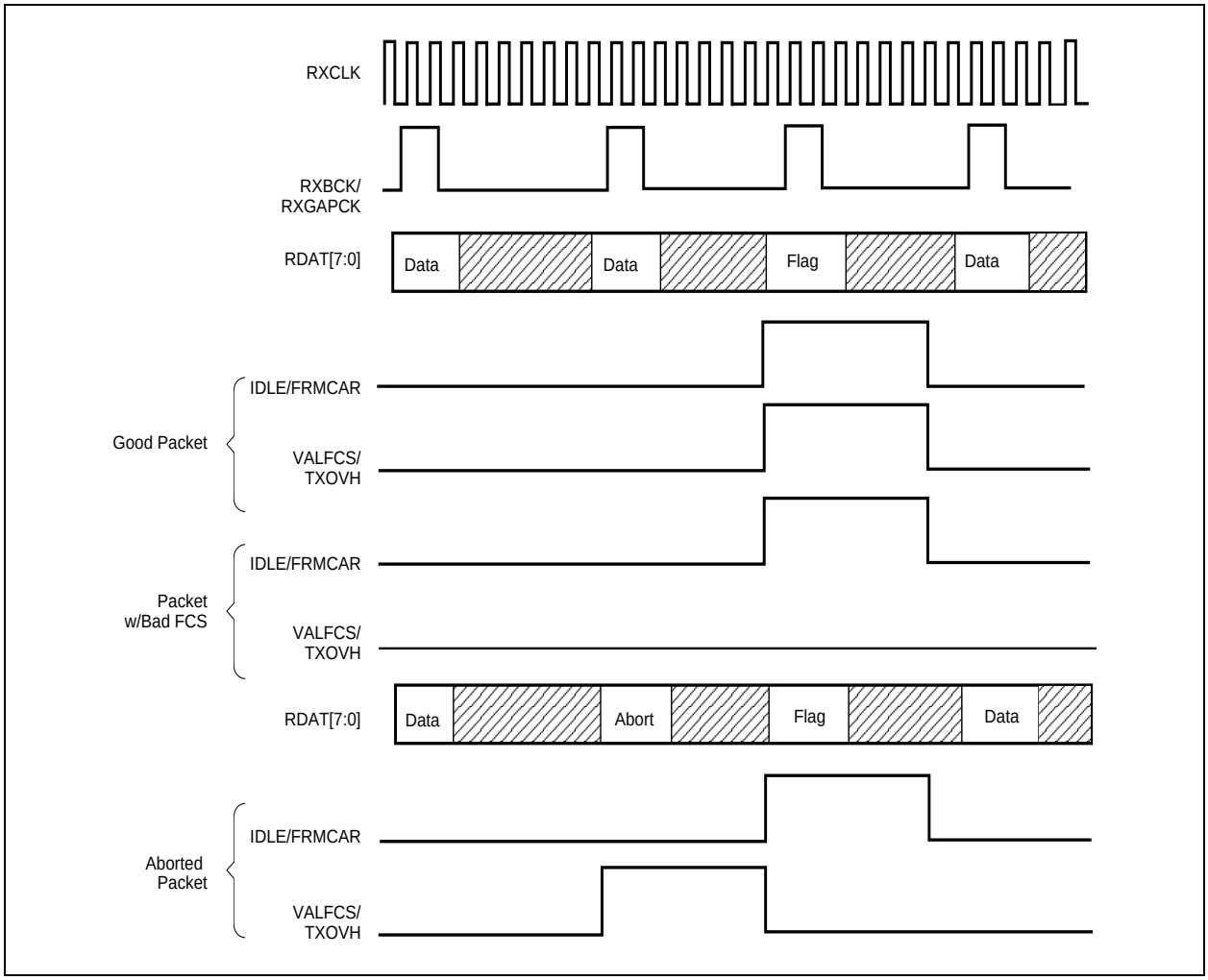
If 32-bit CRC is selected by setting the CRC32 bit high, then the FCS is checked with the polynomial:

$$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+ x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$$

Timing for this operation is shown in Figure 2-14.

Illustrated are cases of a good packet received, a packet received with a bad FCS, and an aborted packet. Each packet is shown with one idle flag marking the end of the packet and the start of the next packet. However, more than one flag can occur in the serial stream. The output data will contain each occurrence of idle or abort flags with a pulse on RXBCK/RXGAPCK.

Figure 2-14. PPDL Receiver Timing



RXBCK/RXGAPCK is generated from the falling edge of the receive serial clock input (either DS3CKI or RXCKI depending on FIFEN) and is present continuously like the transmit byte clock. Nominally there will be one pulse on RXBCK/RXGAPCK for every eight clock cycles on the receive serial clock. When an inserted transparency bit must be deleted or DS3/E3 overhead bits skipped, the RXBCK/RXGAPCK period will be lengthened by one or more serial clock cycles. RXBCK/RXGAPCK is present during the reception of FCS octets and idle flags. The RDAT[7:0], IDLE/FRMCAR, and VALFCS/TXOVH outputs are valid at least one serial clock cycle period before the rising edge of RXBCK/RXGAPCK and are valid for at least two serial clock cycle periods after the falling edge of RXBCK/RXGAPCK.

The parallel interface can be used without transparency bit deletion by setting the DisPPDL bit in the PPDL Control Register to a 1. In this mode, byte synchronization in the transmitter and receiver is achieved from the M-frame sync alignment and zeros detected after strings of five ones are not deleted. This allows the byte-wide interface to be used as the data output in normal DS3/E3 mode rather than the serial output pin. The IDLE/FRMCAR and VALFCS/TXOVH indications are ignored when operating in this mode. Data bytes are received with the same timing relative to RXBCK/RXGAPCK as in HDLC mode. In E3 mode, 190 bytes per frame will be received with byte alignment after the 16 overhead bits (FAS, A, N, 1100).

The PPDL receiver can be used with a nibble-wide interface for DS3 SMDS applications if desired. To enable nibble-wide transmission, both the Nibble Mode Enable and DisPPDL bit controls in the PPDL Control Register should be set to 1. Received data is available on the least significant nibble of the RDAT[7:0] pins with the same timing relative to RXBCK/RXGAPCK (which now occurs every 4 bits). In nibble mode, the nibbles are received MSB first, with the MSB on RDAT[3], 2SB on RDAT[2], 1SB on RDAT[1], and the LSB on RDAT[0]. For E3 SMDS applications, the byte-wide interface should be used.

FCS checking can be limited to the first N bytes of the received message by setting the LimitFCS control bit in the PPDL Control Register. In this mode, the FCS is checked only on the first N bytes received after the opening flag and then held until the end of the message. The locally calculated FCS is then compared to the last two/four bytes in the message to determine if a valid FCS was received. The desired number N can be from 1 to 16 (a value of 0 gives N = 16) and is loaded in the FCSCnt[3:0] control field in the PPDL Control Register. This allows FCS checking only on the header information in a T1 packet voice format.

2.4.9 PPDLONLY Mode

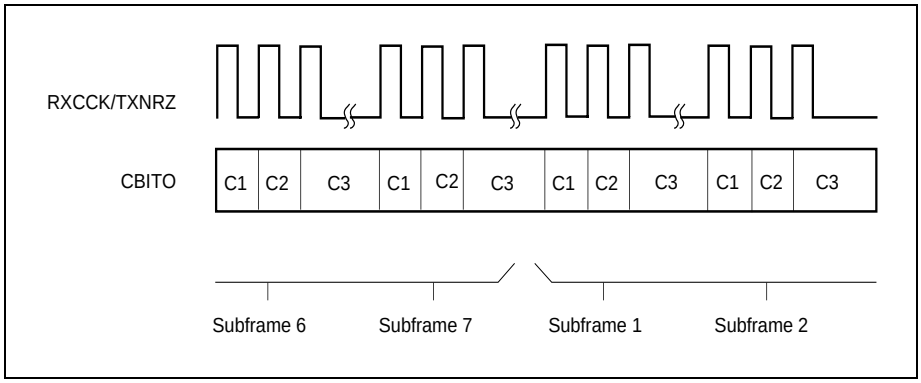
The receiver can be placed in a mode where the entire receive stream is expected to be data with no DS3/E3 overhead bits inserted. This mode is enabled by providing a high input on the PPDLONLY input pin. This mode allows the IC to be used as a high-speed PPDL receiver and can be used at any clock rate up to the full 52 MHz capability of the device. This data interface is described in the PPDL Receiver section of this chapter.

2.4.10 Serial C-Bit Output

All received C-bits are output on the CBITO pin on the rising edge of RXCCK/TZNRZ in DS3 mode. This allows external circuitry to examine individual C-bits if necessary. The timing is shown in Figure 2-15.

The received N-bits are output on the CBITO pin on the rising edge of RXCCK/TZNRZ in E3 mode. This allows external circuitry to process the N-bit if necessary. The relative timing is the same as in DS3 mode except there is only one N-bit per frame.

Figure 2-15. C-Bit Output Timing



2.5 Monitor Mode for Stand-Alone Operation

Operation without a microprocessor is possible with the MON/MIC* pin tied high. In this mode of operation, the transmitter is set to M13 format with External C-Bit Insert [ExtCBit;CR00.2] enabled. E3 mode operation is not available without a microprocessor. External circuitry must format all of the C-bit locations to the desired values and present them on the CBITI pin in response to the TXCCK clock output. Proper C-bit ordering can be determined by the relationship to the input or output M-frame syncs (TDAT[7]/TXSYI or TXSYO). The parallel data input port for the PPDL transmitter is enabled by setting the PAREN input high. Setting the CRC32 input high selects the 32-bit CRC mode. Two special modes are available when in stand-alone operation. When the PAREN input is high and the PPDLONLY input is low, the byte-wide interfaces are enabled with transparency bit insertion/deletion disabled. This allows the CN8330 to be used as a DS3 device with a parallel interface. When the PAREN input is high and the PPDLONLY input is high, the byte-wide interfaces are enabled. Transparency bit insertion/deletion is enabled. DS3 framing is disabled. This allows the CN8330 to be used as a high-speed HDLC formatter. The transmit serial data stream is available in NRZ format on the RXCCK pin in this mode.

Alarm generation in this mode is controlled by the CS/ALM0 and RD*/ALM1 pins. Setting these pins, as described under Mode Control Register in the Registers chapter of this document, will enable transmission of the specified alarm signal (the TxAlm[1:0] bits work identically to the pins).

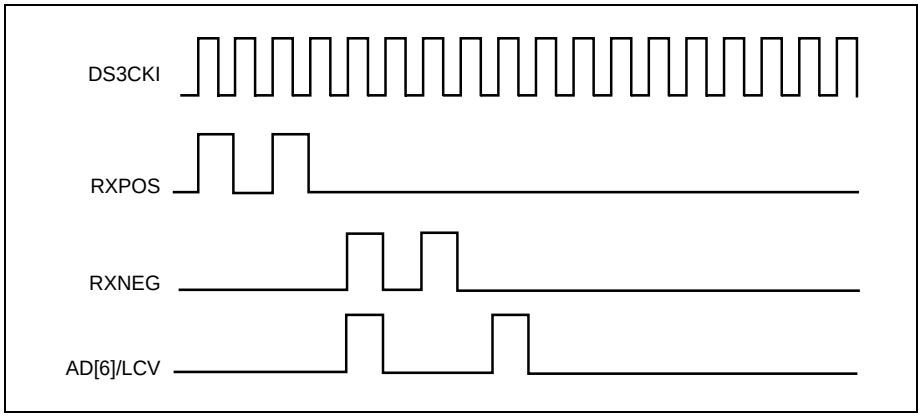
The receiver will monitor all DS3 maintenance alarms and indications and provide occurrences of any alarm on the FRMERR, LCV, PAR, IDLE, YEL, AIS, OOF, and LOS pins (AD[6:0]). These indications can then be counted by external circuitry for appropriate action. The received data is present on the RXDAT pin and, if the parallel port is enabled, on the RDAT[7:0] pins. All C-bits are clocked out on CBITO for external processing.

2.5.1 DS3 Monitor Mode Error Outputs

If stand-alone monitor mode is selected by tying the MON/MIC* pin high, then the CN8330 operates without a microprocessor and the eight address/data pins (AD[7:0]) of the microprocessor interface become DS3 alarm and error indication outputs (Note that E3 framing is not available in monitor mode). Outputs are provided for LOS, OOF, AIS, yellow alarm (X-bit low or A-bit high), idle code detect, parity errors, LCVs, and frame bit errors. All indications except LCV and frame bit errors are level indications and can be counted externally on a per M-frame basis, if desired. The frame error output is a pulse for each error in the M- or F-bit positions and can drive a counter directly. The LCV output will be high for every bit position that is an LCV and can be used with the RXCLK output to facilitate external counting. All indications are active high and can be used to indicate the presence of the condition without reference to the clock output. Figure 2-16 illustrates an LCV indication. The LCV indications are delayed from the pulse inputs due to B3ZS decoding.

Monitor mode is supported only in DS3 mode. Standalone E3 and HDLC monitor mode is not supported.

Figure 2-16. Monitor Mode Error Indication Timing



3.0 Registers

For a summary of all registers, refer to the Register Summary section at the end of this chapter.

3.1 Control Registers

0x00—Mode Control Register (CR00)

7	6	5	4	3	2	1	0
LineLp	SourceLp	TxAlm1	TxAlm0	ExtOvh	ExtCBit	E3Frm	CBitP/DL

LineLp Line Loopback Enable—Set to enable the loopback in the external direction (back to network). This loopback connects the received data stream before B3ZS/HDB3 decoding to the transmitter. All data and overhead bits are looped; and Bipolar Violations (BPVs) are fully preserved per ANSI standard T1.404. The received data is still presented to all receiver blocks and is present on the receiver output pins.

SourceLp Source Loopback Enable—Set to enable the loopback in the internal direction. This loopback connects the encoded transmitter data and clock directly to the receiver B3ZS/HDB3 decoder. Transmission of data on the line is not affected by this loopback.

TxAlm1,0 Transmit Alarm Control—Used to control transmission of various alarm signals. In DS3 mode, the AIS, idle, and yellow alarm signals on the outgoing DS3 stream are controlled as follows:

TxAlm1	TxAlm0	Alarm Action
0	0	Normal, No Alarms Transmitted
0	1	Yellow Alarm (X-bits low) Transmitted
1	0	Idle Code Transmitted
1	1	AIS Transmitted

In E3 mode, the TxAlm0 bit should be set high to transmit the E3 AIS signal and the TxAlm1 bit is set high to transmit the E3 yellow alarm (A-bit high). TxAlm0 bit has precedence in E3 mode.

ExtOvh External Overhead Insert—Set to a 1 to enable insertion of the overhead bits (DS3: X, P, M, and F or E3: FAS, A, and N) from the transmit serial data stream.

ExtCBit External C-Bit Insert—Used to control insertion of data in the C-bit or N-bit positions of the transmit data stream. In DS3 mode, the C-bits are controlled as follows:

U

C-Bit Parity Mode	Ext. C-Bit Insert	C-Bit Source
0	0	Serial Data Stream
0	1	CBITI Pin
1	0	All C-Bits Internally Generated
1	1	Internal Except CP and FEBE from CBITI Pin

In E3 mode, External C-Bit Insert controls insertion of data in the N-bit position of the E3 data stream. The N-bit will come from the CBITI pin when ExtCBit is high, and from the terminal data link transmitter when ExtCBit is low.

E3Frm E3 Framing Mode—Enables the E3 mode framing and transmission circuitry. This control bit has priority over the C-Bit Parity Mode/Enable DLINT bit. Framing insertion and recovery is performed as specified in ITU–T G.751

CBitP/DL C-Bit Parity Mode/Enable DLINT—Selects which type of framing is present on the transmitted DS3 signal. If this bit is low, then the basic DS3 framing mode is used. If this control bit is high, then the C-bit positions are used for the FEBE, FEAC, terminal data link, path parity, and mode indicator bits as defined in T1.107a-1989. When the E3 framing mode bit is high, this bit enables interrupts on the DLINT/SOURCELB output pin.

0x01—Terminal Data Link Control Register (CR01)

This Terminal Data Link Control Register controls functions of the terminal data link as defined in C-bit parity or E3 mode. If C-bit parity or E3 mode is not selected, the contents of this register are ignored.

7	6	5	4	3	2	1	0
RxTDLIE	DisTxTDL	TxByte[2]	TxByte[1]	TxByte[0]	TxAbort	TxFCS	TxMsg

RxTDLIE Receive Terminal Data Link Interrupt Enable—Enables the Receive Terminal Data Link Interrupt bit [RxTDLItr;SR02.2] to appear on the DLINT/SOURCELB output pin.

DisTxTDL Disable Transmit Terminal Data Link—Forces the output of the Transmit Terminal Data Link to all ones.

TxByte[2:0] Byte—A 3-bit pointer to the Transmit Terminal Data Link Message Buffer [TxTDL;0x30–0x37] address containing the last byte to be transmitted.

TxAbort Abort Message—Causes the data link transmitter to halt the message in progress, send an abort flag, and then resume transmission of idle flags on the data link.

TxFCS Send Frame Check Sequence—Used to control the transmission of the FCS at the end of a message block.

TxMsg Send Message—Instructs the transmitter to begin transmission of a message block on the terminal data link. Setting this bit removes the data link from idle flag transmission mode and enables interrupts to the controller for data bytes.

0x02—Status Interrupt Control Register (CR02)

The Status Interrupt Control Register is provided to enable or disable individual interrupt sources. To enable an interrupt from a particular source, the control bit corresponding to that source must be set high in the interrupt control register. This enables the interrupt from that source to appear on the CNTINT/LINELB output pin. If a source has its interrupt control bit set low, then interrupts from this counter will be masked from appearing on CNTINT/LINELB.

7	6	5	4	3	2	1	0
SR6IE	RxFEACIE	LCVCtrIE	FEBECtrIE	PthCtrIE	FerrCtrIE	DgrCtrIE	ParCtrlE

SR6IE Shadow Register Interrupt Enable—A control bit that allows interrupts from the Shadow Status Register [SR06;0x16] to appear on the CNTINT/LINELB output pin.

RxFEACIE Receive FEAC Interrupt Enable—A control bit that allows interrupts from the FEAC receiver to appear on the DLINT/SOURCELB output pin when in C-bit parity mode.

LCVCtrIE Line Code Violation Counter Interrupt Enable—A control bit that allows interrupts from the DS3/E3LCV Counter [SR12,SR13;0x25,0x26] to appear on the CNTINT/LINELB output pin.

FEBECtrIE FEBE Event Counter Interrupt Enable—A control bit that allows interrupts from the DS3 FEBE Event Counter [SR11;0x24] to appear on the CNTINT/LINELB output pin.

PthCtrIE Path Parity Error Counter Interrupt Enable—A control bit that allows interrupts from the Path Parity Error Counter [SR10;0x23] to appear on the CNTINT/LINELB output pin.

FerrCtrIE Frame Error Counter Interrupt Enable—A control bit that allows interrupts from the Frame Error Counter [SR09;0x22] to appear on the CNTINT/LINELB output pin.

DgrCtrIE Disagreement Counter Interrupt Enable—A control bit that allows interrupts from the DS3 Disagreement Counter [SR08;0x21]to appear on the CNTINT/LINELB output pin.

ParCtrIE Parity Error Counter Interrupt Enable—A control bit that allows interrupts from the DS3 Parity Error Counter [SR07;0x20]to appear on the CNTINT/LINELB output pin.

0x03—Transmit FEAC Channel Byte (CR03)

7	6	5	4	3	2	1	0
TxFEAC[7]	TxFEAC[6]	TxFEAC[5]	TxFEAC[4]	TxFEAC[3]	TxFEAC[2]	TxFEAC[1]	TxFEAC[0]

TxFEAC[7:0] Transmit FEAC Channel Message Byte—If the mode is set to C-bit parity, this register will be used as the data byte for the transmit FEAC channel transmitter. When this byte is in the form '0xxxxxx0' it is transmitted after every flag. If there is a one in either the most significant or least significant bit of this register, all ones (idle) will be transmitted on the data link and interrupts from this source will be disabled. Writing to this register clears the Transmit FEAC Channel Interrupt bit [TxFEACItr;SR02.1] in the Data Link Interrupt Status Register [SR02;0x12].

0x04—Feature Control Register (CR04)

The Feature Control Register is provided to enable or disable miscellaneous features in the CN8330.

7	6	5	4	3	2	1	0
TstEqSel	AMI/LCV2	DisEnc	DisLCV/Ferr	ParaEn	FEBEC[3]	FEBEC[2]	FEBEC[1]

TstEqSel Test Equipment Feature Select—Set high to enable direct access to the B3ZS/HDB3 encoder and to enable insertion of LCVs via the TDAT[5]/TXENCI and TDAT[4]/LCVERRI pins, respectively. Normal operation of the transmitter is enabled when this bit is low.

AMI/LCV2 AMI Mode/LCV Type 2—Set high to enable AMI outputs on TXPOS and TXNEG (no B3ZS/HDB3 encoding). If the Test Equipment Feature Select bit is also set high, then this bit selects the type of LCV errors created when TDAT[4]/LCVERRI is active (see Table 2-1).

DisEnc Disable B3ZS/HDB3 Encoding—Set high to disable the B3ZS/HDB3 encoder circuit and provide a unipolar NRZ output instead of B3ZS/HDB3 encoded output pulses. The unipolar output appears at the TXPOS pin and the DS3/E3 input clock is available on the TXNEG pin (see Table 2-1).

DisLCV/Ferr Disable Saturation of Line Code Violation/Frame Errors—Set to allow the LCV and Frame Error Counters to continue counting when the maximum count has been received without enabling the respective interrupt. This is for use with the carry output indications for these counters as described in DS3/E3 Error Counters section in this chapter.

ParaEn Parallel Data Enable—Set high to enable the PPDL transmitter and receiver as the source and sink for data. Eight-bit data bytes on the TDAT[7:0] and RDAT[7:0] buses for the PPDL transmitter and receiver are provided. In E3 mode, the overhead field is also altered as described in Framing-Bit Generation under the Transmitter Operation section in the Functional Description chapter. If this control bit is low, the TDAT[6]/TXDATI and RXDAT data lines are the data input and output, respectively, for the DS3/E3 stream.

FEBEC[3:1] FEBE Pattern Bit Field—Set to the 3-bit sequence that is to be sent each time a FEBE indication is to be transmitted in C-bit parity mode. This pattern is automatically transmitted when the receiver detects an F-bit or path parity error. The pattern must be anything other than all ones to indicate a FEBE to the far end. An all-ones pattern will disable FEBE transmission and should not be used for any other purpose.

0x05—PPDL Control Register (CR05)

The PPDL Control Register is provided to control the mode of operation of the PPDL transmitter and receiver.

7	6	5	4	3	2	1	0
FCSCnt[3]	FCSCnt[2]	FCSCnt[1]	FCSCnt[0]	LimitFCS	CRC32	DisPPDL	Nibble

FCSCnt[3:0] Frame Check Sequence Calculation Count—Determines the number of bytes over which the FCS is to be calculated. The number of bytes for calculation can be from 1 to 16 (a value of 0 results in 16 bytes of calculation).

LimitFCS Limit Frame Check Sequence Calculation—Set to enable FCS calculation only on the first N bytes of an HDLC frame where N is determined by the FCS Calculation Count field. If this bit is low, the FCS will be calculated over all transmitted bytes.

CRC32 32-Bit Cycle Redundancy Check—Set high to enable 32-bit CRC generation and checking on the PPDL. If this bit is low, then 16-bit CRC generation and checking is enabled.

DisPPDL Disable PPDL Transparency Bit—Set high to disable insertion and removal of HDLC transparency bits in the PPDL transmitter and receiver. If this control bit is low, then normal insertion and removal of HDLC transparency bits will occur.

Nibble Nibble Mode Enable—Set to enable the nibble mode interface to the PPDL transmitter and receiver for use in DS3 SMDS/802.6 applications. The Disable PPDL Transparency bit should be set high when nibble mode is enabled.

3.2 Status Registers

There are six Status Registers: five for DS3/E3 status and one to indicate the version number of the IC. Also included is a shadow register for the DS3/E3 maintenance status to latch status indications until read. The contents of these registers are described here and summarized in the Register Summary at the end of this section. The status signals are contained in latches and are applied to the controller data bus on the appropriate read command from the controller. The active state of all bits in the Status Registers is high.

0x10—DS3/E3 Maintenance Status Register (SR00)

The DS3/E3 Maintenance Status Register contains the major DS3/E3 maintenance indicators. Alarm detection details can be found in Alarm Detection in the Receiver Operation section of the Functional Description chapter.

7	6	5	4	3	2	1	0
ReFrm	FrmtID1	FrmtID0	IdleDet	YelDet	AISDet	OOFAlm	LOSAlm

ReFrm Reframe In Progress—Set while the framing circuit is searching for a valid framing pattern in either DS3 or E3 modes.

FrmtID1,0 Format Identification—Identifies the incoming format based on the contents of the application ID channel contained in the first C-bit of subframe 1. This bit pair will be set to 00 to indicate M13 format, 01 to indicate C-bit parity format, and 10 to indicate Syntran format. In E3 mode, these bits are meaningless and should be ignored.

IdleDet Idle Code Detect—Set if there is valid framing and parity, the three C-bits in subframe 3 are zero, both X-bits are equal, and the payload contains a 1100... pattern starting with an 11 after each overhead bit in DS3 mode. This bit will be low in E3 mode since there is no defined E3 idle signal.

YelDet Yellow Alarm Detect—Set for one M-frame interval when both X-bits are low in the previous M-frame in DS3 mode. This bit is set when the received A-bit is high in E3 mode. This bit will not go active if LOSAlm, OOFAlm, or AISDet are active.

AISDet Alarm Indication Signal Detect—Set if there is valid framing and parity, all C-bits are 0, both X-bits are equal, and the payload contains a 1010... pattern starting with a one after each overhead bit in DS3 mode. This bit is set when an unframed all-ones signal is received in E3 mode.

OOFAlm Out of Frame Alarm—Set when any 3 out of 16 consecutive F framing bits are in error or when 2 out of 3 consecutive M frames have errors in the M bit positions in DS3 mode. This bit is set when four consecutive FAS errors have been received in E3 mode. This condition will initiate a reframe.

LOSAlm Loss-Of-Signal Alarm—Indicates that the received signal prior to B3ZS/HDB3 decoding has been low for 175 ± 75 clock cycles. This indicates that the DS3/E3 line signal has been lost. This signal is set as soon as the loss-of-signal condition is detected and is cleared when at least 33 percent (25 percent in E3 mode) one's density is achieved for 175 ± 75 clock cycles

0x11—Counter Interrupt Status Register (SR01)

The Counter Interrupt Status Register contains status information about active interrupts needing service from the controller. This register needs to be read by the controller upon receiving a counter interrupt to determine the source of the interrupt. The interrupt indications are active high in the register and are available even if they are not enabled to be visible on the CNTINT/LINELB output pin. Servicing will clear this interrupt indication as described in Microprocessor Interrupts in the Microprocessor Interface section in the Functional Description chapter. Counter operation is discussed in DS3/E3 Error Counters in the Status Registers section of this chapter.

NOTE(S): Rsvd bits in Control Registers must be set to zero.

7	6	5	4	3	2	1	0
Rsvd	ShdwItr	LCVCtrItr	FEBECtrItr	PthCtrItr	FerrCtrItr	DgrCtrItr	ParCtrlItr

ShdwItr Shadow Status Register Interrupt—Set if any of the bits in the Shadow Status Register get set. This bit is cleared by reading the Shadow Status Register [SR06;0x16].

LCVCtrItr LCV Counter Interrupt—Set high on an LCV error counter roll-over or saturation. The LCV Counter Interrupt Enable bit [LCVCtrIE;CR02.5] determines the status of the counter. This bit is cleared when this status register is read.

FEBECtrItr FEBE Event Counter Interrupt—Set high if the FEBE event counter has either rolled over or is saturated. The FEBE Event Counter Interrupt Enable [FEBECtrIE;CR02.4] determines the status of the counter. This bit is cleared when this status register is read.

PthCtrItr Path Parity Error Counter Interrupt—Set high if the path parity error counter has either rolled over or is saturated. The Parity Error Counter Interrupt Enable bit [PthCtrIE.CR02.3] determines the status of the counter. This bit is cleared when this status register is read.

FerrCtrItr Frame Error Counter Interrupt—Set high when the frame error counter has either rolled over or is saturated. The Frame Error Counter Interrupt Enable [FerrCtrIE;CR02.2] determines the status of the counter. This bit is cleared when this status register is read.

DgrCtrItr Disagreement Counter Interrupt—Set high if the disagreement counters have either rolled over or are saturated. The Disagreement Counter Interrupt Enable bit [DgrCtrIE;CR02.1] determines the status of the counter. This bit is cleared when this status register is read.

ParCtrItr Parity Error Counter Interrupt—Set high if the parity error counter has either rolled over or is saturated. The Parity Error Counter Interrupt Enable bit [ParCtrIE;CR02.0] determines the status of the counter. This bit is cleared when this status register is read.

0x12—Data Link Interrupt Status Register (SR02)

The Data Link Interrupt Status Register contains information about active data link interrupts needing service from the controller. The controller determines the source of the data link interrupt by reading this register. The interrupt indications are active high and can be from four sources: Transmit FEAC Channel, Receive FEAC Channel, Transmit Terminal Data Link, and Receive Terminal Data Link. Servicing an interrupt clears the indication in this register.

NOTE(S): Rsvd bits in Control Registers must be set to zero.

7	6	5	4	3	2	1	0
Rsvd	Rsvd	Rsvd	Rsvd	TxTDLItr	RxTDLItr	TxFEACItr	RxFEACItr

TxTDLItr Transmit Terminal Data Link Interrupt—Set high when the transmitter has latched the present set of controls in the Terminal Data Link Control Register [CR01; 0x01] and is ready for a new set. Writing the Terminal Data Link Control Register clears this interrupt.

RxTDLItr Receive Terminal Data Link Interrupt—Set high by the Receive Data Link circuitry. Reading the Terminal Data Link Status Register clears this interrupt.

TxFEACItr Transmit FEAC Channel Interrupt—Set high indicating that the transmitter is ready for a new byte to be written to the Transmit FEAC Channel Byte Register. Writing the Transmit FEAC Channel Byte clears this interrupt.

RxFEACItr Receive FEAC Channel Interrupt—Set high when a FEAC message byte has been received and placed in the Receive FEAC Channel Byte Register. Reading the Receive FEAC Channel Byte Register clears this interrupt.

0x13—Receive FEAC Channel Byte (SR03)

7	6	5	4	3	2	1	0
RxFEAC[7]	RxFEAC[6]	RxFEAC[5]	RxFEAC[4]	RxFEAC[3]	RxFEAC[2]	RxFEAC[1]	RxFEAC[0]

RxFEAC[7:0] Receive FEAC Channel Message Byte—If the incoming format is C-bit parity, this register contains the received byte from the bit-oriented receive FEAC channel. The receive FEAC channel is only defined in C-bit parity format. Receive FEAC message reception is described in RxFEAC Channel Reception in the Receiver Operation section of the Functional Description chapter. This byte is meaningless in E3 mode and should be ignored.

0x14—Terminal Data Link Status Register (SR04)

The Terminal Data Link Status Register contains the status indications for the LAPD receiver of the terminal data link. This data link is only defined in C-bit parity or E3 modes. Terminal data link reception is described in the Receiver Operation section of the Functional Description chapter.

Terminal data link receiver functions include FCS checking, transparency bit removal, and flag detection. LAPD messages may be read from the Receive Terminal Data Link Message Buffer [RxTDL;0x40–0x47], and require the use of the DLINT/SOURCELB interrupt to synchronize the transfer of message data between the receiver and microprocessor.

NOTE(S): Reserved bits in Control Registers must be set to zero.

7	6	5	4	3	2	1	0
Reserved	Reserved	RxByte[2]	RxByte[1]	RxByte[0]	RxIdle	BadFCS	RxAbort

RxByte[2:0] Byte Pointer—A 3-bit pointer to the last location written in the Receive Terminal Data Link Message Buffer.

RxIdle Idle Code Received—Indicates that an idle flag sequence (01111110) was received on the terminal data link.

BadFCS Bad FCS—Set when an erroneous FCS was received at the end of a message or an idle flag is received that is not byte aligned.

RxAbort Abort Flag Received—Set if an abort sequence (seven consecutive ones) is received on the terminal data link.

0x15—Part Number/Hardware Version Register (SR05)

The Part Number/Hardware Version Register contains a part number in the upper nibble and a version number in the lower nibble. This register is provided so that the processor will know what version of the CN8330 is present. This enables loading of version-specific software, if needed. The part number for the CN8330 framer is 0000. The version number is indicated below and will be incremented with any change in circuitry within the IC.

7	6	5	4	3	2	1	0
Part[3]	Part[2]	Part[1]	Part[0]	Ver[3]	Ver[2]	Ver[1]	Ver[0]

U

Conexent Part Number	Obsolete Base$_2$ Part Number	Hex Value
CN8330EPJ	UGA-330-1	0x01
CN8330EPJB	UGA-330-2	0x02
CN8330EPJC/CN8330EPFC	—	0x03
CN8330EPJD/CN8330EPFD	—	0x04

0x16—Shadow Status Register (SR06)

The Shadow Status Register contains copies of the five least significant bits of the DS3/E3 Maintenance Status Register [SR00;0x10]. Whenever a status indication appears in the DS3/E3 Maintenance Status Register, the corresponding bit is also set in the Shadow Status Register. The bits in this Shadow Status Register are latched and held until the controller reads the register. This register provides a way to monitor transient occurrences of alarm indications without continuously polling the DS3/E3 Maintenance Status Register. An additional bit not contained in the DS3/E3 Maintenance Status Register is All-Ones Detect. If the shadow interrupt is enabled, any occurrence of an indication in bits 0 through 4 will cause an active low interrupt to occur on the CNTINT/LINELB pin.

NOTE(S): Rsvd bits in Control Registers must be set to zero.

7	6	5	4	3	2	1	0
Rsvd	Rsvd	ShdwAll1	ShdwIdle	ShdwYel	ShdwAIS	ShdwOOF	ShdwLOS

ShdwAll1 Shadow All-Ones Detect—Set whenever an unframed all-ones signal has been detected in either DS3 or E3 mode.

ShdwIdle Shadow Idle Code Detect—Set if there is valid framing and parity, the three C-bits in subframe 3 are zero, both X-bits are equal, and the payload contains a 1100... pattern starting with a 11 after each overhead bit in DS3 mode. This bit will be low in E3 mode since there is no defined E3 idle signal.

ShdwYel Shadow Yellow Alarm Detect—Set for one M-frame interval when both X-bits are low in the previous M-frame in DS3 mode. This bit is set when the received A-bit is high in E3 mode.

ShdwAIS Shadow Alarm Indication Signal Detect—Set if there is valid framing and parity, all C-bits are 0, both X-bits are equal, and the payload contains a 1010... pattern starting with a one after each overhead bit in DS3 mode. This bit is set when an unframed all-ones signal is received in E3 mode.

ShdwOOF Shadow Out of Frame—Set when any 3 out of 16 consecutive F framing bits are in error or when 2 out of 3 consecutive M-frames have errors in the M-bit positions in DS3 mode. This bit is set when four consecutive FAS errors have been received in E3 mode. This condition will initiate a reframe.

ShdwLOS Shadow Loss-of-Signal Alarm—Indicates that the received signal prior to B3ZS/HDB3 decoding has been low for 175 ± 75 clock cycles. This indicates that the CN8330 line signal has been lost. This signal is set as soon as the loss-of-signal condition is detected and is cleared when at least 33percent (25 percent in E3 mode) one's density is achieved for 175 ± 75 clock cycles.

0x20–0x26—DS3/E3 Error Counters

There are six error counters for DS3/E3 errors located at addresses 0x20–0x26. All are 8-bit counters with the exception of the DS3 Disagreement [SR08;0x21] and DS3/E3 LCV Counters [SR12,SR13;0x25,0x26]. The 8-bit counters indicate 0 through 255 counts of a particular error. If the interrupt for a particular counter is not enabled, the counter will saturate at 255 when more than 255 counts of that error are received and the saturation indication will appear in the Counter Interrupt Status Register [SR01;0x01]. The saturation indication and the counter will be cleared when the counter is read. If the interrupt for a particular counter is enabled in the Interrupt Control Register [CR02; 0x02], then the counter will not saturate but will roll over and continue counting from zero. An interrupt will be generated on the CNTINT/LINELB output pin and will appear in the Counter Interrupt Status Register when the counter rolls over to a count of zero. The interrupt will be cleared when the Counter Interrupt Status Register is read.

The only valid counters in E3 mode are the DS3/E3 LCV and Frame Error Counters. The DS3/E3 Frame Error Counter [SR09;0x22] counts each occurrence of an incorrect pattern in the 10-bit FAS.

All counters are cleared when read by the microprocessor. The interrupt indication for a particular counter is also cleared when the counter is read. Both nibbles of the DS3 Disagreement Counter [SR08;0x21] are cleared when address 0x21 is read. Each byte of the DS3/E3 LCV Counter is cleared separately when it is read. Software should read the low byte first and then the high byte to prevent any missed counts. All counters are designed so that errors occurring during reads by the microprocessor will not be missed or double-counted. All counters except for LCV and Frame Error are frozen during an OOF condition. The LCV and Frame Error Counters continue counting errors during an OOF condition. Both counters also have ripple carry outputs available when the PPDL port is not in use. These outputs are on the RDAT[5] and IDLE pins, respectively. Saturation of these two counters can be disabled without enabling the respective interrupts by setting the Disable Saturation of LCV/Frame Errors bit [DisLCV/Ferr;CR04.4] in the Feature Control Register [CR04;0x04]. This allows external enlargement of these counters by use of the ripple carry outputs without interruption of the microprocessor.

0x20—DS3 Parity Error Counter (SR07)

7	6	5	4	3	2	1	0
DS3ParCtr[7]	DS3ParCtr[6]	DS3ParCtr[5]	DS3ParCtr[4]	DS3ParCtr[3]	DS3ParCtr[2]	DS3ParCtr[1]	DS3ParCtr[0]

DS3ParCtr[7:0] DS3 Parity Error Counter—Increments for each M-frame in which the calculated parity of the received data bits of the previous M-frame do not match the received parity bits. If the two parity bits are different this counter will increment.

0x21—DS3 Disagreement Counter (SR08)

The DS3 Disagreement Counter consists of two 4-bit counters. Both counters indicate 0 through 15 counts of disagreements in either the two X (yellow alarm) bits or the two P (parity) bits. If the interrupt is not enabled, the counters saturate at 15 when more than 15 counts are received. Saturation of either 4-bit counter will generate a disagreement counter interrupt indication in Counter Interrupt Status Register [SR01;0x11]. If the disagreement interrupt is enabled, the counters will roll over and continue counting after 15 error counts and generate an interrupt in Counter Interrupt Status Register and on the CNTINT/LINELB pin.

7	6	5	4	3	2	1	0
ParDgrCtr[3]	ParDgrCtr[2]	ParDgrCtr[1]	ParDgrCtr[0]	XDgrCtr[3]	XDgrCtr[2]	XDgrCtr[1]	XDgrCtr[0]

ParDgrCtr[3:0] Parity-Bit Disagreement Counter—If the two P-bits in an M-frame are in disagreement, the P-bit disagreement counter nibble will be incremented.

XDgrCtr[3:0] X-Bit Disagreement Counter—If the two X-bits in an M-frame are in disagreement (due to line errors), the X-bit disagreement counter nibble will be incremented.

0x22—DS3/E3 Frame Error Counter (SR09)

7	6	5	4	3	2	1	0
FerrCtr[7]	FerrCtr[6]	FerrCtr[5]	FerrCtr[4]	FerrCtr[3]	FerrCtr[2]	FerrCtr[1]	FerrCtr[0]

FerrCtr[7:0] Frame Error Counter—Increments with each error in the M- or F-bit framing pattern in DS3 mode and with each error in the FAS pattern in E3 mode. Errors are still counted during an OOF condition (OOFAlm = 1).

0x23—DS3 Path Parity Error Counter (SR10)

7	6	5	4	3	2	1	0
DS3PthCtr[7]	DS3PthCtr[6]	DS3PthCtr[5]	DS3PthCtr[4]	DS3PthCtr[3]	DS3PthCtr[2]	DS3PthCtr[1]	DS3PthCtr[0]

DS3PthCtr[7:0] DS3 Path Parity Error Counter—Increments for each M-frame in which the calculated parity of the received data bits of the previous M-frame do not match a majority vote of the three received CP bits (C-bits in subframe 30).

0x24—DS3 FEBE Event Counter (SR11)

7	6	5	4	3	2	1	0
DS3FEBE[7]	DS3FEBE[6]	DS3FEBE[5]	DS3FEBE[4]	DS3FEBE[3]	DS3FEBE[2]	DS3FEBE[1]	DS3FEBE[0]

DS3FEBE[7:0] DS3 FEBE Event Counter— Increments for each M-frame where any C-bit in subframe 4 is zero.

0x25,0x26—DS3/E3 LCV Counter—Low and High Bytes (SR12,SR13)

The DS3/E3 LCV Counter is a 16-bit counter with the low byte located at address 0x25 and the high byte located at address 0x26. If the interrupt for the DS3/E3 LCV Counter is not enabled, the counter will saturate at 65535 and the saturation indication will appear in the Counter Interrupt Status Register [SR01;0x11]. If the interrupt is enabled, the counter will roll over and continue counting as for the 8-bit counters. In DS3 mode, this counter increments upon each occurrence of a Bipolar Violation (BPV) and each sequence of three or more zeroes. In E3 mode, it increments only upon each occurrence of an LCV per ITU-T O.161 (an LCV is defined as two consecutive BPVs of the same polarity).

7	6	5	4	3	2	1	0
LCVCtr[7]	LCVCtr[6]	LCVCtr[5]	LCVCtr[4]	LCVCtr[3]	LCVCtr[2]	LCVCtr[1]	LCVCtr[0]

15	14	13	12	11	10	9	8
LCVCtr[15]	LCVCtr[14]	LCVCtr[13]	LCVCtr[12]	LCVCtr[11]	LCVCtr[10]	LCVCtr[9]	LCVCtr[8]

3.3 Memory Registers

0x30–0x37—Transmit Terminal Data Link Message Buffer (TxTDL)

The Transmit Terminal Data Link Message Buffer locations are loaded with the message bytes to be sent on the terminal data link in response to the Transmit Terminal Data Link Interrupt.

7	6	5	4	3	2	1	0
TxTDL[7]	TxTDL[6]	TxTDL[5]	TxTDL[4]	TxTDL[3]	TxTDL[2]	TxTDL[1]	TxTDL[0]

0x40–0x47—Receive Terminal Data Link Message Buffer (RxTDL)

The Receive Terminal Data Link Message Buffer contains the message bytes received on the terminal data link. The Receive Terminal Data Link Interrupt indicates the presence of data in the receive buffer.

7	6	5	4	3	2	1	0
RxTDL[7]	RxTDL[6]	RxTDL[5]	RxTDL[4]	RxTDL[3]	RxTDL[2]	RxTDL[1]	RxTDL[0]

3.4 Register Summary

Table 3-1. Register Overview

ADDR	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0x00	CR00	R/W	LineLp	SourceLp	TxAlm1	TxAlm0	ExtOvh	ExtCBit	E3Frm	CBitP/DL
0x01	CR01	R/W	RxTDLIE	DisTxTDL	TxByte[2]	TxByte[1]	TxByte[0]	TxAbort	TxFCS	TxMsg
0x02	CR02	R/W	SR6IE	RxFEACIE	LCVCtrIE	FEBECtrIE	PthCtrIE	FerrCtrIE	DgrCtrIE	ParCtrIE
0x03	CR03	R/W	TxFEAC[7]	TxFEAC[6]	TxFEAC[5]	TxFEAC[4]	TxFEAC[3]	TxFEAC[2]	TxFEAC[1]	TxFEAC[0]
0x04	CR04	R/W	TstEqSel	AMI/LCV2	DisEnc	DisLCV/Ferr	ParaEn	FEBEC[3]	FEBEC[2]	FEBEC[1]
0x05	CR05	R/W	FCSCnt[3]	FCSCnt[2]	FCSCnt[1]	FCSCnt[0]	LimitFCS	CRC32	DisPPDL	Nibble

Table 3-2. Status Registers *(1 of 2)*

ADDR	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0x10	SR00	R	ReFrm	FmtID1	FmtID0	IdleDet	YelDet	AISDet	OOFAlm	LOSAlm
0x11	SR01	R	Rsvd	ShdwItr	LCVCtrItr	FEBECtrItr	PthCtrItr	FerrCtrItr	DgrCtrItr	ParCtrItr
0x12	SR02	R	Rsvd	Rsvd	Rsvd	Rsvd	TxTDLItr	RxTDLItr	TxFEACItr	RxFEACItr
0x13	SR03	R	RxFEAC[7]	RxFEAC[6]	RxFEAC[5]	RxFEAC[4]	RxFEAC[3]	RxFEAC[2]	RxFEAC[1]	RxFEAC[0]
0x14	SR04	R	Rsvd	Rsvd	RxByte[2]	RxByte[1]	RxByte[0]	RxIdle	BadFCS	RxAbort
0x15	SR05	R	Part[3]	Part[2]	Part[1]	Part[0]	Ver[3]	Ver[2]	Ver[1]	Ver[0]
0x16	SR06	R	Rsvd	Rsvd	ShdwAll1	ShdwIdle	ShdwYel	ShdwAIS	ShdwOOF	ShdwLOS
0x20	SR07	R	DS3 ParCtr[7]	DS3ParCtr[6]	DS3ParCtr[5]	DS3ParCtr[4]	DS3ParCtr[3]	DS3ParCtr[2]	DS3ParCtr[1]	DS3ParCtr[0]

Table 3-2. Status Registers *(2 of 2)*

ADDR	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0x21	SR08	R	ParDgrCtr[3]	ParDgrCtr[2]	ParDgrCtr[1]	ParDgrCtr[0]	XDgrCtr[3]	XDgrCtr[2]	XDgrCtr[1]	XDgrCtr[0]
0x22	SR09	R	FerrCtr[7]	FerrCtr[6]	FerrCtr[5]	FerrCtr[4]	FerrCtr[3]	FerrCtr[2]	FerrCtr[1]	FerrCtr[0]
0x23	SR10	R	DS3PthCtr[7]	DS3PthCtr[6]	DS3PthCtr[5]	DS3PthCtr[4]	DS3PthCtr[3]	DS3PthCtr[2]	DS3PthCtr[1]	DS3PthCtr[0]
0x24	SR11	R	DS3FEBE[7]	DS3FEBE[6]	DS3FEBE[5]	DS3FEBE[4]	DS3FEBE[3]	DS3FEBE[2]	DS3FEBE[1]	DS3FEBE[0]
0x25	SR12	R	LCVCtr[7]	LCVCtr[6]	LCVCtr[5]	LCVCtr[4]	LCVCtr[3]	LCVCtr[2]	LCVCtr[1]	LCVCtr[0]
0x26	SR13	R	LCVCtr[15]	LCVCtr[14]	LCVCtr[13]	LCVCtr[12]	LCVCtr[11]	LCVCtr[10]	LCVCtr[9]	LCVCtr[8]

Table 3-3. Transmit Terminal Data Link Message Buffer

ADDR	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0x30–0x37	TxTdl	R/W	TxTDL[7]	TxTDL[6]	TxTDL[5]	TxTDL[4]	TxTDL[3]	TxTDL[2]	TxTDL[1]	TxTDL[0]

Table 3-4. Receive Terminal Data Link Message Buffer

ADDR	Register Label	Read Write	Bit Number							
			7	6	5	4	3	2	1	0
0x40–0x47	RxTdl	R/W	RxTDL[7]	RxTDL[6]	RxTDL[5]	RxTDL[4]	RxTDL[3]	RxTDL[2]	RxTDL[1]	RxTDL[0]

4.0 Mechanical/Electrical Specifications

4.1 Timing Requirements

Table 4-1 and Figure 4-1 illustrate the timing requirements for the microprocessor interface. The parameter t_{cyc} is the period of the receive DS3/E3 clock (DS3CKI). This clock signal is used in the read circuit of the microprocessor to ensuring no status events are missed and that counter values are accurately read.

Read operation requires the read strobe to be low for three t_{cyc} clock cycles ensuring that changing status and error counts are properly processed. If a gapped clock is applied to the circuit, it is sufficient to allow three receive clock cycles between read strobes to allow a latching circuit to clear in the microprocessor interface.

Table 4-1. Microprocessor Interface Timing *(1 of 2)*

Symbol	Parameter	Min.	Typical	Max.	Units
t_{as}	Address Setup before ALE Low	7	—	—	ns
t_{cale}	Controller ALE Pulse Width	34	—	—	ns
t_{ah}	Address Hold after ALE Low	10	—	—	ns
t_{rwa}	RD*/WR* High to ALE High	10	—	—	ns
t_{adwrh}	Address/Select to WR* High	117	—	—	ns
t_{adrdl}	Address/Select to RD* Low	17	—	—	ns
t_{wrw} (Read Operation)	RD* Pulse Width(1)	3 × t_{cyc}	—	—	ns
t_{wrw} (Write Operation)	WR* Pulse Width	100	—	—	ns
t_{rdd}	RD* Low to Data Available	—	—	30	ns
t_{rdh}	Read Data Hold Time(2)	3	—	—	ns

Table 4-1. Microprocessor Interface Timing *(2 of 2)*

Symbol	Parameter	Min.	Typical	Max.	Units
t_{clcl}	ALE Low to RD*/WR* Low	10	—	—	ns
t_{ds}	Data Stable Before WR* High	25	—	—	ns
t_{dh}	Data Hold after WR* High	10	—	—	ns
t_{sh}	Address/Select Hold after RD*/WR* Low	110	—	—	ns
—	Controller Port Cycle Time	154	—	—	ns

NOTE(S):
(1) T_{cyc} = Period of clock connected to the DS3CKI pin.
(2) The external address/data bus capacitance will increase the data hold time if the bus remains undriven.

Figure 4-1. Microprocessor Interface Timing

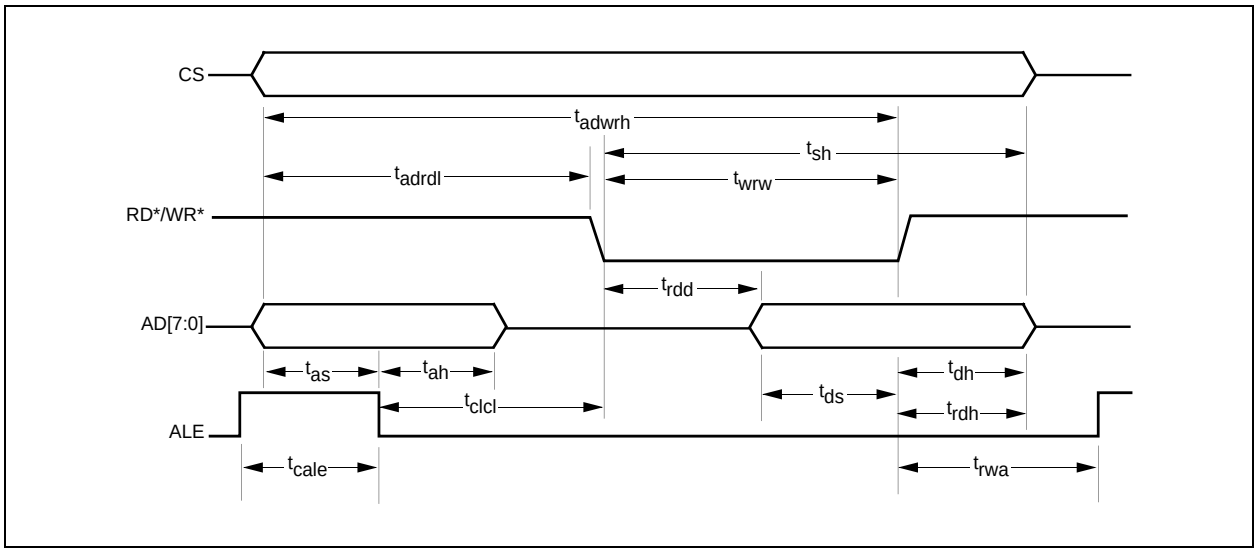


Figure 4-2 and Tables 4-2 through Table 4-4 illustrate the clock and data relationships for all output and input signals. Propagation delays for the output signals are listed below. The output signal timings are relative to the listed edge of the clock. Clock outputs derived from clock inputs are listed with the edge as both. This means that the delay number given applies for either edge. Input signals should have setup and hold times with respect to the listed edge of the given input clock. All times are listed in nanoseconds and are measured with 30 pF loading on the output pins.

Table 4-2. Clock Timing Requirements

Timing Requirements	Clock	Min.	Typical (44.736 MHz)	Typical (34.368 MHz)	Units
Low Pulse Width - ρ_{wl}	RXCKI, DS3CKI, TXCKI	5.0	11.2	14.55	ns
High Pulse Width - ρ_{wh}	RXCKI, DS3CKI, TXCKI	5.0	11.2	14.55	ns
Cycle Time - t_{cyc}	RXCKI, DS3CKI, TXCKI	19.0	22.4	29.1	ns
Cycle Time	—	—	8 RXCKI		ns
Low Pulse Width	RXBCK	6 RXCKI	—	—	ns
High Pulse Width	RXBCK	2 RXCKI	—	—	ns

Figure 4-2. Output and Input Signal Timing

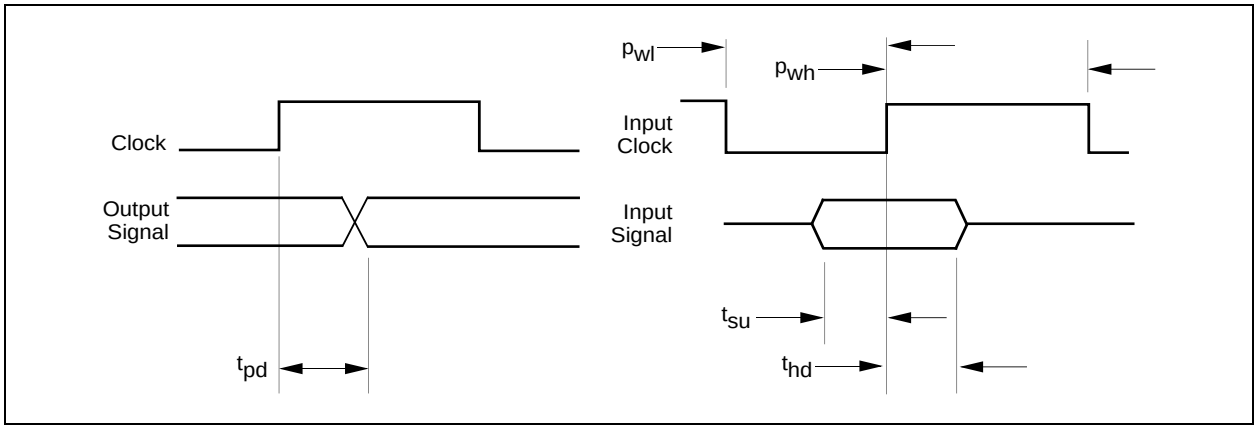


Table 4-3. Output Signal Timing

Output Symbol	Clock	t_{pd} min	t_{pd} max	Edge	Units
RXCLK	DS3CKI/RXCKI	2.8	13.0	Rising	ns
RXMSY	RXCLK	1.8	5.0	Rising	ns
RXDAT	RXCLK	1.6	5.2	Rising	ns
RXCCK	RXCLK	3.2	9.1	Rising	ns
CBITO	RXCCK	t_{cyc}+1.0	t_{cyc}+2.0	Rising	ns
RXOVH	RXCLK	2.5	11.1	Rising	ns
RXBCK	RXCLK	2.0	10.0	Falling	ns
RXGAPCK	DS3CKI/RXCKI	2.8	22.0	Both	ns
RXGAPCK	RXCLK	1.0	9.0	Both	ns
RDAT[7] /TXNRZ	TCLKO	1.2	7.0	Rising	ns
TXPOS/TXNEG	TCLKO	1.2	8.2	Rising	ns
TXSYO	TXCKI	3.2	11.1	Rising	ns
TXGAPCK	TXCKI	2.2	11.7	Both	ns
TXBCK	TXCKI	3.0	16.0	Rising	ns
TCLKO	TXCKI	2.8	12.8	Rising	ns
TXOVH	TXCKI	3.4	15.6	Falling	ns

Table 4-4. Input Setup/Hold Timing

Input Symbol	Clock	t_{su} min	t_{hld} min	Edge	Units
CBITI	TXCCK	2 × t_{cyc}	4 × t_{cyc}	Falling	ns
TDAT[7:0] (Parallel Mode)	TXBCK	–2 × t_{cyc}	Full TXBCK Period	Rising	ns
SNDMSG,SNDFCS	TXBCK	–2 × t_{cyc}	Full TXBCK Period	Rising	ns
TXSYI	TXCKI	1.0	6.0	Rising	ns
TXDATI	TXCKI	1.0	6.0	Falling	ns
TXENI	TCLKO	9.0	0.0	Rising	ns
LCVERRI	TCLKO	9.0	0.0	Rising	ns
RXPOS, RXNEG	DS3CKI	1.0	5.0	Rising	ns

4.2 Environmental Conditions

4.2.1 Power Requirements and Temperature Range

Stresses above those listed as Absolute Maximum Ratings (see Table 4-5) may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	–0.3 to +7.0	Volts
Input Voltage	V_{IN}	–0 to V_{DD} +0.3	Volts
Output Voltage	V_{OUT}	–0.3 to V_{DD} +0.3	Volts
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{STG}	–55 to +150	°C
Operating Supply Voltage	V_{DD}	+4.75 to +5.25	Volts
Thermal Impedance	θ_{JA}	68 PLCB	—
Thermal Impedance	θ_{JA}	80 TOFP	—

4.3 Electrical Characteristics

4.3.1 DC Characteristics

All inputs and bidirectional signals have input thresholds compatible with TTL drive levels. All outputs are CMOS drive levels and can be used with CMOS or TTL logic (see Table 4-6 and Table 4-7). Specific characteristics given in Table 4-6 and Table 4-7 apply over an operating temperature range of –40° to +85°C and a supply voltage range of 4.75 to 5.25 volts, unless otherwise noted.

Table 4-6. DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage	—	4.75	5.00	5.25	V
V_{OH}	All Outputs, except as noted in Table 4-7	I_{OH} = – 4 mA	2.4	4.5	—	V
V_{OL}	All Outputs, except as noted in Table 4-7	I_{OL} = 4 mA	—	0.2	0.4	V
V_{IH}(1)	Input Voltage High	—	2.0	—	—	V
V_{IL}	Input Voltage Low	—	—	—	0.8	V
I_{DD}	Supply Current	V_{DD} = 5.25 V @ 52 MHz	—	—	175	mA
I_{DD}	Supply Current	V_{DD} = 5.25 V @ 45 MHz	—	—	150	mA
I_{IL}	Input Leakage Current	—	—	±1.0	±10	µA
C_{IN}	Input Capacitance	Inputs and AD[7:0]	—	—	3	pF
C_{OUT}	Output Capacitance	All Outputs	—	—	10	pF
—	ESD Protection	MIL-STD-883C Method 3015	2	>3	—	kV
—	Latch-up Input Current	JEDEC JC-40.2	150	>400	—	mA

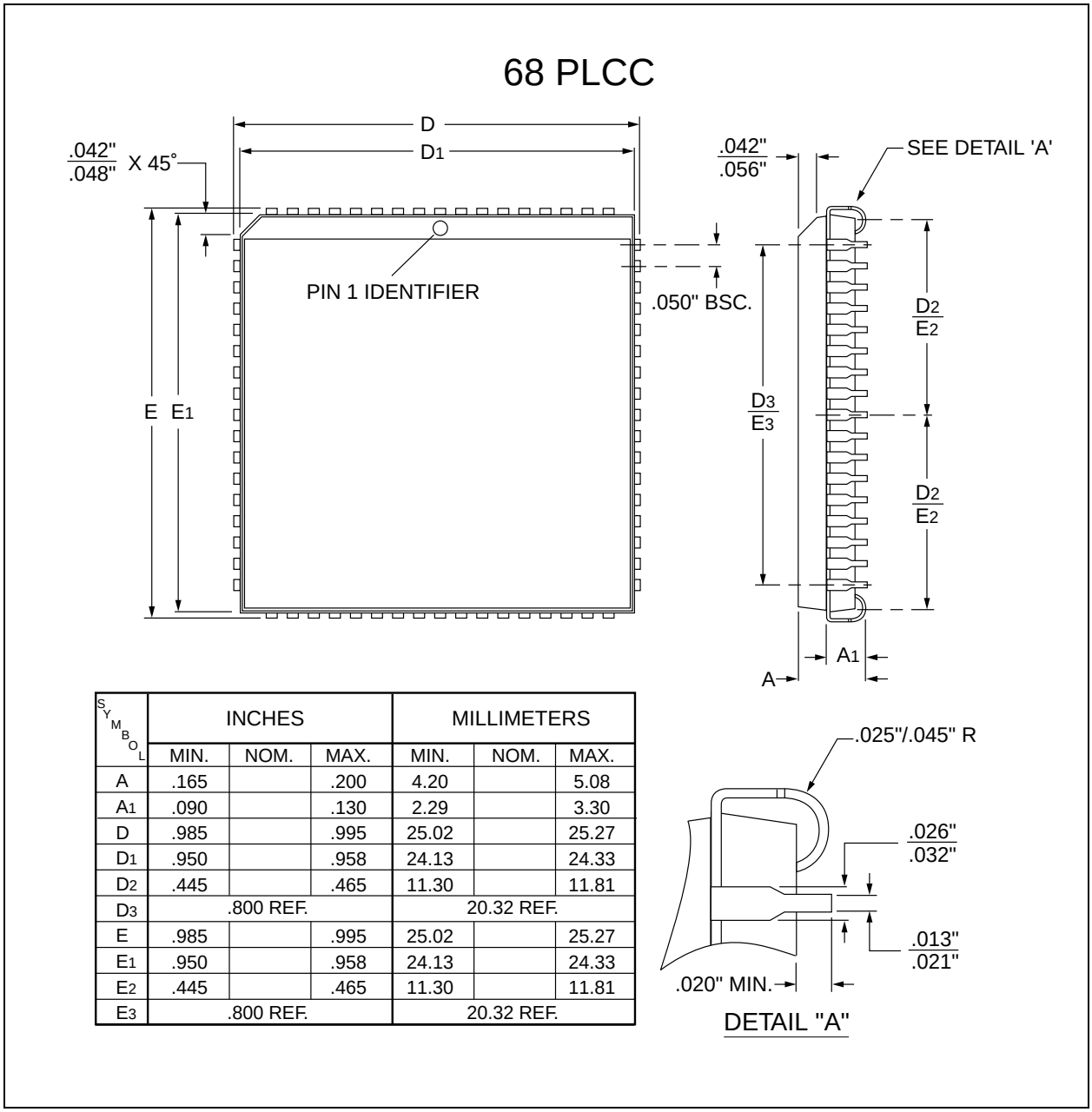
NOTE(S):
(1) Following pins need slightly higher VIH input voltage than specified: TXCKI = 2.2V, INIT_N = 2.1 V

Table 4-7. Output Drive Capability

Output	Pin	Drive Current @ V_{OH} or V_{OL}
RXCLK	22	±8 mA
IDLE	24	±2 mA
VALFCS	25	±8 mA
RDAT[5, 3, 2, 1, 0]	32, 30, 29, 28, 27	±2 mA
CBITO	37	±2 mA
RXCCK	38	±2 mA
TESTO	41	±2 mA
TXCCK	46	±2 mA
TXBCK	57	±8 mA
CNTINT	62	±2 mA
DLINT	63	±2 mA

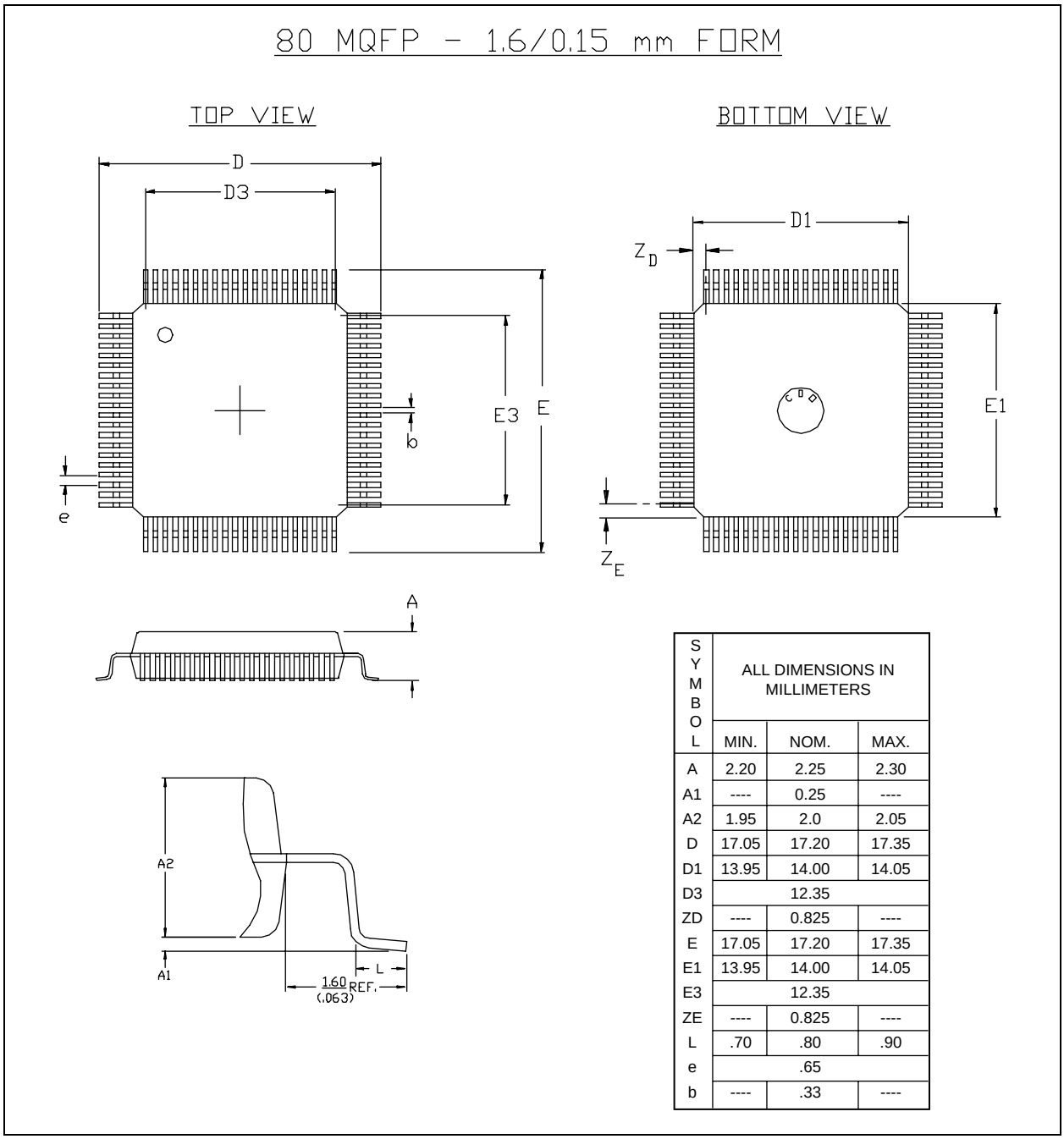
4.4 Mechanical Specifications

Figure 4-3. 68–Pin Plastic Leaded Chip Carrier (J-Bend)



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.165		.200	4.20		5.08
A1	.090		.130	2.29		3.30
D	.985		.995	25.02		25.27
D1	.950		.958	24.13		24.33
D2	.445		.465	11.30		11.81
D3	.800 REF.			20.32 REF.		
E	.985		.995	25.02		25.27
E1	.950		.958	24.13		24.33
E2	.445		.465	11.30		11.81
E3	.800 REF.			20.32 REF.		

Figure 4-4. 80-Pin Metric Quad Flat Pack (MQFP)



SYMBOL	ALL DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.25	2.30
A1	----	0.25	----
A2	1.95	2.0	2.05
D	17.05	17.20	17.35
D1	13.95	14.00	14.05
D3		12.35	
ZD	----	0.825	----
E	17.05	17.20	17.35
E1	13.95	14.00	14.05
E3		12.35	
ZE	----	0.825	----
L	.70	.80	.90
e		.65	
b	----	.33	----

Appendix A Multimegabit HDLC Formatter

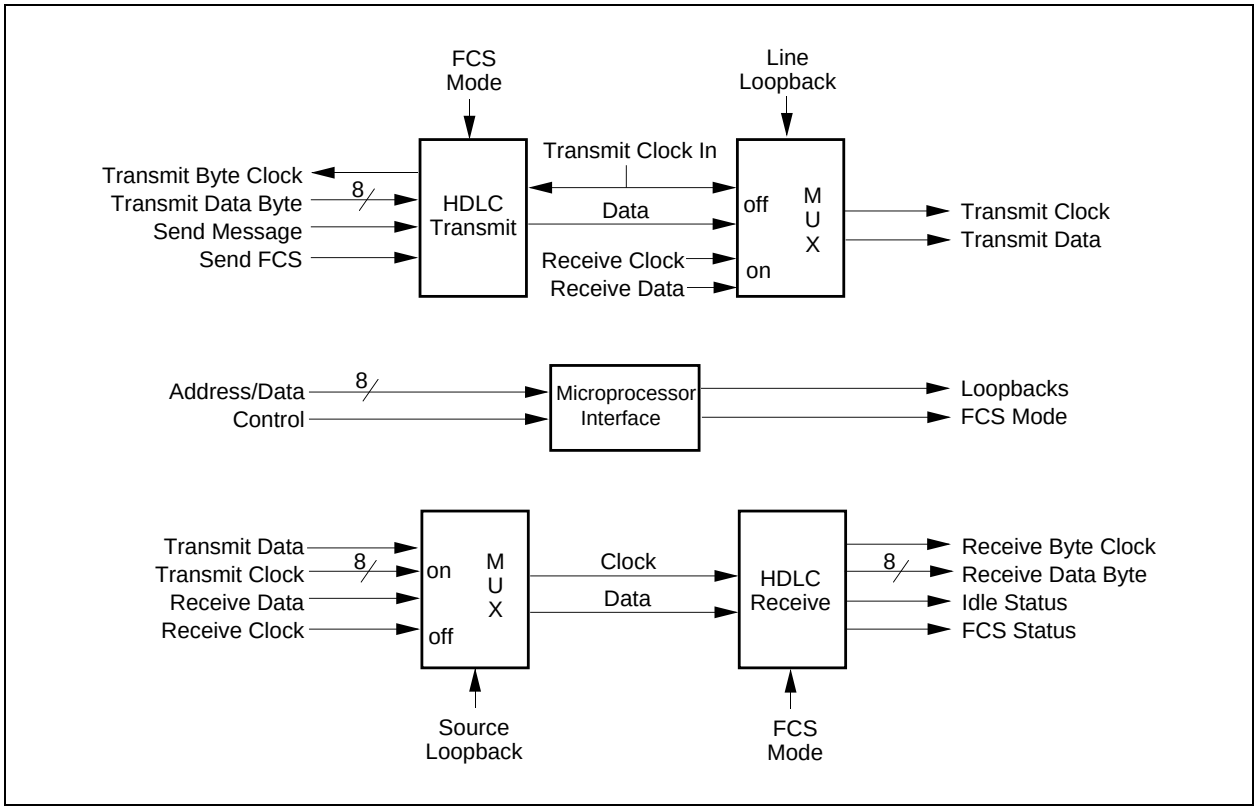
A.1 Introduction

The CN8330 was designed as a DS3/E3 framer with both serial and parallel data inputs. The circuit has an integral High-Level Data Link Control (HDLC) interface that can be used without the insertion of DS3/E3 overhead bits. This mode of operation is documented in this Appendix.

The transmitter is capable of formatting byte-organized data from the Payload Parallel Data Link (PPDL) data port. The parallel data is formatted with idle flags, zero stuffing for transparency, and a selectable 16- or 32-bit Frame Check Sequence (FCS) according to ITU-T standard Q.921 or ISO 3309-1984. Options are provided to allow the formatting of data for packet voice according to ANSI standard T1.312-1991. Serial data can be transmitted at any rate up to 52 Mbps.

The receiver provides complementary operation, deriving byte-organized data and HDLC protocol status including FCS checking at serial rates up to 52 Mbps. Figure A-1 illustrates the major data paths of the HDLC formatter.

Figure A-1. HDLC Formatter Block Diagram



A.2 Block and Logic Diagrams

The transmit serial clock is applied to the TXCKI input of the HDLC transmitter. The circuit generates a byte clock and either idle code, a serialized message byte, an FCS sequence, or an abort sequence on the RXCCK/TXNRZ output pin in response to control signal inputs. At the end of a message, the FCS is generated. Either a 16- or 32-bit Cycle Redundancy Check (CRC) can be generated for the FCS. A line loopback function that will loop the receive input directly to the transmit output for end-to-end loopback is provided.

In the receive direction, serial data is taken from the receiver inputs RXPOS and RXNEG, or, if source loopback is set, from the transmitter output. The serial clock is connected to the DS3CKI pin on the HDLC receiver. The receiver derives bytes of data, a byte clock, idle channel, and valid FCS indications from the received serial data. The source loopback function can be used to provide a diagnostic test of the HDLC transmitter and receiver.

A microprocessor interface is required to configure the circuit for HDLC operation and to control loopbacks and FCS options for the HDLC transmitter and receiver. The control pins consist of the read and write strobes and a chip select signal.

Figure A-2 is a logic diagram showing the functional partitioning of the pins. This diagram pertains only to HDLC mode operation, for which some of the pins are reassigned from CN8330 framer functions, i.e., the transmit data output comes from a pin (RXCCK/TXNRZ) assigned to the receiver in CN8330 framer operation.

Figure A-2. HDLC Formatter Logic Diagram

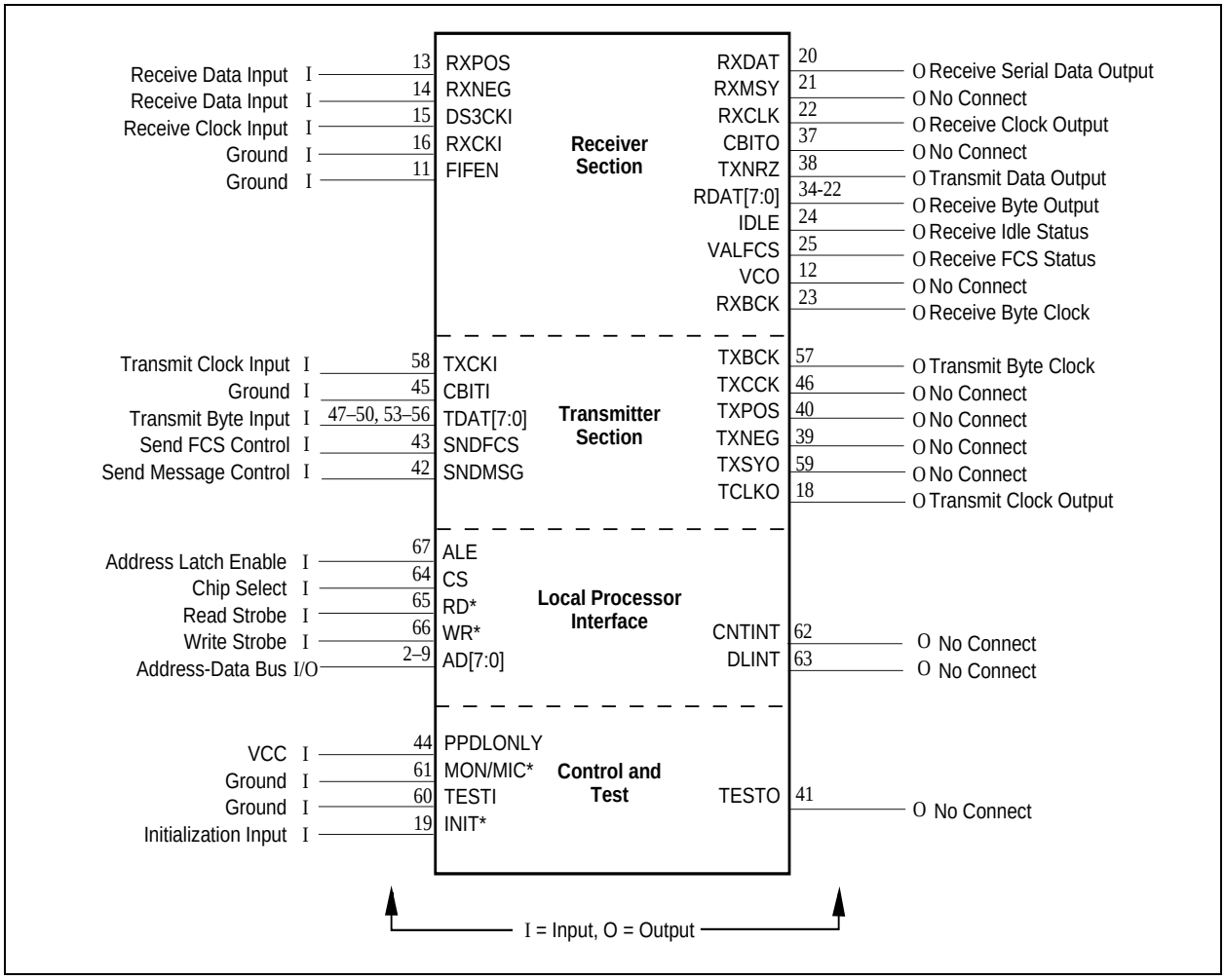
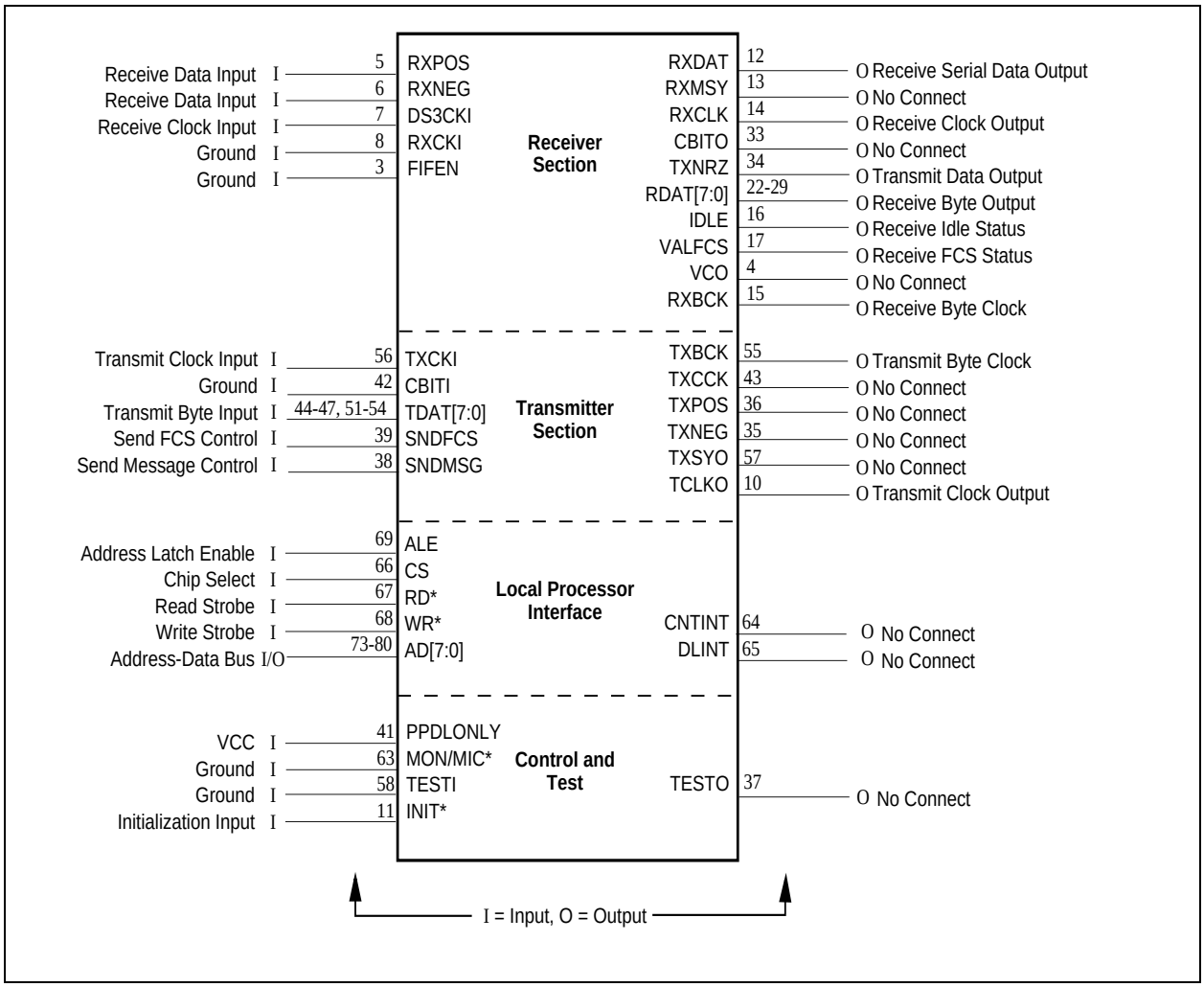


Figure A-3. HDLC Formatter Logic Diagram - 80-Pin MQFP



A.3 PPDL Transmitter

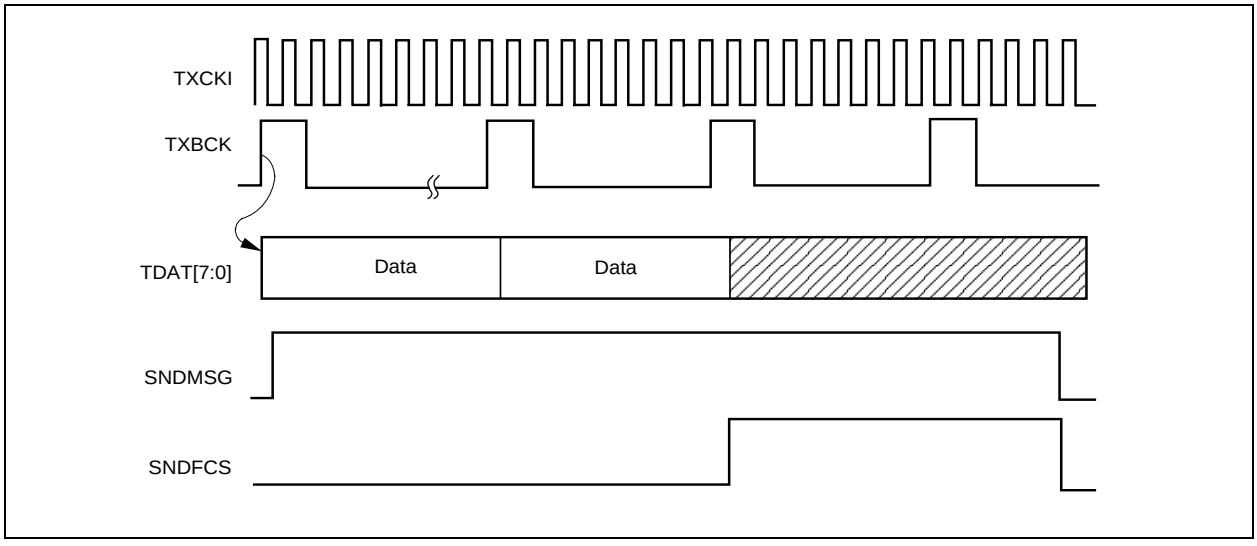
The PPDL transmitter is enabled by setting the Parallel Data Enable bit [ParaEn; CR04.3] in the Feature Control Register [CR04;0x04]. The PPDL formatter is controlled by signals applied on the SNDMSG and SNDFCS pins. Byte-wide data is provided on the TDAT[7:0]. Optional HDLC formatting with 16-bit or 32-bit FCSs are provided.

Transmitter operation is controlled by the SNDMSG and SNDFCS pins. If no message is in progress (SNDMSG and SNDFCS both low), idle flags (01111110) are continuously transmitted in the data stream. Setting SNDMSG high initiates message transmission. Data bytes and control signals are provided in response to the rising edge of the transmit byte clock TXBCK and are sampled internally after the falling edge. The data and controls should be held for a full period of TXBCK. The least significant bit of the transmitted bytes is applied to TDAT[0] and the most significant to TDAT[7]; transmission is least significant bit first. The transmitter performs automatic zero stuffing for transparency and FCS calculation for the data. The message must be an integral number of bytes in length. The FCS is 16 or 32 bits in length depending on the setting of the 32-bit CRC Select control bit [CRC32;CR05.2] in the PPDL Control Register [CR05;0x05]. If this bit is low, the FCS is calculated with the polynomial: $x^{16}+x^{12}+x^5+1$. If a 32-bit CRC is selected by setting the CRC32 high, then SNDFCS shown in Figure A-4 must be high for 4 cycles of the transmit byte clock and the FCS is calculated with the polynomial:

$$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1$$

The FCS is transmitted by setting both the SNDMSG and SNDFCS pins high after the last data byte has been transmitted. SNDFCS should be high for 2 byte clocks in 16-bit FCS mode and for 4 byte clocks in 32-bit FCS mode. An abort sequence may be transmitted by setting SNDFCS high while SNDMSG is set low. Timing for the transmit operation is shown in Figure A-4.

Figure A-4. PPDL Transmitter Timing



The transmit byte clock (TXBCK) is generated from the transmit clock input (TXCKI) and has a duty cycle of 25 percent. TXBCK will nominally be one-eighth of the TXCKI frequency but is influenced by HDLC transparency bit insertions. In the absence of any transparency bit insertions, there will be one pulse on TXBCK for every eight clock cycles of the TXCKI input. When a transparency bit is inserted into the serial transmit data stream, the TXBCK period will be lengthened to nine clock cycles of TXCKI (or 10 clock cycles if two transparency bit insertions occur within the same octet interval). TXBCK is present continuously even during the transmission of idle flags. The actual setup times on TDAT[7:0], SNDMSG, and SNDFCS relative to the rising edge of TXBCK are negative. Therefore, it is possible to read data and control from a RAM or FIFO buffer with the rising edge. CN8330 will sample the data after the falling edge. This allows FIFOs or RAMs with access times of 35–40 ns to be used.

FCS calculation can be limited to the first N bytes of the transmitted message by setting the Limit Frame Check Sequence Calculation [LimitFCS;cr05.3] control bit. In this mode, the FCS is calculated on the first N bytes transmitted after the opening flag and then held until the end of the message. It is then appended to the end of the message in normal fashion. The desired number N can be from 1 to 16 (a value of 0 gives N = 16) and is loaded in the Frame Check Sequence Calculation Count[3:0] [FCSCnt;CR05.7:4] control field. This allows FCS calculation only on the header information in a T1 packet voice format.

A.3.1 PPDL Receiver

The PPDL receiver circuitry is activated when the ParaEn bit in the Feature Control Register is set. The receiver performs idle flag detection, stuffed zero deletion, and FCS checking on the incoming data stream. The recovered data bytes are presented on RDAT[7:0] and are valid on both the rising and falling edges of RXBCK; the least significant bit is on RDAT[0] and the most significant bit is on RDAT[7]; the least significant bit is the first received from the serial input. If the payload stream contains idle flags, the IDLE pin will be high and the flags will be present on RDAT[7:0]. If a valid FCS is received at the end of the message block, then the VALFCS pin will be active high while IDLE is high. At the start of the next message, both indications will go low until the end of the incoming message has been received. If a bad FCS is received, IDLE will go high and VALFCS will remain low. If VALFCS goes high and IDLE does not, an abort sequence was received in the data. If there is only one flag received between incoming packets, there will be only one RXBCK pulse present while IDLE is high. If CRC 32-bit is low, the FCS is checked with the polynomial:

$$x^{16}+x^{12}+x^{5}+1$$

If a 32-bit CRC is selected by setting CRC32 bit high, then the FCS is checked with the polynomial:

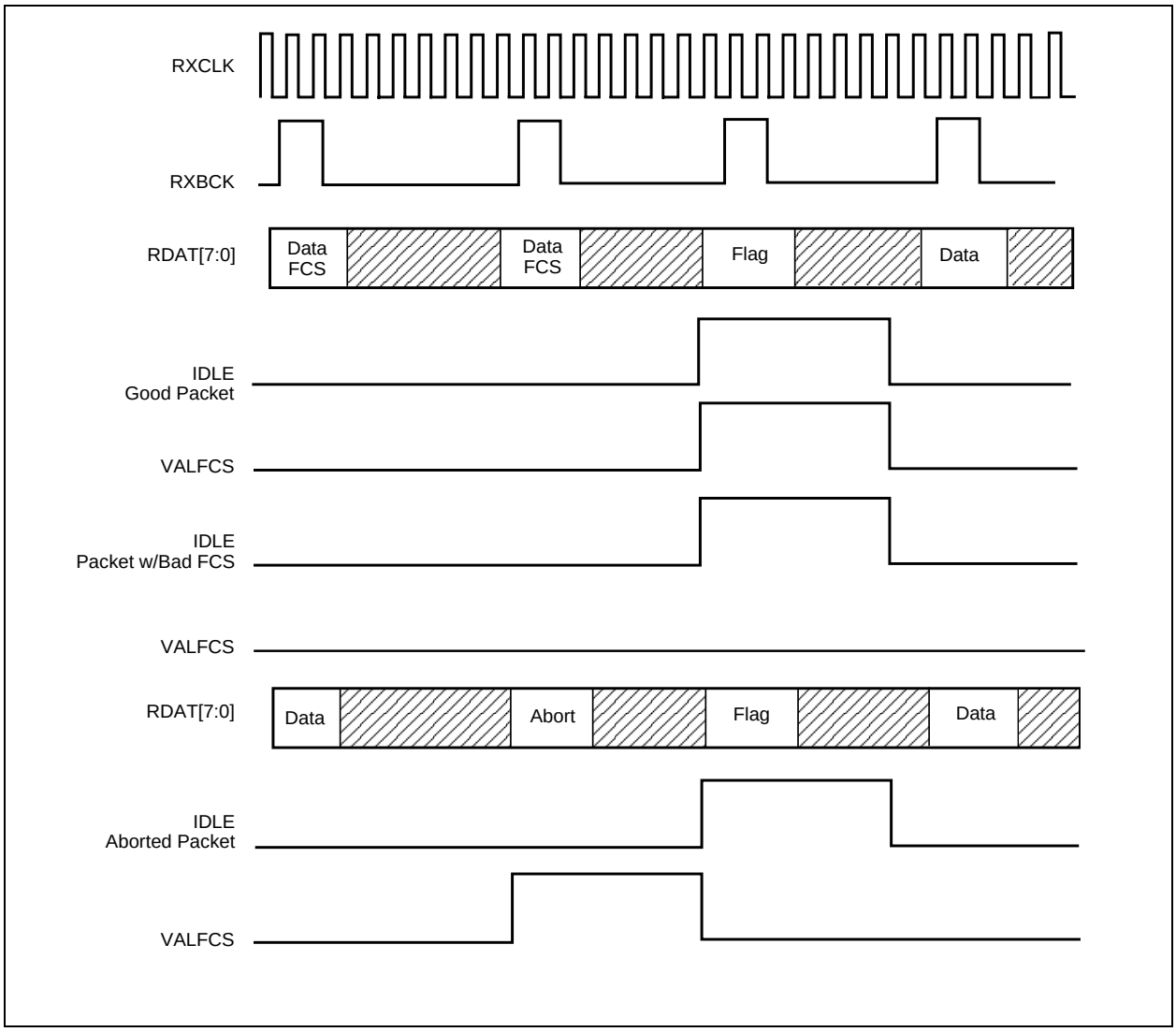
$$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1$$

Timing for this operation is shown in Figure A-5. Shown are cases of a good packet received, a packet received with a bad FCS, and an aborted packet. Each packet is shown with one idle flag marking the end of the packet and the start of the next packet. However, more than one flag can occur in the serial stream. The output data will contain each occurrence of idle or abort flags with a pulse on RXBCK.

The receive byte clock RXBCK is generated from the falling edge of the receive serial clock input on DS3CKI and is present continuously like the transmit byte clock. Nominally there will be one pulse on RXBCK for every eight clock cycles on the receive serial clock. When an inserted transparency bit must be deleted, the RXBCK period will be lengthened by one serial clock cycle. RXBCK is present during the reception of FCS octets and idle flags. On a received message with a valid 16-bit FCS, the last 2 byte clocks prior to IDLE and VALFCS going high will be the received FCS octets that were appended to the end of the message by the transmitter. In 32-bit mode, the last four received octets will be FCS octets. The RDAT[7:0], IDLE, and VALFCS outputs are valid at least one serial clock cycle period before the rising edge of RXBCK and are valid for at least two serial clock cycle periods after the falling edge of RXBCK.

FCS checking can be limited to the first N bytes of the received message by setting the LimitFCS control bit. In this mode, the FCS is checked only on the first N bytes received after the opening flag and then held until the end of the message. The locally calculated FCS is then compared to the last 2/4 bytes in the message to determine if a valid FCS was received. The desired number N can be from 1 to 16 (a value of 0 gives N=16) and is loaded in the FCSCnt control field. This allows FCS checking only on the header information in a T1 packet voice format.

Figure A-5. PPDL Receiver Timing



Control Registers

0x00—Mode Control Register (CR00)

NOTE: Rsvd bits in Control Registers must be set to zero.

7	6	5	4	3	2	1	0
LineLp	SourceLP	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd

LineLp Line Loopback Enable—Set to enable the loopback in the external direction. This loopback connects the received data stream before B3ZS/HDB3 decoding to the transmitter outputs. The received data is still presented to all receiver blocks and is present on the receiver output pins.

SourceLp Source Loopback Enable—Set to enable the loopback in the internal direction. This loopback connects the encoded transmitter data and clock directly to the receiver. Transmission of data on the line is not affected by this loopback.

0x04—Feature Control Register (CR04)

The Feature Control Register is provided to enable or disable miscellaneous features in the CN8330 Framer.

NOTE: Rsvd bits in Control Registers must be set to zero.

7	6	5	4	3	2	1	0
Rsvd	Rsvd	Rsvd	Rsvd	ParaEn	Rsvd	Rsvd	Rsvd

ParaEn Parallel Data Enable—Set high to enable the PPDL transmitter and receiver as the source and sink for data. Eight-bit data bytes are provided on the TDAT[7:0] and RDAT[7:0] buses for the PPDL transmitter and receiver. This bit must be set to 1 for operation as an HDLC formatter.

0x05—PPDL Control Register (CRO5)

The PPDL Control Register is provided to control the mode of operation of the PPDL transmitter and receiver.

NOTE: Rsvd bits in Control Registers must be set to zero.

7	6	5	4	3	2	1	0
FCSCnt[3]	FCSCnt[2]	FCSCnt[1]	FCSCnt[0]	LimitFCS	CRC32	Rsvd	Rsvd

FCSCnt[3:0] FCS Calculation Count—Determines the number of bytes over which the FCS is to be calculated. The number of bytes for calculation can be from 1 to 16 (a value of zero defaults to 16 bytes of calculation).

LimitFCS Limit FCS Calculation—Set to enable FCS calculation only on the first N bytes of an HDLC frame where N is determined by the FCS calculate count field. If this bit is low, the FCS will be calculated over all transmitted bytes.

CRC32 32-Bit CRC Select—Set high to enable 32-bit CRC generation and checking on the PPDL. If this bit is low, then 16-bit CRC generation and checking is enabled.

Appendix B

This appendix describes the various non-conformances associated with this device.

B.1 DS3CKI Clock Duty Cycle

Conexant recommends a 60/40 percent duty cycle maximum for the DS3CKI input.

B.2 Overhead Bit Insertion in E3 Parallel Payload Mode

When the framer is operated in E3 Parallel Payload mode with external overhead insertion enabled, the receive byte clock does not provide pulses where the overhead bits are inserted.

Workaround: An external hardware circuit can be constructed to provide a continuous byte clock synchronous to the receive byte clock. Contact the Conexant applications department for circuit details.

B.3 HDLC Formatter Mode Support While Configured for E3 Framing

This mode was previously selected by configuring the following bits: CR00.3=1 (E3Frm), CR04.3 (ParaEn) and CR05.1=0 (DisPPDL).If this mode is selected, the zero insertion function of the HDLC formatter incorrectly inserts an extra zero when the transmitted HDLC packet contains stuffed zeros that overlap the 16-bit E3 overhead. This transmitter malfunction causes the HDLC receiver to interpret the extra zero as data which results in an FCS errored packet. This problem prevents any customer from developing an E3 framed HDLC mode application. Notice that parallel data still functions properly in E3 mode if CR05.1=1 (DisPPDL).

Workaround: By using two CN8330 devices with one operating in HDLC formatter mode and another device exclusively in E3 mode same results can be achieved.

Appendix C

Here's what we've recommended as a starting point for those customers who need a jitter attenuation PLL for TBR24 compliance in E3 mode.

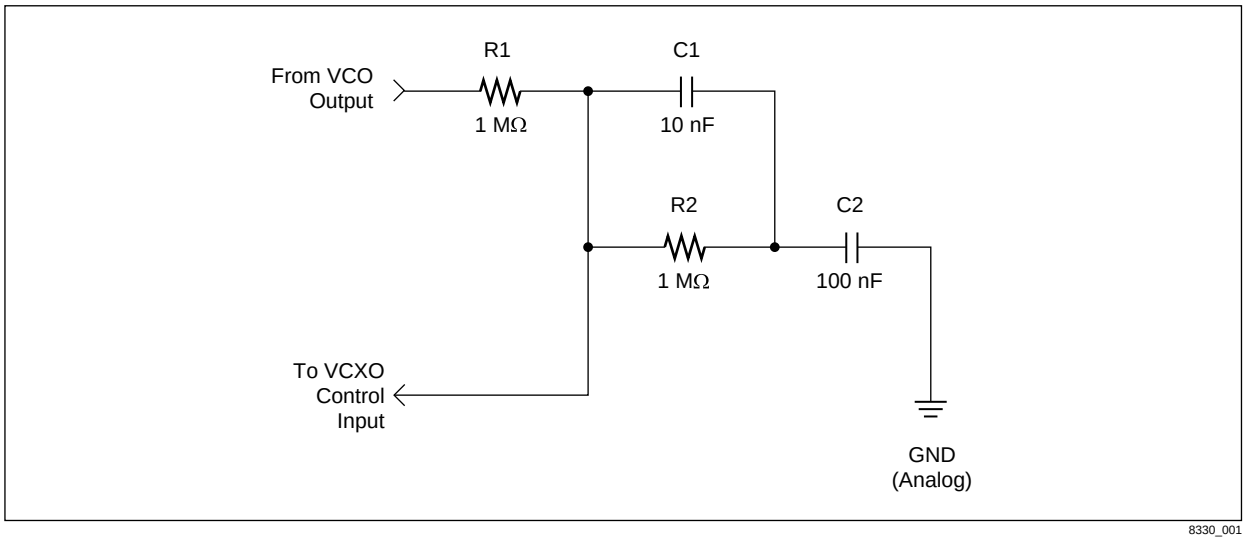
An external jitter attenuation PLL can be implemented for CN8330 with one VCXO and a passive LPF (low pass filter). The VCO output from CN8330 is passed through the LPF to create a control voltage input to the VCXO. The VCXO output then connects to RXCKI (and optionally to TXCKI) input of CN8330.

VCXO Specifications:	T3	E3	Units
Center Frequency:	44.736	34.368	MHz
Frequency Accuracy:	+/- 20	+/- 20	ppm
Frequency Pullability:	+/- 200	+/- 200	ppm

Note: +/- 100 ppm frequency pullability may be adequate.

The LPF circuit is shown below with the RC time constants used to establish the filter's cutoff frequencies as follows:

T1 = R1 x C2
T2 = R2 x C2
T3 = R2 x C1



R and C values shown above are calculated for typical applications.

The overall jitter transfer function also depends on the VCXO control voltage/frequency conversion ratio (Ko) parameter measured in radians per second per volt. In our PLL loop filter calculations, Ko equals approximately 400 for a VCXO with +/- 200 ppm pullability. Given Ko, a 10Hz break frequency is calculated for R1=R2=500K. With a 10Hz break, attenuation at 100Hz is around -12dB, barely sufficient to meet 0.4UI output jitter required with 1.5UI input and 0.08UI intrinsic jitter.

For added margin, R1=R2=1M puts the break frequency at 7Hz.

Several CN8330 customers have tested the jitter attenuation PLL with successfull results using R1=R2=1M. While this LPF should work for both T3 and E3 applications, we have not tested the PLL to comply with any regulatory or interface requirements. LPF cutoff frequencies might have to be scaled to match desired loop timing characteristics or to have the desired cutoff frequency. We recommend all customers conduct performance evaluation and characterization testing of the PLL before sending equipment for certification.



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