

### FEATURES

**33 V supply range**  
**130  $\Omega$  on resistance**  
**Fully specified at  $\pm 15$  V/+12 V**  
**3 V logic-compatible inputs**  
**Rail-to-rail operation**  
**Break-before-make switching action**  
**16-lead TSSOP and 16-lead SOIC\_N**  
**Upgrade for the ADG508A/ADG509A**

### APPLICATIONS

**Audio and video routing**  
**Test equipment**  
**Data acquisition systems**  
**Battery-powered systems**  
**Communication systems**  
**Signal routing**

### FUNCTIONAL BLOCK DIAGRAMS

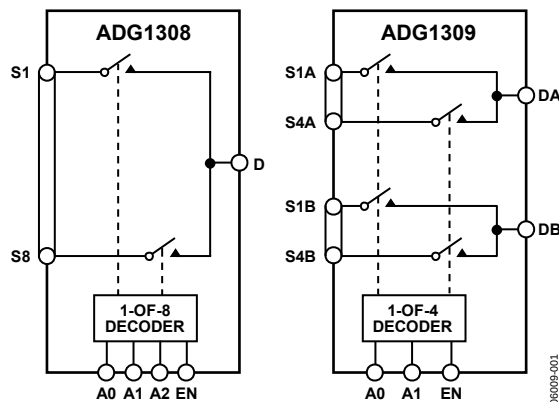


Figure 1.

### GENERAL DESCRIPTION

The ADG1308 and ADG1309 are monolithic analog multiplexers consisting of eight single channels and four differential channels, respectively. The ADG1308 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG1309 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched off.

When the switches are on, each switch conducts equally well in both directions and has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is the low charge injection for minimum transients when switching the digital inputs.

Fast switching speed coupled with high signal bandwidth makes the parts suitable for video signal switching. CMOS construction ensures ultra low power dissipation, making the parts ideally suited for portable and battery-powered instruments.

### PRODUCT HIGHLIGHTS

1. 16-lead TSSOP and 16-lead SOIC\_N available.
2. Pin compatible with the ADG508AKR and the ADG509AKR devices.
3. 3 V, logic-compatible digital input where:  
 $V_{IH} = 2.0$  V and  $V_{IL} = 0.8$  V.
4.  $V_L$  logic power supply not required.
5. Low power consumption.

#### Rev. A

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REVISION HISTORY

|                                                    |    |
|----------------------------------------------------|----|
| <b>1/09—Rev. 0 to Rev. A</b>                       |    |
| Change to I <sub>DD</sub> Parameter, Table 1 ..... | 4  |
| Change to I <sub>DD</sub> Parameter, Table 2 ..... | 5  |
| Updated Outline Dimensions .....                   | 14 |
| <b>4/06—Revision 0: Initial Version</b>            |    |

## SPECIFICATIONS

### DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted.<sup>1</sup>

Table 1.

| Parameter                                             | +25°C       | −40°C to +105°C      | Unit              | Test Conditions/Comments                                                          |
|-------------------------------------------------------|-------------|----------------------|-------------------|-----------------------------------------------------------------------------------|
| ANALOG SWITCH                                         |             |                      |                   |                                                                                   |
| Analog Signal Range                                   |             | $V_{SS}$ to $V_{DD}$ | V                 |                                                                                   |
| On Resistance, $R_{ON}$                               | 130         | 300                  | $\Omega$ typ      | $V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 13                    |
|                                                       | 210         |                      | $\Omega$ max      | $V_{DD} = +13.5\text{ V}$ , $V_{SS} = -13.5\text{ V}$                             |
| On Resistance Match Between Channels, $\Delta R_{ON}$ | 5           |                      | $\Omega$ typ      | $V_S = \pm 10\text{ V}$ , $I_S = -1\text{ mA}$                                    |
|                                                       | 10          |                      | $\Omega$ max      |                                                                                   |
| On Resistance Flatness, $R_{FLAT}$ (On)               | 25          |                      | $\Omega$ typ      | $V_S = -5\text{ V}, 0\text{ V}, +5\text{ V}$ , $I_S = -1\text{ mA}$               |
|                                                       | 70          |                      | $\Omega$ max      |                                                                                   |
| LEAKAGE CURRENTS                                      |             |                      |                   |                                                                                   |
| Source Off Leakage, $I_S$ (Off)                       | $\pm 1$     | $\pm 50$             | nA typ            | $V_D = \pm 10\text{ V}$ , $V_S = -10\text{ V}$ ; see Figure 14                    |
|                                                       |             |                      | nA max            |                                                                                   |
| Drain Off Leakage, $I_D$ (Off)                        | $\pm 1$     | $\pm 50$             | nA typ            | $V_S = 1\text{ V}, 10\text{ V}$ ; $V_D = 10\text{ V}, 1\text{ V}$ ; see Figure 14 |
|                                                       |             |                      | nA max            |                                                                                   |
| Channel On Leakage, $I_D, I_S$ (On)                   | $\pm 1$     | $\pm 50$             | nA typ            | $V_S = V_D = \pm 10\text{ V}$ ; see Figure 15                                     |
|                                                       |             | $\pm 50$             | nA max            |                                                                                   |
| DIGITAL INPUTS                                        |             |                      |                   |                                                                                   |
| Input High Voltage, $V_{INH}$                         | $\pm 0.005$ | 2.0                  | V min             | $V_{IN} = V_{INL}$ or $V_{INH}$                                                   |
| Input Low Voltage, $V_{INL}$                          |             | 0.8                  | V max             |                                                                                   |
| Input Current, $I_{INL}$ or $I_{INH}$                 |             | $\pm 0.1$            | $\mu\text{A}$ max |                                                                                   |
|                                                       |             |                      | $\mu\text{A}$ max |                                                                                   |
| Digital Input Capacitance, $C_{IN}$                   | 5           | pF typ               |                   |                                                                                   |
| DYNAMIC CHARACTERISTICS <sup>2</sup>                  |             |                      |                   |                                                                                   |
| Transition Time, $t_{TRANSITION}$                     | 80          | 190                  | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                        |
|                                                       | 130         |                      | ns max            | $V_S = 10\text{ V}$ ; see Figure 16                                               |
| $t_{ON}$ (EN)                                         | 80          | 120                  | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                        |
|                                                       | 100         |                      | ns max            | $V_S = 10\text{ V}$ ; see Figure 18                                               |
| $t_{OFF}$ (EN)                                        | 85          | 150                  | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                        |
|                                                       | 100         |                      | ns max            | $V_S = 10\text{ V}$ ; see Figure 18                                               |
| Break-Before-Make Time Delay, $t_{BBM}$               | 25          | 10                   | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                        |
|                                                       |             |                      | ns min            | $V_{S1} = V_{S2} = 10\text{ V}$ ; see Figure 17                                   |
| Charge Injection                                      | 2           |                      | pC typ            | $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 19      |
| Off Isolation                                         | 80          |                      | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 20     |
| Channel-to-Channel Crosstalk                          | 80          |                      | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 21     |
| −3 dB Bandwidth                                       | 500         |                      | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 22                          |
| $C_S$ (Off)                                           | 5           |                      | pF typ            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                           |
| $C_D$ (Off)                                           |             |                      |                   |                                                                                   |
| ADG1308                                               | 15          |                      | pF typ            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                           |
| ADG1309                                               | 10          |                      | pF typ            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                           |
| $C_D, C_S$ (On)                                       |             |                      |                   |                                                                                   |
| ADG1308                                               | 20          |                      | pF typ            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                           |
| ADG1309                                               | 15          |                      | pF typ            | $f = 1\text{ MHz}$ , $V_S = 0\text{ V}$                                           |

# ADG1308/ADG1309

| Parameter          | +25°C | −40°C to +105°C  | Unit              | Test Conditions/Comments                              |
|--------------------|-------|------------------|-------------------|-------------------------------------------------------|
| POWER REQUIREMENTS |       |                  |                   | $V_{DD} = +16.5\text{ V}$ , $V_{SS} = -16.5\text{ V}$ |
| $I_{DD}$           | 0.002 | 1.0              | $\mu\text{A typ}$ | Digital inputs = 0 V or $V_{DD}$                      |
|                    |       |                  | $\mu\text{A max}$ |                                                       |
| $I_{DD}$           | 220   | 380              | $\mu\text{A typ}$ | Digital inputs = 5 V                                  |
|                    |       |                  | $\mu\text{A max}$ |                                                       |
| $I_{SS}$           | 0.002 | 1.0              | $\mu\text{A typ}$ | Digital inputs = 0 V or $V_{DD}$ or 5 V               |
|                    |       |                  | $\mu\text{A max}$ |                                                       |
| $V_{DD}/V_{SS}$    |       | $\pm 5/\pm 16.5$ | V min/V max       | $ V_{DD}  =  V_{SS} $                                 |

<sup>1</sup> Temperature range for B version is −40°C to +105°C.  
<sup>2</sup> Guaranteed by design; not subject to production test.

**SINGLE SUPPLY**

$V_{DD} = 12\text{ V}$ ,  $V \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted.<sup>1</sup>

**Table 2.**

| Parameter                                             | +25°C       | –40°C to +105°C | Unit              | Test Conditions/Comments                                                        |
|-------------------------------------------------------|-------------|-----------------|-------------------|---------------------------------------------------------------------------------|
| <b>ANALOG SWITCH</b>                                  |             |                 |                   |                                                                                 |
| Analog Signal Range                                   |             | 0 to $V_{DD}$   | V                 |                                                                                 |
| On Resistance, $R_{ON}$                               | 325         |                 | $\Omega$ typ      | $V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -1\text{ mA}$ ; see Figure 13      |
|                                                       | 500         | 660             | $\Omega$ max      | $V_{DD} = 10.8\text{ V}$ , $V_{SS} = 0\text{ V}$                                |
| On Resistance Match Between Channels, $\Delta R_{ON}$ | 10          |                 | $\Omega$ typ      | $V_S = 0\text{ V}$ to $10\text{ V}$ , $I_S = -1\text{ mA}$                      |
|                                                       | 20          |                 | $\Omega$ max      |                                                                                 |
| On Resistance Flatness, $R_{FLAT}$ (On)               | 65          |                 | $\Omega$ typ      | $V_S = 3\text{ V}$ , $6\text{ V}$ , $9\text{ V}$ , $I_S = -1\text{ mA}$         |
| <b>LEAKAGE CURRENTS</b>                               |             |                 |                   |                                                                                 |
| Source Off Leakage, $I_S$ (Off)                       | $\pm 1$     |                 | nA typ            | $V_{DD} = 13.2\text{ V}$                                                        |
|                                                       |             | $\pm 50$        | nA max            | $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 14 |
| Drain Off Leakage, $I_D$ (Off)                        | $\pm 1$     |                 | nA typ            | $V_S = 1\text{ V}/10\text{ V}$ , $V_D = 10\text{ V}/1\text{ V}$ ; see Figure 14 |
|                                                       |             | $\pm 50$        | nA max            |                                                                                 |
| Channel On Leakage, $I_D$ , $I_S$ (On)                | $\pm 1$     |                 | nA typ            | $V_S = V_D = 1\text{ V}$ or $10\text{ V}$ ; see Figure 15                       |
|                                                       |             | $\pm 50$        | nA max            |                                                                                 |
| <b>DIGITAL INPUTS</b>                                 |             |                 |                   |                                                                                 |
| Input High Voltage, $V_{INH}$                         |             | 2.0             | V min             |                                                                                 |
| Input Low Voltage, $V_{INL}$                          |             | 0.8             | V max             |                                                                                 |
| Input Current, $I_{INL}$ or $I_{INH}$                 | $\pm 0.001$ |                 |                   |                                                                                 |
|                                                       |             | $\pm 0.1$       | $\mu\text{A}$ max | $V_{IN} = V_{INL}$ or $V_{INH}$                                                 |
| Digital Input Capacitance, $C_{IN}$                   | 3           |                 | pF typ            |                                                                                 |
| <b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>            |             |                 |                   |                                                                                 |
| Transition Time, $t_{TRANSITION}$                     | 100         |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 170         | 240             |                   | $V_S = 8\text{ V}$ ; see Figure 16                                              |
| $t_{ON}$ (EN)                                         | 90          |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 110         | 170             |                   | $V_S = 8\text{ V}$ ; see Figure 18                                              |
| $t_{OFF}$ (EN)                                        | 105         |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       | 130         | 180             |                   | $V_S = 8\text{ V}$ ; see Figure 18                                              |
| Break-Before-Make Time Delay, $t_{BBM}$               | 45          |                 | ns typ            | $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$                                      |
|                                                       |             | 20              | ns min            | $V_{S1} = V_{S2} = 8\text{ V}$ ; see Figure 17                                  |
| Charge Injection                                      | 2           |                 | pC typ            | $V_S = 6\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; see Figure 19    |
| Off Isolation                                         | 80          |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 20   |
| Channel-to-Channel Crosstalk                          | 80          |                 | dB typ            | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ ; see Figure 21   |
| –3 dB Bandwidth                                       | 500         |                 | MHz typ           | $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ ; see Figure 22                        |
| $C_S$ (Off)                                           | 5           |                 | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| $C_D$ (Off)                                           |             |                 |                   |                                                                                 |
| ADG1308                                               | 10          |                 | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| ADG1309                                               | 15          |                 | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| $C_D$ , $C_S$ (On)                                    |             |                 |                   |                                                                                 |
| ADG1308                                               | 20          |                 | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| ADG1309                                               | 15          |                 | pF typ            | $f = 1\text{ MHz}$ , $V_S = 6\text{ V}$                                         |
| <b>POWER REQUIREMENTS</b>                             |             |                 |                   |                                                                                 |
| $I_{DD}$                                              | 0.002       |                 | $\mu\text{A}$ typ | $V_{DD} = 13.2\text{ V}$                                                        |
|                                                       |             | 1.0             | $\mu\text{A}$ max | Digital inputs = $0\text{ V}$ or $V_{DD}$                                       |
| $I_{DD}$                                              | 220         |                 | $\mu\text{A}$ typ | Digital inputs = 5                                                              |
|                                                       |             | 380             | $\mu\text{A}$ max |                                                                                 |
| $V_{DD}$                                              |             | 5/16.5          | V min/V max       | $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$                                      |

<sup>1</sup> Temperature range for the B version is –40°C to +105°C.

<sup>2</sup> Guaranteed by design; not subject to production test.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

| Parameter                                                                | Rating                                                                                  |
|--------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| $V_{DD}$ to $V_{SS}$                                                     | 35 V                                                                                    |
| $V_{DD}$ to GND                                                          | −0.3 V to +25 V                                                                         |
| $V_{SS}$ to GND                                                          | +0.3 V to −25 V                                                                         |
| Analog, Digital Inputs <sup>1</sup>                                      | $V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or<br>30 mA (whichever occurs first) |
| Continuous Current, S or D pins                                          | 30 mA                                                                                   |
| Peak Current, S or D pins<br>(Pulsed at 1 ms, 10% Duty<br>Cycle Maximum) | 100 mA                                                                                  |
| Operating Temperature Range                                              |                                                                                         |
| Industrial (B Version)                                                   | −40°C to +105°C                                                                         |
| Storage Temperature Range                                                | −65°C to +150°C                                                                         |
| Junction Temperature                                                     | 150°C                                                                                   |
| TSSOP, $\theta_{JA}$ ,<br>Thermal Impedance                              | 112°C/W                                                                                 |
| 16-Lead SOIC, $\theta_{JA}$ ,<br>Thermal Impedance                       | 77°C/W                                                                                  |
| Reflow Soldering Peak<br>Temperature (Pb-free)                           | 260 (+0/−5)°C                                                                           |

<sup>1</sup> Overvoltages at A, EN, S, or D pins are clamped by internal diodes. Current should be limited to the maximum ratings provided.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

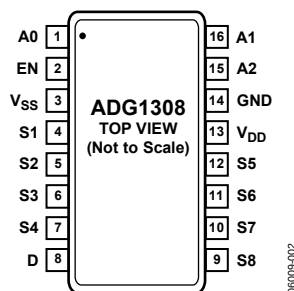


Figure 2. ADG1308 Pin Configuration (TSSOP and SOIC\_N)

Table 4. ADG1308 Pin Function Descriptions

| Pin Number | Mnemonic        | Description                                                                                                                             |
|------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 1          | A0              | Logic Control Input A0.                                                                                                                 |
| 2          | EN              | Active High Digital Input. When low, the device is disabled and all switches are off. When high, Ax logic inputs determine on switches. |
| 3          | V <sub>SS</sub> | Most Negative Power Supply Potential. In single supply applications, this pin can be connected to ground.                               |
| 4          | S1              | Source Terminal 1. Can be an input or an output.                                                                                        |
| 5          | S2              | Source Terminal 2. Can be an input or an output.                                                                                        |
| 6          | S3              | Source Terminal 3. Can be an input or an output.                                                                                        |
| 7          | S4              | Source Terminal 4. Can be an input or an output.                                                                                        |
| 8          | D               | Drain Terminal. Can be an input or an output.                                                                                           |
| 9          | S8              | Source Terminal 8. Can be an input or an output.                                                                                        |
| 10         | S7              | Source Terminal 7. Can be an input or an output.                                                                                        |
| 11         | S6              | Source Terminal 6. Can be an input or an output.                                                                                        |
| 12         | S5              | Source Terminal 5. Can be an input or an output.                                                                                        |
| 13         | V <sub>DD</sub> | Most Positive Power Supply Potential.                                                                                                   |
| 14         | GND             | Ground (0 V) Reference.                                                                                                                 |
| 15         | A2              | Logic Control Input A2.                                                                                                                 |
| 16         | A1              | Logic Control Input A1.                                                                                                                 |

## ADG1308 TRUTH TABLE

Table 5.

| A2             | A1             | A0             | EN | ON SWITCH |
|----------------|----------------|----------------|----|-----------|
| X <sup>1</sup> | X <sup>1</sup> | X <sup>1</sup> | 0  | NONE      |
| 0              | 0              | 0              | 1  | 1         |
| 0              | 0              | 1              | 1  | 2         |
| 0              | 1              | 0              | 1  | 3         |
| 0              | 1              | 1              | 1  | 4         |
| 1              | 0              | 0              | 1  | 5         |
| 1              | 0              | 1              | 1  | 6         |
| 1              | 1              | 0              | 1  | 7         |
| 1              | 1              | 1              | 1  | 8         |

<sup>1</sup> X = Don't care.

# ADG1308/ADG1309

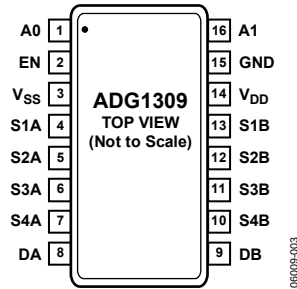


Figure 3. ADG1309 Pin Configuration (TSSOP and SOIC\_N)

Table 6. ADG1309 Pin Function Descriptions

| Pin Number<br>SOIC/TSSOP | Mnemonic        | Description                                                                                                                                         |
|--------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| 1                        | A0              | Logic Control Input A0.                                                                                                                             |
| 2                        | EN              | Active High Digital Input. When low, the device is disabled and all switches are off. When high, A <sub>x</sub> logic inputs determine on switches. |
| 3                        | V <sub>SS</sub> | Most Negative Power Supply Potential. In single supply applications, this pin can be connected to ground.                                           |
| 4                        | S1A             | Source Terminal 1A. Can be an input or an output.                                                                                                   |
| 5                        | S2A             | Source Terminal 2A. Can be an input or an output.                                                                                                   |
| 6                        | S3A             | Source Terminal 3A. Can be an input or an output.                                                                                                   |
| 7                        | S4A             | Source Terminal 4A. Can be an input or an output.                                                                                                   |
| 8                        | DA              | Drain Terminal A. Can be an input or an output.                                                                                                     |
| 9                        | DB              | Drain Terminal B. Can be an input or an output.                                                                                                     |
| 10                       | S4B             | Source Terminal 4B. Can be an input or an output.                                                                                                   |
| 11                       | S3B             | Source Terminal 3B. Can be an input or an output.                                                                                                   |
| 12                       | S2B             | Source Terminal 2B. Can be an input or an output.                                                                                                   |
| 13                       | S1B             | Source Terminal 1B. Can be an input or an output.                                                                                                   |
| 14                       | V <sub>DD</sub> | Most Positive Power Supply Potential.                                                                                                               |
| 15                       | GND             | Ground (0 V) Reference.                                                                                                                             |
| 16                       | A1              | Logic Control Input A1.                                                                                                                             |

## ADG1309 TRUTH TABLE

Table 7.

| AI             | A0             | EN | ON SWITCH PAIR |
|----------------|----------------|----|----------------|
| X <sup>1</sup> | X <sup>1</sup> | 0  | NONE           |
| 0              | 0              | 1  | 1              |
| 0              | 1              | 1  | 2              |
| 1              | 0              | 1  | 3              |
| 1              | 1              | 1  | 4              |

<sup>1</sup> X = Don't care.

## TYPICAL PERFORMANCE CHARACTERISTICS

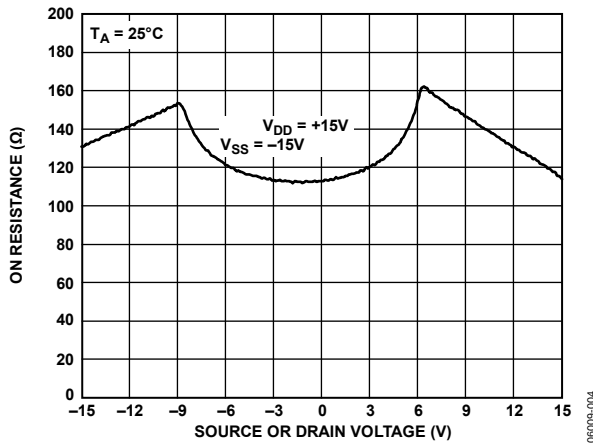


Figure 4. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Dual Supply

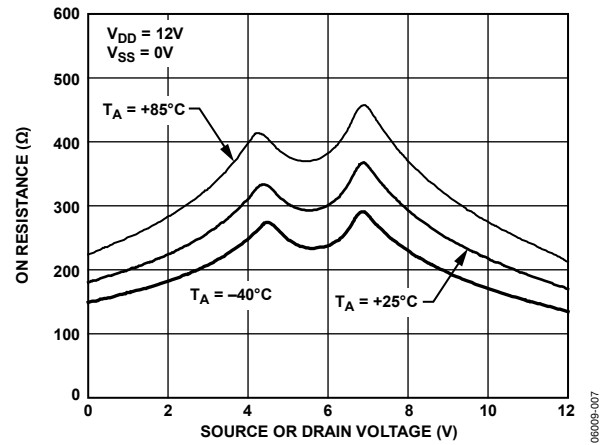


Figure 7. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Single Supply

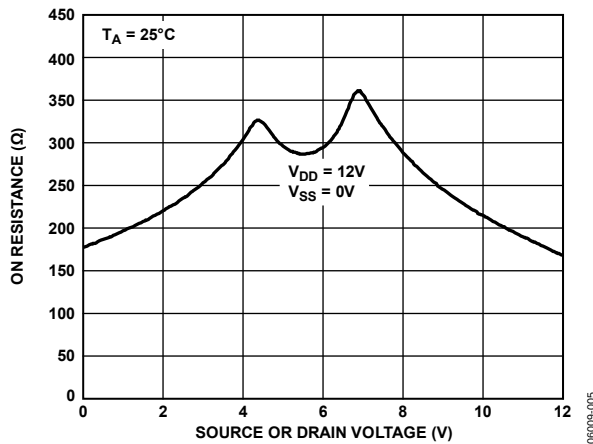


Figure 5. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Single Supply

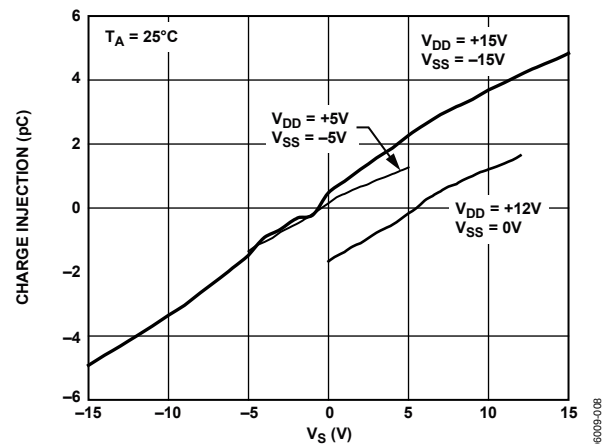


Figure 8. Charge Injection vs. Source Voltage

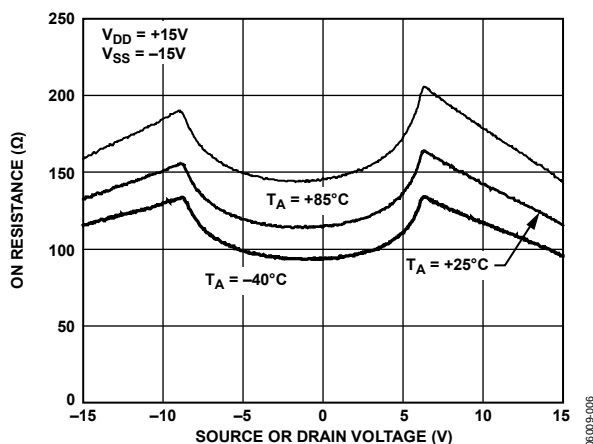


Figure 6. On Resistance as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures, Dual Supply

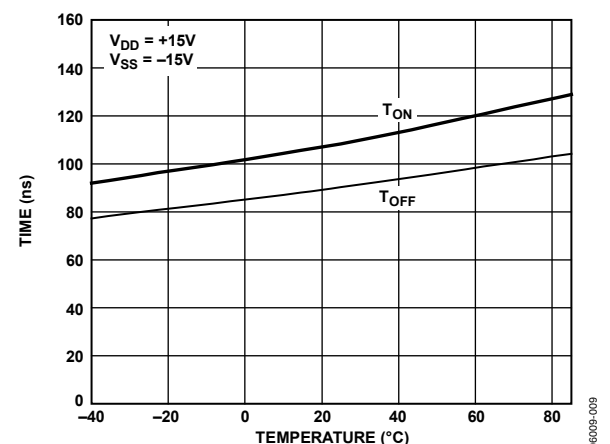


Figure 9.  $T_{ON}/T_{OFF}$  Time vs. Temperature

# ADG1308/ADG1309

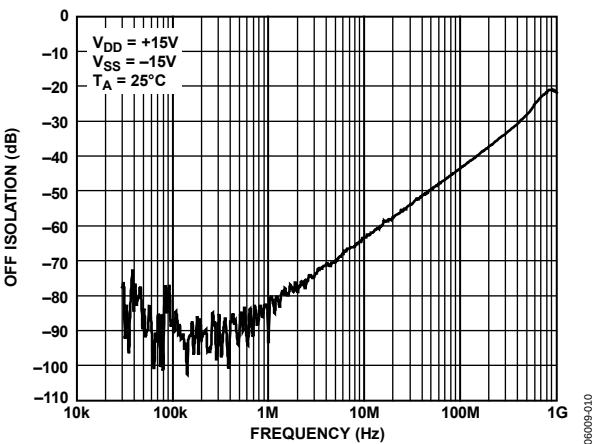


Figure 10. Off Isolation vs. Frequency

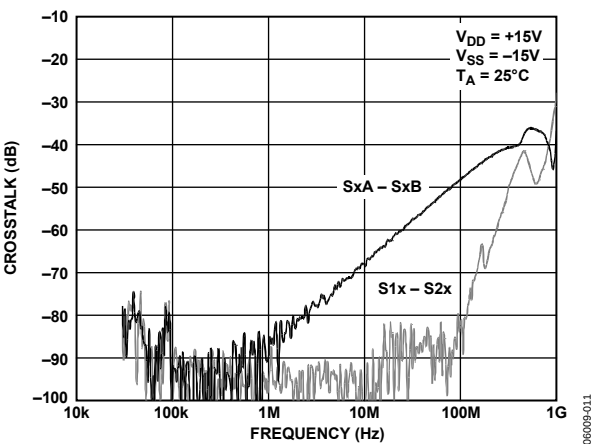


Figure 12. Crosstalk vs. Frequency

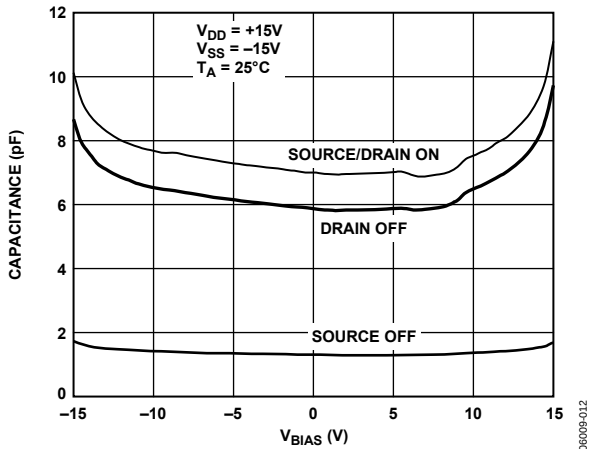


Figure 11. ADG1308 Capacitance vs. Source Voltage,  $\pm 15 V$  Dual Supply

## TEST CIRCUITS

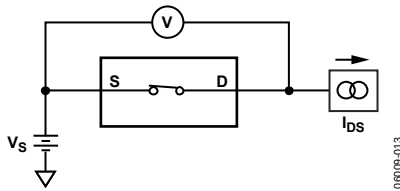


Figure 13. On Resistance

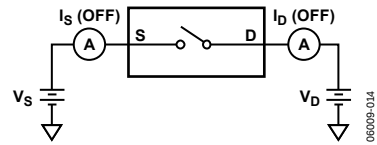


Figure 14. Off Leakage

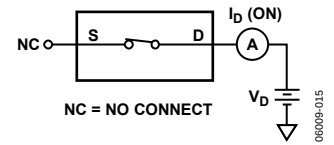


Figure 15. On Leakage

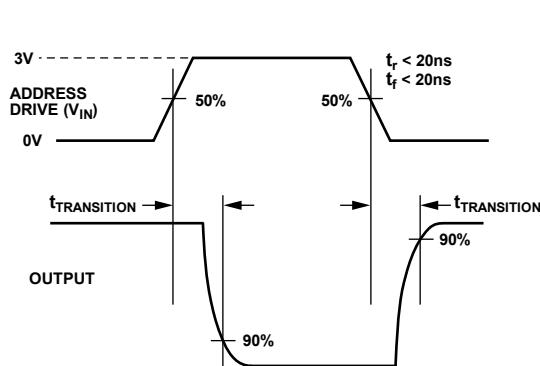
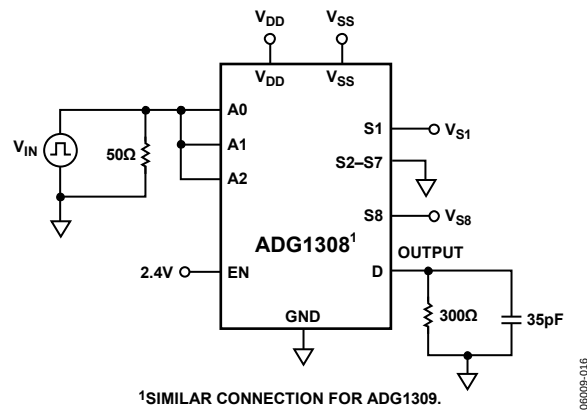


Figure 16. Address to Output Switching Times,  $t_{\text{TRANSITION}}$



<sup>1</sup>SIMILAR CONNECTION FOR ADG1309.

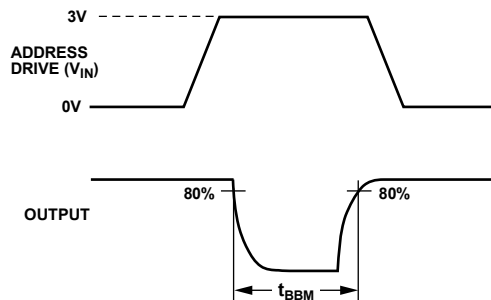
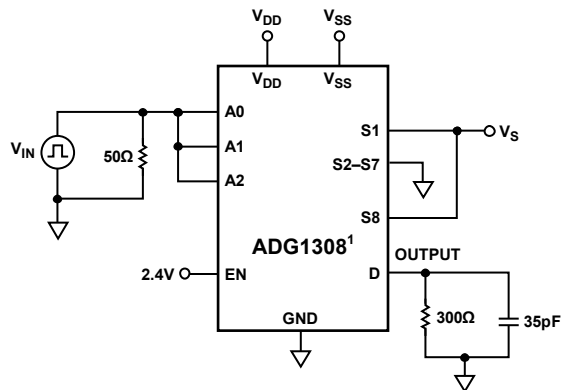


Figure 17. Break-Before-Make Delay,  $t_{\text{BBM}}$



<sup>1</sup>SIMILAR CONNECTION FOR ADG1309.

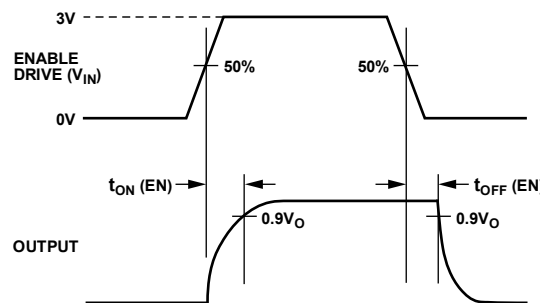
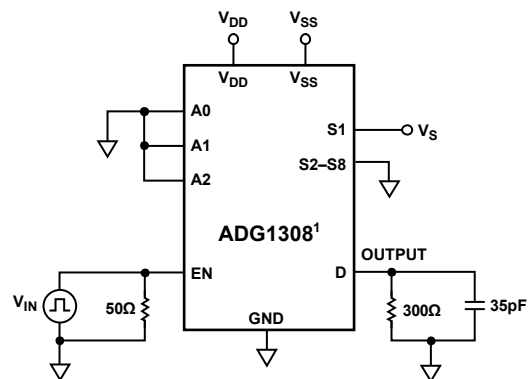
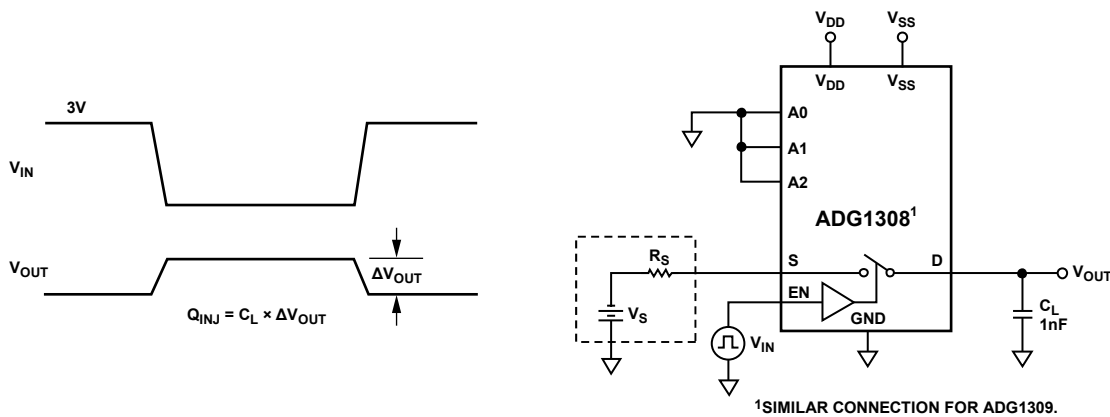


Figure 18. Enable Delay,  $t_{\text{ON}}(\text{EN})$ ,  $t_{\text{OFF}}(\text{EN})$



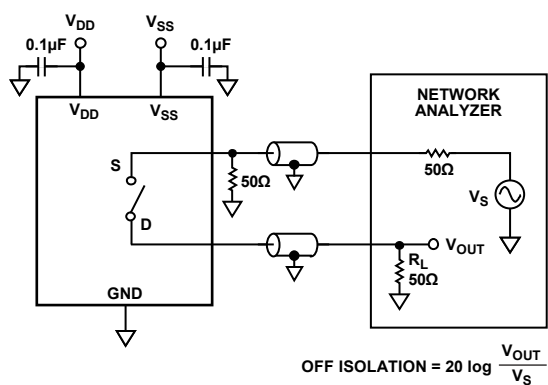
<sup>1</sup>SIMILAR CONNECTION FOR ADG1309.

# ADG1308/ADG1309



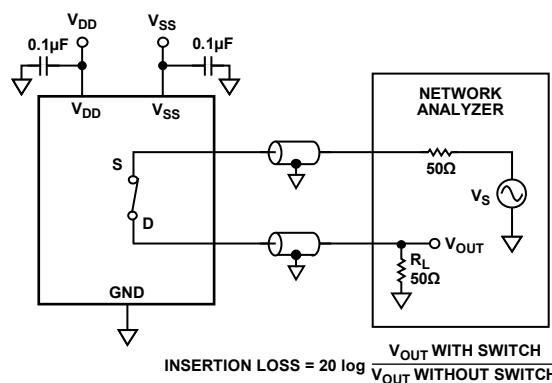
06009-019

Figure 19. Charge Injection



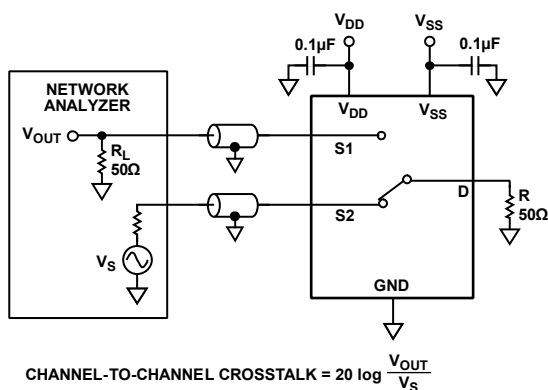
06009-020

Figure 20. Off Isolation



06009-021

Figure 22. Bandwidth



01009-022

Figure 21. Channel-to-Channel Crosstalk

## TERMINOLOGY

### $R_{ON}$

Ohmic resistance between D and S.

### $\Delta R_{ON}$

Difference between the  $R_{ON}$  of any two channels.

### $I_S$ (Off)

Source leakage current when the switch is off.

### $I_D$ (Off)

Drain leakage current when the switch is off.

### $I_D, I_S$ (On)

Channel leakage current when the switch is on.

### $V_D$ ( $V_S$ )

Analog voltage on Terminal D and Terminal S.

### $C_S$ (Off)

Channel input capacitance for off condition.

### $C_D$ (Off)

Channel output capacitance for off condition.

### $C_D, C_S$ (On)

On switch capacitance.

### $C_{IN}$

Digital input capacitance.

### $t_{ON}$ (EN)

Delay time between the 50% and 90% points of the digital input and switch on condition.

### $t_{OFF}$ (EN)

Delay time between the 50% and 90% points of the digital input and switch off condition.

### $t_{TRANSITION}$

Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

### $T_{BBM}$

Off time measured between the 80% point of both switches when switching from one address state to another.

### $V_{INL}$

Maximum input voltage for Logic 0.

### $V_{INH}$

Minimum input voltage for Logic 1.

### $I_{INL}$ ( $I_{INH}$ )

Input current of the digital input.

### $I_{DD}$

Positive supply current.

### $I_{SS}$

Negative supply current.

### Off Isolation

A measure of unwanted signal coupling through an off channel.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

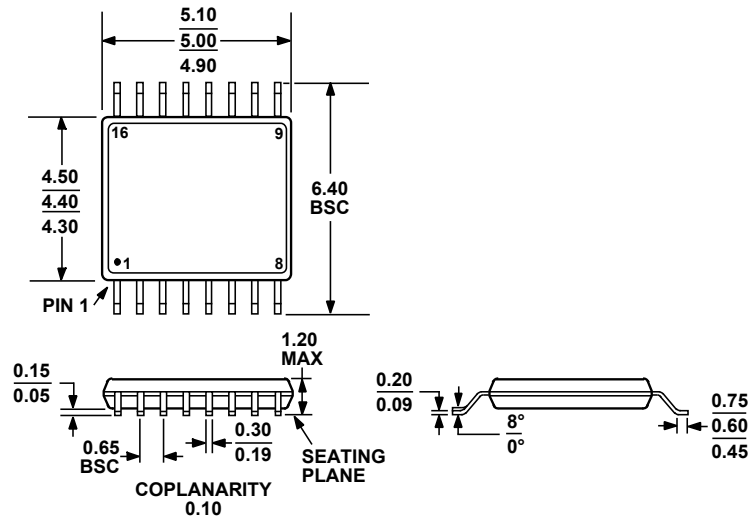
### Bandwidth

The frequency at which the output is attenuated by 3 dB.

### On Response

The frequency response of the on switch.

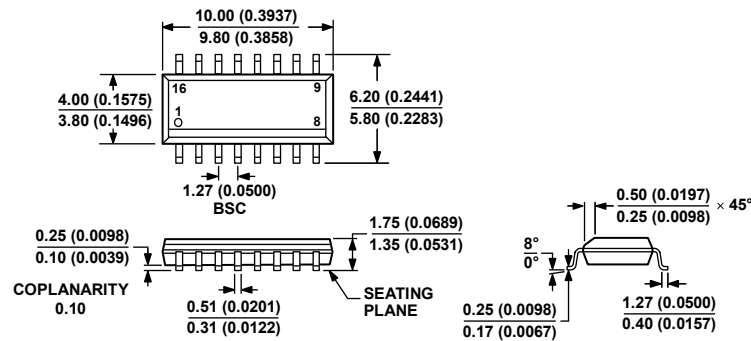
## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 23. 16-Lead Thin Shrink Small Outline Package [TSSOP]  
(RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 24. 16-Lead Standard Small Outline Package [SOIC\_N]

Narrow Body

(R-16)

Dimensions shown in millimeters and (inches)

060606-A

## ORDERING GUIDE

| Model                          | Temperature Range | Package Description                                | Package Option |
|--------------------------------|-------------------|----------------------------------------------------|----------------|
| ADG1308BRUZ <sup>1</sup>       | −40°C to +105°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP]  | RU-16          |
| ADG1308BRUZ-REEL7 <sup>1</sup> | −40°C to +105°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP]  | RU-16          |
| ADG1308BRZ <sup>1</sup>        | −40°C to +105°C   | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16           |
| ADG1308BRZ-REEL7 <sup>1</sup>  | −40°C to +105°C   | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16           |
| ADG1309BRUZ <sup>1</sup>       | −40°C to +105°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP]  | RU-16          |
| ADG1309BRUZ-REEL7 <sup>1</sup> | −40°C to +105°C   | 16-Lead Thin Shrink Small Outline Package [TSSOP]  | RU-16          |
| ADG1309BRZ <sup>1</sup>        | −40°C to +105°C   | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16           |
| ADG1309BRZ-REEL7 <sup>1</sup>  | −40°C to +105°C   | 16-Lead Narrow Body Small Outline Package [SOIC_N] | R-16           |

<sup>1</sup> Z = RoHS Compliant Part.

NOTES

## NOTES

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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