

General Description

The MAX5075 is a +4.5V to +15V push-pull, current-fed topology driver subsystem with an integrated oscillator for use in telecom module power supplies. The device drives two MOSFETs connected to a center-tapped transformer primary providing secondary-side, isolated, negative or positive voltages. This device features a programmable, accurate, integrated oscillator with a synchronizing clock output that synchronizes an external PWM regulator. A single external resistor programs the internal oscillator frequency from 50kHz to 1.5MHz.

The MAX5075 incorporates a dual MOSFET driver with ±3A peak drive currents and 50% duty cycle. The MOSFET driver generates complementary signals to drive external ground-referenced n-channel MOSFETs.

The MAX5075 is available with a clock output frequency to MOSFET driver frequency ratio of 1x, 2x, and 4x. The MAX5075 is available in a thermally enhanced 8-pin µMAX® package and is specified over the -40°C to +125°C operating temperature range.

Applications

Current-Fed, High-Efficiency Power-Supply Modules Power-Supply Building Subsystems Push-Pull Driver Subsystems

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Pin Configuration appears at end of data sheet.

Features

- ♦ Current-Fed, Push-Pull Driver Subsystem
- Programmable, Accurate Internal Oscillator
- ♦ Single +4.5V to +15V Supply Voltage Range
- ♦ Dual ±3A Gate-Drive Outputs
- ♦ 1mA Operating Current at 250kHz with No **Capacitive Load**
- Synchronizing Clock Frequency Generation **Options**
- ♦ Thermally Enhanced 8-Pin µMAX Package
- ♦ -40°C to +125°C Operating Temperature Range

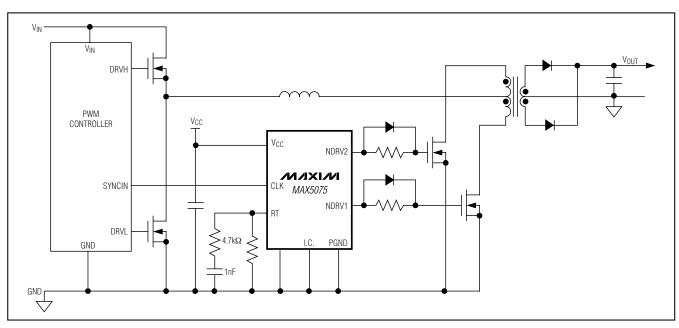
Ordering Information

PART	PIN- PACKAGE	TOP MARK	PKG CODE	f _{CLK} /f _{NDRV} _ RATIO
MAX5075AAUA	8 μMAX-EP*	AAAU	U8E-2	1
MAX5075BAUA	8 μMAX-EP*	AAAV	U8E-2	2
MAX5075CAUA	8 μMAX-EP*	AAAW	U8E-2	4

^{*}EP = Exposed paddle.

Note: All devices specified for -40°C to +125°C operating temperature range.

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

V _{CC} to DGND, PGND	0.3V to +18V
CLK, RT to DGND	
NDRV1, NDRV2 to PGND	$0.3V$ to $(V_{CC} + 0.3V)$
DGND to PGND	0.3V to +0.3V
CLK Current	±20mA
NDRV1, NDRV2 Peak Current (200ns)	±5A
NDRV1, NDRV2 Reverse Current (Latchu	p Current)±500mA

Continuous Power Dissipation ($T_A = +70$ °C)	
8-Pin µMAX (derate 10.3mW/°C above +70°	C)825mW
Operating Temperature Range	40°C to +125°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{CC} = +12V, R_{RT} = 124k\Omega, NDRV1 = NDRV2 = open, T_A = T_J = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are measured at $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY	•			•			•
Input Voltage Supply Range	Vcc			4.5		15.0	V
Switching Supply Current	Iccsw	fosc = 250kHz			1	3	mA
Undervoltage Lockout	V _U VLO	V _{CC} rising		3	3.5	4	V
UVLO Hysteresis					300		mV
OSCILLATOR							
Frequency Range	fosc	(Note 2)		50		1500	kHz
Accuracy		f _{OSC} = 250kHz , 6V ≤ V _{CC} ≤ 15V (Note 3)		-8		+10	%
Oscillator Jitter					±0.6		%
CLK Output High Voltage		La 1ma A	$7V \le V_{CC} \le 15V$	3.9		5.0	- v
		I _{CLK} = 1mA	$4.5V \le V_{CC} \le 7V$	3.35		5.0	
CLK Output Low Voltage		I _{CLK} = -1mA				50	mV
CLK Output Rise Time		C _{CLK} = 30pF			35		ns
CLK Output Fall Time		C _{CLK} = 30pF			10		ns
GATE DRIVERS (NDRV1, NDRV	2)						
Output High Voltage	V _{OH}	I _{NDRV1} = I _{NDRV2} = 100mA		V _{CC} - 0.3			V
Output Low Voltage	V _{OL}	I _{NDRV1} = I _{NDRV2} = -100mA				0.3	V
Output Peak Current	IР	Sourcing and sinking			3		А
Driver Outrout Iron adams		NDRV_ sourcing 100mA			1.8	3	Ω
Driver Output Impedance		NDRV_ sinking 100mA			1.6	2.6	
Latchup Current Protection		Reverse current at NDRV1/NDRV2			400		mA
Rise Time	t _R	C _{LOAD} = 2nF			10		ns
Fall Time	tF	C _{LOAD} = 2nF			10		ns

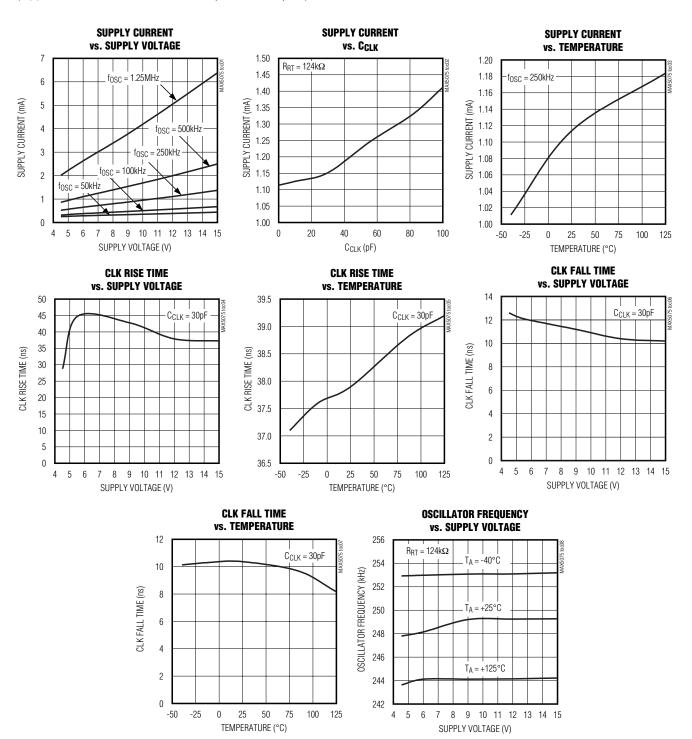
Note 1: The MAX5075 is 100% tested at $T_A = T_J = +125$ °C. All limits over temperature are guaranteed by design.

Note 2: Use the following formula to calculate the MAX5075 oscillator frequency: $f_{OSC} = 10^{12}/(32 \times R_{RT})$.

Note 3: The accuracy of the oscillator's frequency is lower at frequencies greater than 1MHz.

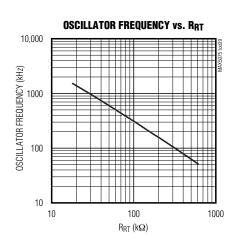
Typical Operating Characteristics

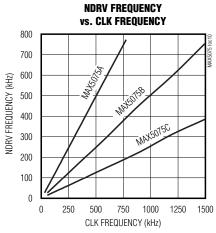
 $(V_{CC} = +12V, R_{RT} = 124k\Omega, NDRV_ = open, CLK = open.)$

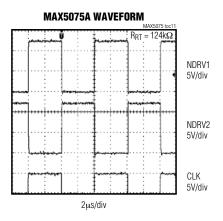


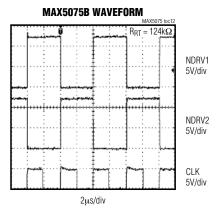
Typical Operating Characteristics (continued)

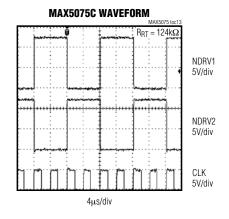
 $(V_{CC} = +12V, R_{RT} = 124k\Omega, NDRV_ = open, CLK = open.)$











Pin Description

PIN	NAME	FUNCTION		
1	CLK	Synchronizing Clock Output. Clock output with a ±10mA peak current drive that can be used to synchronize an external PWM regulator. CLK/NDRV1 frequency has a 1x, 2x, or 4x ratio. See the <i>Synchronizing Clock Output</i> section.		
2	I.C.	Internal Connection. Connect to ground. Internal function.		
3	RT	Oscillator Timing Resistor Connection. Bypass RT with a series combination of a $4.7k\Omega$ resistor and a 1nF capacitor to DGND. Connect a resistor from RT to DGND to set the internal oscillator.		
4	DGND	Digital Ground. Connect DGND to ground plane.		
5	PGND	Power Ground. Connect PGND to ground plane.		
6	NDRV1	Gate Driver 1. Connect NDRV1 to the gate of the external n-channel FET.		
7	NDRV2	Gate Driver 2. Connect NDRV2 to the gate of the external n-channel FET.		
8	Vcc	Power-Supply Input. Bypass V _{CC} to PGND with 0.1µFll1µF ceramic capacitors.		
EP	EP	Exposed Pad. Internally connected to DGND. Connect exposed pad to ground plane.		

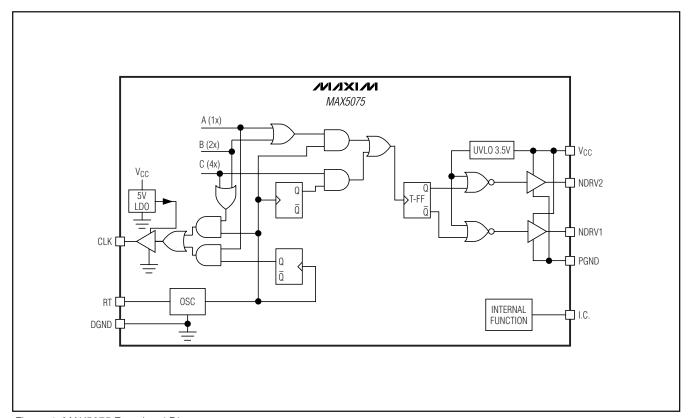


Figure 1. MAX5075 Functional Diagram

Detailed Description

The MAX5075 is a +4.5V to +15V push-pull, current-fed topology driver subsystem with an integrated oscillator for use in 48V module power supplies.

The MAX5075 features a programmable, accurate integrated oscillator with a synchronizing clock output that can be used to synchronize an external PWM stage. A single external resistor programs the internal oscillator frequency from 50kHz to 1.5MHz.

The MAX5075 incorporates a dual MOSFET driver with ±3A peak drive currents and a 50% duty cycle. The MOSFET driver generates complementary signals to drive external ground-referenced n-channel MOSFETs.

The MAX5075 is available with a clock output frequency to MOSFET driver frequency ratios of 1x, 2x, and 4x.

Internal Oscillator

An external resistor at RT programs the MAX5075 internal oscillator frequency from 50kHz to 1.5MHz. The MAX5075A/B NDRV1 and NDRV2 switching frequencies are one-half the programmed oscillator frequency with a nominal 50% duty cycle. The MAX5075C NDRV1 and NDRV2 switching frequencies are one-fourth the oscillator frequency.

Use the following formula to calculate the internal oscillator frequency:

$$f_{OSC} = \frac{10^{12}}{32 \times R_{BT}}$$

where fosc is the oscillator frequency and $\ensuremath{\mathsf{R}}\xspace$ is a resistor connected from RT to DGND in ohms.

Place a series combination of a $4.7 k\Omega$ resistor and a 1nF capacitor from RT to DGND for stability and to filter out noise.

Synchronizing Clock Output

The MAX5075 provides a buffered clock output that can be used to synchronize the oscillator input of a PWM controller. CLK is powered from an internal 5V regulator and sources/sinks up to 10mA. The MAX5075 has internal CLK output frequency to NDRV1 and NDRV2 switching frequency ratios set to 1x, 2x, or 4x (Table 1).

The MAX5075A has a CLK frequency to NDRV_ frequency ratio set to 1x. The MAX5075B has a CLK frequency to NDRV_ frequency ratio set to 2x and the MAX5075C has a CLK frequency to NDRV_ frequency ratio set to 4x. There is a typical 30ns delay from CLK to NDRV_ output.

Table 1. MAX5075 CLK Output Frequency

PART	fclk	fNDRV1	f _{CLK} to f _{SW} RATIO
MAX5075A	fosc / 2	fosc / 2	1
MAX5075B	fosc	fosc / 2	2
MAX5075C	fosc	fosc / 4	4

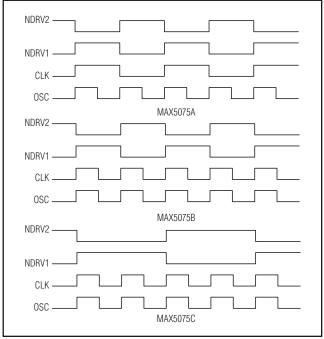


Figure 2. MAX5075 CLK Timing Diagrams

Applications Information

Supply Bypassing

Pay careful attention to bypassing and grounding the MAX5075. Peak supply and output currents may exceed 3A when driving large MOSFETs. Ground shifts due to insufficient device grounding may also disturb other circuits sharing the same ground-return path. Any series inductance in the V_{CC}, NDRV1, NDRV2, and/or GND paths can cause noise due to the very high di/dt when switching the MAX5075 with any capacitive load. Place one or more 0.1µF ceramic capacitors in parallel as close to the device as possible to bypass V_{CC} to PGND. Use a ground plane to minimize ground-return resistance and inductance. Place the external MOSFETs as close as possible to the MAX5075 to further minimize board inductance and AC path impedance.

Power Dissipation

The power dissipation of the MAX5075 is a function of the sum of the quiescent current and the output current (either capacitive or resistive load). Maintain the sum of the currents so the maximum power dissipation limit is not exceeded. The power dissipation (PDISS) due to the quiescent switching supply current (ICCSW) can be calculated as:

For capacitive loads, use the following equation to estimate the power dissipation:

$$PLOAD = 2 \times CLOAD \times VCC^2 \times fNDRV$$

where C_{LOAD} is the capacitive load at NDRV1 and NDRV2, V_{CC} is the supply voltage, and f_{NDRV} is the MAX5075 NDRV_ switching frequency.

Calculate the total power dissipation (PT) as follows:

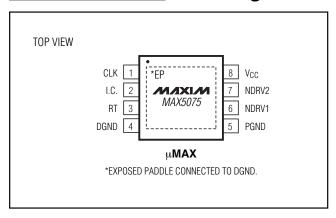
Layout Recommendations

The MAX5075 sources and sinks large currents that can create very fast rise and fall edges at the gate of the switching MOSFETs. The high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. Use the following PC board layout guidelines when designing with the MAX5075:

 Place one or more 0.1µF decoupling ceramic capacitors from V_{CC} to PGND as close to the device as possible. Connect V_{CC} and all ground pins to large copper areas. Place one bulk capacitor of 10µF on the PC board with a low-impedance path to the V_{CC} input and PGND of the MAX5075.

- Two AC current loops form between the device and the gate of the driven MOSFETs. The MOSFETs look like a large capacitance from gate to source when the gate pulls low. The current loop is from the MOSFET gate to NDRV1 and NDRV2 of the MAX5075, to PGND, and to the source of the MOSFET. When the gate of the MOSFET pulls high, the current is from the VCC terminal of the decoupling capacitor, to VCC of the MAX5075, to NDRV1 and NDRV2, and to the MOSFET gate and source. Both charging current and discharging current loops are important. Minimize the physical distance and the impedance in these AC current paths.
- Keep the device as close to the MOSFET as possible.

Pin Configuration



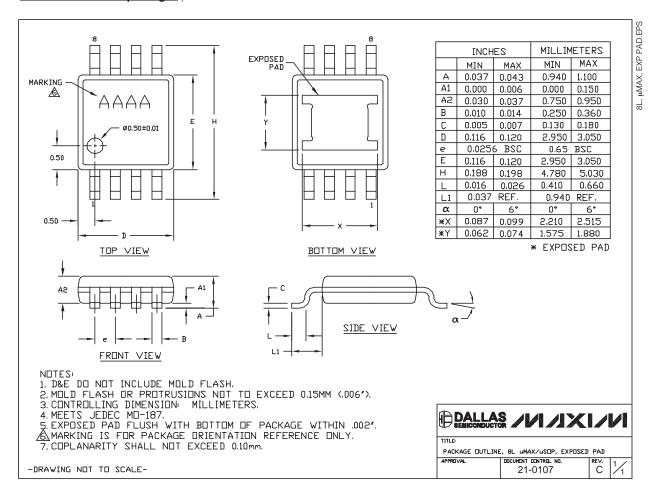
Chip Information

TRANSISTOR COUNT: 1335

PROCESS: BICMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)



_Revision History

Pages changed at Rev 1: 1, 2, 5, 6, 8

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

8 ______Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600



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Тел: +7 (812) 336 43 04 (многоканальный) Email: org@lifeelectronics.ru