500 MHz Dual Integrated DCL with Differential Drive/Receive, Level Setting DACs, and Per Pin PMU

ADATE302-02

FEATURES

Driver
- **3-level driver with high-Z mode and built-in clamps**
- **Precision trimmed output resistance**
- **Low leakage mode (typically <10 nA)**
- **Voltage range: −2.0 V to +6.0 V**
- **1.0 ns minimum pulse width, 1 V terminated**

Comparator
- **Window and differential comparator**
- **>1 GHz input equivalent bandwidth**

Load
- **±12 mA maximum current capability**

Per pin PMU
- **Force voltage range: −2.0 V to +6.0 V**
- **5 current ranges: 25 mA, 2 mA, 200 μA, 20 μA, and 2 μA**

Levels
- **14-bit DAC for DCL levels**
- **Typically <±5 mV INL (calibrated)**
- **16-bit DAC for PMU levels**
- **Typically <±1.5 mV INL (calibrated) linearity in FV mode**

HVOUT output buffer
- **0 V to 13.5 V output range**

Packages
- **84-ball, 9 mm × 9 mm, flip-chip BGA**
- **100-lead TQFP_EP**

1.7 W per channel with no load

APPLICATIONS

Automatic test equipment
Semiconductor test systems
Board test systems
Instrumentation and characterization equipment

GENERAL DESCRIPTION

The ADATE302-02 is a complete, single-chip solution that performs the pin electronic functions of the driver, the comparator, and the active load (DCL), per pin PMU, and dc levels for ATE applications. The device also contains an HVOUT driver with a VHH buffer capable of generating up to 13.5 V.

The driver features three active states: data high mode, data low mode, and term mode, as well as an inhibit state. The inhibit state, in conjunction with the integrated dynamic clamp, facilitates the implementation of a high speed active termination. The output voltage range is −2.0 V to +6.0 V to accommodate a wide variety of test devices.

The ADATE302-02 can be used as either a dual single-ended drive/receive channel or a single differential drive/receive channel. Each channel of the ADATE302-02 features a high speed window comparator for functional testing as well as a per pin PMU with FV or FI and MV or MI functions. All necessary dc levels for DCL functions are generated by on-chip 14-bit DACs. The per pin PMU features an on-chip 16-bit DAC for high accuracy and contains integrated range resistors to minimize external component counts.

The ADATE302-02 uses a serial bus to program all functional blocks and has an on-board temperature sensor for monitoring the device temperature.

Rev. A
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6/08—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

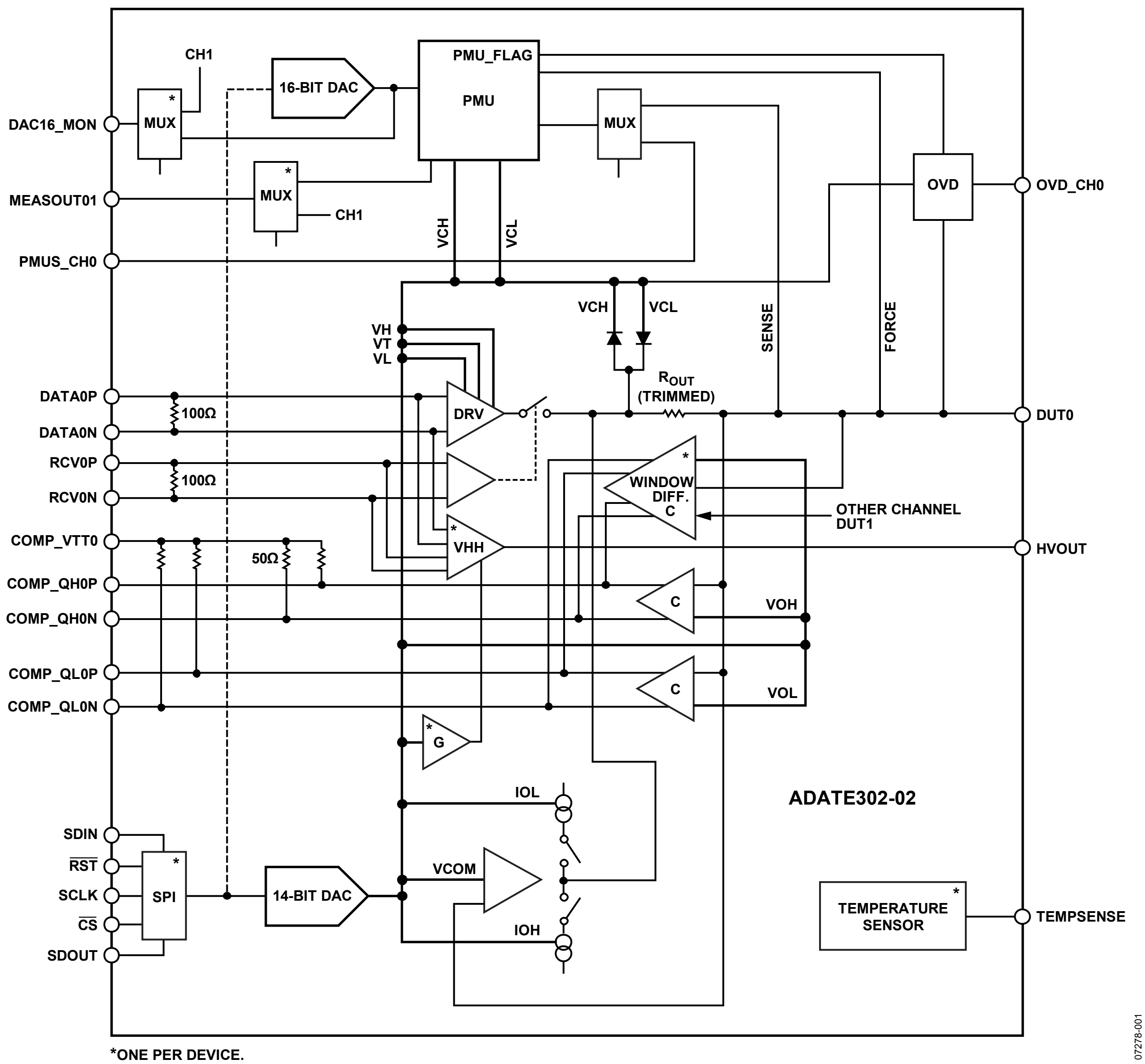


Figure 1. Functional Block Diagram with One of Two Channels Shown

SPECIFICATIONS

V_{DD} = 10.0 V, V_{CC} = 3.3 V, V_{SS} = −5.75 V, V_{PLUS} = 16.75 V, V_{COMP_VTTx} = 1.5 V, V_{REF} = 5.0 V, V_{REF_GND} = 0.0 V. All default test conditions are as defined in Table 38. All specified values are at T_J = 80°C, where T_J corresponds to the internal temperature sensor, unless otherwise noted. Temperature coefficients are measured at T_J = 80°C ± 20°C, unless otherwise noted. Typical values are based on design, simulation analyses, and/or limited bench evaluations. Typical values are not tested or guaranteed. Test levels are specified in the Explanation of Test Levels section.

TOTAL FUNCTION

Table 1.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
TOTAL FUNCTION						
Output Leakage Current						
PE Disable, Range E	−20.0	+6.0	+20.0	nA	P	−2.0 V < V_{DUTx} < +6.0 V; PMU and PE disabled via SPI; VCH = 7.0 V, VCL = −2.5 V
PE Disable, Range A, B, C, D		7.5		nA	C_T	−2.0 V < V_{DUTx} < +6.0 V; PMU and PE disabled via SPI; VCH = 7.0 V, VCL = −2.5 V
High-Z Mode	−400	+15	+400	nA	P	−2.0 V < V_{DUTx} < +6.0 V; PMU disabled and PE enabled via SPI; RCVx pins active, VCH = 7.0 V, VCL = −2.5V
Output Capacitance		4		pF	S	VTERM mode operation
DUT Pin Range	−2.0		+6.0	V	D	
POWER SUPPLIES						
Total Supply Range, V_{PLUS} to V_{SS}		22.5	23.25	V	D	Defines PSRR conditions
VPLUS Supply, V_{PLUS}	16.25	16.75	17.25	V	D	Defines PSRR conditions
Positive Supply, V_{DD}	9.5	10.0	10.5	V	D	Defines PSRR conditions
Negative Supply, V_{SS}	−6.0	−5.75	−5.5	V	D	Defines PSRR conditions
Logic Supply, V_{CC}	3.1	3.3	3.5	V	D	Defines PSRR conditions
Comparator Termination, V_{COMP_VTTx}	1	1.5	3.3	V	D	
V_{PLUS} Supply Current, I_{PLUS}	−1.0	+1.3	+4.0	mA	P	HVOUT disabled
V_{PLUS} Supply Current, I_{PLUS}	4.0	12.7	17.0	mA	P	HVOUT enabled, RCVx pins active, no load, VHH = 12 V
Logic Supply Current, I_{CC}	1.0	2.7	10.0	mA	P	Quiescent (SPI is static)
Comparator Termination Current, I_{COMP_VTTx}	40.0	46	70.0	mA	P	
Positive Supply Current, I_{DD}	140.0	190	256.0	mA	P	Load power down (IOH = IOL = 0 mA)
	170.0	231	311.0	mA	P	Load active off (IOH = IOL = 12 mA)
Negative Supply Current, I_{SS}	200.0	272	406.0	mA	P	Load power down (IOH = IOL = 0 mA)
	230.0	311	461.0	mA	P	Load active off (IOH = IOL = 12 mA)
Total Power Dissipation	2.5	3.55	4.0	W	P	Load power down (IOH = IOL = 0 mA)
	3.0	4.2	5.5	W	P	Load active off (IOH = IOL = 12 mA)
TEMPERATURE MONITORS						
Temperature Sensor Gain		10		mV/K	C_T	
Temperature Sensor Accuracy Without Calibration over 25°C to 100°C		6		°C	C_T	Temperature voltage available on Pin A1 at all times and on Pin K1 when selected (see Table 25 and Table 37)
VREF INPUT						
Reference Input Voltage Range for DACs (VREF Pin)	4.95	5	5.05	V	D	Referenced to V_{REF_GND}; not referenced to V_{DUTGND}
Input Bias Current		0.08	100	µA	P	Tested with 5 V applied

DRIVER

VH − VL ≥ 200 mV (to meet dc/ac specifications).

Table 2.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
DC SPECIFICATIONS						
High-Speed Differential Logic Input Characteristics (DATAx, RCVx)						
Input Termination Resistance	92	100	108	Ω	P	Push 6 mA into xP pins, force 1.3 V on xN pins; measure voltage from xP to xN, calculate resistance (V/I)
Input Voltage Differential	0.2		1.0	V	P_F	
Common-Mode Voltage	0.85		3.5	V	P_F	
Input Bias Current	−20.0	+4.0	+20.0	µA	P	Each pin tested at 2.85 V and 0.35 V, while other high speed pin left open
Pin Output Characteristics						
Output High Range, VH	−1.9		+6.0	V	D	
Output Low Range, VL	−2.0		+5.9	V	D	
Output Term Range, VT	−2.0		+6.0	V	D	
Functional Amplitude (VH − VL)	0.0	8.0		V	D	Amplitude can be programmed to VH = VL, accuracy specifications apply when VH − VL ≥ 200 mV
DC Output Current Limit Source	75	100	120	mA	P	Driver high, VH = 6.0 V, short DUTx pin to −2.0 V, measure current
DC Output Current Limit Sink	−120	−100	−75	mA	P	Driver low, VL = −2.0 V, short DUTx pin to 6.0 V, measure current
Output Resistance, ±50 mA	45.0	48.5	51.0	Ω	P	Source: driver high, VH = 3.0 V, I_{DUTx} = 1 mA and 50 mA; sink: driver low, VL = 0.0 V, I_{DUTx} = −1 mA and −50 mA; $\Delta V_{DUTx}/\Delta I_{DUTx}$
ABSOLUTE ACCURACY						VH tests done with VL = −2.5 V and VT = −2.5 V; VL tests done with VH = 7.5 V and VT = 7.5 V; VT tests done with VL = −2.5 V and VH = 7.5 V; unless otherwise specified
VH, VL, VT Uncalibrated Accuracy	−300	±75	+300	mV	P	Error measured at calibration points of 0 V and 5 V
VH, VL, VT Offset Tempco		±450		µV/°C	C_T	Measured at calibration points
VH, VL, VT DNL		±1		mV	C_T	After two-point gain/offset calibration
VH, VL, VT INL	−10	±2.5	+10	mV	P	After two-point gain/offset calibration; measured over driver output ranges
VH, VL, VT Resolution		0.6	1	mV	P_F	After two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 0 V and 5 V
DUTGND Voltage Accuracy	−7	±1.3	+7	mV	P	Over ±0.1 V range; measured at end points of VH, VL, and VT functional range
VH, VL, VT Crosstalk		±2		mV	C_T	VL = −2.0 V: VH = −1.9 V → 6.0 V, VT = −2.0 V → 6.0 V; VH = 6.0 V: VL = −2.0 V → 5.9 V, VT = −2.0 V → 6.0 V; VT = 1.5 V: VL = −2.0 V → 5.9 V, VH = −1.9 V → 6.0 V; dc crosstalk on VL, VH, VT output level when other driver DACs are varied
Overall Voltage Accuracy		±10		mV	C_T	Sum of INL, crosstalk, DUTGND, and tempco over ±5°C, after gain/offset calibration
VH, VL, VT DC PSRR		±15		mV/V	C_T	Measured at calibration points
AC SPECIFICATIONS						
Rise/Fall Times						Toggle DATAx pins
0.2 V Programmed Swing		683		ps	C_B	VH = 0.2 V, VL = 0.0 V, terminated; 20% to 80%
1.0 V Programmed Swing		521		ps	C_B	VH = 1.0 V, VL = 0.0 V, terminated; 20% to 80%
1.8 V Programmed Swing	430	524	630	ps	P/C_B	VH = 1.8 V, VL = 0.0 V, terminated; 20% to 80%
2.0 V Programmed Swing		531		ps	C_B	VH = 2.0 V, VL = 0.0 V, terminated; 20% to 80%
3.0 V Programmed Swing		589		ps	C_B	VH = 3.0 V, VL = 0.0 V, terminated; 20% to 80%
3.0 V Programmed Swing		811		ps	C_B	VH = 3.0 V, VL = 0.0 V, unterminated; 10% to 90%
5.0 V Programmed Swing		1105		ps	C_B	VH = 5.0 V, VL = 0.0 V, unterminated; 10% to 90%
Rise to Fall Matching		6		ps	C_B	VH = 1.0 V, VL = 0.0 V, terminated; rise to fall within one channel

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
Minimum Pulse Width						Toggle DATAx pins
2.0 V Programmed Swing		1.2		ns	C_B	VH = 2.0 V, VL = 0.0 V, terminated; timing error ±27 ps
		1.2		ns	C_B	VH = 2.0 V, VL = 0.0 V, terminated; less than 10% amplitude degradation
		1.0		ns	C_B	VH = 2.0 V, VL = 0.0 V, terminated; less than 20% amplitude degradation
Maximum Toggle Rate		500		MHz	C_B	VH = 2.0 V, VH = 0.0 V, terminated, 18% amplitude degradation
Dynamic Performance, Drive (VH to VL and VL to VH)						Toggle DATAx pins
Propagation Delay Time		2.1		ns	C_B	VH = 2.0 V, VL = 0.0 V, terminated
Propagation Delay Tempco		4.5		ps/°C	C_T	VH = 1.8 V, VL = 0.0 V, terminated
Delay Matching						VH = 2.0 V, VL = 0.0 V, terminated
Edge to Edge		41		ps	C_B	Rising vs. falling
Channel to Channel		±15		ps	C_B	Rising vs. rising, falling vs. falling
Delay Change vs. Duty Cycle		±30		ps	C_B	VH = 3.0 V, VL = 0.0 V, terminated; 5% to 95% duty cycle; 1 MHz
Overshoot and Undershoot		48		mV	C_B	VH = 3.0 V, VL = 0.0 V, terminated
Settling Time (VH to VL)						Toggle DATAx pins
To Within 3% of Final Value		1.2		ns	C_B	VH = 3.0 V, VL = 0.0 V, terminated
To Within 1% of Final Value		14		ns	C_B	VH = 3.0 V, VL = 0.0 V, terminated
Dynamic Performance, VTERM (VH or VL to VT and VT to VH or VL)						Toggle RCVx pins
Propagation Delay Time		2.7		ns	C_B	VH = 3.0 V, VT = 1.5 V, VL = 0.0 V, terminated
Delay Matching, Edge to Edge		59		ps	C_B	VH = 3.0 V, VT = 1.5 V, VL = 0.0 V, terminated; rising vs. falling
Propagation Delay Tempco		5.5		ps/°C	C_T	VH = 3.0 V, VT = 1.5 V, VL = 0.0 V, terminated
Transition Time, Active to VT, VT to Active		0.614		ns	C_B	VH = 3.0 V, VT = 1.5 V, VL = 0.0 V, terminated; 20% to 80%
Dynamic Performance, Inhibit (VH or VL to/from Inhibit)						Toggle RCVx pins
Propagation Delay Time						VH = +1.0 V, VL = −1.0 V, terminated
Active to Inhibit		2.7		ns	C_B	
Inhibit to Active		3.7		ns	C_B	
Transition Time						VH = +1.0 V, VL = −1.0 V, terminated; 20% to 80%
Active to Inhibit		1.3		ns	C_B	
Inhibit to Active		0.4		ns	C_B	
I/O Spike		157		mV	C_B	VH = 0.0 V, VL = 0.0 V, terminated

REFLECTION CLAMP

Clamp accuracy specifications apply when VCH > VCL.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
VCH						
Range	−1.0		+6.0	V	D	
Uncalibrated Accuracy	−200	±45	+200	mV	P	Driver high-Z, sinking 1 mA; VCH error measured at calibration points of 0 V and 5 V
Resolution		0.6	0.75	mV	P_F	Driver high-Z, sinking 1 mA; after two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 0 V and 5 V
DNL		±1		mV	C_T	Driver high-Z, sinking 1 mA; after two-point gain/offset calibration
INL	−40	±2	+40	mV	P	Driver high-Z, sinking 1 mA; after two-point gain/offset calibration; measured over VCH range of −1 V to +6 V
Tempco		−0.5		mV/°C	C_T	Measured at calibration points
VCL						
Range	−2		+5.0	V	D	
Uncalibrated Accuracy	−200	±70	+200	mV	P	Driver high-Z, sourcing 1 mA; VCL error measured at calibration points of 0 V and 5 V
Resolution		0.6	0.75	mV	P_F	Driver high-Z, sourcing 1 mA; after two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 0 V and 5 V
DNL		±1		mV	C_T	Driver high-Z, sourcing 1 mA; after two-point gain/offset calibration
INL	−40	±2	+40	mV	P	Driver high-Z, sourcing 1 mA; after two-point gain/offset calibration; measured over VCL range of −2 V to +5 V
Tempco		0.6		mV/°C	C_T	Measured at calibration points
DC CLAMP CURRENT LIMIT						
VCH	−120	−83	−60	mA	P	Driver high-Z, VCH = 0 V, VCL = −2.0 V, V_{DUTx} = 5 V
VCL	60	86	120	mA	P	Driver high-Z, VCH = 6.0 V, VCL = 5.0 V, V_{DUTx} = 0.0 V
DUTGND VOLTAGE ACCURACY	−7	±1	+7	mV	P	Over ±0.1 V range; measured at the end points of VCH and VCL functional range

NORMAL WINDOW COMPARATOR

VOH tests done with VOL = −2.0 V, VOL tests done with VOH = 6.0 V, unless otherwise specified.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Range	−2.0		+6.0	V	D	
Differential Voltage Range	±0.1		±8.0	V	D	
Comparator Input Offset Voltage Accuracy, Uncalibrated	−150	±30	+150	mV	P	Offset measured at calibration points of 0 V and 5 V
Comparator Threshold Resolution		0.61	1	mV	P_F	After two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 0 V and 5 V
Comparator Threshold DNL		±1		mV	C_T	After two-point gain/offset calibration
Comparator Threshold INL	−7	±1.2	+7	mV	P	After two-point gain/offset calibration; measured over VOH, VOL range of −2.0 V to +6.0 V
Comparator Input Offset Voltage Tempco		±200		μV/°C	C_T	Measured at calibration points

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
DUTGND Voltage Accuracy	−7	±0.5	+7	mV	P	Over ±0.1 V range; measured at end points of VOH and VOL functional range
Comparator Uncertainty Range		5.3		mV	C_B	V_{DUTx} = 0 V, sweep comparator threshold to determine uncertainty region
DC Hysteresis		0.5		mV	C_B	V_{DUTx} = 0 V
DC PSRR		±5		mV/V	C_T	Measured at calibration points
Digital Output Characteristics						
Internal Pull-Up Resistance to Comparator, COMP_VTTx Pin	46	50	54	Ω	P	Pull 1 mA and 10 mA from Logic 1 leg and measure ΔV to calculate resistance; measured ΔV/9 mA; done for both comparator logic states
V_{COMP_VTTx} Range	1	1.5	3.3	V	D	
Common-Mode Voltage		V_{COMP_VTTx} − 0.3		V	C_T	Measured with 100 Ω differential termination
	V_{COMP_VTTx} − 0.5		V_{COMP_VTTx}	V	P	Measured with no external termination
Differential Voltage		250		mV	C_T	Measured with 100 Ω differential termination
	450	500	550	mV	P	Measured with no external termination
Rise/Fall Time, 20% to 80%		222		ps	C_B	Measured with each comparator leg terminated 50 Ω to GND
AC SPECIFICATIONS						Input transition time = 600 ps, 10% to 90%; measured with each comparator leg terminated 50 Ω to GND; unless otherwise specified
Propagation Delay, Input to Output		1.4		ns	C_B	V_{DUTx} = 0 V to 1.0 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.5 V, VOL = −2.0 V; low-side measurement: VOH = 6.0 V, VOL = 0.5 V
Propagation Delay Tempco		4		ps/°C	C_T	V_{DUTx} = 0 V to 0.9 V swing, driver VTERM mode, VT = 0.0 V; VOL = VOH = 0.45 V
Propagation Delay Matching						V_{DUTx} = 0 V to 1.0 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.5 V, VOL = −2.0 V; low-side measurement: VOH = 6.0 V, VOL = 0.5 V
High Transition to Low Transition		39		ps	C_B	
High to Low Comparator		±30		ps	C_B	
Propagation Delay Change with Respect to						
Slew Rate, 600 ps and 1 ns (10% to 90%)		19		ps	C_B	V_{DUTx} = 0 V to 0.5 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.25 V, VOL = −2.0 V; low-side measurement: VOH = 6.0 V, VOL = 0.25 V
Overdrive, 250 mV and 1.0 V		65		ps	C_B	For 250 mV: V_{DUTx} = 0 V to 0.5 V swing; for 1.0 V: V_{DUTx} = 0 V to 1.25 V swing; driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.25 V, VOL = −2.0 V; low-side measurement: VOH = 6.0 V, VOL = 0.25 V; input transition time = 400 ps (10%/90%)
Pulse Width, 1 ns, 5 ns, 10 ns, and 15 ns		27		ps	C_B	V_{DUTx} = 0 V to 1.0 V swing @ 32.0 MHz, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.5 V, VOL = −2.0 V; low-side measurement: VOH = 6.0 V, VOL = 0.5 V; input transition time = 400 ps (10%/90%)
Duty Cycle, 5% to 95%		11.8		ps	C_B	V_{DUTx} = 0 V to 1.0 V swing @ 1.0 MHz, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.5 V, VOL = −2.0 V; low-side measurement: VOH = 6.0 V, VOL = 0.5 V; input transition time = 400 ps (10%/90%)

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
Minimum Pulse Width		1		ns	C_B	V_{DUTx} = 0 V to 1.0 V swing, driver VTERM mode, VT = 0.0 V; less than 10% amplitude degradation measured by shmoo; input transition time = 400 ps (10%/90%)
Input Equivalent Bandwidth, Terminated		1000		MHz	C_B	V_{DUTx} = 0 V to 1.0 V swing, driver VTERM mode, VT = 0.0 V; as measured by shmoo; input transition time = 400 ps (10%/90%)
ERT High-Z Mode, 3 V, 20% to 80%		0.9		ns	C_B	V_{DUTx} = 0 V to 3.0 V swing, driver high-Z; as measured by shmoo

DIFFERENTIAL COMPARATOR

VOH tests done with VOL = −1.1 V, VOL tests done with VOH = 1.1 V, unless otherwise specified.

Table 5.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Range	−1.5		+4.5	V	D	
Operational Differential Voltage Range	±0.05		±1.1	V	D	
Maximum Differential Voltage Range			±8	V	D	
Comparator Input Offset Voltage Accuracy, Uncalibrated	−150	±25	+150	mV	P	Offset measured at differential calibration points of +1 V and −1 V, with common mode = 0 V
VOH, VOL Resolution		0.61	1	mV	P_F	After two-point gain/offset calibration; range/number of DAC bits as measured at differential calibration points of +1 V and −1 V, with common mode = 0 V
VOH, VOL DNL		±1		mV	C_T	After two-point gain/offset calibration; common mode = 0 V
VOH, VOL INL	−7	±1.0	+7	mV	P	After two-point gain/offset calibration; measured over VOH, VOL range of −1.1 V to +1.1 V, common mode = 0 V
VOH, VOL Offset Voltage Tempco		±200		μV/°C	C_T	Measured at calibration points
Comparator Uncertainty Range		18		mV	C_B	V_{DUTx} = 0 V, sweep comparator threshold to determine uncertainty region
DC Hysteresis		0.5		mV	C_B	V_{DUTx} = 0 V
CMRR			1	mV/V	P	Offset measured at common-mode voltage points of −1.5 V and +4.5 V, with differential voltage = 0 V
DC PSRR		±15		mV/V	C_T	Measured at calibration points
AC SPECIFICATIONS						Input transition time = 600 ps, 10% to 90%, measured with each comparator leg terminated 50 Ω to GND
Propagation Delay, Input to Output		1.4		ns	C_B	V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.0 V, VOL = −1.1 V; low-side measurement: VOH = 1.1 V, VOL = 0.0 V; repeat for other DUT channel
Propagation Delay Tempco		4		ps/°C	C_T	V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing, driver VTERM mode, VT = 0.0 V; VOL = VOH = 0.0 V; repeat for other DUT channel
Propagation Delay Matching						V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.0 V, VOL = −1.1 V; low-side measurement: VOH = 1.1 V, VOL = 0.0 V; repeat for other DUT channel
High Transition to Low Transition		27		ps	C_B	
High to Low Comparator		±32		ps	C_B	
Propagation Delay Change with Respect to						V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.0 V, VOL = −1.1 V; low-side measurement: VOH = 1.1 V,

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
						VOL = 0.0 V; repeat for other DUT channel
Slew Rate, 400 ps and 1 ns (10% to 90%)		25		ps	C_B	V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.0 V, VOL = −1.1 V; low-side measurement: VOH = 1.1 V, VOL = 0.0 V; repeat for other DUT channel
Overdrive, 250 mV and 750 mV		79		ps	C_B	V_{DUT0} = 0 V, for 250 mV: V_{DUT1} = 0 V to 0.5 V swing; for 750 mV: V_{DUT1} = 0 V to 1.0 V swing, driver VTERM mode, VT = 0.0 V; VOH = −0.25 V; repeat for other DUT channel with comparator threshold = 0.25 V
Pulse Width, 1 ns, 5 ns, 10 ns, and 15 ns		56		ps	C_B	V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing @ 32 MHz, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.0 V, VOL = −1.1 V; low-side measurement: VOH = 1.1 V, VOL = 0.0 V; repeat for other DUT channel
Duty Cycle, 5% to 95%		16		ps	C_B	V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing @ 32 MHz, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.0 V, VOL = −1.1 V; low-side measurement: VOH = 1.1 V, VOL = 0.0 V; repeat for other DUT channel
Minimum Pulse Width		1		ns	C_B	V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.0 V, VOL = −1.1 V; low-side measurement: VOH = 1.1 V, VOL = 0.0 V; less than 22% amplitude degradation measured by shmoo; repeat for other DUT channel
Input Equivalent Bandwidth, Terminated		500		MHz	C_B	V_{DUT0} = 0 V, V_{DUT1} = −0.5 V to +0.5 V swing, driver VTERM mode, VT = 0.0 V; high-side measurement: VOH = 0.0 V, VOL = −1.1 V; low-side measurement: VOH = 1.1 V, VOL = 0.0 V

ACTIVE LOAD

See Table 30 for load control information.

Table 6.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
DC SPECIFICATIONS						Load active on, RCVx pins active, unless otherwise noted
Input Characteristics						
VCOM Voltage Range	−1.75		+5.75	V	D	
V_{DUTx} Range	−2.0		+6.0	V	D	
VCOM Accuracy, Uncalibrated	−200	±25	+200	mV	P	IOH = IOL = 6 mA, VCOM error measured at calibration points of 0 V and 5 V
VCOM Resolution		0.61	1	mV	P_F	IOH = IOL = 6 mA, after two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 0 V and 5 V
VCOM DNL		±1		mV	C_T	IOH = IOL = 6 mA, after two-point gain/offset calibration
VCOM INL	−7	±2	+7	mV	P	IOH = IOL = 6 mA, after two-point gain/offset calibration; measured over VCOM range of −1.75 V to +5.75 V
DUTGND Voltage Accuracy	−7	±1	+7	mV	P	Over ±0.1 V range; measured at end points of VCOM functional range
Output Characteristics						
IOL						
Maximum Source Current	12			mA	D	
Uncalibrated Offset	−600.0	±100	+600.0	μA	P	IOH = 0 mA, VCOM = 1.5 V, V_{DUTx} = 0.0 V, IOL offset calculated from calibration points of 1 mA and 11 mA
Uncalibrated Gain	−12	±1	+12	%	P	IOH = 0 mA, VCOM = 1.5 V, V_{DUTx} = 0.0 V, IOL gain calculated from calibration points of 1 mA and 11 mA
Resolution		1.5	2	μA	P_F	IOH = 0 mA, VCOM = 1.5 V, V_{DUTx} = 0.0 V, after two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 1 mA and 11 mA
DNL		±3.0		μA	C_T	IOH = 0 mA, VCOM = 1.5 V, V_{DUTx} = 0.0 V, after two-point gain/offset calibration
INL	−70	±20	+70	μA	P	IOH = 0 mA, VCOM = 1.5 V, V_{DUTx} = 0.0 V, after two-point gain/offset calibration; measured over IOL range of 0 mA to 12 mA
90% Commutation Voltage			0.25	V	P	IOH = IOL = 12 mA, VCOM = 2.0 V, measure IOL reference at V_{DUTx} = −1.0 V, measure IOL current at V_{DUTx} = 1.75 V, ensure >90% of reference current
IOH						
Maximum Sink Current	12			mA	D	
Uncalibrated Offset	−600.0	±100	+600.0	μA	P	IOL = 0 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, IOH offset calculated from calibration points of 1 mA and 11 mA
Uncalibrated Gain	−12	±1	+12	%	P	IOL = 0 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, IOH gain calculated from calibration points of 1 mA and 11 mA
Resolution		1.5	2	μA	P_F	IOL = 0 mA, VCOM = 1.5 V, V_{DUTx} = 3.0 V, after two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 1 mA and 11 mA
DNL		±3.0		μA	C_T	IOL = 0 mA, VCOM = 1.5V, V_{DUTx} = 3.0 V, after two-point gain/offset calibration
INL	−70	±20	+70	μA	P	IOL = 0 mA, VCOM = 1.5V, V_{DUTx} = 3.0 V, after two-point gain/offset calibration; measured over IOH range of 0 mA to 12 mA
90% Commutation Voltage			0.25	V	P	IOH = IOL = 12 mA, VCOM = 2.0 V, measure IOH reference at V_{DUTx} = 5.0 V, measure IOH current at V_{DUTx} = 2.25 V, ensure >90% of reference current
Output Current Tempco		±1.5		μA/°C	C_T	Measured at calibration points

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
AC SPECIFICATIONS						Load active on, unless otherwise noted
Dynamic Performance						
Propagation Delay, Load Active On to Load Active Off; 50%, 90%		4.1		ns	C_B	Toggle RCVx pins, DUTx terminated 50 Ω to GND, IOH = IOL = 12 mA, VH = VL = 0 V, VCOM = +1.25 V for IOL and VCOM = −1.25 V for IOH; measured from 50% point of RCVxP − RCVxN to 90% point of final output, repeat for drive low and high
Propagation Delay, Load Active Off to Load Active On; 50%, 90%		11		ns	C_B	Toggle RCVx pins, DUTx terminated 50 Ω to GND, IOH = IOL = 12 mA, VH = VL = 0 V, VCOM = +1.25 V for IOL and VCOM = −1.25 V for IOH; measured from 50% point of RCVxP − RCVxN to 90% point of final output, repeat for drive low and high
Propagation Delay Matching		6.9		ns	C_B	Toggle RCVx pins, DUTx terminated 50 Ω to GND, IOH = IOL = 12 mA, VH = VL = 0 V, VCOM = +1.25 V for IOL and VCOM = −1.25 V for IOH; active on vs. active off, repeat for drive low and high
Load Spike		156		mV	C_B	Toggle RCVx pins, DUTx terminated 50 Ω to GND, IOH = IOL = 0 mA, VH = VL = 0 V, VCOM = +1.25 V for IOL and VCOM = −1.25 V for IOH; repeat for drive low and high
Settling Time to 90%		1.6		ns	C_B	Toggle RCVx pins, DUTx terminated 50 Ω to GND, IOH = IOL = 12 mA, VH = VL = 0 V, VCOM = +1.25 V for IOL and VCOM= −1.25 V for IOH; measured at 90% of final value

PMU

FV = force voltage, MV = measure voltage, FI = force current, MI = measure current, FN = force nothing.

Table 7.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
FORCE VOLTAGE (FV)						
Current Range A	±25			mA	D	
Current Range B	±2			mA	D	
Current Range C	±200			μA	D	
Current Range D	±20			μA	D	
Current Range E	±2			μA	D	
Force Input Voltage Range at Output For All Ranges	−2.0		+6.0	V	D	
Force Voltage Uncalibrated Accuracy for Range C	−100	±25	+100	mV	P	PMU enabled, FV, PE disabled, error measured at calibration points of 0 V and 5 V
Force Voltage Uncalibrated Accuracy for All Ranges		±25		mV	C_T	PMU enabled, FV, PE disabled, error measured at calibration points of 0 V and 5 V; repeat for each PMU current range
Force Voltage Offset Tempco for All Ranges		±25		μV/°C	C_T	Measured at calibration points for each PMU current range
Force Voltage Gain Tempco for All Ranges		±75		ppm/°C	C_T	Measured at calibration points for each PMU current range
Forced Voltage INL	−7	±2	+7	mV	P	PMU enabled, FV, Range C, PE disabled, after two-point gain/offset calibration; measured over output range of −2.0 V to +6.0 V
Force Voltage Compliance vs. Current Load						PMU enabled, FV, PE disabled, force −2.0 V, measure voltage while PMU sinking zero- and full-scale current; measure ΔV; force 6.0 V, measure voltage while PMU sourcing zero- and full-scale current; measure ΔV; repeat for each PMU current range
Range A		±4		mV	C_T	
Range B to Range E		±1		mV	C_T	

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
Current Limit, Source and Sink						
Range A	108	135	180	% FS	P	PMU enabled, FV, PE disabled; sink: force 2.5 V, short DUTx to 6.0 V; source: force 2.5 V, short DUTx to −1.0 V; Range A FS = 25 mA, 108% FS = 27 mA, 180% FS = 45 mA
Range B to Range E	120	140	180	% FS	P	PMU enabled, FV, PE disabled; sink: force 2.5 V, short DUTx to 6.0 V; source: force 2.5 V, short DUTx to −1.0 V; repeat for each PMU current range; example: Range B FS = 2 mA, 120% FS = 2.4 mA, 180% FS = 3.6 mA
DUTGND Voltage Accuracy	−7	±1	+7	mV	P	Over ±0.1 V range; measured at end points of FV functional range
MEASURE CURRENT (MI)						V_{DUTx} externally forced to 0.0 V, unless otherwise specified; ideal MEASOUT transfer functions: $V_{MEASOUT01}$ [V] = ($I_{MEASOUT01}$ × 5/FSR) + 2.5 + V_{DUTGND} I($V_{MEASOUT01}$) [A] = ($V_{MEASOUT01}$ − V_{DUTGND} − 2.5) × FSR/5
Measure Current, Pin DUTx Voltage Range for All Ranges	−2.0		+6.0	V	D	
Measure Current Uncalibrated Accuracy						
Range A		±650		µA	C_T	PMU enabled, FIMI, PE disabled, error at calibration points of −20 mA and 20 mA, error = (I($V_{MEASOUT01}$) − I_{DUTx})
Range B	−400	±20	+400	µA	P	PMU enabled, FIMI, PE disabled, error at calibration points of −1.6 mA and 1.6 mA, error = (I($V_{MEASOUT01}$) − I_{DUTx})
Range C		± 2.00		µA	C_T	PMU enabled, FIMI, PE disabled, error at calibration points of ±80% FS, error = (I($V_{MEASOUT01}$) − I_{DUTx})
Range D		±0.20		µA	C_T	PMU enabled, FIMI, PE disabled, error at calibration points of ±80% FS, error = (I($V_{MEASOUT01}$) − I_{DUTx})
Range E		±0.02		µA	C_T	PMU enabled, FIMI, PE disabled, error at calibration points of ±80% FS, error = (I($V_{MEASOUT01}$) − I_{DUTx})
Measure Current Offset Tempco						
Range A		±2.5		µA/°C	C_T	Measured at calibration points
Range B		±125		nA/°C	C_T	Measured at calibration points
Range C		±20		nA/°C	C_T	Measured at calibration points
Range D and Range E		±4		nA/°C	C_T	Measured at calibration points
Measure Current Gain Error, Nominal Gain = 1						
Range A		−3.5		%	C_T	PMU enabled, FIMI, PE disabled, gain error from calibration points of ±80% FS
Range B	−20	±2	+20	%	P	PMU enabled, FIMI, PE disabled, gain error from calibration points of ±1.6 mA
Range C to Range E		±2		%	C_T	PMU enabled, FIMI, PE disabled, gain error from calibration points of ±80% FS
Measure Current Gain Tempco						Measured at calibration points
Range A		±300		ppm/°C	C_T	
Range B to Range E		±50		ppm/°C	C_T	
Measure Current INL						
Range A		±0.05		% FSR	C_T	PMU enabled, FIMI, PE disabled, after two-point gain/offset calibration, measured over FSR output of −25 mA to +25 mA
Range B	−0.02	±0.005	0.02	% FSR	P	PMU enabled, FIMI, PE disabled, after two-point gain/offset calibration measured over FSR output of −2 mA to +2 mA
Range B to Range E		±0.005		% FSR	C_T	PMU enabled, FIMI, PE disabled, after two-point gain/offset calibration; measured over FSR output
FVMI DUT Pin Voltage Rejection	−0.01		0.01	% FSR/V	P	PMU enabled, FVMI, PE disabled, force −1 V and +5 V into load of 1 mA; measure ΔI reported at MEASOUT01
DUTGND Voltage Accuracy		±2.5		mV	C_T	Over ±0.1 V range; measured at end points of MI functional range

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
FORCE CURRENT (FI)						V_{DUTx} externally forced to 0.0 V, unless otherwise specified Ideal force current transfer function: I_{FORCE} = (PMUDAC − 2.5) × (FSR/5)
Force Current, DUTx Pin Voltage Range for All Ranges	−2.0		+6.0	V	D	
Force Current Uncalibrated Accuracy						
Range A	−5.0	±0.5	+5.0	mA	P	PMU enabled, FIMI, PE disabled, error at calibration points of −20 mA and +20 mA
Range B	−400	±40	+400	µA	P	PMU enabled, FIMI, PE disabled, error at calibration points of −1.6 mA and +1.6 mA
Range C	−40	±4	+40	µA	P	PMU enabled, FIMI, PE disabled, error at calibration points of ±80% FS
Range D	−4	±0.4	+4	µA	P	PMU enabled, FIMI, PE disabled, error at calibration points of ±80% FS
Range E	−400	±75	+400	nA	P	PMU enabled, FIMI, PE disabled, error at calibration points of ±80% FS
Force Current Offset Tempco						
Range A		±1		µA/°C	C_T	Measured at calibration points
Range B		±80		nA/°C	C_T	Measured at calibration points
Range C to Range E		±4		nA/°C	C_T	Measured at calibration points
Forced Current Gain Error, Nominal Gain = 1	−20	±4	+20	%	P	PMU enabled, FIMI, PE disabled, gain error from calibration points of ±80% FS
Forced Current Gain Tempco						Measured at calibration points
Range A		−500		ppm/°C	C_T	
Range B to Range E		±75		ppm/°C	C_T	
Force Current INL						
Range A	−0.3	±0.05	+0.3	% FSR	P	PMU enabled, FIMI, PE disabled, after two-point gain/offset calibration; measured over FSR output of −25 mA to +25 mA
Range B to Range E	-0.2	±0.015	0.2	% FSR	P	PMU enabled, FIMI, PE disabled, after two-point gain/offset calibration; measured over FSR output
Force Current Compliance vs. Voltage Load						PMU enabled, FIMV, PE disabled; force positive full-scale current driving −2.0 V and +6.0 V, measure ΔI @ DUTx pin; force negative full-scale current driving −2.0 V and +6.0 V, measure ΔI @ DUTx pin
Range A to Range D	−0.6	±0.06	+0.6	% FSR	P	
Range E	−1.0	+±0.1	+1.0	% FSR	P	
MEASURE VOLTAGE						
Measure Voltage Range	−2.0		+6.0	V	D	
Measure Voltage Uncalibrated Accuracy	−25	±2.0	+25	mV	P	PMU enabled, FVMV, Range B, PE disabled, error at calibration points of 0 V and 5 V, error = ($V_{MEASOUT01}$ − V_{DUTx})
Measure Voltage Offset Tempco		±10		µV/°C	C_T	Measured at calibration points
Measure Voltage Gain Error	−2	±0.01	+2	%	P	PMU enabled, FVMV, Range B, PE disabled, gain error from calibration points of 0 V and 5 V
Measure Voltage Gain Tempco		25		ppm/°C	C_T	Measured at calibration points
Measure Voltage INL	−7	±1	+7	mV	P	PMU enabled, FVMV, Range B, PE disabled, after two-point gain/offset calibration; measured over output range of −2.0 V to +6.0 V
Rejection of Measure V vs. I_{DUTx}	−1.5	±0.1	+1.5	mV	P	PMU enabled, FVMV, Range D, PE disabled, force 0 V into load of −10 µA and +10 µA; measure ΔV reported at MEASOUT01

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
MEASOUT01 DC CHARACTERISTICS						
MEASOUT01 Voltage Range	−2.0		+6.0	V	D	
DC Output Current			4	mA	D	
MEASOUT01 Pin Output Impedance		25	200	Ω	P	PMU enabled, FVMV, PE disabled; source resistance: PMU force 6.0 V and load with 0 mA and 4 mA; sink resistance: PMU force −2.0 V and load with 0 mA and −4 mA; resistance = ΔV/ΔI at MEASOUT01 pin
Output Leakage Current When Tristated	−1		+1	µA	P	Tested at −2.0 V and +6.0 V
Output Short-Circuit Current	−25		+25	mA	P	PMU enabled, FVMV, PE disabled; source: PMU force 6.0 V, short MEASOUT01 to −2.0 V; sink: PMU force −2.0 V, short MEASOUT01 to 6.0 V
VOLTAGE CLAMPS						
Low Clamp Range (VCL)	−2.0		+4.0	V	D	
High Clamp Range (VCH)	0.0		6.0	V	D	
Positive Clamp Voltage Droop	−300	+50	+300	mV	P	PMU enabled, FIMI, Range A, PE disabled, PMU clamps enabled, VCH = 5 V, VCL = −1 V, PMU force 1 mA and 25 mA into open; ΔV seen at DUTx pin
Negative Clamp Voltage Droop	−300	−50	+300	mV	P	PMU enabled, FIMI, Range A, PE disabled, PMU clamps enabled, VCH = 5 V, VCL = −1 V, PMU force −1 mA and −25 mA into open; ΔV seen at DUTx pin
Uncalibrated Accuracy	−250	±100	+250	mV	P	PMU enabled, FIMI, Range B, PE disabled, PMU damps enabled, PMU force ±1 mA into open; VCH errors at calibration points of 0 V and 5 V; VCL errors at the calibration points of 0 V and 4 V
INL	−70	±5	+70	mV	P	PMU enabled, FIMI, Range B, PE disabled, PMU damps enabled, PMU force ±1 mA into open; after two-point gain/offset calibration; measured over PMU clamp range
DUTGND Voltage Accuracy		±1		mV	C_T	Over ±0.1 V range; measured at end points of PMU clamp functional range
SETTLING/SWITCHING TIMES						SCAP = 330 pF, FFCAP = 220 pF
Voltage Force Settling Time to 0.1% of Final Value						PMU enabled, FV, PE disabled, program PMUDAC steps of 500 mV and 5.0 V; simulation of worst case, 2000 pF load, PMUDAC step of 5.0 V
Range A, 200 pF and 2000 pF Load		15		µs	S	
Range B, 200 pF and 2000 pF Load		20		µs	S	
Range C, 200 pF and 2000 pF Load		124		µs	S	
Range D, 200 pF and 2000 pF Load		1015		µs	S	
Range E, 200 pF and 2000 pF Load		3455		µs	S	
Voltage Force Settling Time to 1.0% of Final Value						PMU enabled, FV, PE disabled, start with PMUDAC programmed to 0.0 V, program PMUDAC to 500 mV
Range A, 200 pF and 2000 pF Load		8.0		µs	C_B	
Range B, 200 pF and 2000 pF Load		8.0		µs	C_B	
Range C, 200 pF and 2000 pF Load		8.0		µs	C_B	
Range D, 200 pF Load		8.1		µs	C_B	
Range D, 2000 pF Load		585		µs	C_B	
Range E, 200 pF Load		8.1		µs	C_B	
Range E, 2000 pF Load		590		µs	C_B	

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
Voltage Force Settling Time to 1.0% of Final Value						PMU enabled, FV, PE disabled, start with PMUDAC programmed to 0.0 V, program PMUDAC to 5.0 V
Range A, 200 pF and 2000 pF Load		4.2		µs	C_B	
Range B, 200 pF Load		4.4		µs	C_B	
Range B, 2000 pF Load		7.6		µs	C_B	
Range C, 200 pF Load		6.3		µs	C_B	
Range C, 2000 pF Load		8.1		µs	C_B	
Range D, 200 pF Load		130		µs	C_B	
Range D, 2000 pF Load		280		µs	C_B	
Range E, 200 pF Load		390		µs	C_B	
Range E, 2000 pF Load		605		µs	C_B	
Current Force Settling Time to 0.1% of Final Value						PMU enabled, FI, PE disabled, start with PMUDAC programmed to 0 current, program PMUDAC to FS current
Range A, 200 pF in Parallel with 120 Ω		8.2		µs	S	
Range B, 200 pF in Parallel with 1.5 kΩ		9.4		µs	S	
Range C, 200 pF in Parallel with 15.0 kΩ		30		µs	S	
Range D, 200 pF in Parallel with 150 kΩ		281		µs	S	
Range E, 200 pF in Parallel with 1.5 MΩ		2668		µs	S	
Current Force Settling Time to 1.0% of Final Value						PMU enabled, FI, PE disabled, start with PMUDAC programmed to 0 current, program PMUDAC to FS current
Range A, 200 pF in Parallel with 120 Ω		3.3		µs	C_B	
Range B, 200 pF in Parallel with 1.5 kΩ		4.4		µs	C_B	
Range C, 200 pF in Parallel with 15.0 kΩ		8		µs	C_B	
Range D, 200 pF in Parallel with 150 kΩ		205		µs	C_B	
Range E, 200 pF in Parallel with 1.5 MΩ		505		µs	C_B	
INTERACTION AND CROSSTALK						
Measure Voltage Channel-to-Channel Crosstalk		±0.125		% FSR	C_T	PMU enabled, FIMV, PE disabled, Range B, forcing 0 mA into 0 V load; other channel: Range A, forcing a step of 0 mA to 25 mA into 0 V load; report ΔV of MEASOUT01 pin under test; 0.125% × 8.0 V = 10 mV
Measure Current Channel-to-Channel Crosstalk		±0.01		% FSR	C_T	PMU enabled, FVMI, PE disabled, Range E, forcing 0 V into 0 mA current load; other channel: Range E, forcing a step of 0 V to 5 V into 0 mA current load; report ΔV of MEASOUT01 pin under test; 0.01% × 5.0 V = 0.5 mV

EXTERNAL SENSE (PMUS_CHx)

Table 8.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
Voltage Range	−2.0		+6.0	V	D	
Input Leakage Current	−20		+20	nA	P	Tested at −2.0 V and +6.0 V

DUTGND INPUT

Table 9.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
Input Voltage Range, Referenced to GND	−0.1		+0.1	V	D	
Input Bias Current		1	100	μA	P	Tested at −100 mV and +100 mV

SERIAL PERIPHERAL INTERFACE

Table 10.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
Serial Input Logic High	1.8		V_{CC}	V	P_F	
Serial Input Logic Low	0		0.7	V	P_F	
Input Bias Current	−10	+1	+10	μA	P	Tested at 0.0 V and 3.3 V
SCLK Clock Rate		50		MHz	P_F	
SCLK Pulse Width		9		ns	C_T	
SCLK Crosstalk on DUTx Pin		8		mV	C_B	PE disabled, PMU FV enabled and forcing 0 V
Serial Output Logic High	V_{CC} − 0.4		V_{CC}	V	P_F	Sourcing 2 mA
Serial Output Logic Low	0		0.8	V	P_F	Sinking 2 mA
Update Time		10		μs	D	Maximum delay time required for the part to enter a stable state after a serial bus command is loaded

HVOUT DRIVER

Table 11.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
VHH BUFFER						VHH = (VT + 1 V) × 2 + DUTGND
Voltage Range	5.9		V_{PLUS} − 3.25	V	D	V_{PLUS} = 16.75 V nominal; in this condition, V_{HVOUT} maximum = 13.5 V
Output High	13.5			V	P	VHH mode enabled, RCVx pins active, VHH level = full scale, sourcing 15 mA
Output Low			5.9	V	P	VHH mode enabled, RCVx pins active, VHH level = zero scale, sinking 15 mA
Accuracy Uncalibrated	−500	±100	+500	mV	P	VHH mode enabled, RCVx pins active, V_{HVOUT} error measured at calibration points of 7 V and 12 V
Offset Tempco		1		mV/°C	C_T	Measured at calibration points
Resolution		1.21	1.5	mV	P_F	VHH mode enabled, RCVx pins active, after two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 7 V and 12 V
INL	−30	±15	+30	mV	P	VHH mode enabled, RCVx pins active, after two-point gain/offset calibration; measured over VHH range of 5.9 V to 13.5 V
DUTGND Voltage Accuracy		±1		mV	C_T	Over ±0.1 V range; measured at end points of VHH functional range
Output Resistance		1	10	Ω	P	VHH mode enabled, RCVx pins active, source: VHH = 10.0 V, I_{HVOUT} = 0 mA and 15 mA; sink: VHH = 6.5 V, I_{HVOUT} = 0 mA and −15 mA; ΔV/ΔI
DC Output Current Limit Source	60		100	mA	P	VHH mode enabled, RCVx pins active, VHH = 10.0 V, short HVOUT pin to 5.9 V, measure current
DC Output Current Limit Sink	−100		−60	mA	P	VHH mode enabled, RCVx pins active, VHH = 6.5 V, short HVOUT pin to 14.1 V, measure current
Rise Time (From VL or VH to VHH)		175		ns	C_B	VHH mode enabled, toggle RCVx pins, VHH = 13.5 V, VL = VH = 3.0 V; 20% to 80%, for DATAx high and DATAx low

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
Fall Time (From VHH to VL or VH)		23		ns	C_B	VHH mode enabled, toggle RCVx pins, VHH = 13.5 V, VL = VH = 3.0 V; 20% to 80%, for DATAx high and DATAx low
Preshoot, Overshoot, and Undershoot		±100		mV	C_B	VHH mode enabled, toggle RCVx pins, VHH = 13.5 V, VL = VH = 3.0 V; for DATAx high and DATAx low
VL/VH BUFFER						
Voltage Range	−0.1		+6.0	V	D	
Accuracy Uncalibrated	−500	±100	+500	mV	P	VHH mode enabled, RCVx pins inactive, error measured at calibration points of 0 V and 5 V
Offset Tempco		1		mV/°C	C_T	Measured at calibration points
Resolution		0.61	0.75	mV	P_F	VHH mode enabled, RCVx pins inactive, after two-point gain/offset calibration; range/number of DAC bits as measured at calibration points of 0 V and 5 V
INL	−20	±4	+20	mV	P	VHH mode enabled, RCVx pins inactive, after two-point gain/offset calibration; measured over range of −0.1 V to +6.0 V
DUTGND Voltage Accuracy		±2		mV	C_T	Over ±0.1 V range; measured at end points of VH and VL, functional range
Output Resistance	46	48	50	Ω	P	VHH mode enabled, RCVx pins inactive, source: VH = 3.0 V, I_{HVOUT} = 1 mA and 50 mA; sink: VL = 2.0 V, I_{HVOUT} = −1 mA and −50 mA; ΔV/ΔI
DC Output Current Limit Source	60		100	mA	P	VHH mode enabled, RCVx pins inactive, VH = 6.0 V, short HVOUT pin to −0.1 V, DATAx high, measure current
DC Output Current Limit Sink	−100		−60	mA	P	VHH mode enabled, RCVx pins inactive, VL = −0.1 V, short HVOUT pin to 6.0 V, DATAx low, measure current
Rise Time (VL to VH)		10.0		ns	C_B	VHH mode enabled, RCVx pins inactive, VL = 0.0 V, VH = 3.0 V, toggle DATAx pins; 20% to 80%
Fall Time (VH to VL)		11.3		ns	C_B	VHH mode enabled, RCVx pins inactive, VL = 0.0 V, VH = 3.0 V, toggle DATAx pins; 20% to 80%
Preshoot, Overshoot, and Undershoot		±54		mV	C_B	VHH mode enabled, RCV inactive, VL = 0.0 V, VH = 3.0 V, toggle DATAx pins

OVERVOLTAGE DETECTOR (OVD)

Table 12.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
DC CHARACTERISTICS						
Programmable Voltage Range	−3.0		+7.0	V	D	
Accuracy Uncalibrated	−200		+200	mV	P	OVD offset errors measured at programmed levels of 7.0 V and −3.0 V
Hysteresis		112		mV	C_B	
LOGIC OUTPUT CHARACTERISTICS						
Off State Leakage		10	1000	nA	P	Disable OVD alarm, apply 3.3 V to OVD_CHx pin, measure leakage current
Maximum On Voltage @100 µA		0.2	0.7	V	P	Activate alarm, force 100 µA into OVD_CHx, measure active alarm voltage
Propagation Delay		1.8		µs	C_B	For OVD high: DUTx = 0 V to 6 V swing, OVD_CHx high = 3.0 V, OVD_CHx low = −3.0 V; for OVD_CHx low: DUTx = 0 V to 6 V swing, OVD_CHx high = 7.0 V, OVD_CHx low = 3.0 V

16-BIT DAC MONITOR MUX

Table 13.

Parameter	Min	Typ	Max	Unit	Test Level	Conditions/Comments
DC CHARACTERISTICS						
Programmable Voltage Range	−2.5		+7.5	V	D	
Output Resistance		16		kΩ	C_T	PMUDAC = 0.0 V, FV, I = 0 µA, 200 µA; ΔV/ΔI

ABSOLUTE MAXIMUM RATINGS

Table 14.

Parameter	Rating
Supply Voltages	
Positive Supply Voltage (V_{DD} to GND)	−0.5 V to +11.0 V
Positive V_{CC} Supply Voltage (V_{CC} to GND)	−0.5 V to +4.0 V
Negative Supply Voltage (V_{SS} to GND)	−6.25 V to +0.5 V
Supply Voltage Difference (V_{DD} to V_{SS})	−1.0 V to +16.5 V
Reference Ground (DUTGND to GND)	−0.5 V to +0.5 V
AGND to DGND	−0.5 V to +0.5 V
VPLUS Supply Voltage (V_{PLUS} to GND)	−0.5 V to +17.5 V
Input Voltages	
Input Common-Mode Voltage	V_{SS} to V_{DD}
Short-Circuit Voltage[1]	−3.0 V to +8.0 V
High Speed Input Voltage[2]	0 to V_{CC}
High Speed Differential Input Voltage[3]	0 to V_{CC}
VREF	−0.5 V to +5.5 V
DUTx I/O Pin Current	
DCL Maximum Short-Circuit Current[4]	±140 mA
Temperature	
Operating Temperature, Junction	125°C
Storage Temperature Range	−65°C to +150°C

[1] R_L = 0 Ω, V_{DUTx} continuous short-circuit condition (VH, VL, VT, high-Z, VCOM, clamp modes).
[2] DATAxP, DATAxN, RCVxP, RCVxN, under source R = 0 Ω.
[3] DATAxP to DATAxN, RCVxP, RCVxN.
[4] R_L = 0 Ω, V_{DUTx} = −3 V to +8 V; DCL current limit. Continuous short-circuit condition. ADATE302-02 must current limit and survive continuous short circuit.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 15. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
84-Ball CSP_BGA	31.1	0.51	°C/W

EXPLANATION OF TEST LEVELS

D Definition

S Design verification simulation

P 100% production tested

P_F Functionally checked during production test

C_T Characterized on tester

C_B Characterized on bench

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

	10	9	8	7	6	5	4	3	2	1
A	HVOUT	PMUS_CH0	VSSO_0 (DRIVE)	DUT0	VDDO_0 (DRIVE)	VDDO_1 (DRIVE)	DUT1	VSSO_1 (DRIVE)	PMUS_CH1	TEMPSENSE
B	VPLUS	SCAP0	VSS	AGND	VDD	VDD	AGND	VSS	SCAP1	VDD/VDD_ TMPSNS
C	FFCAP_0B	AGND	DATA0N	VSS	VDD	VDD	VSS	DATA1N	AGND	FFCAP_1B
D	OVD_CH0	VDD	DATA0P					DATA1P	VDD	OVD_CH1
E	FFCAP_0A	VSS	RCV0N					RCV1N	VSS	FFCAP_1A
F	AGND	AGND	RCV0P					RCV1P	AGND	AGND
G	COMP_QL0P	COMP_QL0N	COMP_VTT0					COMP_VTT1	COMP_QL1N	COMP_QL1P
H	COMP_QH0P	COMP_QH0N	AGND	VSS	VDD	VDD	VSS	AGND	COMP_QH1N	COMP_QH1P
J	AGND	AGND	AGND	$\overline{\text{RST}}$	SDIN	DGND	DAC16_MON	AGND	AGND	AGND
K	VREF_GND	VREF	AGND	VCC	SCLK	SDOUT	$\overline{\text{CS}}$	AGND	DUTGND	MEASOUT01/ TEMPSENSE

07278-002

Figure 2. 84-Ball BGA Pin Configuration, Bottom Side (BGA Balls Are Visible)

Table 16. Pin Function Descriptions

BGA Designator	Mnemonic	Description
A1	TEMPSENSE	Temperature Sense Output
A2	PMUS_CH1	PMU External Sense Path Channel 1
A3	VSSO_1 (Drive)	Driver Output Supply −5.75 V Channel 1
A4	DUT1	Device Under Test Channel 1
A5	VDDO_1 (Drive)	Driver Output Supply +10.0 V Channel 1
A6	VDDO_0 (Drive)	Driver Output Supply +10.0 V Channel 0
A7	DUT0	Device Under Test Channel 0
A8	VSSO_0 (Drive)	Driver Output Supply −5.75 V Channel 0
A9	PMUS_CH0	PMU External Sense Path Channel 0
A10	HVOUT	High Voltage Driver Output
B1	VDD/VDD_TMPSNS	Temperature Sense Supply +10.0 V
B2	SCAP1	PMU Stability Capacitor Connection Channel 1 (330 pF)

BGA Designator	Mnemonic	Description
B3	VSS	Supply −5.75 V
B4	AGND	Analog Ground
B5	VDD	Supply +10.0 V
B6	VDD	Supply +10.0 V
B7	AGND	Analog Ground
B8	VSS	Supply −5.75 V
B9	SCAP0	PMU Stability Capacitor Connection Channel 0 (330 pF)
B10	VPLUS	Supply +16.75 V
C1	FFCAP_1B	PMU Feedforward Capacitor Connection B Channel 1 (220 pF)
C2	AGND	Analog Ground
C3	DATA1N	Driver Data Input (Negative) Channel 1
C4	VSS	Supply −5.75 V
C5	VDD	Supply +10.0 V
C6	VDD	Supply +10.0 V
C7	VSS	Supply −5.75 V
C8	DATA0N	Driver Data Input (Negative) Channel 0
C9	AGND	Analog Ground
C10	FFCAP_0B	PMU Feedforward Capacitor Connection B Channel 0 (220 pF)
D1	OVD_CH1	Overvoltage Detection Flag Output Channel 1
D2	VDD	Supply +10.0 V
D3	DATA1P	Driver Data Input (Positive) Channel 1
D8	DATA0P	Driver Data Input (Positive) Channel 0
D9	VDD	Supply +10.0 V
D10	OVD_CH0	Overvoltage Detection Flag Output Channel 0
E1	FFCAP_1A	PMU Feedforward Capacitor Connection A Channel 1 (220 pF)
E2	VSS	Supply −5.75 V
E3	RCV1N	Receive Data Input (Negative) Channel 1
E8	RCV0N	Receive Data Input (Negative) Channel 0
E9	VSS	Supply −5.75 V
E10	FFCAP_0A	PMU Feedforward Capacitor Connection A Channel 0 (220 pF)
F1	AGND	Analog Ground
F2	AGND	Analog Ground
F3	RCV1P	Receive Data Input (Positive) Channel 1
F8	RCV0P	Receive Data Input (Positive) Channel 0
F9	AGND	Analog Ground
F10	AGND	Analog Ground
G1	COMP_QL1P	Low-Side Comparator Output (Positive) Channel 1
G2	COMP_QL1N	Low-Side Comparator Output (Negative) Channel 1
G3	COMP_VTT1	Comparator Supply Termination Channel 1
G8	COMP_VTT0	Comparator Supply Termination Channel 0
G9	COMP_QL0N	Low-Side Comparator Output (Negative) Channel 0
G10	COMP_QL0P	Low-Side Comparator Output (Positive) Channel 0
H1	COMP_QH1P	High-Side Comparator Output (Positive) Channel 1
H2	COMP_QH1N	High-Side Comparator Output (Negative) Channel 1
H3	AGND	Analog Ground
H4	VSS	Supply −5.75 V
H5	VDD	Supply +10.0 V
H6	VDD	Supply +10.0 V
H7	VSS	Supply −5.75 V
H8	AGND	Analog Ground

BGA Designator	Mnemonic	Description
H9	COMP_QH0N	High-Side Comparator Output (Negative) Channel 0
H10	COMP_QH0P	High-Side Comparator Output (Positive) Channel 0
J1	AGND	Analog Ground
J2	AGND	Analog Ground
J3	AGND	Analog Ground
J4	DAC16_MON	16-Bit DAC Monitor Mux Output
J5	DGND	Digital Ground
J6	SDIN	Serial Peripheral Interface (SPI) Data In
J7	$\overline{\text{RST}}$	Serial Peripheral Interface (SPI) Reset
J8	AGND	Analog Ground
J9	AGND	Analog Ground
J10	AGND	Analog Ground
K1	MEASOUT01/TEMPSENSE	Muxed Output Shared by PMU MEASOUT Channel 0, PMU MEASOUT Channel 1, Temperature Sense and Temperature Sense GND Reference
K2	DUTGND	DUT Ground Reference
K3	AGND	Analog Ground
K4	$\overline{\text{CS}}$	Serial Peripheral Interface (SPI) Chip Select
K5	SDOUT	Serial Peripheral Interface (SPI) Data Out
K6	SCLK	Serial Peripheral Interface (SPI) Clock
K7	VCC	Supply +3.3 V
K8	AGND	Analog Ground
K9	VREF	+5 V DAC Reference Voltage
K10	VREF_GND	DAC Ground Reference

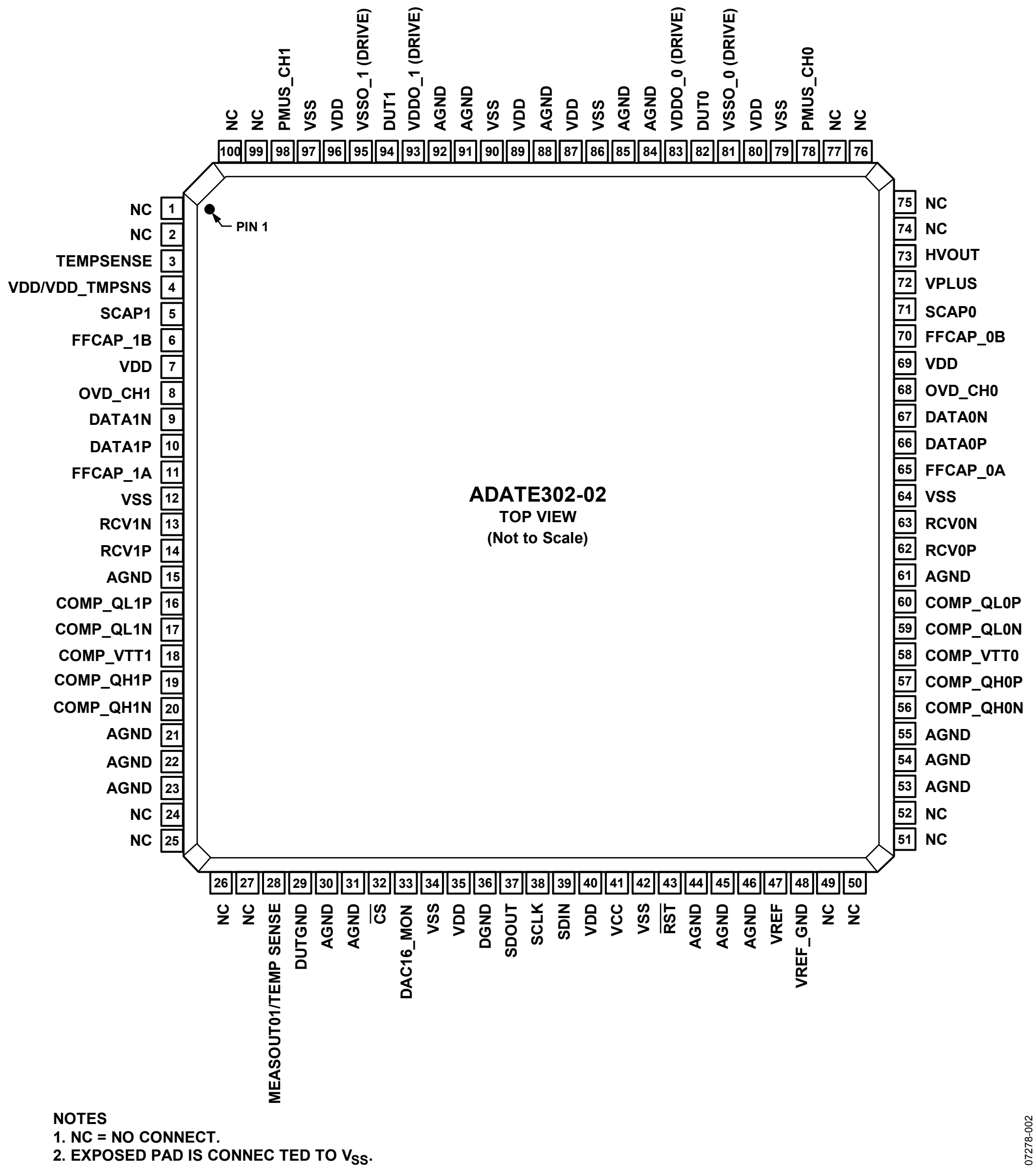


Figure 3. 100-Lead TQFP_EP Pin Configuration

Table 17. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	NC	No Connect. No physical connection to die.
2	NC	No Connect. No physical connection to die.
3	TEMPSENSE	Temperature Sense Output.
4	VDD/VDD_TMPSNS	Temperature Sense Supply +10.0 V.
5	SCAP1	PMU Stability Capacitor Connection Channel 1 (330 pF).
6	FFCAP_1B	PMU Feed Forward Capacitor Connection B Channel 1 (220 pF).
7	VDD	Supply +10.0 V.
8	OVD_CH1	Overvoltage Detection Flag Output Channel 1.
9	DATA1N	Driver Data Input (Negative) Channel 1.
10	DATA1P	Driver Data Input (Positive) Channel 1.
11	FFCAP_1A	PMU Feedforward Capacitor Connection A Channel 1 (220 pF).
12	VSS	Supply −5.75 V.

Pin No.	Mnemonic	Description
13	RCV1N	Receive Data Input (Negative) Channel 1.
14	RCV1P	Receive Data Input (Positive) Channel 1.
15	AGND	Analog Ground.
16	COMP_QL1P	Low-Side Comparator Output (Positive) Channel 1.
17	COMP_QL1N	Low-Side Comparator Output (Negative) Channel 1.
18	COMP_VTT1	Comparator Supply Channel 1.
19	COMP_QH1P	High-Side Comparator Output (Positive) Channel 1.
20	COMP_QH1N	High-Side Comparator Output (Negative) Channel 1.
21	AGND	Analog Ground.
22	AGND	Analog Ground.
23	AGND	Analog Ground.
24	NC	No Connect. No physical connection to die.
25	NC	No Connect. No physical connection to die.
26	NC	No Connect. No physical connection to die.
27	NC	No Connect. No physical connection to die.
28	MEASOUT01/TEMP SENSE	Shared Muxed Output. Muxed output shared by PMU MEASOUT Channel 0, PMU MEASOUT Channel 1, and the temperature sense and temperature sense GND reference.
29	DUTGND	Device Under Test Ground Reference.
30	AGND	Analog Ground.
31	AGND	Analog Ground.
32	$\overline{\text{CS}}$	Serial Peripheral Interface (SPI®) Chip Select.
33	DAC16_MON	16-Bit DAC Monitor Mux Output.
34	VSS	Supply −5.75 V.
35	VDD	Supply +10.0 V.
36	DGND	Digital Ground.
37	SDOUT	Serial Programmable Interface (SPI) Data Output.
38	SCLK	Serial Programmable Interface (SPI) Clock.
39	SDIN	Serial Programmable Interface (SPI) Data Input.
40	VDD	Supply +10.0 V.
41	VCC	Supply +3.3 V.
42	VSS	Supply −5.75 V.
43	$\overline{\text{RST}}$	Serial Peripheral Interface (SPI) Reset.
44	AGND	Analog Ground.
45	AGND	Analog Ground.
46	AGND	Analog Ground.
47	VREF	+5 V DAC Reference Voltage.
48	VREF_GND	DAC Ground Reference.
49	NC	No Connect. No physical connection to die.
50	NC	No Connect. No physical connection to die.
51	NC	No Connect. No physical connection to die.
52	NC	No Connect. No physical connection to die.
53	AGND	Analog Ground.
54	AGND	Analog Ground.
55	AGND	Analog Ground.
56	Comp_QH0N	High-Side Comparator Output (Negative) Channel 0.
57	Comp_QH0P	High-Side Comparator Output (Positive) Channel 0.
58	Comp_VTT0	Comparator Supply Channel 0.
59	Comp_QL0N	Low-Side Comparator Output (Negative) Channel 0.
60	Comp_QL0P	Low-Side Comparator Output (Positive) Channel 0.

Pin No.	Mnemonic	Description
61	AGND	Analog Ground.
62	RCV0P	Receive Data Input (Positive) Channel 0.
63	RCV0N	Receive Data Input (Negative) Channel 0.
64	VSS	Supply −5.75 V.
65	FFCAP_0A	PMU Feedforward Capacitor Connection A Channel 0 (220 pF).
66	DATA0P	Driver Data Input (Positive) Channel 0.
67	DATA0N	Driver Data Input (Negative) Channel 0.
68	OVD_CH0	Overvoltage Detection Flag Output Channel 0.
69	VDD	Supply +10.0 V.
70	FFCAP_0B	PMU Feedforward Capacitor Connection B Channel 0 (220 pF).
71	SCAP0	PMU Stability Capacitor Connection Channel 0 (330 pF).
72	VPLUS	Supply +16.75 V.
73	HVOUT	High Voltage Driver Output.
74	NC	No Connect. No physical connection to die.
75	NC	No Connect. No physical connection to die.
76	NC	No Connect. No physical connection to die.
77	NC	No Connect. No physical connection to die.
78	PMUS_CH0	PMU External Sense Path Channel 0.
79	VSS	Supply −5.75 V.
80	VDD	Supply +10.0 V.
81	VSSO_0 (DRIVE)	Driver Output Supply −5.75 V Channel 0.
82	DUT0	Device Under Test Channel 0.
83	VDDO_0 (DRIVE)	Driver Output Supply +10.0 V Channel 0.
84	AGND	Analog Ground.
85	AGND	Analog Ground.
86	VSS	Supply −5.75 V.
87	VDD	Supply +10.0 V.
88	AGND	Analog Ground.
89	VDD	Supply +10.0 V.
90	VSS	Supply −5.75 V.
91	AGND	Analog Ground.
92	AGND	Analog Ground.
93	VDDO_1 (DRIVE)	Driver Output Supply +10.0 V Channel 1.
94	DUT1	Device Under Test Channel 1.
95	VSSO_1 (DRIVE)	Driver Output Supply −5.75 V Channel 1.
96	VDD	Supply +10.0 V.
97	VSS	Supply −5.75 V.
98	PMUS_CH1	PMU External Sense Path Channel 1.
99	NC	No Connect. No physical connection to die.
100	NC	No Connect. No physical connection to die.
EP		Exposed Pad. The exposed pad is connected to V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

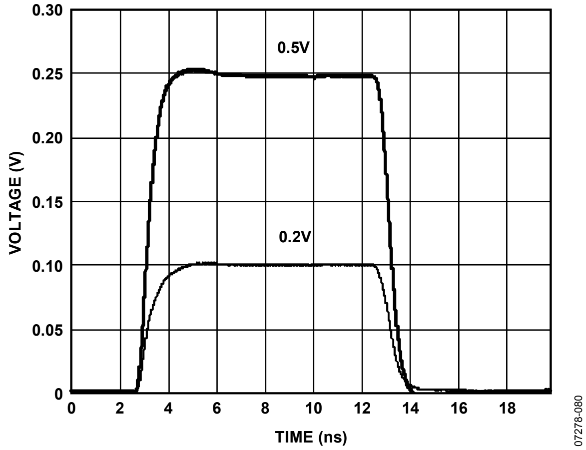


Figure 4. Driver Small Signal Response; VH = 0.2 V, 0.5 V; VL = 0.0 V; 50 Ω Termination

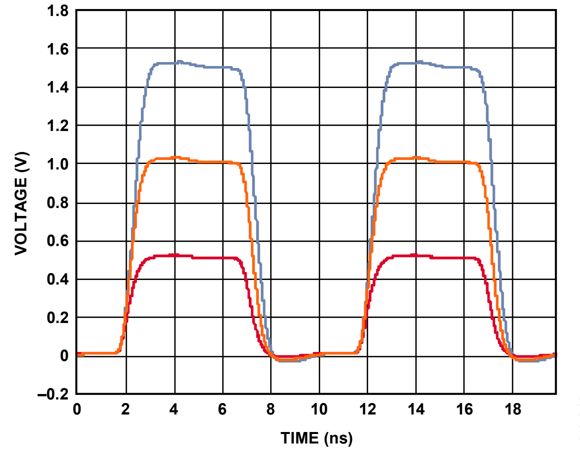


Figure 7. 100 MHz Driver Response; VH = 1.0 V, 2.0 V, 3.0 V; VL = 0.0 V; 50 Ω Termination

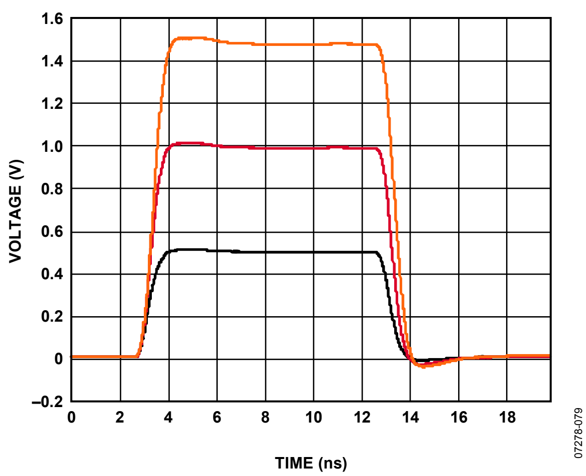


Figure 5. Driver Large Signal Response; VH = 1.0 V, 2.0 V, 3.0 V; VL = 0.0 V; 50 Ω Termination

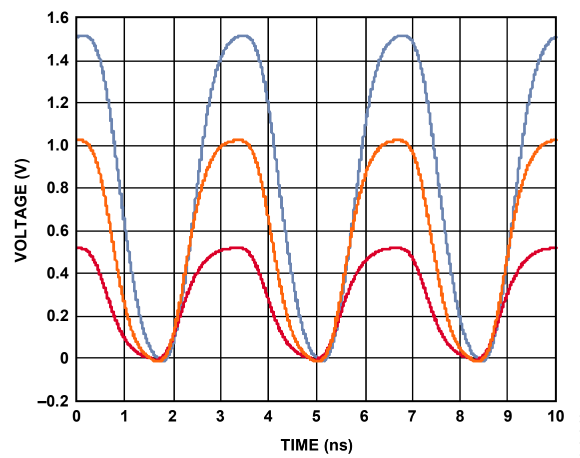


Figure 8. 300 MHz Driver Response; VH = 1.0 V, 2.0 V, 3.0 V; VL = 0.0 V; 50 Ω Termination

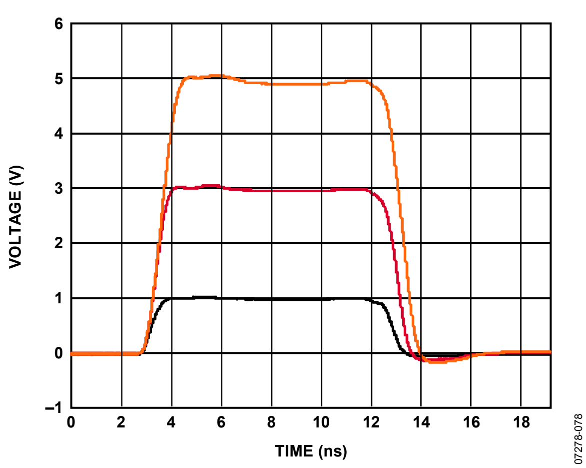


Figure 6. Driver Large Signal Response; VH = 1.0 V, 3.0 V, 5.0 V; VL = 0.0 V; 500 Ω Termination

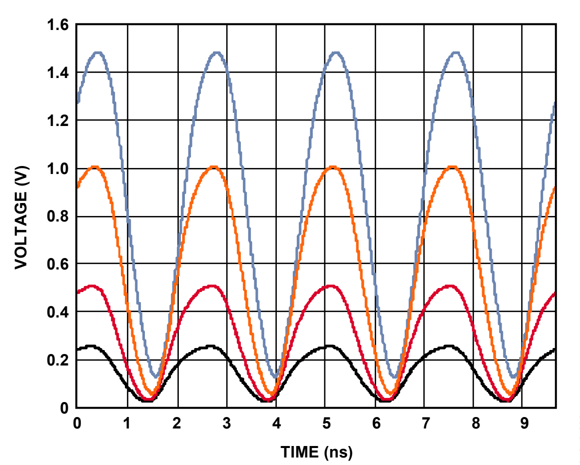


Figure 9. 400 MHz Driver Response; VH = 0.5 V, 1.0 V, 2.0 V, 3.0 V; VL = 0.0 V; 50 Ω Termination

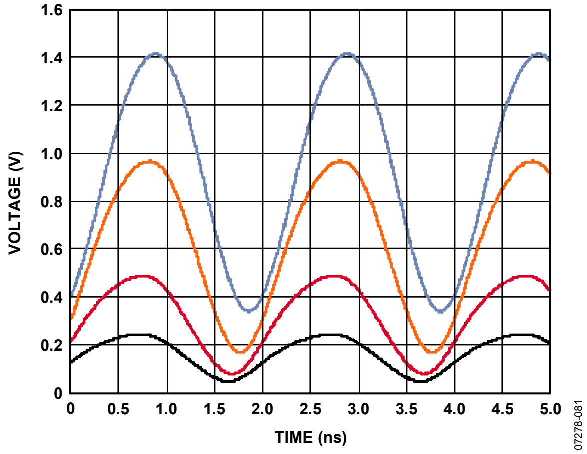


Figure 10. 500 MHz Driver Response; VH = 0.5 V, 1.0 V, 2.0 V, 3.0 V; VL = 0.0 V; 50 Ω Termination

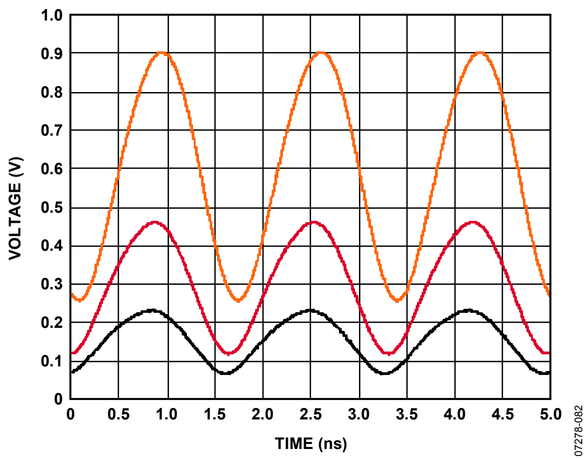


Figure 11. 600 MHz Driver Response; VH = 0.5 V, 1.0 V, 2.0 V; VL = 0.0 V; 50 Ω Termination

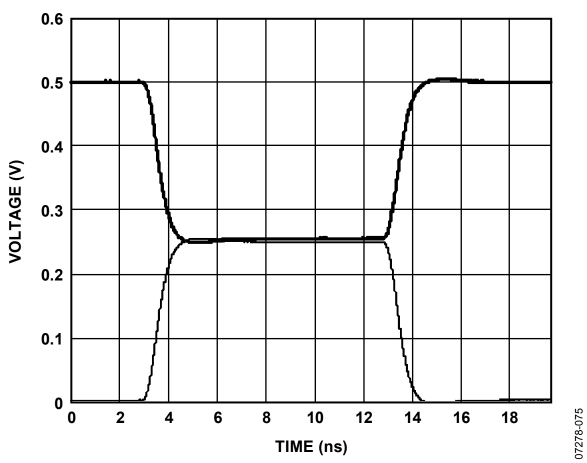


Figure 12. Driver Active (VH/VL) to/from VTERM Transition; VH = 1.0 V; VT = 0.5 V; VL = 0.0 V

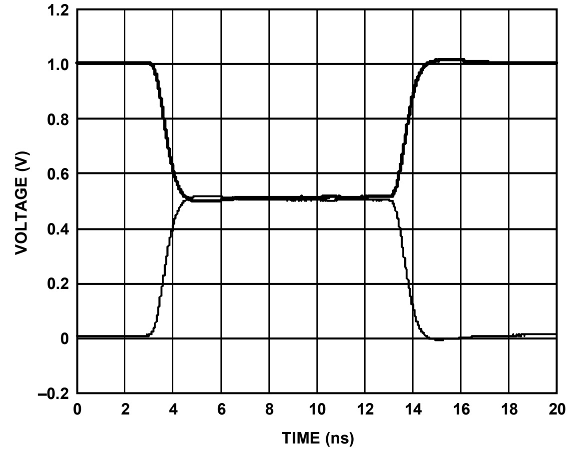


Figure 13. Driver Active (VH/VL) to/from VTERM Transition; VH = 2.0 V; VT = 1.0 V; VL = 0.0 V

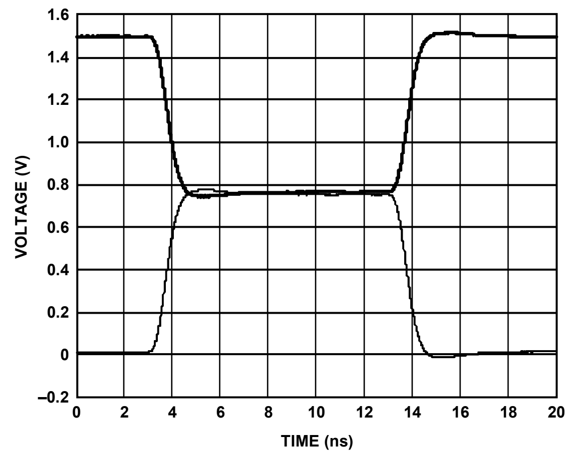


Figure 14. Driver Active (VH/VL) to/from VTERM Transition; VH = 3.0 V; VT = 1.5 V; VL = 0.0 V

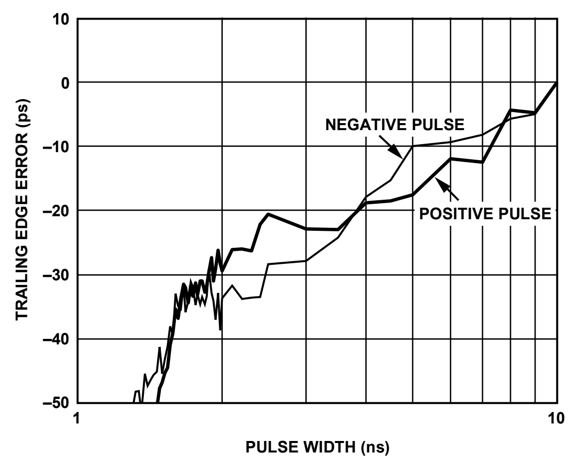


Figure 15. Driver Minimum Pulse Width; VH = 0.2 V; VL = 0.0 V

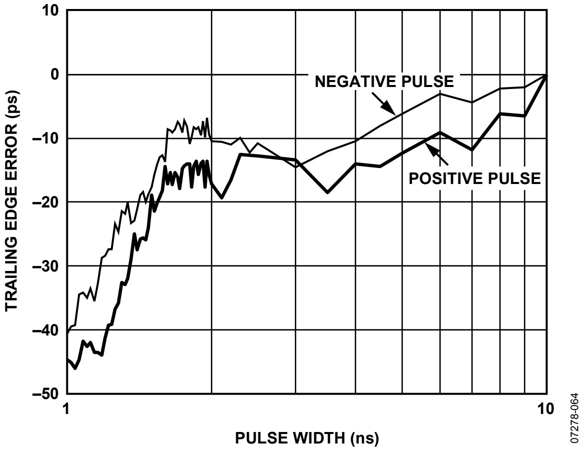


Figure 16. Driver Minimum Pulse Width; VH = 0.5 V; VL = 0.0 V

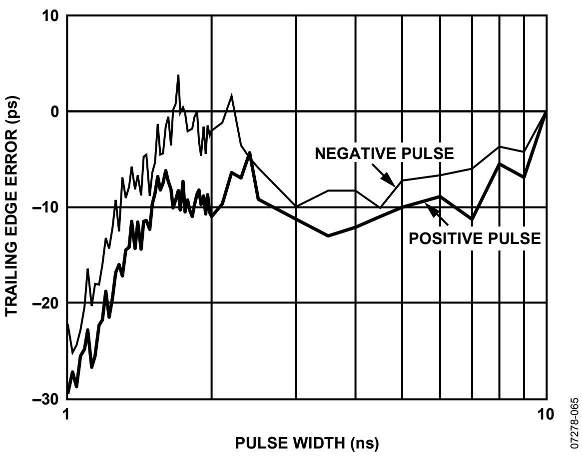


Figure 17. Driver Minimum Pulse Width; VH = 1.0 V; VL = 0.0 V

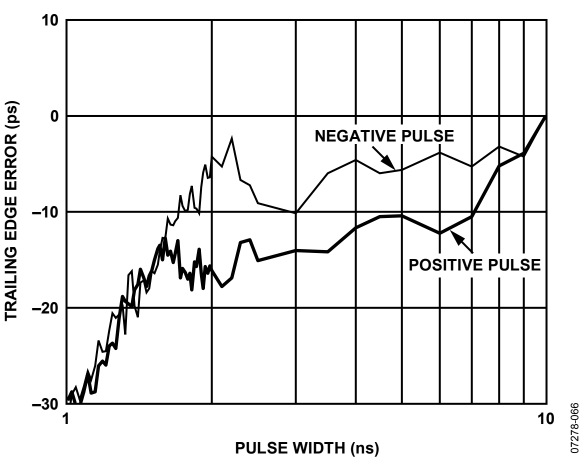


Figure 18. Driver Minimum Pulse Width; VH = 2.0 V; VL = 0.0 V

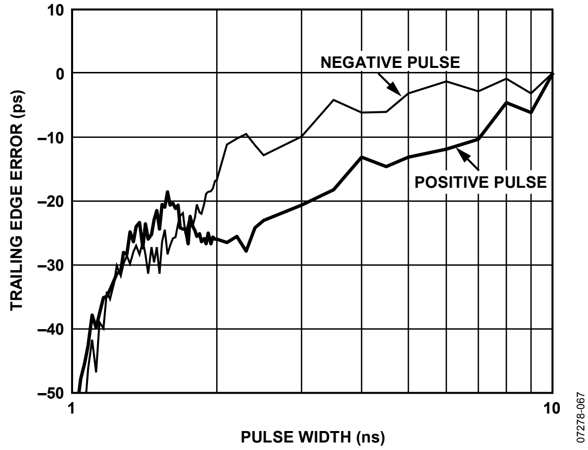


Figure 19. Driver Minimum Pulse Width; VH = 3.0 V; VL = 0.0 V

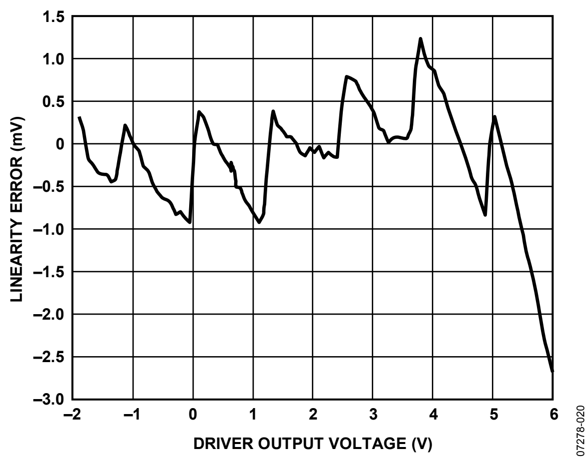


Figure 20. Driver VH Linearity Error

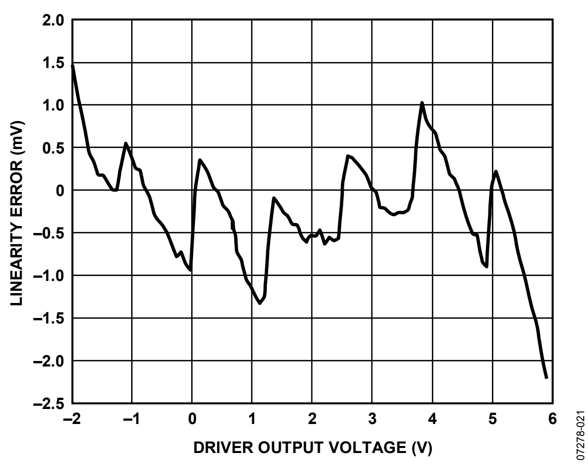


Figure 21. Driver VL Linearity Error

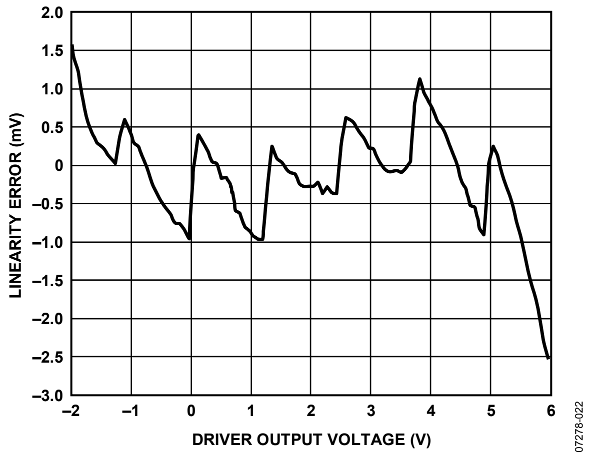


Figure 22. Driver VT Linearity Error

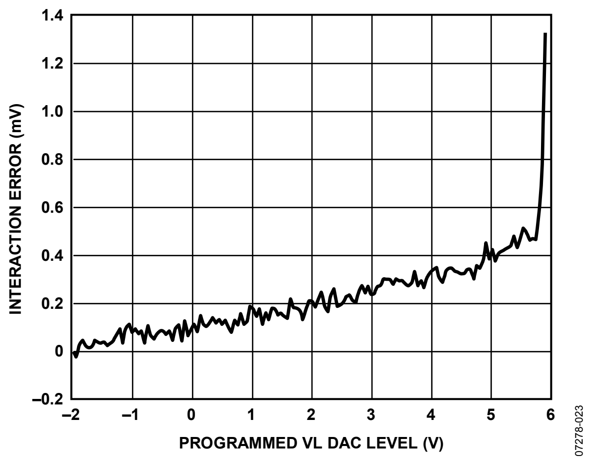


Figure 23. Driver Interaction Error; VH = 6.0 V; VL Swept from −2.0 V to +5.9 V

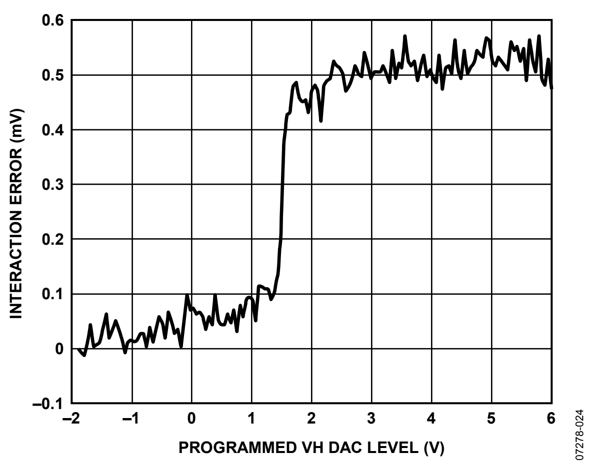


Figure 24. Driver Interaction Error; VT = 1.5 V; VH Swept from −1.9 V to +6.0 V

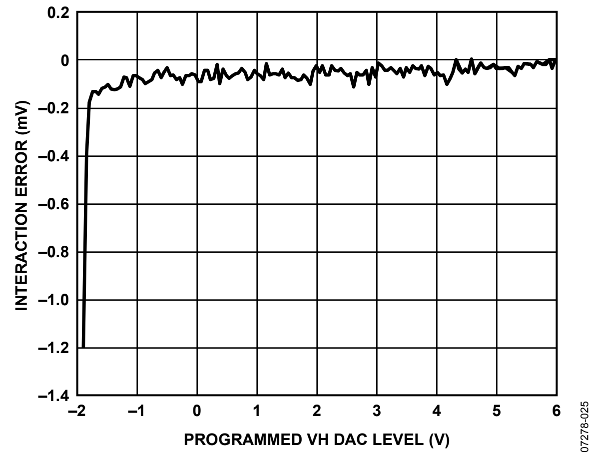


Figure 25. Driver Interaction Error; VL = −2.0 V; VH Swept from −1.9 V to +6.0 V

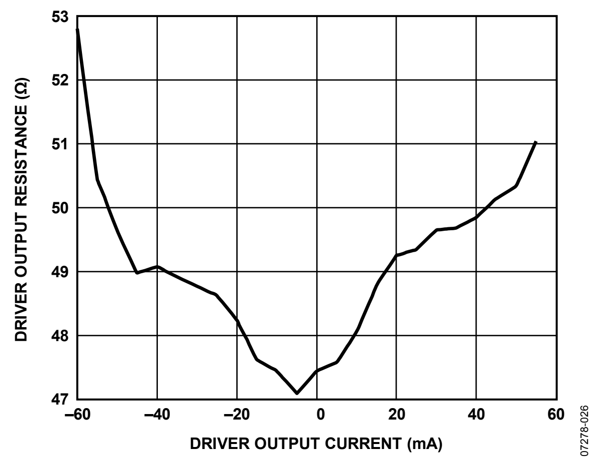


Figure 26. Driver Output Resistance vs. Output Current

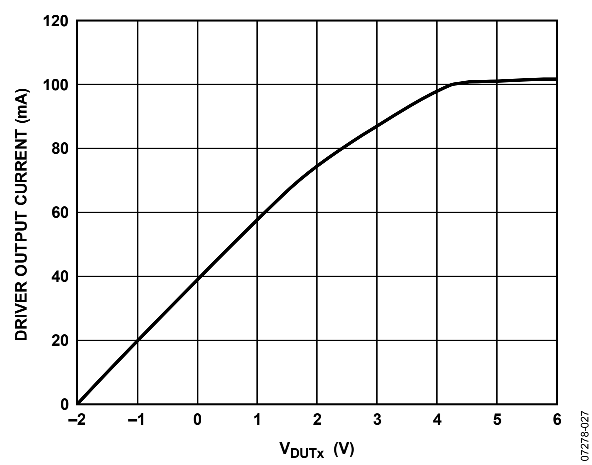


Figure 27. Driver Output Current Limit; Driver Programmed to −2.0 V; V_{DUTx} Swept from −2.0 V to +6.0 V

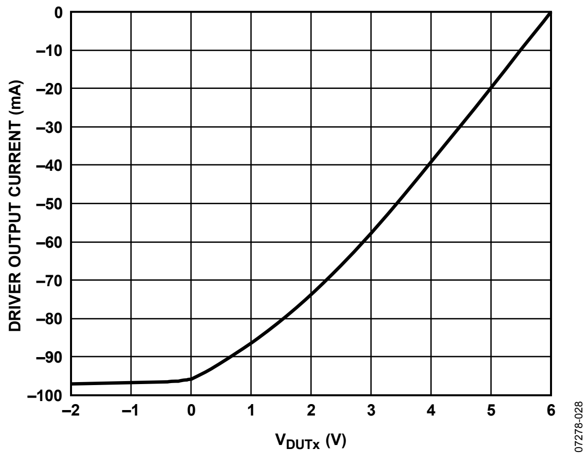


Figure 28. Driver Output Current Limit; Driver Programmed to 6.0 V; V_{DUTx} Swept from −2.0 V to +6.0 V

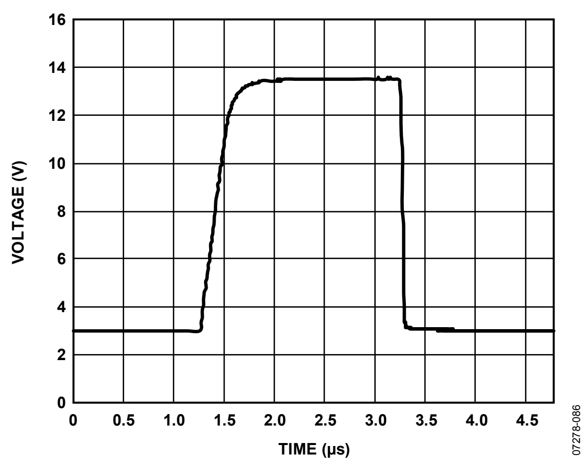


Figure 29. HVOUT VHH Response; VHH = 13.5 V

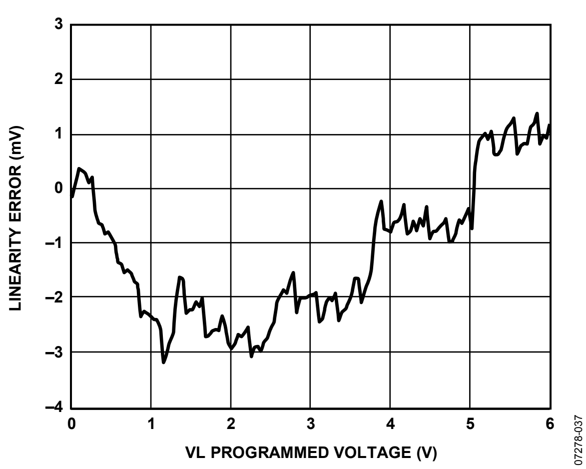


Figure 30. HVOUT VL Linearity Error

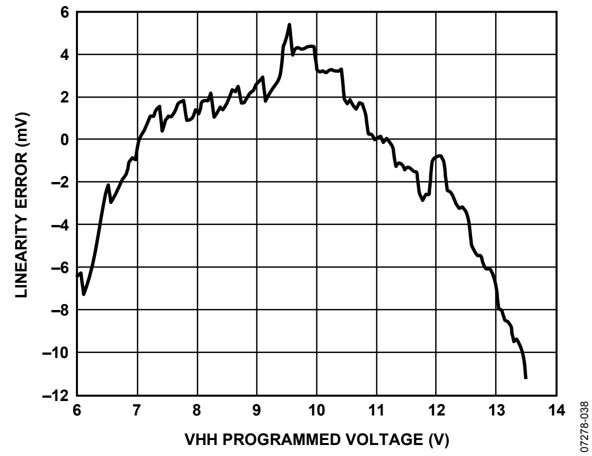


Figure 31. HVOUT VHH Linearity Error

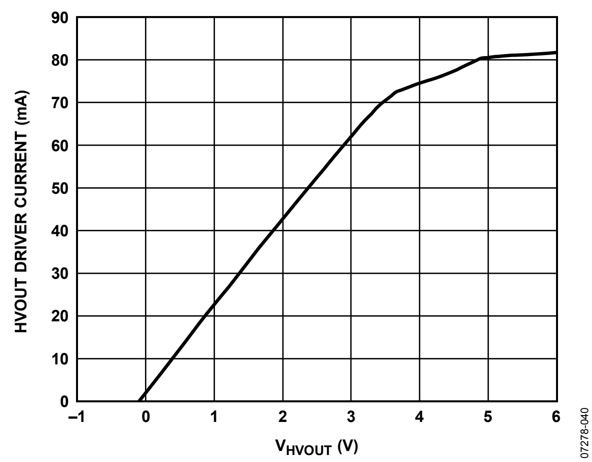


Figure 32. HVOUT VH Current Limit; VH = −0.1 V; V_{HVOUT} Swept from −0.1 V to +6.0 V

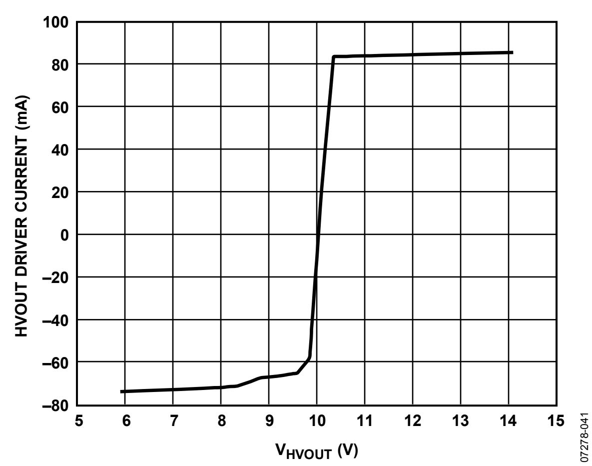


Figure 33. HVOUT VHH Current Limit; VHH = 10.0 V; V_{HVOUT} Swept from 5.9 V to 14.1 V

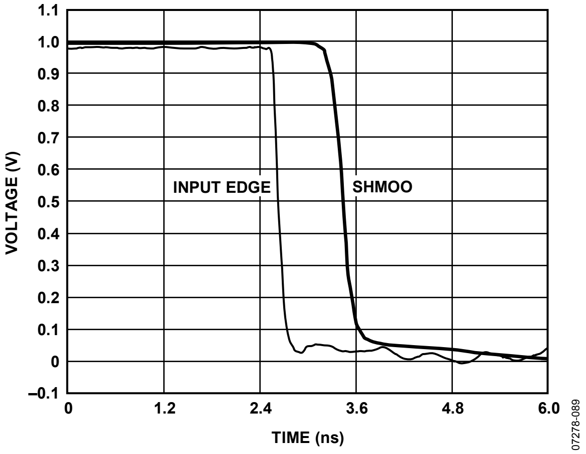


Figure 34. Comparator Shmoo;
1.0 V Swing; 200 ps (10%/90%)

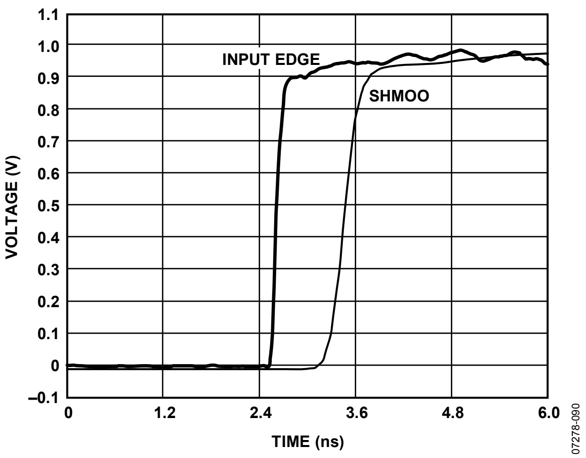


Figure 35. Comparator Shmoo;
1.0 V Swing; 200 ps (10%/90%)

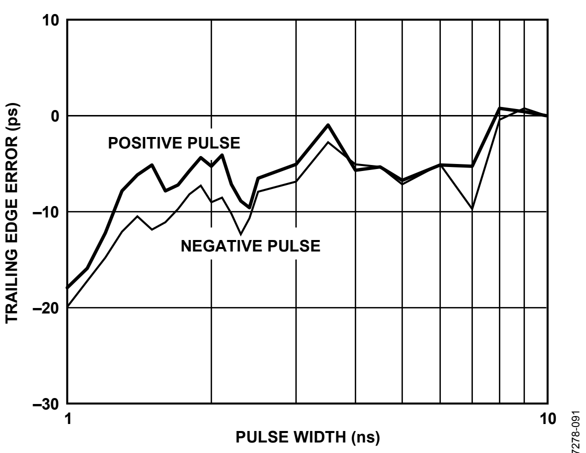


Figure 36. Comparator Minimum Pulse Width Input;
1.0 V Swing; 200 ps (10%/90%)

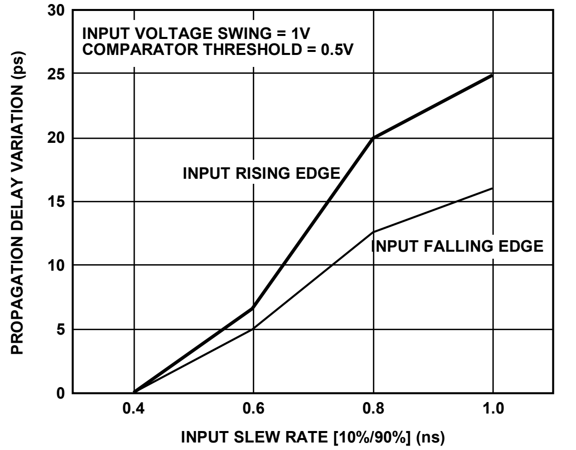


Figure 37.Comparator Slew Rate Dispersion

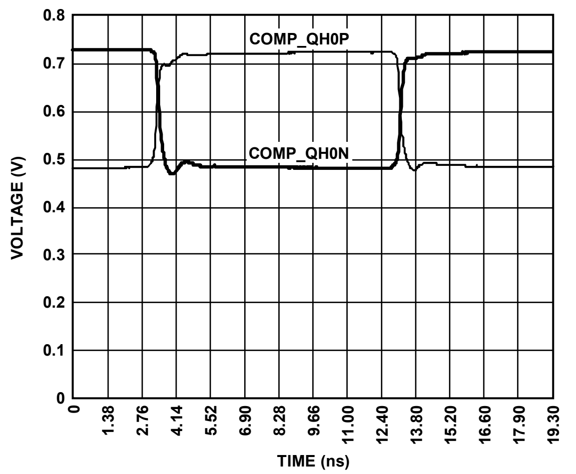


Figure 38. Comparator Output Waveform; COMP_QH0P, COMP_QH0N

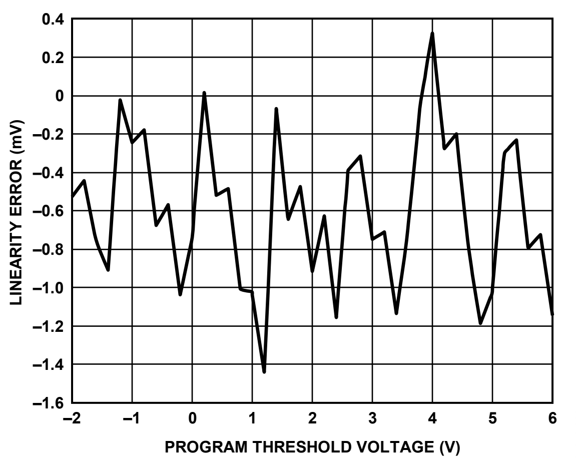


Figure 39. Comparator Threshold Linearity

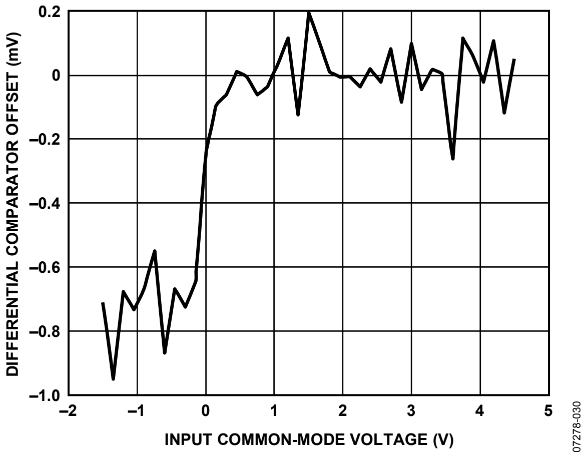


Figure 40. Differential Comparator CMRR

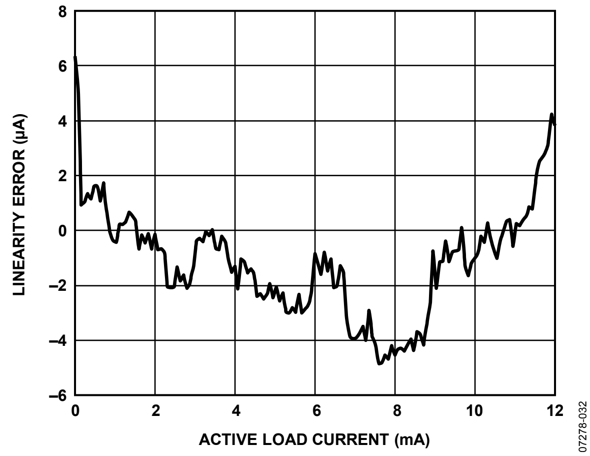


Figure 43. Active Load Current Linearity

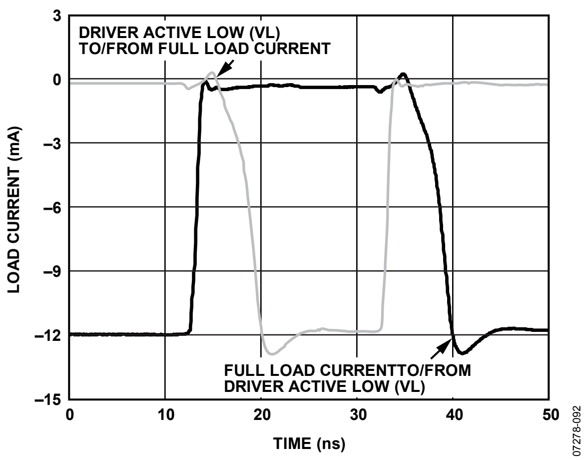


Figure 41. Active Load Response

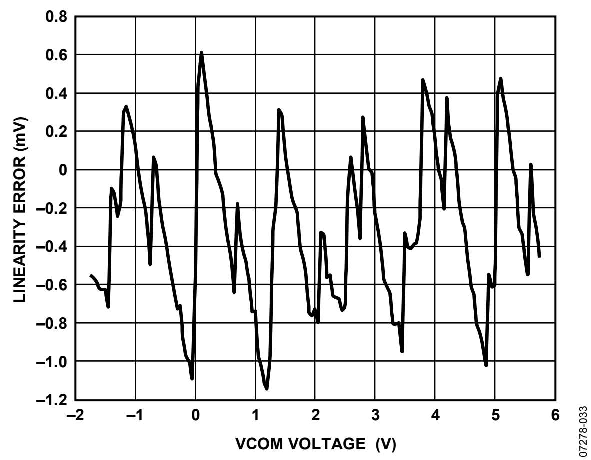


Figure 44. Active Load VCOM Linearity

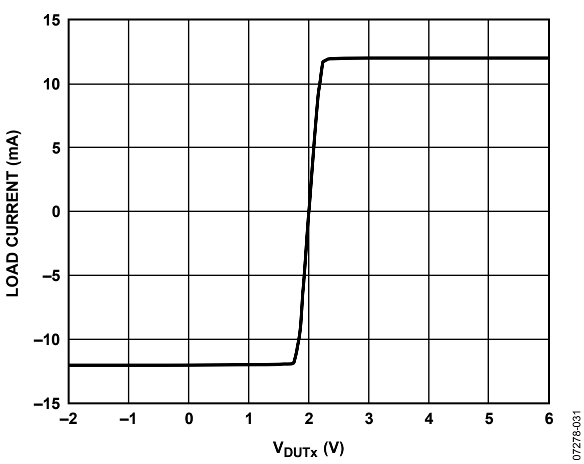


Figure 42. Active Load Commutation Response;
VCOM = 2.0 V; IOH = IOL = 12 mA

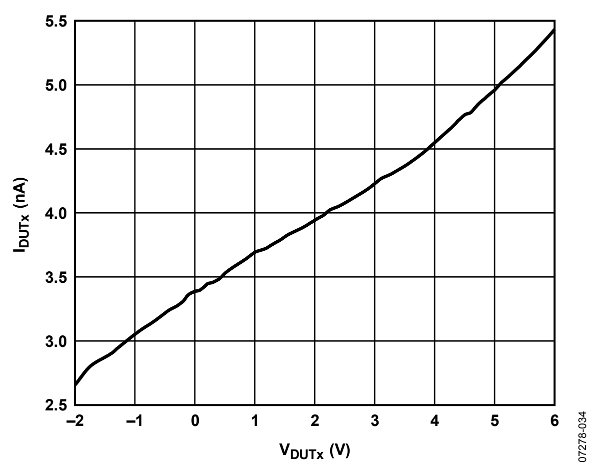


Figure 45. DUTx Pin Leakage Current in Low Leakage Mode

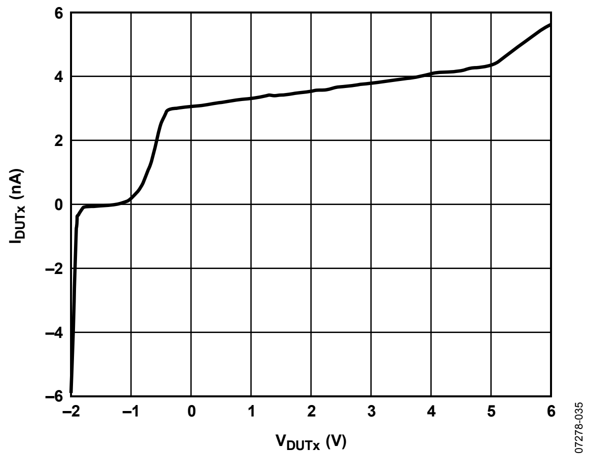


Figure 46. DUTx Pin Leakage Current in High-Z Mode

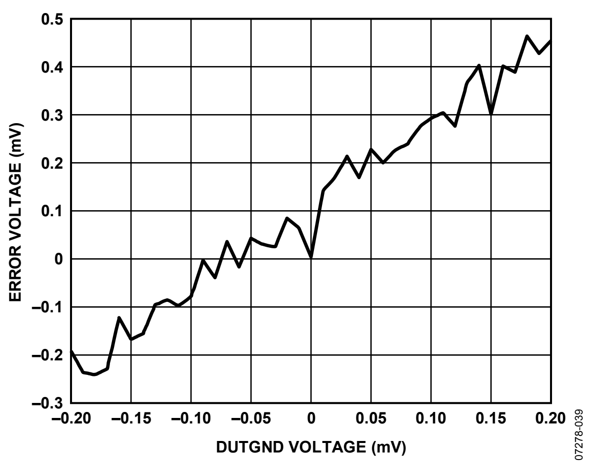


Figure 47. DUTGND Voltage Effects

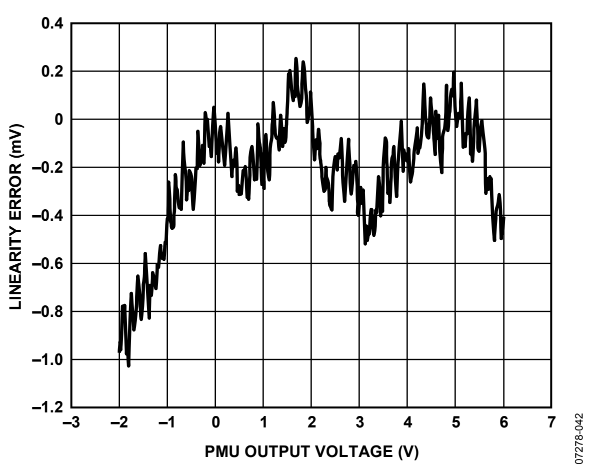


Figure 48. PMU Force Voltage Linearity

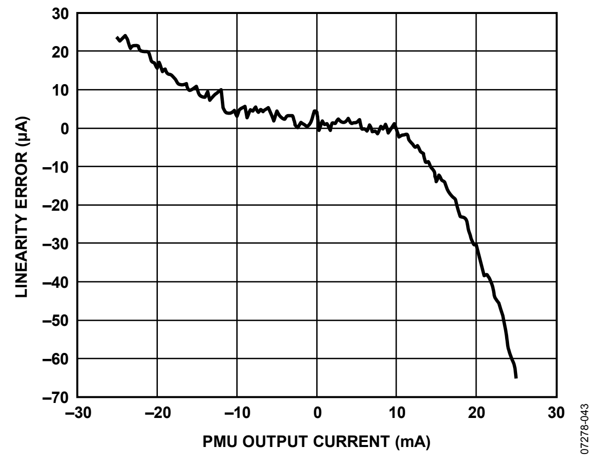


Figure 49. PMU Force Current Range A Linearity

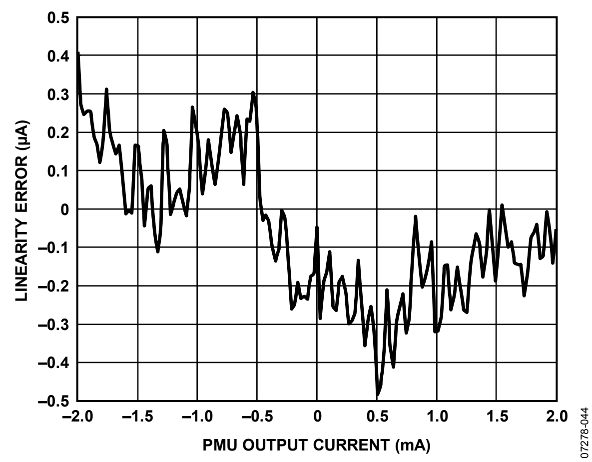


Figure 50. PMU Force Current Range B Linearity

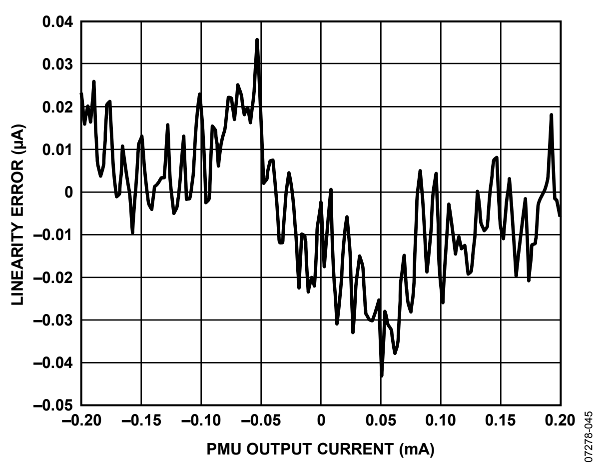


Figure 51. PMU Force Current Range C Linearity

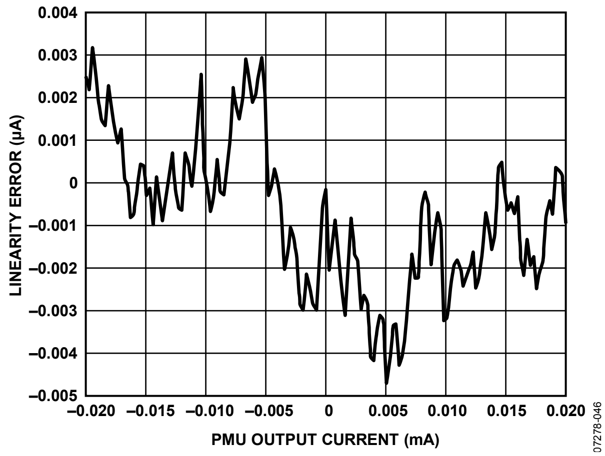


Figure 52. PMU Force Current Range D Linearity

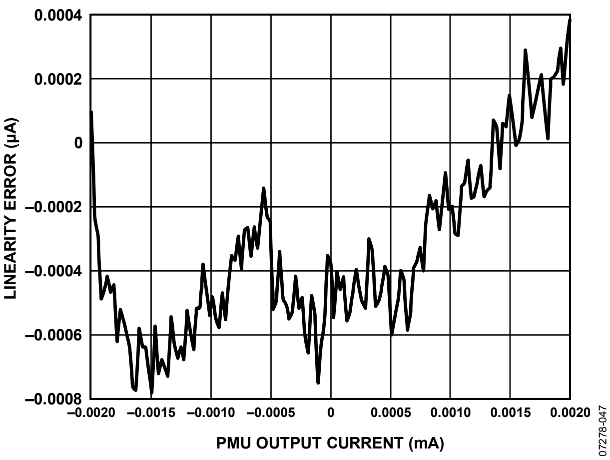


Figure 53. PMU Force Current Range E Linearity

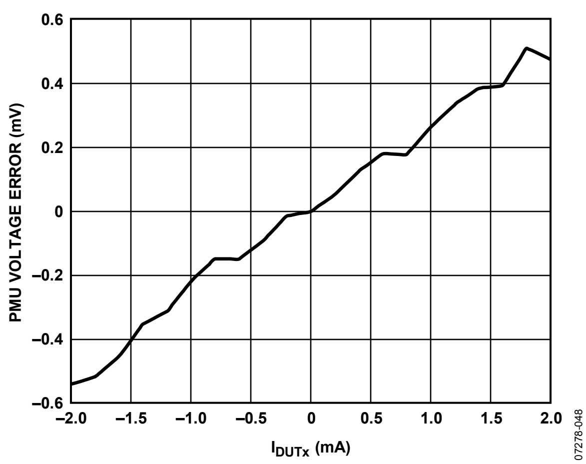


Figure 54. PMU Force Voltage Range B Output Voltage Error at 6.0 V vs. Output Current

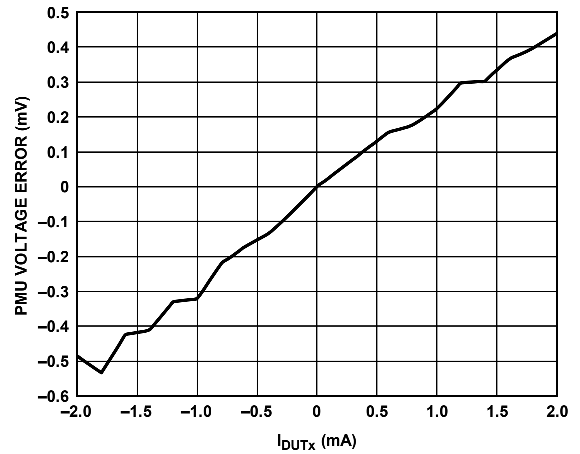


Figure 55. PMU Force Voltage Range B Output Voltage Error at −2.0 V vs. Output Current

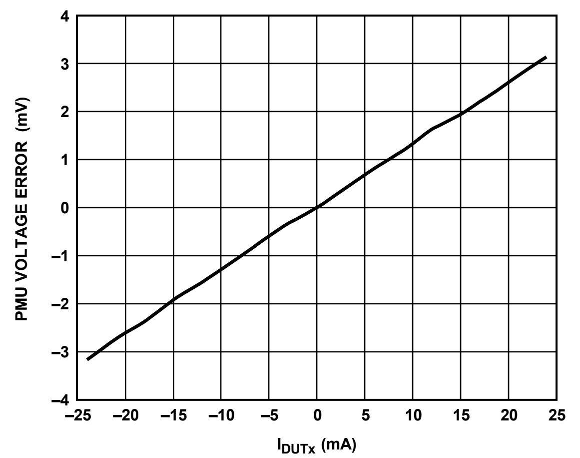


Figure 56. PMU Force Voltage Range A Output Voltage Error at 6.0 V vs. Output Current

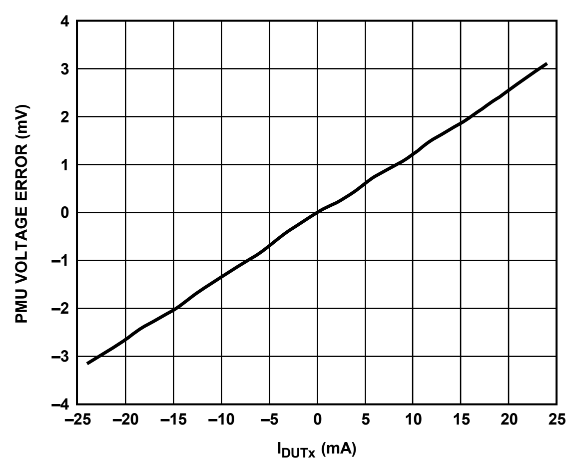


Figure 57. PMU Force Voltage Range A Output Voltage Error at −2.0 V vs. Output Current

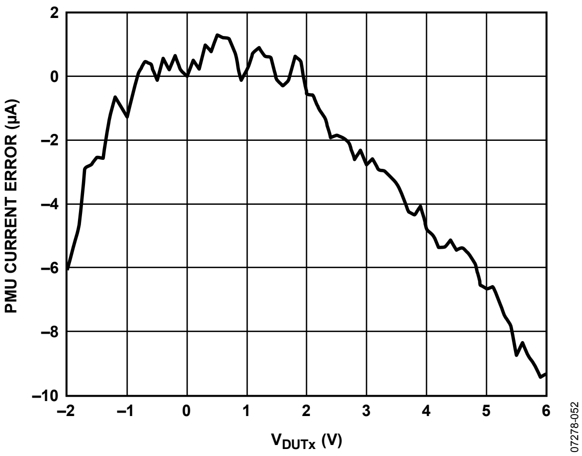


Figure 58. PMU Force Current Range A Output Current Error at −25 mA vs. Output Voltage

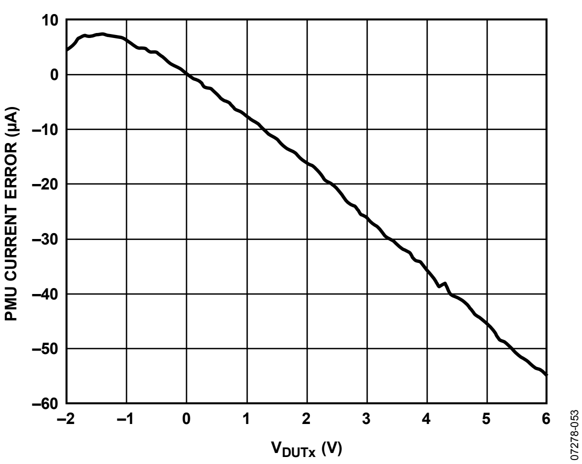


Figure 59. PMU Force Current Range A Output Current Error at 25 mA vs. Output Voltage; Output Voltage Is Pulled Externally

Figure 60. PMU Force Current Range B Output Current Error at −2 mA vs. Output Voltage; Output Voltage Is Pulled Externally

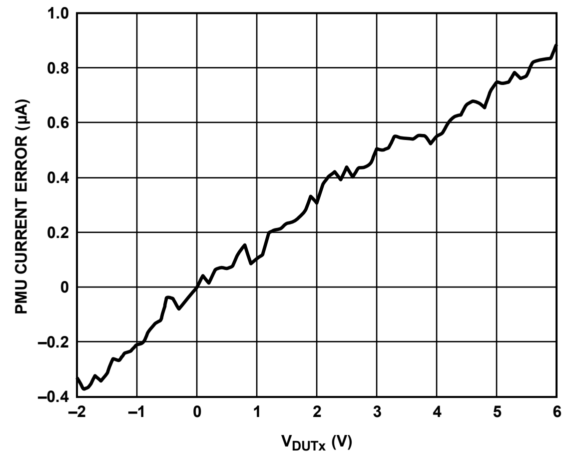


Figure 61. PMU Force Current Range B Output Current Error at 2 mA vs. Output Voltage; Output Voltage Is Pulled Externally

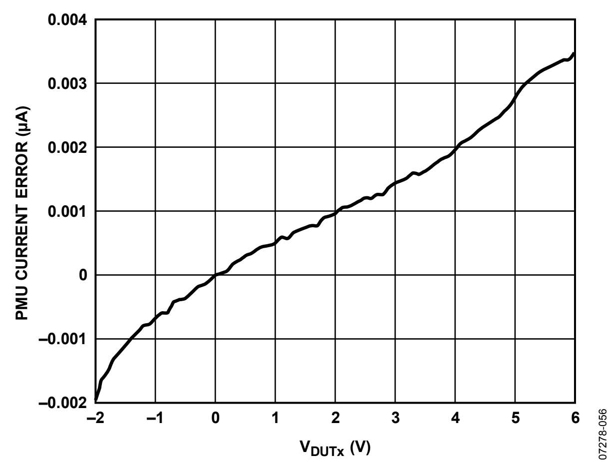


Figure 62. PMU Force Current Range E Output Current Error at −2 µA vs. Output Voltage; Output Voltage Is Pulled Externally

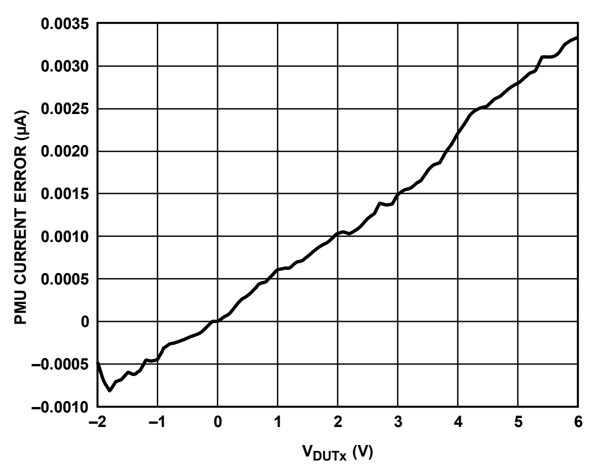


Figure 63. PMU Force Current Range E Output Current Error at 2 µA vs. Output Voltage; Output Voltage Is Pulled Externally

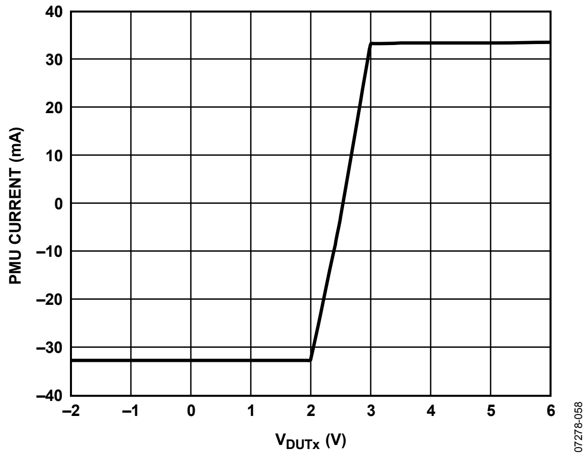


Figure 64. PMU Range A Internal Current Limit, Programmed to Force 2.5 V; V_{DUTx} Swept from −2.0 V to +6.0 V

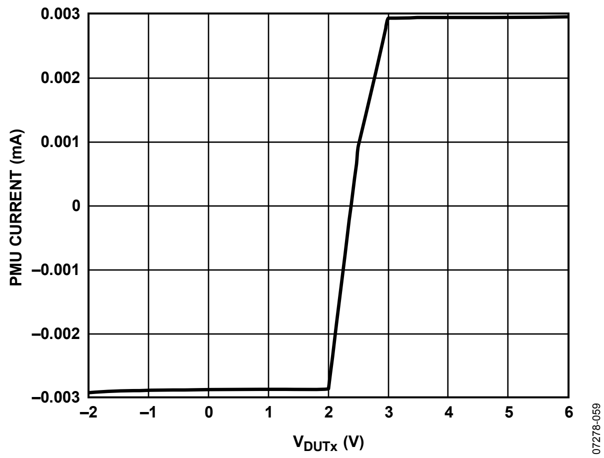


Figure 65. PMU Range E Internal Current Limit, Programmed to Force 2.5 V; V_{DUTx} Swept from −2.0 V to +6.0 V

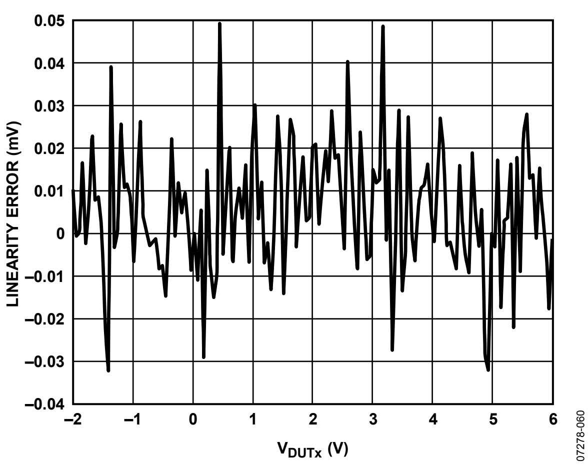


Figure 66. PMU Range B Measure Voltage Linearity

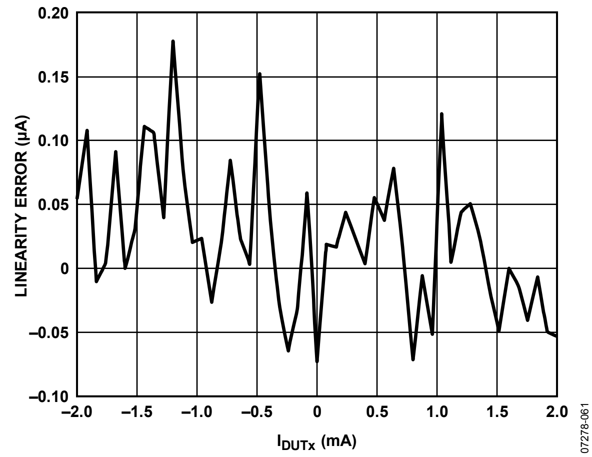


Figure 67. PMU Range B Measure Current Linearity

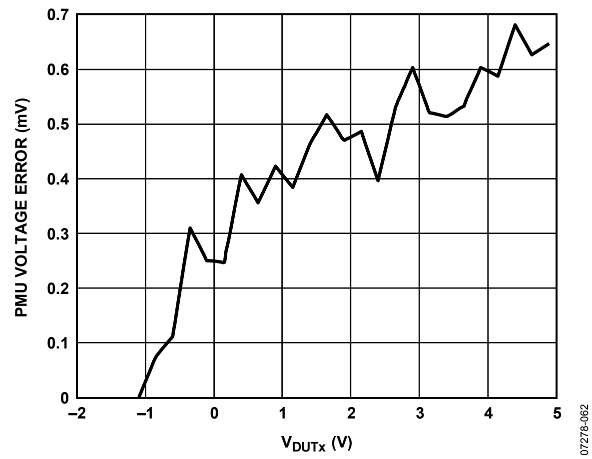


Figure 68. PMU Measure Current CMRR, Externally Pulling 1 mA, FVMI; Error of MI vs. External 1 mA

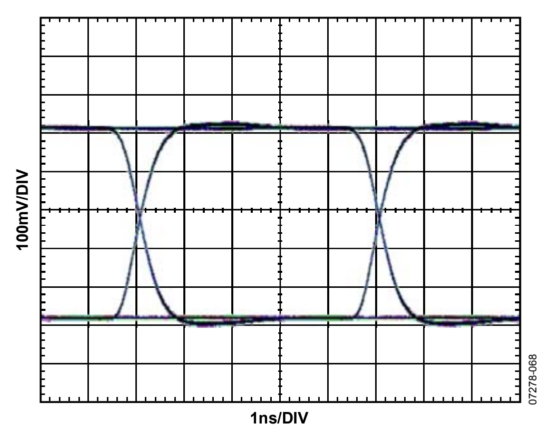


Figure 69. Eye Diagram, 200 Mbps, PRBS31; VH = 1.0 V; VL = 0.0 V

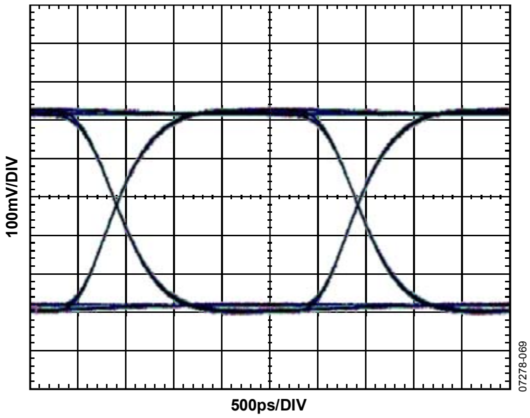


Figure 70. Eye Diagram, 400 Mbps, PRBS31; VH = 1.0 V; VL = 0.0 V

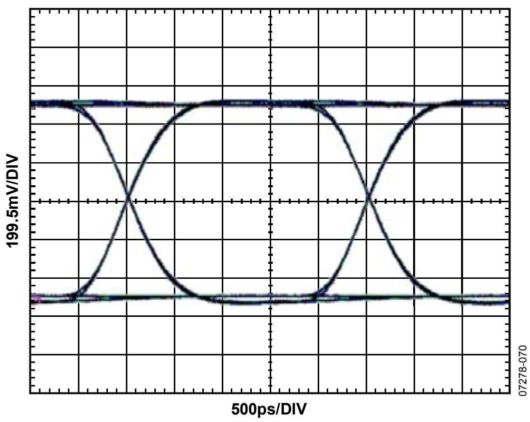


Figure 71. Eye Diagram, 400 Mbps, PRBS31; VH = 2.0 V; VL = 0.0 V

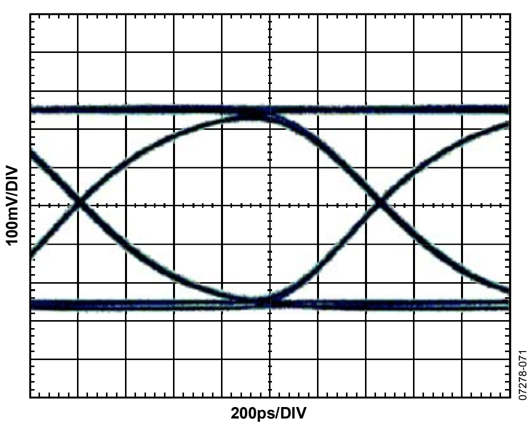


Figure 72. Eye Diagram, 800 Mbps, PRBS31; VH = 1.0 V; VL = 0.0 V

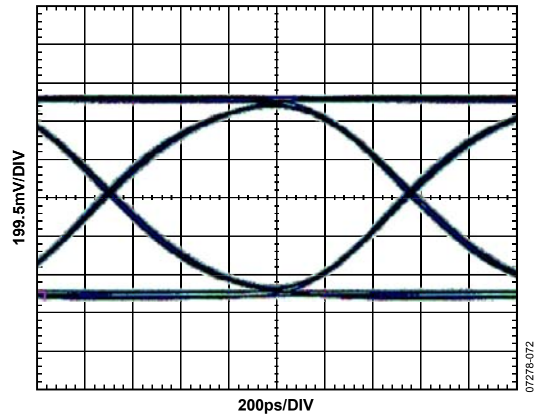


Figure 73. Eye Diagram, 800 Mbps, PRBS31; VH = 2.0 V; VL= 0.0 V

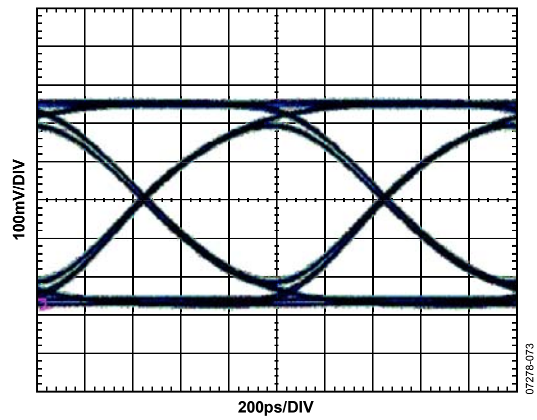


Figure 74. Eye Diagram, 1000 Mbps, PRBS31; VH = 1.0 V; VL = 0.0 V

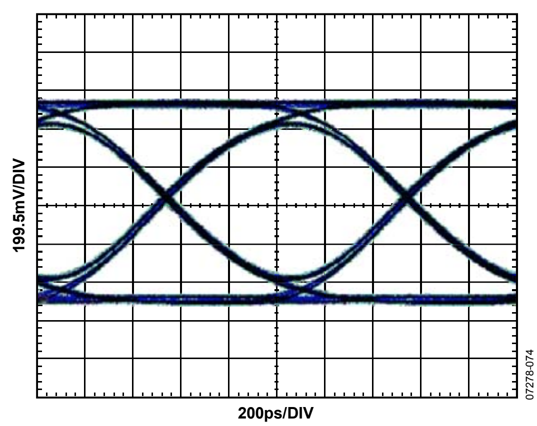


Figure 75. Eye Diagram, 1000 Mbps, PRBS31; VH = 2.0 V; VL = 0.0 V

SERIAL PERIPHERAL INTERFACE DETAILS

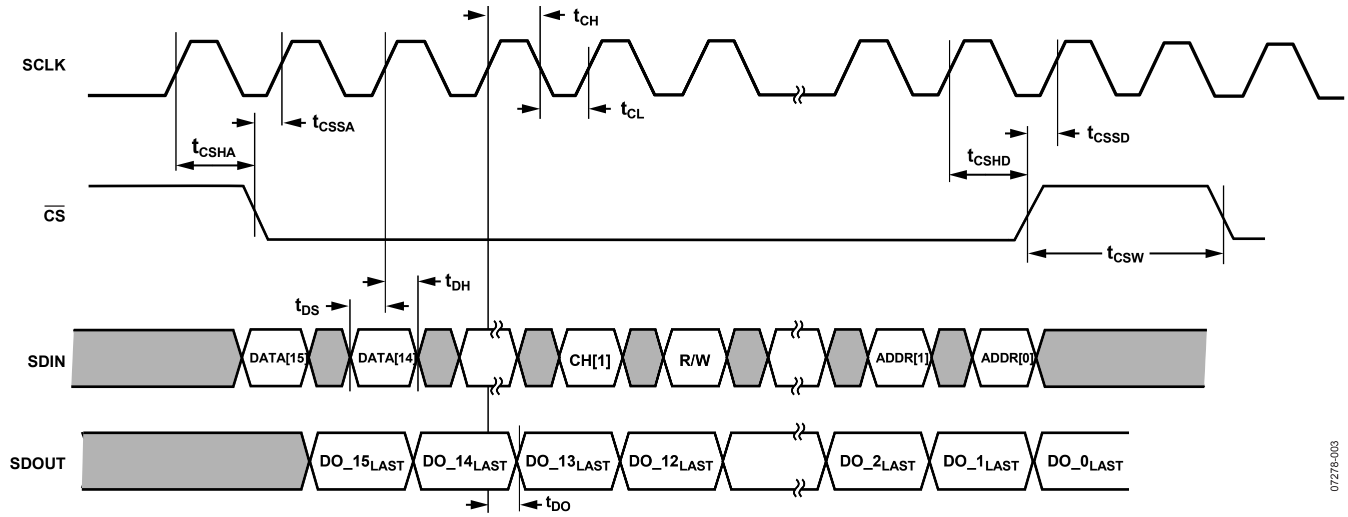


Figure 76. SPI Timing Diagram

Table 18. Serial Peripheral Interface Timing Requirements

Symbol	Parameter	Min	Max	Unit
t_{CH}	SCLK minimum high	9.0		ns
t_{CL}	SCLK minimum low	9.0		ns
t_{CSHA}	$\overline{CS}$ assert hold	3.0		ns
t_{CSSA}	$\overline{CS}$ assert setup	3.0		ns
t_{CSHD}	$\overline{CS}$ deassert hold	3.0		ns
t_{CSSD}	$\overline{CS}$ deassert setup	3.0		ns
t_{DH}	SDIN hold	3.0		ns
t_{DS}	SDIN setup	3.0		ns
t_{DO}	SDOUT Data Out		15.0	ns
t_{CSW}	$\overline{CS}$ minimum between assertions[1]	2		SCLK cycles
	$\overline{CS}$ minimum directly after a read request	3		SCLK cycles
t_{CSTP}	Minimum delay after $\overline{CS}$ is deasserted before SCLK can be stopped (not shown in Figure 76); this allows any internal operations to complete	16		SCLK cycles

[1] Extra cycle is needed after read request to prime read data into SPI shift register.

DEFINITION OF SPI WORD

The SPI can take variable length words, depending on the operation. At most, the word is 24 bits longs: 16 bits of data, two channel selects, one R/W selector, and a 5-bit address.

Depending on the operation, the data can be smaller (or nonexistent in the case of a read operation).

Example 1

Write 16 bits of data to a register or DAC; unused MSBs are ignored. For example, Bit 15 and Bit 14 are ignored, and Bit 13 through Bit 0 are applied to the 14-bit DAC.

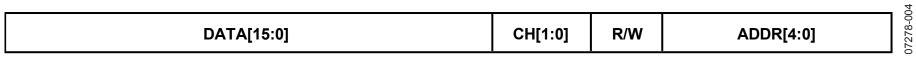


Figure 77.

Example 2

Write 14 bits of data to the DAC.

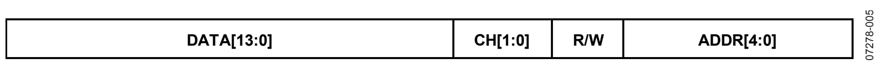


Figure 78.

Example 3a

Write two bits of data to the 2-bit register.

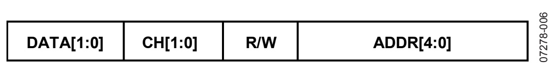


Figure 79.

Example 3b

Write two bits of data to the 2-bit register. Bit 15 through Bit 2 are ignored, while Bit 1 through Bit 0 are applied to the register.

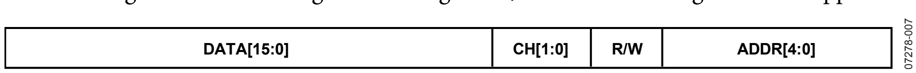


Figure 80.

Example 4

Read request and follow with a 2nd instruction (could be NOP) to clock out the data.

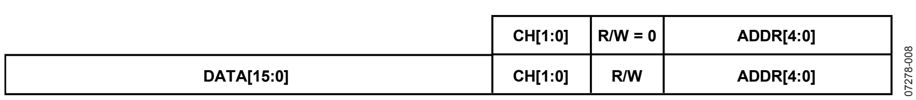


Figure 81.

Table 19. Channel Selection

Channel 1	Channel 0	Channel Selected
0	0	NOP (no channel selected, no register changes)
0	1	Channel 0 selected
1	0	Channel 1 selected
1	1	Channel 0 and Channel 1 selected

Table 20. R/W Definition

R/W	Description
0	Current register specified by address is shifted out of SDOUT on next shift operation
1	Current data is written to register specified by address and channel select

WRITE OPERATION

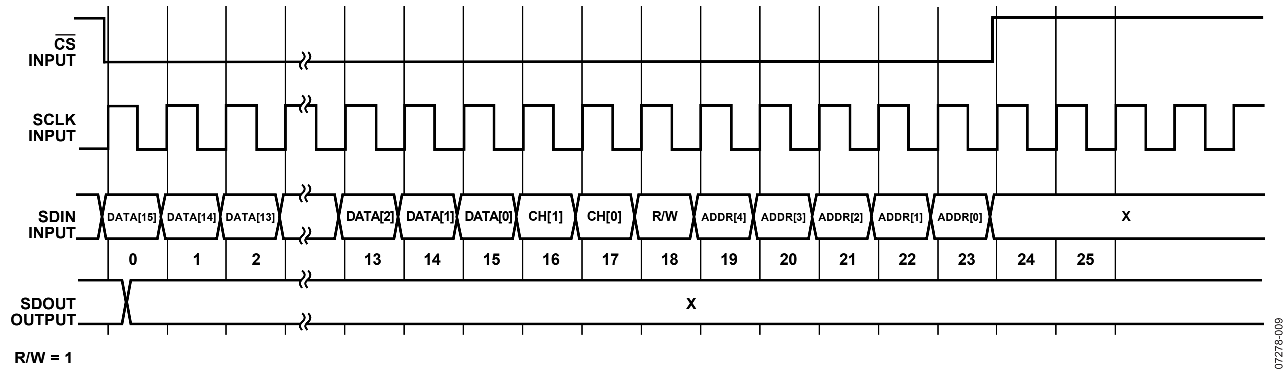


Figure 82. 16-Bit SPI Write

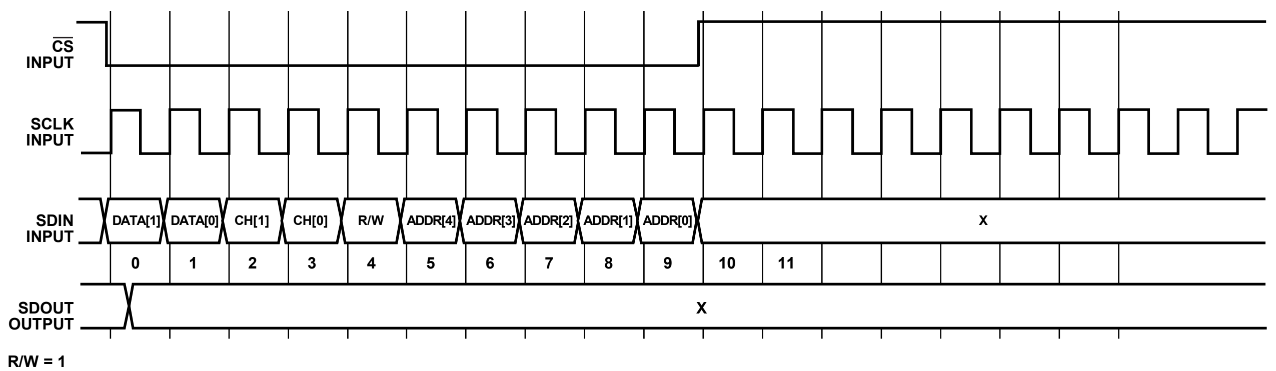


Figure 83. 2-Bit SPI Write

READ OPERATION

The read operation is a two-stage operation. First, a word is shifted in, specifying which register to read. $\overline{CS}$ is deasserted for three clock cycles, and then a second word is shifted in to get the readback data. This second word can be either another operation or an NOP address. If another operation is shifted in, it needs to shift in at least eight bits of data to read back the previous specified data. The NOP address can be used for this read if there is no need to write/read another register. It is strongly recommended that the NOP address be used for all reads for clarity of operations.

Any register read that is less than 16 bits has zeros filled in the top bits to make it a 16-bit word.

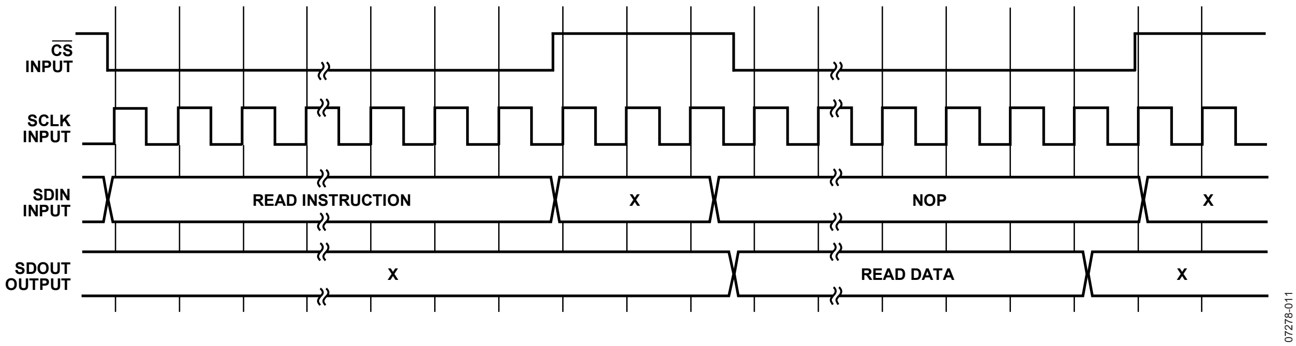


Figure 84. SPI Read Overview

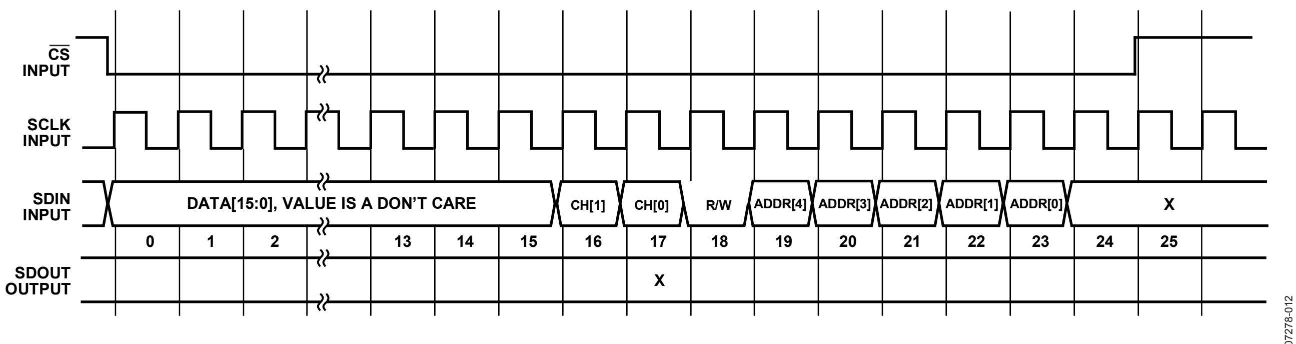


Figure 85. SPI Read—Details of Read Request

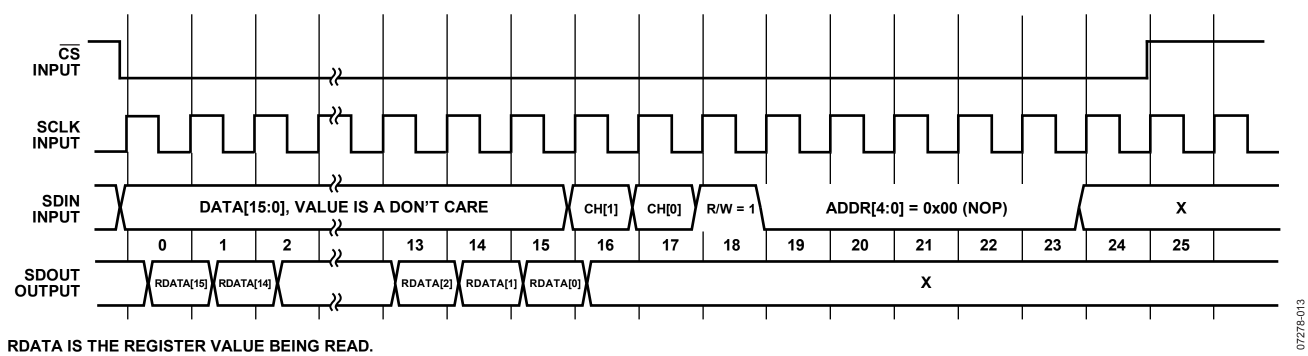


Figure 86. SPI Read—Details of Read Out

RESET OPERATION

The ADATE302-02 contains an asynchronous reset feature. The ADATE302-02 can be reset to the default values shown in Table 21 by utilizing the $\overline{RST}$ pin. To initiate the reset operation, deassert the $\overline{RST}$ pin for a minimum of 100 ns and deassert the $\overline{CS}$ pin for a minimum of two SCLK cycles.

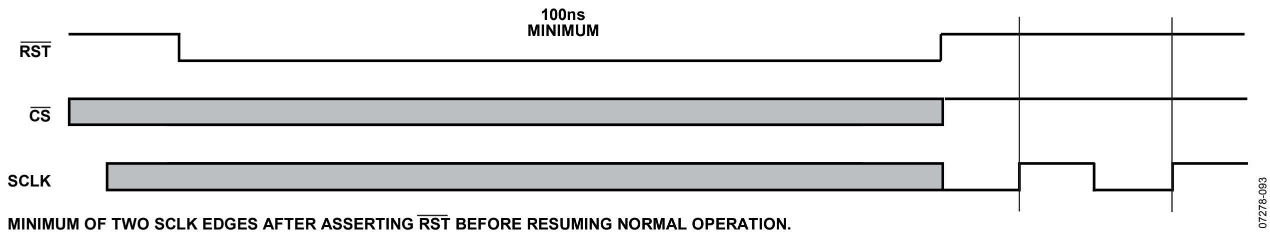


Figure 87. Reset Operation

REGISTER MAP

The ADDR[4:0] bits determine the destination register of the data being written to the ADATE302-02.

Table 21. Register Selection

Data[15:0]	CH[1:0]	R/W	ADDR[4:0]	Register Selected	Reset State
N/A	N/A	N/A	0x00	NOP	N/A
Data[13:0]	CH[1:0]	R/W	0x01	VH DAC level	4096d
Data[13:0]	CH[1:0]	R/W	0x02	VL DAC level	4096d
Data[13:0]	CH[1:0]	R/W	0x03	VT/VCOM DAC level	4096d
Data[13:0]	CH[1:0]	R/W	0x04	VOL DAC level	4096d
Data[13:0]	CH[1:0]	R/W	0x05	VOH DAC level	4096d
Data[13:0]	CH[1:0]	R/W	0x06	VCH DAC level	4096d
Data[13:0]	CH[1:0]	R/W	0x07	VCL DAC level	4096d
Data[13:0]	CH[1:0]	R/W	0x08	V(IOH) DAC level	4096d
Data[13:0]	CH[1:0]	R/W	0x09	V(IOL) DAC level	4096d
Data[13:0]	CH[1]	R/W	0x0A	OVD high level	4096d
Data[13:0]	CH[0]	R/W	0x0A	OVD low level	4096d
Data[15:0]	CH[1:0]	R/W	0x0B	PMUDAC level	16384d
Data[2:0]	CH[1:0]	R/W	0x0C	PE/PMU enable	000b
Data[2:0]	CH[1:0]	R/W	0x0D	Channel state	000b
Data[9:0]	CH[1:0]	R/W	0x0E	PMU state	0d
Data[2:0]	CH[1:0]	R/W	0x0F	PMU measure enable	000b
Data[0]	CH[1:0]	R/W	0x10	Differential comparator enable	0b
Data[1:0]	CH[1:0]	R/W	0x11	16-bit DAC monitor	00b
Data[1:0]	CH[1:0]	R/W	0x12	OVD_CHx alarm mask	01b
Data[2:0]	CH[1:0]	R	0x13	OVD_CHx alarm state	N/A
N/A	N/A	N/A	0x14 to 0x1F	Reserved	N/A

DETAILS OF REGISTERS

Table 22. PE/PMU Enable (ADDR[4:0] = 0x0C)

Bit	Name	Description
Data[2]	PMU enable	0 = disable PMU force output and clamps, place PMU in MV mode 1 = enable PMU force output When set to 0, the PMU State bits are ignored, except for PMU Sense Path (Data[7]).
Data[1]	Force VT	0 = normal driver operation 1 = force driver to V_T See Table 30 for complete functionality of this bit.
Data[0]	PE disable	0 = enable driver functions 1 = disable driver (low leakage) See Table 30 for complete functionality of this bit.

Table 23. Channel State (ADDR[4:0] = 0x0D)

Bit	Name	Description
Data[2]	HVOUT mode select	0 = HVOUT driver in low impedance 1 = enable HVOUT driver This bit affects Channel 0 only. Ensure that Channel 0 bit in SPI write is active. Channel 1 bit in SPI write is don't care.
Data[1]	Load enable	0 = disable load 1 = enable load See Table 30 for complete functionality of this bit.
Data[0]	Driver high-Z/VT	0 = enable driver high-Z function 1 = enable driver VTERM function See Table 30 for complete functionality of this bit.

Table 24. PMU State (ADDR[4:0] = 0x0E)[1, 2]

Bit	Name	Description
Data[9:8]	PMU input selection	00 = V_{DUTGND} (calibrated for 0.0 V voltage reference) 01 = 2.5 V + V_{DUTGND} (calibrated for 0.0 A current reference) 1X = PMUDAC
Data[7]	PMU sense path	0 = internal sense 1 = external sense
Data[6]	Reserved	
Data[5]	PMU clamp enable	0 = disable clamps 1 = enable clamps
Data[4]	PMU measure V/I	0 = measure voltage mode 1 = measure current mode
Data[3]	PMU force V/I	0 = force voltage mode 1 = force current mode
Data[2:0]	PMU range	0XX = Range E (2 μA) 100 = Range D (20 μA) 101 = Range C (200 μA) 110 = Range B (2 mA) 111 = Range A (25 mA)

[1] Note that when the ADDR[4:0] = 0x0C PMU enable bit (Data[2]) = 0, the PMU force outputs and clamps are disabled, and the PMU is placed into measure voltage mode. Data[9:8] and Data[6:0] of the PMU state register are ignored, and only Data[7], the PMU sense path bit, is valid.
[2] X = don't care.

Table 25. PMU Measure Enable (ADDR[4:0] = 0x0F)[1]

Bit	Name	Description
Data[2:1]	MEASOUT01 select	00 = PMU MEASOUT Channel 0 01 = PMU MEASOUT Channel 1 10 = Temp sensor ground reference 11 = Temp sensor
Data[0]	MEASOUT01 output enable	0 = MEASOUT01 is tristated 1 = MEASOUT01 is enabled

[1] This register is written to or read from if either of the CH[1:0] bits is 1.

Table 26. Differential Comparator Enable (ADDR[4:0] = 0x10)[1]

Bit	Name	Description
Data[0]	Differential comparator enable	0 = differential comparator is disabled, Channel 0 normal window comparator (NWC) outputs are on Channel 0 1 = differential comparator is enabled, the differential comparator outputs are on Channel 0

[1] This register is written to or read from if either of the CH[1:0] bits is 1.

Table 27. DAC16_MON (16-Bit DAC Monitor) (ADDR[4:0] = 0x11)[1]

Bit	Name	Description
Data[1]	16-bit DAC mux enable	0 = 16-bit DAC mux is tristated 1 = 16-bit DAC mux is enabled
Data[0]	16-bit DAC mux select	0 = 16-bit DAC Channel 0 1 = 16-bit DAC Channel 1

[1] This register is written to or read from if either of the CH[1:0] bits is 1.

Table 28. OVD_CHx Alarm Mask (ADDR[4:0] = 0x12)

Bit	Name	Description
Data[1]	PMU mask	0 = disable PMU alarm flag 1 = enable PMU alarm flag
Data[0]	OVD mask	0 = disable OVD alarm flag 1 = enable OVD alarm flag

Table 29. OVD_CHx Alarm State (ADDR[4:0] = 0x13)[1]

Bit	Name	Description
Data[2]	PMU clamp flag	0 = PMU not clamped 1 = PMU clamped
Data[1]	OVD high flag	0 = DUT voltage < OVD high voltage 1 = DUT voltage > OVD high voltage
Data[0]	OVD low flag	0 = DUT voltage > OVD low voltage 1 = DUT voltage < OVD low voltage

[1] This register is a read-only register.

USER INFORMATION

Table 30. Driver and Load Truth Table[1]

Registers				Signals			
PE Disable Data[0] ADDR[4:0] = 0x0C	Force VT Data[1] ADDR[4:0] = 0x0C	Load Enable Data[1] ADDR[4:0] = 0x0D	Driver High-Z/VT Data[0] ADDR[4:0] = 0x0D	DATAx	RCVx	Driver State	Load State
1	X	X	X	X	X	High-Z without clamps	Power-down
0	1	X	X	X	X	VT	Power-down
0	0	0	0	0	0	VL	Power-down
0	0	0	0	0	1	High-Z with clamps	Power-down
0	0	0	0	1	0	VH	Power-down
0	0	0	0	1	1	High-Z with clamps	Power-down
0	0	0	1	0	0	VL	Power-down
0	0	0	1	0	1	VT	Power-down
0	0	0	1	1	0	VH	Power-down
0	0	0	1	1	1	VT	Power-down
0	0	1	0	0	0	VL	Active off
0	0	1	0	0	1	High-Z with clamps	Active on
0	0	1	0	1	0	VH	Active off
0	0	1	0	1	1	High-Z with clamps	Active on
0	0	1	1	0	0	VL	Active on
0	0	1	1	0	1	High-Z with clamps	Active on
0	0	1	1	1	0	VH	Active on
0	0	1	1	1	1	High-Z with clamps	Active on

[1] X = don't care.

Table 31. HVOUT Truth Table[1]

HVOUT Mode Select Data[2] ADDR[4:0] = 0x0D	Channel 0 RCV	Channel 0 Data	HVOUT Driver Output
1	1	X	VHH mode; VHH = (VT + 1 V) × 2 + DUTGND (Channel 0 VT DAC)
1	0	0	VL (Channel 0 VL DAC)
1	0	1	VH (Channel 0 VH DAC)
0	X	X	Disabled (HVOUT pin set to 0 V low impedance)

[1] X = don't care.

Table 32. Comparator Truth Table

Differential Comparator Enable Data[0] ADDR[4:0] = 0x10	COMP_QH0	COMP_QL0	COMP_QH1	COMP_QL1
0	Normal window mode Logic high: VOH0 < V_{DUT0} Logic low: VOH0 > V_{DUT0}	Normal window mode Logic high: VOL0 < V_{DUT0} Logic low: VOL0 > V_{DUT0}	Normal window mode Logic high: VOH1 < V_{DUT1} Logic low: VOH1 > V_{DUT1}	Normal window mode Logic high: VOL1 < V_{DUT1} Logic low: VOL1 > V_{DUT1}
1	Differential comparator mode Logic high: VOH0 < $V_{DUT0} - V_{DUT1}$ Logic low: VOH0 > $V_{DUT0} - V_{DUT1}$	Differential comparator mode Logic high: VOL0 < $V_{DUT0} - V_{DUT1}$ Logic low: VOL0 > $V_{DUT0} - V_{DUT1}$	Normal window mode Logic high: VOH1 < V_{DUT1} Logic low: VOH1 > V_{DUT1}	Normal window mode Logic high: VOL1 < V_{DUT1} Logic low: VOL1 > V_{DUT1}

DETAILS OF DACs vs. LEVELS

There are ten 14-bit DACs per channel. These DACs provide levels for the driver, comparator, load currents, VHH buffer, OVD, and clamp levels. There are three versions of output levels:

- −2.5 V to +7.5 V; tracks DUTGND. Controls VH, VL, VT/VCOM/VHH, VOH, VOL, VCH, and VCL levels.
- −3.0 V to +7.0 V; tracks DUTGND. Controls OVD levels.
- −2.5 V to +7.5 V; does not track DUTGND. Controls IOH and IOL levels.

There is one 16-bit DAC per channel. This DAC provides the levels for the PMU. The output level is:

- −2.5 V to +7.5 V; tracks DUTGND. Controls PMU levels.

Table 33. Level Transfer Functions

DAC Transfer Function	Programmable Range[1] (All 0s to All 1s)	Levels
$V_{OUT} = 2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{14})) - 0.5 \times (V_{REF} - V_{REF\_GND}) + V_{DUTGND}$ $Code = [V_{OUT} - V_{DUTGND} + 0.5 \times (V_{REF} - V_{REF\_GND})] \times [(2^{14})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−2.5 V to +7.5 V	VH, VL, VT/VCOM, VOL, VOH, VCH, VCL
$V_{OUT} = 4.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{14})) - 1.0 \times (V_{REF} - V_{REF\_GND}) + 2.0 + V_{DUTGND}$ $Code = [V_{OUT} - V_{DUTGND} - 2.0 + 1.0 \times (V_{REF} - V_{REF\_GND})] \times [(2^{14})/(4.0 \times (V_{REF} - V_{REF\_GND}))]$	−3.0 V to +17.0 V	VHH
$V_{OUT} = 2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{14})) - 0.6 \times (V_{REF} - V_{REF\_GND}) + V_{DUTGND}$ $Code = [V_{OUT} - V_{DUTGND} + 0.6 \times (V_{REF} - V_{REF\_GND})] \times [(2^{14})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−3.0 V to +7.0 V	OVD
$I_{OUT} = [2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{14})) - 0.5 \times (V_{REF} - V_{REF\_GND})] \times (0.012/5.0)$ $Code = [(I_{OUT} \times (5.0/0.012)) + 0.5 \times (V_{REF} - V_{REF\_GND})] \times [(2^{14})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−6 mA to +18 mA	IOH, IOL
$V_{OUT} = 2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{16})) - 0.5 \times (V_{REF} - V_{REF\_GND}) + V_{DUTGND}$ $Code = [V_{OUT} - V_{DUTGND} + 0.5 \times (V_{REF} - V_{REF\_GND})] \times [(2^{16})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−2.5 V to +7.5 V	PMUDAC
$I_{OUT} = [2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{16})) - 0.5 \times (V_{REF} - V_{REF\_GND}) - 2.5] \times (0.050/5.0)$ $Code = [(I_{OUT} \times (5.0/0.050)) + 2.5 + 0.5 \times (V_{REF} - V_{REF\_GND})] \times [(2^{16})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−50 mA to +50 mA	PMUDAC (PMU FI Range A)
$I_{OUT} = [2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{16})) - 0.5 \times (V_{REF} - V_{REF\_GND}) - 2.5] \times (0.004/5.0)$ $Code = [(I_{OUT} \times (5.0/0.004)) + 2.5 + 0.5 \times (V_{REF} - V_{REF\_GND})] \times [(2^{16})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−4 mA to +4 mA	PMUDAC (PMU FI Range B)
$I_{OUT} = [2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{16})) - 0.5 \times (V_{REF} - V_{REF\_GND}) - 2.5] \times (0.0004/5.0)$ $Code = [(I_{OUT} \times (5.0/0.0004)) + 2.5 + 0.5 \times (V_{REF} - V_{REF\_GND})] \times [(2^{16})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−400 µA to +400 µA	PMUDAC (PMU FI Range C)
$I_{OUT} = [2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{16})) - 0.5 \times (V_{REF} - V_{REF\_GND}) - 2.5] \times (0.00004/5.0)$ $Code = [(I_{OUT} \times (5.0/0.00004)) + 2.5 + 0.5 \times (V_{REF} - V_{REF\_GND})] \times [(2^{16})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−40 µA to +40 µA	PMUDAC (PMU FI Range D)
$I_{OUT} = [2.0 \times (V_{REF} - V_{REF\_GND}) \times (Code/(2^{16})) - 0.5 \times (V_{REF} - V_{REF\_GND}) - 2.5] \times (0.000004/5.0)$ $Code = [(I_{OUT} \times (5.0/0.000004)) + 2.5 + 0.5 \times (V_{REF} - V_{REF\_GND})] \times [(2^{16})/(2.0 \times (V_{REF} - V_{REF\_GND}))]$	−4 µA to +4 µA	PMUDAC (PMU FI Range E)

[1] Programmable range includes margin outside of specified part performance, allowing for offset/gain calibration.

Table 34. Load Transfer Functions

Load Level	Transfer Function[1]
IOL	V(IOL)/5 V × 12 mA
IOH	V(IOH)/5 V × 12 mA

[1] V(IOH), V(IOL) DAC levels are not referenced to DUTGND.

Table 35. PMU Transfer Functions

PMU Mode	Transfer Function
Force Voltage	$V_{OUT} = PMUDAC$
Measure Voltage	$V_{MEASOUT01} = V_{DUTx}$ (internal sense) or $V_{MEASOUT01} = V_{PMUS\_CHx}$ (external sense)
Force Current	$I_{OUT} = [PMUDAC - (V_{REF}/2)]/(R^1 \times 5)$
Measure Current	$V_{MEASOUT01} = (V_{REF}/2) + V_{DUTGND} + (I_{DUTx} \times 5 \times R^1)$

[1] R = 20 Ω for Range A; 250 Ω for Range B; 2.5 kΩ for Range C; 25 kΩ for Range D; 250 kΩ for Range E.

Table 36. PMU User Required Capacitors

Capacitor	Location
220 pF	Across Pin C10 (FFCAP_0B) and Pin E10 (FFCAP_0A)
220 pF	Across Pin C1 (FFCAP _1B) and Pin E1 (FFCAP_1A)
330 pF	Between GND and Pin B9 (SCAP0)
330 pF	Between GND and Pin B2 (SCAP1)

Table 37. Temperature Sensor

Temperature	Output
0 K	0 V
300 K	3 V
x K	(x K) × 10 mV/K

Table 38. Default Test Conditions

Name	Default Test Condition
VH DAC Level	2.0 V
VL DAC Level	0.0 V
VT/VCOM DAC Level	1.0 V
VOL DAC Level	−2.0 V
VOH DAC Level	6.0 V
VCH DAC Level	7.5 V
VCL DAC Level	−2.5 V
IOH DAC Level	0.0 A
IOL DAC Level	0.0 A
OVD Low DAC Level	−2.5 V
OVD High DAC Level	6.5 V
PMUDAC DAC Level	0.0 V
PE/PMU Enable	0x0000: PMU disabled, not force VT, PE enabled
Channel State	0x0000: HVOUT mode disabled, load disabled, VTERM inactive
PMU State	0x0000: input of DUTGND, internal sense, clamps disabled, FVMV, Range E
PMU Measure Enable	0x0000: MEASOUT01 pin tristated
Differential Comparator Enable	0x0000: normal window comparator mode
16-Bit DAC Monitor	0x0000: DAC16_MON tristated
OVD_CHx Alarm Mask	0x0000: disable alarm functions
Data Input	Logic low
Receive Input	Logic low
DUTx Pin	Unterminated
Comparator Output	Unterminated

RECOMMENDED PMU MODE SWITCHING SEQUENCES

To minimize any possible aberrations and voltage spikes on the DUT output, specific mode switching sequences are recommended for the following transitions:

- PMU disable to PMU enable
- PMU force voltage mode to PMU force current mode
- PMU force current mode to PMU force voltage mode.

PMU Disable to PMU Enable

Step 1: See Table 39 for state of registers in PMU disabled mode.

Table 39.

Register	Bit	Setting
PE/PMU Enable Register, ADDR[4:0] = 0x0C	Data[2]	0
PMU State Register, ADDR[4:0] = 0x0E	Data[9:8]	XX
	Data[7]	X
	Data[6]	X
	Data[5]	X
	Data[4]	X
	Data[3]	X
	Data[2:0]	XXX

Step 2: Write to Register ADDR[4:0] = 0x0E (see Table 40).

Table 40.

Register	Bit	Setting	Comments
PMU State Register, ADDR[4:0] = 0x0E	Data[9:8]	1X or 00	Set desired input selection
	Data[7]	X	
	Data[6]	X	
	Data[5]	X	
	Data[4]	X	
	Data[3]	0	This bit must be set to force voltage mode to reduce aberrations
	Data[2:0]	XXX	Set desired range

Step 3: Write to Register ADDR[4:0] = 0x0C (see Table 41).

Table 41.

Register	Bit	Setting	Comments
PE/PMU Enable Register, ADDR[4:0] = 0x0C	Data[2]	1	PMU is now enabled in force voltage mode

PMU Force Voltage Mode to PMU Force Current Mode

Step 1: See Table 42 for state of registers in force voltage mode.

Table 42.

Register	Bit	Setting
PE/PMU Enable Register, ADDR[4:0] = 0x0C	Data[2]	1
PMU State Register, ADDR[4:0] = 0x0E	Data[9:8]	XX
	Data[7]	X
	Data[6]	X
	Data[5]	X
	Data[4]	X
	Data[3]	0
	Data[2:0]	XXX

Step 2: Write to Register ADDR[4:0] = 0x0E (see Table 43).

Table 43.

Register	Bit	Setting	Comments
PMU State Register, ADDR[4:0] = 0x0E	Data[9:8]	01	Set 2.5 V + V_{DUTGND} input selection
	Data[7]	X	
	Data[6]	X	
	Data[5]	X	
	Data[4]	X	
	Data[3]	1	Set to force current mode
	Data[2:0]	0XX	2 μA range has the minimum offset current

Step 3: Write to Register ADDR[4:0] = 0x0B (see Table 44).

Table 44.

Register	Bit	Setting	Comments
PMUDAC Level, ADDR[4:0] = 0x0B	Data[15:0]	X	Update the PMUDAC level register to the desired value

Step 4: Write to Register ADDR[4:0] = 0x0E (see Table 45).

Table 45.

Register	Bit	Setting	Comments
PMU State Register, ADDR[4:0] = 0x0E	Data[9:8]	1X	PMUDAC input selection
	Data[7]	X	
	Data[6]	X	
	Data[5]	X	
	Data[4]	X	
	Data[3]	1	Set to force current mode
	Data[2:0]	XXX	Set to the desired current range

Transition from PMU Force Current Mode to PMU Force Voltage Mode

Step 1: See Table 46 for state of registers in force current mode.

Table 46.

Register	Bits	Setting
PE/PMU Enable Register, ADDR[4:0] = 0x0C	Data[2]	1
PMU State Register, ADDR[4:0] = 0x0E	Data[9:8]	XX
	Data[7]	X
	Data[6]	X
	Data[5]	X
	Data[4]	X
	Data[3]	1
	Data[2:0]	XXX

Step 2: Write to Register ADDR[4:0] = 0x0E (see Table 47).

Table 47.

Register	Bits	Setting	Comments
PMU State Register, ADDR[4:0] = 0x0E	Data[9:8]	00	Set DUTGND input selection
	Data[7]	X	
	Data[6]	X	
	Data[5]	X	
	Data[4]	X	
	Data[3]	0	Set to force voltage mode
	Data[2:0]	XXX	Set to the desired current range

Step 3: Write to Register ADDR[4:0] = 0x0B (see Table 48).

Table 48.

Register	Bits	Setting	Comments
PMUDAC Level, ADDR[4:0] = 0x0B	Data[15:0]	X	Update the PMUDAC level register to the desired value

Step 4: Write to Register ADDR[4:0] = 0x0E (see Table 49).

Table 49.

Register	Bits	Setting	Comments
PMU State Register, ADDR[4:0] = 0x0E	Data[9:8]	1X	PMUDAC input selection
	Data[7]	X	
	Data[6]	X	
	Data[5]	X	
	Data[4]	X	
	Data[3]	0	Force voltage mode
	Data[2:0]	XXX	

BLOCK DIAGRAMS

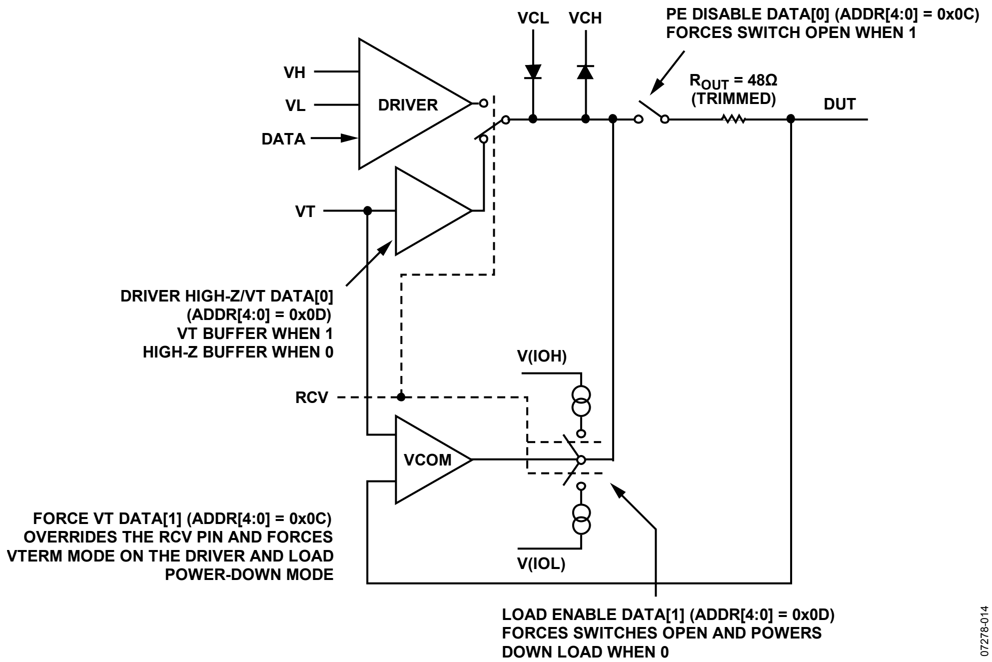


Figure 88. Driver and Load Block Diagram

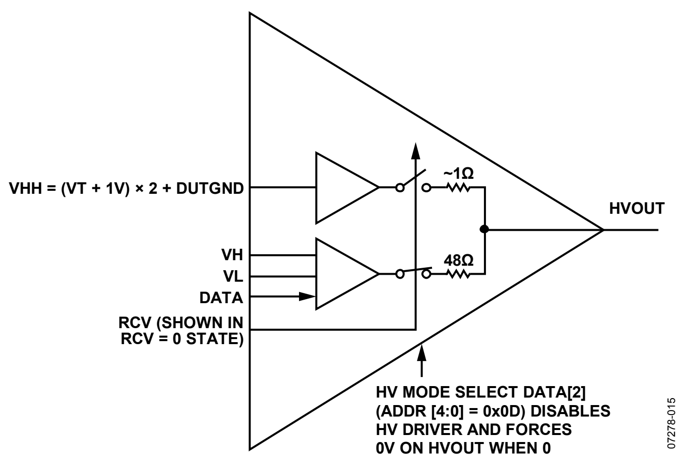


Figure 89. HVOUT Driver Output Stage

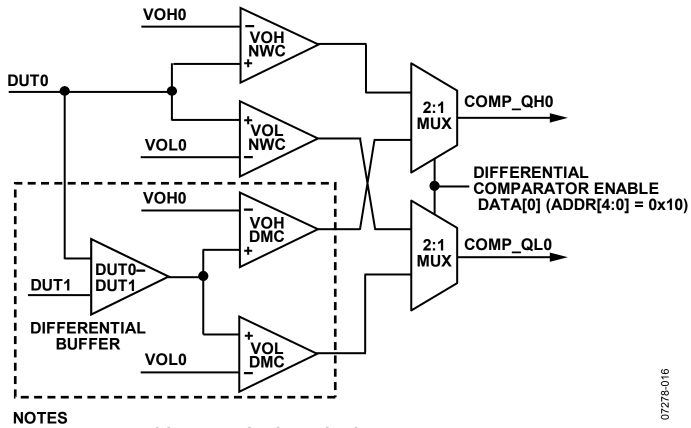


Figure 90. Comparator Block Diagram

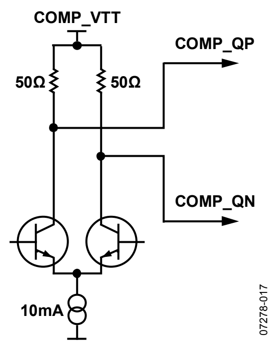


Figure 91. Comparator Output Scheme

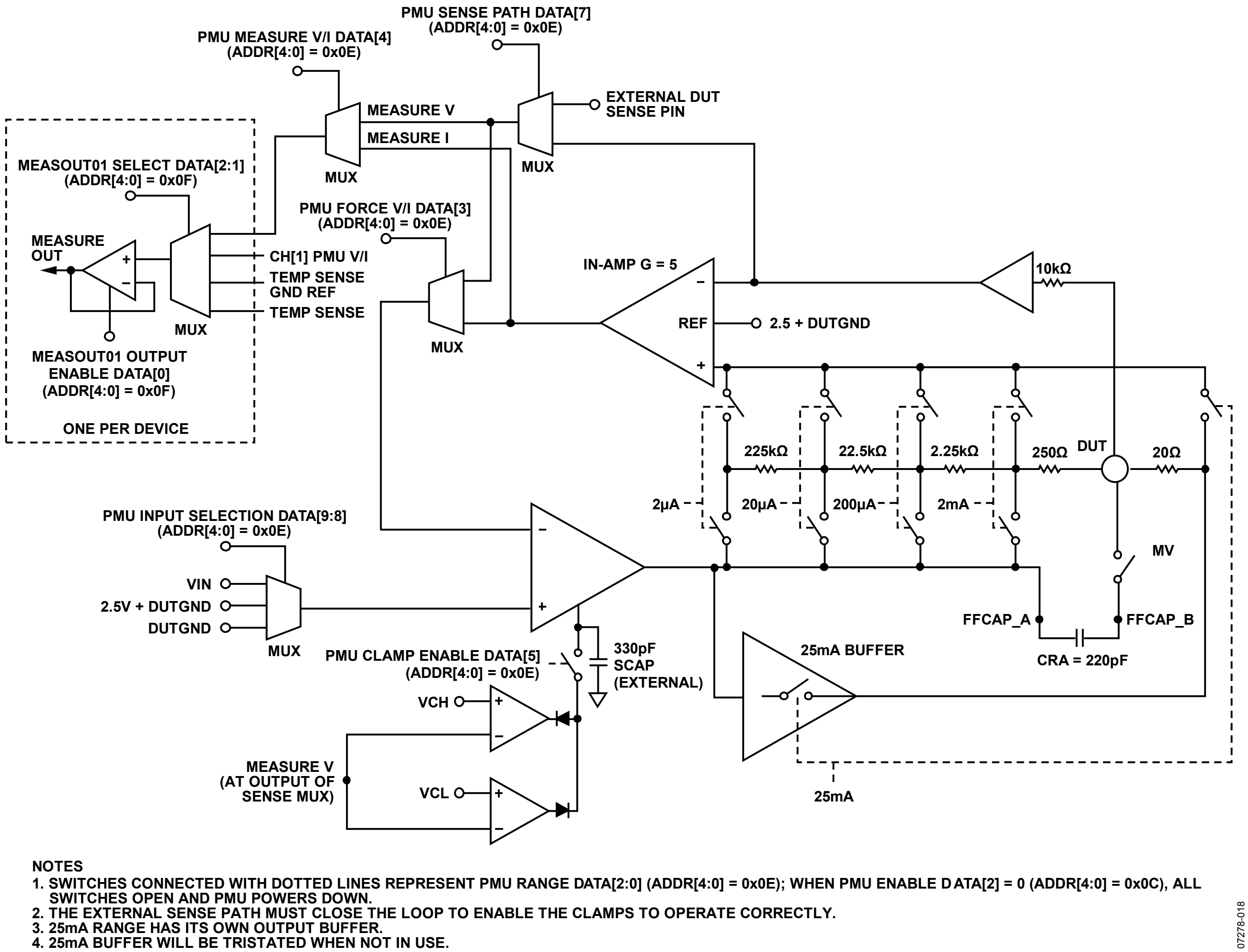
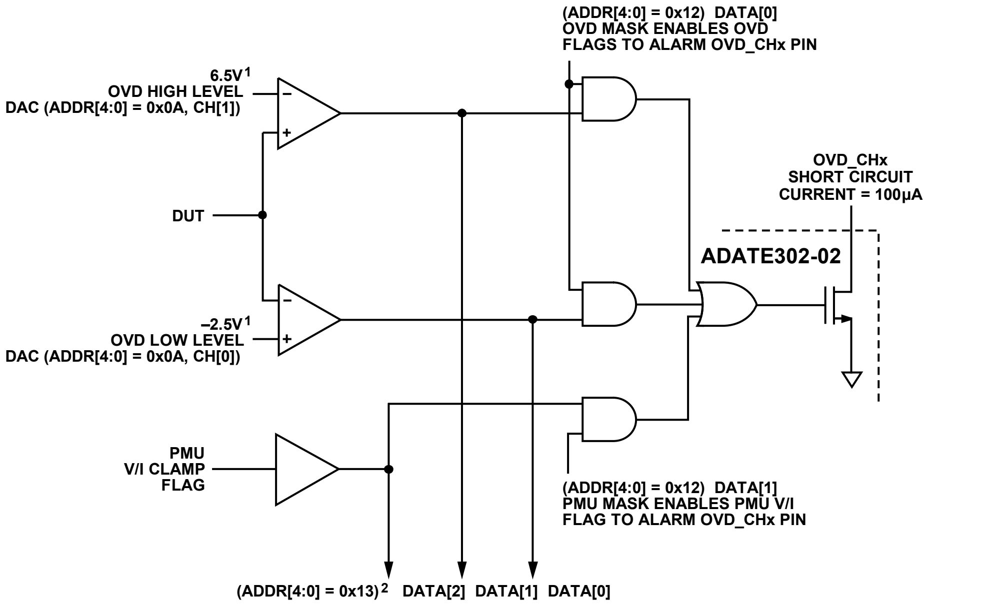


Figure 92. PMU Block Diagram

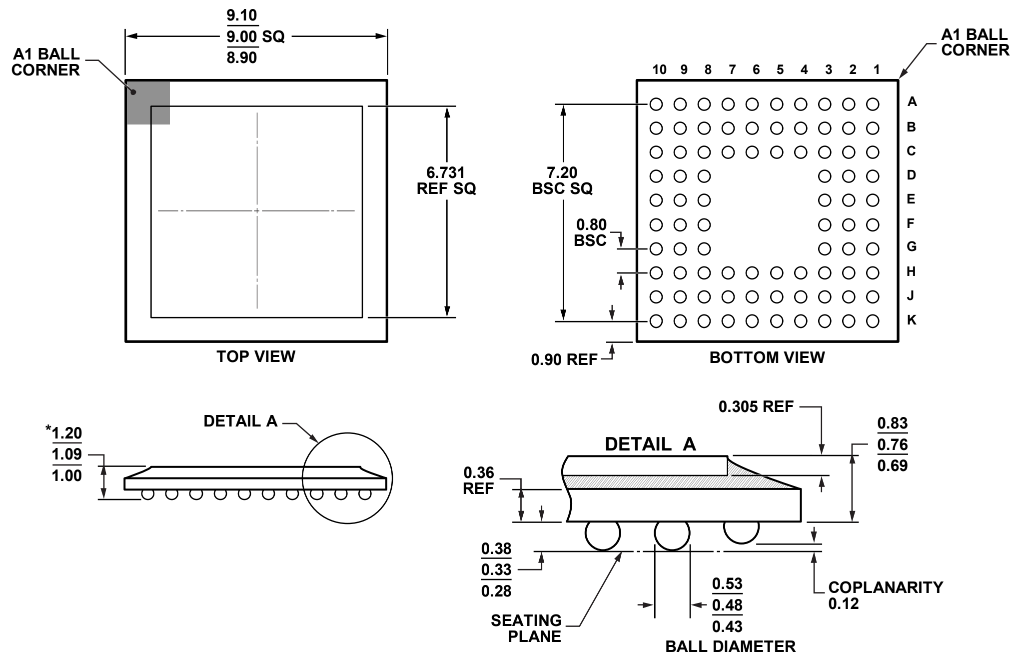


[1] THE OVD HIGH/LOW LEVEL DAC IS SHARED BY EACH CHANNEL; THEREFORE, ONLY ONE OVD HIGH/LOW VOLTAGE LEVEL CAN BE SET PER CHIP. THE OVD DACs PROVIDE A VOLTAGE RANGE OF –3V TO +7V. THE RECOMMENDED HIGH/LOW SETTINGS ARE +6.5V/–2.5V. (THESE VALUES NEED TO BE PROGRAMMED BY THE USER UPON STARTUP/RESET.)

[2] THIS IS A READ ONLY REGISTER THAT ALLOWS THE USER TO DETERMINE THE CAUSE OF THE ACTIVE OVD FLAG.

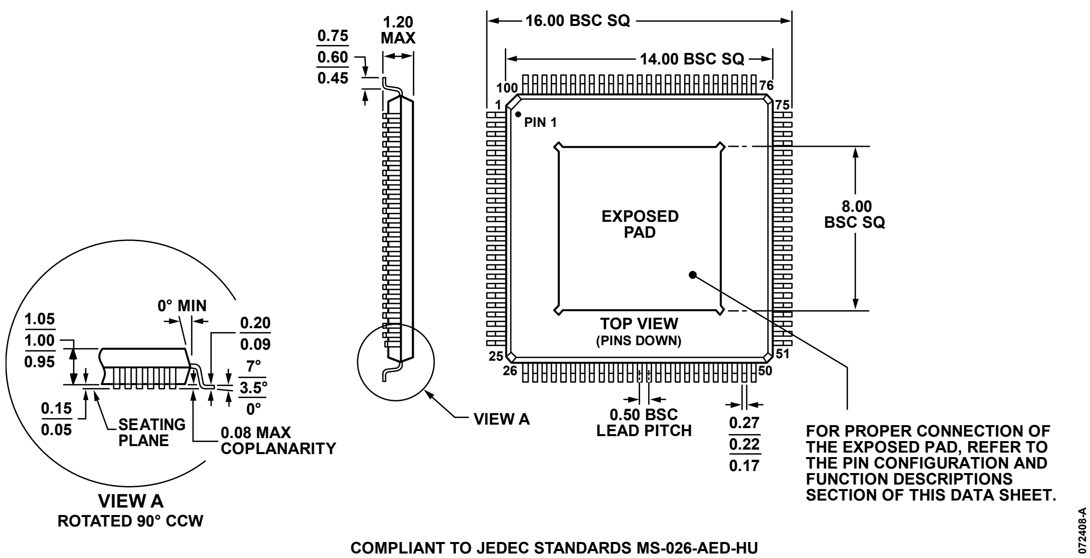
Figure 93. OVD Block Diagram

OUTLINE DIMENSIONS



*COMPLIANT TO JEDEC STANDARDS MO-219 WITH EXCEPTION TO PACKAGE HEIGHT.

Figure 94. 84-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-84-2)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-AED-HU

Figure 95. 100-Lead Thin Quad Flatpack, Exposed Pad [TQFP_EP]
(SV-100-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADATE302-02BBCZ[1]	−40°C to +85°C	84-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-84-2
ADATE302-02BSVZ[1]	−40°C to +85°C	100-Lead Thin Quad Flatpack, Exposed Pad [TQFP_EP]	SV-100-7

[1] Z = RoHS Compliant Part.

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