

LTC3876EUHF

High Efficiency, Dual Output DDR Power Supply

DESCRIPTION

Demonstration circuit 1631A is a dual output DDR2/3 power supply operating with a switching frequency of 400kHz over an input voltage range of 4.5V to 14V. The fixed on-time valley current mode control of the LTC[®]3876 allows for a fast load step response (see Figure 3). The load step response can be tested with the onboard load step circuit and a bench pulse generator.

The demo board uses a high density, two sided drop-in layout. The entire converter, excluding the bulk output and input capacitors, fits within a compact 1.5" × 1.0" area on the board. The package style for the LTC3876EUHF is a 38-pin 5mm × 7mm QFN with an exposed ground pad.

The main features of the board are listed below:

- MODE jumper to program either discontinuous mode (DCM) or forced continuous mode (FCM) at light or no load.
- EXTVCC pin.
- PLLIN pin to synchronize the converter to an external clock.
- Remote sensing for V_{DDQ} .
- RUN pin, PGOOD pin and TRACK/SS pin.

Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY (T_A = 25°C)

| PARAMETER | CONDITIONS | VALUE |
|---|--|--------------------|
| Minimum Input Voltage | | 4.5V |
| Maximum Input Voltage | | 14V |
| Output Voltage V_{DDQ} | $I_{DDQ} = 0A$ to 20A, $V_{IN} = 4.5V$ to 14V | 1.8V/1.5V ± 2% |
| Output Voltage V_{TT} | $I_{TT} = 0A$ to 10A, $V_{IN} = 4.5V$ to 14V, $V_{TTR} = 0.9V/0.75V$ | $V_{TTR} \pm 15mV$ |
| V_{DDQ} Maximum Output Current, I_{DDQ} | $V_{IN} = 4.5V$ to 14V, $V_{DDQ} = 1.5V$ | 20A |
| V_{TT} Maximum Output Current, I_{TT} | $V_{IN} = 4.5V$ to 14V, $V_{TT} = 0.75V$ | 10A |
| Nominal Switching Frequency | | 400kHz |
| Efficiency See Figure 2 | $V_{DDQ} = 1.5V$, $I_{DDQ} = 20A$, $V_{IN} = 12V$ | 87% |

QUICK START PROCEDURE

Demonstration circuit 1631A is easy to set up to evaluate the performance of the LTC3876EUHF. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

- 1) With power off, connect the input supply, load and meters as shown in Figure 1. Preset the load to 0A and V_{IN} supply to be 0V. Place jumpers in the following positions:

| | | |
|-----|------|--------------------------|
| JP1 | MODE | CCM |
| JP2 | RUN1 | ON |
| JP4 | VFB1 | DDR3($V_{DDQ} = 1.5V$) |

Set jumper JP4 to DDR2 to make V_{DDQ} equal to 1.8V.

- 2) Adjust the input voltage to be between 4.5V to 14V. V_{DDQ} should be $1.5V \pm 2\%$.
 V_{TT} should be $0.75V \pm 2\%$.
- 3) Next, apply 20A load to V_{DDQ} and recheck V_{DDQ} voltage.

- 4) Apply 10A load to V_{TT} and recheck V_{TT} voltage.
- 5) Once the DC regulation is confirmed, observe the output voltage ripple, load step response, efficiency and other parameters.
- 6) (Optional) To check the current sinking capability of the V_{TT} output, connect a power resistor between V_{IN} and V_{TT} . The sinking current I_{SINK} can be calculated by $I_{SINK} = (V_{IN} - V_{TT})/R_{LOAD}$. The sinking current should not be more than 10A. The load resistor should be able to take maximum power of $P_{LOAD} = (V_{IN} - V_{TT}) \cdot I_{SINK}$. If an active load is used in the V_{TT} sinking current test, the ground of the active load should be floated/isolated.

Note 1. Use the BNC connectors labeled V_{DDQ} or V_{TT} to measure the output voltage ripple,

Note 2. Do not apply the load from the V_{DDQ}^+ turret to the V_{DDQ}^- turret or from the V_{TT}^+ turret to the V_{TT}^- turret. These turrets are only intended to monitor the voltage across COUT1 and COUT5 respectively. Heavy load currents applied across these turrets may damage the converter.

LOAD STEP TRANSIENT TESTING

Demonstration circuit 1631A provides a simple load step circuit consisting of a MOSFET and sense resistor for each rail. To apply a load step, follow the steps below.

- 1) Preset the amplitude of a pulse generator to 0.0V and the duty cycle to 5% or less.
- 2) Connect the scope to the V_{DDQ} BNC connectors for the rail under test with a coax cable. To monitor the load step current, connect the scope probe across the IO1(2)STEP and GND turrets for that rail.

- 3) Connect the output of the pulse generator to the IO1(2)STEP CLK turret for the rail under test and connect the return to one of the GND turrets.

- 4) With the converter running, slowly increase the amplitude of the pulse generator output to provide the desired load step pulse height. The scaling for the LOAD STEP signal is 2.5mV/A.

LOAD STEP TRANSIENT TESTING

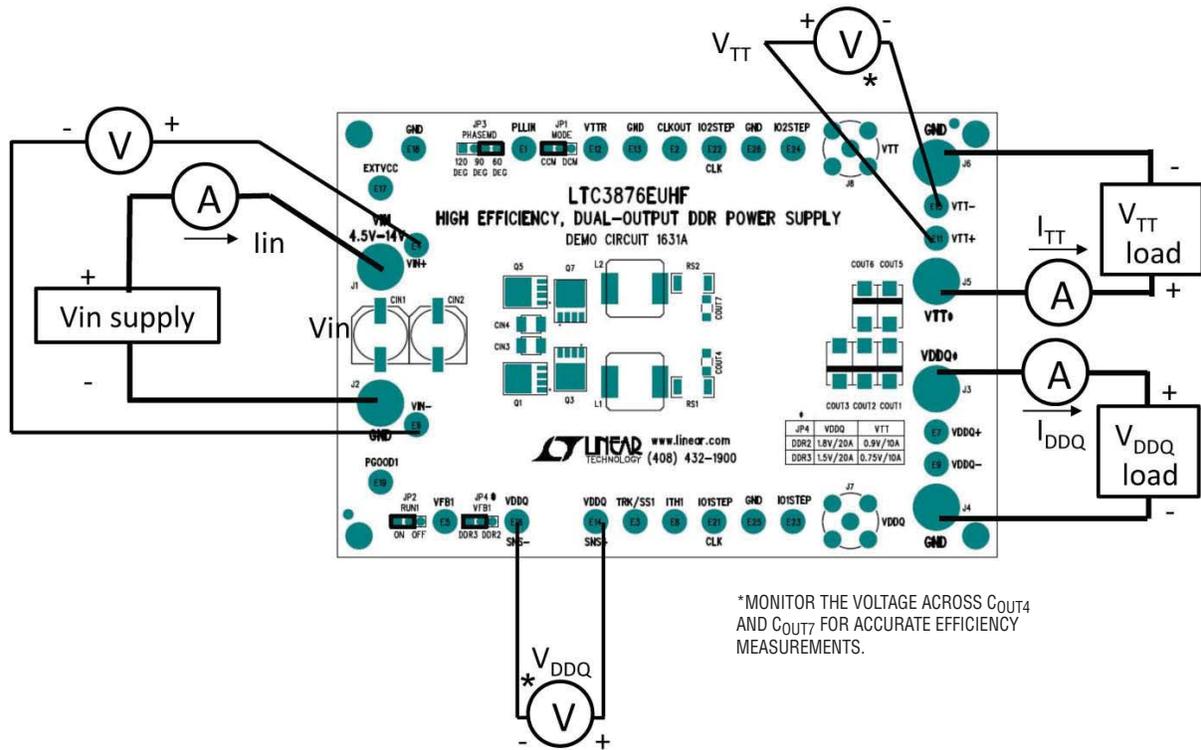


Figure 1. Proper Measurement Equipment Setup

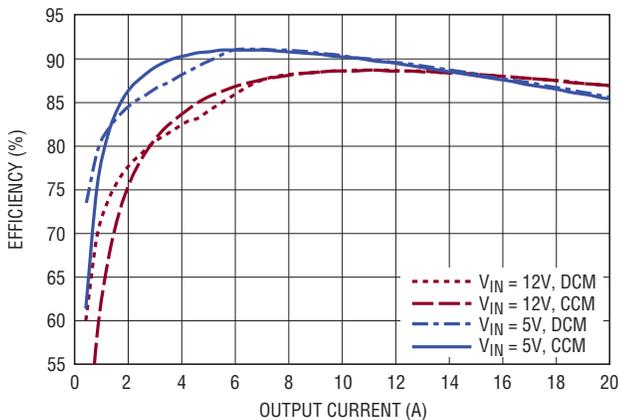


Figure 2. Efficiency Curves for the DC1631A VDDQ

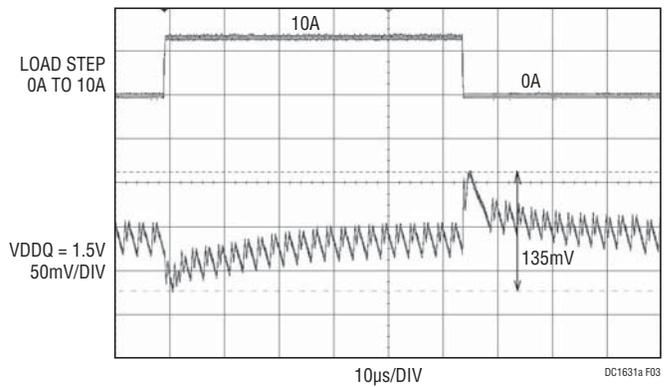


Figure 3. Load Step Response of the VDDQ on the DC1631A at $V_{IN} = 12V$. $C_{OUT} = 2 \times$ Sanyo 2R5TPE330M9 || $1 \times 100\mu F$ X5R 6.3V 1206, $L = 0.47\mu H$, $f_{SW} = 400kHz$

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PARTS LIST

| ITEM | QTY | REFERENCE | PART DESCRIPTION | MANUFACTURER/PART NUMBER |
|--|-----|--|--|-----------------------------------|
| Required Circuit Components | | | | |
| 1 | 2 | C8, C10 | CAP, 0603 100pF 10% 25V X7R | AVX 06033C101KAT |
| 2 | 4 | C4, C7, C14, C15 | CAP, 0603 1nF 10% 50V X7R | AVX 06035C102KAT |
| 3 | 3 | C2, C6, C16 | CAP, 0603 0.1 μ F 10% 25V X7R | TDK C1608X7R1E104K |
| 4 | 6 | C9, C11, C12, C18, C19, C20 | CAP, 0603 1 μ F 10% 16V X5R | AVX 0603YD105KAT |
| 6 | 1 | C17 | CAP, 1206 2.2 μ F 10% 10V X7R | TAIYO YUDEN LMK316B7225KL-T |
| 7 | 1 | C13 | CAP, 0805 4.7 μ F 10% 10V X5R | TAIYO YUDEN LMK212BJ475KG-T |
| 8 | 1 | CIN3 | CAP, 1210 10 μ F 20% 50V X5R | TAIYO YUDEN UMK325BJ106MM-T |
| 9 | 2 | COUT4, COUT7 | CAP, 1206 100 μ F 20% 6.3V X5R | MURATA GRM31CR60J107ME39L |
| 10 | 3 | COUT1, COUT2, COUT5 | CAP, 7343 330 μ F 20% 2.5V POSCAP | SANYO 2R5TPE330M9 |
| 11 | 1 | CIN4 | CAP, 1210 10 μ F 10% 25V X7R | AVX, 12103C106KAT2A |
| 12 | 2 | D2, D1 | DIODE, CMDSH-3 SOD323 | CENTRAL SEMI. CMDSH-3TR |
| 13 | 2 | L1, L2 | IND, 0.47 μ H | WE 7443330047 |
| 14 | 2 | Q1, Q5 | XSTR, N-CHANNEL MOSFET | RENESAS RJK0305DPB |
| 15 | 3 | Q3, Q4, Q7 | XSTR, N-CHANNEL MOSFET | RENESAS RJK0330DPB |
| 16 | 1 | RS1 | RES, 2010 0.001 Ω 1% 1/2W | VISHAY WSL20101L000FEA |
| 17 | 1 | RS2 | RES, 2010 0.002 Ω 1% 1/2W | VISHAY WSL20102L000FEA |
| 18 | 10 | R4, R5, R15, R19, R20, R27, R29, R34, R42, R43 | RES, 0603 0 Ω JUMPER | VISHAY CRCW06030000Z0EA |
| 19 | 1 | R23 | RES, 0603 2.2 Ω 5% 1/10W | VISHAY CRCW06032R20JNEA |
| 20 | 4 | R7, R14, R24, R40 | RES, 0603 10 Ω 5% 1/10W | VISHAY CRCW060310R0JNEA |
| 21 | 4 | R9, R10, R38, R39 | RES, 0603 100 Ω 5% 1/10W | VISHAY CRCW0603100RJNEA |
| 22 | 1 | R25 | RES, 0603 7.5k Ω 1% 1/10W | VISHAY CRCW06037K50FKEA |
| 23 | 2 | R2, R12 | RES, 0603 20k Ω 1% 1/10W | VISHAY CRCW060320K0FKEA |
| 24 | 1 | R21 | RES, 0603 15k Ω 1% 1/10W | VISHAY CRCW060315K0FKEA |
| 25 | 1 | R8 | RES, 0603 30.1k Ω 1% 1/10W | VISHAY CRCW060330K1FKEA |
| 26 | 1 | R13 | RES, 0603 60.4k Ω 1% 1/10W | VISHAY CRCW060360K4FKEA |
| 27 | 2 | R11, R44 | RES, 0603 100k Ω 1% 1/10W | VISHAY CRCW0603100KFKEA |
| 28 | 1 | U1 | IC, LTC3876EUHF | LINEAR TECHNOLOGY LTC3876EUHF |
| 29 | 2 | L1, L2 | IND, 0.47 μ H | WE 7443330047 |
| Additional Demo Board Circuit Components | | | | |
| 1 | 1 | CIN1, CIN2 | CAP, 180 μ F 20% 16V OSCON | SANYO 16SVP180M |
| 2 | 8 | C22 TO C29 | CAP, 1206 1 μ F 10% 16V X5R | AVX 1206YD105KAT |
| 3 | 4 | R46, R47, R49, R50 | RES, 1206 0.005 Ω 1% 1/4W | VISHAY WSL12065L000FEA |
| 4 | 2 | R48, R51 | RES, 0603 10k Ω 1% 1/10W | VISHAY CRCW060310K0FKEA |
| 5 | 2 | Q9, Q10 | N-Channel 30-V MOSFET, TO-252 | VISHAY, SUD50N03-09P-E3 |
| 6 | 24 | E1 TO E9, E11 TO E19, E21 TO E26 | TESTPOINT, TURRET, 0.094" PBF | MILL-MAX, 2501-2-00-80-00-00-07-0 |
| Hardware/Components (For Demo Board Only) | | | | |
| 1 | 1 | JP3 | HEADER, 4PIN | SAMTEC, TMM104-02-L-S |
| 2 | 3 | JP1, JP2, JP4 | HEADER, 3PIN, 2mm | SAMTEC, TMM103-02-L-S |
| 3 | 4 | XJP1, XJP2, XJP3, XJP4 | SHUNT, 2mm | SAMTEC, 2SN-BK-G |
| 4 | 4 | MTG 4 CORNERS | STAND-OFF, NYLON (SNAP ON), 0.25" TALL | KEYSTONE, 8831 |
| 5 | 6 | J1, J2, J3, J4, J5, J6 | JACK, BANANA | KEYSTONE 575-4 |
| 6 | 2 | J7, J8 | CONN., VERT. PC-MNT BNC 50 Ω | CONNEX 112404 |

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