100-Pin TQFP & 165-Bump BGA
Commercial Temp

9Mb Pipelined and Flow Through Synchronous NBT SRAM

250 MHz–150 MHz
1.8 V or 2.5 V V_{DD}
1.8 V or 2.5 V I/O

Features

- User-configurable Pipeline and Flow Through mode
- NBT (No Bus Turn Around) functionality allows zero wait read-write-read bus utilization
- Fully pin-compatible with both pipelined and flow through NtRAM™, NoBL™ and ZBT™ SRAMs
- IEEE 1149.1 JTAG-compatible Boundary Scan
- 1.8 V or 2.5 V core power supply
- 1.8 V or 2.5 V I/O supply
- $\overline{\text{LBO}}$ pin for Linear or Interleave Burst mode
- Pin-compatible with 2M, 4M, and 18M devices
- Byte write operation (9-bit Bytes)
- 3 chip enable signals for easy depth expansion
- ZZ pin for automatic power-down
- JEDEC-standard packages
- RoHS-compliant 100-lead TQFP and 165-bump BGA packages available

Functional Description

The GS881Z18/32/36C(T/D)-xxxV is a 9Mbit Synchronous Static SRAM. GSI's NBT SRAMs, like ZBT, NtRAM, NoBL or other pipelined read/double late write or flow through read/single late write SRAMs, allow utilization of all available bus bandwidth by eliminating the need to insert deselect cycles when the device is switched from read to write cycles.

Because it is a synchronous device, address, data inputs, and read/ write control inputs are captured on the rising edge of the input clock. Burst order control ($\overline{\text{LBO}}$) must be tied to a power rail for proper operation. Asynchronous inputs include the Sleep mode enable, ZZ and Output Enable. Output Enable can be used to override the synchronous control of the output drivers and turn the RAM's output drivers off at any time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation required by asynchronous SRAMs and simplifies input signal timing.

The GS881Z18/32/36C(T/D)-xxxV may be configured by the user to operate in Pipeline or Flow Through mode. Operating as a pipelined synchronous device, in addition to the rising-edge-triggered registers that capture input signals, the device incorporates a rising-edge-triggered output register. For read cycles, pipelined SRAM output data is temporarily stored by the edge triggered output register during the access cycle and then released to the output drivers at the next rising edge of clock.

The GS881Z18/32/36C(T/D)-xxxV is implemented with GSI's high performance CMOS technology and is available in JEDEC-standard 100-pin TQFP and 165-bump BGA packages.

Parameter Synopsis

		-250	-200	-150	Unit
Pipeline 3-1-1-1	t_{KQ}	3.0	3.0	3.8	ns
	tCycle	4.0	5.0	6.7	ns
	Curr (x18)	175	150	125	mA
	Curr (x32/x36)	200	165	145	mA
Flow Through 2-1-1-1	t_{KQ}	5.5	6.5	7.5	ns
	tCycle	5.5	6.5	7.5	ns
	Curr (x18)	135	125	113	mA
	Curr (x32/x36)	155	140	125	mA

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GS881Z18C881Z32CT-xxxV 100-Pin TQFP Pinout (Package T)

Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

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GS881Z32CT-xxxV 100-Pin TQFP Pinout (Package T)

Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

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GS881Z36CT-xxxV 100-Pin TQFP Pinout (Package T)

Note:
Pins marked with NC can be tied to either V_{DD} or V_{SS}. These pins can also be left floating.

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100-Pin TQFP Pin Descriptions

Symbol	Type	Description
A_0, A_1	In	Burst Address Inputs; Preload the burst counter
A	In	Address Inputs
CK	In	Clock Input Signal
$\overline{B}_A$	In	Byte Write signal for data inputs DQ_A; active low
$\overline{B}_B$	In	Byte Write signal for data inputs DQ_B; active low
$\overline{B}_C$	In	Byte Write signal for data inputs DQ_C; active low
$\overline{B}_D$	In	Byte Write signal for data inputs DQ_D; active low
$\overline{W}$	In	Write Enable; active low
$\overline{E}_1$	In	Chip Enable; active low
E_2	In	Chip Enable—Active High. For self decoded depth expansion
$\overline{E}_3$	In	Chip Enable—Active Low. For self decoded depth expansion
$\overline{G}$	In	Output Enable; active low
ADV	In	Advance/$\overline{Load}$; Burst address counter control pin
$\overline{CKE}$	In	Clock Input Buffer Enable; active low
NC	—	No Connect
DQ_A	I/O	Byte A Data Input and Output pins
DQ_B	I/O	Byte B Data Input and Output pins
DQ_C	I/O	Byte C Data Input and Output pins
DQ_D	I/O	Byte D Data Input and Output pins
DQP_A	I/O	9th Data I/O Pin; Byte A
DQP_B	I/O	9th Data I/O Pin; Byte B
DQP_C	I/O	9th Data I/O Pin; Byte C
DQP_D	I/O	9th Data I/O Pin; Byte D
ZZ	In	Power down control; active high
$\overline{FT}$	In	Pipeline/Flow Through Mode Control; active low
$\overline{LBO}$	In	Linear Burst Order; active low.
TMS		Scan Test Mode Select
TDI		Scan Test Data In
TDO		Scan Test Data Out
TCK		Scan Test Clock
V_{DD}	In	Core power supply
V_{SS}	In	Ground
V_{DDQ}	In	Output driver power supply

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165 Bump BGA—x18 Commom I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BB}$	NC	$\overline{E3}$	$\overline{CKE}$	ADV	A17	A	A	A
B	NC	A	E2	NC	$\overline{BA}$	CK	$\overline{W}$	$\overline{G}$	NC	A	NC	B
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ_A	C
D	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A	D
E	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A	E
F	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A	F
G	NC	DQ_B	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_A	G
H	$\overline{FT}$	MCH	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ	H
J	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC	J
K	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC	K
L	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC	L
M	DQ_B	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	NC	M
N	DQ_B	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC	P
R	$\overline{LBO}$	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13 mm x 15 mm Body—1.0 mm Bump Pitch

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165 Bump BGA—x32 Common I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BC}$	$\overline{BB}$	$\overline{E3}$	$\overline{CKE}$	ADV	A17	A	NC	A
B	NC	A	E2	$\overline{BD}$	$\overline{BA}$	CK	$\overline{W}$	$\overline{G}$	NC	A	NC	B
C	NC	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	C
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B	D
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B	E
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B	F
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B	G
H	$\overline{FT}$	MCH	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ	H
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A	J
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A	K
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A	L
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A	M
N	NC	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	NC	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC	P
R	$\overline{LBO}$	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13 mm x 15 mm Body—1.0 mm Bump Pitch

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165 Bump BGA—x36 Common I/O—Top View (Package D)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	A	$\overline{E1}$	$\overline{BC}$	$\overline{BB}$	$\overline{E3}$	$\overline{CKE}$	ADV	A	A	NC	A
B	NC	A	E2	$\overline{BD}$	$\overline{BA}$	CK	$\overline{W}$	$\overline{G}$	NC	A	NC	B
C	DQP_C	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQP_B	C
D	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B	D
E	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B	E
F	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B	F
G	DQ_C	DQ_C	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_B	DQ_B	G
H	$\overline{FT}$	MCH	NC	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	NC	NC	ZZ	H
J	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A	J
K	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A	K
L	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A	L
M	DQ_D	DQ_D	V_{DDQ}	V_{DD}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DDQ}	DQ_A	DQ_A	M
N	DQP_D	NC	V_{DDQ}	V_{SS}	NC	NC	NC	V_{SS}	V_{DDQ}	NC	DQP_A	N
P	NC	NC	A	A	TDI	A1	TDO	A	A	A	NC	P
R	$\overline{LBO}$	NC	A	A	TMS	A0	TCK	A	A	A	A	R

11 x 15 Bump BGA—13 mm x 15 mm Body—1.0 mm Bump Pitch

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GS881Z18/32/36D 165-Bump BGA Pin Description

Symbol	Type	Description
A_0, A_1	I	Address field LSBs and Address Counter Preset Inputs
A	I	Address Inputs
$\overline{B}_A$	In	Byte Write signal for data inputs DQ_A; active low
$\overline{B}_B$	In	Byte Write signal for data inputs DQ_B; active low
$\overline{B}_C$	In	Byte Write signal for data inputs DQ_C; active low
$\overline{B}_D$	In	Byte Write signal for data inputs DQ_D; active low
NC	—	No Connect
CK	I	Clock Input Signal; active high
$\overline{CKE}$	I	Clock Enable; active low
$\overline{W}$	I	Write Enable; active low
$\overline{E}_1$	I	Chip Enable; active low
$\overline{E}_3$	I	Chip Enable; active low
E_2	I	Chip Enable; active high
$\overline{G}$	I	Output Enable; active low
DQ_A	I/O	Byte A Data Input and Output pins
DQ_B	I/O	Byte B Data Input and Output pins
DQ_C	I/O	Byte C Data Input and Output pins
DQ_D	I/O	Byte D Data Input and Output pins
DQP_A	I/O	9th Data I/O Pin; Byte A
DQP_B	I/O	9th Data I/O Pin; Byte B
DQP_C	I/O	9th Data I/O Pin; Byte C
DQP_D	I/O	9th Data I/O Pin; Byte D
ADV	I	Burst address counter advance enable; active high
ZZ	I	Sleep mode control; active high
$\overline{FT}$	I	Flow Through or Pipeline mode; active low
$\overline{LBO}$	I	Linear Burst Order mode; active low
TMS	I	Scan Test Mode Select
TDI	I	Scan Test Data In
TDO	O	Scan Test Data Out
TCK	I	Scan Test Clock
MCH	—	Must Connect High
DNU	—	Do Not Use
V_{DD}	I	Core power supply
V_{SS}	I	I/O and Core Ground
V_{DDQ}	I	Output driver power supply

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GS881Z18/32/36C881Z18/32/36C881Z18C(T/D)-xxxV NBT SRAM Functional Block Diagram

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Functional Details

Clocking

Deassertion of the Clock Enable ($\overline{CKE}$) input blocks the Clock input from reaching the RAM's internal circuits. It may be used to suspend RAM operations. Failure to observe Clock Enable set-up or hold requirements will result in erratic operation.

Pipeline Mode Read and Write Operations

All inputs (with the exception of Output Enable, Linear Burst Order and Sleep) are synchronized to rising clock edges. Single cycle read and write operations must be initiated with the Advance/$\overline{Load}$ pin (ADV) held low, in order to load the new address. Device activation is accomplished by asserting all three of the Chip Enable inputs ($\overline{E}_1$, E_2 and $\overline{E}_3$). Deassertion of any one of the Enable inputs will deactivate the device.

Function	$\overline{W}$	$\overline{B}_A$	$\overline{B}_B$	$\overline{B}_C$	$\overline{B}_D$
Read	H	X	X	X	X
Write Byte “a”	L	L	H	H	H
Write Byte “b”	L	H	L	H	H
Write Byte “c”	L	H	H	L	H
Write Byte “d”	L	H	H	H	L
Write all Bytes	L	L	L	L	L
Write Abort/NOP	L	H	H	H	H

Read operation is initiated when the following conditions are satisfied at the rising edge of clock: $\overline{CKE}$ is asserted low, all three chip enables ($\overline{E}_1$, E_2, and $\overline{E}_3$) are active, the write enable input signals $\overline{W}$ is deasserted high, and ADV is asserted low. The address presented to the address inputs is latched in to address register and presented to the memory core and control logic. The control logic determines that a read access is in progress and allows the requested data to propagate to the input of the output register. At the next rising edge of clock the read data is allowed to propagate through the output register and onto the output pins.

Write operation occurs when the RAM is selected, CKE is active and the write input is sampled low at the rising edge of clock. The Byte Write Enable inputs ($\overline{B}_A$, $\overline{B}_B$, $\overline{B}_C$ & $\overline{B}_D$) determine which bytes will be written. All or none may be activated. A write cycle with no Byte Write inputs active is a no-op cycle. The pipelined NBT SRAM provides double late write functionality, matching the write command versus data pipeline length (2 cycles) to the read command versus data pipeline length (2 cycles). At the first rising edge of clock, Enable, Write, Byte Write(s), and Address are registered. The Data In associated with that address is required at the third rising edge of clock.

Flow Through Mode Read and Write Operations

Operation of the RAM in Flow Through mode is very similar to operations in Pipeline mode. Activation of a read cycle and the use of the Burst Address Counter is identical. In Flow Through mode the device may begin driving out new data immediately after new address are clocked into the RAM, rather than holding new data until the following (second) clock edge. Therefore, in Flow Through mode the read pipeline is one cycle shorter than in Pipeline mode.

Write operations are initiated in the same way, but differ in that the write pipeline is one cycle shorter as well, preserving the ability to turn the bus from reads to writes without inserting any dead cycles. While the pipelined NBT RAMs implement a double late write protocol, in Flow Through mode a single late write protocol mode is observed. Therefore, in Flow Through mode, address and control are registered on the first rising edge of clock and data in is required at the data input pins at the second rising edge of clock.

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Synchronous Truth Table

Operation	Type	Address	CK	$\overline{CKE}$	ADV	$\overline{W}$	$\overline{Bx}$	$\overline{E}1$	E2	$\overline{E}3$	$\overline{G}$	ZZ	DQ	Notes
Read Cycle, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	L	L	Q	
Read Cycle, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	L	L	Q	1,10
NOP/Read, Begin Burst	R	External	L-H	L	L	H	X	L	H	L	H	L	High-Z	2
Dummy Read, Continue Burst	B	Next	L-H	L	H	X	X	X	X	X	H	L	High-Z	1,2,10
Write Cycle, Begin Burst	W	External	L-H	L	L	L	L	L	H	L	X	L	D	3
Write Abort, Begin Burst	D	None	L-H	L	L	L	H	L	H	L	X	L	High-Z	1
Write Cycle, Continue Burst	B	Next	L-H	L	H	X	L	X	X	X	X	L	D	1,3,10
Write Abort, Continue Burst	B	Next	L-H	L	H	X	H	X	X	X	X	L	High-Z	1,2,3,10
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	H	X	X	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	X	H	X	L	High-Z	
Deselect Cycle, Power Down	D	None	L-H	L	L	X	X	X	L	X	X	L	High-Z	
Deselect Cycle, Continue	D	None	L-H	L	H	X	X	X	X	X	X	L	High-Z	1
Sleep Mode		None	X	X	X	X	X	X	X	X	X	H	High-Z	
Clock Edge Ignore, Stall		Current	L-H	H	X	X	X	X	X	X	X	L	-	4

Notes:

1. Continue Burst cycles, whether read or write, use the same control inputs. A Deselect continue cycle can only be entered into if a Deselect cycle is executed first.
2. Dummy Read and Write abort can be considered NOPs because the SRAM performs no operation. A Write abort occurs when the $\overline{W}$ pin is sampled low but no Byte Write pins are active so no write operation is performed.
3. $\overline{G}$ can be wired low to minimize the number of control signals provided to the SRAM. Output drivers will automatically turn off during write cycles.
4. If $\overline{CKE}$ High occurs during a pipelined read cycle, the DQ bus will remain active (Low Z). If $\overline{CKE}$ High occurs during a write cycle, the bus will remain in High Z.
5. X = Don't Care; H = Logic High; L = Logic Low; $\overline{Bx}$ = High = All Byte Write signals are high; $\overline{Bx}$ = Low = One or more Byte/Write signals are Low
6. All inputs, except $\overline{G}$ and ZZ must meet setup and hold times of rising clock edge.
7. Wait states can be inserted by setting $\overline{CKE}$ high.
8. This device contains circuitry that ensures all outputs are in High Z during power-up.
9. A 2-bit burst counter is incorporated.
10. The address counter is incriminated for all Burst continue cycles.

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Pipelined and Flow Through Read Write Control State Diagram

Key

Notes:

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.

2. W, R, B, and D represent input command codes as indicated in the Synchronous Truth Table.

Current State and Next State Definition for Pipelined and Flow Through Read/Write Control State Diagram

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Pipeline Mode Data I/O State Diagram

Key

Notes:

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.
2. W, R, B, and D represent input command codes as indicated in the Truth Tables.

Current State and Next State Definition for Pipeline Mode Data I/O State Diagram

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Flow Through Mode Data I/O State Diagram

Key

Notes:

1. The Hold command ($\overline{CKE}$ Low) is not shown because it prevents any state change.

2. W, R, B, and D represent input command codes as indicated in the Truth Tables.

Current State and Next State Definition for: Pipeline and Flow through Read Write Control State Diagram

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Burst Cycles

Although NBT RAMs are designed to sustain 100% bus bandwidth by eliminating turnaround cycle when there is transition from read to write, multiple back-to-back reads or writes may also be performed. NBT SRAMs provide an on-chip burst address generator that can be utilized, if desired, to further simplify burst read or write implementations. The ADV control pin, when driven high, commands the SRAM to advance the internal address counter and use the counter generated address to read or write the SRAM. The starting address for the first cycle in a burst cycle series is loaded into the SRAM by driving the ADV pin low, into Load mode.

Burst Order

The burst address counter wraps around to its initial state after four addresses (the loaded address and three more) have been accessed. The burst sequence is determined by the state of the Linear Burst Order pin ($\overline{LBO}$). When this pin is low, a linear burst sequence is selected. When the RAM is installed with the LBO pin tied high, Interleaved burst sequence is selected. See the tables below for details.

Mode Pin Functions

Mode Name	Pin Name	State	Function
Burst Order Control	$\overline{LBO}$	L	Linear Burst
		H	Interleaved Burst
Output Register Control	$\overline{FT}$	L	Flow Through
		H or NC	Pipeline
Power Down Control	ZZ	L or NC	Active
		H	Standby, $I_{DD} = I_{SB}$

Note:
There is a pull-up device on the $\overline{FT}$ pin and a pull-down device on the ZZ pin , so this input pin can be unconnected and the chip will operate in the default states as specified in the above tables.

Burst Counter Sequences

Linear Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	10	11	00
3rd address	10	11	00	01
4th address	11	00	01	10

Note:
The burst counter wraps to initial state on the 5th clock.

Interleaved Burst Sequence

	A[1:0]	A[1:0]	A[1:0]	A[1:0]
1st address	00	01	10	11
2nd address	01	00	11	10
3rd address	10	11	00	01
4th address	11	10	01	00

Note:
The burst counter wraps to initial state on the 5th clock.

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Sleep Mode

During normal operation, ZZ must be pulled low, either by the user or by it's internal pull down resistor. When ZZ is pulled high, the SRAM will enter a Power Sleep mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM operates normally after ZZ recovery time.

Sleep mode is a low current, power-down mode in which the device is deselected and current is reduced to $I_{SB}2$. The duration of Sleep mode is dictated by the length of time the ZZ is in a high state. After entering Sleep mode, all inputs except ZZ become disabled and all outputs go to High-Z The ZZ pin is an asynchronous, active high input that causes the device to enter Sleep mode. When the ZZ pin is driven high, $I_{SB}2$ is guaranteed after the time tZZI is met. Because ZZ is an asynchronous input, pending operations or operations in progress may not be properly completed if ZZ is asserted. Therefore, Sleep mode must not be initiated until valid pending operations are completed. Similarly, when exiting Sleep mode during tZZR, only a Deselect or Read commands may be applied while the SRAM is recovering from Sleep mode.

Sleep Mode Timing Diagram

Designing for Compatibility

The GSI NBT SRAMs offer users a configurable selection between Flow Through mode and Pipelinemode via the $\overline{FT}$ signal found on Pin 14. Not all vendors offer this option, however most mark Pin 14 as V_{DD} or V_{DDQ} on pipelined parts and V_{SS} on flow through parts. GSI NBT SRAMs are fully compatible with these sockets.

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Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 4.6	V
V_{DDQ}	Voltage on V_{DDQ} Pins	–0.5 to V_{DD}	V
$V_{I/O1}$	Voltage on I/O Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
$V_{I/O2}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 4.6 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DD} +0.5 (≤ 4.6 V max.)	V
I_{IN}	Input Current on Any Pin	+/–20	mA
I_{OUT}	Output Current on Any I/O Pin	+/–20	mA
P_D	Package Power Dissipation	1.5	W
T_{STG}	Storage Temperature	–55 to 125	^oC
T_{BIAS}	Temperature Under Bias	–55 to 125	^oC

Notes:

1. Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Absolute Maximum Ratings, for an extended period of time, may affect reliability of this component.
2. Both $V_{I/O1}$ and $V_{I/O2}$ must be met.

Power Supply Voltage Ranges (1.8 V/2.5 V Version)

Parameter	Symbol	Min.	Typ.	Max.	Unit
1.8 V Supply Voltage	V_{DD1}	1.7	1.8	2.0	V
2.5 V Supply Voltage	V_{DD2}	2.3	2.5	2.7	V
1.8 V V_{DDQ} I/O Supply Voltage	V_{DDQ1}	1.7	1.8	V_{DD}	V
2.5 V V_{DDQ} I/O Supply Voltage	V_{DDQ2}	2.3	2.5	V_{DD}	V

Note:

V_{DDQ} must be less than or equal to V_{DD} + 0.3 V at all times.

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V_{DDQ2} & V_{DDQ1} Range Logic Levels

Parameter	Symbol	Min.	Typ.	Max.	Unit
V_{DD} Input High Voltage	V_{IH}	$0.6*V_{DD}$	—	V_{DD} + 0.3	V
V_{DD} Input High Voltage	$V_{IH(I/O)1}$	$0.6*V_{DD}$	—	V_{DD} + 0.3	V
V_{DD} Input High Voltage	$V_{IH(I/O)2}$	$0.6*V_{DD}$	—	V_{DDQ} + 0.3	V
V_{DD} Input Low Voltage	V_{IL}	–0.3	—	$0.3*V_{DD}$	V

Notes:
1. V_{IH} (max) must be met for any instantaneous value of V_{DD}.
2. $V_{IH(I/O)1}$ (max) must be met for any instantaneous value of V_{DD}.
3. $V_{IH(I/O)2}$ (max) must be met for any instantaneous value of V_{DDQ}.
4. V_{DD} needs to power-up before or at the same time as V_{DDQ} to make sure V_{IH} (max) is not exceeded.

Recommended Operating Temperatures

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient Temperature (Commercial Range Versions)	T_A	0	25	70	°C

Note:
Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
100 TQFP	4-layer	38.7	33.5	31.9	27.6	10.6

Notes:
1. Thermal Impedance data is based on a number of of samples from mulitple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

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Undershoot Measurement and Timing

Overshoot Measurement and Timing

Note:
Input Under/overshoot voltage must be –2 V > Vi < V_{DDn}+2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tKC.

Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 2.5 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	8	10	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0 V	12	14	pF

Note:
These parameters are sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	V_{DD}/2
Output reference level	V_{DDQ}/2
Output load	Fig. 1

Notes:
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
3. Device is deselected as defined by the Truth Table.

Figure 1

Output Load 1

* Distributed Test Jig Capacitance

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DC Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–1 uA	1 uA
$\overline{FT}$ Input Current	I_{IN}	$V_{DD} \geq V_{IN} \geq 0$ V	–100 uA	100 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DD}	–1 uA	1 uA
1.8 V Output High Voltage	V_{OH1}	I_{OH} = –4 mA, V_{DDQ} = 1.7 V	V_{DDQ} – 0.4 V	—
2.5 V Output High Voltage	V_{OH2}	I_{OH} = –8 mA, V_{DDQ} = 2.375 V	1.7 V	—
1.8 V Output Low Voltage	V_{OL1}	I_{OL} = 4 mA	—	0.4 V
2.5 V Output Low Voltage	V_{OL2}	I_{OL} = 8 mA	—	0.4 V

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Operating Currents

Parameter	Test Conditions	Mode		Symbol	-250	-200	-150	Unit
					0 to 70°C	0 to 70°C	0 to 70°C	
Operating Current	Device Selected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Output open	(x32/x36)	Pipeline	I_{DD} I_{DDQ}	180 20	150 15	125 20	mA
			Flow Through	I_{DD} I_{DDQ}	140 15	125 15	110 15	mA
		(x18)	Pipeline	I_{DD} I_{DDQ}	165 10	140 10	115 10	mA
			Flow Through	I_{DD} I_{DDQ}	125 10	115 10	105 8	mA
Standby Current	$ZZ \geq V_{DD} - 0.2$ V	—	Pipeline	I_{SB}	25	25	25	mA
			Flow Through	I_{SB}	25	25	25	mA
Deselect Current	Device Deselected; All other inputs $\geq V_{IH}$ or $\leq V_{IL}$	—	Pipeline	I_{DD}	45	45	40	mA
			Flow Through	I_{DD}	40	40	40	mA

Notes:

1. I_{DD} and I_{DDQ} apply to any combination of V_{DD1}, V_{DD2}, V_{DDQ1}, and V_{DDQ2} operation.
2. All parameters listed are worst case scenario.

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AC Electrical Characteristics

	Parameter	Symbol	-250		-200		-150		Unit
			Min	Max	Min	Max	Min	Max	
Pipeline	Clock Cycle Time	tKC	4.0	—	5.0	—	6.7	—	ns
	Clock to Output Valid	tKQ	—	3.0	—	3.0	—	3.8	ns
	Clock to Output Invalid	tKQX	1.5	—	1.5	—	1.5	—	ns
	Clock to Output in Low-Z	tLZ[1]	1.5	—	1.5	—	1.5	—	ns
	Setup time	tS	1.2	—	1.4	—	1.5	—	ns
	Hold time	tH	0.2	—	0.4	—	0.5	—	ns
Flow Through	Clock Cycle Time	tKC	5.5	—	6.5	—	7.5	—	ns
	Clock to Output Valid	tKQ	—	5.5	—	6.5	—	7.5	ns
	Clock to Output Invalid	tKQX	2.0	—	2.0	—	2.0	—	ns
	Clock to Output in Low-Z	tLZ[1]	2.0	—	2.0	—	2.0	—	ns
	Setup time	tS	1.5	—	1.5	—	1.5	—	ns
	Hold time	tH	0.5	—	0.5	—	0.5	—	ns
	Clock HIGH Time	tKH	1.3	—	1.3	—	1.5	—	ns
	Clock LOW Time	tKL	1.7	—	1.7	—	1.7	—	ns
	Clock to Output in High-Z	tHZ[1]	1.5	2.5	1.5	3.0	1.5	3.0	ns
	$\overline{G}$ to Output Valid	tOE	—	2.5	—	3.0	—	3.8	ns
	$\overline{G}$ to output in Low-Z	tOLZ[1]	0	—	0	—	0	—	ns
	$\overline{G}$ to output in High-Z	tOHZ[1]	—	2.5	—	3.0	—	3.0	ns
	ZZ setup time	tZZS[2]	5	—	5	—	5	—	ns
	ZZ hold time	tZZH[2]	1	—	1	—	1	—	ns
	ZZ recovery	tZZR	20	—	20	—	20	—	ns

Notes:

1. These parameters are sampled and are not 100% tested.
2. ZZ is an asynchronous signal. However, in order to be recognized on any given clock cycle, ZZ must meet the specified setup and hold times as specified above.

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Pipeline Mode Timing (NBT)

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Flow Through Mode Timing (NBT)

*Note: $\overline{E}$ = High(False) if $\overline{E1}$ = 1 or E2 = 0 or $\overline{E3}$ = 1

JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DDQ}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

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JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as Test Access Port orTAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

Bypass Register

The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

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JTAG TAP Block Diagram

* For the value of M, see the BSDL file, which is available at by contacting us at apps@gsitechnology.com.

Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Not Used																				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	0	0	1	1

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Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram

Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is

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loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

RFU

These instructions are Reserved for Future Use. In this device they replicate the BYPASS instruction.

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JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
RFU	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
SAMPLE/ PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
RFU	110	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

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JTAG Port Recommended Operating Conditions and DC Characteristics (1.8/2.5 V Version)

Parameter	Symbol	Min.	Max.	Unit	Notes
1.8 V Test Port Input Low Voltage	V_{ILJ1}	–0.3	0.3 * V_{DD1}	V	1
2.5 V Test Port Input Low Voltage	V_{ILJ2}	–0.3	0.3 * V_{DD2}	V	1
1.8 V Test Port Input High Voltage	V_{IHJ1}	0.6 * V_{DD1}	V_{DD1} +0.3	V	1
2.5 V Test Port Input High Voltage	V_{IHJ2}	0.6 * V_{DD2}	V_{DD2} +0.3	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	1.7	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.4	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DDQ} – 100 mV	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	100 mV	V	5, 9

Notes:
1. Input Under/overshoot voltage must be –2 V < Vi < V_{DDn} +2 V not to exceed 4.6 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
3. $0\ V \leq V_{IN} \leq V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DDQ} supply.
6. I_{OHJ} = –4 mA
7. I_{OLJ} = + 4 mA
8. I_{OHJC} = –100 uA
9. I_{OLJC} = +100 uA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	V_{DDQ}/2
Output reference level	V_{DDQ}/2

JTAG Port AC Test Load

* Distributed Test Jig Capacitance

Notes:
1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

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JTAG Port Timing Diagram

JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

Boundary Scan (BSDL Files)

For information regarding the Boundary Scan Chain, or to obtain BSDL files for this part, please contact our Applications Engineering Department at: apps@gsitechnology.com.

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TQFP Package Drawing (Package T)

Symbol	Description	Min.	Nom.	Max
A1	Standoff	0.05	0.10	0.15
A2	Body Thickness	1.35	1.40	1.45
b	Lead Width	0.20	0.30	0.40
c	Lead Thickness	0.09	—	0.20
D	Terminal Dimension	21.9	22.0	22.1
D1	Package Body	19.9	20.0	20.1
E	Terminal Dimension	15.9	16.0	16.1
E1	Package Body	13.9	14.0	14.1
e	Lead Pitch	—	0.65	—
L	Foot Length	0.45	0.60	0.75
L1	Lead Length	—	1.00	—
Y	Coplanarity			0.10
θ	Lead Angle	0°	—	7°

Notes:
1. All dimensions are in millimeters (mm).
2. Package width and length do not include mold protrusion.

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Package Dimensions—165-Bump FPBGA (Package D)

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Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number[1]	Type	Voltage Option	Package	Speed[2] (MHz/ns)	T_A[3]
512K x 18	GS881Z18CT-250V	NBT	1.8 V or 2.5 V	TQFP	250/5.5	C
512K x 18	GS881Z18CT-200V	NBT	1.8 V or 2.5 V	TQFP	200/6.5	C
512K x 18	GS881Z18CT-150V	NBT	1.8 V or 2.5 V	TQFP	150/7.5	C
256K x 32	GS881Z32CT-250V	NBT	1.8 V or 2.5 V	TQFP	250/5.5	C
256K x 32	GS881Z32CT-200V	NBT	1.8 V or 2.5 V	TQFP	200/6.5	C
256K x 32	GS881Z32CT-150V	NBT	1.8 V or 2.5 V	TQFP	150/7.5	C
256K x 36	GS881Z36CT-250V	NBT	1.8 V or 2.5 V	TQFP	250/5.5	C
256K x 36	GS881Z36CT-200V	NBT	1.8 V or 2.5 V	TQFP	200/6.5	C
256K x 36	GS881Z36CT-150V	NBT	1.8 V or 2.5 V	TQFP	150/7.5	C
512K x 18	GS881Z18CGT-250V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	250/5.5	C
512K x 18	GS881Z18CGT-200V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	200/6.5	C
512K x 18	GS881Z18CGT-150V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	150/7.5	C
256K x 32	GS881Z32CGT-250V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	250/5.5	C
256K x 32	GS881Z32CGT-200V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	200/6.5	C
256K x 32	GS881Z32CGT-150V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	150/7.5	C
256K x 36	GS881Z36CGT-250V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	250/5.5	C
256K x 36	GS881Z36CGT-200V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	200/6.5	C
256K x 36	GS881Z36CGT-150V	NBT	1.8 V or 2.5 V	RoHS-compliant TQFP	150/7.5	C
512K x 18	GS881Z18CD-250V	NBT	1.8 V or 2.5 V	165 BGA	250/5.5	C
512K x 18	GS881Z18CD-200V	NBT	1.8 V or 2.5 V	165 BGA	200/6.5	C
512K x 18	GS881Z18CD-150V	NBT	1.8 V or 2.5 V	165 BGA	150/7.5	C
256K x 32	GS881Z32CD-250V	NBT	1.8 V or 2.5 V	165 BGA	250/5.5	C
256K x 32	GS881Z32CD-200V	NBT	1.8 V or 2.5 V	165 BGA	200/6.5	C
256K x 32	GS881Z32CD-150V	NBT	1.8 V or 2.5 V	165 BGA	150/7.5	C
256K x 36	GS881Z36CD-250V	NBT	1.8 V or 2.5 V	165 BGA	250/5.5	C
256K x 36	GS881Z36CD-200V	NBT	1.8 V or 2.5 V	165 BGA	200/6.5	C
256K x 36	GS881Z36CD-150V	NBT	1.8 V or 2.5 V	165 BGA	150/7.5	C

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS881Z36CT-150VT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user .
3. T_A = C = Commercial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings

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Ordering Information—GSI NBT Synchronous SRAM

Org	Part Number[1]	Type	Voltage Option	Package	Speed[2] (MHz/ns)	T_A[3]
512K x 18	GS881Z18CD-250IV	NBT	1.8 V or 2.5 V	165 BGA	250/5.5	I
512K x 18	GS881Z18CGD-250V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	250/5.5	C
512K x 18	GS881Z18CGD-200V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	200/6.5	C
512K x 18	GS881Z18CGD-150V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	150/7.5	C
256K x 32	GS881Z32CGD-250V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	250/5.5	C
256K x 32	GS881Z32CGD-200V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	200/6.5	C
256K x 32	GS881Z32CGD-150V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	150/7.5	C
256K x 36	GS881Z36CGD-250V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	250/5.5	C
256K x 36	GS881Z36CGD-200V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	200/6.5	C
256K x 36	GS881Z36CGD-150V	NBT	1.8 V or 2.5 V	RoHS-compliant 165 BGA	150/7.5	C

Notes:

1. Customers requiring delivery in Tape and Reel should add the character “T” to the end of the part number. Example: GS881Z36CT-150VT.
2. The speed column indicates the cycle frequency (MHz) of the device in Pipeline mode and the latency (ns) in Flow Through mode. Each device is Pipeline/Flow through mode-selectable by the user .
3. T_A = C = Commercial Temperature Range.
4. GSI offers other versions this type of device in many different configurations and with a variety of different features, only some of which are covered in this data sheet. See the GSI Technology web site (www.gsitechnology.com) for a complete listing of current offerings

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9Mb Sync SRAM Datasheet Revision History

File Name	Types of Changes Format or Content	Revision
881ZxxB_V_r1		• Creation of new datasheet
881ZxxB_V_r1; 881ZxxB_V_r1_01	Content	• Removed parity references (pg. 1, 16, 17) • Added note to TQFP pinouts (pg. 2, 3, 4)
881ZxxB_V_r1_01; 881ZxxB_V_r1_02	Content	• Update to MP datasheet
881ZVxxC_r1_03	Content	• Updated Absolute Maximum Ratings • Deleted conditional text
881ZVxxC_r1_04	Content	• Updated Absolute Maximum Ratings • Added thermal information • Updated Ordering Information
881ZVxxC_r1_05_Com	Content	• Updated Absolute Maximum Ratings • Removed all Ind Temp references

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ООО «ЛайфЭлектроникс» “LifeElectronics” LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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