8-Channel, I²C, 12-Bit SAR ADC with Temperature Sensor

Data Sheet

AD7291

FEATURES

- 12-bit SAR ADC
  - 8 single-ended analog input channels
  - Analog input range: 0 V to 2.5 V
- 12-bit temperature-to-digital converter
  - Temperature sensor accuracy of ±1°C typical
- Channel sequencer operation
- Specified for V_{DD} of 2.8 V to 3.6 V
- Logic voltage V_{DRIVE} = 1.65 V to 3.6 V
- Internal 2.5 V reference
- I²C-compatible serial interface supports standard and fast speed modes
- Out of range indicator/alert function
- Autocycle mode
- Power-down current: 12 µA maximum
- Temperature range: −40°C to +125°C
- 20-lead LFCSP package

FUNCTIONAL BLOCK DIAGRAM

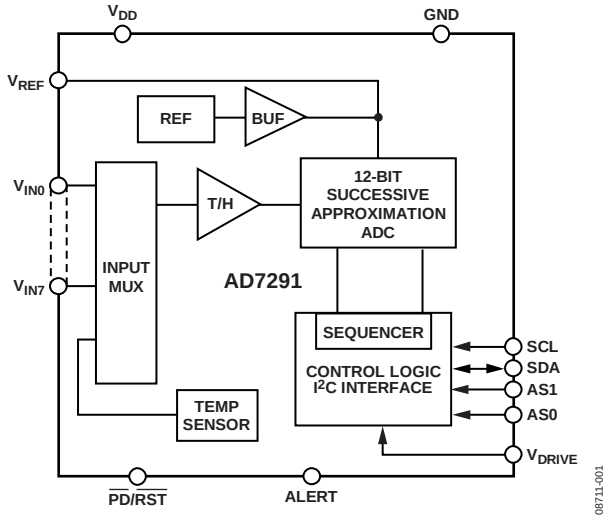

Figure 1.

GENERAL DESCRIPTION

The AD7291 is a 12-bit, low power, 8-channel, successive approximation analog-to-digital converter (ADC) with an internal temperature sensor.

The device operates from a single 3.3 V power supply and features an I²C-compatible interface. The device contains a 9-channel multiplexer and a track-and-hold amplifier than can handle frequencies up to 30 MHz. The device has an on-chip 2.5 V reference that can be disabled to allow the use of an external reference.

The AD7291 provides a 2-wire serial interface compatible with I²C interfaces. The I²C interface supports standard and fast I²C interface modes. The AD7291 normally remains in a partial power-down state while not converting and powers up for conversions. The conversion process can be controlled by a command mode where conversions occur across I²C write operations or an autocycle mode selected through software control.

The AD7291 includes a high accuracy band gap temperature sensor, which is monitored and digitized by the 12-bit ADC to give a resolution of 0.25°C.

The AD7291 offers a programmable sequencer, which enables the selection of a preprogrammable sequence of channels for conversion.

On-chip limit registers can be programmed with high and low limits for the conversion results; an out-of-range indicator output (ALERT) becomes active when the programmed high or low limits are violated by the conversion result. This output can be used as an interrupt.

PRODUCT HIGHLIGHTS

1. Ideally suited to monitoring system variables in a variety of systems including telecommunications, process control, and industrial control.
2. I²C-compatible serial interface, which supports standard and fast modes.
3. Automatic partial power-down while not converting to maximize power efficiency.
4. Channel sequencer operation.
5. Integrated temperature sensor with 0.25°C resolution.
6. Out of range indicator that can be software disabled or enabled.

Table 1. AD7291 and Related Products

Device	Resolution	Interface	Features
AD7291	12-bit	I²C	8-channel, I²C, 12-bit SAR ADC with temperature sensor
AD7298	12-bit	SPI	8-channel, 1 MSPS, 12-bit SAR ADC with temperature sensor

Rev. C
Document Feedback

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8/2011—Rev. 0 to Rev. A

Changes to Temperature Sensor—Internal, Accuracy Parameter, Table 2 ... 3

1/2011—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.8 V to 3.6 V; V_{DRIVE} = 1.65 V to 3.6 V; f_{SCL} = 400 kHz, fast SCLK mode; V_{REF} = 2.5 V internal/external; T_A = −40°C to +125°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
DYNAMIC PERFORMANCE					f_{IN} = 1 kHz sine wave
Signal-to-Noise Ratio (SNR)[2]	70	71		dB	
Signal-to-Noise (+ Distortion) Ratio (SINAD)[2]	70	71		dB	
Total Harmonic Distortion (THD)[2]		−84	−78	dB	
Spurious-Free Dynamic Range (SFDR)		−85	−80	dB	
Intermodulation Distortion (IMD)					f_A = 5.4 kHz, f_B = 4.6 kHz
Second-Order Terms		−88		dB	
Third-Order Terms		−88		dB	
Channel-to-Channel Isolation		−100		dB	f_{IN} = 10 kHz
Full Power Bandwidth[3]		30		MHz	At 3 dB
		10		MHz	At 0.1 dB
DC ACCURACY					
Resolution	12			Bits	
Integral Nonlinearity (INL)[2]		±0.5	±1	LSB	
Differential Nonlinearity (DNL)[2]		±0.5	±0.99	LSB	Guaranteed no missed codes to 12 bits
Offset Error[2]		±2	±4.5	LSB	
Offset Error Matching[2]		±2.5	±4.5	LSB	
Offset Temperature Drift		4		ppm/°C	
Gain Error[2]		±1	±4	LSB	
Gain Error Matching[2]		±1	±2.5	LSB	
Gain Temperature Drift		0.5		ppm/°C	
ANALOG INPUT					
Input Voltage Ranges	0		V_{REF}	V	
DC Leakage Current		±0.01	±1	µA	
Input Capacitance[3]		34		pF	When in track
		8		pF	When in hold
REFERENCE INPUT/OUTPUT					
Reference Output Voltage[4]	2.4925	2.5	2.5075	V	±0.3% maximum at 25°C
Long-Term Stability		150		ppm	For 1000 hours
Output Voltage Hysteresis		50		ppm	
Reference Input Voltage Range[5]	1		2.5	V	
DC Leakage Current		±0.01	±1	µA	External reference applied to Pin V_{REF}
V_{REF} Output Impedance		1		Ω	
Reference Temperature Coefficient		12	35	ppm/°C	
V_{REF} Noise[3]		60		µV rms	Bandwidth = 10 MHz
LOGIC INPUTS (SDA, SCL)					
Input High Voltage, V_{INH}	0.7 × V_{DRIVE}			V	
Input Low Voltage, V_{INL}			0.3 × V_{DRIVE}	V	
Input Current, I_{IN}		±0.01	±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]		6		pF	
Input Hysteresis, V_{HYST}	0.1 × V_{DRIVE}			V	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} − 0.3			V	V_{DRIVE} < 1.8
	V_{DRIVE} − 0.2			V	V_{DRIVE} ≥ 1.8
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA

Parameter	Min	Typ	Max	Unit[1]	Test Conditions/Comments
Floating State Leakage Current		±0.01	±1	µA	
Floating State Output Capacitance[3]		8		pF	
TEMPERATURE SENSOR—INTERNAL					
Operating Range	−40		+125	°C	
Accuracy		±1	±2	°C	T_A = −40°C to +85°C
		±1	±3	°C	T_A = 85°C to 125°C
Resolution		0.25		°C	LSB size
CONVERSION RATE					
Conversion Time		3.2		µs	
Autocycle Update Rate[6]		50		µs	
Throughput Rate			22.22	kSPS	f_{SCL} = 400 kHz
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{DD}	2.8	3	3.6	V	
V_{DRIVE}	1.65	3	3.6	V	
I_{TOTAL}[7, 8]					
Normal Mode (Operational)		2.9	3.5	mA	
Normal Mode (Static)		2.9	3.3	mA	
Full Power-Down Mode		0.3	1.6	µA	T_A = −40°C to +25°C
		1.6	4.5	µA	T_A = >25°C to 85°C
		4.9	12	µA	T_A = >85°C to 125°C
Power Dissipation[8]					
Normal Mode (Operational)		8.7	10.5	mW	V_{DD} = 3 V, V_{DRIVE} = 3 V
		10.4	12.6	mW	
Normal Mode (Static)		10.4	11.9	mW	
Full Power-Down Mode		1.1	5.8	µW	T_A = −40°C to +25°C
		5.8	16.2	µW	T_A = >25°C to 85°C
		17.6	43.2	µW	T_A = >85°C to 125°C

[1] All specifications expressed in decibels are referred to full-scale input, FSR, and tested with an input signal at 0.5 dB below full scale, unless otherwise specified.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] Refers to Pin V_{REF} specified for 25°C.
[5] A correction factor can be required on the temperature sensor results when using an external V_{REF} (see the Temperature Sensor Averaging section).
[6] Sampled during initial release to ensure compliance; not subject to production testing.
[7] I_{TOTAL} is the total current flowing in V_{DD} and V_{DRIVE}.
[8] I_{TOTAL} and power dissipation are specified with V_{DD} = V_{DRIVE} = 3.6 V, unless otherwise noted.

I²C TIMING SPECIFICATIONS

Guaranteed by initial characterization. All values were measured with the input filtering enabled. C_B refers to the capacitive load on the bus line, with t_R and t_F measured between 0.3 × V_{DRIVE} and 0.7 × V_{DRIVE} (see Figure 2). V_{DD} = 2.8 V to 3.6 V; V_{DRIVE} = 1.65 V to 3.6 V; V_{REF} = 2.5 V internal/external; T_A = −40°C to +125°C, unless otherwise noted.

Table 3.

		Limit at T_{MIN}, T_{MAX}				
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**	**Description**
f_{SCL}	Standard mode			100	kHz	Serial clock frequency
	Fast mode			400	kHz	
t_1	Standard mode	4			µs	t_{HIGH}, SCL high time
	Fast mode	0.6			µs	
t_2	Standard mode	4.7			µs	t_{LOW}, SCL low time
	Fast mode	1.3			µs	
t_3	Standard mode	250			ns	$t_{SU;DAT}$, data setup time
	Fast mode	100			ns	
t_4[1]	Standard mode	0		3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0		0.9	µs	
t_5	Standard mode	4.7			µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6			µs	
t_6	Standard mode	4			µs	$t_{HD;STA}$, hold time for a repeated start condition
	Fast mode	0.6			µs	
t_7	Standard mode	4.7			µs	t_{BUF}, bus-free time between a stop and a start condition
	Fast mode	1.3			µs	
t_8	Standard mode	4			µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6			µs	
t_9	Standard mode			1000	ns	t_{RDA}, rise time of the SDA signal
	Fast mode	20 + 0.1 C_B		300	ns	
t_{10}	Standard mode			300	ns	t_{FDA}, fall time of the SDA signal
	Fast mode	20 + 0.1 C_B		300	ns	
t_{11}	Standard mode			1000	ns	t_{RCL}, rise time of the SCL signal
	Fast mode	20 + 0.1 C_B		300	ns	
t_{11A}	Standard mode			1000	ns	t_{RCL1}, rise time of the SCL signal after a repeated
	Fast mode	20 + 0.1 C_B		300	ns	start condition and after an acknowledge bit
t_{12}	Standard mode			300	ns	t_{FCL}, fall time of the SCL signal
	Fast mode	20 + 0.1 C_B		300	ns	
t_{SP}	Fast mode	0		50	ns	Pulse width of the suppressed spike
$t_{POWER-UP}$				6	ms	Power-up and acquisition time

[1] A device must provide a data hold time for SDA to bridge the undefined region of the SCL falling edge.

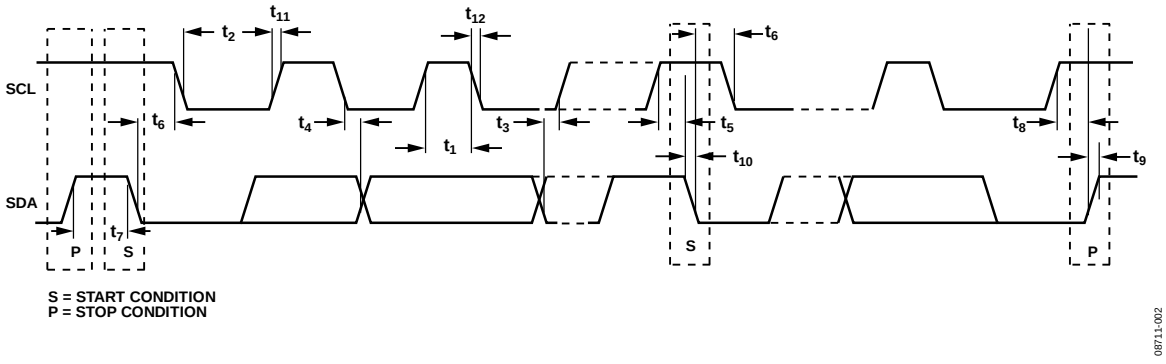

Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to GND1, GND	−0.3 V to +5 V
V_{DRIVE} to GND1, GND	−0.3 V to +5 V
Analog Input Voltage to GND1	−0.3 V to +3 V
Digital Input Voltage to GND1	−0.3 V to V_{DRIVE} + 0.3 V
Digital Output Voltage to GND1	−0.3 V to V_{DRIVE} + 0.3 V
V_{REF} to GND1	−0.3 V to +3 V
GND to GND1	−0.3 V to +0.3 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb-free Temperature, Soldering Reflow	260(+0)°C
ESD	2 kV

[1]Transient currents of up to 100 mA do not cause latch-up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP	52	6.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

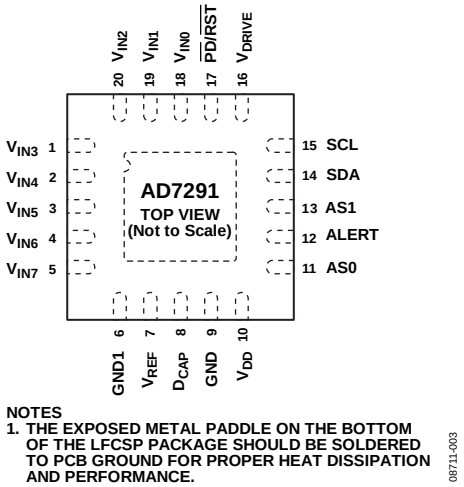

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 5, 18 to 20	V_{IN3}, V_{IN4}, V_{IN5}, V_{IN6}, V_{IN7}, V_{IN0}, V_{IN1}, V_{IN2}	Analog Inputs. The AD7291 has eight single-ended analog inputs that are multiplexed into the on-chip track-and-hold amplifier. Each input channel can accept analog inputs from 0 V to 2.5 V. Any unused input channels must be connected to GND1 to avoid noise pickup.
6	GND1	Ground. Ground reference point for the internal reference circuitry on the AD7291. All analog input signals and the external reference signals must be referred to this GND1 voltage. The GND1 pin must be connected to the ground plane of a system. All ground pins must ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. The V_{REF} pin must be decoupled to this ground pin via a 10 µF decoupling capacitor.
7	V_{REF}	Internal Reference/External Reference Supply. The nominal internal reference voltage of 2.5 V appears at this pin. Provided the output is buffered, the on-chip reference can be taken from this pin and applied externally to the rest of a system. Decoupling capacitors must be connected to this pin to decouple the reference buffer. For best performance, it is recommended to use a 10 µF decoupling capacitor on this pin to GND1. The internal reference can be disabled and an external reference supplied to this pin if required. The input voltage range for the external reference is 2.0 V to 2.5 V.
8	D_{CAP}	Decoupling Capacitor Pin. Decoupling capacitors (1 µF recommended) are connected to this pin to decouple the internal LDO.
9	GND	Ground. Ground reference point for all analog and digital circuitry on the AD7291. The GND pin must be connected to the ground plane of the system. All ground pins must ideally be at the same potential and must not be more than 0.3 V apart, even on a transient basis. Both D_{CAP} and V_{DD} pins must be decoupled to this GND pin.
10	V_{DD}	Supply Voltage, 2.8 V to 3.6 V. This supply must be decoupled to GND with 10 µF and 100 nF decoupling capacitors.
11, 13	AS0, AS1	Logic Input. Together, the logic state of these two inputs selects a unique I^2C address for the AD7291. See Table 31 for details. The device address depends on the voltage applied to these pins.
12	ALERT	Digital Output. This pin acts as an out-of-range indicator and, if enabled, becomes active when the conversion result violates the $DATA_{HIGH}$ or $DATA_{LOW}$ register values. See the Limit Registers (0x04 to 0x1E) section.
14	SDA	Digital Input/Output. Serial bus bidirectional data. This open-drain output requires a pull-up resistor. The output coding is straight binary for the voltage channels and twos complement for the temperature sensor result.
15	SCL	Digital Input. Serial I^2C Bus Clock. This input requires a pull-up resistor. The data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes.
16	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines the voltage at which the interface operates. This pin must be decoupled to GND. The voltage range on this pin is 1.65 V to 3.6 V and can be less than the voltage at V_{DD} but must never exceed it by more than 0.3 V.
17	$\overline{PD}/\overline{RST}$	Power-Down Pin. This pin places the device into a full power-down mode and enables power conservation when operation is not required. This pin can be used to reset the device by toggling the pin low for a minimum of 1 ns and a maximum of 100 ns. If the maximum time is exceeded, the device enters power-down mode. When placing the device in full power-down mode, the analog inputs must be returned to 0 V.
EPAD	EPAD	Exposed Paddle. The exposed metal paddle on the bottom of the LFCSP package must be soldered to PCB ground for proper functionality and heat dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

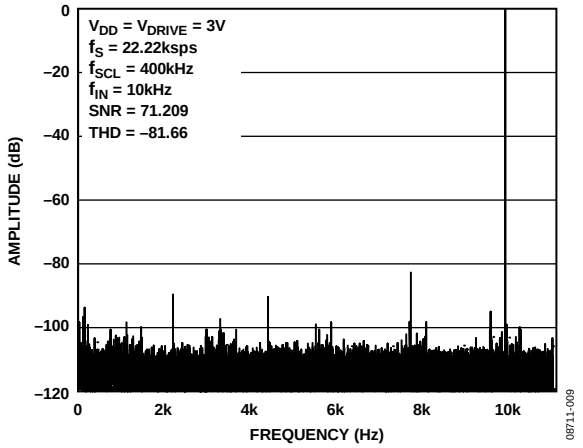

Figure 4. Typical FFT

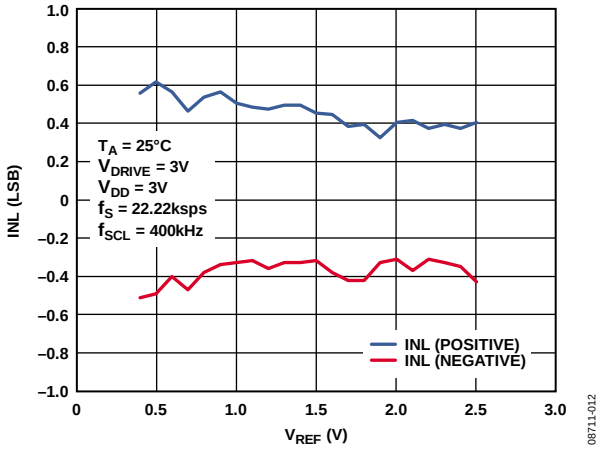

Figure 7. INL vs. External V_{REF}

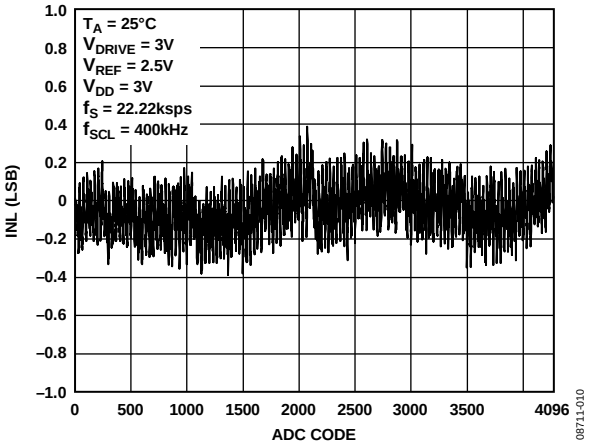

Figure 5. Typical ADC INL

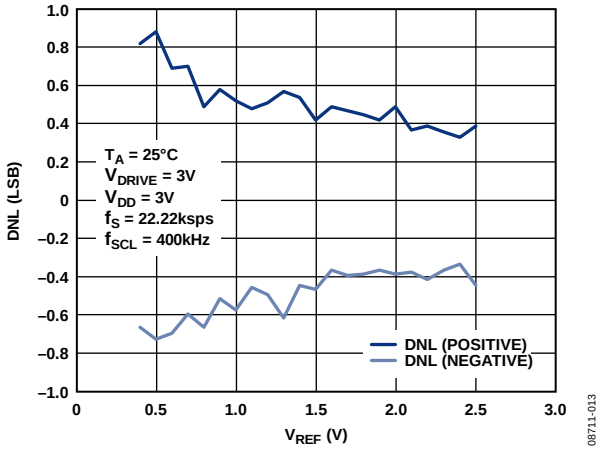

Figure 8. DNL vs. External V_{REF}

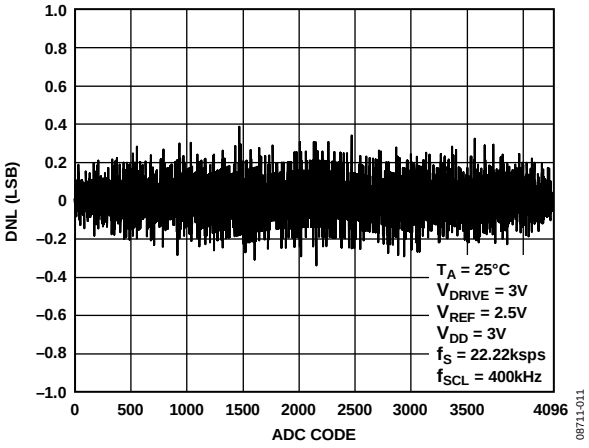

Figure 6. Typical ADC DNL

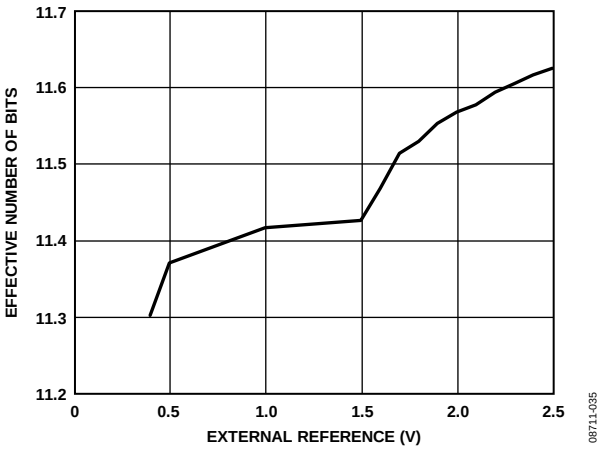

Figure 9. Effective Number of Bits vs. V_{REF}, f_{SCL} = 400 kHz

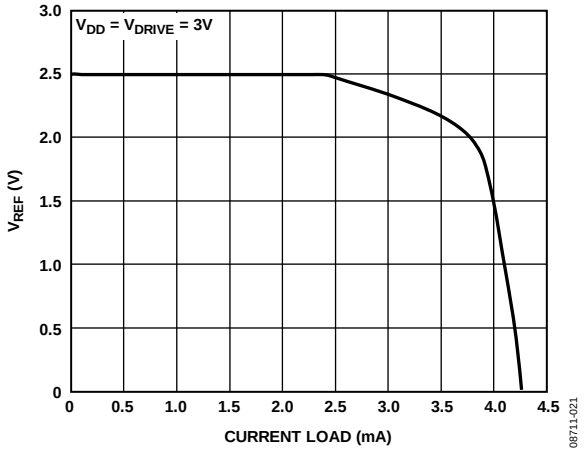

Figure 10. V_{REF} vs. Reference Output Drive

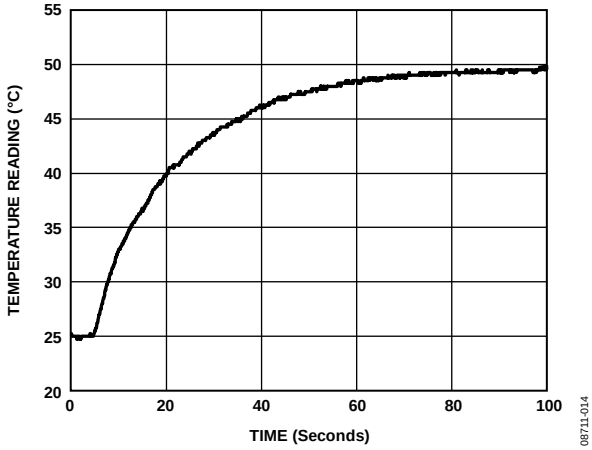

Figure 11. Response to Thermal Shock from Room Temperature into 50°C Stirred Oil

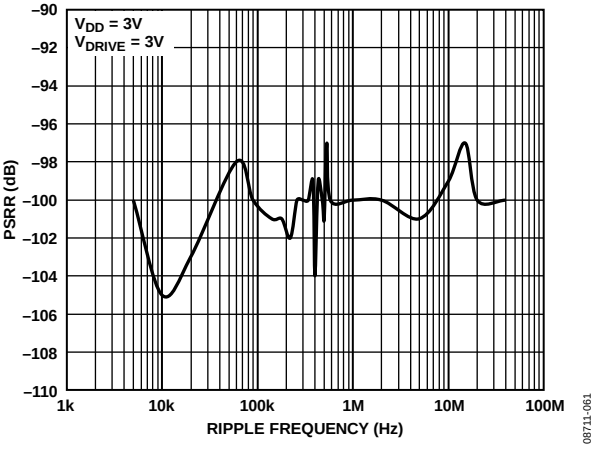

Figure 12. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

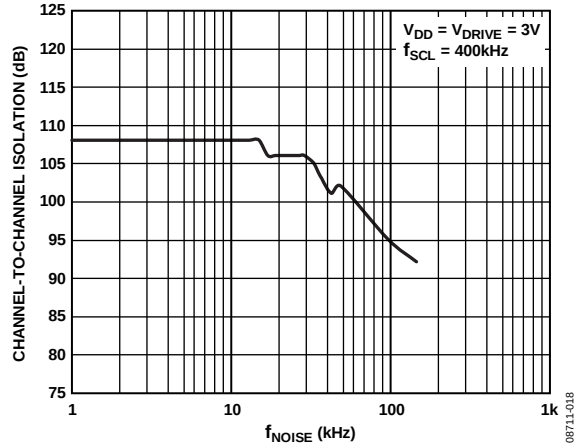

Figure 13. Channel-to-Channel Isolation, f_{IN} = 10 kHz

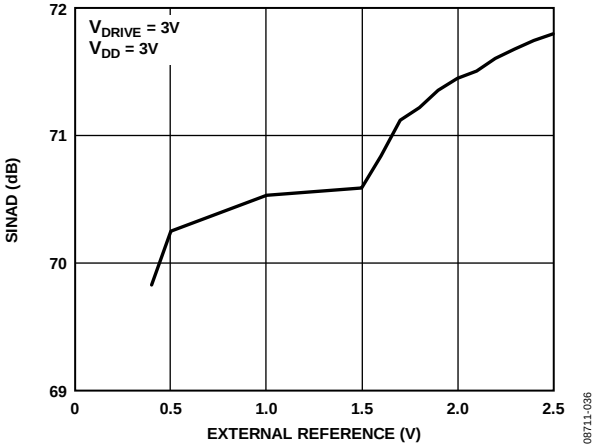

Figure 14. SINAD vs. Reference Voltage, f_{SCL} = 400 kHz, f_S = 22.22 kSPS

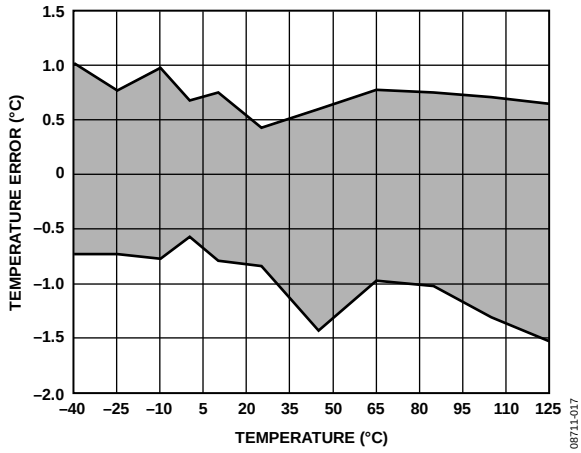

Figure 15. Temperature Accuracy at 3 V

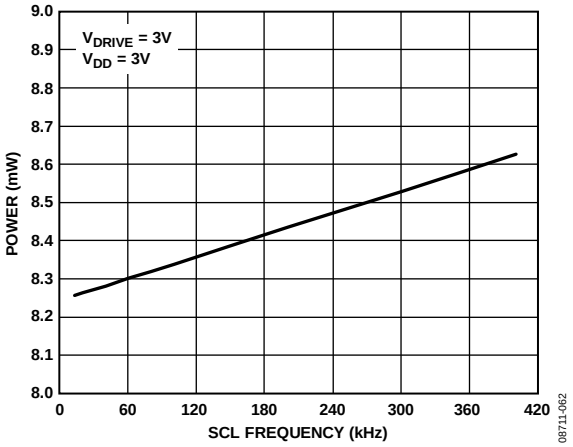

Figure 16. Power vs. Throughput in Normal Mode

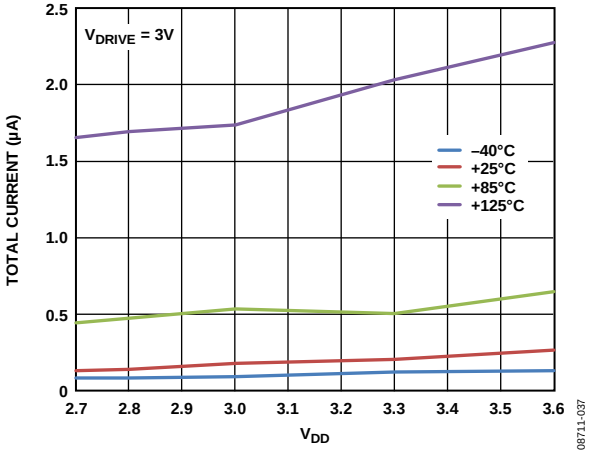

Figure 17. Full Shutdown Current vs. Supply Voltage for Various Temperatures

TERMINOLOGY

Signal-to-Noise and Distortion Ratio (SINAD)
The measured ratio of signal-to-noise and distortion at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal-to-noise and distortion ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\text{-}to\text{-}(Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

Thus, the SINAD is 74 dB for an ideal 12-bit converter.

Total Harmonic Distortion (THD)
The ratio of the rms sum of harmonics to the fundamental. For the AD7291, it is defined as

$$THD\ (\text{dB}) = 20 \log \frac{\sqrt{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Peak Harmonic or Spurious Noise
The ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Typically, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n equals zero. For example, second-order terms include (fa + fb) and (fa − fb), while third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7291 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves while the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of intermodulation distortion is, like the THD specification, the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals, expressed in dB.

Aperture Delay
The measured interval between the sampling clock leading edge and the point at which the ADC takes the sample.

Aperture Jitter
This is the sample-to-sample variation in the effective point in time at which the sample is taken.

Full-Power Bandwidth
The input frequency at which the amplitude of the reconstructed fundamental is reduced by 0.1 dB or 3 dB for a full-scale input.

Power Supply Rejection Ratio (PSRR)
PSRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV p-p sine wave applied to the ADC V_{DD} supply of frequency, f_S. The frequency of the input varies from 5 kHz to 25 MHz.

$$PSRR\ (\text{dB}) = 10 \log(Pf/Pf_S)$$

where:
Pf is the power at frequency, f, in the ADC output.
Pf_S is the power at frequency, f_S, in the ADC output.

Integral Nonlinearity
The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints are zero scale, a point 1 LSB below the first code transition, and full scale, a point 1 LSB above the last code transition.

Differential Nonlinearity
The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
The deviation of the first code transition (00…000) to (00…001) from the ideal—that is, GND1 + 1 LSB.

Offset Error Match
The difference in offset error between any two channels.

Gain Error
The deviation of the last code transition (111…110) to (111…111) from the ideal (that is, V_{REF} − 1 LSB) after the offset error is adjusted out.

Gain Error Match
The difference in gain error between any two channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns to track mode at the end of conversion. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach the final value, within ±1 LSB, after the end of conversion.

CIRCUIT INFORMATION

The AD7291 includes an 8-channel multiplexer, an on-chip track-and-hold amplifier, an analog-to-digital converter (ADC), an on-chip oscillator, internal data registers, an internal temperature sensor, and an I²C-compatible serial interface, all housed in a 20-lead LFCSP. This package offers considerable space-saving advantages over alternative solutions. The device can operate from a single supply from 2.8 V to 3.6 V and offers 12 bits of resolution. The AD7291 has eight single-ended input channels and an on-chip ±12 ppm reference. The analog input range for the AD7921 is 0 V to V_{REF}. The AD7291 includes a high accuracy band gap temperature sensor, which is monitored and digitized by the 12-bit ADC to give a resolution of 0.25°C.

The AD7291 typically remains in a partial power-down state while not converting. When supplies are first applied, the device powers up in a partial power-down state. Power-up is initiated prior to a conversion, and the device returns to partial power-down mode when the conversion is complete. Conversions can be initiated by using the autocycle mode or command mode where wake-up and a conversion occur during a write address function. When the conversion is complete, the AD7291 again enters partial power-down mode.

In command mode at the beginning of a read, the AD7291 wakes up completely, that is, becomes fully functional and completes the conversion while the address is being read out. In autocylce mode, conversions occur at 50 µs intervals; that is, the AD7291 exits partial power-down mode and powers up fully at 50 µs intervals. This automatic partial power-down feature allows power saving between conversions. Any read or write operation across the I²C interface can occur while the device is in partial power-down mode.

CONVERTER OPERATION

The AD7291 is a 12-bit successive approximation ADC based around a capacitive DAC. Figure 18 and Figure 19 show simplified schematics of the ADC during the acquisition and conversion phase, respectively. The ADC comprises control logic, SAR, and a capacitive DAC that are used to add and subtract fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. Figure 18 shows the acquisition phase. SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor acquires the signal on the selected V_{IN} channel.

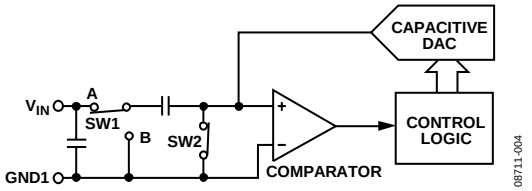

Figure 18. ADC Acquisition Phase

When the ADC starts a conversion (see Figure 19), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to add and subtract fixed amounts of charge to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code. Figure 21 shows the transfer functions of the ADC.

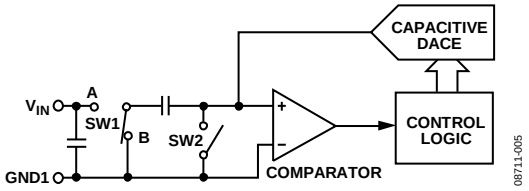

Figure 19. ADC Conversion Phase

ANALOG INPUT

Figure 20 shows an equivalent circuit of the analog input structure of the AD7291. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care must be taken to ensure that the analog input signal never exceeds the internally generated LDO voltage of 2.5 V (D_{CAP}) by more than 300 mV. This causes the diodes to become forward biased and start conducting current into the substrate. The maximum current these diodes can conduct without causing irreversible damage to the device is 10 mA. Capacitor C1, in Figure 20, is typically about 8 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of a switch (track-and-hold switch) and the on resistance of the input multiplexer. The total resistance is typically about 155 Ω. Capacitor C2 is the ADC sampling capacitor and has a capacitance of 34 pF typically.

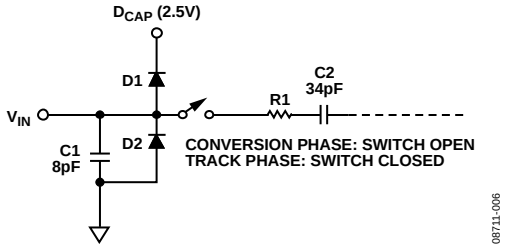

Figure 20. Equivalent Analog Input Circuit

For ac applications, removing high frequency components from the analog input signal is recommended by using an RC low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratios are critical, the analog input must be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC. This can necessitate the use of an input buffer amplifier. The choice of the op amp is a function of the particular application performance criteria.

ADC TRANSFER FUNCTION

The output coding of the AD7291 is straight binary for the analog input channel conversion results and twos complement for the temperature conversion result. The designed code transitions occur at successive LSB values (that is, 1 LSB, 2 LSBs, and so forth). The LSB size is $V_{REF}/4096$ for the AD7291. The ideal transfer characteristic for the AD7291 for straight binary coding is shown in Figure 21.

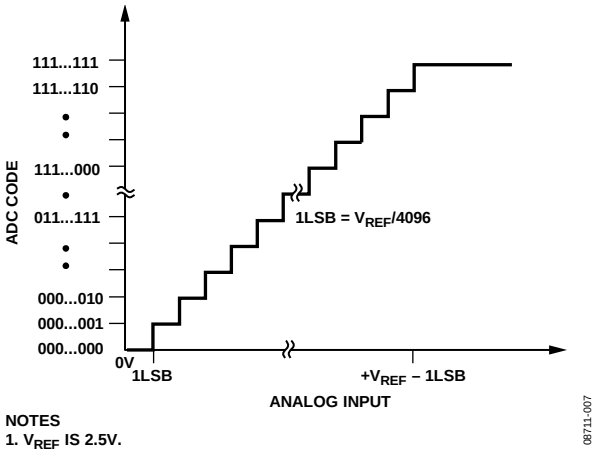

Figure 21. Straight Binary Transfer Characteristic

TEMPERATURE SENSOR OPERATION

The AD7291 contains one local temperature sensor. The on-chip, band gap temperature sensor measures the temperature of the AD7291 die.

The temperature sensor module on the AD7291 is based on the three current principle (see Figure 22), where three currents are passed through a diode and the forward voltage drop is measured, allowing the temperature to be calculated free of errors caused by series resistance.

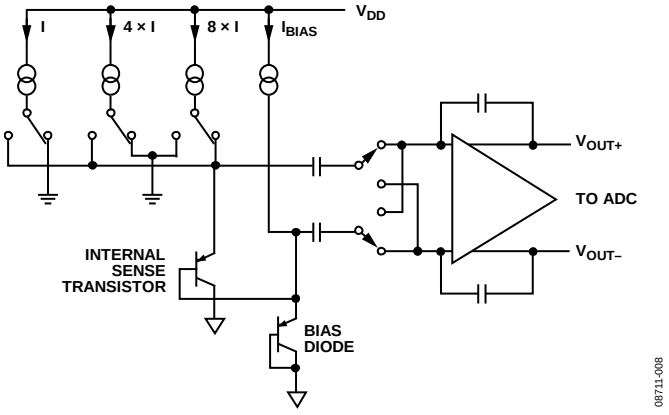

Figure 22. Top Level Structure of Internal Temperature Sensor

Each input integrates, in turn, over a period of several hundred microseconds. This takes place continuously in the background, leaving the user free to perform conversions on the other channels. When integration is complete, a signal passes to the control logic to initiate a conversion automatically.

If the ADC is in command mode and performing a voltage conversion, the AD7291 waits for it to complete and then initiates a temperature sensor conversion. If the ADC is not performing voltage conversions, temperature conversions occur at 5 ms intervals.

In autocycle mode, the conversion is inserted into an appropriate place in the current sequence. If the ADC is idle, the conversion takes place immediately. The T_{SENSE} conversion result register stores the result of the last conversion on the temperature channel; this can be read at any time.

Theoretically, the temperature measuring circuit can measure temperatures from −512°C to +511°C with a resolution of 0.25°C. However, temperatures outside T_A (the specified temperature range for the AD7291) are outside the guaranteed operating temperature range of the device. The temperature sensor is enabled by setting the TSENSE bit in the command register.

TEMPERATURE SENSOR AVERAGING

The AD7291 incorporates a temperature sensor averaging feature to enhance the accuracy of the temperature measurements. The temperature averaging feature is performed continuously in the background provided the TSENSE bit in the command register is enabled. The temperature is measured each time a T_{SENSE} conversion is performed and a moving average method is used to determine the result in the T_{SENSE} average result register. The average result is given by the following equation:

$$T_{SENSE}AVG = \frac{7}{8}(Previous\_Average\_Result) + \frac{1}{8}(Current\_Result)$$

The average result is then available in the T_{SENSE} average result register whose content is updated after every T_{SENSE} conversion.

The first T_{SENSE} conversion result given by the AD7291 after the temperature sensor is selected in the command register (Bit D7) is the actual first T_{SENSE} conversion result, and this result remains valid until the next T_{SENSE} conversion is completed and the result register is updated.

Temperature Value Format

One LSB of the ADC corresponds to 0.25°C. The temperature reading from the ADC is stored in a 12-bit twos complement format, to accommodate both positive and negative temperature measurements. Sample temperature values are listed in Table 7. The temperature conversion formulas are as follows:

Positive Temperature = *ADC Code*/4

Negative Temperature = (4096 − *ADC Code*)/4

The previous formulae are for a V_{REF} of 2.5 V only. If an external reference is used, the temperature sensor requires an external reference of between 2 V and 2.5 V for correct operation. The temperature results (in Celsius) are calculated using the following formula, where V_{EXT_REF} is the value of the external reference voltage.

$$Temperature = V_{EXT\_REF}\left(\frac{ADCCode}{10} + 109.3\right) - 273.15$$

Table 7. Temperature Data Format

Temperature (°C)	Digital Output
−40	1111 0110 0000
−25	1111 1001 1100
−10	1111 1101 1000
−0.25	1111 1111 1111
0	0000 0000 0000
+0.25	0000 0000 0001
+10	0000 0010 1000
+25	0000 0110 0100
+50	0000 1100 1000
+75	0001 0010 1100
+100	0001 1001 0000
+105	0001 1010 0100
+125	0001 1111 0100

V_{DRIVE}

V_{DRIVE} controls the voltage at which the serial interface operates. V_{DRIVE} allows the ADC to easily interface to both 1.8 V and 3 V processors. For example, if the AD7291 is operated with a V_{DD} of 3.3 V, the V_{DRIVE} pin can be powered from a 1.8 V supply. This enables the AD7291 to operate with a larger dynamic range with a V_{DD} of 3.3 V while still being able to interface to 1.8 V processors. Take care to ensure that V_{DRIVE} does not exceed V_{DD} by more than 0.3 V (see the Absolute Maximum Ratings section).

THE INTERNAL OR EXTERNAL REFERENCE

The AD7291 can operate with either the internal 2.5 V on-chip reference or an externally applied reference. The EXT_REF bit in the command register is used to determine whether the internal reference is used. If the EXT_REF bit is selected in the command register, an external reference can be supplied through the V_{REF} pin. On power-up, the internal reference is enabled. Suitable external reference sources for the AD7291 include AD780, AD1582, ADR431, REF193, and ADR391.

The internal reference circuitry consists of a 2.5 V band gap reference and a reference buffer. When the AD7291 operates in internal reference mode, the 2.5 V internal reference is available at the V_{REF} pin, which must be decoupled to GND1 using a 10 µF capacitor. It is recommended that the internal reference be buffered before applying it elsewhere in the system.

The internal reference is capable of sourcing up to 2 mA of current when the converter is static. The reference buffer requires 5.5 ms to power up and charge the 10 µF decoupling capacitor during the power-up time.

RESET

The AD7291 includes a reset feature, which can be used to reset the device and the content of all internal registers including the command register to their default state. To activate the reset operation, the $\overline{PD}/\overline{RST}$ pin must be brought low for a minimum of 1 ns and a maximum of 100 ns and be asynchronous to the clock; therefore, it can be triggered at any time. If the $\overline{PD}/\overline{RST}$ pin is held low for greater than 100 ns, the device enters full power-down mode. It is imperative that the $\overline{PD}/\overline{RST}$ pin be held at a stable logic level at all times to ensure normal operation.

INTERNAL REGISTER STRUCTURE

The AD7291 contains 34 internal registers (see Figure 23) that are used to store conversion results, high and low conversion limits, and information to configure and control the device. There are 33 data registers and one address pointer register.

Each data register has an address that the address pointer register points to when communicating with it. Table 9 details which registers are read, write, or read/write.

ADDRESS POINTER REGISTER

The address pointer register is the register to which the first data byte of every write operation is written automatically; therefore, this register does not have and does not require an address. The address pointer register is an 8-bit register in which the six LSBs are used as pointer bits to store an address that points to one of the AD7291 data registers. The first byte following each write address is to the address pointer register, containing the address of one of the data registers. The six LSBs select the data register to which subsequent data bytes are written. Only the six LSBs of this register are used to select a data register. During power-up, the address pointer register contains all 0s, pointing to the command register.

Table 8. Address Pointer Register

D1	D0	P5	P4	P3	P2	P1	P0
0	0	Register select					

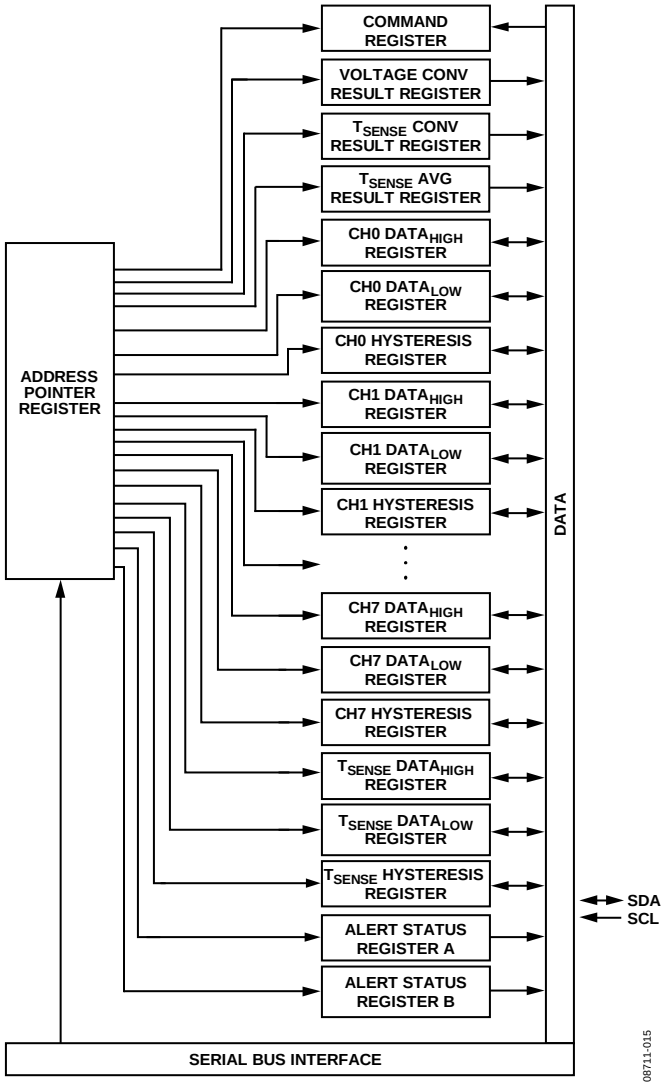

Figure 23. AD7291 Register Structure

Table 9. AD7291 Register Addresses

Hex Code	P5	P4	P3	P2	P1	P0	Registers	Read/Write
0x00	0	0	0	0	0	0	Command register	Write.
0x01	0	0	0	0	0	1	Voltage conversion result register	Read.
0x02	0	0	0	0	1	0	T_{SENSE} conversion result register	Read.
0x03	0	0	0	0	1	1	T_{SENSE} average result register	Read.
0x04	0	0	0	1	0	0	CH0 $DATA_{HIGH}$ register	Read/write.
0x05	0	0	0	1	0	1	CH0 $DATA_{LOW}$ register	Read/write.
0x06	0	0	0	1	1	0	CH0 hysteresis register	Read/write.
0x07	0	0	0	1	1	1	CH1 $DATA_{HIGH}$ register	Read/write.
0x08	0	0	1	0	0	0	CH1$DATA_{LOW}$ register	Read/write.
0x09	0	0	1	0	0	1	CH1 hysteresis register	Read/write.
0x0A	0	0	1	0	1	0	CH2 $DATA_{HIGH}$ register	Read/write.
0x0B	0	0	1	0	1	1	CH2 $DATA_{LOW}$ register	Read/write.
0x0C	0	0	1	1	0	0	CH2 hysteresis register	Read/write.
0x0D	0	0	1	1	0	1	CH3 $DATA_{HIGH}$ register	Read/write.
0x0E	0	0	1	1	1	0	CH3 $DATA_{LOW}$ register	Read/write.
0x0F	0	0	1	1	1	1	CH3 hysteresis register	Read/write.
0x10	0	1	0	0	0	0	CH4 $DATA_{HIGH}$ register	Read/write.
0x11	0	1	0	0	0	1	CH4 $DATA_{LOW}$ register	Read/write.
0x12	0	1	0	0	1	0	CH4 hysteresis register	Read/write.
0x13	0	1	0	0	1	1	CH5 $DATA_{HIGH}$ register	Read/write.
0x14	0	1	0	1	0	0	CH5 $DATA_{LOW}$ register	Read/write.
0x15	0	1	0	1	0	1	CH5 hysteresis register	Read/write.
0x16	0	1	0	1	1	0	CH6 $DATA_{HIGH}$ register	Read/write.
0x17	0	1	0	1	1	1	CH6 $DATA_{LOW}$ register	Read/write.
0x18	0	1	1	0	0	0	CH6 hysteresis register	Read/write.
0x19	0	1	1	0	0	1	CH7 $DATA_{HIGH}$ register	Read/write.
0x1A	0	1	1	0	1	0	CH7 $DATA_{LOW}$ register	Read/write.
0x1B	0	1	1	0	1	1	CH7 hysteresis register	Read/write.
0x1C	0	1	1	1	0	0	T_{SENSE} $DATA_{HIGH}$ register	Read/write.
0x1D	0	1	1	1	0	1	T_{SENSE} $DATA_{LOW}$ register	Read/write.
0x1E	0	1	1	1	1	0	T_{SENSE} hysteresis register	Read/write.
0x1F	0	1	1	1	1	1	Alert Status Register A	Read.
0x20	1	0	0	0	0	0	Alert Status Register B	Read.
0x3F	1	1	1	1	1	1	Factory test mode	The user must not access this register.

COMMAND REGISTER (0x00)

The command register is a 16-bit write-only register that is used to set the operating modes of the AD7291. The bit functions are outlined in Table 10. A two-byte write is necessary when writing to the command register. MSB denotes the first bit in the data stream. During power-up, the default content of the command register is all 0s.

Table 10. Command Register Bits and Default Settings at Power-Up

	MSB								LSB
Channel Bit	**D15 to DB8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Function	CH0 to CH7	TSENSE	Don't care	Noise-delayed bit trial and sampling	EXT_REF	Polarity of ALERT pin (active high/ active low)	Clear alert	RESET	Autocycle mode
Setting	Enable = 1 Disable = 0	Enable = 1 Disable = 0	0	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Active low = 1 Active high = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0	Enable = 1 Disable = 0

Table 11. Command Register Bit Function Descriptions

Bit	Mnemonic	Comment
D15 to D8	CH0 to CH7	These 8-channel address bits select the analog input channel(s) to be converted. A 1 in any of Bit D15 to Bit D8 selects a channel for conversion. If more than one channel bit is set to 1, the AD7291 sequences through the selected channels, starting with the lowest channel. All unused channels must be set to 0. A channel or sequence of channels for conversion must be selected in the command register, prior to initiating a conversion.
D7	TSENSE	This bit enables temperature conversions, which occur in the background at 5 ms intervals. The results can be read from the T_{SENSE} conversion result register (0x02) and the T_{SENSE} average result register (0x03). For details, refer to the Temperature Sensor Operation section.
D6	Don't care	
D5	Noise-delayed bit trial and sampling	When this function is enabled, it delays the critical sampling intervals and bit trials when there is activity on the I^2C bus, thus ensuring improved dc performance of the AD7291. When this feature is enabled, the conversion time can vary. This bit is disabled on power-up, and it is recommended to write a 1 to enable this feature for normal operation.
D4	EXT_REF	Writing a Logic 1 to this bit enables the use of an external reference. The input voltage range for the external reference is 2 V to 2.5 V. The external reference must not exceed 2.5 V or the device performance will be adversely affected. During power-up, the default configuration has the internal reference enabled.
D3	Polarity of ALERT pin	This bit determines the active polarity of the ALERT pin. The ALERT pin is configured for active low operation if this bit is set to 1 and active high if this bit is set to 0. The default configuration on power-up is active high (0).
D2	Clear alert	This bit clears the content of the alert status register. Once the content of both alert status registers is cleared, this bit must be reprogrammed to a Logic 0 to ensure that future alerts are detected.
D1	RESET	Setting this bit resets the contents of all internal registers in the AD7291 to their default states including the command register itself. This bit is automatically returned to 0 once the reset is completed to enable the internal registers to be reprogrammed.
D0	Autocycle mode	Writing a 1 to this bit enables the autocycle mode of operation. In this mode, the channels selected in Bit D15 to Bit D8 are continuously converted by the AD7291. This function is used in conjunction with the limit registers, which can be programmed to issue an alert if the conversion result exceeds the preset limit for any channel selected for conversion.

Table 12. Channel Selection Bits for Command Register

D15	D14	D13	D12	D11	D10	D9	D8	Selected Analog Input Channel	Comments
0	0	0	0	0	0	0	0	No channel selected	If more than one channel is selected, the AD7291 converts the selected channels starting with the lowest channel in the sequence.
0	0	0	0	0	0	0	1	Convert on Channel 7 (V_{IN7})	
0	0	0	0	0	0	1	0	Convert on Channel 6 (V_{IN6})	
0	0	0	0	0	1	0	0	Convert on Channel 5 (V_{IN5})	
0	0	0	0	1	0	0	0	Convert on Channel 4 (V_{IN4})	
0	0	0	1	0	0	0	0	Convert on Channel 3 (V_{IN3})	
0	0	1	0	0	0	0	0	Convert on Channel 2 (V_{IN2})	
0	1	0	0	0	0	0	0	Convert on Channel 1 (V_{IN1})	
1	0	0	0	0	0	0	0	Convert on Channel 0 (V_{IN0})	

Table 13. T_{SENSE} Data Format

Input	D11 (MSB)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
Value (°C)	−512	+256	+128	+64	+32	+16	+8	+4	+2	+1	+0.5	+0.25

Sample Delay and Bit Trial Delay

Ideally, no I²C bus activity must occur while an ADC conversion is taking place. However, this cannot be possible, for example, when operating in autocycle mode. It is therefore recommended to enable the noise delayed bit trial and sampling function by writing a 1 to Bit D5 in the command register. This mechanism delays critical sample intervals and bit trials while there is activity on the I²C bus. This results in a quiet period for each bit decision, and conversion results are less susceptible to interference from external noise.

On power-up, the bit trial and sample interval delay mechanism is not enabled. It is recommended that this feature must be enabled for normal operation. When enabled, the AD7291 delays the bit trials, mitigating against the effect of activity on the I²C bus. In cases where there is excessive activity on the interface lines, enabling these bits can cause the overall conversion time to increase.

The AD7291 also incorporates functionality that allows it to reject glitches shorter than 50 ns. This feature improves the noise susceptibility of the device.

VOLTAGE CONVERSION RESULT REGISTER (0x01)

The voltage conversion result register is a 16-bit read-only register that stores the conversion result from the ADC in straight binary format. A 2-byte read is necessary to read data from this register. Table 14 and Table 15 show the contents of the first and second bytes of data to be read from the AD7291. Each AD7291 conversion result consists of four channel address bits (see Table 14 and Table 15) and the 12-bit data result. Bit D15 to Bit D12 are the channel address bits that identify the ADC channel that corresponds to the subsequent result. Bit D11 to Bit D0 contain the most recent ADC result.

Table 14. Conversion Value Register (First Read)

				MSB			
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
ADD3	ADD2	ADD1	ADD0	B11	B10	B9	B8

Table 15. Conversion Value Register (Second Read)

							LSB
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
B7	B6	B5	B4	B3	B2	B1	B0

Table 16. Channel Address Bits for the Result Register

ADD2	ADD2	ADD1	ADD0	Analog Input Channel
0	0	0	0	V_{IN0}
0	0	0	1	V_{IN1}
0	0	1	0	V_{IN2}
0	0	1	1	V_{IN3}
0	1	0	0	V_{IN4}
0	1	0	1	V_{IN5}
0	1	1	0	V_{IN6}
0	1	1	1	V_{IN7}
1	0	0	0	T_{SENSE}
1	0	0	1	T_{SENSE} average result

Temperature Value Format

The temperature reading from the ADC is stored in an 11-bit twos complement format, D11 to D0, to accommodate both positive and negative temperature measurements. The temperature data format is provided in Table 13.

T_{SENSE} CONVERSION RESULT REGISTER (0x02)

The T_{SENSE} result register is a 16-bit read-only register used to store the ADC data generated from the internal temperature sensor. This register stores the temperature readings from the ADC in a 12-bit twos complement format, D11 to D0, and uses Bit D15 to Bit D12 to store the channel address bits. Conversions take place approximately every 5 ms. Table 13 details the temperature data format that applies to the internal temperature sensor.

Table 17. T_{SENSE} Conversion Result Register (First Read)

MSB

D15	D14	D13	D12	D11	D10	D9	D8
ADD3	ADD2	ADD1	ADD0	B11	B10	B9	B8

Table 18. T_{SENSE} Result Register (Second Read)

LSB

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

TSENSE AVERAGE RESULT REGISTER (0X03)

The T_{SENSE} average result register is a 16-bit read-only register used to store the average result from the internal temperature sensor. This register stores the average temperature readings from the ADC in an 11-bit twos complement format, D11 to D0, and uses Bit D15 to Bit D12 to store the channel address bits. The T_{SENSE} average result register is updated after every T_{SENSE} conversion is completed. The first T_{SENSE} average conversion result given by the AD7291 after averaging is enabled is the actual first T_{SENSE} conversion result. Table 13 details the temperature data format, which applies to the internal temperature sensor. See the Temperature Sensor Averaging section for more details.

Table 19. T_{SENSE} Average Result Register (First Read)

MSB

D15	D14	D13	D12	D11	D10	D9	D8
ADD3	ADD2	ADD1	ADD0	B11	B10	B9	B8

Table 20. T_{SENSE} Average Result Register (Second Read)

LSB

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

LIMIT REGISTERS (0X04 TO 0X1E)

The AD7291 has nine pairs of limit registers. Each pair stores high and low conversion limits for each analog input channel and the internal temperature sensor. Each pair of limit registers has one associated hysteresis register. All 27 registers are 16 bits wide; only the 12 LSBs of the registers are used for the AD7291. The four MSBs, D15 and D12, in these registers must contain 0s. During power-up, the contents of the $DATA_{HIGH}$ register for each analog voltage channel is full scale (0x0FFF), while the default contents of the $DATA_{LOW}$ voltage channels registers is zero scale (0x0000). The output coding of the AD7291 is twos complement for the temperature conversion result. The default content for the T_{SENSE} $DATA_{HIGH}$ register is 0x07FF, while the default content of the T_{SENSE} $DATA_{LOW}$ register is 0x0800. The AD7291 signals an alert in hardware if the conversion result moves outside the upper or lower limit set by the limit registers.

$DATA_{HIGH}$ Register

The $DATA_{HIGH}$ registers for CH0 to CH7 and the internal temperature sensor are 16-bit read/write registers; only the 12 LSBs of each register are used. Bit D15 to Bit D12 are not used in the register and are set to 0s. This register stores the upper limit that activates the ALERT output. If the value in the conversion result register is greater than the value in the $DATA_{HIGH}$ register, an ALERT occurs for that channel. When the conversion result returns to a value at least N LSBs below the $DATA_{HIGH}$ register value, the ALERT output pin is reset. The value of N is taken from the hysteresis register associated with that channel. The ALERT pin can also be reset by writing to Bit D2 in the command register.

Table 21. $DATA_{HIGH}$ Register (First Read/Write)

MSB

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	B11	B10	B9	B8

Table 22. $DATA_{HIGH}$ Register (Second Read/Write)

LSB

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

$DATA_{LOW}$ Register

The $DATA_{LOW}$ register for each channel is a 16-bit read/write register; only the 12 LSBs of each register are used. Bit D15 to Bit D12 are not used in the register and are set to 0s. The register stores the lower limit that activates the ALERT output. If the value in the T_{SENSE} conversion result register is less than the value in the $DATA_{LOW}$ register, an ALERT occurs for that channel. When the conversion result returns to a value at least N LSBs above the $DATA_{LOW}$ register value, the ALERT output pin is reset. The value of N is taken from the hysteresis register associated with that channel. The ALERT output pin can also be reset by writing to Bit D2 in the command register.

Table 23. $DATA_{LOW}$ Register (First Read/Write)

MSB

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	B11	B10	B9	B8

Table 24. $DATA_{LOW}$ Register (Second Read/Write)

LSB

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

HYSTERESIS REGISTER

Each analog input channel and the internal temperature sensor has a hysteresis register, which is a 16-bit read/write register. Only the 12 LSBs are used. Bit D15 to Bit D12 are not used in the register and are set to 0s. The hysteresis register stores the hysteresis value, N, when using the limit registers. Each pair of limit registers has a dedicated hysteresis register. The hysteresis value determines the reset point for the ALERT pin if a violation of the limits occurs. For example, if a hysteresis value of eight LSBs is required on the upper and lower limits of Channel 0, the 16-bit word, 0000 0000 0000 1000, must be written to the hysteresis register of CH0, the address of which is 0x06 (see Table 25 and Table 26). During power-up, the hysteresis registers content defaults to all zeros (0x0000). If a hysteresis value is required, that value must be written to the hysteresis register for the channel in question.

Table 25. Hysteresis Register (First Read/Write Byte)

MSB

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	B11	B10	B9	B8

Table 26. Hysteresis Register (Second Read/Write Byte)

LSB

D7	D6	D5	D4	D3	D2	D1	D0
B7	B6	B5	B4	B3	B2	B1	B0

ALERT STATUS REGISTER A AND ALERT STATUS REGISTER B (0x1F AND 0x20)

The alert status registers are 16-bit, read-only registers that provide information on an alert event. If a conversion result activates the ALERT pin, as described in the Limit Registers (0x04 to 0x1E) section, the alert status register can be read to gain further information. There are two alert status registers in the AD7291; Alert Status Register A, which stores alerts for the analog voltage conversion channels (see Table 27 and Table 28) and Alert Status Register B, which stores alerts for the internal temperature sensor only (see Table 29 and Table 30).

Both alert status registers contain two status bits per channel, one corresponding to the $DATA_{HIGH}$ limit and the other to the $DATA_{LOW}$ limit. The bit with a status of 1 shows where the violation occurred—that is, on which channel—and whether the violation occurred on the upper or lower limit. If a second alert event occurs on the other channel between receiving the first alert and interrogating the alert status register, the corresponding bit for that alert event is also set. The entire contents of the alert status register can be cleared by writing 1 to Bit D2 in the command register.

For example, if Bit D14 in Alert Status Register A is set to 1, the lower limit on Channel 7 (Register 0x1A) is violated, while if Bit D11 is set 1, the upper limit on Channel 5 is violated (Register 0x13).

The $TSENSE_{HIGH}$ and $TSENSE\_AVG_{HIGH}$ alerts are determined by comparison with the T_{SENSE} $DATA_{HIGH}$ register (Register 0x1C). Likewise, the $TSENSE_{LOW}$ and $TSENSE\_AVG_{LOW}$ alerts are determined by comparison with the T_{SENSE} $DATA_{LOW}$ register (Register 0x1D).

Table 27. Alert Status Register A (First Read Byte)

D15	D14	D13	D12	D11	D10	D9	D8
$CH7_{HIGH}$	$CH7_{LOW}$	$CH6_{HIGH}$	$CH6_{LOW}$	$CH5_{HIGH}$	$CH5_{LOW}$	$CH4_{HIGH}$	$CH4_{LOW}$

Table 28. Alert Status Register A (Second Read Byte)

D7	D6	D5	D4	D3	D2	D1	D0
$CH3_{HIGH}$	$CH3_{LOW}$	$CH2_{HIGH}$	$CH2_{LOW}$	$CH1_{HIGH}$	$CH1_{LOW}$	$CH0_{HIGH}$	$CH0_{LOW}$

Table 29. Alert Status Register B (First Read Byte)

D15	D14	D13	D12	D11	D10	D9	D8
0	0	0	0	0	0	0	0

Table 30. Alert Status Register B (Second Read Byte)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	$TSENSE\_AVG_{HIGH}$	$TSENSE\_AVG_{LOW}$	$TSENSE_{HIGH}$	$TSENSE_{LOW}$

I²C INTERFACE

Control of the AD7291 is carried out via the I²C compatible serial bus. The AD7291 is connected to this bus as a slave device under the control of a master device such as the processor.

SERIAL BUS ADDRESS BYTE

The first byte the user writes to the device is the slave address byte. Similar to all I²C-compatible devices, the AD7291 has a 7-bit serial address. The three MSBs of this address are set to 010. The four LSBs are user-programmable by the three-state input pins, AS0 and AS1, as shown in Table 31.

In Table 31, H means tie the pin to V_{DRIVE}, L means tie the pin to GND, and NC refers to a pin left floating. Note that in this final case, the stray capacitance on the pin must be less than 30 pF to allow correct detection of the floating state; therefore, any PCB trace must be kept as short as possible.

Table 31. Slave Address Control Using Three-State Input Pins

		Slave Address (A6 to A0)	
AS1	**AS0**	**Binary**	**Hex**
H	H	010 0000	0x20
H	NC	010 0010	0x22
H	L	010 0011	0x23
NC	H	010 1000	0x28
NC	NC	010 1010	0x2A
NC	L	010 1011	0x2B
L	H	010 1100	0x2C
L	NC	010 1110	0x2E
L	L	010 1111	0x2F

GENERAL I2C TIMING

Figure 24 shows the timing diagram for general read and write operations using an I²C-compliant interface.

When no device is driving the bus, both SCL and SDA are high. This is known as the idle state. When the bus is idle, the master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The master device is responsible for generating the clock.

Data is sent over the serial bus in groups of nine bits—eight bits of data from the transmitter followed by an acknowledge bit (ACK) from the receiver. Data transitions on the SDA line must occur during the low period of the clock signal and remain stable during the high period. The receiver must pull the SDA line low during the acknowledge bit to signal that the preceding byte is received correctly. If this is not the case, cancel the transaction.

The first byte that the master sends must consist of a 7-bit slave address, followed by a data direction bit. Each device on the bus has a unique slave address; therefore, the first byte sets up communication with a single slave device for the duration of the transaction.

The transaction can be used either to write to a slave device (data direction bit = 0) or to read data from it (data direction bit = 1). In the case of a read transaction, it is often necessary first to write to the slave device (in a separate write transaction) to tell it from which register to read. Reading and writing cannot be combined in one transaction.

When the transaction is complete, the master can keep control of the bus, initiating a new transaction by generating another start bit (high-to-low transition on SDA while SCL is high). This is known as a repeated start (SR). Alternatively, the bus can be relinquished by releasing the SCL line followed by the SDA line. This low-to-high transition on SDA while SCL is high is known as a stop bit (P), and it leaves the I²C bus in the idle state (no current is consumed by the bus).

The example in Figure 24 shows a simple write transaction with an AD7291 as the slave device. In this example, the AD7291 register pointer is being set up for a future read transaction.

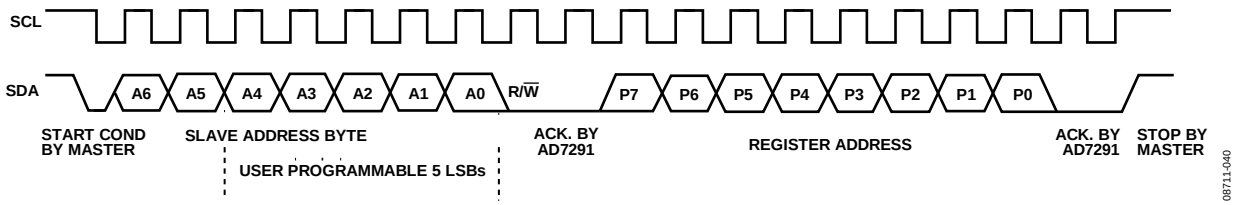

Figure 24. General I²C Timing

WRITING TO THE AD7291

WRITING TWO BYTES OF DATA TO A 16-BIT REGISTER

All registers on the AD7921 are 16-bit registers; therefore, two bytes of data are required to write a value to any one of these registers. Writing two bytes of data to a register consists of the following sequence (see Figure 25):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a register address. The slave asserts an acknowledge on SDA.
5. The master sends the first data byte (most significant).
6. The slave asserts an acknowledge on SDA.
7. The master sends the second data byte (least significant).
8. The slave asserts an acknowledge on SDA.
9. The master asserts a stop condition on SDA to end the transaction.

WRITING TO MULTIPLE REGISTERS

Writing to multiple address registers consists of the following steps (see Figure 26):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device (AD7291) asserts an acknowledge on SDA.
4. The master sends a register address, for example, the CH1 $DATA_{HIGH}$ register address.
5. The slave (AD7291) asserts an acknowledge on SDA.
6. The master sends the first data byte.
7. The slave (AD7291) asserts an acknowledge on SDA.
8. The master sends the second data byte.
9. The slave (AD7291) asserts an acknowledge on SDA.
10. The master sends a second register address, for example, the command register.
11. The slave (AD7291) asserts an acknowledge on SDA.
12. The master sends the first data byte.
13. The slave (AD7291) asserts an acknowledge on SDA.
14. The master sends the second data byte.
15. The slave (AD7291) asserts an acknowledge on SDA.
16. The master asserts a stop condition on SDA to end the transaction.

The previous example details writing to two registers only (the CH1 $DATA_{HIGH}$ register address and the command register). However, the AD7291 can read from multiple registers in one write operation as shown in Figure 26.

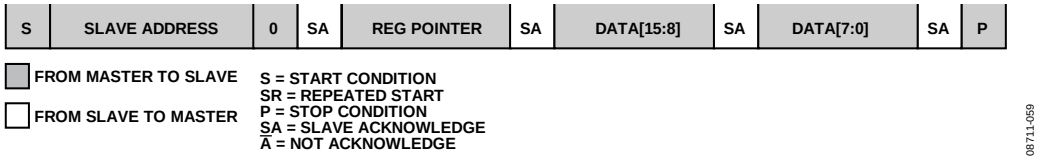

Figure 25. Writing Two Bytes of Data to a 16-Bit Register

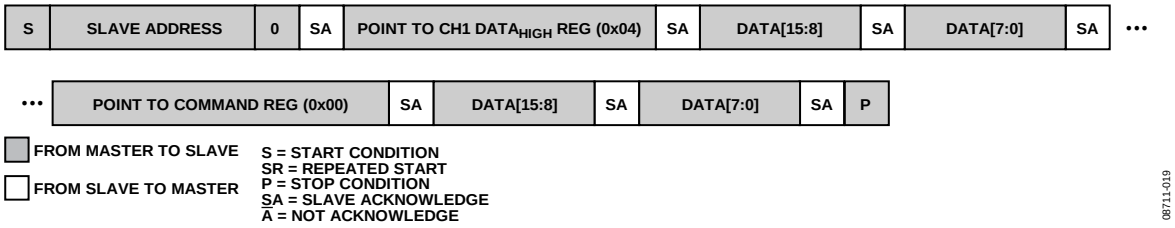

Figure 26. Writing to Multiple Registers

READING DATA FROM THE AD7291

READING TWO BYTES OF DATA FROM A 16-BIT REGISTER

Reading the contents from any of the 16-bit registers is a 2-byte read operation. In this protocol, the first part of the transaction writes to the register pointer. When the register address is set up, any number of reads can be performed from that particular register without having to write to the address pointer register again. When the required number of reads is completed, the master must not acknowledge the final byte. This tells the slave to stop transmitting, allowing a stop condition to be asserted by the master. Further reads from this register can be performed in a future transaction without having to rewrite to the register pointer.

If a read from a different address is required, the relevant register address has to be written to the address pointer register and, again, any number of reads from this register can then be performed. In the following example, the master device reads three lots of 2-byte data from a slave device but as many lots consisting of two bytes can be read as required. This protocol assumes that the particular register address is set up by a single-byte write operation to the address pointer register.

Reading two bytes of data from a 16-bit register consists of the following sequence (see Figure 27):

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts an acknowledge on SDA.
6. The master receives a second data byte.
7. The master asserts an acknowledge on SDA.
8. The master receives a data byte.
9. The master asserts an acknowledge on SDA.
10. The master receives a second data byte.
11. The master asserts an acknowledge on SDA.
12. The master receives a data byte.
13. The master asserts an acknowledge on SDA.
14. The master receives a second data byte.
15. The master asserts a not acknowledge on SDA to notify the slave that the data transfer is complete.
16. The master asserts a stop condition on SDA to end the transaction.

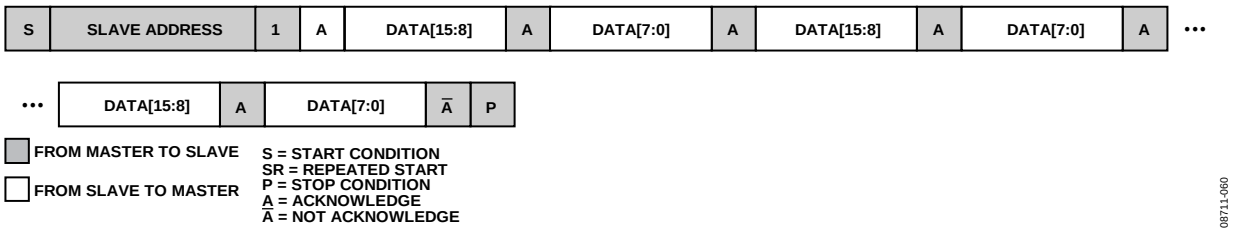

Figure 27. Reading Three Lots of Two Bytes of Data from the Conversion Result Register

MODES OF OPERATION

When supplies are first applied to the AD7291, the ADC powers up in partial power-down mode and normally remains in this partial power-down state while not converting. Once the master addresses the AD7291, it exits partial power-down. There are two methods of initiating a conversion on the AD7291: command mode and autocycle mode.

COMMAND MODE

In command mode, the AD7291 converts on demand on either a single channel or a sequence of channels. Writing in the command register puts the device into command mode. This is the default mode of operation and allows a conversion to be automatically selected any time a write operation occurs to the command register. To enter this mode, the required combination of channels is written into the command register (Register 0x00). Following the write operation, the AD7291 must be addressed again to indicate that a read operation is required. The read then takes place from the voltage or temperature conversion result register. For the first conversion to occur, the address pointer written to the AD7291 must point to the voltage conversion result register or T_{SENSE} conversion result register. The conversion is completed while the first four channel address bits are read. The next conversion in the sequence takes place once the next read from the result register is initiated.

When operating the device in fast mode, the acquisition and conversion times combined take approximately 4.45 µs (1.25 µs acquisition time plus 3.2 µs conversion time). When in command mode, the device cycles through the selected channels from the lowest selected channel in the sequence to the next lowest until all the channels in the sequence are converted.

To exit the command mode, the master must not acknowledge the final byte of data. This stops the AD7291 transmitting, allowing the master to assert a stop condition on the bus. On the receipt of a stop condition, the AD7291 stops converting and enters partial power-down mode, but the content of the command register is preserved. Once the device is readdressed and a read is initiated from the voltage conversion register, the AD7291 begins converting on the previously selected sequence of channels. The conversion sequence starts converting the first selected channel in the sequence; that is, if Channel 1, Channel 2, and Channel 3 are selected and a stop condition occurs after the Channel 1 result is read, on resumption of conversions, Channel 1 is reconverted and the conversion sequence continues.

The example in Figure 28 shows the command mode converting on a sequence of channels including V_{IN0}, V_{IN1}, and V_{IN2}.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device (AD7291) asserts an acknowledge on SDA.
4. The master sends the command register address (0x00).
5. The slave asserts an acknowledge on SDA.
6. The master sends the first data byte (0xE0) to the command register, which selects the V_{IN0}, V_{IN1}, and V_{IN2} channels.
7. The slave asserts an acknowledge on SDA.
8. The master sends the second data byte (0x20) to the command register.
9. The slave asserts an acknowledge on SDA.
10. The master sends the result register address (0x01).
11. The slave asserts an acknowledge on SDA. An optional repeated start (SR) command can be asserted at this point to ensure the bus is not relinquished by the master.
12. The master sends the 7-bit slave address followed by the read bit (high).
13. The slave (AD7291) asserts an acknowledge on SDA.
14. The master receives a data byte, which contains the four channel address bits and the four MSBs of the converted result for Channel V_{IN0}.
15. The master then asserts an acknowledge on SDA.
16. The master receives the second data byte, which contains the eight LSBs of the converted result for Channel V_{IN0}. The master then asserts an acknowledge on SDA.
17. Step 14 to Step 16 are repeated for Channel V_{IN1} and Channel V_{IN2}.
18. Once the master has received the results from all the selected channels, the slave again converts and outputs the result for the first channel in the selected sequence. Step 14 to Step 16 are repeated.
19. The master asserts a not acknowledge on SDA and a stop condition on SDA to end the conversion and exit command mode.

To change the conversion sequence, rewrite a new sequence to the command mode. If a new write to the command register is performed while an existing conversion sequence is underway, the existing conversion sequence is terminated and the next conversion performed is the first selected channel from the new sequence. The maximum throughput that can be achieved using this mode with a 400 kHz I^2C clock is (400 kHz/18) = 22.2 kSPS.

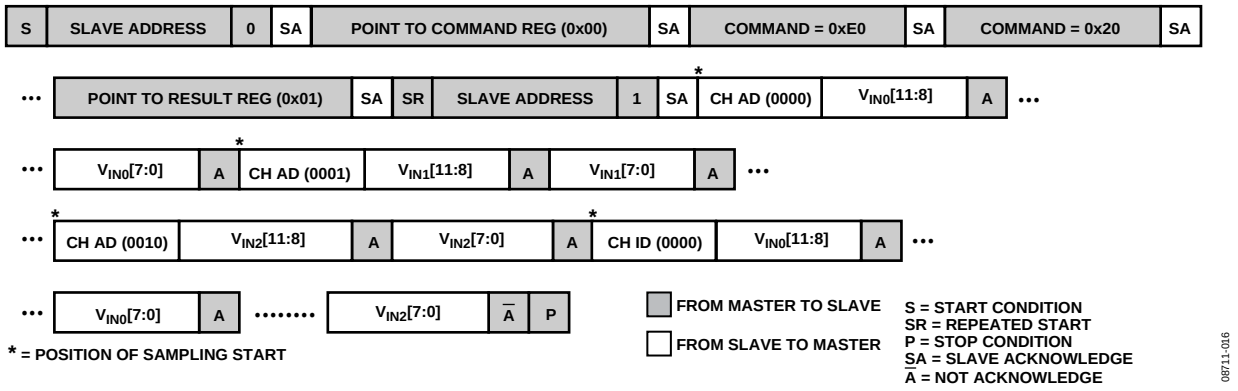

Figure 28. Command Mode Operation

AUTOCYCLE MODE

The AD7291 can be configured to convert continuously on a programmable sequence of channels, making it the ideal mode of operation for system monitoring. This mode is useful for monitoring signals, such as battery voltage and temperature, alerting only when the limits are violated.

Conversions take place in the background approximately every 50 µs, and are transparent to the master. The acquisition and conversion times combined for any channel take approximately 3.6 µs. Typically, this mode is used to automatically monitor a selection of channels with either the limit registers programmed to signal an out-of-range condition via the alert function or the minimum/maximum recorders tracking the variation over time of a particular channel. Reads and writes can be performed at any time (the ADC voltage conversion result register, Register 0x01, contains the most recent conversion result).

During power-up, this mode is disabled. To enable this mode, write to Bit D0 in the command register (Register 0x00) and select the desired channels for conversion by writing to the corresponding channel bits (Bit D15 to Bit D8).

If more than one channel bit is set in the configuration register, the ADC automatically cycles through the channel sequence starting with the lowest channel and working up through the sequence. Once the sequence is complete, the ADC starts converting on the lowest channel again, continuing to loop through the sequence until this mode is exited. Once a conversion is completed, the conversion result is compared with the content of the limit registers, and alert status registers are automatically updated. If a violation of the limit registers is found, the ALERT pin is asserted with the polarity determined by Bit D3 in the command register.

If a command mode conversion is required while the autocycle mode is active, it is necessary to disable the autocycle mode before proceeding to the command mode. This is achieved by setting Bit D0 of the command register to 1. When the command mode conversion is complete, the user can reenable autocycle mode by setting Bit D0 to 1 in the command register. In autocycle mode, the AD7291 does not enter partial power-down on receipt of a stop condition; therefore, conversions and alert monitoring continue to function.

OUTLINE DIMENSIONS

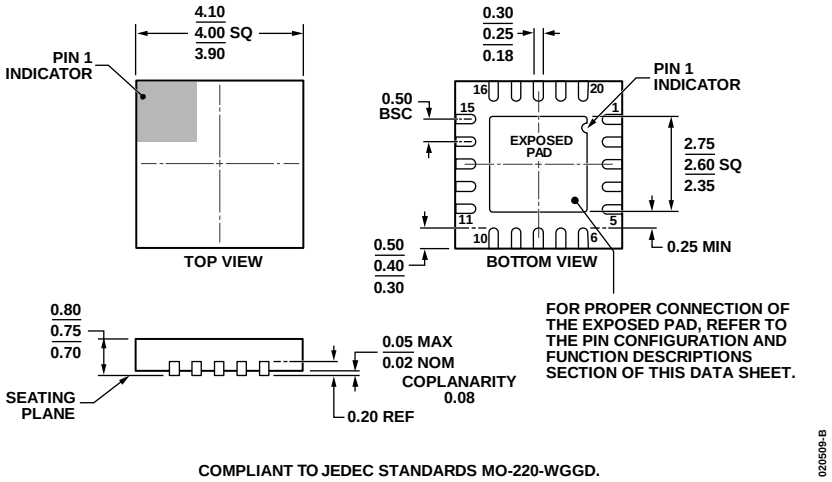

Figure 29. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD7291BCPZ	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-8
AD7291BCPZ-RL7	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-8
EVAL-AD7291SDZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

D08711-0-10/16(C)

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