Freescale Semiconductor
Data Sheet: Advance Information

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MPC5748G

MPC5748G Microcontroller Datasheet

Features

- 2 x 160 MHz Power Architecture® e200Z4 Dual issue, 32-bit CPU
  - Single precision floating point operations
  - 8 KB instruction cache and 4 KB data cache
  - Variable length encoding (VLE) for significant code density improvements
- 1 x 80 MHz Power Architecture® e200Z2 Single issue, 32-bit CPU
  - Using variable length encoding (VLE) for significant code size footprint reduction
- End to end ECC
  - All bus masters, for example, cores generate single error correction, double error detection (SECDED) code for every bus transaction
  - SECDED covers 64-bit data and 29-bit address
- Memory interfaces
  - 6 MB on-chip flash supported with the flash controller
  - 3 x flash page buffers (3 port flash controller)
  - 768 KB on-chip SRAM across three RAM ports
- Clock interfaces
  - 8-40 MHz external crystal (FXOSC)
  - 16 MHz IRC (FIRC)
  - 128 KHz IRC (SIRC)
  - 32 KHz external crystal (SXOSC)
  - Clock Monitor Unit (CMU)
  - Frequency modulated phase-locked loop (FMPLL)
  - Real Time Counter (RTC)
- System Memory Protection Unit (SMPU) with up to 32 region descriptors and 16-byte region granularity
- 16 Semaphores to manage access to shared resource
- Interrupt controller (INTC) capable of routing interrupts to any CPU
- Multiple crossbar switch architecture for concurrent access to peripherals, flash, and RAM from multiple bus masters
- 32-channels eDMA controller with multiple transfer request sources using DMAMUX
- Boot Assist Flash (BAF) supports internal flash programming via a serial link (LIN / SCI)
- Analog
  - Two analog-to-digital converters (ADC), one 10-bit and one 12-bit
  - Three analogue comparators
  - Cross Trigger Unit to enable synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
- Communication
  - Four Deserial Peripheral Interface (DSPI)
  - Six Serial Peripheral interface (SPI)
  - 18 serial communication interface (LIN) modules
  - Eight enhanced FlexCAN3 with FD support
  - Four inter-IC communication interface (IIC)
  - One USB OTG Controller (USB_0) and One USB SPH Controller (USB_1) with ULPI Interface.
  - ENET complex (10/100 Ethernet) that supports Multi queue with AVB support, 1588, and MII/RMII
  - 2 x ENET with L2 switch
  - Secure Digital Hardware Controller (uSDHC)
  - Dual-channel FlexRay Controller
- Audio
  - 3 x Synchronous Audio Interface (SAI)
  - Fractional clock dividers (FCD) operating in conjunction with the SAIs
- Configurable I/O domains supporting FLEXCAN, LINFlex, Ethernet, USB, MLB, uSDHC and general I/O
- Supports wake-up from low power modes via the WKUP controller
- On-chip voltage regulator (VREG)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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Preliminary

- Debug functionality
  - e200Z2 core:NDI per IEEE-ISTO 5001-2008 Class3+
  - e200Z4 core(s): NDI per IEEE-ISTO 5001-2008 Class 3+

- Timer
  - 16 Periodic Interrupt Timers (PITs)
  - Three System Timer Module (STM)
  - Four Software WatchDog Timers (SWT)
  - 96 Configurable Enhanced Modular Input Output Subsystem (eMIOS) channels

- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1) and 1149.7 (cJTAG)

- Security
  - Hardware Security Module (HSMv2)
  - Password and Device Security (PASS and TDM) supporting advanced censorship and life-cycle management
  - One Fault Collection and Control Unit (FCCU) to collect faults and issue interrupts

- Functional Safety
  - ISO26262 ASIL compliance

- Multiple operating modes
  - Includes enhanced low power operation

Table of Contents

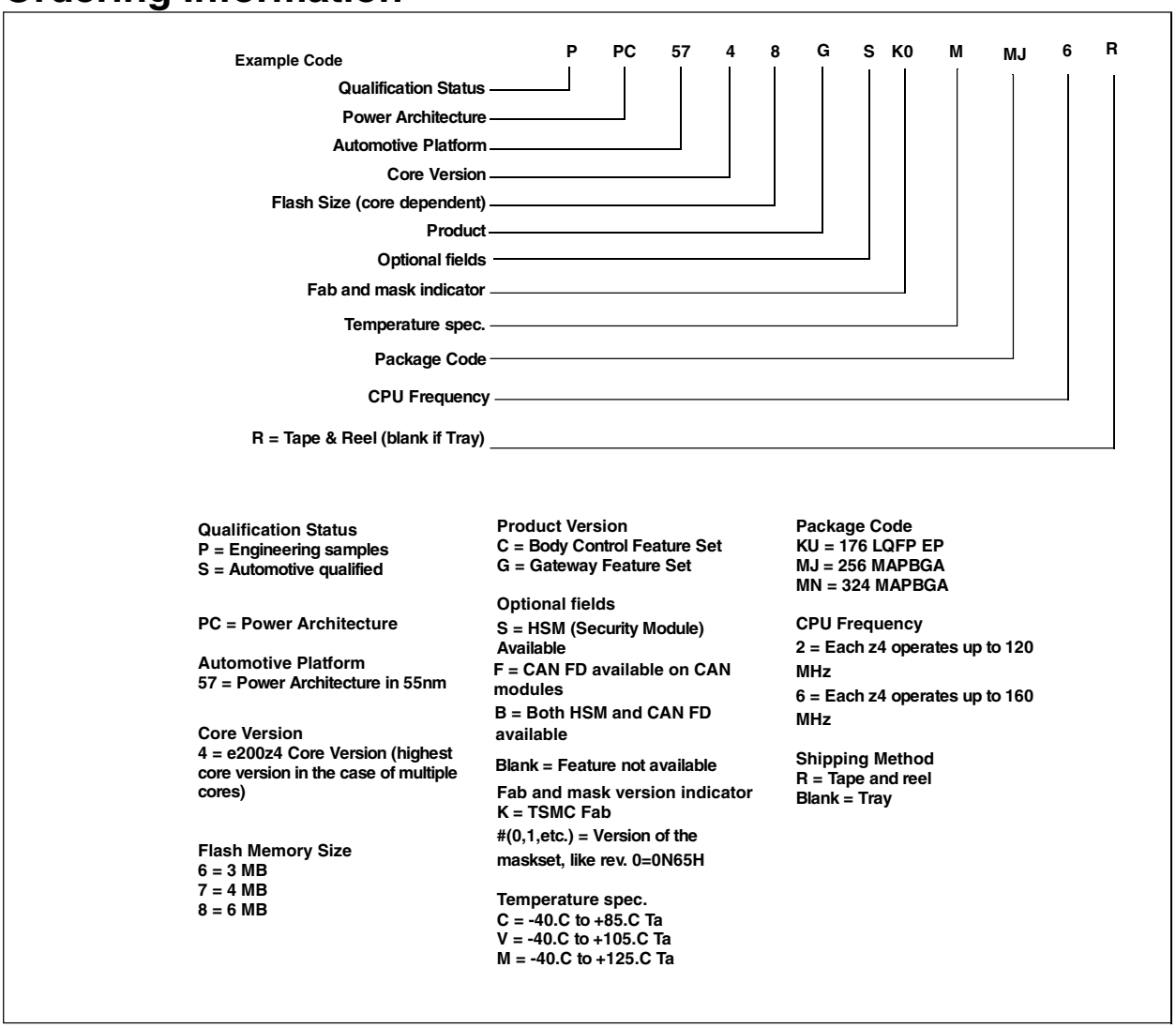
1 Ordering parts....4
1.1 Determining valid orderable parts....4
1.2 Ordering Information....4
2 General....5
2.1 Introduction....5
2.2 Absolute maximum ratings....5
2.3 Recommended operating conditions....6
2.4 Voltage regulator electrical characteristics....8
2.5 Voltage monitor electrical characteristics....11
2.6 Supply current characteristics....12
2.7 Electrostatic discharge (ESD) characteristics....16
2.8 Electromagnetic Compatibility (EMC) specifications....16
3 I/O parameters....17
3.1 AC specifications @ 3.3 V Range....17
3.2 DC electrical specifications @ 3.3V Range....17
3.3 AC specifications @ 5 V Range....18
3.4 DC electrical specifications @ 5 V Range....19
3.5 Functional reset pad electrical specifications....20
3.6 PORST electrical specifications....21
4 Peripheral operating requirements and behaviours....22
4.1 Analog....22
4.1.1 ADC electrical specifications....22
4.1.2 Analogue Comparator (CMP) electrical specifications....25
4.2 Clocks and PLL interfaces modules....26
4.2.1 Main oscillator electrical characteristics....26
4.2.2 32 kHz Oscillator electrical specifications....28
4.2.3 16 MHz RC Oscillator electrical specifications....28
4.2.4 128 KHz Internal RC oscillator Electrical specifications....29
4.2.5 PLL electrical specifications....29
4.3 Memory interfaces....31
4.3.1 Flash memory program and erase specifications. 31
4.3.2 Flash memory Array Integrity and Margin Read specifications....32
4.3.3 Flash memory module life specifications....32
4.3.4 Data retention vs program/erase cycles....33
4.3.5 Flash memory AC timing specifications....34
4.3.6 Flash read wait state and address pipeline control settings....35
4.4 Communication interfaces....35
4.4.1 DSPI timing....35
4.4.2 FlexRay electrical specifications....41
4.4.2.1 FlexRay timing....41
4.4.2.2 TxEN....42
4.4.2.3 TxD....43
4.4.2.4 RxD....44
4.4.3 uSDHC specifications....45
4.4.4 Ethernet switching specifications....46
4.4.5 MediaLB (MLB) electrical specifications....47
4.4.5.1 MLB 3-pin interface DC characteristics....47
4.4.5.2 MLB 3-pin interface electrical specifications....48
4.4.6 USB electrical specifications....50
4.4.6.1 USB electrical specifications....50
4.4.6.2 ULPI timing specifications....50
4.4.7 SAI electrical specifications....51
4.5 On-chip peripherals....54
4.5.1 On-chip peripherals....54
4.6 Debug specifications....55
4.6.1 JTAG interface timing....55
4.6.2 Nexus timing....57
4.6.3 WKUP/NMI timing....59
4.6.4 External interrupt timing (IRQ pin)....60
5 Thermal attributes....60
5.1 Thermal attributes....60
6 Dimensions....63
6.1 Obtaining package dimensions....63
7 Pinouts....63
7.1 Package pinouts and signal descriptions....63
8 Revision History....64

1 Ordering parts

1.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.freescale.com and perform a part number search for the following device number: MPC5748G .

1.2 Ordering Information



2 General

2.1 Introduction

The electrical specifications are preliminary and are initial evaluation. These specifications are not fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

2.2 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions	Min	Max[1]	Unit
$V_{DD_HV_A}$, $V_{DD_HV_B}$, $V_{DD_HV_C}$[2]	3.3 V - 5. 5V input/output supply voltage	—	–0.3	6.0	V
V_{SS_HV}	Input/output ground voltage	—	–0.1	0.1	V
$V_{DD_HV_FLA}$[3, 4]	3.3 V flash supply voltage (when supplying from an external source in bypass mode)	—	–0.3	3.63	V
$V_{DD_LP_DEC}$[5]	Decoupling pin for low power regulators[6]	—	–0.3	1.32	V
$V_{DD_HV_ADC1_REF}$[7]	3.3 V / 5.0 V ADC1 high reference voltage	—	–0.3	6	V
$V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$	3.3 V to 5.5V ADC supply voltage	—	–0.3	6.0	V
$V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$	3.3V to 5.5V ADC supply ground	—	–0.1	0.1	V
V_{INA}	Voltage on analog pin with respect to ground (V_{SS_HV})	—	–0.3	$V_{DD_HV_x}$ + 0.3	V
V_{IN}	Voltage on any digital pin with respect to ground (V_{SS_HV})	Relative to $V_{DD_HV_A}$, $V_{DD_HV_B}$, $V_{DD_HV_C}$	–0.3	$V_{DD_HV_x}$ + 0.3	V

Table continues on the next page...

Table 1. Absolute maximum ratings (continued)

Symbol	Parameter	Conditions	Min	Max[1]	Unit
I_{INJPAD}	Injected input current on any pin during overload condition	Always	–5	5	mA
I_{INJSUM}	Absolute sum of all injected input currents during overload condition	—	–50	50	mA
T_{ramp}	Supply ramp rate	—	0.5 V / min	100V/ms	—
Ta[8]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	–55	165	°C

1. Absolute maximum voltages are currently maximum burn-in voltages. Absolute maximum specifications for device stress have not yet been determined.
2. VDD_HV_B and VDD_HV_C are common together on the 176 LQFP package.
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. VDD_HV_FLA must be disconnected from ANY power sources when VDD_HV_A = 5V
5. This pin should be decoupled with low ESR 1 µF capacitor.
6. Not available for input voltage, only for decoupling internal regulators
7. 10-bit ADC does not have dedicated reference and its reference is double bonded to 10-bit ADC supply(VDD_HV_ADC0).
8. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA. SeeThermal attributes

2.3 Recommended operating conditions

NOTE

- For normal device operations, all supplies must be within operating range corresponding to the range mentioned in following tables. This is required even if some of the features are not used.
- If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be externally supplied using a 3.3V source. If VDD_HV_A is in 3.3V range, VDD_HV_FLA should be shorted to VDD_HV_A.

Table 2. Recommended operating conditions ($V_{DD_HV_x}$ = 3.3 V)

Symbol	Parameter	Conditions	Min[1]	Max	Unit
$V_{DD_HV_A}$[2] $V_{DD_HV_B}$[2] $V_{DD_HV_C}$[2]	3.3 V input/output supply voltage	—	3.15	3.6	V
V_{SS_HV}	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FLA}$[3]	3.3 V flash supply voltage (generated internally)	—	3.15	3.6	V
$V_{DD_HV_ADC1_REF}$	3.3 V / 5.0 V ADC1 high reference voltage	—	3.0	5.5	V
$V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$	3.3 V ADC supply voltage	—	3.15	3.6 [4]	V

Table continues on the next page...

Table 2. Recommended operating conditions ($V_{DD_HV_x}$ = 3.3 V) (continued)

Symbol	Parameter	Conditions	Min[1]	Max	Unit
$V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$	3.3 V ADC supply ground	—	0	0	V
V_{DD_LV}[5]	Internal supply voltage	—	1.2	1.32	V
$V_{IN1_CMP_REF}$[5, 6, 7]	Analog Comparator DAC reference voltage	—	3.15	3.6 [6]	V
V_{SS_LV}	Internal reference voltage	—	0	0	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A[8]	Ambient temperature under bias	$f_{CPU} \leq 160$ MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where the LVD_IO_A_LO resets the device. When voltage drops below VLVD_IO_A_LO, device is reset.
2. VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. For example, if VDD_HV_A = 5V, then VDD_HV_B and VDD_HV_C can both be 3.3V. However, care must be taken over ADC inputs that operate across the IO segments (Subject to Note 1).
3. VDD_HV_FLA must be connected to VDD_HV_A when VDD_HV_A = 3.3V
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from VDD_HV_B domain hence VDD_HV_ADC1 should be within ±100 mV of VDD_HV_B when these channels are used for ADC_1.
5. Only applicable when supplying from external source.
6. VIN1_CMP_REF ≤ VDD_HV_A
7. This supply is shorted VDD_HV_A on lower packages.
8. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA. SeeThermal attributes

NOTE

- If VDD_HV_A is in 5V range, it is necessary to use internal Flash supply 3.3V regulator. VDD_HV_FLA should not be supplied externally and should only have decoupling capacitor.

Table 3. Recommended operating conditions ($V_{DD_HV_x}$ = 5 V)

Symbol	Parameter	Conditions	Min[1]	Max	Unit
$V_{DD_HV_A}$[2] $V_{DD_HV_B}$[2] $V_{DD_HV_C}$[2]	5.0 V input/output supply voltage	—	4.5	5.5	V
V_{SS_HV}	Input/output ground voltage	—	0	0	V
$V_{DD_HV_FLA}$[3]	3.3 V flash supply voltage	—	3.15	3.6	V
$V_{DD_HV_ADC1_REF}$	3.3 V / 5.0 V ADC1 high reference voltage	—	3.0	5.5	V
$V_{DD_HV_ADC0}$ $V_{DD_HV_ADC1}$	3.3 V / 5.0 V ADC supply voltage	—	3.0	5.5	V
$V_{SS_HV_ADC0}$ $V_{SS_HV_ADC1}$	5.0 V ADC supply ground	—	0	0	V

Table continues on the next page...

Table 3. Recommended operating conditions ($V_{DD_HV_x}$ = 5 V) (continued)

Symbol	Parameter	Conditions	Min[1]	Max	Unit
V_{DD_LV}[4]	Internal supply voltage	—	1.2	1.32	V
V_{SS_LV}	Internal reference voltage	—	0	0	V
I_{INJPAD}	Injected input current on any pin during overload condition	—	-3.0	3.0	mA
T_A[5]	Ambient temperature under bias	$f_{CPU} \leq 160$ MHz	–40	125	°C
T_J	Junction temperature under bias	—	–40	150	°C

1. Device will be functional down (and electrical specifications as per various datasheet parameters will be guaranteed) to the point where the LVD_IO_A_LO resets the device. When voltage drops below VLVD_IO_A_LO, device is reset.
2. VDD_HV_A, VDD_HV_B and VDD_HV_C are all independent supplies and can each be set to 3.3V or 5V. For example, if VDD_HV_A = 5V, then VDD_HV_B and VDD_HV_C can both be 3.3V. However, care must be taken over ADC inputs that operate across the IO segments.
3. When VDD_HV is in 5 V range, VDD_HV_FLA cannot be supplied externally.This pin is decoupled with C_{flash_reg}.
4. PA3, PA7, PA10, PA11 and PE12 ADC_1 channels are coming from VDD_HV_B domain hence VDD_HV_ADC1 should be within ±100 mV of VDD_HV_B when these channels are used for ADC_1.
5. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA. SeeThermal attributes

2.4 Voltage regulator electrical characteristics

The voltage regulator is composed of the following blocks:

- Choice of generating supply voltage for the core area.
  - Control of external NPN ballast transistor
  - Connecting an external 1.25V (nominal) directly without the NPN ballast
- Internal generation of the 3.3V flash supply when device connected in 5V applications
- External bypass of the 3.3V flash regulator when device connected in 3.3V applications
- Low voltage detector - low range (LVD_IO_A_LO) for 3.3 V to 5V supply to IO ($V_{DD_HV_A}$)
- Low voltage detector - high range (LVD_IO_A_Hi) for the 3.3 V to 5V supply (VDD_HV_A)
- Low voltage detector (LVD_FLASH) for 3.3 V flash supply (VDD_HV_FLA)
- Various low voltage detectors (LVD_LV_x) for 1.2 V digital core supply (VDD_LV)
- High voltage detector (HVD_LV_cold) for 1.2 V digital core supply (VDD_LV)
- Power on Reset (POR_LV) for 1.25 V digital core supply (VDD_LV)
- Power on Reset (POR_HV) for 3.3V to 5V supply (VDD_HV_A)

The following bipolar transistors[1] are supported, depending on the device performance requirements. As a minimum the following must be considered when determining the most appropriate solution to maintain the device under its maximum power dissipation capability: current, ambient temperature, mounting pad area, duty cycle and frequency for Idd, collector voltage, etc

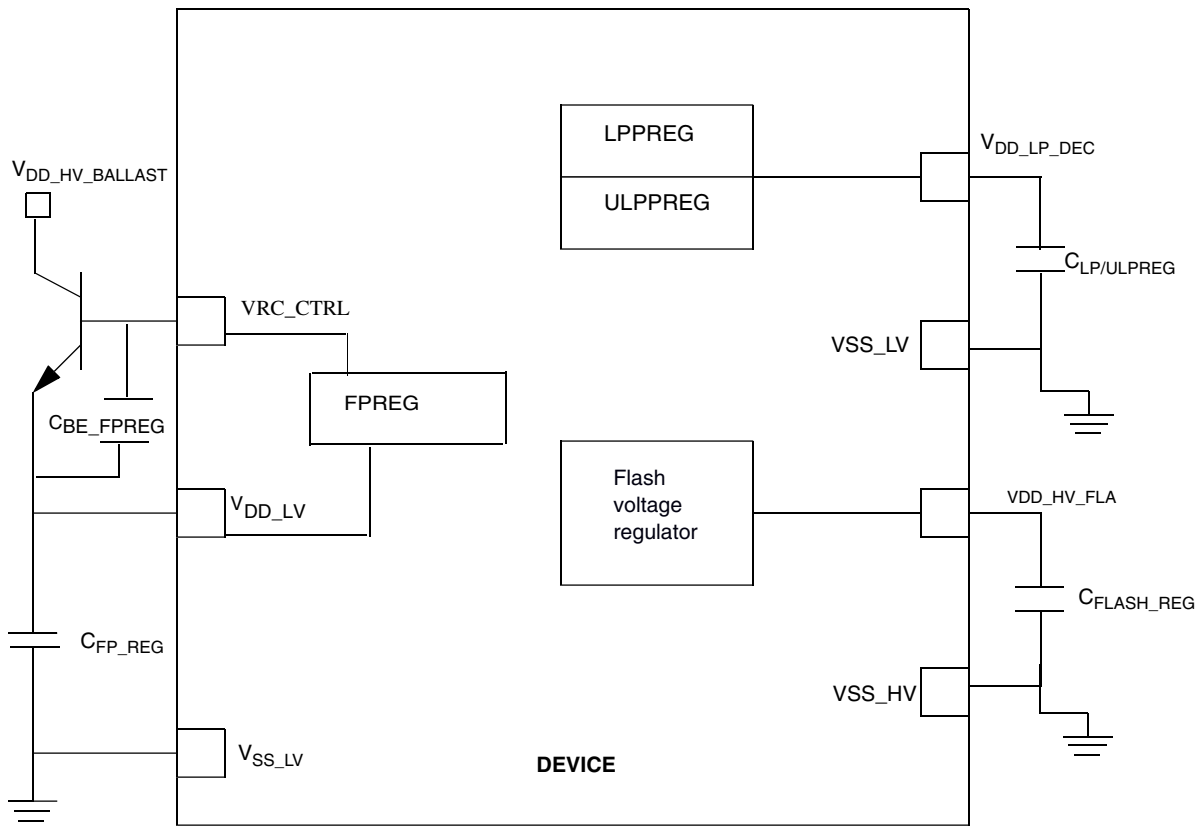


Figure 1. Voltage regulator capacitance connection

Table 4. Voltage regulator electrical specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{fp_reg}[1]	External decoupling / stability capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2[2]	3	µF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
C_{lp/ulp_reg}	External decoupling / stability capacitor for internal low power regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.8	1	1.4	µF
	Combined ESR of external capacitor	—	0.001	—	0.1	Ohm

Table continues on the next page...

1. These are guaranteed ballasts.

Table 4. Voltage regulator electrical specifications (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{be_fpreg}	Capacitor in parallel to base-emitter	BCP68 and BCP56		3.3		nF
		MJD31		4.7		
C_{flash_reg}[3]	External decoupling / stability capacitor for internal Flash regulators	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1.32	2.2	3	µF
	Combined ESR of external capacitor	—	0.001	—	0.03	Ohm
$C_{HV_VDD_A}$	VDD_HV_A supply capacitor	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	µF
C_{HV_ADC0} C_{HV_ADC1}	HV ADC supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	1	—	—	µF
C_{HV_ADR}	HV ADC SAR reference supply decoupling capacitances	Min, max values shall be granted with respect to tolerance, voltage, temperature, and aging variations.	0.47	—	—	µF
$V_{DD_HV_BALLAST}$	FPREG Ballast collector supply voltage	When collector of NPN ballast is directly supplied by an on board supply source (not shared with VDD_HV_A supply pin) without any series resistance, that is, $R_{C_BALLAST}$ less than 0.01 Ohm.	2.25	—	5.5	V
$R_{C_BALLAST}$	Series resistor on collector of FPREG ballast	When VDD_HV_BALLAST is shorted to VDD_HV_A on the board	—	—	0.1	Ohm
t_{SU}	Start-up time after main supply stabilization	Cfp_reg = 3 µF	—	74	—	µs
t_{ramp}	Load current transient	Iload from 15% to 55% C_{fp_reg} = 3 µF		1.0		µs

1. Split capacitance on each pair VDD_LV pin should sum up to a total value of C_{fp_reg}
2. Typical values will vary over temperature, voltage, tolerance, drift, but total variation must not exceed minimum and maximum values.
3. It is required to minimize the board parasitic inductance from decoupling capacitor to VDD_HV_FLA pin and the routing inductance should be less than 1nH.

2.5 Voltage monitor electrical characteristics

Table 5. Voltage monitor electrical characteristics

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2, 2]	Reset Type	Min	Typ	Max	V
V_{POR_LV}	LV supply power on reset detector	Fall	Untrimmed	Yes	No	Powerup	0.930	0.979	1.028	V
			Trimmed				0.959	0.979	0.999	V
		Rise	Untrimmed				0.980	1.029	1.078	V
			Trimmed				1.009	1.029	1.049	V
$V_{HVD_LV_cold}$	LV external supply high voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.330	1.345	1.360	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.350	1.365	1.380	V
$V_{LVD_LV_PD2_hot}$	LV internal supply low voltage monitoring, detecting in the PD2 core (hot) area	Fall	Untrimmed	Yes	No	Powerup	1.080	1.120	1.160	V
			Trimmed				1.130	1.145	1.160	V
		Rise	Untrimmed				1.100	1.140	1.180	V
			Trimmed				1.150	1.165	1.180	V
$V_{LVD_LV_PD1_hot}$	LV internal supply low voltage monitoring, detecting in the PD1 core (hot) area	Fall	Untrimmed	Yes	No	Powerup	1.080	1.120	1.160	V
			Trimmed				1.114	1.137	1.160	V
		Rise	Untrimmed				1.100	1.140	1.180	V
			Trimmed				1.134	1.157	1.180	V
$V_{LVD_LV_PD0_hot}$	LV internal supply low voltage monitoring, detecting in the PD0 core (hot) area	Fall	Untrimmed	Yes	No	Powerup	1.080	1.120	1.160	V
			Trimmed				1.114	1.137	1.160	V
		Rise	Untrimmed				1.100	1.140	1.180	V
			Trimmed				1.134	1.157	1.180	V
V_{POR_HV}	HV supply power on reset detector	Fall	Untrimmed	Yes	No	Powerup	2.700	2.850	3.000	V
			Trimmed				2.815	2.873	2.930	V
		Rise	Untrimmed				2.750	2.900	3.050	V
			Trimmed				2.845	2.903	2.960	V
$V_{LVD_IO_A_LO}$[3]	HV IO_A supply low voltage monitoring - low range	Fall	Untrimmed	Yes	No	Powerup	2.750	2.923	3.095	V
			Trimmed				2.978	3.039	3.100	V
		Rise	Untrimmed				2.780	2.953	3.125	V
			Trimmed				3.008	3.069	3.130	V

Table continues on the next page...

Table 5. Voltage monitor electrical characteristics (continued)

Symbol	Parameter	State	Conditions	Configuration			Threshold			Unit
				Power Up [1]	Mask Opt[2, 2]	Reset Type	Min	Typ	Max	V
$V_{LVD_IO_A_HI}$[3]	HV IO_A supply low voltage monitoring - high range	Fall	Trimmed	No	Yes	Functional	Disabled at Start			
							4.068	4.151	4.234	V
		Rise	Trimmed				Disabled at Start			
							4.118	4.201	4.284	V
V_{LVD_FLASH}	Flash supply low voltage monitoring	Fall	Untrimmed	Yes	No	Powerup	2.898	3.004	3.110	V
			Trimmed				2.900	2.930	2.960	V
		Rise	Untrimmed				2.918	3.024	3.130	V
			Trimmed				2.920	2.950	2.980	V
V_{LVD_FLASH} during low power mode using LPBG as reference[4]		Fall	Untrimmed				Disable			
			Trimmed				2.650	2.704	2.758	V
		Rise	Untrimmed				Disable			
			Trimmed				2.670	2.724	2.778	V
$V_{LVD_LV_PD2_cold}$	LV internal supply low voltage monitoring, detecting at the device pin	Fall	Untrimmed	No	Yes	Functional	Disabled at Start			
			Trimmed				1.145	1.160	1.175	V
		Rise	Untrimmed				Disabled at Start			
			Trimmed				1.165	1.180	1.195	V

1. All monitors that are active at power-up will gate the power up recovery and prevent exit from POWERUP phase until the minimum level is crossed. These monitors can in some cases be masked during normal device operation, but when active will always generate a destructive reset.
2. Voltage monitors marked as non maskable are essential for device operation and hence cannot be masked.
3. There is no voltage monitoring on the VDD_HV_B and VDD_HV_C I/O segments. For applications requiring monitoring of these segments, either connect these to VDD_HV_A at the pcb level or monitor externally.
4. LVD_FLASH is active in low power modes to ensure that VDD_HV_FLA does not drop below 2.5V, so that Flash can exit from low power mode upon wakeup.

2.6 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

NOTE

The ballast must be chosen in accordance with the ballast transistor supplier operating conditions and recommendations.

Table 6. Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{DD_FULL} 2, 3	RUN Full Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85°C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	310	520	mA
		T_a = 105°C	—	—	540	mA
		T_a = 125 °C[4]	—	—	575	mA
I_{DD_GWY} 5, 6	RUN Gateway Mode Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85°C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 160MHz	—	—	460	mA
		T_a = 105°C	—	—	486	mA
		T_a = 125°C[4]	—	—	521	mA
$I_{DD_BODY_1}$ 7, 8	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85 °C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 120MHz	—	—	345	mA
		T_a = 105 °C	—	—	370	mA
		T_a = 125°C [4]	—	—	405	mA
IDD_BODY_2[9, 10]	RUN Body Mode Profile Operating current	LV supply + HV supply + HV Flash supply + 2 x HV ADC supplies T_a = 85 °C V_{DD_LV} = 1.25 V VDD_HV_A = 5.5V SYS_CLK = 80MHz	—	—	275	mA
		T_a = 105 °C	—	—	300	mA
		T_a = 125 °C [4]	—	—	336	mA

Table continues on the next page...

Table 6. Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
I_{DD_STOP}	STOP mode Operating current	T_a = 25 °C V_{DD_LV} = 1.25 V	—	11	—	mA
		T_a = 55 °C V_{DD_LV} = 1.25 V	—	—	TBD	
		T_a = 125 °C [4] V_{DD_LV} = 1.25 V	—	—	160	
I_{DD_HALT}	HALT mode Operating current	T_a = 25 °C V_{DD_LV} = 1.25 V	—	—	TBD	mA
		T_a = 55 °C V_{DD_LV} = 1.25 V	—	—	TBD	
		T_a = 125 °C [4] V_{DD_LV} = 1.25 V	—	—	TBD	
$I_{DD_HV_ADC_REF}$[11, 12]	ADC REF Operating current	T_a = 25 °C 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF}$ = 3.6 V	—	200	400	µA
		T_a = 125 °C [4] 2 ADCs operating at 80 MHz $V_{DD_HV_ADC_REF}$ = 5.5 V	—	200	400	
$I_{DD_HV_ADCx}$[12]	ADC HV Operating current	T_a = 25 °C ADC operating at 80 MHz $V_{DD_HV_ADC}$ = 3.6 V	—	1	2	mA
		T_a = 125 °C [4] ADC operating at 80 MHz $V_{DD_HV_ADC}$ = 5.5 V	—	1.2	2	
$I_{DD_HV_FLASH}$	Flash Operating current during read access	T_a = 125 °C [4] 3.3 V supplies x MHz frequency	—	40	45	mA

1. The content of the Conditions column identifies the components that draw the specific current.
2. ALL Modules enabled at maximum frequency: 2 x e200Z4 @160 MHz, e200Z2 at 80 MHz, Platform @160MHz, DMA (SRAM to SRAM), all SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals (500 pll clock cycles), ENET0 transmitting, MLB transmitting, FlexRay transmitting, USB-SPH transmitting (USB-OTG only clocked), 2 x I2C transmitting (rest clocked), 1 x SAI transmitting (rest clocked), ADC0 converting using BCTU triggers triggered through PIT (other ADC clocked), RTC running, 3 x STM running, 2 x DSPI transmitting (rest clocked), 2 x SPI transmitting (rest clocked), 4 x CAN state machines working(rest clocked), 9 x LINFLEX transmitting (rest clocked), 1 x EMIOS clocked (used OPWFMB mode) (Others clock gated), SDHC,3 x CMP only clocked, FIRC, SIRC, FXOSC, SXOSC, PLL running. All others modules clock gated if not specifically mentioned. I/O supply current excluded.
3. Recommended Transistors:MJD31 @ 85°C, 105°C and 125°C.
4. Tj=150°C. Assumes Ta=125°C
   - Assumes maximum θJA. SeeThermal attributes
5. Enabled Modules in Gateway mode: 2 x e200Z4 @160 MHz (Instruction and Data cache enabled), Platform @160MHz, e200Z2 at 80 MHz(Instruction cache enabled), all SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), ENET0 transmitting, MLB

transmitting, FlexRay transmitting, USB-SPH Transmitting, USB-OTG clocked, 2 x I2C transmitting, (2 x I2C clock gated), 1 x SAI transmitting (2 x SAI clock gated), ADC0 converting in continuous mode (ADC1 clock gated), PIT clocked, RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(Other DSPS clock gated), 2 x SPI transmitting(Other SPIs clock gated), 4 x FlexCAN state machines clocked(other FLEXCAN clock gated), 4 x LINFLEX transmitting (Other clock gated), 1x EMIOS clocked(used OPWFMB mode) (Others clock gated), FIRC, SIRC, FXOSC, SXOSC, PLL running, BCTU, DMA_CH_MUX, ACMP clock gated. All others modules clock gated if not specifically mentioned. I/O supply current excluded

6. Recommended Transistors:MJD31@85°C, 105°C and 125°C.
7. Enabled Modules in Body mode enabled at maximum frequency: 2 x e200Z4 @120Mhz(Instruction and Data cache enabled),Platform@120MHz, SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT(ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(others DSPIs clocked), 2 x SPI transmitting(others clocked), 4 x FlexCAN state machines working(others clocked), 9xLINFLEX transmitting (others clocked), 1xEMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC,CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
8. Recommended Transistors:BCP56, BCP68 or MJD31@85°C, BCP56, BCP68 or MJD31@105°C and MJD31@125°C.
9. Enabled Modules in Body mode enabled at maximum frequency:2 x e200Z4 @80Mhz(Instruction and Data cache enabled),Platform@80MHz, SRAMs accessed in parallel, Flash access(prefetch is disabled while buffers are enabled), HSM reading from flash at regular intervals(500 pll clock cycles), DMA (SRAM to SRAM), ADC0 converting using BCTU triggers which are triggered through PIT(ADC1 clocked), RTC clocked, 3 x STM clocked, 2 x DSPI transmitting(others DSPIs clocked), 2 x SPI transmitting(others clocked), 4 x FlexCAN state machines working(others clocked), 9xLINFLEX transmitting (others clocked), 1xEMIOS operational (used OPWFMB mode) (others clocked), FIRC, SIRC, FXOSC, SXOSC, PLL running, MEMU, FCCU, SIUL, SDHC,CMP clocked, e200Z2, ENET, MLB, SAI, I2C, FlexRay, USB clock gated. All others modules clock gated if not specifically mentioned I/O supply current excluded
10. Recommended Transistors:BCP56, BCP68 or MJD31@85°C, 105°C and 125°C
11. Internal structures hold the input voltage less than $V_{DD_HV_ADC_REF}$ + 1.0 V on all pads powered by V_{DDA} supplies, if the maximum injection current specification is met (3 mA for all pins) and V_{DDA} is within the operating voltage specifications.
12. This value is the total current for two ADCs.Each ADC might consume upto 2mA at max.

Table 7. Low Power Unit (LPU) Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
LPU_RUN	with 256K RAM, but only one RAM being accessed	T_a = 25 °C SYS_CLK = 16MHz ADC0 = OFF, SPI0 = OFF, LIN0 = OFF, CAN0 = OFF	—	10		mA
		T_a = 125 °C SYS_CLK = 16MHz ADC0 = ON, SPI0 = ON, LIN0 = ON, CAN0 = ON	—		26	
LPU_STOP	with 256K RAM	T_a = 25 °C	—	0.15	—	mA
		T_a = 125 °C	—		10.6	

1. The content of the Conditions column identifies the components that draw the specific current.

Table 8. STANDBY Current consumption characteristics

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY0	STANDBY with 8K RAM	T_a = 25 °C	—	45	—	µA
		T_a = 125 °C	—		2400	
STANDBY1	STANDBY with 64K RAM	T_a = 25 °C	—	46.5	—	µA
		T_a = 125 °C	—		3000	
STANDBY2	STANDBY with 128K RAM	T_a = 25 °C	—	48.1	—	µA
		T_a = 125 °C	—		3700	

Table continues on the next page...

Table 8. STANDBY Current consumption characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
STANDBY3	STANDBY with 256K RAM	T_a = 25 °C	—	51.3	—	µA
		T_a = 125 °C	—		5100	

1. The content of the Conditions column identifies the components that draw the specific current.

2.7 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

NOTE

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 9. ESD ratings

Symbol	Parameter	Conditions[1]	Class	Max value[2]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	V

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.

2.8 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from Freescale on request.

3 I/O parameters

3.1 AC specifications @ 3.3 V Range

Table 10. Functional Pad AC Specifications @ 3.3 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	ipp_sre[1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		6/6		1.5/1.5	25	11
	2.5/2.5	7.5/7.5	0.9/0.9	3/3	50	
	6.4/5	19.5/19.5	3.5/2.5	12/12	200	
	2.2/2.5	8/8	0.6/0.8	3.5/3.5	25	10
	0.090	1.1	0.035	1.1	asymmetry[2]	
	2.9/3.5	11.5/11.5	1.8/1.2	6.5/6.5	50	
	11/8	35/31	7.7/5	25/21	200	
	8.3/9.6	45/45	4/3.5	25/25	50	01[3]
	13.5/15	65/65	6.3/6.2	30/30	200	
	13/13	75/75	6.8/6	40/40	50	00[3]
	21/22	100/100	11/11	51/51	200	
pad_i_hv/pad_sr_hv (input)[4]		2/2		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. This row specifies the min and max asymmetry between both the prop delay and the edge rates for a given PVT and 25pF load. Required for the Flexray spec.
3. Slew rate control modes
4. Input slope = 2ns

NOTE

Data based on characterization results, not tested in production.

3.2 DC electrical specifications @ 3.3V Range

Table 11. DC electrical specifications @ 3.3V Range

Symbol	Parameter	Value		Unit
		Min	Max	
dVdd[1]	LV (core) Supply Voltage	1.08	1.32	V
VDD_HV_x[1]	I/O Supply Voltage	2.97	3.63	V

Table continues on the next page...

Table 11. DC electrical specifications @ 3.3V Range (continued)

Symbol	Parameter	Value		Unit
		Min	Max	
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x	VDD_HV_x+ 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	dVss - 0.3	0.40 * VDD_HV_x	V
Vhys	CMOS Input Buffer Hysteresis	0.1 * VDD_HV_x		V
Pull_Ioh	Weak Pullup Current[2]	15	50	µA
Pull_Iol	Weak Pulldown Current[3]	15	50	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[4]	0.8 *VDD_HV_x	—	V
Vol	Output Low Voltage[5]	—	0.2 *VDD_HV_x	V
Ioh_f	Full drive Ioh[6] (ipp_sre[1:0] = 11)	18	70	mA
Iol_f	Full drive Iol[6] (ipp_sre[1:0] = 11)	21	120	mA
Ioh_h	Half drive Ioh[6] (ipp_sre[1:0] = 10)	9	35	mA
Iol_h	Half drive Iol[6] (ipp_sre[1:0] = 10)	10.5	60	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad = 0 V
3. Measured when pad = VDD_HV_x
4. Measured when pad is sourcing 2 mA
5. Measured when pad is sinking 2 mA
6. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

3.3 AC specifications @ 5 V Range

Table 12. Functional Pad AC Specifications @ 5 V Range

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	ipp_sre[1:0]
	Min	Max	Min	Max		MSB,LSB
pad_sr_hv (output)		4.5/4.5		1.2/1.2	25	11
		5.1/5.1		2/2	50	
		13/13		8/8	200	
		5.25/5.25		2/2	25	10
		8/8		4/4	50	
		22/22		16/16	200	
		27/27		12/12	50	01[2]
		40/40		24/24	200	
		40/40		24/24	50	00[2]
		65/65		50/50	200	

Table continues on the next page...

Table 12. Functional Pad AC Specifications @ 5 V Range (continued)

Symbol	Prop. Delay (ns)[1] L>H/H>L		Rise/Fall Edge (ns)		Drive Load (pF)	ipp_sre[1:0]
	Min	Max	Min	Max		MSB,LSB
pad_i_hv/pad_sr_hv (input)		1.5/1.5		0.5/0.5	0.5	NA

1. As measured from 50% of core side input to Voh/Vol of the output
2. Slew rate control modes

3.4 DC electrical specifications @ 5 V Range

Table 13. DC electrical specifications @ 5 V Range

Symbol	Parameter	Value		Unit
		Min	Max	
dVdd[1]	LV (core) Supply Voltage	1.08	1.32	V
VDD_HV_x[1]	I/O Supply Voltage	4.5	5.5	V
Vih	CMOS Input Buffer High Voltage (with hysteresis disabled)	0.55 * VDD_HV_x	VDD_HV_x + 0.3	V
Vil	CMOS Input Buffer Low Voltage (with hysteresis disabled)	dVss - 0.3	0.40 * VDD_HV_x	V
Vhys	CMOS Input Buffer Hysteresis	0.1 * VDD_HV_x		V
Pull_Ioh	Weak Pullup Current[2]	30	80	µA
Pull_Iol	Weak Pulldown Current[3]	30	80	µA
Iinact_d	Digital Pad Input Leakage Current (weak pull inactive)	-2.5	2.5	µA
Voh	Output High Voltage[4]	0.8 * VDD_HV_x	—	V
Vol	Output Low Voltage[5]	—	0.2 * VDD_HV_x	V
Ioh_f	Full drive Ioh[6] (ipp_sre[1:0] = 11)	38	132	mA
Iol_f	Full drive Iol[6] (ipp_sre[1:0] = 11)	48	220	mA
Ioh_h	Half drive Ioh[6] (ipp_sre[1:0] = 10)	19	66	mA
Iol_h	Half drive Iol[6] (ipp_sre[1:0] = 10)	24	110	mA

1. Max power supply ramp rate is 500 V / ms
2. Measured when pad = 0 V
3. Measured when pad = VDD_HV_x
4. Measured when pad is sourcing 2 mA
5. Measured when pad is sinking 2 mA
6. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

3.5 Functional reset pad electrical specifications

The device implements a dedicated bidirectional RESET pin.

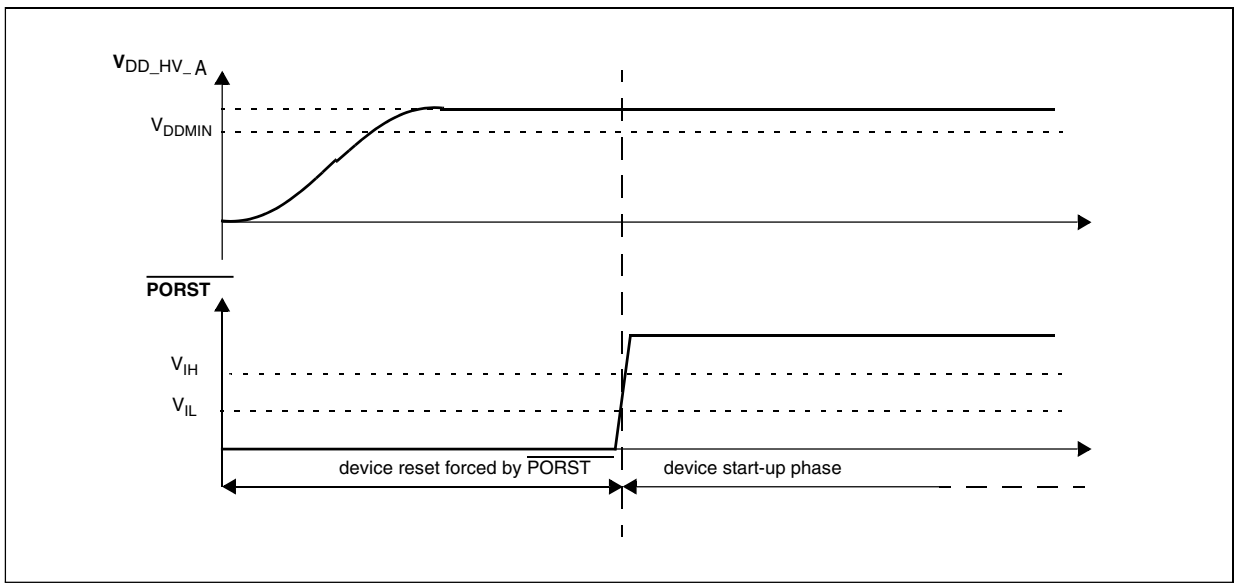


Figure 2. Start-up reset requirements

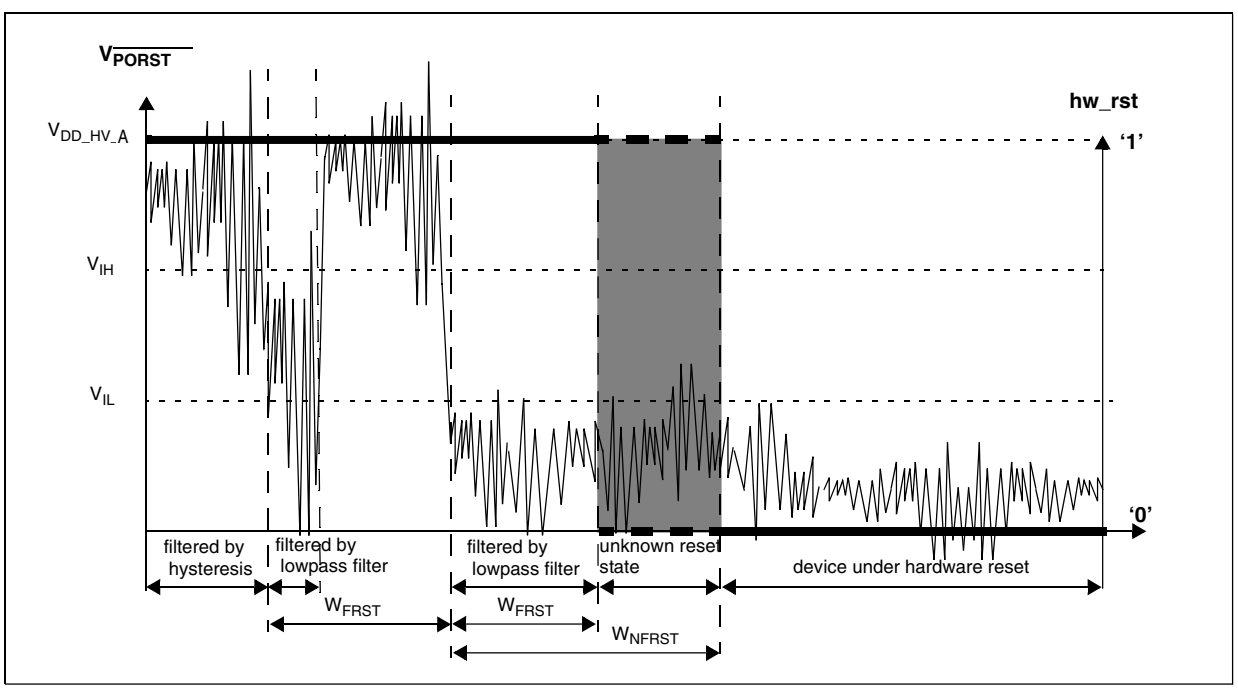


Figure 3. Noise filtering on reset signal

Table 14. Functional reset pad electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input high level TTL (Schmitt Trigger)	—	2.0	—	$V_{DD_HV_A}$ +0.4	V
V_{IL}	Input low level TTL (Schmitt Trigger)	—	–0.4	—	0.8	V
V_{HYS}	Input hysteresis TTL (Schmitt Trigger)	—	300	—	—	mV
V_{DD_POR}	Minimum supply for strong pull-down activation	—	—	—	1.2	V
I_{OL_R}	Strong pull-down current [1]	Device under power-on reset $V_{DD_HV_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD_HV_A}$	0.2	—	—	mA
		Device under power-on reset $V_{DD_HV_A}$= V_{DD_POR} V_{OL} = 0.35*$V_{DD_HV_IO}$	11	—	—	mA
W_{FRST}	$\overline{\text{RESET}}$ input filtered pulse	—	—	—	500	ns
W_{NFRST}	$\overline{\text{RESET}}$ input not filtered pulse	—	2000	—	—	ns
$\|I_{WPU}\|$	Weak pull-up current absolute value	RESET pin V_{IN} = V_{DD}	23	—	82	µA

1. Strong pull-down is active on PHASE0, PHASE1, PHASE2, and the beginning of PHASE3 for RESET.

3.6 PORST electrical specifications

Table 15. PORST electrical specifications

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
W_{FPORST}	$\overline{\text{PORST}}$ input filtered pulse	—	—	200	ns
$W_{NFPORST}$	$\overline{\text{PORST}}$ input not filtered pulse	500	—	—	ns
V_{IH}	Input high level	—	0.65 x $V_{DD_HV_A}$	—	ns
V_{IL}	Input low level	—	0.35 x $V_{DD_HV_A}$	—	ns

4 Peripheral operating requirements and behaviours

4.1 Analog

4.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

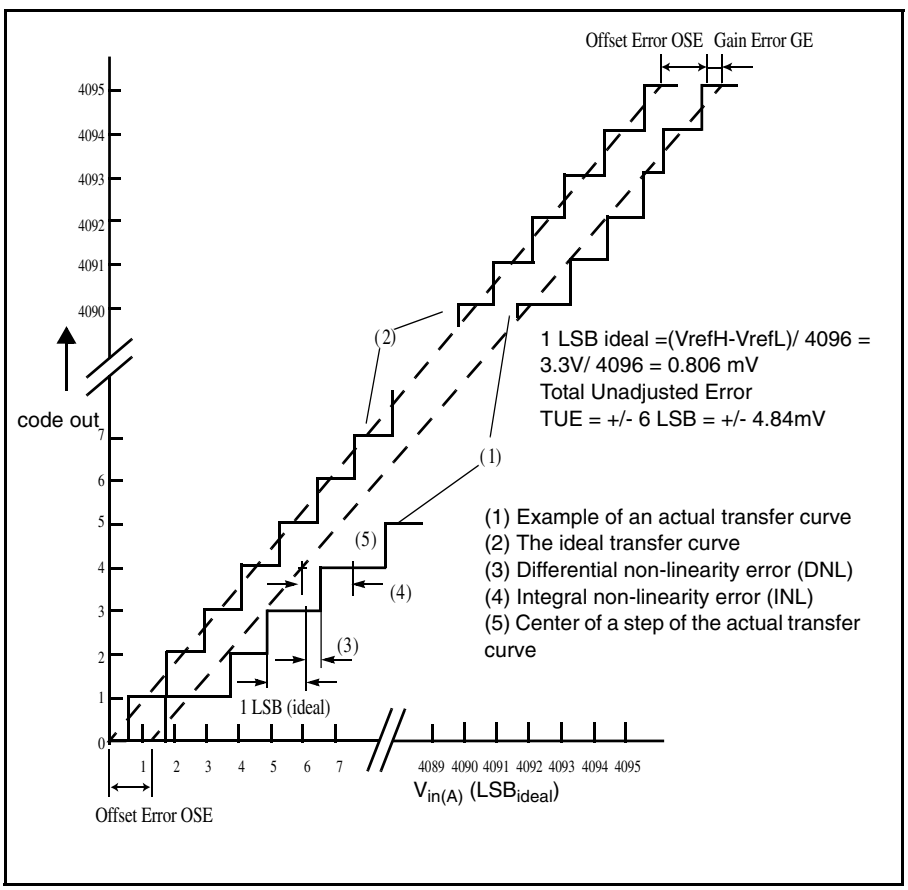


Figure 4. ADC characteristics and error definitions

4.1.1.1 Input impedance and ADC accuracy

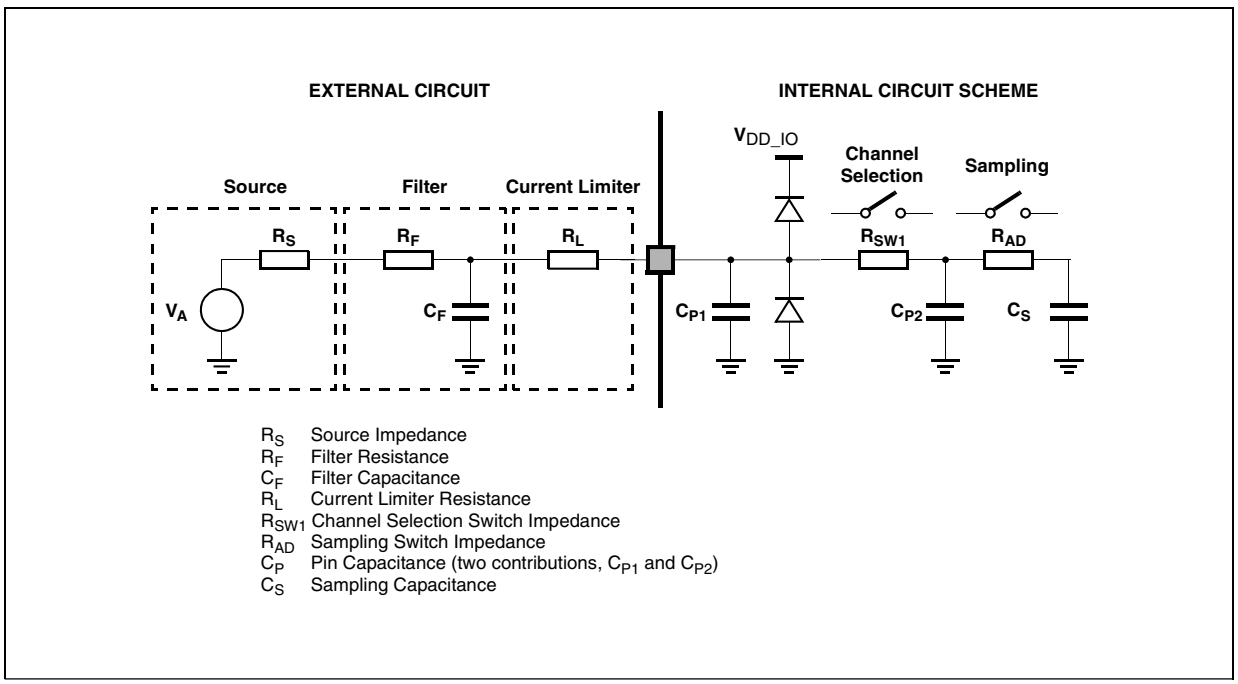


Figure 5. Input equivalent circuit

Table 16. ADC conversion characteristics (for 12-bit)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency)	—	15.2	80	80	MHz
f_s	Sampling frequency	80 MHz	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	275	800	—	ns
t_{conv}	Conversion time[4]	80 MHz	650	—	—	ns
t_{total_conv}	Total Conversion time t_{sample} + t_{conv} (for standard and extended channels)	80 MHz	1.5[5]	—	—	µs
	Total Conversion time t_{sample} + t_{conv} (for precision channels)		1	—	—	
C_S[6]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[6]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[6]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[6]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD}[6]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity	—	–1	—	1	LSB

Table continues on the next page...

Table 16. ADC conversion characteristics (for 12-bit) (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–4	—	4	LSB
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ	Without current injection	–6	+/-4	6	LSB
	STOP mode to Run mode recovery time				< 1	µs

1. Recomended operating range, unless otherwise specified and analog input voltage from $V_{SS_HV_ADC1}$ to $V_{SS_HV_ADC_REF}$.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. Apart from tsample and tconv, few cycles are used up in ADC digital interface and hence the overall throughput from the ADC is lower.
6. See Figure 5.

Table 17. ADC conversion characteristics (for 10-bit)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
f_{CK}	ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.)	—	15.2	80	80	MHz
f_s	Sampling frequency	—	—	—	1.00	MHz
t_{sample}	Sample time[3]	80 MHz@ 100 ohm source impedance	275	800	—	ns
t_{conv}	Conversion time[4]	80 MHz	550	—	—	ns
t_{total_conv}	Total Conversion time tsample + tconv (for standard channels)	80 MHz	1	—	—	µs
	Total Conversion time tsample + tconv (for extended channels)		1.5	—	—	
C_S[5]	ADC input sampling capacitance	—	—	3	5	pF
C_{P1}[5]	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}[5]	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}[5]	Internal resistance of analog source	V_{REF} range = 4.5 to 5.5 V	—	—	0.3	kΩ
		V_{REF} range = 3.15 to 3.6 V	—	—	875	Ω
R_{AD}[5]	Internal resistance of analog source	—	—	—	825	Ω
INL	Integral non-linearity	—	–2	—	2	LSB
DNL	Differential non-linearity[6]	—	–1	—	1	LSB
OFS	Offset error	—	–4	—	4	LSB
GNE	Gain error	—	–4	—	4	LSB

Table continues on the next page...

Table 17. ADC conversion characteristics (for 10-bit) (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
ADC Analog Pad (pad going to one ADC)	Max leakage	150 °C	—	—	250	nA
	Max positive/negative injection		–5	—	5	mA
$TUE_{IS1WINJ}$	Total unadjusted error for IS1WINJ	Without current injection	–4	+/-3	4	LSB
	STOP mode to Run mode recovery time				< 1	µs

1. V_{DD} = 3.3 V -5.5, T_J = –40 to +150 °C, unless otherwise specified and analog input voltage from $V_{SS_HV_ADC0}$ to $V_{DD_HV_ADC0}$.
2. The internally generated clock (known as AD_clk or ADCK) could be same as the peripheral clock or half of the peripheral clock based on register configuration in the ADC.
3. During the sample time the input capacitance C_S can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming.
4. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 5
6. No missing codes.

Table 18. ADC supply configurations

	VALID CASE 1	VALID CASE 2	VALID CASE 3	VALID CASE 4
VDD_HV_ADC1	5V	5V	3.3V	3.3V
VDD_HV_ADC1_REF	3.3V	5V	3.3V	5V
ADC1 input pin range	0V to IO segment supply voltage where that input pin resides	0 to IO segment supply voltage where that input pin resides	0 to IO segment supply voltage where that input pin resides	0 to IO segment supply voltage where that input pin resides
ADC1 result	Valid up to 3.3V, then full-scale reached	Valid up to 5V	Valid up to 3.3V, then full-scale reached	Valid up to 5V

NOTE

The ADC input pins sit across all three I/O segments, VDD_HV_A, VDD_HV_B and VDD_HV_C.

4.1.2 Analogue Comparator (CMP) electrical specifications

Table 19. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	250	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	5	10	µA
V_{AIN}	Analog input voltage	V_{SS}	—	$V_{IN1_CMP_REF}$	V
V_{AIO}	Analog input offset voltage	-20	—	20	mV

Table continues on the next page...

Table 19. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 0	—	0	—	mV
	• CR0[HYSTCTR] = 10	—	10	—	mV
	• CR0[HYSTCTR] = 20	—	20	—	mV
	• CR0[HYSTCTR] = 30	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD_HV_A}$ – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation Delay, High Speed Mode (+/-100mV)	—	50	—	ns
	Propagation Delay, High Speed Mode (+/-20mV)	—	120	—	ns
	Analog comparator initialization delay, High Speed Mode[2]	—	4		µs
	Analog comparator initialization delay, Low Power Mode	—	100		µs
I_{DAC6b}	6-bit DAC current adder (when enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to $V_{DD_HV_A}$-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

4.2 Clocks and PLL interfaces modules

4.2.1 Main oscillator electrical characteristics

This device provides a driver for oscillator in pierce configuration with amplitude control. Controlling the amplitude allows a more sinusoidal oscillation, reducing in this way the EMI. Other benefits arises by reducing the power consumption. This Loop Controlled Pierce (LCP mode) requires good practices to reduce the stray capacitance of traces between crystal and MCU.

An operation in Full Swing Pierce (FSP mode), implemented by an inverter is also available in case of parasitic capacitances and cannot be reduced by using crystal with high equivalent series resistance. For this mode, a special care needs to be taken regarding the serial resistance used to avoid the crystal overdrive.

Other two modes called External (EXT Wave) and disable (OFF mode) are provided. For EXT Wave, the drive is disabled and an external source of clock within CMOS level based in analog oscillator supply can be used. When OFF, EXTAL is pulled down by 240 Kohms resistor and the feedback resistor remains active connecting XTAL through EXTAL by 1M resistor.

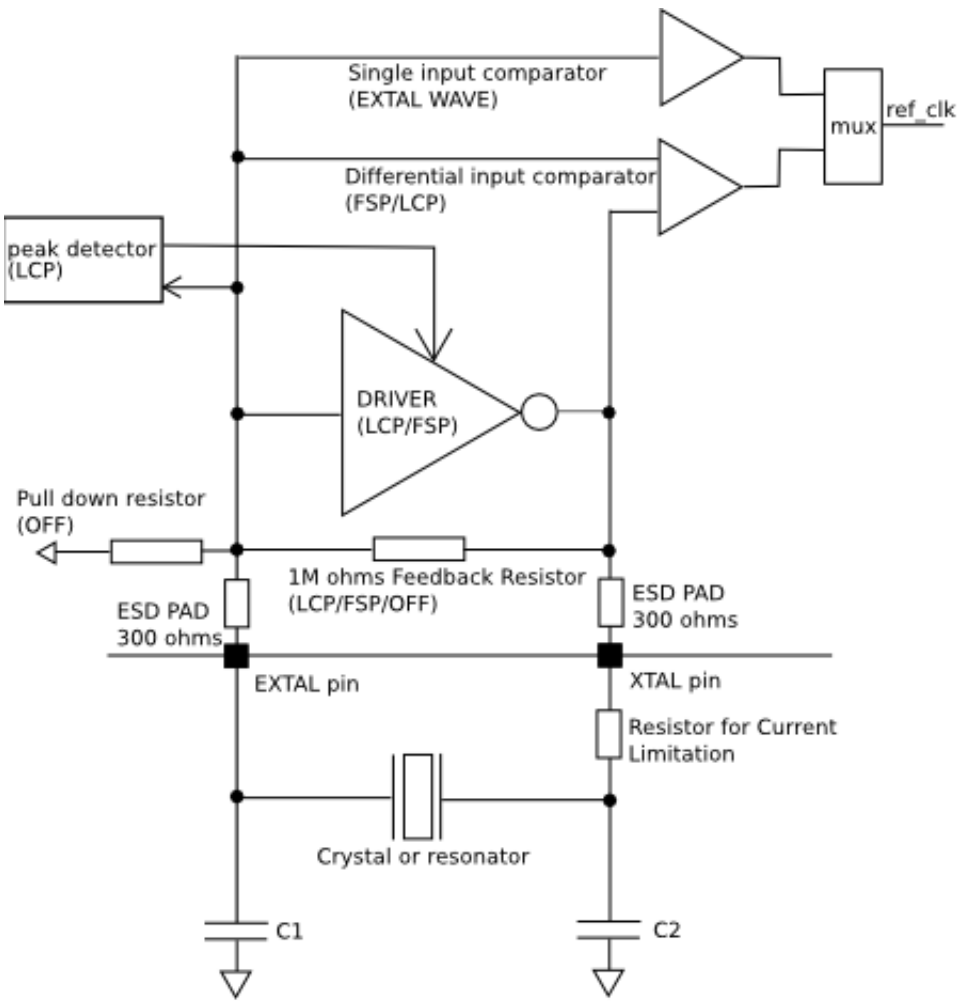


Figure 6. Oscillator connections scheme

Table 20. Main oscillator electrical characteristics

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
f_{XOSCHS}	Oscillator frequency	FSP/LCP		4		40	MHz
$g_{mXOSCHS}$	Driver Transconductance	FSP/LCP	1		23		mA/V

Table continues on the next page...

Table 20. Main oscillator electrical characteristics (continued)

Symbol	Parameter	Mode	Conditions	Min	Typ	Max	Unit
V_{XOSCHS}	Oscillation Amplitude	LCP[1, 2]	4 MHz		1.0		V_{PP}
			8 MHz		1.0		
			16 MHz		1.0		
			40 MHz		0.8		
$T_{XOSCHSSU}$	Startup time	FSP/LCP[3]	4-40 MHz		1		ms
	Supply current	FSP	8 MHz		2.2		mA
			16 MHz		2.2		
			40 MHz		3.2		
		LCP	8 MHz		141		uA
			16 MHz		252		
			40 MHz		518		
V_{IH}	Input High level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3	1.25	1.45		V
V_{IL}	Input low level CMOS Schmitt trigger	EXT Wave	Oscillator supply=3.3			1.95	V

1. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board.
2. Typ value for oscillator supply 3.3 V@27 °C
3. Values are very dependent on crystal or resonator used and parasitic capacitance observed in the board

4.2.2 32 kHz Oscillator electrical specifications

Table 21. 32 kHz oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{osc_lo}	Oscillator crystal or resonator frequency		32		40	KHz
t_{cst}	Crystal Start-up Time[1, 2]				2	s

1. This parameter is characterized before qualification rather than 100% tested.
2. Proper PC board layout procedures must be followed to achieve specifications.

4.2.3 16 MHz RC Oscillator electrical specifications

Table 22. 16 MHz RC Oscillator electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	IRC target frequency	—	—	16	—	MHz

Table continues on the next page...

Table 22. 16 MHz RC Oscillator electrical specifications (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$F_{Untrimmed}$	IRC frequency (untrimmed)	—	10.16	—	22.02	MHz
PTA	IRC frequency variation after trimming	—	-5	—	5	%
$T_{startup}$	Startup time	—		—	1	us
T_{STJIT}	Cycle to cycle jitter		—	—	1.5	%
T_{LTJIT}	Long term jitter		—	—	0.02	%
I_{VDDHV}	Current consumption on 3.3 V power supply	After $T_{startup}$	—	—	75	µA
I_{VDDLV}	Current consumption on 1.2 V power supply	After $T_{startup}$	—	—	25	µA

NOTE

The above start up time of 1 us is equivalent to 16 cycles of 16 MHz.

4.2.4 128 KHz Internal RC oscillator Electrical specifications

Table 23. 128 KHz Internal RC oscillator electrical specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_{oscu}[1]	Oscillator frequency	Uncalibrated	96	128	200	KHz
Fosc[1]		Calibrated	122	128	134	KHz
	Temperature dependence				270	ppm/C
	Supply dependence				10	%/V
	Supply current	Clock running			2.75	µA
		Clock stopped			200	nA

1. Vdd=1.2 V, 1.32V, T_a=-40 C, 125 C

4.2.5 PLL electrical specifications

Table 24. PLL electrical specifications

Parameter	Min	Typ	Max	Unit	Comments
Input Frequency	8		40	MHz	
Input Clock Low Level	0	0	0		Square wave clock
Input Clock High Level	1.08	1.2	1.32	V	Square wave clock
VCO Frequency Range	600		1280	MHz	

Table continues on the next page...

Table 24. PLL electrical specifications (continued)

Parameter	Min	Typ	Max	Unit	Comments
Duty Cycle at pllclkout	48%	(N+1)/ (2xN)	52%		with even division at output with odd division(N) at output
Regulator Maximum Output Current	0.75			mA	
Analog Supply	1.08	1.2	1.32		
Digital Supply (V_{DD_LV})	1.08	1.2	1.32		
Period Jitter			See Table 25	ps	NON SSCG mode
TIE			See Table 25		at 960 M Integrated over 1MHz offset not valid in SSCG mode
Modulation Depth (Center Spread)	+/- 0.25%		+/- 4.0%		
Modulation Depth (Down Spread)	+/- 0.5%		+/- 8.0%		
Modulation Frequency			32	KHz	
Lock Time	20		60	µs	Calibration mode
	10		30	µs	Calibration bypass mode (wake-up mode)
PLL reset assertion time			5	µs	
Power Consumption			1 mA (avdd) 0.5 mA (dvdd)		at 1280 MHz VCO clock T_A=25°C

Table 25. Jitter calculation

Type of jitter	Jitter due to Supply Noise (ps) J_{SN} [1]	Jitter due to Fractional Mode (ps) J_{SDM} [2]	Jitter due to Fractional Mode J_{SSCG} (ps) [3]	1 Sigma Random Jitter J_{RJ} (ps) [4]	Total Period Jitter (ps)
Period Jitter	60 ps	3% of pllclkout1,2	Modulation depth	0.1% of pllclkout1,2	$+/-(J_{SN}+J_{SDM}+J_{SSCG}+N^{[4]} \times J_{RJ}$
Long Term Jitter (Integer Mode)					N x J_{RJ}
Long Term jitter (Fractional Mode)					N x J_{RJ}

1. This jitter component is due to self noise generated due to bond wire inductances on different PLL supplies. The jitter value is valid for inductor value of 5nH or less each on avdd, avss, dvdd, dvss.
2. This jitter component is added when the PLL is working in the fractional mode.
3. This jitter component is added when the PLL is working in the Spread Spectrum Mode. Else it is 0.
4. The value of N is dependent on the accuracy requirement of the application. See Table 26.

Table 26. Percentage of sample exceeding specified value of jitter

N	Percentage of samples exceeding specified value of jitter (%)
1	31.73
2	4.55
3	0.27

Table continues on the next page...

Table 26. Percentage of sample exceeding specified value of jitter (continued)

N	Percentage of samples exceeding specified value of jitter (%)
4	6.30 × 1e-03
5	5.63 × 1e-05
6	2.00 × 1e-07
7	2.82 × 1e-10

4.3 Memory interfaces

4.3.1 Flash memory program and erase specifications

NOTE

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within an SoC, and represent average currents for given supplies and operations.

Table 27 shows the estimated Program/Erase times.

Table 27. Flash memory program and erase specifications

Symbol	Characteristic[1]	Typ[2]	Factory Programming[3, 4]		Field Update			Unit
			Initial Max	Initial Max, Full Temp	Typical End of Life[5]	Lifetime Max[6]		
			$20°C \le T_A \le 30°C$	$-40°C \le T_J \le 150°C$	$-40°C \le T_J \le 150°C$	≤ 1,000 cycles	≤ 250,000 cycles	
t_{dwpgm}	Doubleword (64 bits) program time	43	100	150	55	500		µs
t_{ppgm}	Page (256 bits) program time	73	200	300	108	500		µs
t_{qppgn}	Quad-page (1024 bits) program time	268	800	1,200	396	2,000		µs
t_{16kers}	16 KB Block erase time	168	290	320	250	1,000		ms
t_{16kpgn}	16 KB Block program time	34	45	50	40	1,000		ms
t_{32kers}	32 KB Block erase time	217	360	390	310	1,200		ms
t_{32kpgm}	32 KB Block program time	69	100	110	90	1,200		ms
t_{64kers}	64 KB Block erase time	315	490	590	420	1,600		ms
t_{64kpgm}	64 KB Block program time	138	180	210	170	1,600		ms
$t_{256kers}$	256 KB Block erase time	884	1,520	2,030	1,080	4,000	—	ms
$t_{256kpgm}$	256 KB Block program time	552	720	880	650	4,000	—	ms

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ T_J ≤ 150°C, full spec voltage.

4.3.2 Flash memory Array Integrity and Margin Read specifications

Table 28. Flash memory Array Integrity and Margin Read specifications

Symbol	Characteristic	Min	Typical	Max[1, 1]	Units [2, 2]
$t_{ai16kseq}$	Array Integrity time for sequential sequence on 16KB block.	—	—	512 x Tperiod x Nread	—
$t_{ai32kseq}$	Array Integrity time for sequential sequence on 32KB block.	—	—	1024 x Tperiod x Nread	—
$t_{ai64kseq}$	Array Integrity time for sequential sequence on 64KB block.	—	—	2048 x Tperiod x Nread	—
tai256kseq	Array Integrity time for sequential sequence on 256KB block.	—	—	8192 x Tperiod x Nread	—
$t_{mr16kseq}$	Margin Read time for sequential sequence on 16KB block.	73.81	—	110.7	µs
$t_{mr32kseq}$	Margin Read time for sequential sequence on 32KB block.	128.43	—	192.6	µs
$t_{mr64kseq}$	Margin Read time for sequential sequence on 64KB block.	237.65	—	356.5	µs
$t_{mr256kseq}$	Margin Read time for sequential sequence on 256KB block.	893.01	—	1,339.5	µs

1. Array Integrity times need to be calculated and is dependant on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

4.3.3 Flash memory module life specifications

Table 29. Flash memory module life specifications

Symbol	Characteristic	Conditions	Min	Typical	Units
Array P/E cycles	Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1, 1]	—	250,000	—	P/E cycles
	Number of program/erase cycles per block for 256 KB blocks.[2, 2]	—	1,000	250,000	P/E cycles

Table continues on the next page...

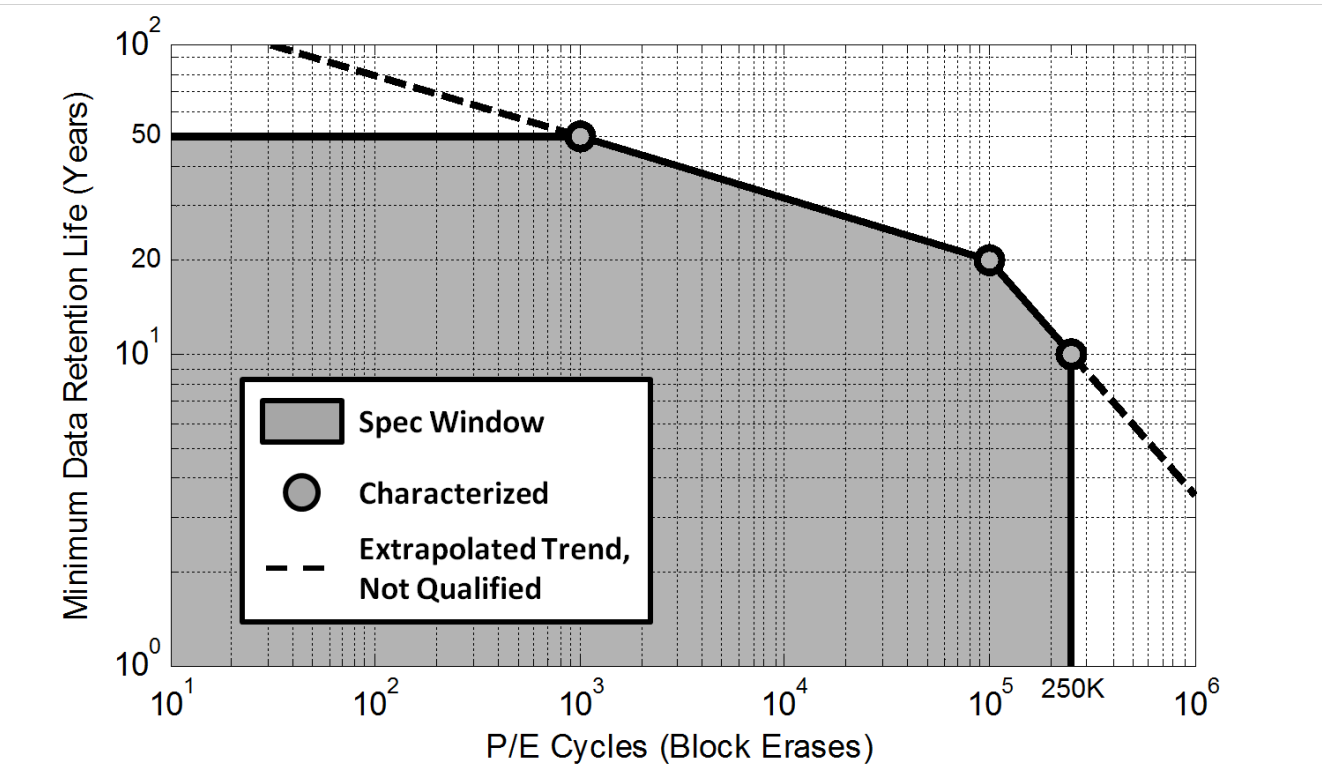
Table 29. Flash memory module life specifications (continued)

Symbol	Characteristic	Conditions	Min	Typical	Units
Data retention	Minimum data retention.	Blocks with 0 - 1,000 P/E cycles.	50	—	Years
		Blocks with 100,000 P/E cycles.	20	—	Years
		Blocks with 250,000 P/E cycles.	10	—	Years

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

4.3.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.



4.3.5 Flash memory AC timing specifications

Table 30. Flash memory AC timing specifications

Symbol	Characteristic	Min	Typical	Max	Units
t_{psus}	Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1.	—	7 plus four system clock periods	9.1 plus four system clock periods	µs
t_{esus}	Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{res}	Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low.	—	—	100	ns
t_{done}	Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared.	—	—	5	ns
t_{dones}	Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1.	—	16 plus four system clock periods	20.8 plus four system clock periods	µs
t_{drcv}	Time to recover once exiting low power mode.	16 plus seven system clock periods.	—	45 plus seven system clock periods	µs
$t_{aistart}$	Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP	—	—	5	ns
t_{aistop}	Time from 1 to 0 transition of UTO-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request.	—	—	80 plus fifteen system clock periods	ns
t_{mrstop}	Time from 1 to 0 transition of UTO-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request.	10.36 plus four system clock periods	—	20.42 plus four system clock periods	µs

4.3.6 Flash read wait state and address pipeline control settings

The following table describes the recommended RWSC and APC settings at various operating frequencies based on specified intrinsic flash access times of the flash module controller array at 125 °C.

Table 31. Flash Read Wait State and Address Pipeline Control Guidelines

Operating frequency (f_{sys})[1]	RWSC	APC	Flash read latency on mini-cache miss (# of f_{sys} clock periods)	Flash read latency on mini-cache hit (# of f_{sys} clock periods)
40 MHz	1	0,1	3	1
80 MHz	2	0,1	5	1
120 MHz	3	0,1	6	1
160 MHz	4	0,1	7	1

1. Packaged parts (-40 to 150ºC)

4.4 Communication interfaces

4.4.1 DSPI timing

Table 32. DSPI electrical specifications

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
1	t_{SCK}	DSPI cycle time	Master (MTFE = 0)	25	—	50	—	ns
			Slave (MTFE = 0)	40	—	60	—	
2	t_{CSC}	PCS to SCK delay	—	16	—	—	—	ns
3	t_{ASC}	After SCK delay	—	16	—	—	—	ns
4	t_{SDC}	SCK duty cycle	—	$t_{SCK}/2$ - 10	$t_{SCK}/2$ + 10	—	—	ns
5	t_A	Slave access time	$\overline{SS}$ active to SOUT valid	—	40	—	—	ns
6	t_{DIS}	Slave SOUT disable time	$_{SS}$ inactive to SOUT High-Z or invalid	—	10	—	—	ns
7	t_{PCSC}	PCSx to $\overline{PCSS}$ time	—	13	—	—	—	ns
8	t_{PASC}	$\overline{PCSS}$ to PCSx time	—	13	—	—	—	ns

Table continues on the next page...

Table 32. DSPI electrical specifications (continued)

No	Symbol	Parameter	Conditions	High Speed Mode		low Speed mode		Unit
				Min	Max	Min	Max	
9	t_{SUI}	Data setup time for inputs	Master (MTFE = 0)	NA	—	20	—	ns
			Slave	2	—	2	—	
			Master (MTFE = 1, CPHA = 0)	15	—	8[1, 1]	—	
			Master (MTFE = 1, CPHA = 1)	15	—	20	—	
10	t_{HI}	Data hold time for inputs	Master (MTFE = 0)	NA	—	–5	—	ns
			Slave	4	—	4	—	
			Master (MTFE = 1, CPHA = 0)	0	—	11[1]	—	
			Master (MTFE = 1, CPHA = 1)	0	—	-5	—	
11	t_{SUO}	Data valid (after SCK edge)	Master (MTFE = 0)	—	NA	—	4	ns
			Slave	—	15	—	23	
			Master (MTFE = 1, CPHA = 0)	—	4	—	16[1]	
			Master (MTFE = 1, CPHA = 1)	—	4	—	4	
12	t_{HO}	Data hold time for outputs	Master (MTFE = 0)	NA	—	–2	—	ns
			Slave	4	—	6	—	
			Master (MTFE = 1, CPHA = 0)	-2	—	10[1]	—	
			Master (MTFE = 1, CPHA = 1)	–2	—	–2	—	

1. SMPL_PTR should be set to 1

NOTE

Restriction For High Speed modes

- DSPI2, DSPI3, SPI1 and SPI2 will support 40MHz Master mode SCK
- DSPI2, DSPI3, SPI1 and SPI2 will support 25MHz Slave SCK frequency
- Only one {SIN,SOUT and SCK} group per DSPI/SPI will support high frequency mode
- For Master mode MTFE will be 1 for high speed mode
- For high speed slaves, their master have to be in MTFE=1 mode or should be able to support 15ns tSUO delay

NOTE

For numbers shown in the following figures, see Table 32

Table 33. Continuous SCK timing

Spec	Characteristics	Pad Drive/Load	Value	
			Minimum	Maximum
tSCK	SCK cycle timing	strong/50pf	100ns	
	PCS valid after SCK	strong/50pf		15ns
	PCS valid after SCK	strong/50pf	-4ns	

Table 34. DSPI high speed mode I/Os

DSPI	High speed SCK	High speed SIN	High speed SOUT
DSPI2	GPIO[78]	GPIO[76]	GPIO[77]
DSPI3	GPIO[100]	GPIO[101]	GPIO[98]
SPI1	GPIO[173]	GPIO[175]	GPIO[176]
SPI2	GPIO[79]	GPIO[110]	GPIO[111]

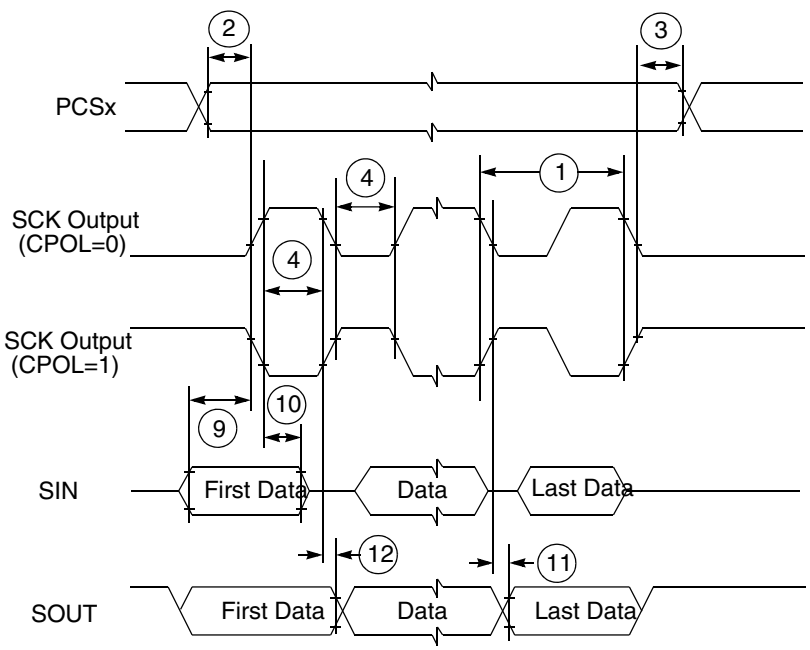


Figure 7. DSPI classic SPI timing — master, CPHA = 0

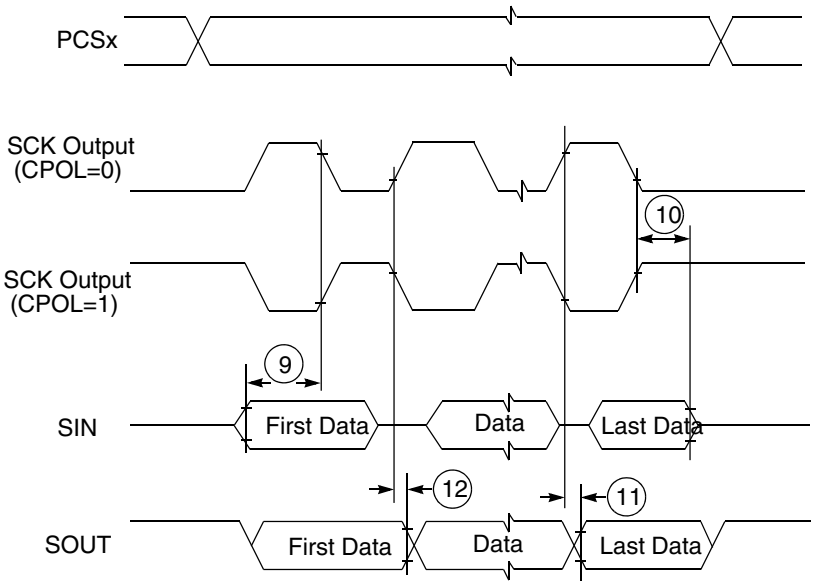


Figure 8. DSPI classic SPI timing — master, CPHA = 1

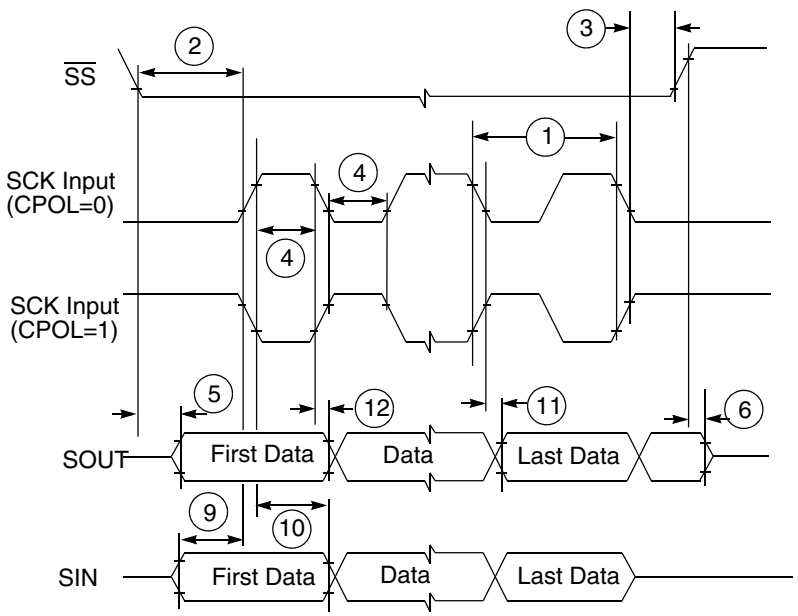


Figure 9. DSPI classic SPI timing — slave, CPHA = 0

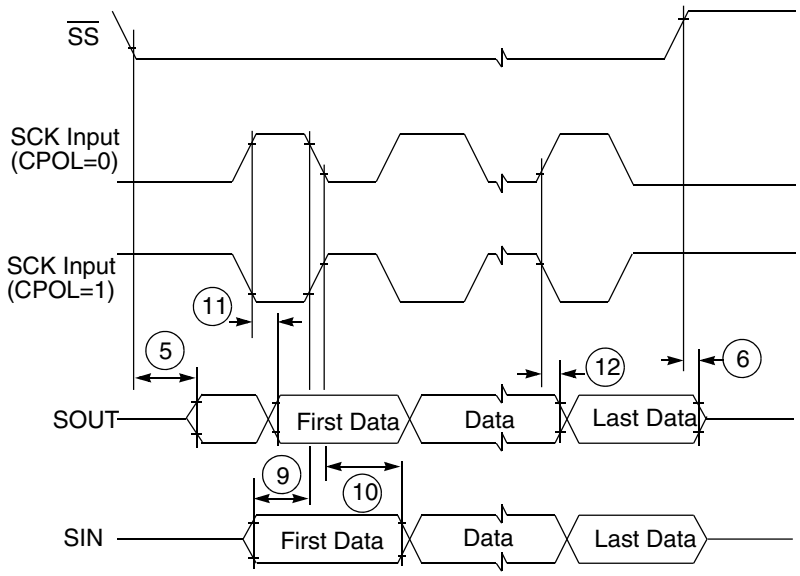


Figure 10. DSPI classic SPI timing — slave, CPHA = 1

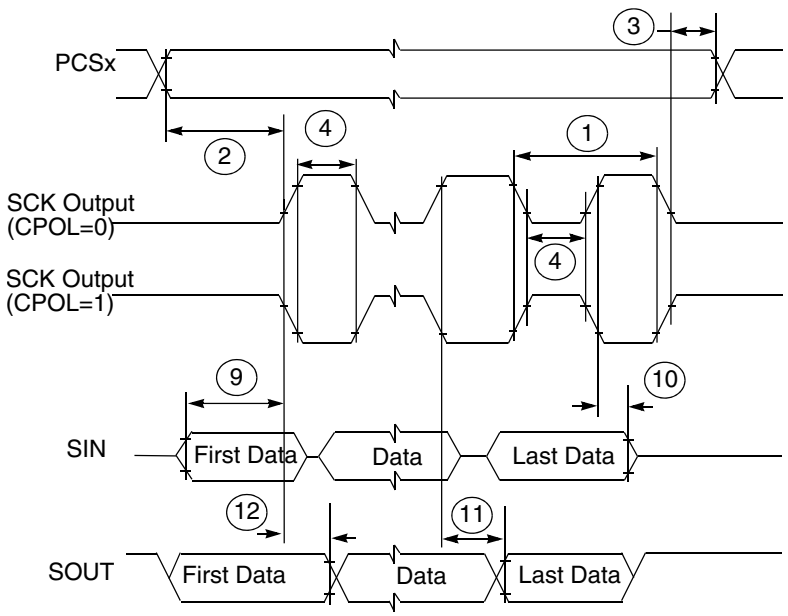


Figure 11. DSPI modified transfer format timing — master, CPHA = 0

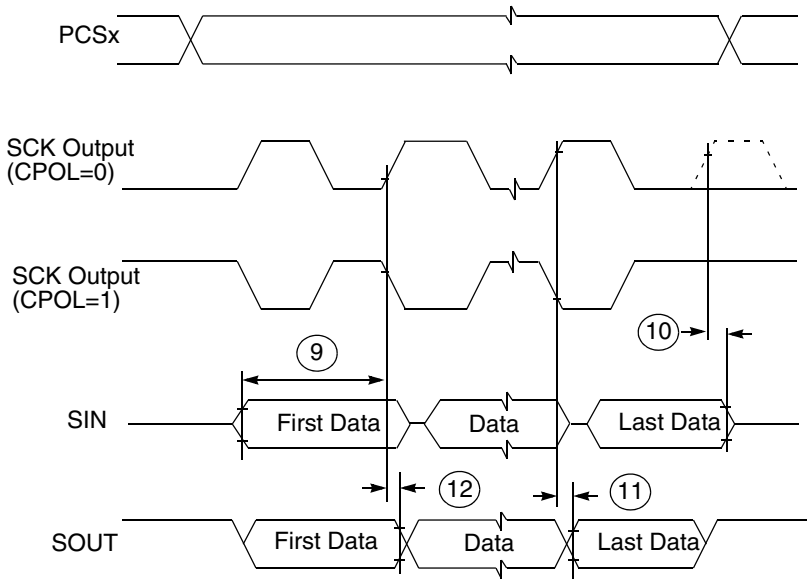


Figure 12. DSPI modified transfer format timing — master, CPHA = 1

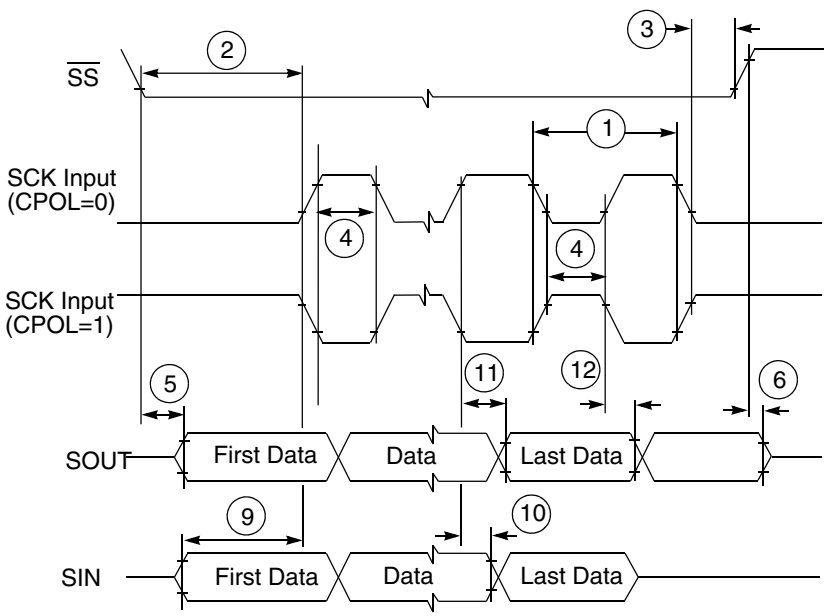


Figure 13. DSPI modified transfer format timing – slave, CPHA = 0

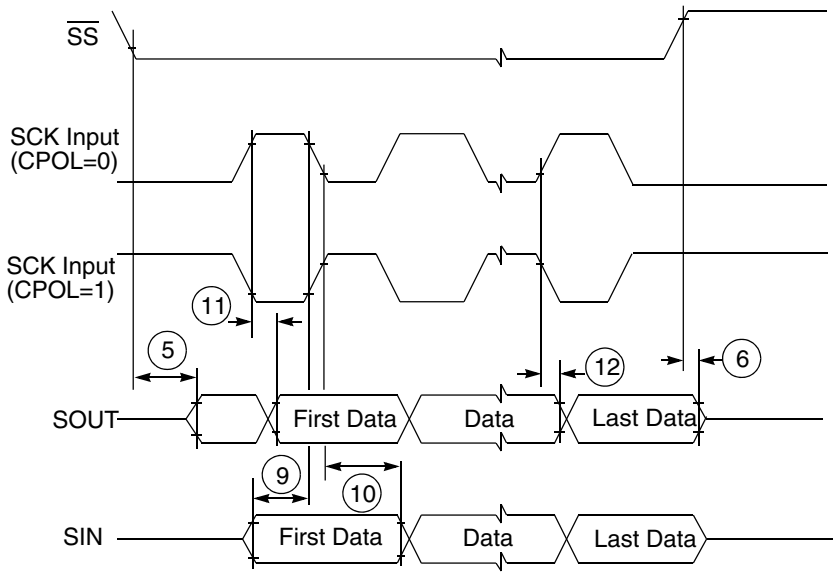


Figure 14. DSPI modified transfer format timing — slave, CPHA = 1

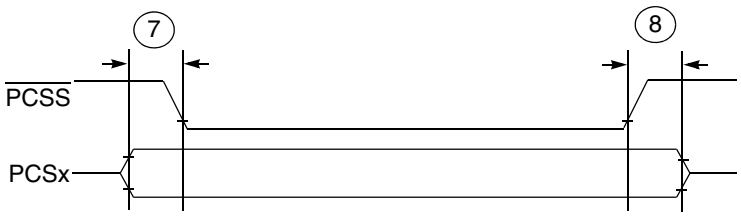


Figure 15. DSPI PCS strobe (PCSS) timing

4.4.2 FlexRay electrical specifications

4.4.2.1 FlexRay timing

This section provides the FlexRay Interface timing characteristics for the input and output signals. It should be noted that these are recommended numbers as per the FlexRay EPL v3.0 specification, and subject to change per the final timing analysis of the device.

4.4.2.2 TxEN

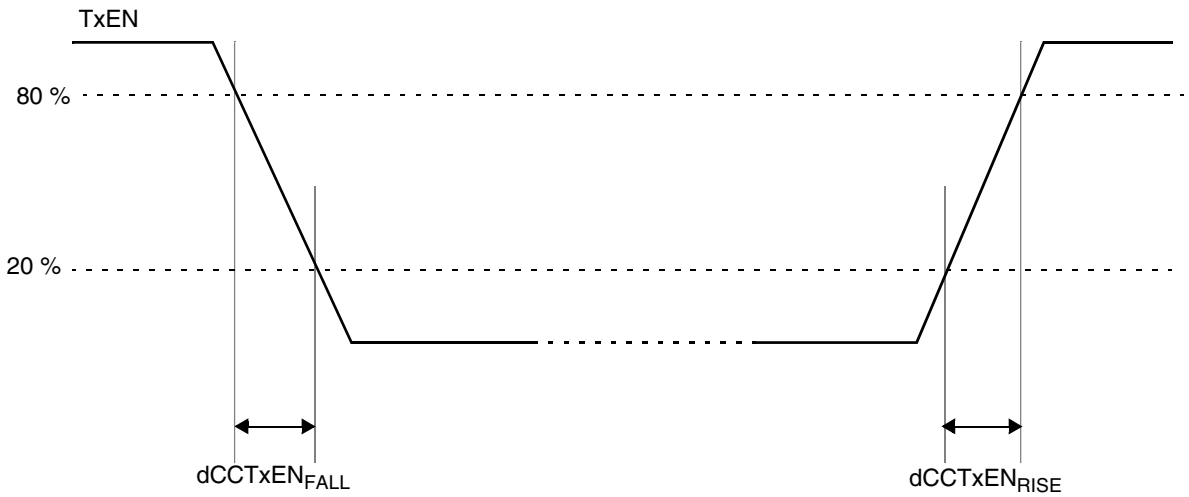


Figure 16. TxEN signal

Table 35. TxEN output characteristics[1]

Name	Description	Min	Max	Unit
$dCCTxEN_{RISE25}$	Rise time of TxEN signal at CC		9	ns
$dCCTxEN_{FALL25}$	Fall time of TxEN signal at CC		9	ns
$dCCTxEN_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge		25	ns
$dCCTxEN_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge		25	ns

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxEN pin load maximum 25 pF

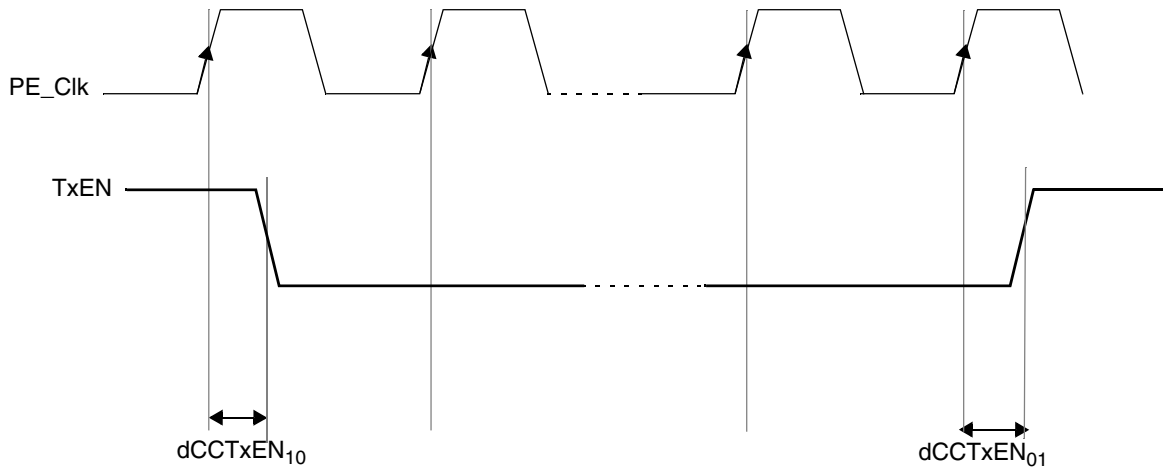


Figure 17. TxEN signal propagation delays

4.4.2.3 TxD

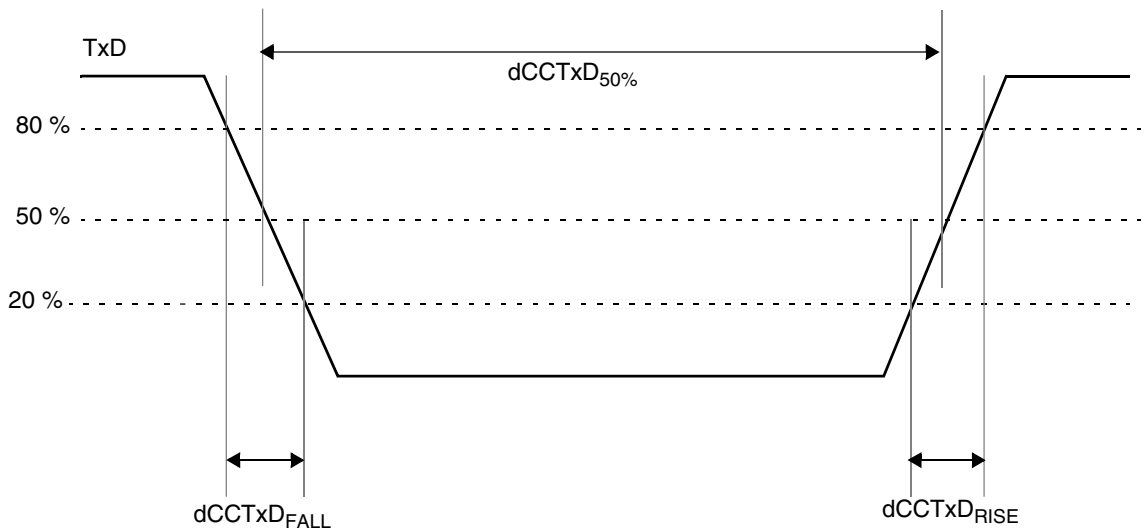


Figure 18. TxD Signal

Table 36. TxD output characteristics

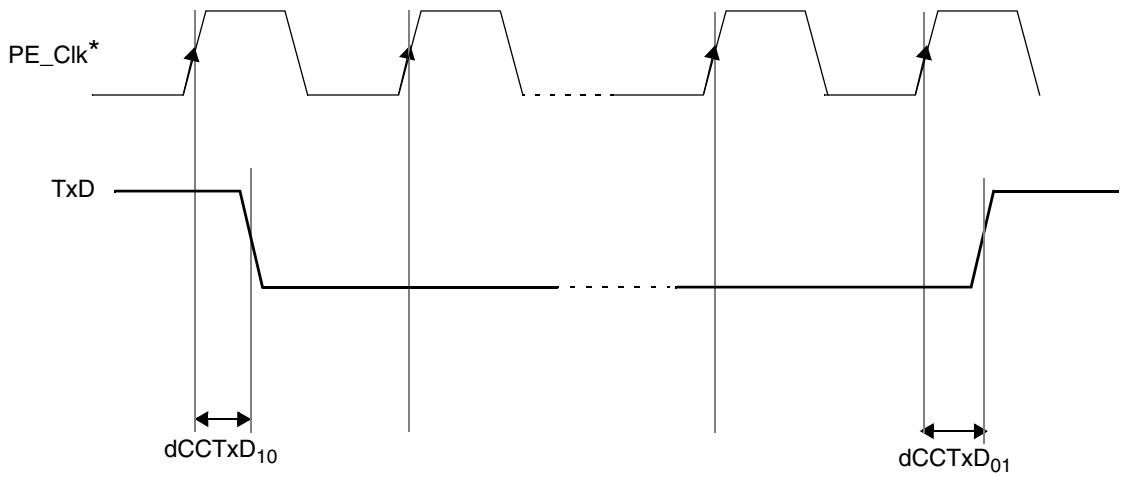
Name	Description[1]	Min	Max	Unit
$dCCT_{xAsym}$	Asymmetry of sending CC @ 25 pF load (=dCCTxD50% - 100 ns)	–2.45	2.45	ns
$dCCTxD_{RISE25}$+$dCCTxD_{FALL25}$	Sum of Rise and Fall time of TxD signal at the output		9[2]	ns

Table continues on the next page...

Table 36. TxD output characteristics (continued)

Name	Description[1]	Min	Max	Unit
$dCCTxD_{01}$	Sum of delay between Clk to Q of the last FF and the final output buffer, rising edge		25	ns
$dCCTxD_{10}$	Sum of delay between Clk to Q of the last FF and the final output buffer, falling edge		25	ns

1. All parameters specified for $V_{DD_HV_IOx}$ = 3.3 V -5%, +±10%, TJ = –40 °C / 150 °C, TxD pin load maximum 25 pF.
2. For 3.3 V ± 10% operation, this specification is 10 ns.



*FlexRay Protocol Engine Clock

Figure 19. TxD Signal propagation delays

4.4.2.4 RxD

Table 37. RxD input characteristic

Name	Description[1]	Min	Max	Unit
C_CCRxD	Input capacitance on RxD pin		7	pF
uCCLogic_1	Threshold for detecting logic high	35	70	%
uCCLogic_0	Threshold for detecting logic low	30	65	%
$dCCRxD_{01}$	Sum of delay from actual input to the D input of the first FF, rising edge		10	ns
$dCCRxD_{10}$	Sum of delay from actual input to the D input of the first FF, falling edge		10	ns

1. All parameters specified for VDD_HV_IOx = 3.3 V -5%, +±10%, TJ = –40 oC / 150 oC.

4.4.3 uSDHC specifications

Table 38. uSDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
	Card input clock				
SD1	fpp	Clock frequency (Identification mode)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed)	0	25	MHz
	fpp	Clock frequency (SD\SDIO high speed)	0	40	MHz
	fpp	Clock frequency (MMC full speed)	0	20	MHz
	f_{OD}	Clock frequency (MMC full speed)	0	40	MHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	6.5	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

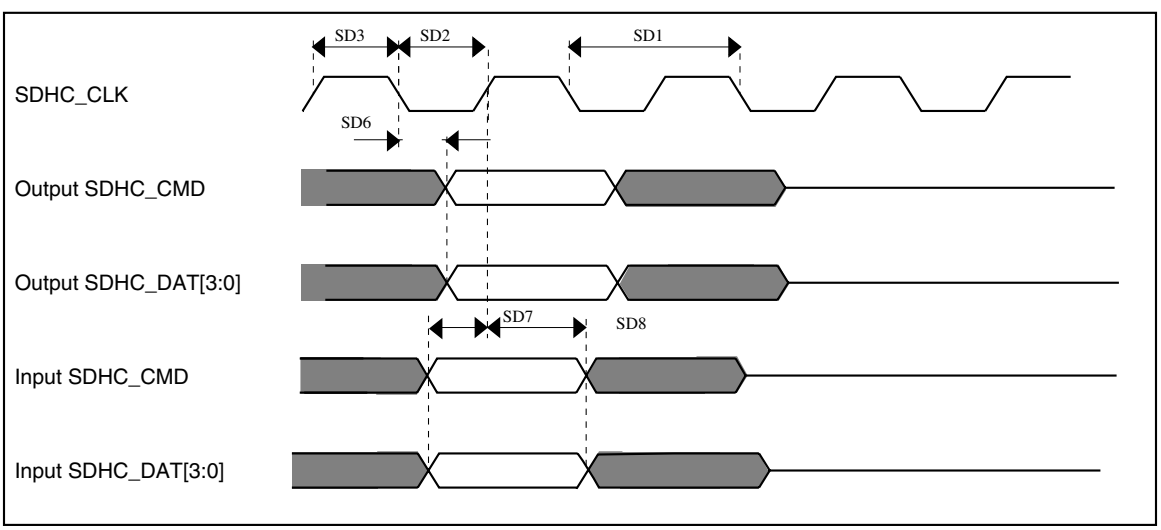


Figure 20. uSDHC timing

4.4.4 Ethernet switching specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

4.4.4.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Table 39. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

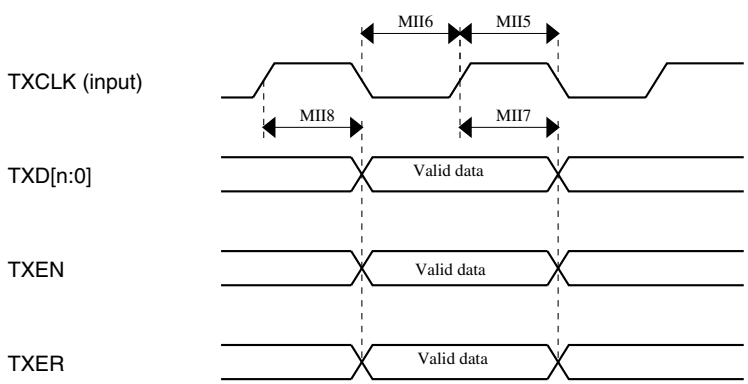


Figure 21. RMII/MII transmit signal timing diagram

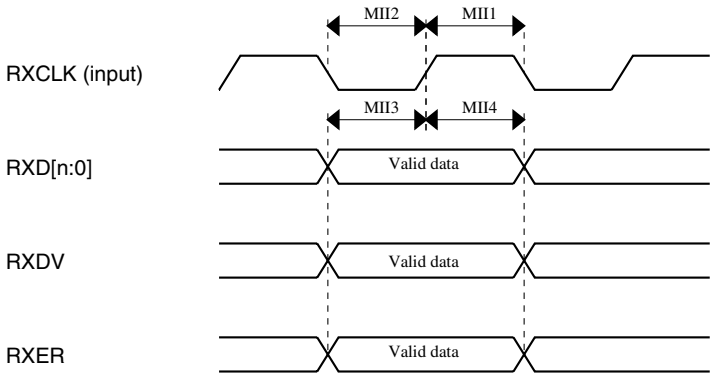


Figure 22. RMII/MII receive signal timing diagram

4.4.4.2 RMII signal switching specifications

The following timing specs meet the requirements for RMII style interfaces for a range of transceiver devices.

Table 40. RMII signal switching specifications

Num	Description	Min.	Max.	Unit
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
RMII1	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

4.4.5 MediaLB (MLB) electrical specifications

4.4.5.1 MLB 3-pin interface DC characteristics

The section lists the MLB 3-pin interface electrical characteristics.

Table 41. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V

Table continues on the next page...

Table 41. MediaLB 3-Pin Interface Electrical DC Specifications (continued)

Parameter	Symbol	Test Conditions	Min	Max	Unit
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = –6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	I_{IL}	0 < Vin < VDD	—	±10	µA

1. Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

4.4.5.2 MLB 3-pin interface electrical specifications

This section describes the timing electrical information of the MLB module.

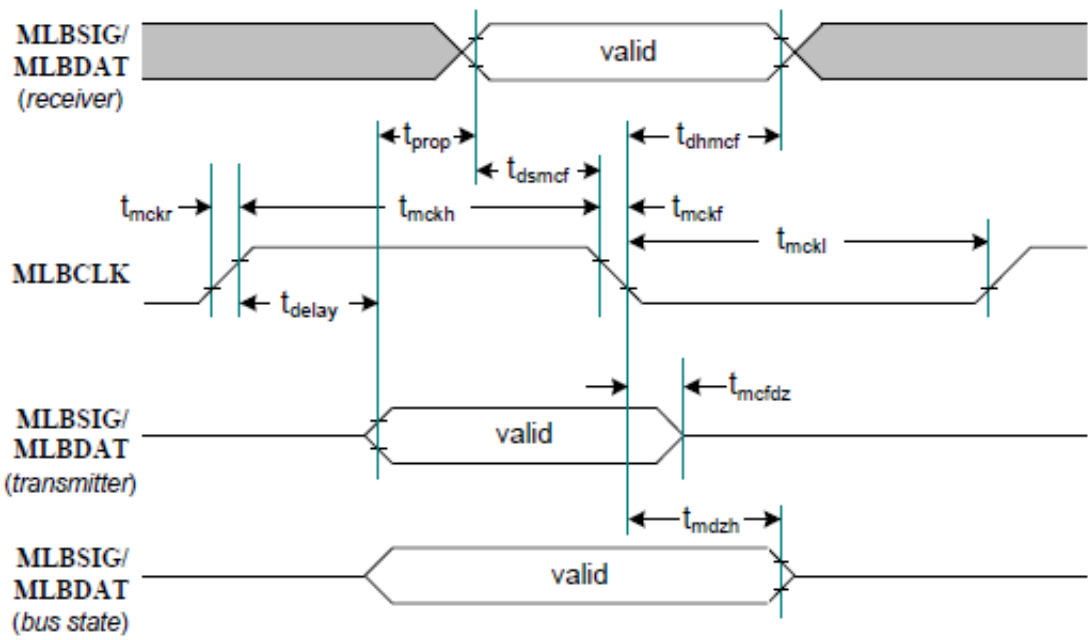


Figure 23. MediaLB 3-Pin Timing

Ground = 0.0 V; Load Capacitance = 60 pF, input transition= 1 ns ; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 42. MLB 3-Pin 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
MLBCLK rise time	$t_{mck}r$		3	ns	$V_{IL\ to\ V_{IH}}$
MLBCLK fall time	$t_{mck}f$		3	ns	$V_{IH\ to\ V_{IL}}$

Table continues on the next page...

Table 42. MLB 3-Pin 256/512 Fs Timing Parameters (continued)

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK low time[1]	$t_{mck}l$	30 14	—	ns	256xFs 512xFs
MLBCLK high time	$t_{mck}h$	30 14	—	ns	256xFs 512xFs
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mcfdz}	—	ns	—
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	$t_{mck}l$	ns	2
Bus output hold from MLBCLK low	t_{mdzh}	4	—	ns	2

1. MLBCLK low/high time includes the pluse width variation.
2. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 1024 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 43. MLB 3-Pin 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056 -	- 51.2	MHz MHz	1024 x fs at 44.0 kHz 1024 x fs at 50.0 kHz
MLBCLK rise time	f_{mckr}		1	ns	$V_{IL\ to}$ V_{IH}
MLBCLK fall time	f_{mckf}		1	ns	$V_{IH\ to}$ V_{IL}
MLBCLK low time	t_{mckl}	6.1	—	ns	2
MLBCLK high time	t_{mckh}	9.3	—	ns	2
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	1	—	ns	
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	t_{mcfdz}	—	ns	
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	t_{mckl}	ns	3
Bus Hold from MLBCLK low	t_{mdzh}	2	—	ns	3

1. The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.
2. MLBCLK low/high time includes the pluse width variation.

3. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

4.4.6 USB electrical specifications

4.4.6.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit http://www.usb.org.

4.4.6.2 ULPI timing specifications

The ULPI interface is fully compliant with the industry standard UTMI+ Low Pin Interface. Control and data timing requirements for the ULPI pins are given in the following table. These timings apply to synchronous mode only. All timings are measured with respect to the clock as seen at the USB_CLKIN pin.

Table 44. ULPI timing specifications

Num	Description	Min.	Typ.	Max.	Unit
	USB_CLKIN operating frequency	—	60	—	MHz
	USB_CLKIN duty cycle	—	50	—	%
U1	USB_CLKIN clock period	—	16.67	—	ns
U2	Input setup (control and data)	5	—	—	ns
U3	Input hold (control and data)	1	—	—	ns
U4	Output valid (control and data)	—	—	9.5	ns
U5	Output hold (control and data)	1	—	—	ns

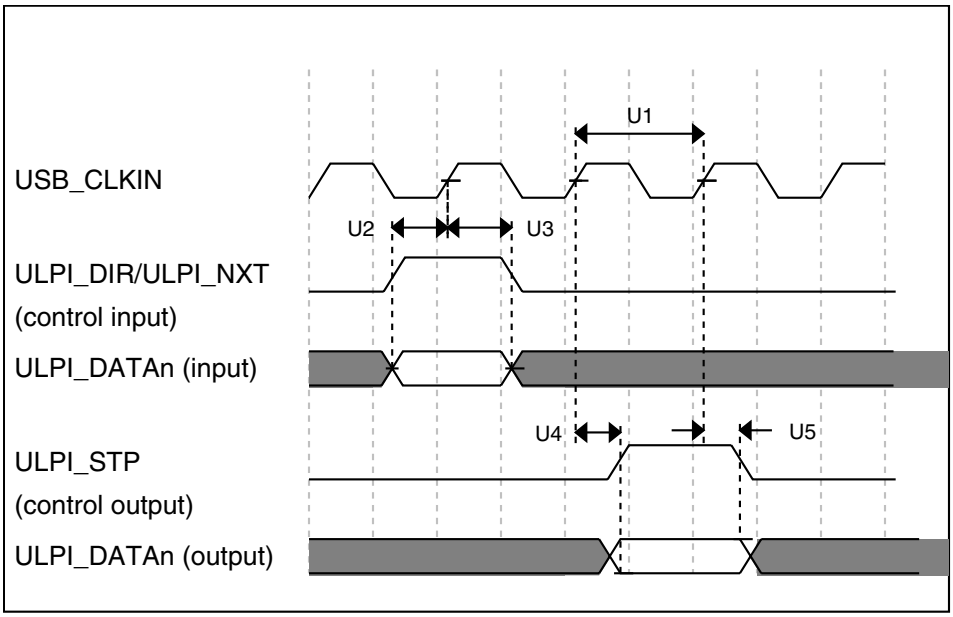


Figure 24. ULPI timing diagram

4.4.7 SAI electrical specifications

All timing requirements are specified relative to the clock period or to the minimum allowed clock period of a device

Table 45. Master mode SAI Timing

no	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S1	SAI_MCLK cycle time	40	-	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	-	BCLK period
S4	SAI_BCLK pulse width high/low	45%	55%	ns
S5	SAI_BCLK to SAI_FS output valid	-	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	-	ns
S7	SAI_BCLK to SAI_TXD valid	-	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	-	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	28	-	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	-	ns

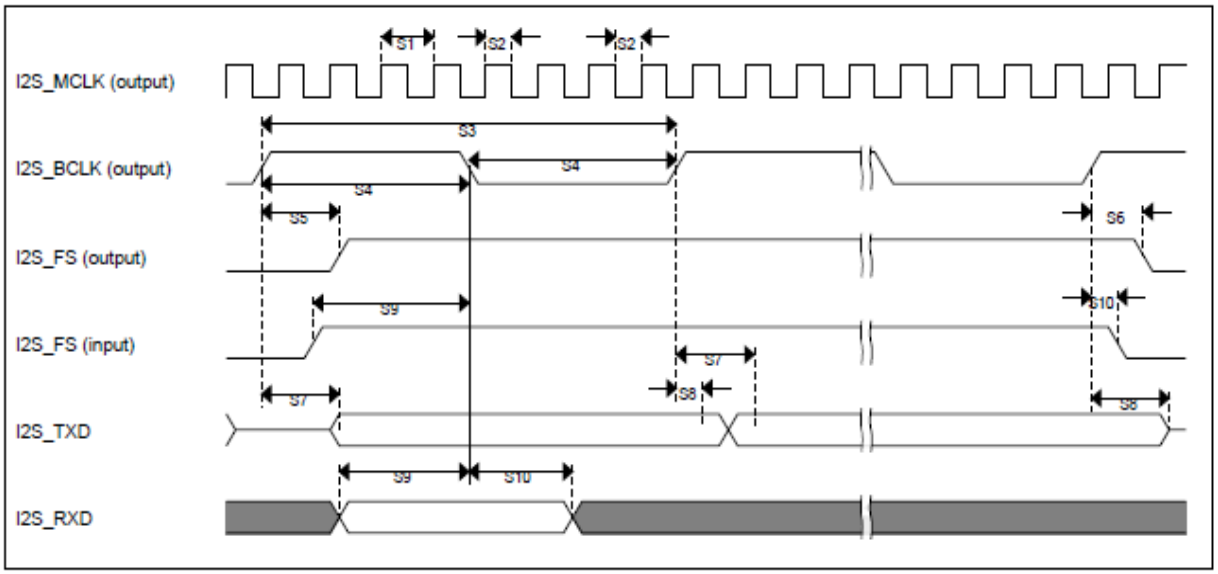


Figure 3. SAI Timing — Master Modes

Figure 25. Master mode SAI Timing

Table 46. Slave mode SAI Timing

No	Parameter	Value		Unit
		Min	Max	
	Operating Voltage	2.7	3.6	V
S11	SAI_BCLK cycle time (input)	80	-	ns
S12	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	-	ns
S14	SAI_FS input hold after SAI_BCLK	2	-	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	-	28	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	-	ns
S17	SAI_RXD setup before SAI_BCLK	10	-	ns
S18	SAI_RXD hold after SAI_BCLK	2	-	ns

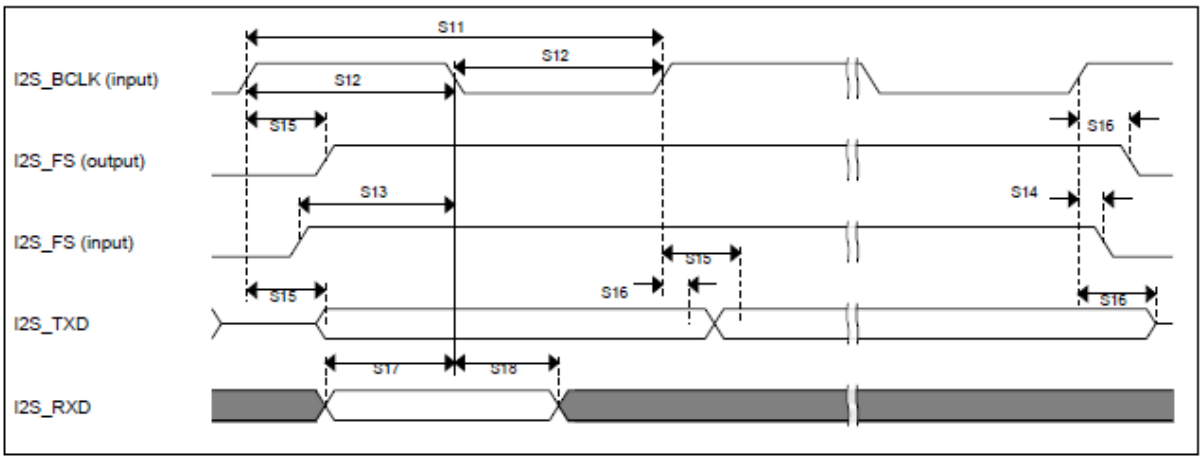


Figure 26. Slave mode SAI Timing

4.5 On-chip peripherals

4.5.1 On-chip peripherals

Table 47. On-chip peripherals current consumption

Symbol	Parameter	Conditions		Value	Unit
IDD_HV_A(CAN)	CAN (FlexCAN) supply current on VDD_HV_A	500 Kbps 125 Kbps	Total (static + dynamic) consumption: FlexCAN in loop-back mode XTAL@8 MHz used as CAN engine clock source Message sending period is 580 µs	TBD	µA
IDD_HV_A(eMIOS)	eMIOS supply current on VDD_HV_A		Static consumption: eMIOS channel OFF Global prescaler enabled Dynamic consumption: It does not change varying the frequency (0.003 mA)	TBD	
IDD_HV_A(SCI)	SCI (LINFlex) supply current on VDD_HV_A		Total (static + dynamic) consumption: LIN mode Baudrate: 20 Kbps	TBD	
IDD_HV_A(SPI)	SPI (DSPI) supply current on VDD_HV_A		Ballast static consumption (only clocked) Ballast dynamic consumption (continuous communication): Baudrate: 2 Mbit Transmission every 8 µs Frame: 16 bits	TBD	
IDD_HV_A(ADC)	ADC supply current on VDD_HV_A	VDD = 5.5 V	Ballast static consumption (no conversion) Ballast dynamic consumption (continuous conversion)	TBD	mA
IDD_HV_ADC0	ADC_0 supply current on VDD_HV_ADC0	VDD = 5.5 V	Analog static consumption (no conversion) Analog dynamic consumption (continuous conversion)	TBD	µA mA
IDD_HV_ADC1	ADC_1 supply current on VDD_HV_ADC1	VDD = 5.5 V	Analog static consumption (no conversion) Analog dynamic consumption (continuous conversion)	TBD	µA mA

Table continues on the next page...

Table 47. On-chip peripherals current consumption (continued)

Symbol	Parameter	Conditions		Value	Unit
IDD_HV(FLASH)	CFlash + DFlash supply current on VDD_HV_ADC	VDD = 5.5 V	_	TBD	mA
IDD_HV(PLL)	PLL supply current on VDD_HV	VDD = 5.5 V	_	TBD	

4.6 Debug specifications

4.6.1 JTAG interface timing

Table 48. JTAG pin AC electrical characteristics [1]

#	Symbol	Characteristic	Min	Max	Unit
1	t_{JCYC}	TCK Cycle Time[2]	62.5	—	ns
2	t_{JDC}	TCK Clock Pulse Width	40	60	%
3	$t_{TCKRISE}$	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	TMS, TDI Data Hold Time	5	—	ns
6	t_{TDOV}	TCK Low to TDO Data Valid	—	20[3]	ns
7	t_{TDOI}	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	TCK Low to TDO High Impedance	—	15	ns
11	t_{BSDV}	TCK Falling Edge to Output Valid	—	600[4]	ns
12	t_{BSDVZ}	TCK Falling Edge to Output Valid out of High Impedance	—	600	ns
13	t_{BSDHZ}	TCK Falling Edge to Output High Impedance	—	600	ns
14	t_{BSDST}	Boundary Scan Input Valid to TCK Rising Edge	15	—	ns
15	t_{BSDHT}	TCK Rising Edge to Boundary Scan Input Invalid	15	—	ns

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
4. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

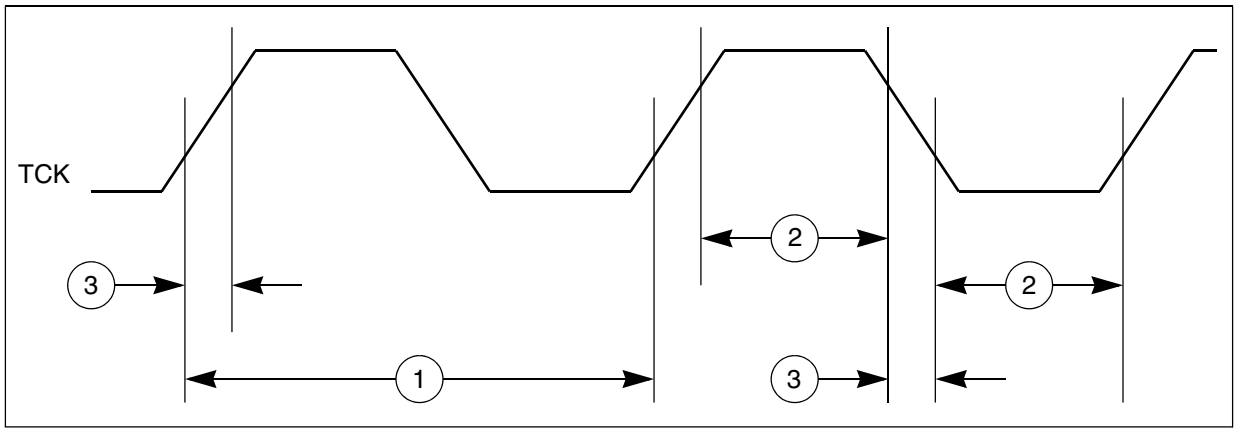


Figure 27. JTAG test clock input timing

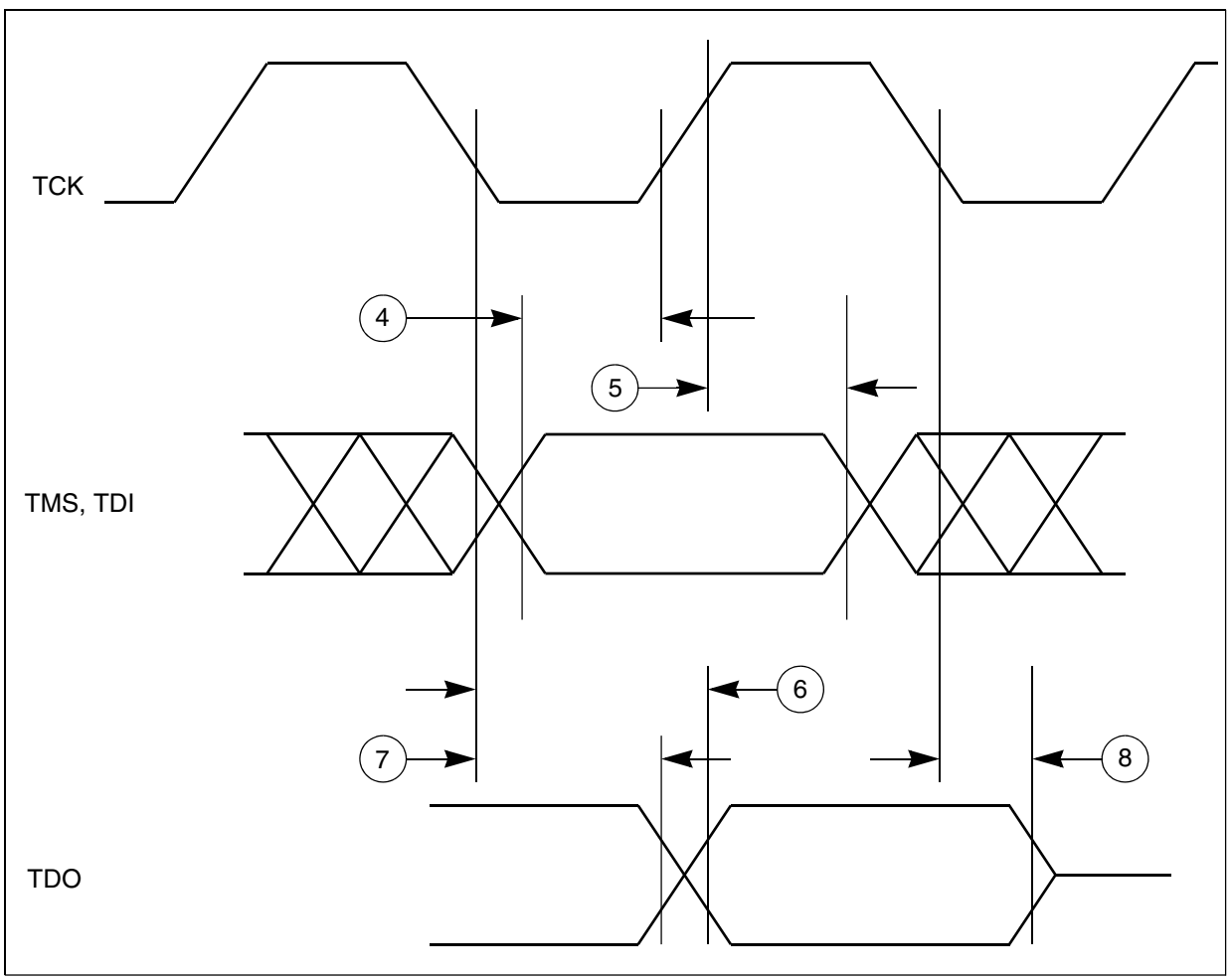


Figure 28. JTAG test access port timing

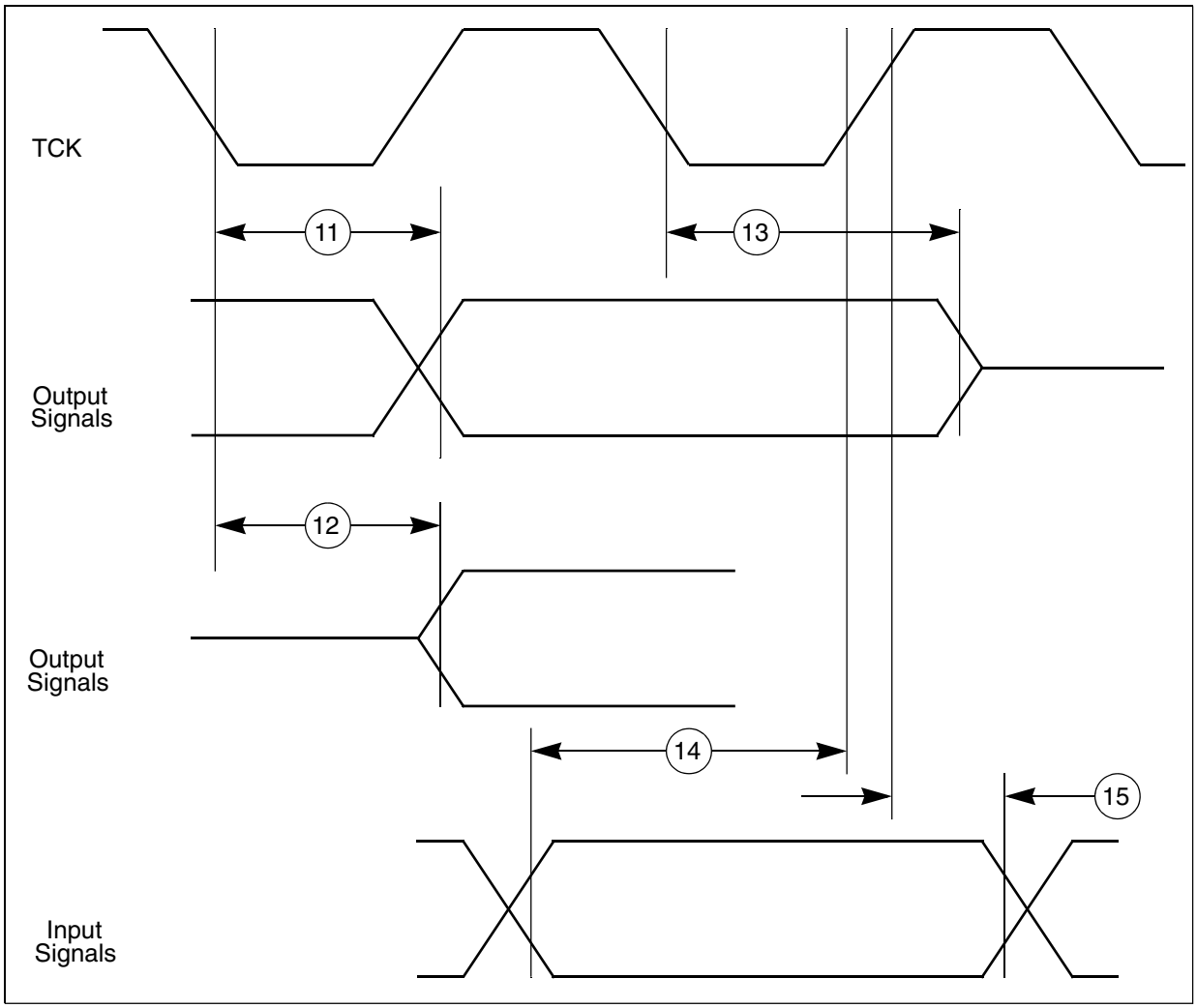


Figure 29. JTAG boundary scan timing

4.6.2 Nexus timing

Table 49. Nexus debug port timing [1]

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{MCYC}	MCKO Cycle Time	—	15.6	—	ns
2	t_{MDC}	MCKO Duty Cycle	—	40	60	%
3	t_{MDOV}	MCKO Low to MDO, $\overline{\text{MSEO}}$, $\overline{\text{EVTO}}$ Data Valid[2]	—	–0.1	0.25	tMCYC
4	t_{EVTIPW}	$\overline{\text{EVTI}}$ Pulse Width	—	4	—	tTCYC
5	t_{EVTOPW}	$\overline{\text{EVTO}}$ Pulse Width	—	1	—	tMCYC
6	t_{TCYC}	TCK Cycle Time[3]	—	62.5	—	ns
7	t_{TDC}	TCK Duty Cycle	—	40	60	%
8	t_{NTDIS}, t_{NTMSS}	TDI, TMS Data Setup Time	—	8	—	ns

Table continues on the next page...

Table 49. Nexus debug port timing [1] (continued)

No.	Symbol	Parameter	Conditions	Min	Max	Unit
9	t_{NTDIH}, t_{NTMSH}	TDI, TMS Data Hold Time	—	5	—	ns
10	t_{JOV}	TCK Low to TDO/RDY Data Valid	—	0	25	ns

1. JTAG specifications in this table apply when used for debug functionality. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal.
2. For all Nexus modes except DDR mode, MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
3. The system clock frequency needs to be four times faster than the TCK frequency.

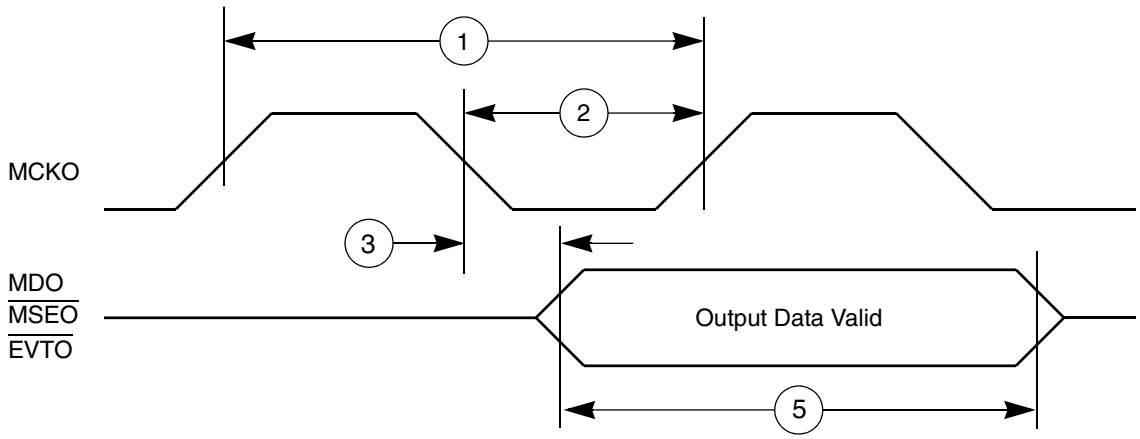


Figure 30. Nexus output timing

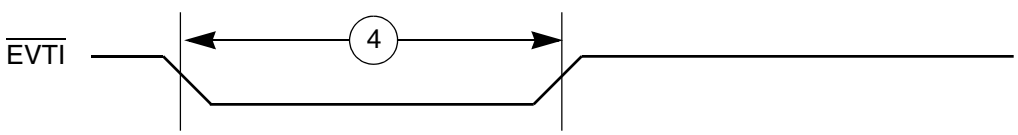


Figure 31. Nexus EVTI Input Pulse Width

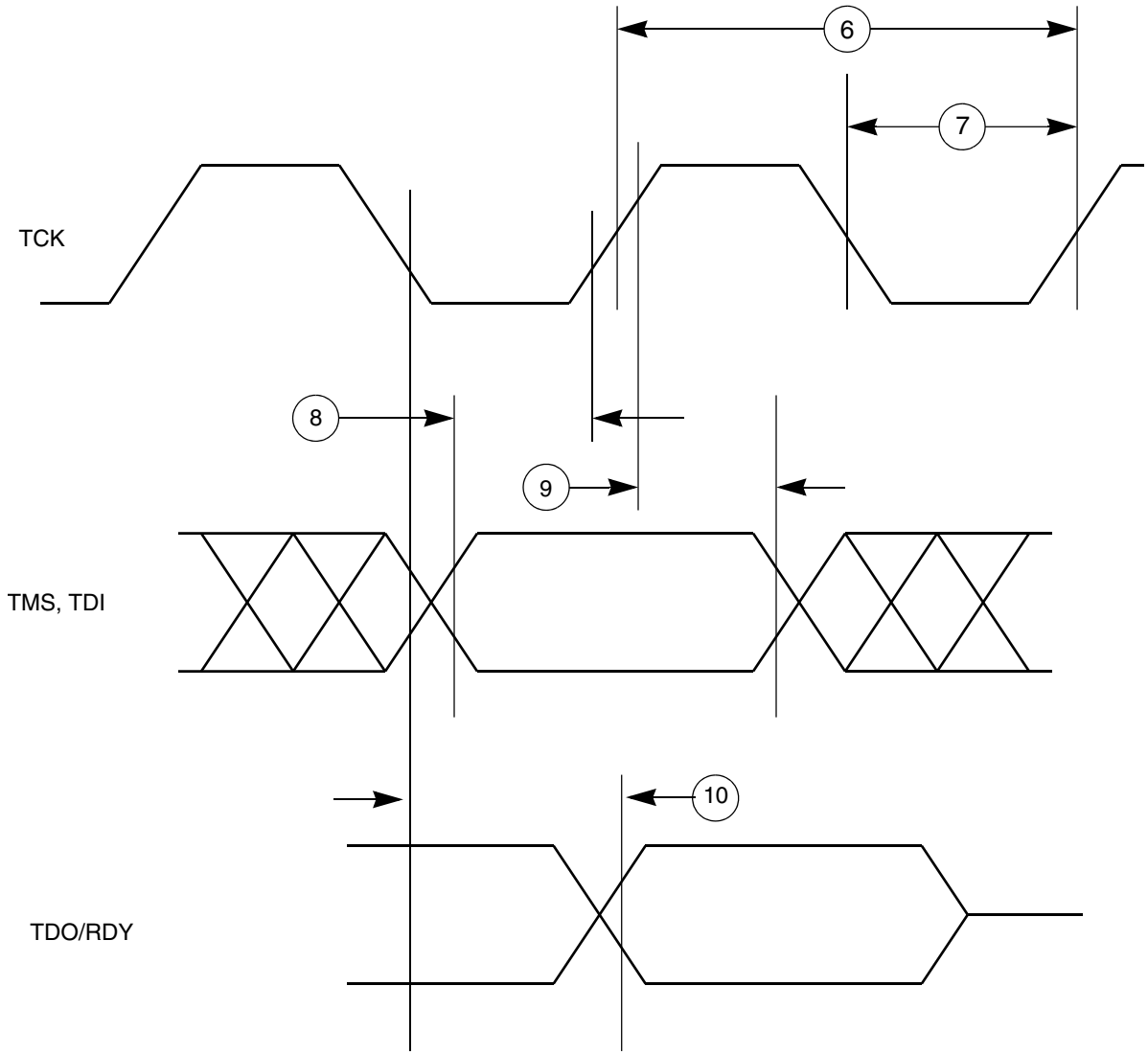


Figure 32. Nexus TDI, TMS, TDO timing

4.6.3 WKUP/NMI timing

Table 50. WKUP/NMI glitch filter

No.	Symbol	Parameter	Min	Typ	Max	Unit
1	W_{FNMI}	NMI pulse width that is rejected	—	—	20	ns
2	$W_{NFNMI}D$	NMI pulse width that is passed	400	—	—	ns

4.6.4 External interrupt timing (IRQ pin)

Table 51. External interrupt timing specifications

No.	Symbol	Parameter	Conditions	Min	Max	Unit
1	t_{IPWL}	IRQ pulse width low	—	3	—	t_{CYC}
2	t_{IPWH}	IRQ pulse width high	—	3	—	t_{CYC}
3	t_{ICYC}	IRQ edge to edge time	—	6	—	t_{CYC}

These values applies when IRQ pins are configured for rising edge or falling edge events, but not both.

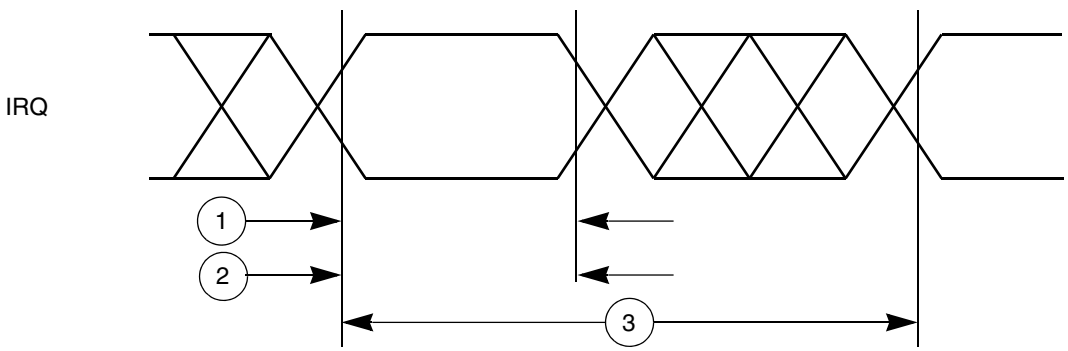


Figure 33. External interrupt timing

5 Thermal attributes

5.1 Thermal attributes

Board type	Symbol	Description	176LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	22	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	36	°C/W	1,3

Table continues on the next page...

Board type	Symbol	Description	176LQFP	Unit	Notes
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	16	°C/W	4
—	$R_{\theta JB}$	Thermal resistance, junction to board	11	°C/W	5
—	$R_{\theta JCtop}$	Thermal resistance, junction to case top	8	°C/W	6
—	$R_{\theta JCbotttom}$	Thermal resistance, junction to case bottom	0.5	°C/W	7
—	Ψ_{JT}	Thermal characterization parameter, junction to package top	1	°C/W	8

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	25.5	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.0	°C/W	1,2, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	18.1	°C/W	13
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	14.8	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	10.4	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	8.4	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top natural convection)	0.45	°C/W	6

Table continues on the next page...

Thermal attributes

Board type	Symbol	Description	324 MAPBGA	Unit	Notes
—	Ψ_{JB}	Thermal characterization parameter, junction to package top natural convection)	2.65	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	29.4	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	19.3	°C/W	1,2, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	21.4	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	14.8	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	11	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	9.5	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	0.5	°C/W	6

Table continues on the next page...

Board type	Symbol	Description	256 MAPBGA	Unit	Notes
—	Ψ_{JB}	Thermal characterization parameter, junction to package top outside center (natural convection)	2.8	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.,
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.
7. Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

6 Dimensions

6.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.freescale.com and perform a keyword search for the drawing's document number:

Package	Freescale Document Number
176-pin LQFP	98ASA00673D
256 MAPBGA	98ASA00346D
324 MAPBGA	98ASA10582D

7 Pinouts

7.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

8 Revision History

The following table provides a revision history for this document.

Table 52. Revision History

Rev. No.	Date	Substantial Changes
Rev1	14 March 2013	Initial Release
Rev1.1	16 May 2013	Updated Pinouts section

Rev2	22 May 2014	• Removed Category (SR, CC, P, T, D, B) column from all the table of the Datasheet
		• Revised the feature list.
		• Revised Introduction section to remove classification information.
		• Updated optional information in the ordering information figure.
		• Revised Absolute maximum rating section:
		  • Removed category column from table
		  • Added footnote at Ta
		• Revised Recommended operating conditions section
		  • Added notes
		  • Updated table: Recommended operating conditions (VDD_HV_x = 3.3 V)
		  • Updated table: Recommended operating conditions (VDD_HV_x = 5 V)
		• Revised Voltage regulator electrical characteristics
		  • Updated text describing bipolar transistors
		  • Updated figure: Voltage regulator capacitance connection
		  • Updated table: Voltage regulator electrical specifications
		  • Removed Brownout information
		• Revised Voltage monitor electrical characteristics table

Table continues on the next page...

Table 52. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• Revised Supply current characteristics section
		  • Updated table: Current consumption characteristics
		  • Updated table: Low Power Unit (LPU) Current consumption characteristics
		  • STANDBY Current consumption characteristics
		• Revised Electromagnetic Interference (EMI) characteristics section
		• Revised DC electrical specifications @ 3.3V Range table for naming convections.
		• Revised DC electrical specifications @ 5 V Range table for naming conventions
		• Deleted MLB 6-pin Electrical Specifications
		• Removed PORST characteristics from Functional reset pad electrical characteristics table
		• Added section PORST electrical characteristics
		• Revised Input impedance and ADC accuracy section to remove SNR, THD, SINAD, ENOB,
		• Revised 32 kHz oscillator electrical specifications table to remove 'Vpp' row.
		• Updated 16 MHz RC Oscillator electrical specifications table for statuptime, cycle to cycle jitter, and lonf term jitter
		• Updated 128 KHz Internal RC oscillator electrical specifications table.
		• Updated PLL electrical specifications table
		• Added Jitter Calculation table
		• Added Percentage of Sample exceeding specified value of jitter table

Table continues on the next page...

Table 52. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• Revised Memory interfaces section
		• Revised Communication interfaces section
		  • Updated note
		  • Added Continuous SCK timing table
		  • Added DSPI high speed mode I/Os table
		• Updated input transition value in section MLB 3-pin interface electrical specifications
		• Deleted MLB 6-pin interface DC characteristics section
		• Deleted MLB 6-pin interface AC characteristics section
		• Updated JTAG pin AC electrical characteristics table
		• Revised table under Thermal attributes section
		• Updated Obtaining package dimensions section for Freescale Document numbers

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
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