



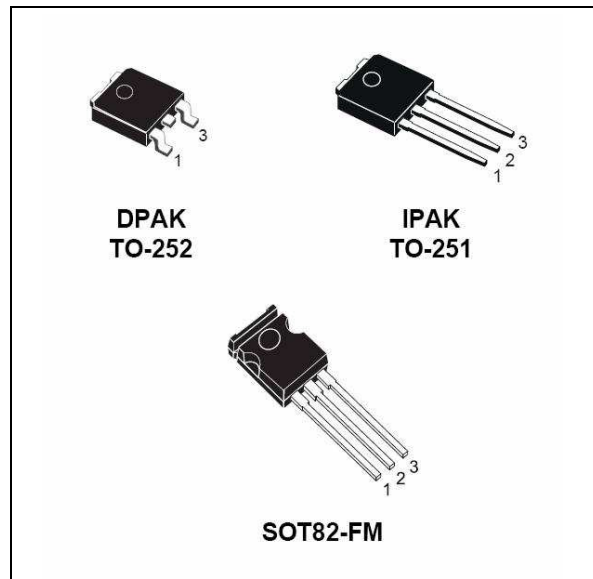
VND7N04, VND7N04-1 VNK7N04FM

"OMNIFET":
Fully autoprotected power MOSFET

Features

Type	V _{clamp}	R _{DS(on)}	I _{lim}
VND7N04	42 V	0.14 Ω	7 A
VND7N04-1	42 V	0.14 Ω	7 A
VNK7N04FM	42 V	0.14 Ω	7 A

- Linear current limitation
- Thermal shut down
- Short circuit protection
- Integrated clamp
- Low current drawn from input pin
- Diagnostic feedback through input pin
- ESD protection
- Direct access to the gate of the power MOSFET (analog driving)
- Compatible with standard power MOSFET



Description

The VND7N04, VND7N04-1 and VNK7N04FM are monolithic devices made using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear current limitation and overvoltage clamp protect the chip in harsh environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

Table 1. Device summary

Part number	Order code
VND7N04	VND7N04, VND7N04-1-E, VND7N04-E, VND7N0413TR, VND7N04TR-E
VND7N04-1	VND7N04-1
VNK7N04FM	VNK7N04FM

Contents

1	Block diagram	3
2	Electrical specification	4
	2.1 Absolute maximum rating	4
	2.2 Thermal data	4
	2.3 Electrical characteristics	4
3	Protection features	7
4	Package information	13
5	Revision history	16

2 Electrical specification

2.1 Absolute maximum rating

Table 2. Absolute maximum rating

Symbol	Parameter	Value		Unit
		DPAK IPAK	SOT-82FM	
V _{DS}	Drain-source voltage (V _{in} = 0)	Internally clamped		V
V _{in}	Input voltage	18		V
I _D	Drain current	Internally limited		A
I _R	Reverse DC output current	-7		A
V _{esd}	Electrostatic discharge (C = 100 pF, R=1.5 KΩ)	2000		V
P _{tot}	Total dissipation at T _c = 25 °C	60	9	W
T _j	Operating junction temperature	Internally limited		°C
T _c	Case operating temperature	Internally limited		°C
T _{stg}	Storage temperature	-55 to 150		°C

2.2 Thermal data

Table 3. Thermal data

		DPAK/IPAK	SOT82-FM	
R _{thj-case}	Thermal resistance junction-case max	3.75	14	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	100	100	°C/W

2.3 Electrical characteristics

Table 4. Electrical characteristics: off

(-40 < T_j < 125 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CLAMP}	Drain-source clamp voltage	I _D = 200 mA V _{in} = 0	32	42	52	V
V _{CLTH}	Drain-source clamp threshold voltage	I _D = 2 mA V _{in} = 0	31			V
V _{INCL}	Input-source reverse clamp voltage	I _{in} = -1 mA	-1.1		-0.25	V
I _{DSS}	Zero input voltage drain current (V _{in} = 0)	V _{DS} = 13 V V _{in} = 0 V _{DS} = 25 V V _{in} = 0			75 200	μA μA
I _{ISS}	Supply current from input pin	V _{DS} = 0 V V _{in} = 10 V		250	550	μA

Table 5. Electrical characteristics: on

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IN(th)}$	Input threshold voltage	$V_{DS} = V_{in}$ $I_D + I_{in} = 1$ mA	0.8		3	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{in} = 10$ V $I_D = 3.5$ A			0.14	Ω
		$V_{in} = 5$ V $I_D = 3.5$ A			0.28	Ω
		$-40 < T_j < 25$ °C				
		$V_{in} = 10$ V $I_D = 3.5$ A			0.28	Ω
		$V_{in} = 5$ V $I_D = 3.5$ A			0.56	Ω
		$T_j = 125$ °C				

Table 6. Electrical characteristics: dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 13$ V $I_D = 3.5$ A	2	5		S
C_{oss}	Output capacitance	$V_{DS} = 13$ V $f = 1$ MHz $V_{in} = 0$		250	500	pF

1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

Table 7. Electrical characteristics: switching

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_d(on)$	Turn-on delay time	$V_{DD} = 15$ V $I_d = 3.5$ A		50	150	ns
t_r	Rise time	$V_{gen} = 10$ V $R_{gen} = 10$ Ω		60	180	ns
$t_d(off)$	Turn-off delay time	(see Figure 26)		130	300	ns
t_f	Fall time			50	200	ns
$t_d(on)$	Turn-on delay time	$V_{DD} = 15$ V $I_d = 3.5$ A		140	500	ns
t_r	Rise time	$V_{gen} = 10$ V $R_{gen} = 1000$ Ω		0.4	1.1	μ s
$t_d(off)$	Turn-off delay time	(see Figure 26)		2.5	7	μ s
t_f	Fall time			1	4	μ s
$(di/dt)_{on}$	Turn-on current slope	$V_{DD} = 15$ V $I_D = 3.5$ A $V_{in} = 10$ V $R_{gen} = 10$ Ω		50		A/ μ s
Q_i	Total input charge	$V_{DD} = 12$ V $I_D = 3.5$ A $V_{in} = 10$ V		18		nC

Table 8. Electrical characteristics: source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 3.5$ A $V_{in} = 0$			1.7	V
$t_{rr}^{(2)}$	Reverse recovery time	$I_{SD} = 3.5$ A $di/dt = 100$ A/ μ s		40		ns
$Q_{rr}^{(2)}$	Reverse recovery charge	$V_{DD} = 30$ V $T_j = 25$ °C		0.2		μ C
$I_{RRM}^{(2)}$	Reverse recovery current	(see test circuit, Figure 28)		3.6		A

1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

2. Parameters guaranteed by design/characterization

Table 9. Electrical characteristics: protection

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain current limit	$V_{in} = 10\text{ V } V_{DS} = 13\text{ V}$	4	7	11	A
		$V_{in} = 5\text{ V } V_{DS} = 13\text{ V}$	4	7	11	A
$t_{dim}^{(1)}$	Step response	$V_{in} = 10\text{ V}$		13	20	μs
	Current limit	$V_{in} = 5\text{ V}$		15	25	μs
$T_{jsh}^{(1)}$	Overtemperature shutdown		150			$^{\circ}\text{C}$
$T_{jrs}^{(1)}$	Overtemperature reset		135			$^{\circ}\text{C}$
$I_{gf}^{(1)}$	Fault sink current	$V_{in} = 10\text{ V } V_{DS} = 13\text{ V}$		50		mA
		$V_{in} = 5\text{ V } V_{DS} = 13\text{ V}$		20		mA
$E_{as}^{(1)}$	Single pulse avalanche energy	starting $T_j = 25^{\circ}\text{C } V_{DD} = 20\text{ V}$ $V_{in} = 10\text{ V } R_{gen} = 1\text{ K}\Omega L = 30\text{ mH}$	0.4			J

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

3 Protection features

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current (I_{ISS}) flows into the Input pin in order to supply the internal circuitry.

The device integrates:

- Overvoltage clamp protection: internally set at 42 V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- Linear current limiter circuit: limits the drain current I_D to I_{lim} whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .
- Overtemperature and short circuit protection: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150 °C. The device is automatically restarted when the chip temperature falls below 135 °C.
- Status feedback: in the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω . The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

Figure 2. Thermal impedance for DPAK / IPAK

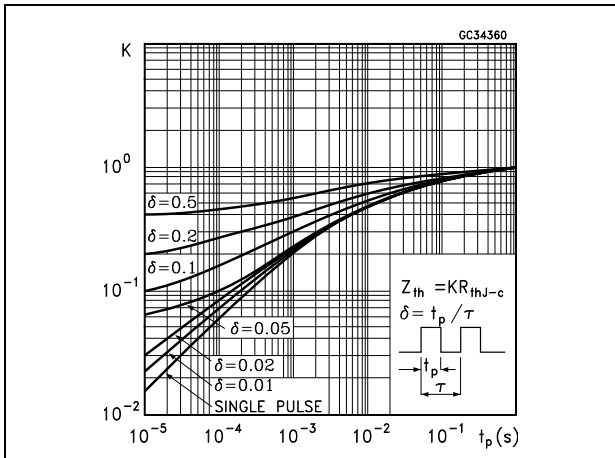


Figure 3. Derating curve

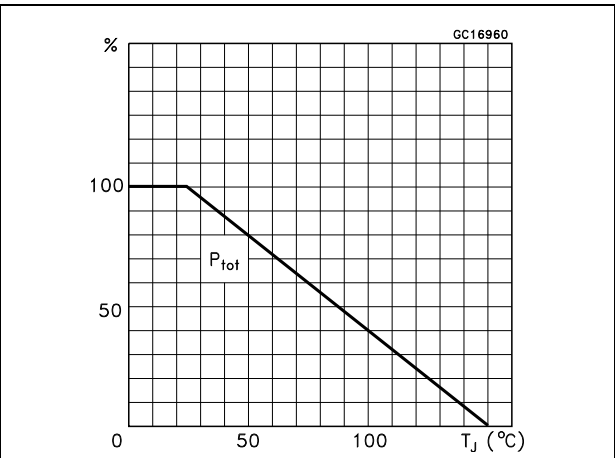


Figure 4. Output characteristics

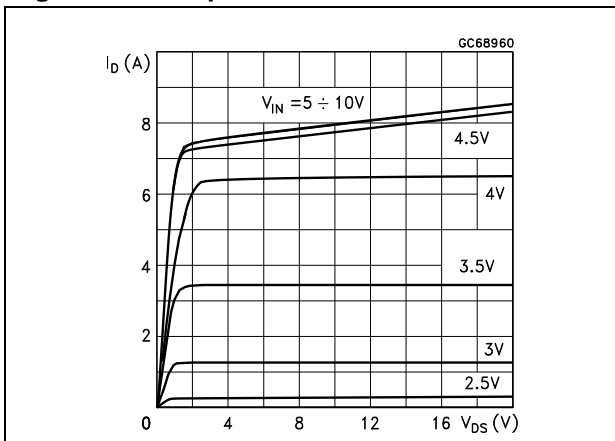


Figure 5. Transconductance

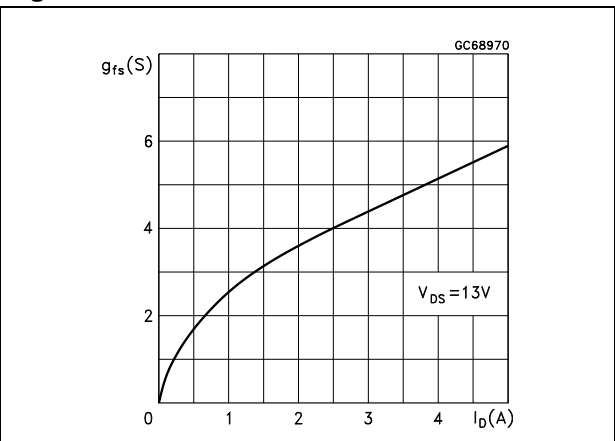


Figure 6. Static drain-source on resistance vs input voltage

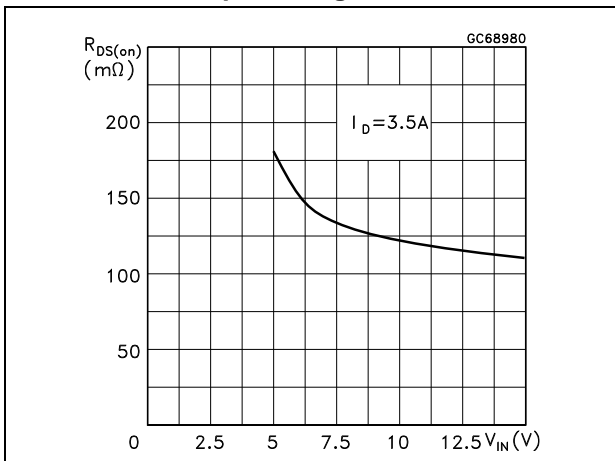


Figure 7. Static drain-source on resistance (part 1/2)

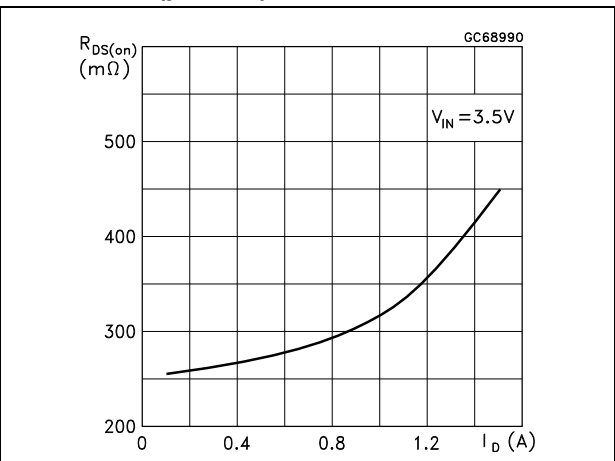


Figure 8. Static drain-source on resistance (part 2/2)

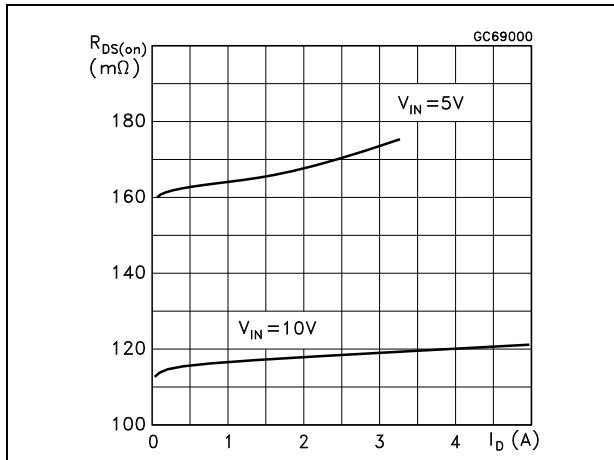


Figure 9. Input charge vs input voltage

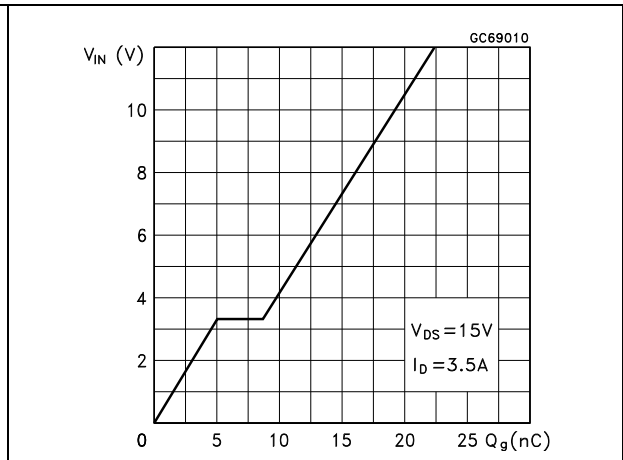


Figure 10. Capacitance variations

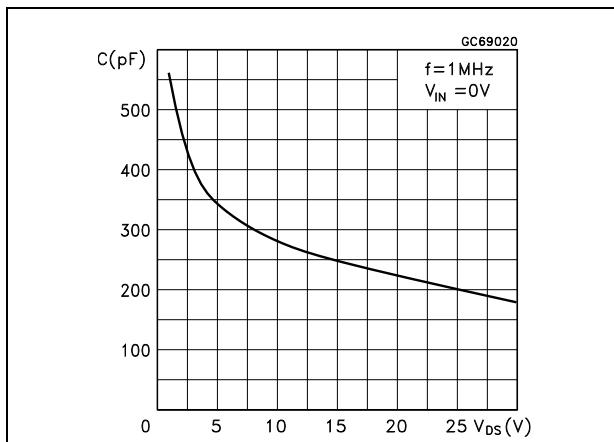


Figure 11. Normalized input threshold voltage vs temperature

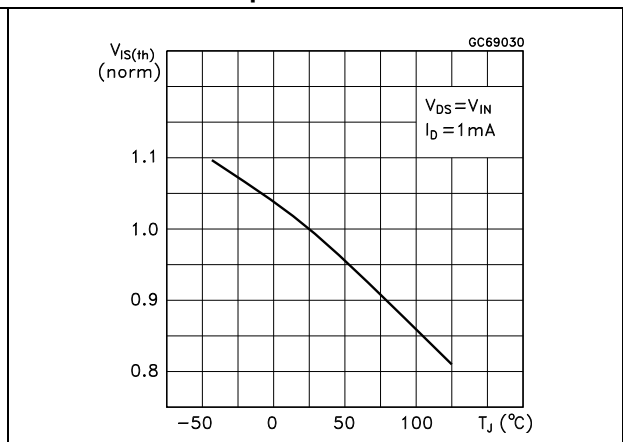


Figure 12. Normalized on resistance vs temperature (part 1/2)

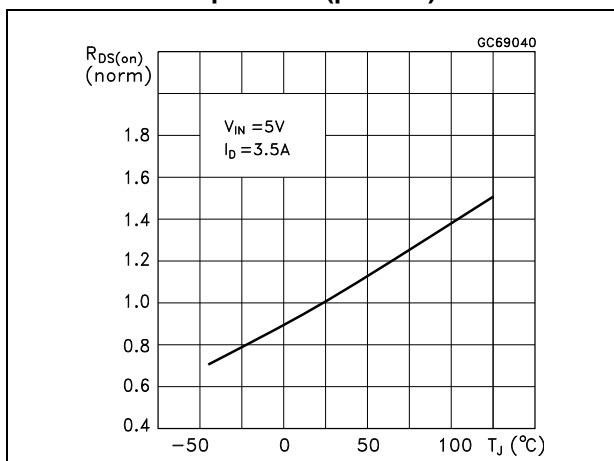


Figure 13. Normalized on resistance vs temperature (part 2/2)

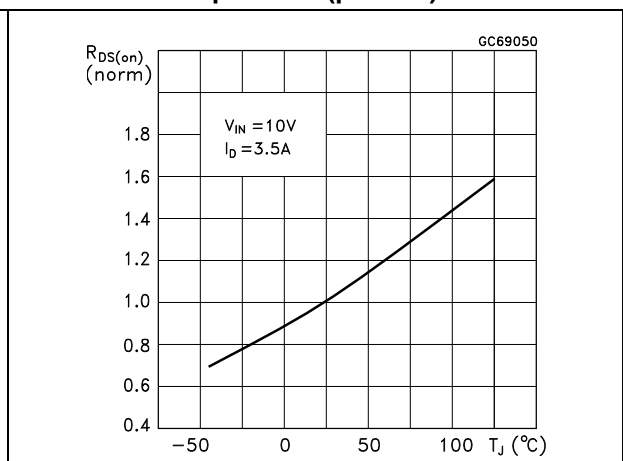


Figure 14. Turn-on current slope(part 1/2)

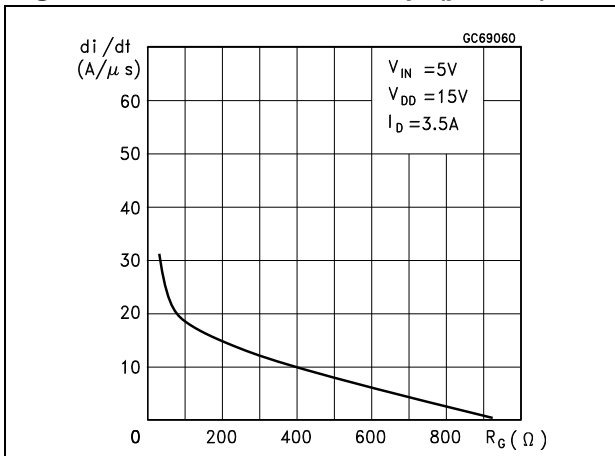


Figure 15. Turn-on current slope(part 2/2)

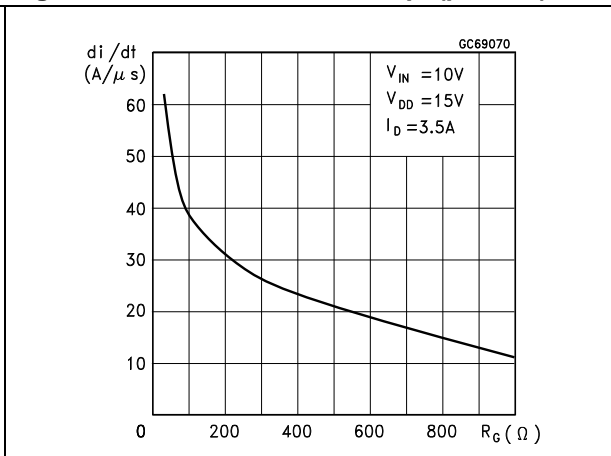


Figure 16. Turn-off drain-source voltage slope (part 1/2)

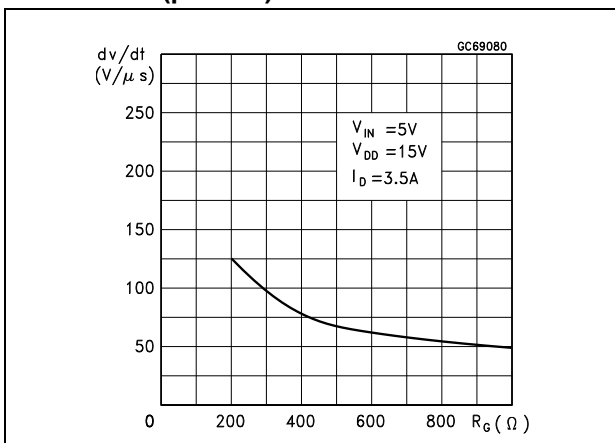


Figure 17. Turn-off drain-source voltage slope (part 2/2)

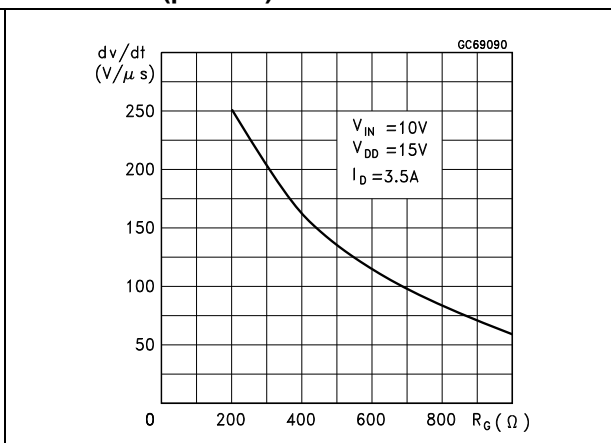


Figure 18. Switching time resistive load (part 1/3)

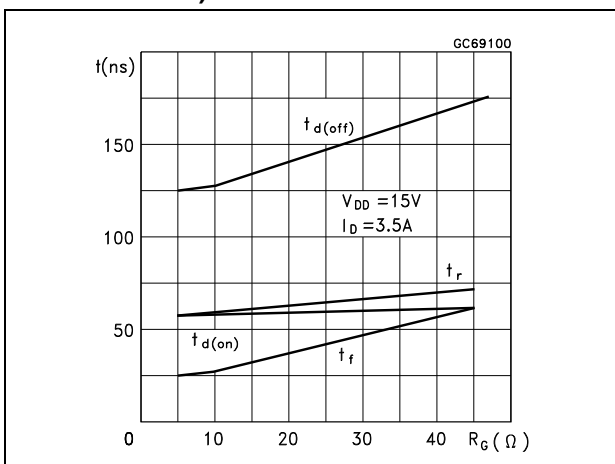


Figure 19. Switching time resistive load (part 2/3)

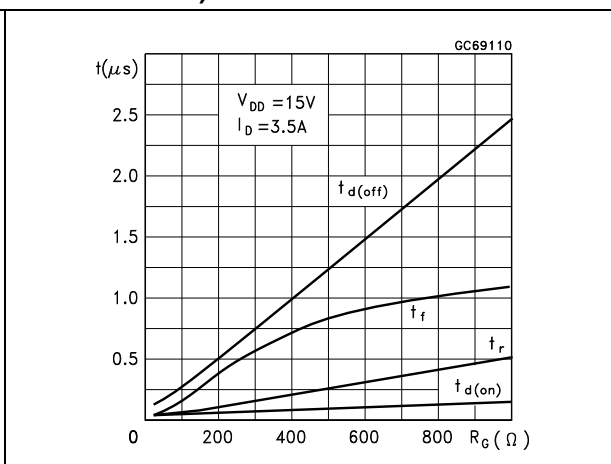


Figure 20. Switching time resistive load (part 3/3)

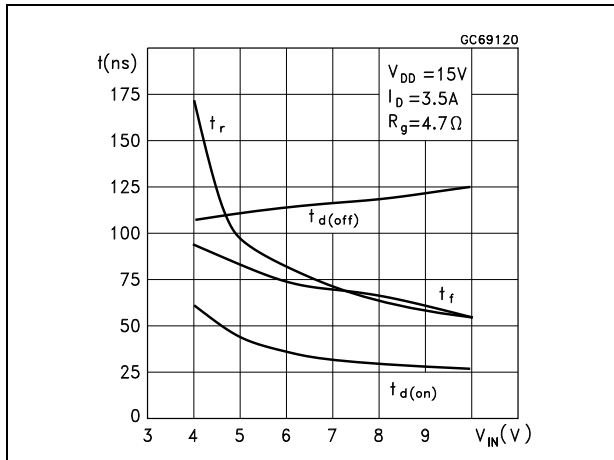


Figure 22. Step response current limit

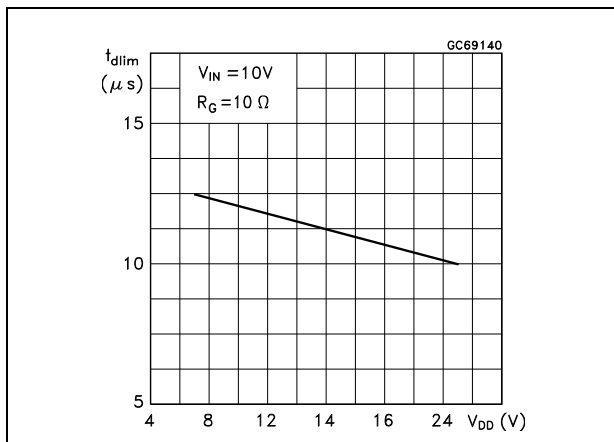


Figure 21. Current limit vs junction temperature

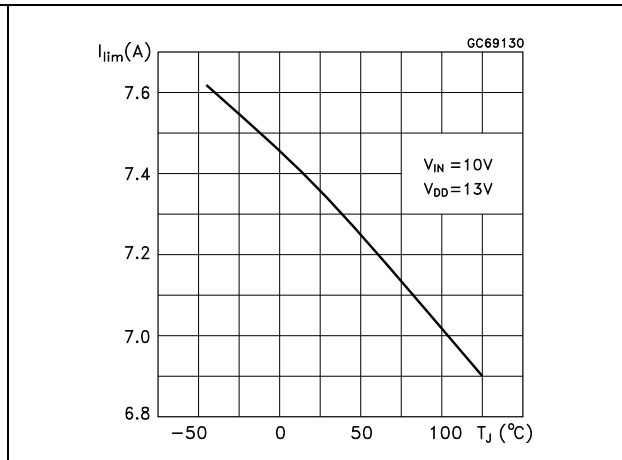


Figure 23. Source drain diode forward characteristics

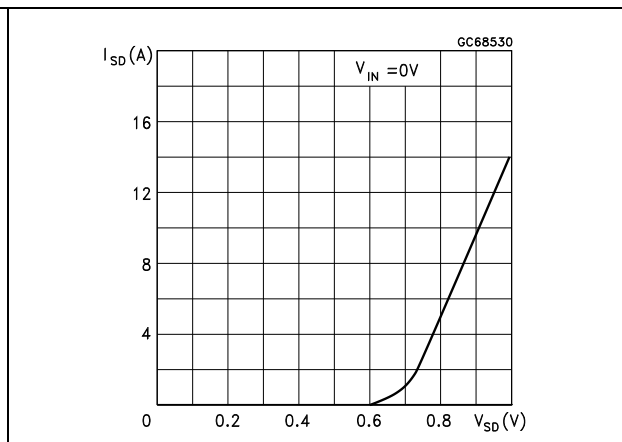


Figure 24. Unclamped inductive load test circuits

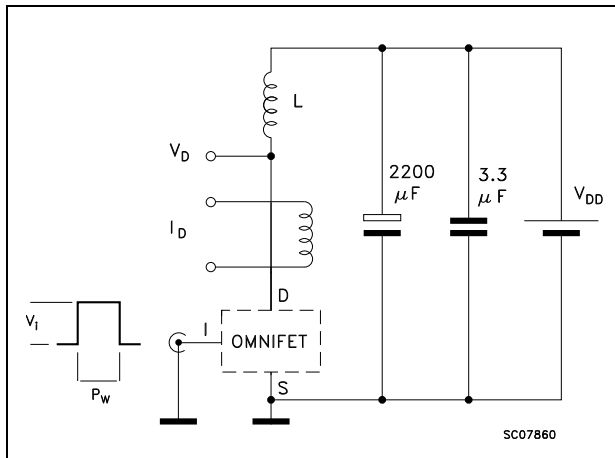


Figure 25. Unclamped inductive waveforms

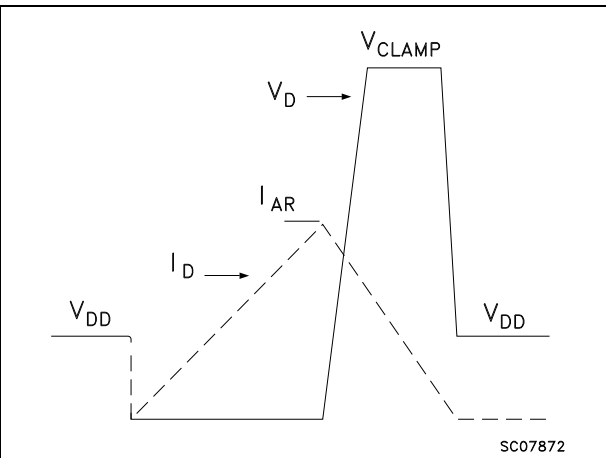


Figure 26. Switching times test circuits for resistive load

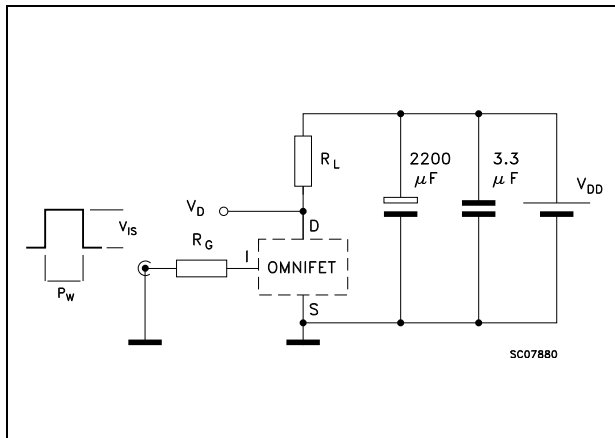


Figure 27. Input charge test circuit

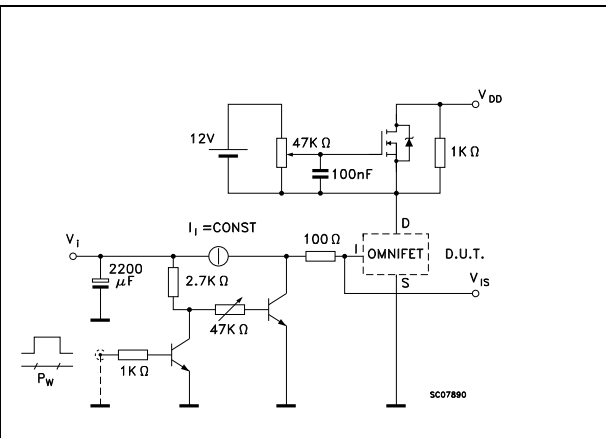
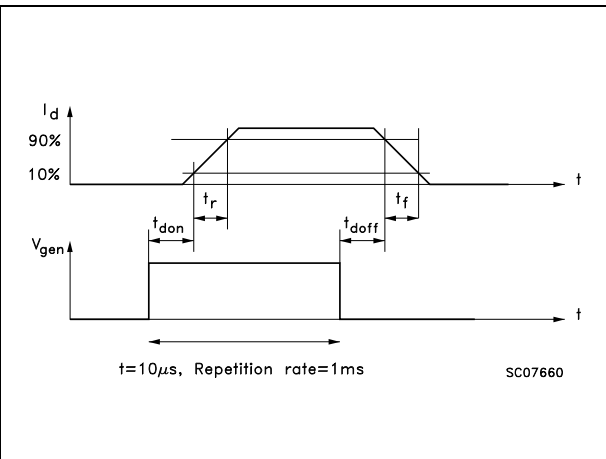
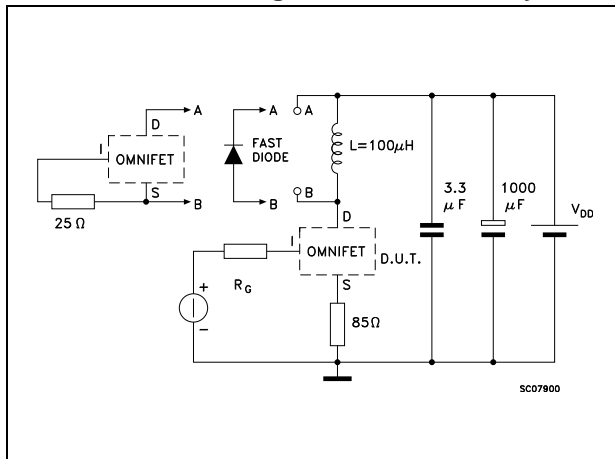


Figure 28. Test circuit for inductive load switching and diode recovery times

Figure 29. Waveforms



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

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Figure 30. TO-252 (DPAK) mechanical data

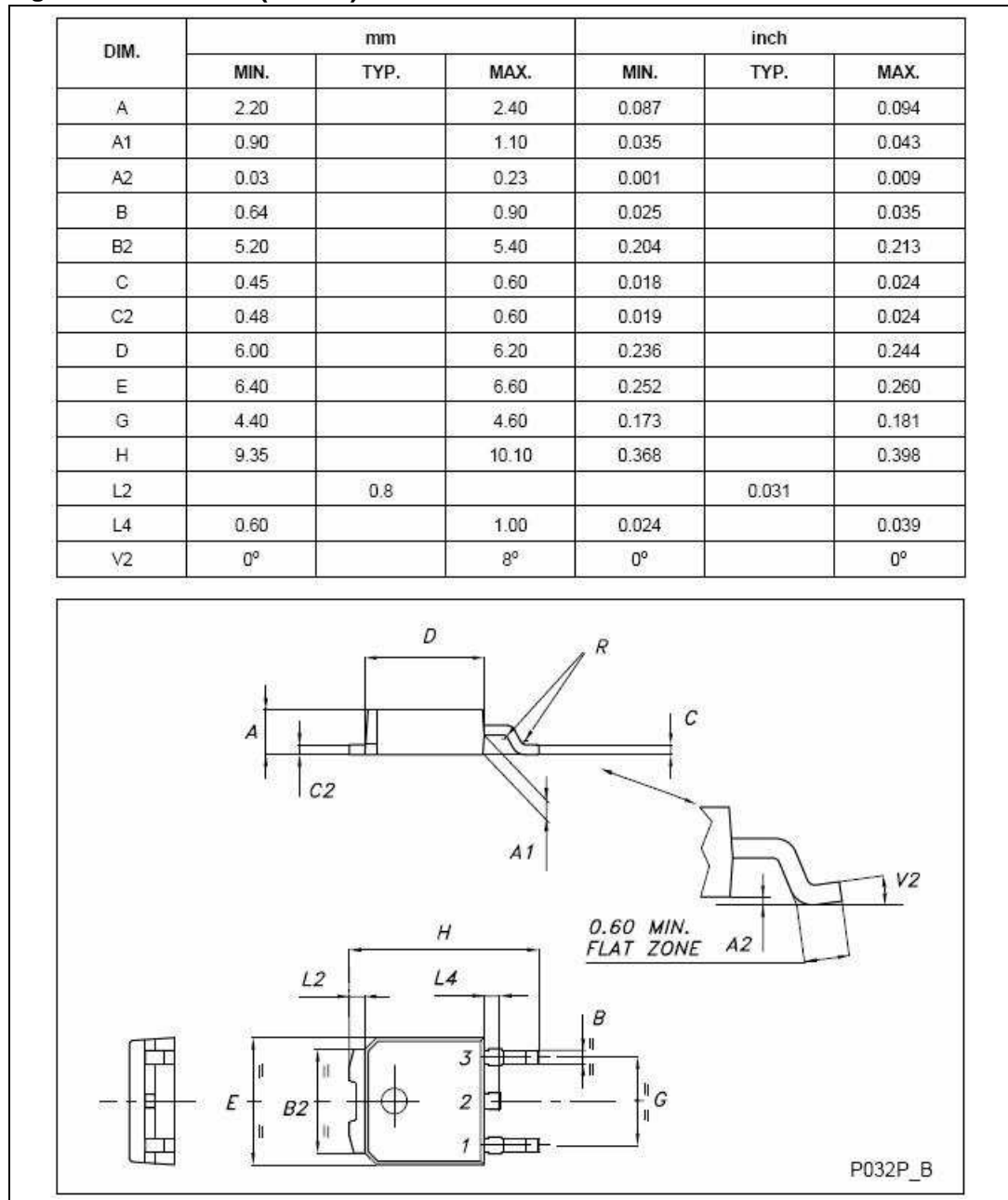
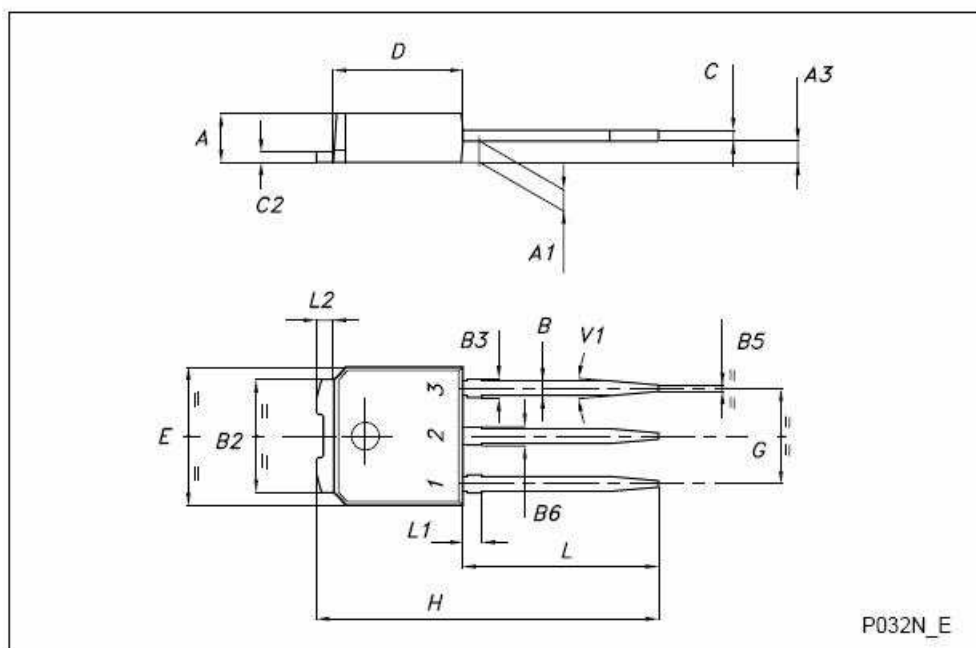


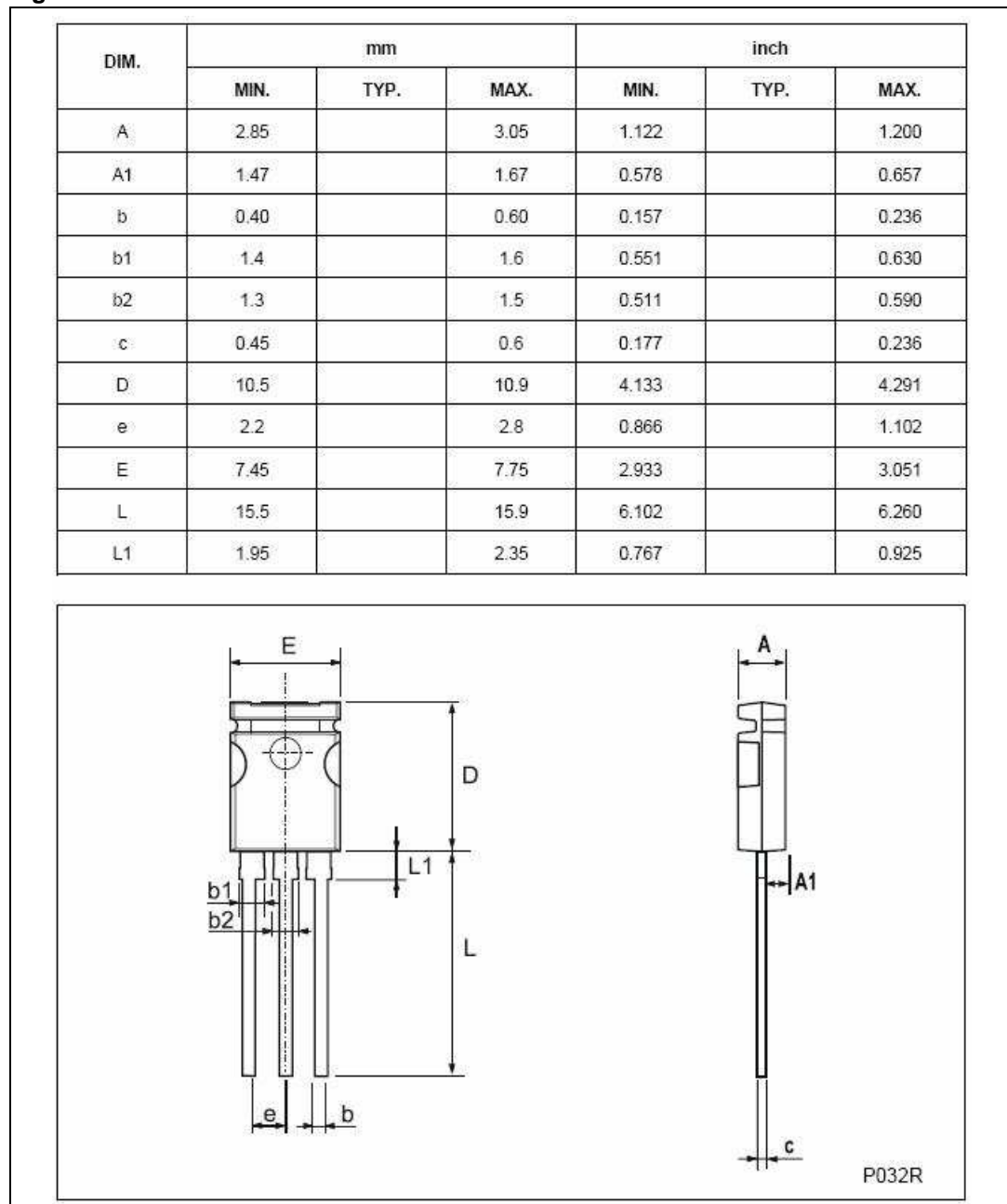
Figure 31. TO-251 (IPAK) mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A3	0.70		1.30	0.028		0.051
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
B3			0.85			0.033
B5		0.30			0.012	
B6			0.95			0.037
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.237		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	15.90		16.30	0.626		0.642
L	9.00		9.40	0.354		0.370
L1	0.80		1.20	0.031		0.047
L2		0.80	1.00		0.031	0.039
V1		10°			10°	



P032N_E

Figure 32. SOT-82FM mechanical data



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Jun-2004	0.1	Initial release.
18-Mar-2009	1	Document reformatted. Added Table 1: Device summary on page 1 . Updated Section 4: Package information on page 13

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
21-Jun-2004	1	Initial release.
25-Sep-2013	2	Updated Disclaimer

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