

General-Purpose 6ch Electronic Volume with Built-in Advanced Switch

BD3460FS

General Description

BD3460FS is a 6ch electronic volume which has the best audio efficiency in the industry. It has a ground isolation amplifier when connecting with external voice inputs such as portable audio and car navigation. Also, BD3460FS has a volume switching shock sound prevention technique called "Advanced Switch," supporting the construction of high quality car audio space by simple control.

Features

- Reduce switching noise of volume by using Advanced Switch circuit.
- Built-in buffered stereo ground isolation amplifier inputs, ideal for external input.
- Energy-saving design resulting in low-current consumption by utilizing the Bi-CMOS process. It has the advantage in quality over scaling down the power heat control of the internal regulators.
- Arranges all I/O terminals together for easier PCB layout and smaller PCB area.
- I²C BUS can be controlled by 3.3V / 5V.

Applications

It is optimal for car audio. It can also be used for car navigation, audio equipment of mini Compo, micro Compo, DVD, TV, etc.

Key Specifications

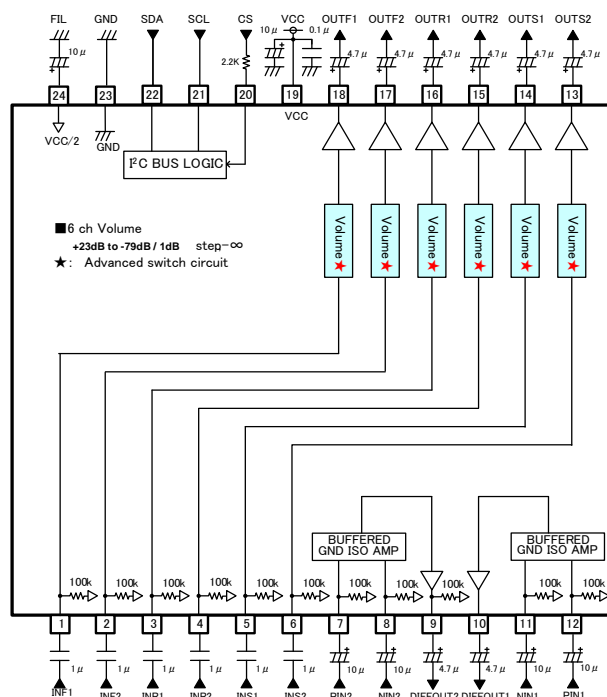
- Power Supply Voltage Range: 7.0V to 9.5V
- Circuit Current (no signal): 25mA (Typ)
- Total Harmonic Distortion: 0.0004%(Typ)
- Maximum Input Voltage: 2.35Vrms (Typ)
- Cross-talk Between Selectors: -105dB (Typ)
- Volume Control Range: +23dB to -79dB
- Output Noise Voltage: 1.9μVrms(Typ)
- Residual Output Noise Voltage: 1.6μVrms (Typ)
- Operating Temperature Range: -40°C to +85°C

Package

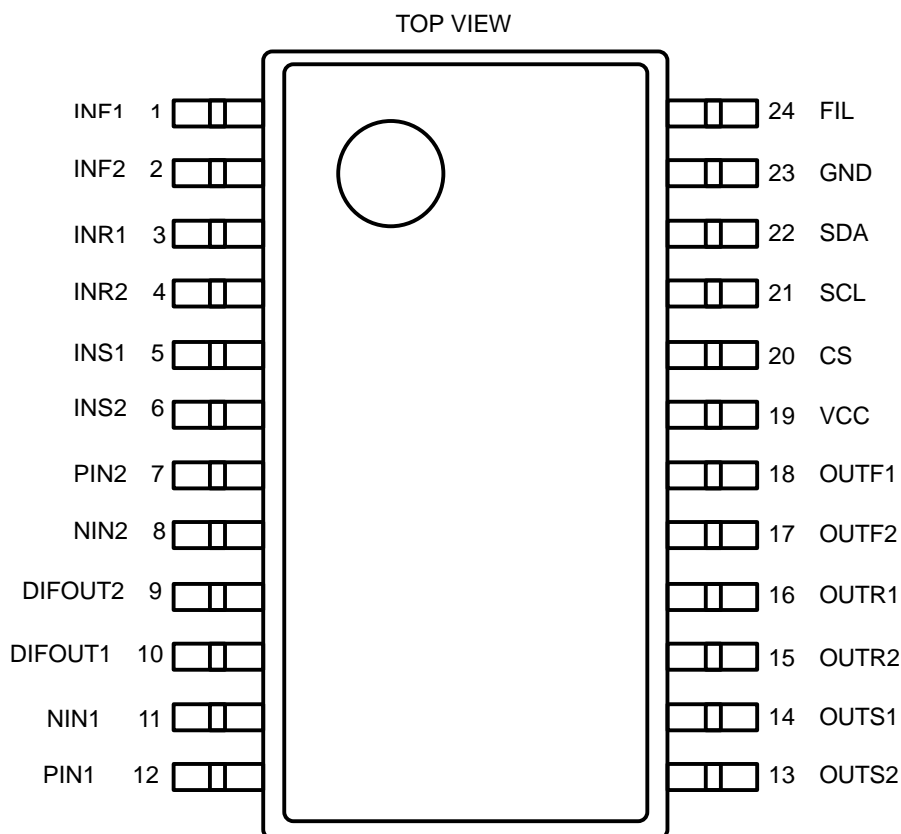
W(Typ) x D(Typ) x H(Max)



Typical Application Circuit



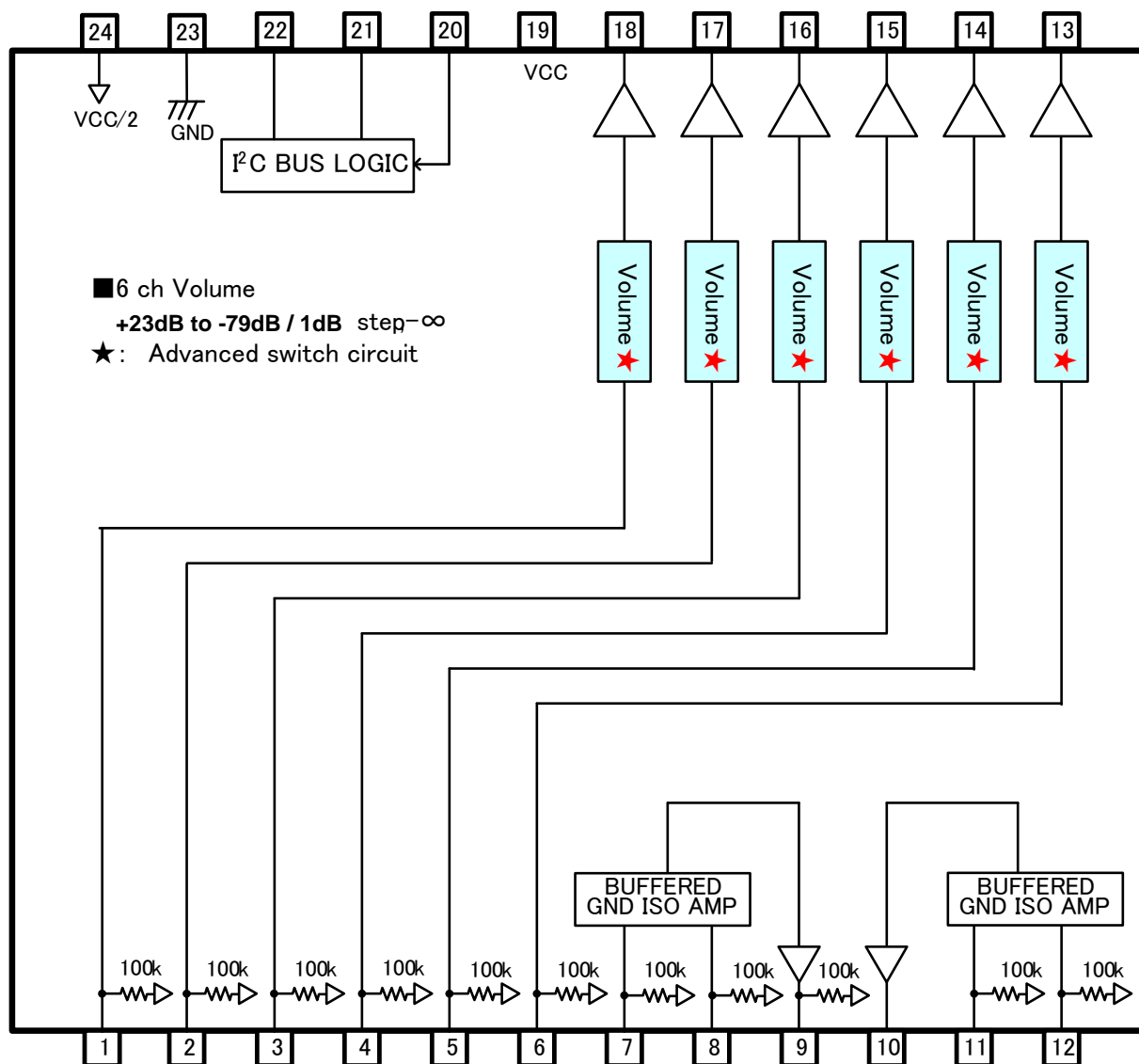
Pin Configuration



Pin Descriptions

Pin No.	Pin Name	Description	Pin No.	Pin Name	Description
1	INF1	1ch Front input terminal	13	OUTS2	2ch Subwoofer output terminal
2	INF2	2ch Front input terminal	14	OUTS1	1ch Subwoofer output terminal
3	INR1	1ch Rear input terminal	15	OUTR2	2ch Rear output terminal
4	INR2	2ch Rear input terminal	16	OUTR1	1ch Rear output terminal
5	INS1	1ch Subwoofer input terminal	17	OUTF2	2ch Front output terminal
6	INS2	2ch Subwoofer input terminal	18	OUTF1	1ch Front output terminal
7	PIN2	2ch DIFF amp positive input terminal	19	VCC	Power supply terminal
8	NIN2	2ch DIFF amp negative input terminal	20	CS	Chip select terminal
9	DIFOUT2	2ch DIFF amp output terminal	21	SCL	I ² C Communication clock terminal
10	DIFOUT1	1ch DIFF amp output terminal	22	SDA	I ² C Communication data terminal
11	NIN1	1ch DIFF amp negative input terminal	23	GND	GND terminal
12	PIN1	1ch DIFF amp positive input terminal	24	FIL	VCC/2 terminal

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V _{CC}	10.0V	V
Input Voltage	V _{IN}	V _{CC} +0.3 to GND-0.3	V
Power Dissipation	P _d	1 (Note 1)	W
Storage Temperature	T _{stg}	-55 to +150	°C

(Note 1) This value decreases 8mW/°C for Ta=25°C or more.

ROHM standard board shall be mounted. Thermal resistance $\theta_{ja} = 125(^{\circ}\text{C}/\text{W})$.

ROHM standard board Size : 70 x 70 x 1.6(mm³)

Material : FR4 glass epoxy board (3% or less of copper foil area)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V _{CC}	7.0 to 9.5	V
Temperature	T _{opr}	-40 to +85	°C

Electrical Characteristics

(Unless specified, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN}=1Vrms, R_g=600Ω, R_L=10kΩ, INF1 input, Volume 0dB)

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
GENERAL	Circuit Current (no signal)	I _Q	-	25	40	mA	No signal
	Voltage Gain	G _V	-1.5	0	+1.5	dB	G _V =20log(V _{OUT} /V _{IN})
	Channel Balance	CB	-1.5	0	+1.5	dB	CB=G _{V1} -G _{V2}
	Total Harmonic Distortion	THD	-	0.0004	0.05	%	V _{OUT} =1Vrms BW=400Hz-30kHz
	Output Noise Voltage *	V _{NO}	-	1.9	10	μVrms	R _g =0Ω BW=IHF-A
	Residual Output Noise Voltage *	V _{NOR}	-	1.6	10	μVrms	Volume=-∞dB R _g =0Ω BW=IHF-A
	Cross-talk Between Channels *	CTC	-	-105	-90	dB	R _g =0Ω CTC=20log(V _{OUT} /V _{IN}) BW=IHF-A
	Ripple Rejection	RR	-	-80	-40	THD	f=100Hz V _{RR} =100mVrms RR=20log(V _{OUT} /V _{CCIN})
DIFF	Input Impedance	R _{IN_D}	70	100	130	kΩ	
	Common Mode Rejection Ratio *	CMRR	50	65	-	dB	PIN and NIN input CMRR=20log10(V _{IN} /V _{OUT}) BW=IHF-A

Electrical Characteristics – continued

(Unless specified, Ta=25°C, V_{CC}=8.5V, f=1kHz, V_{IN}=1Vrms, R_g=600Ω, R_L=10kΩ, INF1 input, Volume 0dB)

BLOCK	Parameter	Symbol	Limit			Unit	Conditions
			Min	Typ	Max		
VOLUME	Input Impedance	R _{IN_V}	70	100	130	kΩ	
	Maximum Input Voltage	V _{IM}	2	2.35	-	Vrms	V _{IM} AT THD+N(V _{OUT})=1% BW=400Hz-30kHz
	Maximum Gain	G _{V_BST}	21	23	25	dB	Gain=23dB V _{IN} =100mVrms G _V =20log(V _{OUT} /V _{IN})
	Maximum Attenuation *	G _{V_MIN}	-	-109	-90	dB	Volume=-∞dB G _V =20log(V _{OUT} /V _{IN}) BW=IHF-A
	Step Resolution	G _{V_STEP}	-	1	-	dB	GAIN&ATT=+23dB to -79dB
	Gain Set Error	G _{V_ERR}	-2	0	+2	dB	Gain=+1dB to +23dB
	Attenuation Set Error 1	G _{V_ERR1}	-2	0	+2	dB	ATT=-1dB to -15dB
	Attenuation Set Error 2	G _{V_ERR2}	-3	0	+3	dB	ATT=-16dB to -47dB
	Attenuation Set Error 3	G _{V_ERR3}	-4	0	+4	dB	ATT=-48dB to -79dB
	Output Impedance	R _{OUT}	-	-	50	Ω	V _{IN} =100mVrms
	Maximum Output Voltage	V _{OM}	2	2.35	-	Vrms	THD+N=1% BW=400Hz-30kHz

VP-9690A(Average value detection, effective value display) filter by Matsushita Communication is used for * measurement.
Phase between input / output is same.

Typical Performance Curves

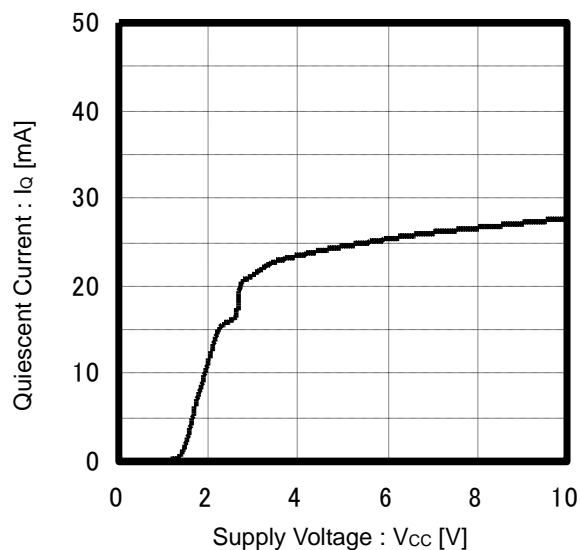


Figure 1. Quiescent Current vs Supply Voltage

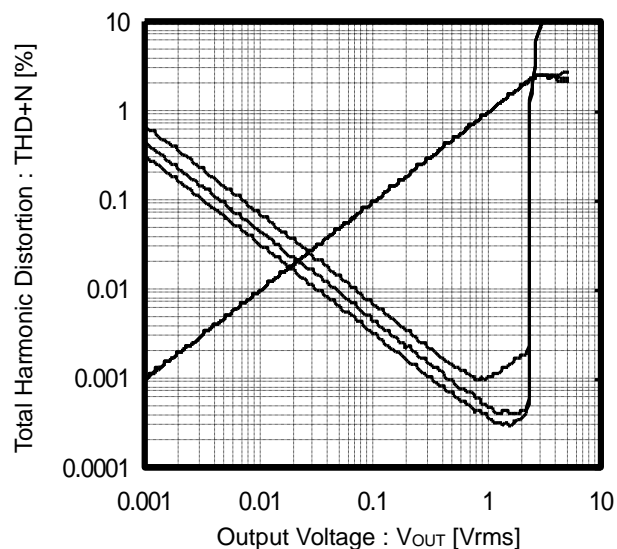


Figure 2. Total Harmonic Distortion vs Output Voltage

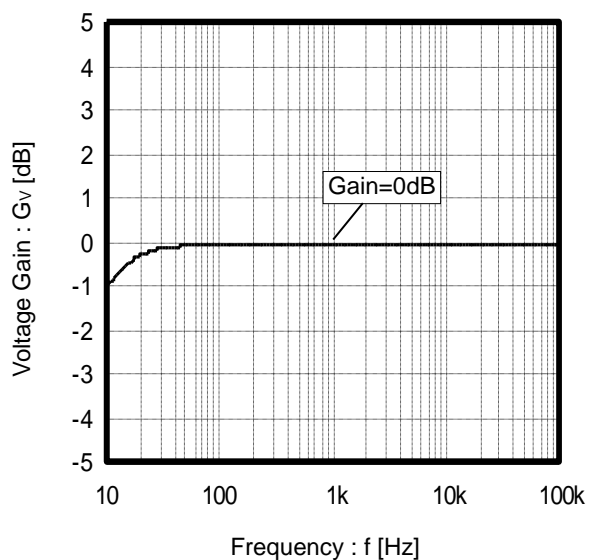
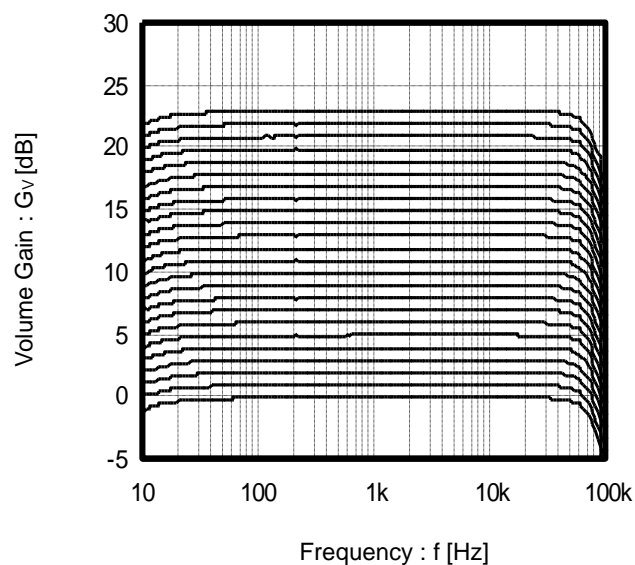


Figure 3. Voltage Gain vs Frequency

Figure 4. Volume Gain vs Frequency
(-0dB to +23dB)

Typical Performance Curves – continued

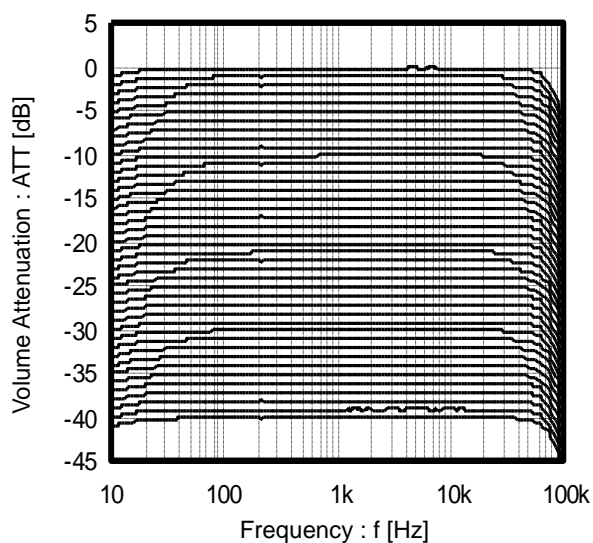


Figure 5. Volume Gain vs Frequency 1
(+0dB to -40dB)

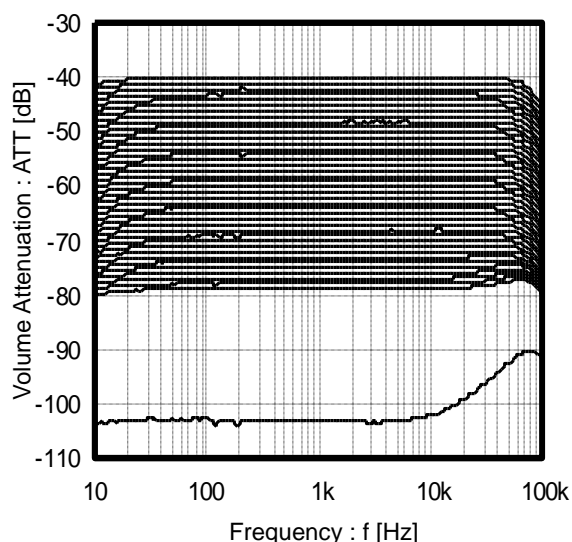


Figure 6. Volume Gain vs Frequency 2
(-41dB to -79dB)

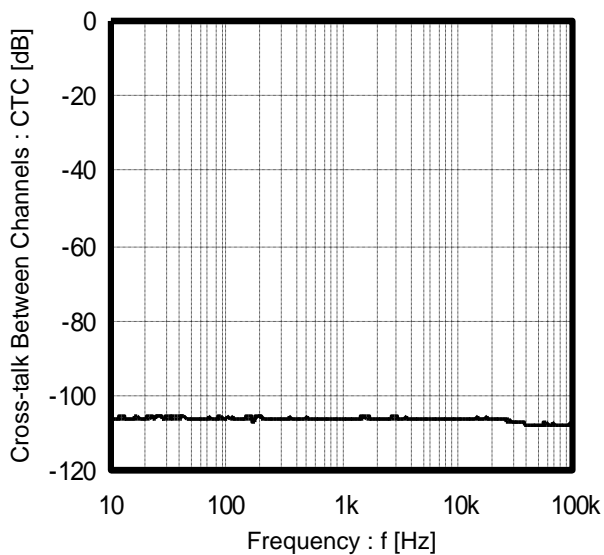


Figure 7. Cross-talk Between Channels vs Frequency

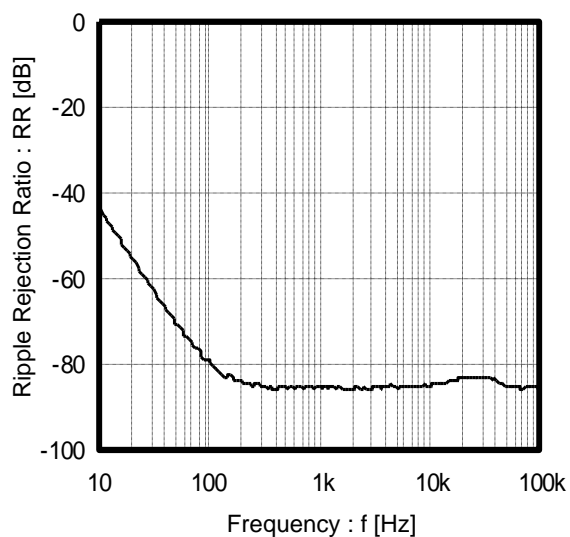


Figure 8. Ripple Rejection Ratio vs Frequency

Typical Performance Curves – continued

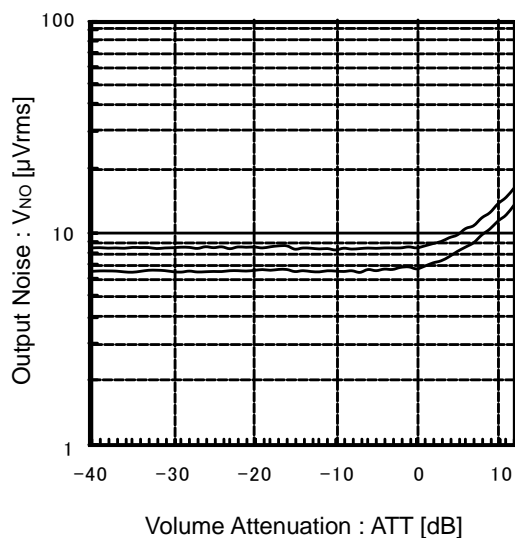


Figure 9. Output Noise vs Volume Attenuation

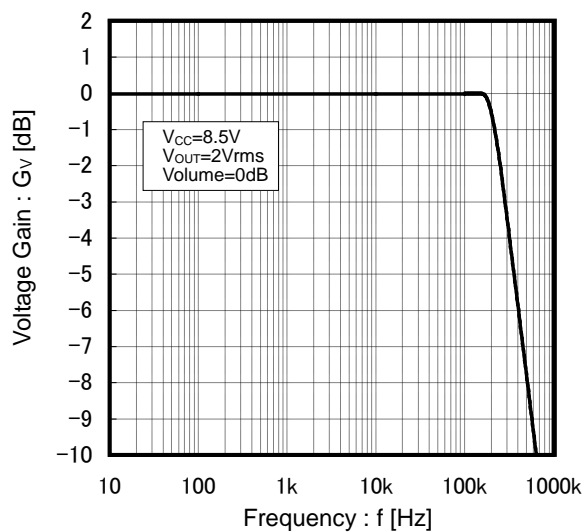


Figure 10. Volume Gain of Large Output Level vs Frequency

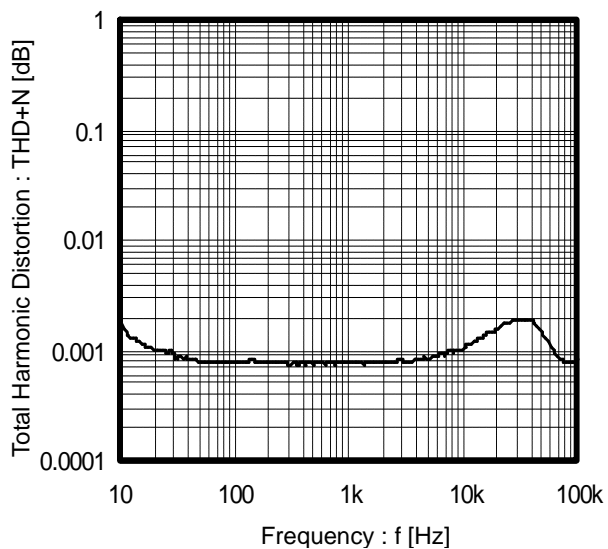


Figure 11. Total Harmonic Distortion vs Frequency

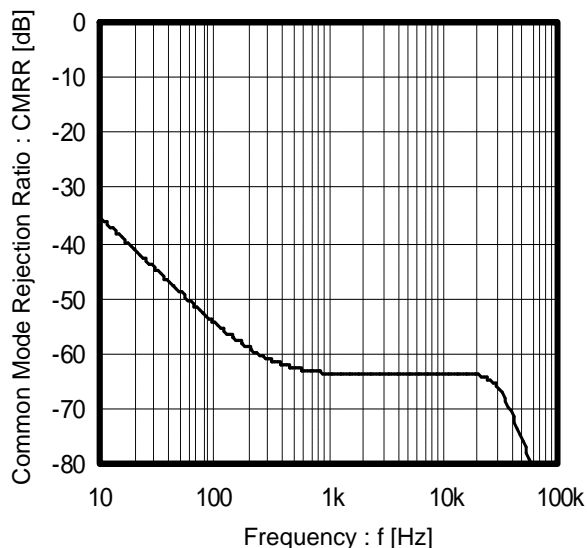


Figure 12. Common Mode Rejection Ratio vs Frequency

Typical Performance Curves – continued

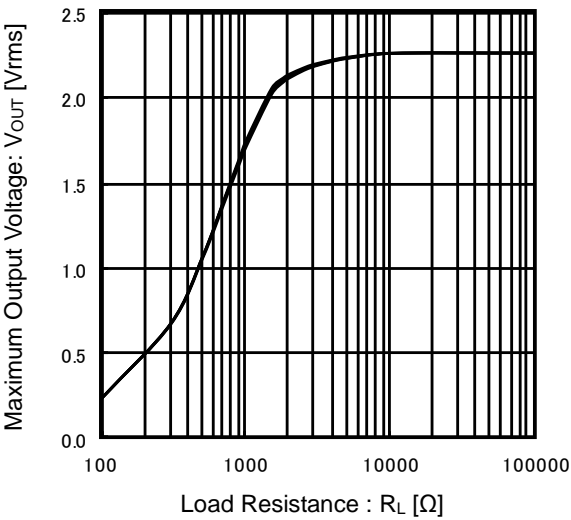


Figure 13. Maximum Output Voltage vs Load Resistance

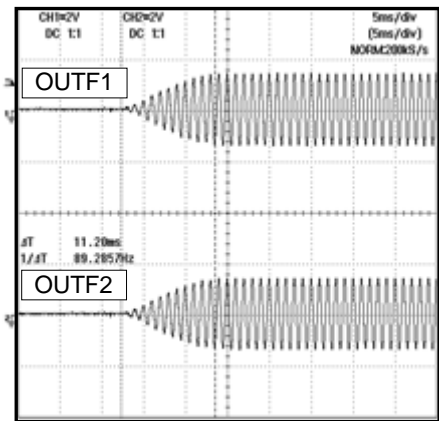


Figure 14. Advanced Switch 1

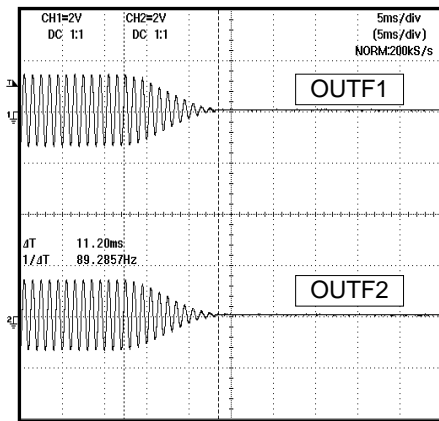


Figure 15. Advanced Switch 2

Timing Chart

CONTROL SIGNAL SPECIFICATIONS

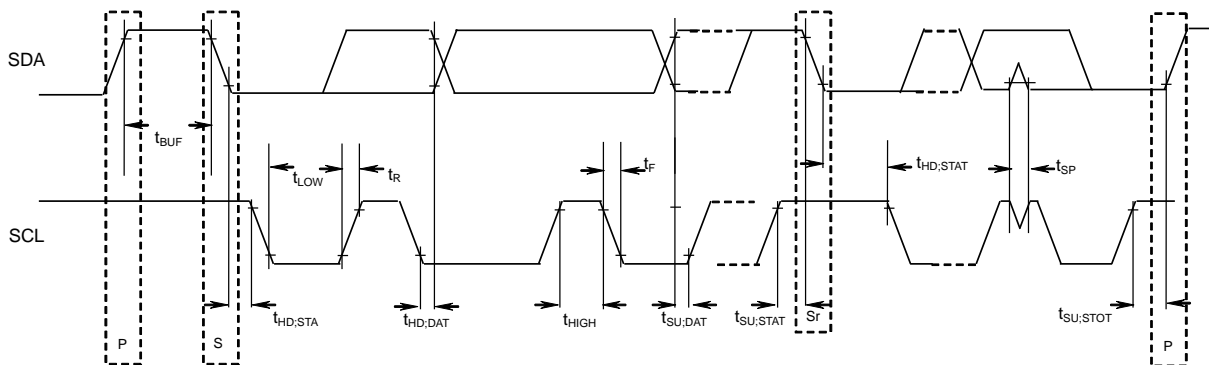
(1) Electrical Specifications and Timing for Bus Lines and I/O Stages

Figure 16. I²C-bus Signal Timing Diagram

Table 1 Characteristics of the SDA and SCL bus lines for I²C-bus devices
(Unless specified, Ta=25°C, VCC=8.5V)

	Parameter	Symbol	Fast-mode I²C-bus		Unit
			Min	Max	
1	SCL clock frequency	f _{SCL}	0	400	kHz
2	Bus free time between a STOP and START condition	t _{BUF}	1.3	-	μs
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	t _{HD,STA}	0.6	-	μs
4	LOW period of the SCL clock	t _{LOW}	1.3	-	μs
5	HIGH period of the SCL clock	t _{HIGH}	0.6	-	μs
6	Set-up time for a repeated START condition	t _{SU,STA}	0.6	-	μs
7	Data hold time	t _{HD,DAT}	0 (Note)	-	μs
8	Data set-up time	t _{SU,DAT}	100	-	ns
9	Set-up time for STOP condition	t _{SU,STO}	0.6	-	μs

All values referred to VIH Min and VIL Max Levels (see Table 2).

(Note) To avoid sending right after the fall-edge of SCL (VIHmin of the SCL signal), the transmitter sets a holding time of 300ns or more for the SDA signal.
About 7(t_{HD,DAT}), 8(t_{SU,DAT}), make it the setup which a margin is fully in.

Table 2 Characteristics of the SDA and SCL I/O stages for I²C-bus devices

	Parameter	Symbol	Fast-mode devices		Unit
			Min	Max	
10	LOW level input voltage	V _{IL}	-0.5	+1	V
11	HIGH level input voltage	V _{IH}	2.3	-	V
12	Pulse width of spikes which must be suppressed by the input filter.	t _{SP}	0	50	ns
13	LOW level output voltage (open drain or open collector) at 3mA sink current	V _{OL1}	0	0.4	V
14	Input current of each I/O pin with an input voltage between 0.4V and 4.5V	I _I	-10	+10	μA

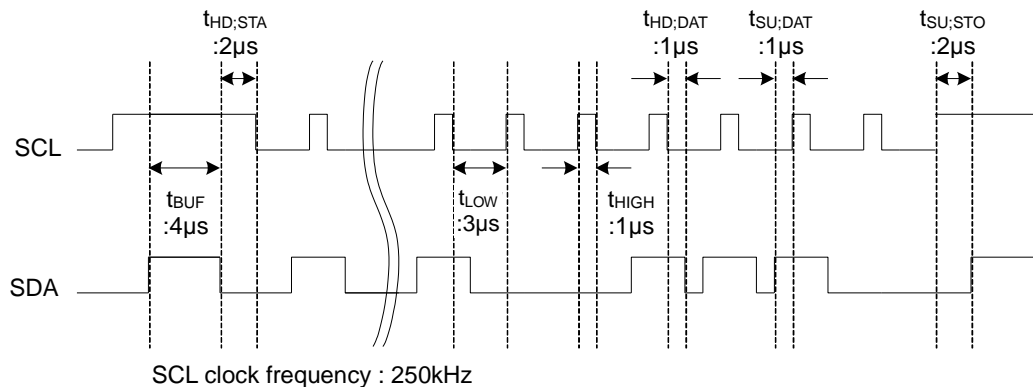


Figure 17. I²C Command Data Transmission Timing Diagram

(2) I²C BUS FORMAT

MSB	LSB	MSB	LSB	MSB	LSB		
S	Slave Address	A	Select Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit
S		= Start condition (Recognition of start bit)					
Slave Address		= Recognition of slave address. The first 7 bits correspond to the slave address.					
		The least significant bit is "L" which corresponds to write mode.					
A		= ACKNOWLEDGE bit (Recognition of acknowledgement)					
Select Address		= Select address corresponding to volume, bass or treble.					
Data		= Data on every volume and tone.					
P		= Stop condition (Recognition of stop bit)					

(3) I²C BUS Interface Protocol

(a) Basic Format

MSB	LSB	MSB	LSB	MSB	LSB		
S	Slave Address	A	Select Address	A	Data	A	P

(b) Automatic Increment (Select Address increases (+1) according to the number of data.)

MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB		
S	Slave Address	A	Select Address	A	Data1	A	Data2	A	...	DataN	A	P	

(Example) ① Data1 shall be set as data of address specified by Select Address.

② Data2 shall be set as data of address specified by Select Address +1.

③ DataN shall be set as data of address specified by Select Address +N-1.

(c) Configuration Unavailable for Transmission (In this case, only Select Address1 is set.)

MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB	MSB	LSB		
S	Slave Address	A	Select Address1	A	Data	A	Select Address 2	A	Data	A	P		

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.

(4) Slave Address

Because the slave address can be changed by the setting of CS, it is possible to use two chips at the same time on identical BUS.

	MSB							LSB	
SEL Voltage Condition	A6	A5	A4	A3	A2	A1	A0	R/W	
GND to 0.2 x V _{CC}	1	0	0	0	0	0	0	0	80H
0.8 x V _{CC} to V _{CC}	1	0	0	0	0	1	0	0	84H

Establish the CS voltage to define the setting.

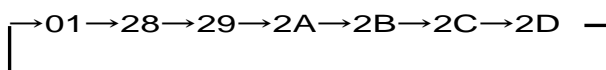
(5) Select Address & Data

Items to be set	Select Address (hex)	MSB	Data						LSB
		D7	D6	D5	D4	D3	D2	D1	D0
Initial Setup 1	01	0	0	0	0	0	0	0	0
Volume 1ch Front	28	Volume Gain / Attenuation							
Volume 2ch Front	29	Volume Gain / Attenuation							
Volume 1ch Rear	2A	Volume Gain / Attenuation							
Volume 2ch Rear	2B	Volume Gain / Attenuation							
Volume 1ch Sub	2C	Volume Gain / Attenuation							
Volume 2ch Sub	2D	Volume Gain / Attenuation							
Test Mode	F0	0	0	0	0	0	0	0	0
System Reset	FE	1	0	0	0	0	0	0	1

 Advanced Switch

(Note)

1. The Advanced Switch works in the latch part while changing from one function to another.
2. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.



Select address 28, 29, 2A, 2B, 2C, 2D (hex)

Gain & ATT	MSB	Volume Gain/Attenuation						LSB
	D7	D6	D5	D4	D3	D2	D1	D0
Prohibition (Note)	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1
	:	:	:	:	:	:	:	:
	0	1	1	0	1	0	0	0
23dB	0	1	1	0	1	0	0	1
22dB	0	1	1	0	1	0	1	0
21dB	0	1	1	0	1	0	1	1
:	:	:	:	:	:	:	:	:
-78dB	1	1	0	0	1	1	1	0
-78dB	1	1	0	0	1	1	1	0
-79dB	1	1	0	0	1	1	1	1
Prohibition (Note)	1	1	0	1	0	0	0	0
	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0
-∞dB	1	1	1	1	1	1	1	1

(Note) Gain is set to “-∞dB” when sending “Prohibition data”.

(6) About Power ON Reset


Initialization inside IC is carried out at one of supply voltage circuits. Initial data is sent to all addresses at supply voltage on. Mute is ON until this initial data is sent.

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Rise Time of VCC	t _{RISE}	20	-	-	μsec	V _{CC} rise time from 0V to 3V
VCC Voltage of Release Power ON Reset	V _{POR}	-	4.1	-	V	

Application Information

1. Volume Gain/Attenuation of the details

(dB)	D7	D6	D5	D4	D3	D2	D1	D0	(dB)	D7	D6	D5	D4	D3	D2	D1	D0
+23	0	1	1	0	1	0	0	1	-29	1	0	0	1	1	1	0	1
+22	0	1	1	0	1	0	1	0	-30	1	0	0	1	1	1	1	0
+21	0	1	1	0	1	0	1	1	-31	1	0	0	1	1	1	1	1
+20	0	1	1	0	1	1	0	0	-32	1	0	1	0	0	0	0	0
+19	0	1	1	0	1	1	0	1	-33	1	0	1	0	0	0	0	1
+18	0	1	1	0	1	1	1	0	-34	1	0	1	0	0	0	1	0
+17	0	1	1	0	1	1	1	1	-35	1	0	1	0	0	0	1	1
+16	0	1	1	1	0	0	0	0	-36	1	0	1	0	0	1	0	0
+15	0	1	1	1	0	0	0	1	-37	1	0	1	0	0	1	0	1
+14	0	1	1	1	0	0	1	0	-38	1	0	1	0	0	1	1	0
+13	0	1	1	1	0	0	1	1	-39	1	0	1	0	0	1	1	1
+12	0	1	1	1	0	1	0	0	-40	1	0	1	0	1	0	0	0
+11	0	1	1	1	0	1	0	1	-41	1	0	1	0	1	0	0	1
+10	0	1	1	1	0	1	1	0	-42	1	0	1	0	1	0	1	0
+9	0	1	1	1	0	1	1	1	-43	1	0	1	0	1	0	1	1
+8	0	1	1	1	1	0	0	0	-44	1	0	1	0	1	1	0	0
+7	0	1	1	1	1	0	0	1	-45	1	0	1	0	1	1	0	1
+6	0	1	1	1	1	0	1	0	-46	1	0	1	0	1	1	1	0
+5	0	1	1	1	1	0	1	1	-47	1	0	1	0	1	1	1	1
+4	0	1	1	1	1	1	0	0	-48	1	0	1	1	0	0	0	0
+3	0	1	1	1	1	1	0	1	-49	1	0	1	1	0	0	0	1
+2	0	1	1	1	1	1	1	0	-50	1	0	1	1	0	0	1	0
+1	0	1	1	1	1	1	1	1	-51	1	0	1	1	0	0	1	1
0	1	0	0	0	0	0	0	0	-52	1	0	1	1	0	1	0	0
-1	1	0	0	0	0	0	0	1	-53	1	0	1	1	0	1	0	1
-2	1	0	0	0	0	0	1	0	-54	1	0	1	1	0	1	1	0
-3	1	0	0	0	0	0	1	1	-55	1	0	1	1	0	1	1	1
-4	1	0	0	0	0	1	0	0	-56	1	0	1	1	1	0	0	0
-5	1	0	0	0	0	1	0	1	-57	1	0	1	1	1	0	0	1
-6	1	0	0	0	0	1	1	0	-58	1	0	1	1	1	0	1	0
-7	1	0	0	0	0	1	1	1	-59	1	0	1	1	1	0	1	1
-8	1	0	0	0	1	0	0	0	-60	1	0	1	1	1	1	0	0
-9	1	0	0	0	1	0	0	1	-61	1	0	1	1	1	1	0	1
-10	1	0	0	0	1	0	1	0	-62	1	0	1	1	1	1	1	0
-11	1	0	0	0	1	0	1	1	-63	1	0	1	1	1	1	1	1
-12	1	0	0	0	1	1	0	0	-64	1	1	0	0	0	0	0	0
-13	1	0	0	0	1	1	0	1	-65	1	1	0	0	0	0	0	1
-14	1	0	0	0	1	1	1	0	-66	1	1	0	0	0	0	1	0
-15	1	0	0	0	1	1	1	1	-67	1	1	0	0	0	0	1	1
-16	1	0	0	1	0	0	0	0	-68	1	1	0	0	0	1	0	0
-17	1	0	0	1	0	0	0	1	-69	1	1	0	0	0	1	0	1
-18	1	0	0	1	0	0	1	0	-70	1	1	0	0	0	1	1	0
-19	1	0	0	1	0	0	1	1	-71	1	1	0	0	0	1	1	1
-20	1	0	0	1	0	1	0	0	-72	1	1	0	0	1	0	0	0
-21	1	0	0	1	0	1	0	1	-73	1	1	0	0	1	0	0	1
-22	1	0	0	1	0	1	1	0	-74	1	1	0	0	1	0	1	0
-23	1	0	0	1	0	1	1	1	-75	1	1	0	0	1	0	1	1
-24	1	0	0	1	1	0	0	0	-76	1	1	0	0	1	1	0	0
-25	1	0	0	1	1	0	0	1	-77	1	1	0	0	1	1	0	1
-26	1	0	0	1	1	0	1	0	-78	1	1	0	0	1	1	1	0
-27	1	0	0	1	1	0	1	1	-79	1	1	0	0	1	1	1	1
-28	1	0	0	1	1	1	0	0	-∞	1	1	1	1	1	1	1	1

 : Initial condition

2. Application Circuit Diagram

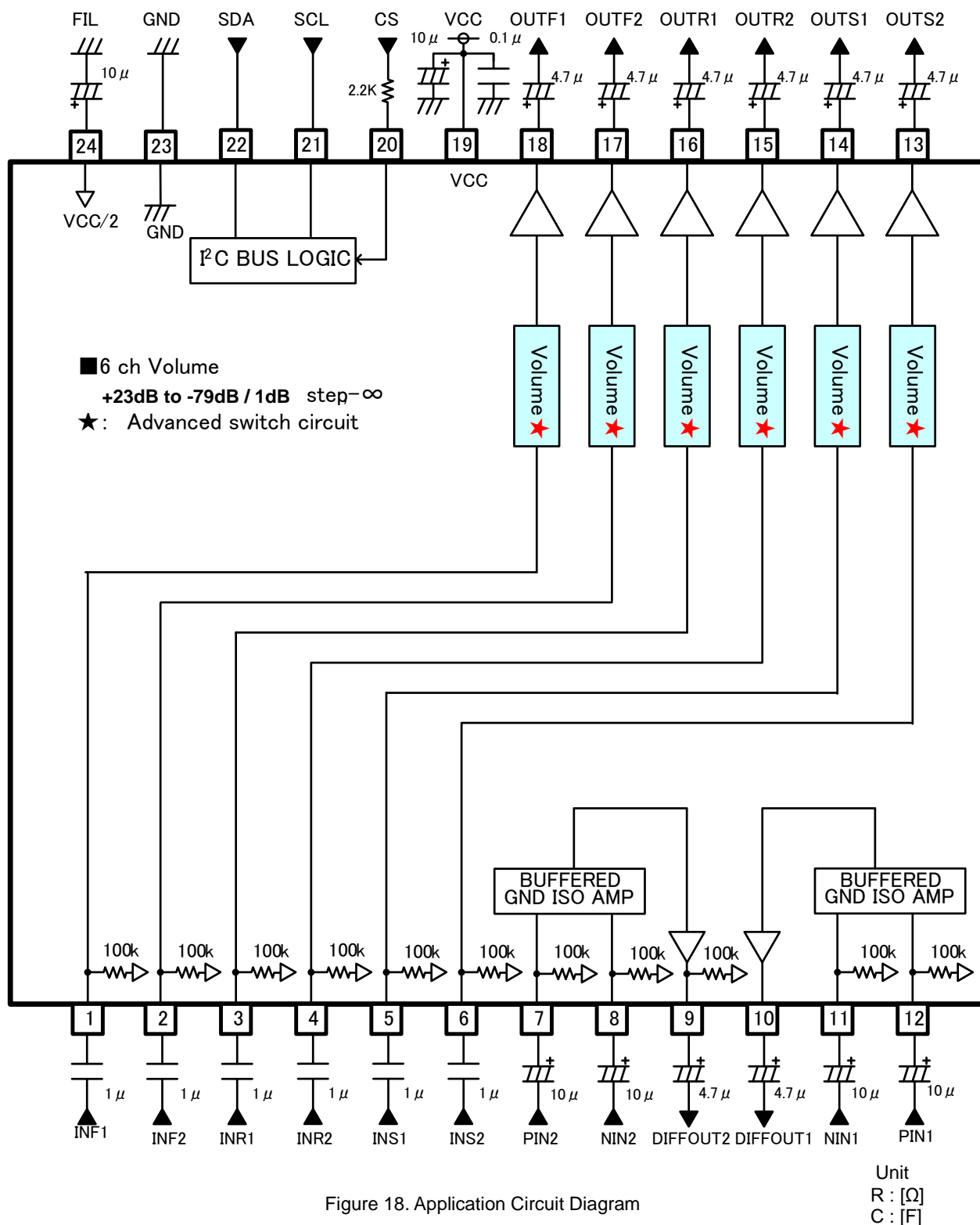


Figure 18. Application Circuit Diagram

Notes on wiring

- ① Please connect the decoupling capacitor of a power supply in the shortest distance as much as possible to GND.
- ② Lines of GND shall be one-point connected.
- ③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
- ④ Lines of SCL and SDA of I²C BUS shall not be parallel if possible.
The lines shall be shielded, if they are adjacent to each other.
- ⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.

Power Dissipation

About the thermal design by the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

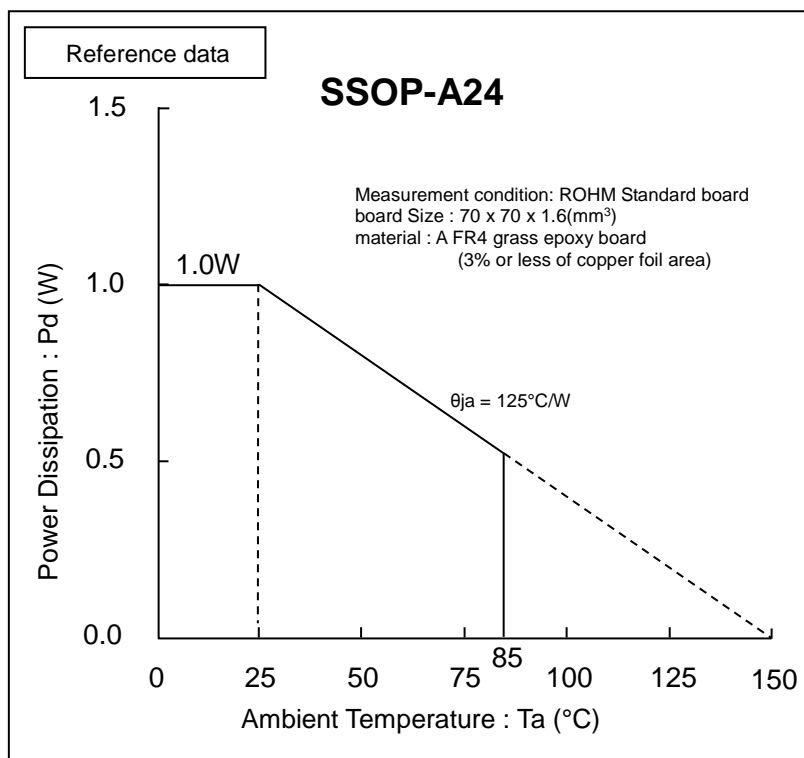
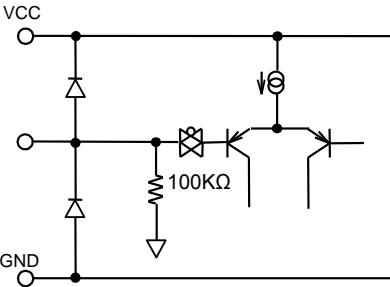
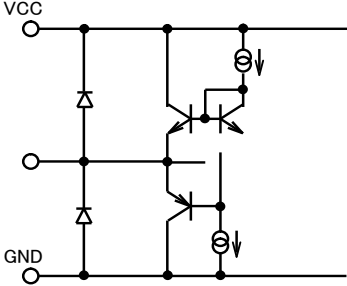
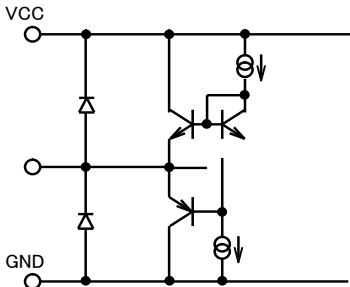


Figure 19. Temperature Derating Curve (SSOP-A24)

(Note) Values are actual measurements and are not guaranteed.

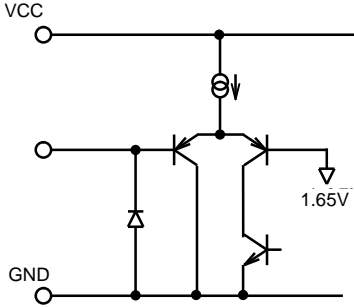
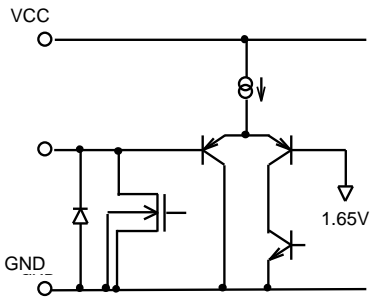
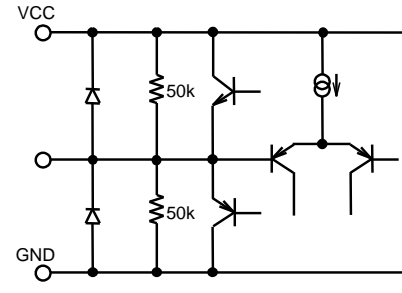
Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalent Circuits

Terminal No.	Terminal Voltage	Equivalent Circuit	Terminal Description
INF1 INF2 INR1 INR2 INS1 INS2 PIN2 NIN2 NIN1 PIN1	4.25		Signal input terminal. The input impedance is 100kΩ (typ).
DIFOUT2 DIFOUT1 OUTS2 OUTS1 OUTR2 OUTR1 OUTF2 OUTF1	4.25		Fader output terminal.
CS	-		Slave address selection terminal. “CS” is “High” to slave address “84 H” “CS” is “Low” to slave address “80 H”

The values in the input/output equivalent circuits are reference values only and are not guaranteed.

I/O Equivalent Circuits – continued

Terminal Name	Terminal Voltage	Equivalent Circuit	Terminal Description
VCC	8.5		Power supply terminal.
SCL	-		Clock input terminal of I ² C BUS communication.
SDA	-		Data input of I ² C BUS communication.
GND	0		Ground terminal.
FIL	4.25		Voltage terminal for reference bias of analog signal system. The simple pre-charge circuit and simple discharge circuit for an external capacitor are built in.

The values in the input/output equivalent circuits are reference values only and are not guaranteed.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

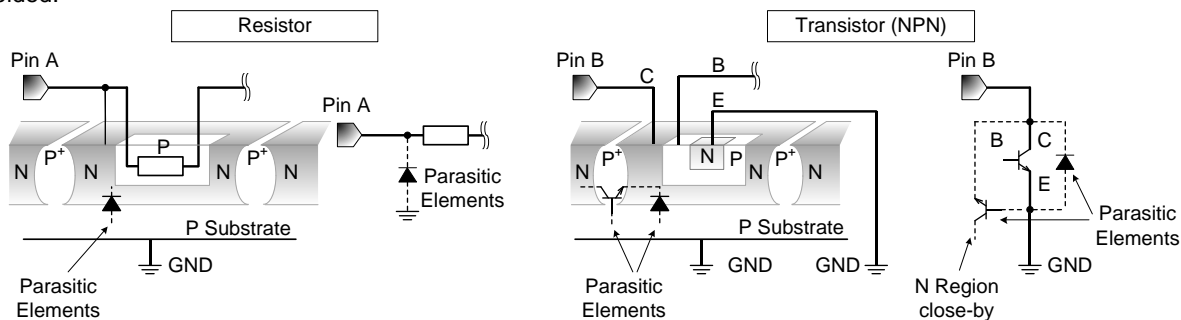
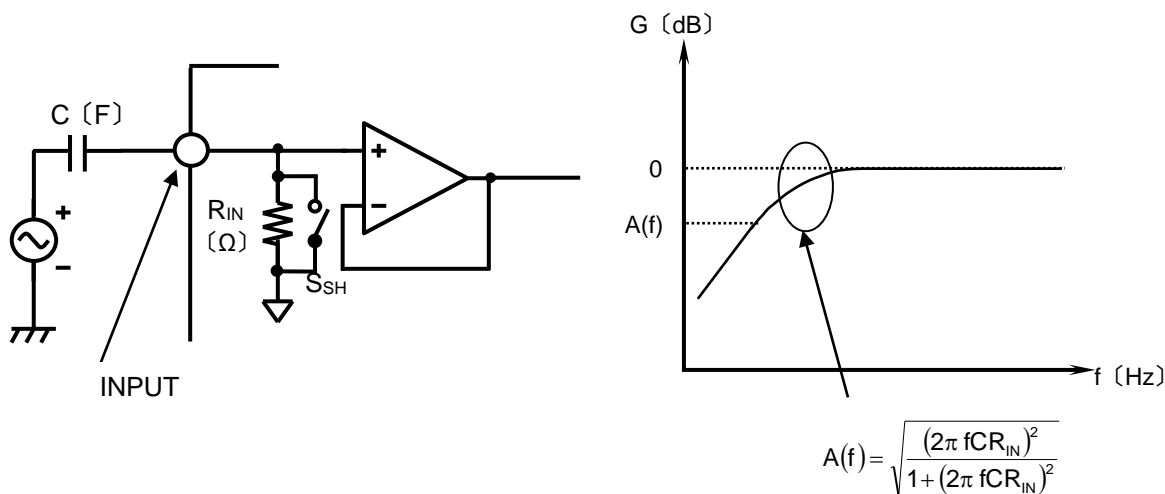


Figure 20. Example of monolithic IC structure

13. About a Signal Input Part

About Input Coupling Capacitor Constant Value

The constant value of input coupling capacitor C(F) is decided with respect to the input impedance $R_{IN}(\Omega)$ at the input signal terminal of the IC. The first HPF characteristic of RC is composed.



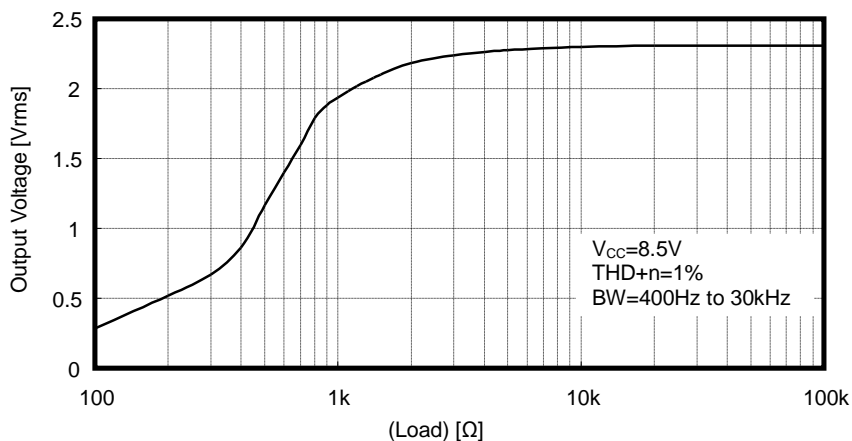
Operational Notes – continued

14. About Output Load Characteristics

The usages of output load are below (reference). Please use more than 10[k Ω](TYP) load.

Output pin on target

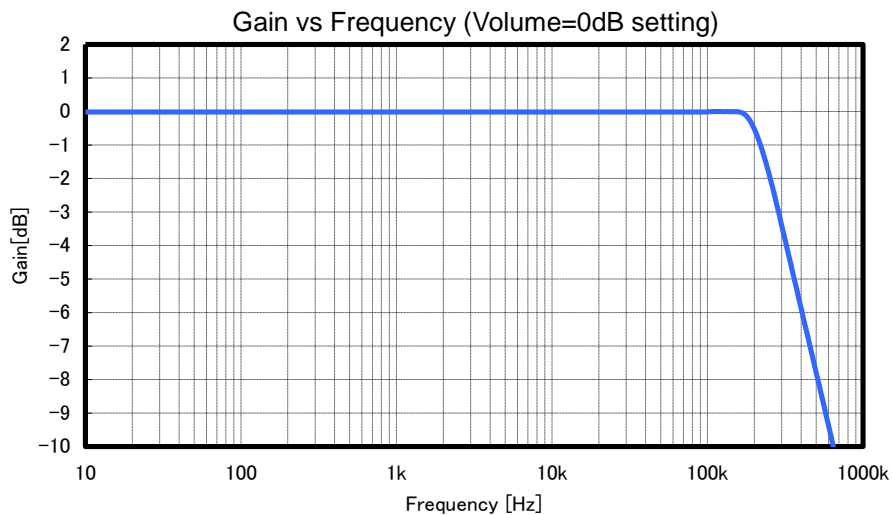
Pin Name	Pin name	Pin name	Pin name
OUTF1	OUTR1	OUTS1	DIFOUT1
OUTF2	OUTR2	OUTS2	DIFOUT2



Output Load Characteristic at $V_{CC}=8.5V$ (Reference)

15. Frequency Characteristic at Large Output Level

High slew-rate amplifiers are used for high quality sound. This IC corresponds to “192kHz sampling on DVD-Audio” which is highest quality. Output level is “2Vrms, 192kHz flat (typ)”.
(See the below graph (reference)).

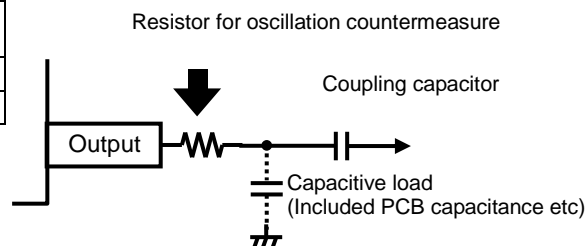


Operational Notes – continued

16. Oscillation Countermeasure for GND Isolation Amplifier Outputs

Using higher capacitor than 10pF at GND isolation amplifier outputs (DIFOUT1, DIFOUT2) may cause oscillation. As oscillation countermeasure, insert resistor in series to terminal directly as below.

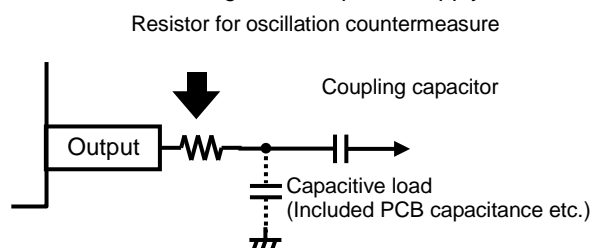
Capacitance	Resistor in series to terminal directly
$C < 10\text{pF}$	Not necessary
$10 < C < 100\text{pF}$	220Ω



17. Oscillation Countermeasure for Volume Outputs at Power Supply ON/OFF

If using higher capacitor than 22pF at volume outputs, oscillation may occur for a moment when turning ON/OFF power supply (when V_{CC} is about 3V to 4V). As oscillation countermeasure, insert resistor in series to terminal directly as below, and set volume output mute outside this device when turning ON/OFF power supply.

Capacitance	Resistor in series to terminal directly
$C < 22\text{pF}$	Not necessary
$22 < C < 220\text{pF}$	220Ω

18. I²C BUS Transferring Data

[1] Types of Data Transfer

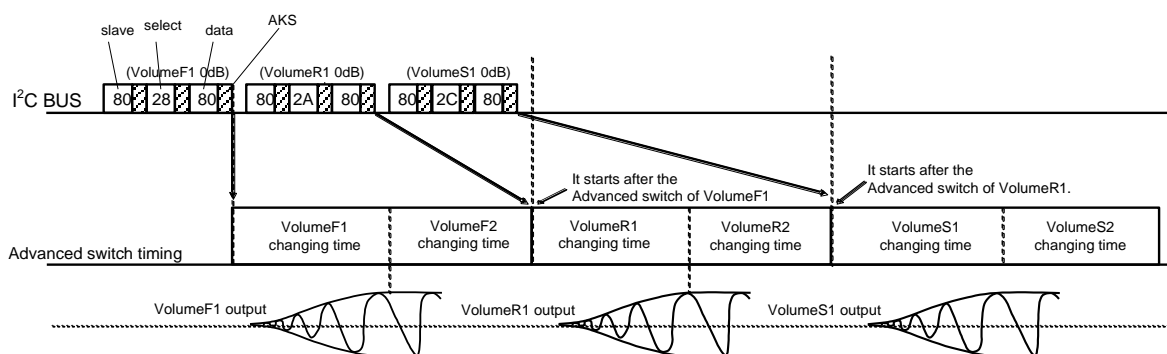
1-1. The data transfer without Advanced Switch (data transfer without data latching format) does not have regulations on transferring data.

1-2. The data transfer with Advanced Switch (data transfer with data latching format) does not have regulations on transferring data too. But Advanced Switch data transfer follows the order in [2]

[2] Advanced Switch Data Transfer

2-1. The timing chart of Advanced Switch data transfer is as follows.

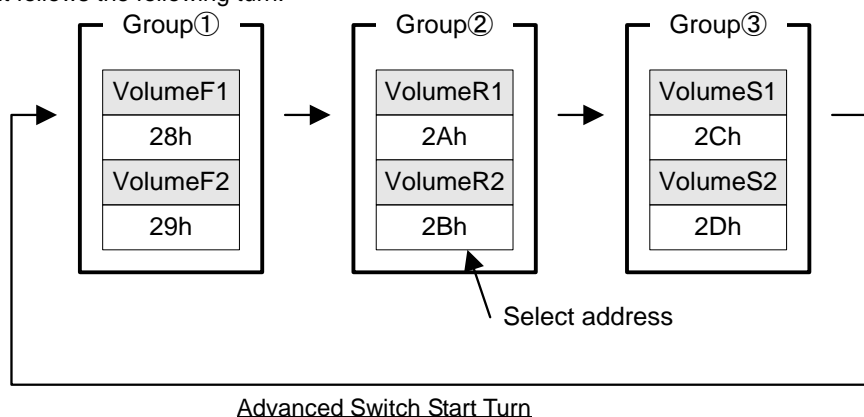
■ Data transfer example 1



It is the same even if it transfers data in auto increment mode.

Operational Notes – continued

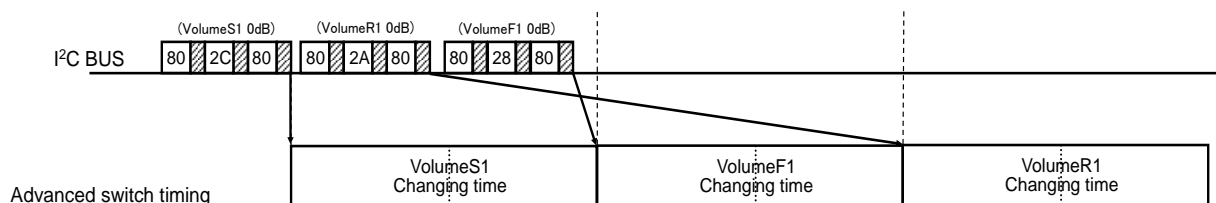
There are no timing regulations in I²C BUS transferring data. But the changing time starts after the end of the present change. In addition, the timing of Advanced Switch is not dependent on transferring data turn. Instead, it follows the following turn.



(Note) The block in the same group can start the Advanced Switch at the same time.

■ Data Transfer Example 2

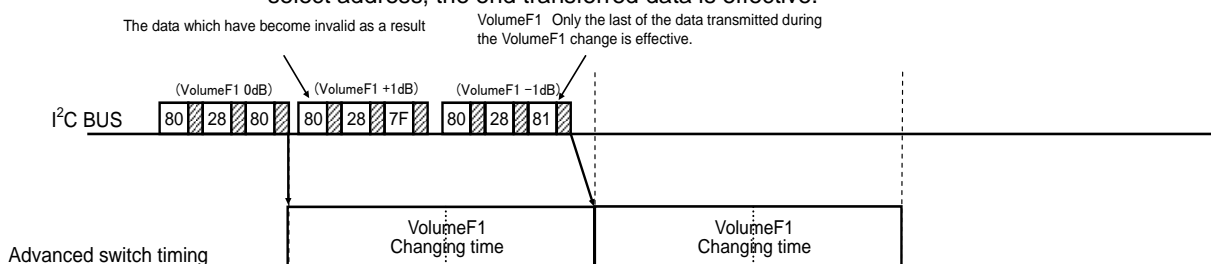
The data transfer turn differs from the actual change turn as shown below.



Please transfer data after the present Advanced Switch, if it wants to make a transferring data turn and Advanced Switch turn the same.

■ Data Transfer Example 3

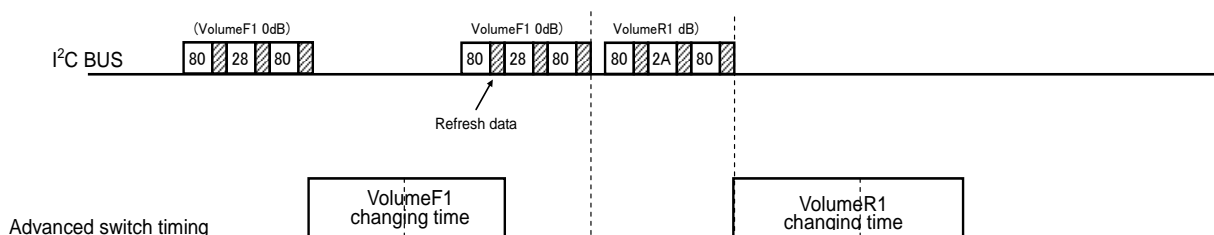
Priority is given to the data of the same select address when it is transferred to the timing which Advanced Switch has not ended. In addition, when two or more data are transferred to the same select address, the end transferred data is effective.



■ Data Transfer Example 4

Refresh data is the same as the present setup data, therefore Advanced Switch does not change.

The gain change data of other channels are transferred after refresh data as shown below.



Operational Notes – continued

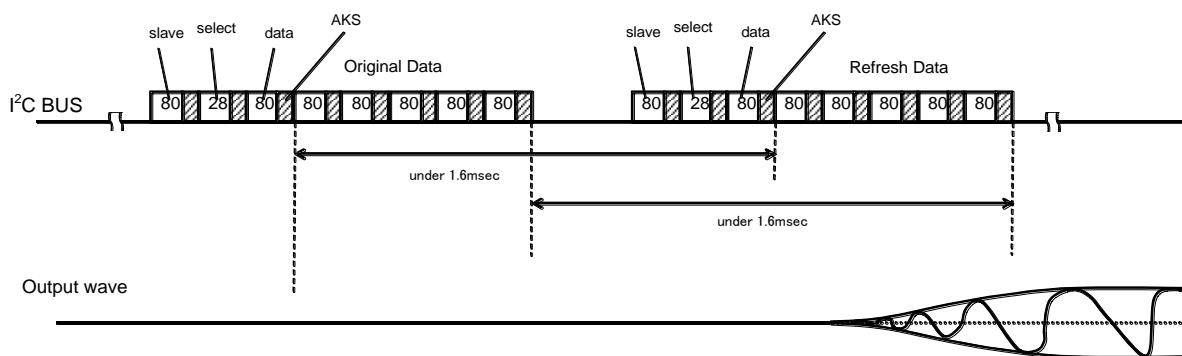
[3] Attention of Transferring Data

BD3460FS cannot set the data transfer from a microcomputer correctly on very rare occasions. In such cases, the following phenomenon may occur.

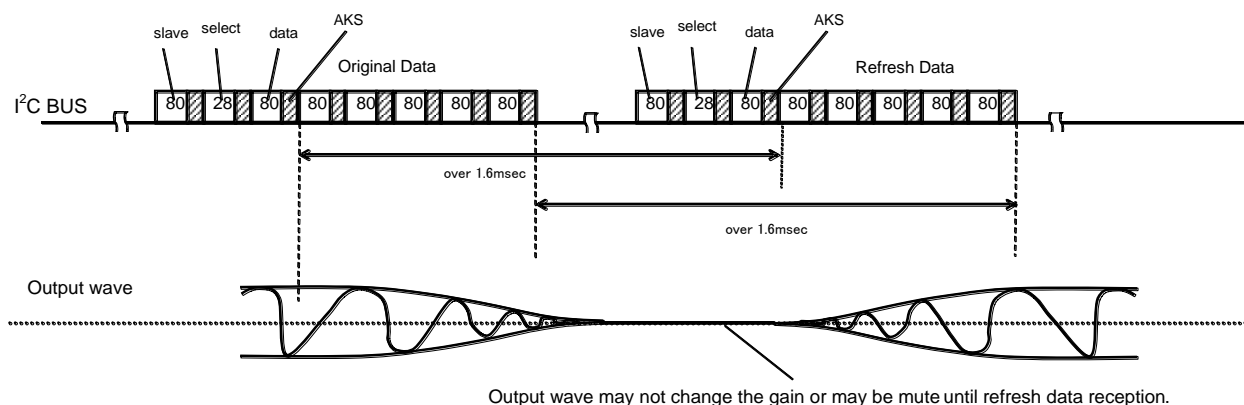
1. Volume gain does not change.
2. Volume gain changes to MUTE.

Therefore, the data transfer from a microcomputer should send data as shown in the following conditions.

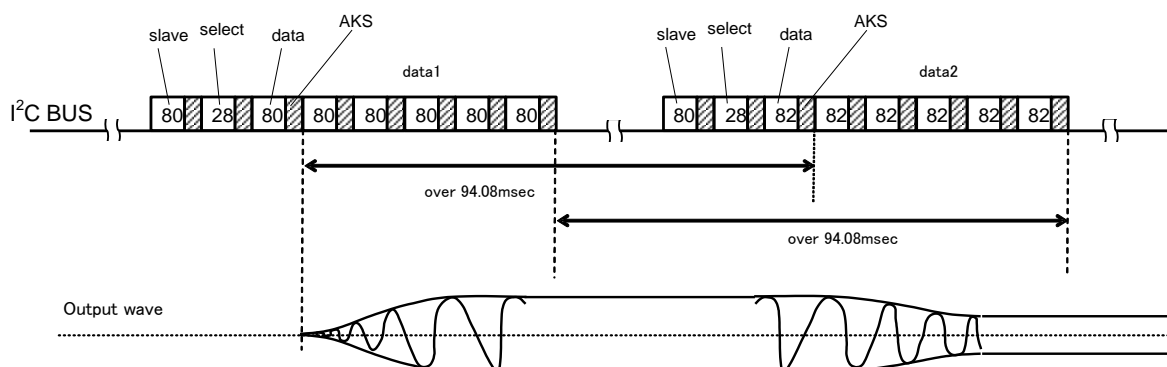
- ① When the Volume change data send, please send the same data twice as below.



If Refresh data can't be sent like ① timing, the output wave may be mute momentarily.



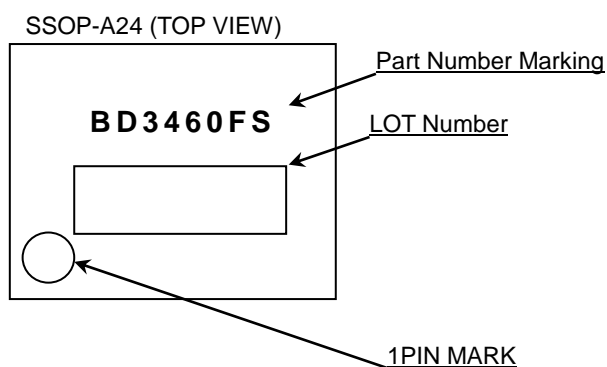
- ② If Volume change data can send over 94.08msec interval transferring data, there is no need to send Refresh data.



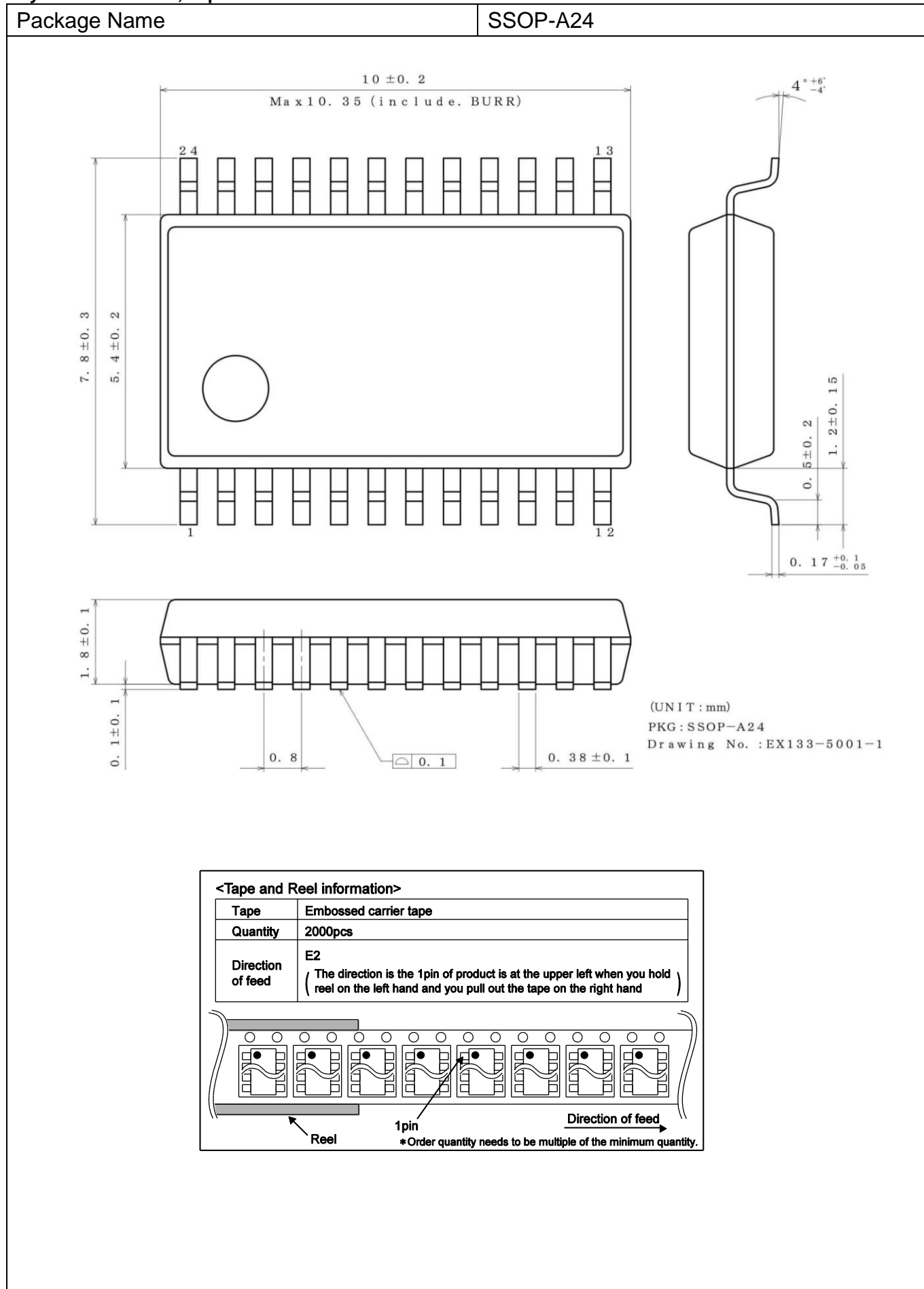
Ordering Information

B D 3 4 6 0 F S							-	E 2
Part Number							Package FS: SSOP-A24	Packaging and forming specification E2: Embossed tape and reel

Marking Diagram



Physical Dimension, Tape and Reel Information



Revision History

Date	Revision	Changes
16.Dec.2015	001	New Release

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