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November 1992 Revised April 2005

74VHC244 Octal Buffer/Line Driver with 3-STATE Outputs

General Description

The VHC244 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC244 is a non-inverting 3-STATE buffer having two active-LOW output enables. These devices are designed to be used as 3-STATE memory address drivers, clock drivers, and bus oriented transmitter/receivers.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

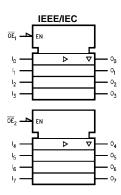
- High Speed: t_{PD} = 3.9ns (typ) at V_{CC} = 5V
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Power down protection is provided on all inputs
- Low noise: V_{OLP} = 0.6V (typ)
- Low power dissipation: $I_{CC} = 4 \mu A \text{ (max)} @ T_A = 25 ^{\circ}C$
- Pin and function compatible with 74HC244

Ordering Code:

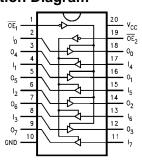
Order Number	Package Number	Package Description
74VHC244M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC244SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC244MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC244N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code. Pb-Free package per JEDEC J-STD-020B.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
I ₀ –I ₇	Inputs
O ₀ –O ₇	3-STATE Outputs

Truth Tables

Inp	uts	Outputs				
OE ₁	I _n	(Pins 12, 14, 16, 18)				
L	L	L				
L	Н	Н				
Н	Х	Z				

Inp	uts	Outputs					
OE ₂	l _n	(Pins 3, 5, 7, 9)					
L	L	L					
L	Н	Н					
Н	Х	Z					

H = HIGH Voltage Level
L = LOW Voltage Level
I = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 1)

DC V $_{\rm CC}$ /GND Current (I $_{\rm CC}$) ± 75 mA Storage Temperature (T $_{\rm STG}$) -65°C to +150°C

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Recommended Operating Conditions (Note 2)

Input Rise and Fall Time (t_r, t_f)

$$\begin{split} \text{V}_{\text{CC}} &= 3.3 \text{V} \pm 0.3 \text{V} & \text{0 ns/V} \sim 100 \text{ ns/V} \\ \text{V}_{\text{CC}} &= 5.0 \text{V} \pm 0.5 \text{V} & \text{0 ns/V} \sim 20 \text{ ns/V} \end{split}$$

Note 1: Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	CC T _A = 25°C			T _A = -40°	C to +85°C	Units	Conditions	
Symbol		(V)	Min	Тур	Max	Min	Max	Units	Conditions	
V _{IH}	HIGH Level	2.0	1.5			1.5		V		
	Input Voltage	3.0 - 5.5	0.7 V _{CC}			0.7 V _{CC}		V		
V _{IL}	LOW Level	2.0			0.5		0.5	V		
	Input Voltage	3.0 - 5.5			$0.3 V_{\rm CC}$		$0.3 V_{\rm CC}$	V		
V _{OH}	HIGH Level	2.0	1.9	2.0		1.9			$V_{IN} = V_{IH}$ $I_{OH} = -50 \mu A$	
	Output Voltage	3.0	2.9	3.0		2.9		V	or V _{IL}	
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V	$I_{OH} = -4 \text{ mA}$	
		4.5	3.94			3.80		V	$I_{OH} = -8 \text{ mA}$	
V _{OL}	LOW Level	2.0		0.0	0.1		0.1		$V_{IN} = V_{IH}$ $I_{OL} = 50 \mu A$	
	Output Voltage	3.0		0.0	0.1		0.1	V	or V _{IL}	
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V	$I_{OL} = 4 \text{ mA}$	
		4.5			0.36		0.44	V	$I_{OL} = 8 \text{ mA}$	
I _{OZ}	3-STATE Output	5.5			±0.25		±2.5	μΑ	$V_{IN} = V_{IH}$ or V_{IL}	
Off-State Current									$V_{OUT} = V_{CC}$ or GND	
I _{IN}	Input Leakage Current	put Leakage Current 0 - 5.5			±0.1		±1.0	μΑ	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current				4.0		40.0	μА	V _{IN} = V _{CC} or GND	

Noise Characteristics

Symbol	Parameter	v _{cc}	T _A = 25°C		Units	Conditions		
	i didilicio	(V)	Тур	Limits	Omio	Conditions		
V _{OLP}	Quiet Output Maximum	5.0	0.6	0.9	V	C _L = 50 pF		
(Note 3)	Dynamic V _{OL}							
V _{OLV}	Quiet Output Minimum	5.0	-0.6	-0.9	V	C _L = 50 pF		
(Note 3)	Dynamic V _{OL}							
V _{IHD}	Minimum HIGH Level	5.0		3.5	V	C _L = 50 pF		
(Note 3)	Dynamic Input Voltage							
V _{ILD}	Maximum HIGH Level	5.0		1.5	V	C _L = 50 pF		
(Note 3)	Dynamic Input Voltage							

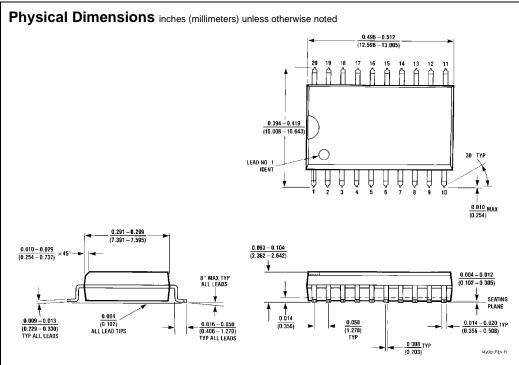
Note 3: Parameter guaranteed by design.

AC Electrical Characteristics

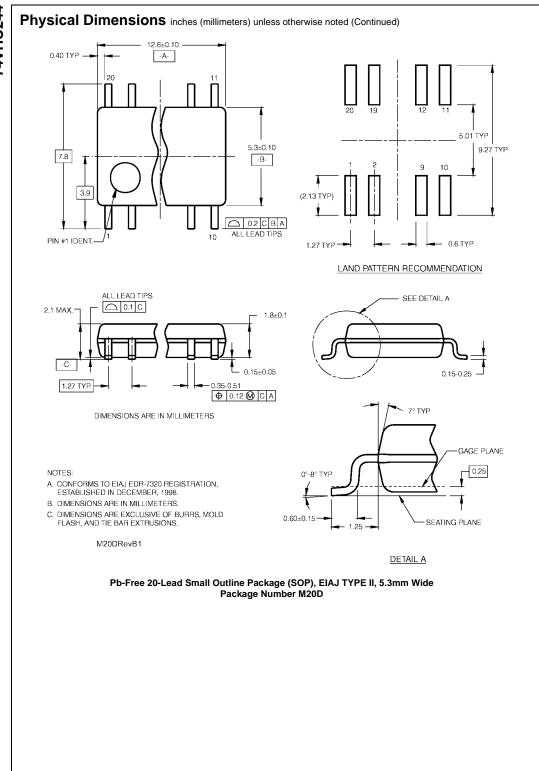
Symbol	Parameter	V _{CC}			$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			Conditions		
		(V)	Min	Тур	Max	Min	Max	Units	Conc	antionis
t _{PLH}	Propagation Delay	3.3 ± 0.3		5.8	8.4	1.0	10.0	ns		$C_L = 15 pF$
t _{PHL}	Time			8.3	11.9	1.0	13.5	115		$C_L = 50 \text{ pF}$
		5.0 ± 0.5		3.9	5.5	1.0	6.5	ns	İ	C _L = 15 pF
				5.4	7.5	1.0	8.5	115		$C_L = 50 pF$
t _{PZL}	3-STATE Output	3.3 ± 0.3		6.6	10.6	1.0	12.5	ns		$C_L = 15 pF$
t _{PZH}	Enable Time			9.1	14.1	1.0	16.0			$C_L = 50 \text{ pF}$
		5.0 ± 0.5		4.7	7.3	1.0	8.5	no	KL = 1 K22	$C_L = 15 pF$
		3.0 ± 0.5		6.2	9.3	1.0	10.5	ns		$C_L = 50 \text{ pF}$
t _{PLZ}	3-STATE Output	3.3 ± 0.3		10.3	14.0	1.0	16.0	ns	$R_L = 1 \text{ k}\Omega$	C _L = 50 pF
t_{PHZ}	Disable Time	5.0 ± 0.5		6.7	9.2	1.0	10.5	115		$C_L = 50 pF$
toslh	Output to Output	3.3 ± 0.3			1.5		1.5	ns	(Note 4)	$C_L = 50 \text{ pF}$
toshl	Skew	5.0 ± 0.5			1.0		1.0	115		$C_L = 50 \text{ pF}$
C _{IN}	Input Capacitance			4	10		10	pF	V _{CC} = Ope	n
C _{OUT}	Output Capacitance			6				pF	V _{CC} = 5.0\	/
C _{PD}	Power Dissipation Capacitance			19				pF	(Note 5)	

 $\textbf{Note 4:} \ \mathsf{Parameter guaranteed by design.} \ t_{\mathsf{OSLH}} = |t_{\mathsf{PLHmax}} - t_{\mathsf{PLHmin}}|; \ t_{\mathsf{OSHL}} = |t_{\mathsf{PHLmax}} - t_{\mathsf{PHLmin}}|.$

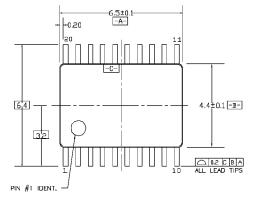
Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (OPR.) = C_{PD} * V_{CC} * f_{IN} + I_{CO} /8 (per bit).

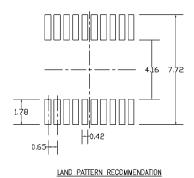


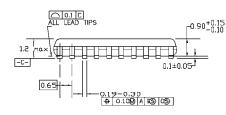
20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)











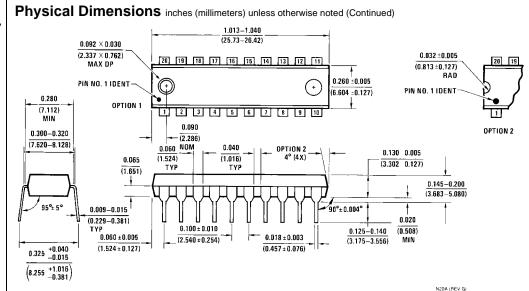
NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

R0.09min GAGE PLANE - 8°7 -0.6±0.1-0.09min DETAIL A

MTC20REVD1

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

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