Data Sheet April 26, 2006 FN2950.3

CMOS Serial Controller Interface

The Intersil 82C52 is a high performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG) on a single chip. Utilizing the Intersil advanced Scaled SAJI IV CMOS process, the 82C52 will support data rates up to 1M baud asynchronously with a 16X clock (16MHz clock frequency).

The on-chip Baud Rate Generator can be programmed for any one of 72 different baud rates using a single industry standard crystal or external frequency source. A unique pre-scale divide circuit has been designed to provide standard RS-232-C baud rates when using any one of three industry standard crystals (1.8432MHz, 2.4576MHz, or 3.072MHz).

A programmable buffered clock output (CO) is available and can be programmed to provide either a buffered oscillator or 16X baud rate clock for general purpose system usage.

Ordering Information

1M BAUD	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
CP82C52	CP82C52	0 to +70	PDIP	E28.6
CP82C52Z (Note)	CP82C52Z	0 to +70	PDIP (Pb-Free)**	E28.6
IP82C52	IP82C52	-40 to +85	PDIP	E28.6
CS82C5296	CS82C52	0 to +70	PLCC (Tape & Reel)	N28.45
CS82C52Z* (Note)	CS82C52Z	0to +70	PLCC (Pb-Free)	N28.45
IS82C52	IS82C52	-40 to +85	PLCC	N28.45
IS82C52Z* (Note)	IS82C52Z	-40 to +85	PLCC (Pb-Free)	N28.45
ID82C52	ID82C52	-40 to +85	CERDIP	F28.6
MD82C52/B	MD82C52/B	-55 to +125		F28.6
8501501XA	8501501XA		SMD#	F28.6
MR82C52/B		-55 to +125	CLCC	J28.A
85015013A	85015013A		SMD#	J28.A

*Add "96" suffix for tape and reel.

**Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Single Chip UART/BRG
- DC to 16MHz (1M Baud) Operation
- Crystal or External Clock Input
- On-Chip Baud Rate Generator - 72 Selectable Baud Rates
- Interrupt Mode with Mask Capability
- Microprocessor Bus Oriented Interface
- 80C86 Compatible
- Single +5V Power Supply
- Low Power Operation . . . . . 1mA/MHz Typ
- Modem Interface
- Line Break Generation and Detection
- Operating Temperature Range:
  - C82C52 . . . . . .0°C to +70°C
  - I82C52 . . . . . -40°C to +85°C
  - M82C52 . . . . . -55°C to +125°C
- Pb-Free Plus Anneal Available (RoHS Compliant)

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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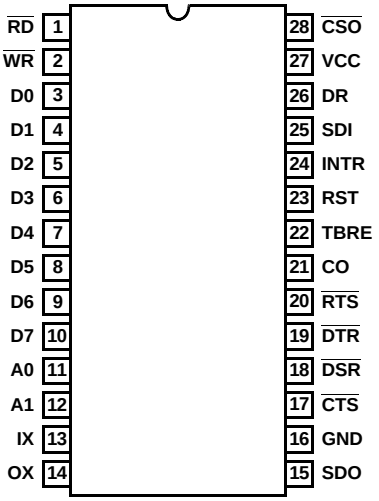
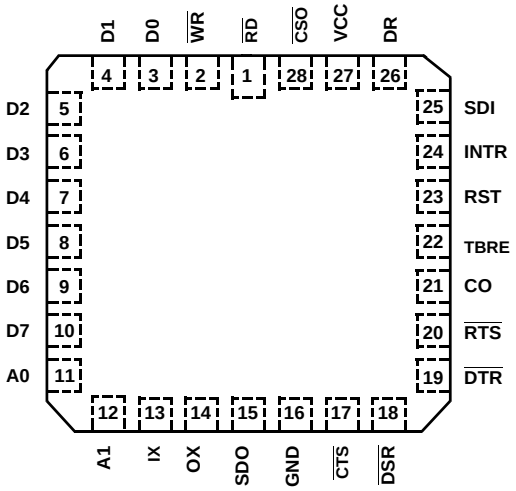
Pinouts

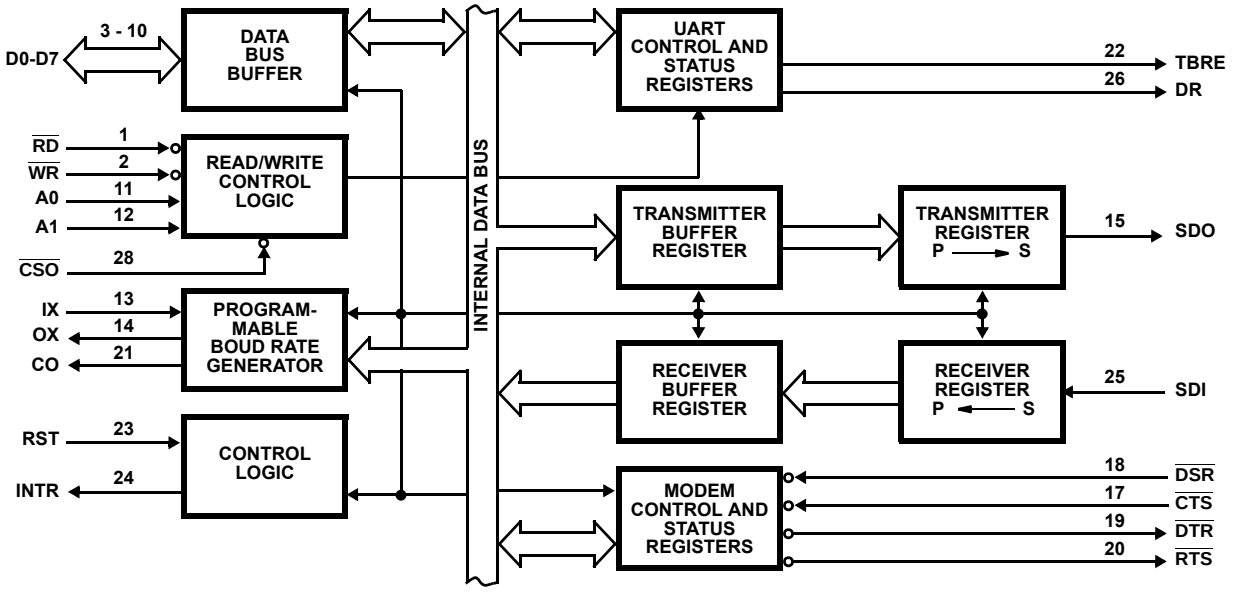
82C52 (PDIP, CERDIP)
TOP VIEW



82C52 (PLCC, CLCC)
TOP VIEW



Block Diagram



Pin Description

SYMBOL	PIN NO.	TYPE	ACTIVE LEVEL	DESCRIPTION
$\overline{RD}$	1	I	Low	READ: The $\overline{RD}$ input causes the 82C52 to output data to the data bus (D0-D7). The data output depends upon the state of the address inputs (A0-A1). $\overline{CS0}$ enables the $\overline{RD}$ input.
$\overline{WR}$	2	I	Low	WRITE: The $\overline{WR}$ input causes data from the data bus (D0-D7) to be input to the 82C52. Addressing and chip select action is the same as for read operations.
D0-D7	3-10	I/O	High	DATA BITS 0-7: The Data Bus provides eight, three-state input/output lines for the transfer of data, control and status information between the 82C52 and the CPU. For character formats of less than 8 bits, the corresponding D7, D6 and D5 are considered “don't cares” for data WRITE operations and are 0 for data READ operations. These lines are normally in a high impedance state except during read operations. D0 is the Least Significant Bit (LSB) and is the first serial data bit to be received or transmitted.
A0, A1	11, 12	I	High	ADDRESS INPUTS: The address lines select the various internal registers during CPU bus operations.
IX, OX	13, 14	I/O		CRYSTAL/CLOCK: Crystal connections for the internal Baud Rate Generator. IX can also be used as an external clock input in which case OX should be left open.
SDO	15	O	High	SERIAL DATA OUTPUT: Serial data output from the 82C52 transmitter circuitry. A Mark (1) is a logic one (high) and Space (0) is logic zero (low). SD0 is held in the Mark condition when $\overline{CTS}$ is false, when RST is true, when the Transmitter Register is empty, or when in the Loop Mode.
GND	16		Low	GROUND: Power supply ground connection.
$\overline{CTS}$	17	I	Low	CLEAR TO SEND: The logical state of the $\overline{CTS}$ line is reflected in the $\overline{CTS}$ bit of the Modem Status Register. Any change of state in $\overline{CTS}$ causes INTR to be set true when INTEN and MIEN are true. A false level on $\overline{CTS}$ will inhibit transmission of data on the SD0 output and will hold SD0 in the Mark (high) state. If $\overline{CTS}$ goes false during transmission, the current character being transmitted will be completed. $\overline{CTS}$ does not affect Loop Mode operation.
$\overline{DSR}$	18	I	Low	DATA SET READY: The logical state of the $\overline{DSR}$ line is reflected in the Modem Status Register. Any change of state of $\overline{DSR}$ will cause INTR to be set if INTEN and MIEN are true. The state of this signal does not affect any other circuitry within the 82C52.
$\overline{DTR}$	19	O	Low	DATA TERMINAL READY: The $\overline{DTR}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the Modem Control Register (MCR). This signal is cleared (high) by writing a logic 0 in the $\overline{DTR}$ bit in the MCR or whenever a reset (RST = high) is applied to the 82C52.
$\overline{RTS}$	20	O	Low	REQUEST TO SEND: The $\overline{RTS}$ signal can be set (low) by writing a logic 1 to the appropriate bit in the MCR. This signal is cleared (high) by writing a logic 0 to the $\overline{RTS}$ bit in the MCR or whenever a reset (RST = high) is applied to the 82C52.
CO	21	O		CLOCK OUT: This output is user programmable to provide either a buffered IX output or a buffered Baud Rate Generator (16X) clock output. The buffered IX (Crystal or external clock source) output is provided when the Baud Rate Select Register (BRSR) bit 7 is set to a zero. Writing a logic one to BRSR bit 7 causes the CO output to provide a buffered version of the internal Baud Rate Generator clock which operates at sixteen times the programmed baud rate. On reset D7 (CO select) is reset to 0.
TBRE	22	O	High	TRANSMITTER BUFFER REGISTER EMPTY: The TBRE output is set (high) whenever the Transmitter Buffer Register (TBR) has transferred its data to the Transmit Register. Application of a reset (RST) to the 82C52 will also set the TBRE output. TBRE is cleared (low) whenever data is written to the TBR.
RST	23	I	High	RESET: The RST input forces the 82C52 into an “Idle” mode in which all serial data activities are suspended. The Modem Control Register (MCR) along with its associated outputs are cleared. The UART Status Register (USR) is cleared except for the TBRE and TC bits, which are set. The 82C52 remains in an “Idle” state until programmed to resume serial data activities. The RST input is a Schmitt triggered input.
INTR	24	O	High	INTERRUPT REQUEST: The INTR output is enabled by the INTEN bit in the Modem Control Register (MCR). The MIEN bit selectively enables modem status changes to provide an input to the INTR logic. Figure 9 in Design Information shows the overall relationship of these interrupt control signals.

Pin Description (Continued)

SYMBOL	PIN NO.	TYPE	ACTIVE LEVEL	DESCRIPTION
SDI	25	I	High	SERIAL DATA INPUT: Serial data input to the 82C52 receiver circuits. A Mark (1) is high, and a Space (0) is low. Data inputs on SDI are disabled when operating in the loop mode or when RST is true.
DR	26	O	High	DATA READY: A true level indicates that a character has been received, transferred to the RBR, and is ready for transfer to the CPU. DR is reset on a data READ of the Receiver Buffer Register (RBR) or when RST is true.
V_{CC}	27		High	V_{CC}: +5V positive power supply pin. A 0.1µF decoupling capacitor from V_{CC} (Pin 27) to GND (Pin 16) is recommended.
$\overline{CS0}$	28	I	Low	CHIP SELECT: The chip select input acts as an enable signal for the $\overline{RD}$ and $\overline{WR}$ input signals.

Reset

During and after power-up, the 82C52 Reset Input (RST) must be held high for at least two IX clock cycles in order to initialize and drive the 82C52 circuits to an idle mode until proper programming can be done. A high on RST causes the following events to occur

- Resets the internal Baud Rate Generator (BRG) circuit clock counters and bit counters. The Baud Rate Select Register (BRSR) is not affected (except for bit 7 which is reset to 0).
- Clears the UART Status Register (USR) except for Transmission Complete (TC) and Transmit Buffer Register Empty (TBRE) which are set. The Modem Control Register (MCR) is also cleared. All of the discrete lines, memory elements and miscellaneous logic associated with these register bits are also cleared or turned off. Note that the UART Control Register (UCR) is not affected.

Following removal of the reset condition (RST = low), the 82C52 remains in the idle mode until programmed to its desired system configuration.

Programming The 82C52

The complete functional definition of the 82C52 is programmed by the systems software. A set of control words (UCR, BRSR and MCR) must be sent out by the CPU to initialize the 82C52 to support the desired communication format. These control words will program the character length, number of stop bits, even/odd/no parity, baud rate, etc. Once programmed, the 82C52 is ready to perform its communication functions.

The control registers can be written to in any order. However, the MCR should be written to last because it controls the interrupt enables, modem control outputs and the receiver enable bit. Once the 82C52 is programmed and operational, these registers can be updated any time the 82C52 is not immediately transmitting or receiving data.

Table 1. Shows the control signals required to access 82C52 internal registers.

UART Control Register (UCR)

The UCR is a write only register which configures the UART transmitter and receiver circuits. Data bits D7 and D6 are not used but should always be set to a logic zero (0) in order to insure software compatibility with future product upgrades. During the Echo Mode, the transmitter always repeats the received word and parity, even when the UCR is programmed with different or no parity. See Figure 1.

TABLE 1.

$\overline{CS0}$	A1	A0	$\overline{WR}$	$\overline{RD}$	OPERATION
0	0	0	0	1	Data Bus → Transmitter Buffer Register (TBR)
0	0	0	1	0	Receiver Buffer Register (RBR) → Data Bus
0	0	1	0	1	Data Bus → UART Control Register (UCR)
0	0	1	1	0	UART Status Register (USR) → Data Bus
0	1	0	0	1	Data Bus → Modem Control Register (MCR)
0	1	0	1	0	MCR → Data Bus
0	1	1	0	1	Data Bus → Bit Rate Select Register (BRSR)
0	1	1	1	0	Modem Status Register (MSR) → Data Bus

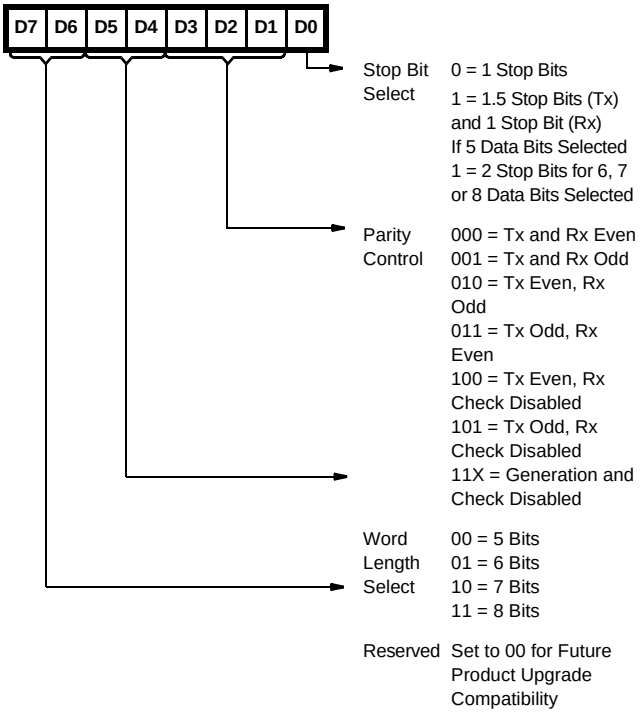


FIGURE 1. UCR

Baud Rate Select Register (BRSR)

The 82C52 is designed to operate with a single crystal or external clock driving the IX input pin. The Baud Rate Select Register is used to select the divide ratio (one of 72) for the internal Baud Rate Generator circuitry. The internal circuitry is separated into two separate counters, a Prescaler and a Divisor Select. The Prescaler can be set to any one of four division rates, ÷1, ÷3, ÷4, or ÷5.

The Prescaler design has been optimized to provide standard baud rates using any one of three popular crystal frequencies. By using one of these common system clock frequencies, 1.8432MHz, 2.4576MHz or 3.072MHz and Prescaler divide ratios of ÷3, ÷4, or ÷5 respectively, the Prescaler output will provide a constant 614.4KHz. When this frequency is further divided by the Divisor Select counter, any of the standard baud rates from 50 Baud to 38.4Kbaud can be selected (see Table 2). Non-standard baud rates up to 1Mbaud can be selected by using different input frequencies (crystal or an external frequency input up to 16MHz) and/or different Prescaler and Divisor Select ratios.

Regardless of the baud rate, the baud rate generator provides a clock which is 16 times the desired baud rate. For example, in order to operate at a 1Mbaud data rate, a 16MHz crystal, a Prescale rate of ÷1, and a Divisor Select rate of “external” would be used. This would provide a 16MHz clock as the output of the Baud Rate Generator to the Transmitter and Receiver circuits.

The CO select bit in the BRSR selects whether a buffered version of the external frequency input (IX input) or the Baud Rate Generator output (16x baud rate clock) will be output on the CO output (pin 21). The Baud Rate Generator output will always be a 50% nominal duty cycle except when “external” is selected and the Prescaler is set to ÷3 or ÷5.

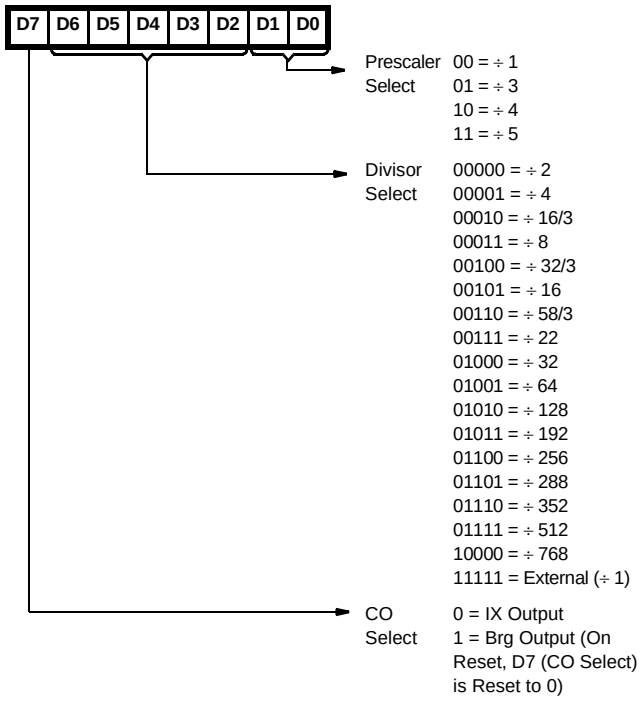


FIGURE 2. BRSR

TABLE 2.

BAUD RATE	DIVISOR
38.4K	External
19.2K	2
9600	4
7200	16/3
4800	8
3600	32/3
2400	16
2000†	58/3
1800†	22
1200	32
600	64
300	128
200	192
150	256
134.5†	288
110†	352
75	512
50	768

NOTE: These baud rates are based upon the following input frequency/ Prescale divisor combinations.
1.8432MHz and Prescale = ÷ 3
2.4576MHz and Prescale = ÷ 4
3.072MHZ and Prescale = ÷ 5

† All baud rates are exact except for:

BAUD RATE	ACTUAL	PERCENT ERROR
1800	1745.45	3.03%
2000	1986.2	0.69%
134.5	133.33	0.87%
110	109.09	0.83%

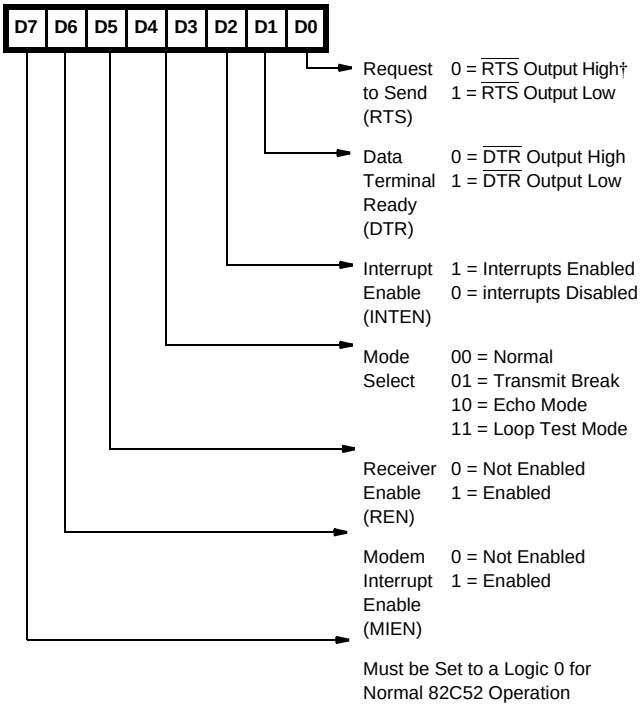
Modem Control Register

The MCR is a general purpose control register which can be written to and read from. The $\overline{RTS}$ and $\overline{DTR}$ outputs are directly controlled by their associated bits in this register. Note that a logic one asserts a true logic level (low) at these output pins. The Interrupt Enable (INTEN) bit is the overall control for the INTR output pin. When INTEN is false, INTR is held false (low).

The Operating Mode bits configure the 82C52 into one of four possible modes. “Normal” configures the 82C52 for normal full or half duplex communications. “Transmit Break”' enables the transmitter to only transmit break characters (Start, Data and Stop bits all are logic zero). The Echo Mode causes any data that is received on the SDI input pin to be retransmitted on the SDO output pin. Note that this output is

a buffered version of the data seen on the SDI input and is not a resynchronized output. Also note that normal UART transmission via the Transmitter Register is disabled when operating in the Echo mode (see Figure 4). The Loop Test Mode internally routes transmitted data to the receiver circuitry for the purpose of self test. The transmit data is disabled from the SDO output pin. The Receiver Enable bit gates off the input to the receiver circuitry when in the false state.

Modem Interrupt Enable will permit any change in modem status line inputs ($\overline{CTS}$, $\overline{DSR}$) to cause an interrupt when this bit is enabled. Bit D7 must always be written to with a logic zero to insure correct 82C52 operation.



† See Modem Status Register description for a description of register flag images with respect to output pins.

FIGURE 3. MCR

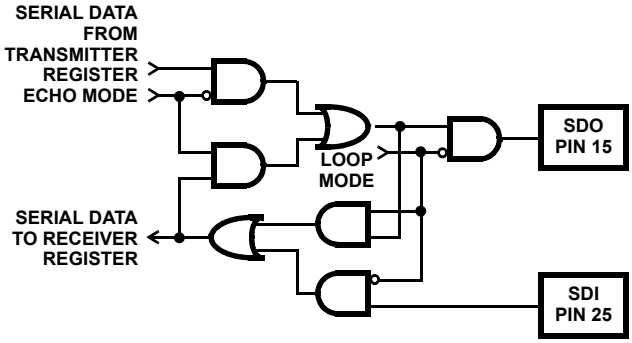


FIGURE 4. LOOP AND ECHO MODE FUNCTIONALITY

UART Status Register (USR)

The USR provides a single register that the controlling sys tem can examine to determine if errors have occurred or if other status changes in the 82C52 require attention. For this reason, the USR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the 82C52.

Three error flags OE, FE and PE report the status of any error conditions detected in the receiver circuitry. These error flags are updated with every character received during reception of the stop bits. The Overrun Error (OE) indicates that a character in the Receiver Register has been received and cannot be transferred to the Receiver Buffer Register (RBR) because the RBR was not read by the CPU. Framing Error (FE) indicates that the last character received in the RBR contained improper stop bits. This could be caused by the absence of the required stop bit(s) or by a stop bit(s) that was too short to be properly detected. Parity Error (PE) indicates that the last character received in the RBR contained a parity error based on the programmed parity of the receiver and the calculated parity of the received character data and parity bits.

The Received Break (RBRK) status bit indicates that the last character received was a break character. A break character would be considered to be an invalid data character in that the entire character including parity and stop bits are a logic zero.

The Modem Status bit is set whenever a transition is detected on any of the Modem input lines ($\overline{CTS}$ or $\overline{DSR}$). A subsequent read of the Modem Status Register will show the state of these two signals. Assertion of this bit will cause an interrupt (INTR) to be generated if the MIEN and INTEN bits in the MCR register are enabled.

The Transmission Complete (TC) bit indicates that both the TBR and Transmitter Registers are empty and the 82C52 has completed transmission of the last character it was commanded to transmit. The assertion of this bit will cause an interrupt (INTR) if the INTEN bit in the MCR register is true.

The Transmitter Buffer Register Empty (TBRE) bit indicates that the TBR register is empty and ready to receive another character.

The Data Ready (DR) bit indicates that the RBR has been loaded with a received character (including Break) and that the CPU may access this data.

Assertion of the TBRE or DR bits do not affect the INTR logic and associated INTR output pin since the 82C52 has been designed to provide separate requests via the DR and TBRE output pins. If a single interrupt for any status change in the 82C52 is desired this can be accomplished by using an 82C59A Interrupt controller with DR, TBRE, and INTR as inputs. (See Figure 11).

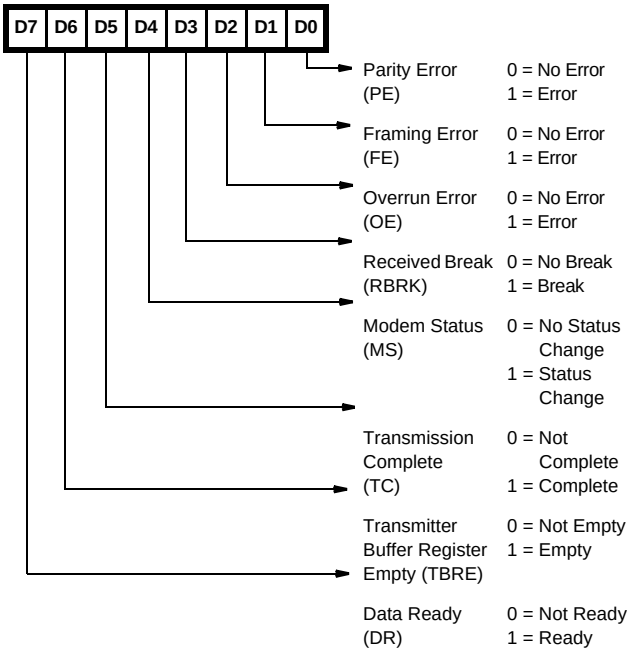


FIGURE 5. USR

Modem Status Register (MSR)

The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the 82C52. Like all of the register images of external pins in the 82C52, true logic levels are represented by a high (1) signal level. By following this consistent definition, the system software need not be concerned with whether external signals are high or low true. In particular, the modem signal inputs are low true, thus a 0 (true assertion) at a modem input pin is represented by a 1 (true) in the MSR.

Any change of state in any modem input signals will set the Modem Status (MS) bit in the USR register. When this happens, an interrupt (INTR) will be generated if the MIEN and INTEN bits of the MCR are enabled.

The Data Set Ready (DSR) input is a status indicator from the modem to the 82C52 which indicates that the modem is ready to provide received data to the 82C52 receiver circuitry.

Clear to Send (CTS) is both a status and control signal from the modem that tells the 82C52 that the modem is ready to receive transmit data from the 82C52 transmitter output (SDO). A high (false) level on this input will inhibit the 82C52 from beginning transmission and if asserted in the middle of a transmission will only permit the 82C52 to finish transmission of the current character.

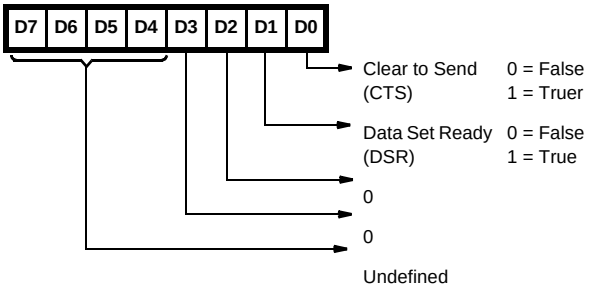


FIGURE 6. MSR

Receiver Buffer Register (RBR)

The receiver circuitry in the 82C52 is programmable for 5, 6, 7 or 8 data bits per character. For words of less than 8 bits, the data is right justified to the Least Significant Bit (LSB = D0). Bit D0 of a data word is always the first data bit received. The unused bits in a less than 8-bit word, at the parallel interface, are set to a logic zero (0) by the 82C52.

Received data at the SDI input pin is shifted into the Receiver Register by an internal 1x clock which has been synchronized to the incoming data based on the position of the start bit. When a complete character has been shifted into the Receiver Register, the assembled data bits are parallel loaded into the Receiver Buffer Register. Both the DR output pin and DR flag in the USR register are set. This double buffering of the received data permits continuous reception of data without losing any of the received data.

While the Receiver Register is shifting a new character into the 82C52, the Receiver Buffer Register is holding a previously received character for the system CPU to read. Failure to read the data in the RBR before complete reception of the next character can result in the loss of the data in the Receiver Register. The OE flag in the USR register indicates the overrun condition.

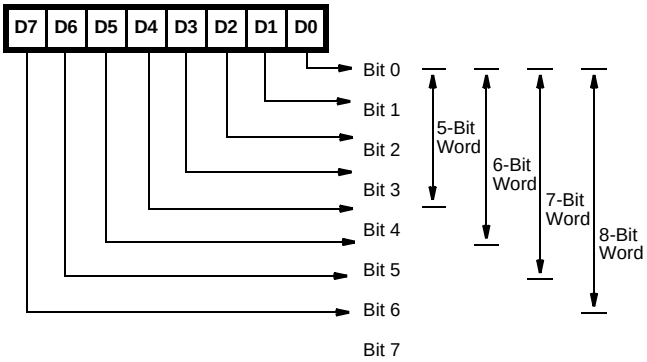


FIGURE 7. RBR

Transmitter Buffer Register (TBR)

The Transmitter Buffer Register (TBR) accepts parallel data from the data bus (D0-D7) and holds it until the Transmitter Register is empty and ready to accept a new character for

transmission. The transmitter always has the same word length and number of stop bits as the receiver. For words of less than 8 bits the unused bits at the microprocessor data bus are ignored by the transmitter.

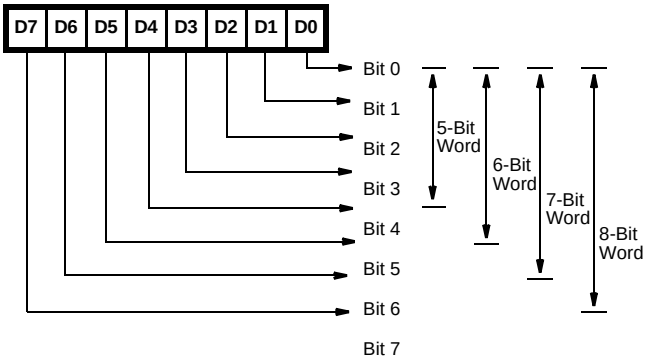


FIGURE 8. TBR

Bit 0, which corresponds to D0 at the data bus, is always the first serial data bit transmitted. Provision is made for the transmitter parity to be the same or different from the receiver. The TBRE output pin and flag (USR register) reflect the status of the TBR. The TC flag (USR register) indicates when both TBR and TR are empty.

82C52 Interrupt Structure

The 82C52 has provisions for software masking of interrupts generated for the INTR output pin. Two control bits in the MCR register, MIEN and INTEN, control modem status interrupts and overall 82C52 interrupts respectively. Figure 9 illustrates the logical control function provided by these signals.

The modem status inputs ($\overline{DSR}$ and $\overline{CTS}$) will trigger the edge detection circuitry with any change of status. Reading the MSR register will clear the detect circuit but has no effect on the status bits themselves. These status bits always reflect the state of the input pins regardless of the mask control signals. Note that the state (high or low) of the status bits are inverted versions of the actual input pins.

The edge detection circuits for the USR register signals will trigger only for a positive edge (true assertion) of these status bits. Reading the USR register not only clears the edge detect circuit but also clears (sets to 0) all of the status bits. The output pins associated with these status bits are not affected by reading the USR register.

A hardware reset of the 82C52 sets the TC status bit in the USR. When interrupts are subsequently enabled an interrupt can occur due to the fact that the positive edge detection circuitry in the interrupt logic has detected the setting of the TC bit. If this interrupt is not desired the USR should be read prior to enabling interrupts. This action resets the positive edge detection circuitry in the interrupt control logic (Figure 9).

NOTE: For USR and MSR, the setting of status bits is inhibited during status register READ operations. If a status condition is generated during a READ operation, the status bit is not set until the trailing edge of the $\overline{RD}$ pulse.

If the bit was already set at the time of the READ operation, and the same status condition occurs, that status bit will be cleared at the trailing edge of the $\overline{RD}$ pulse instead of being set again.

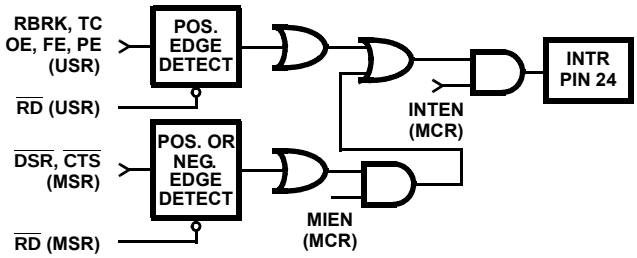


FIGURE 9. 82C52 INTERRUPT STRUCTURE

Software Reset

A software reset of the 82C52 is a useful method for returning to a completely known state without exercising a complete system reset. Such a reset would consist of writing to the UCR, BRSR and MCR registers. The USR and RBR registers should be read prior to enabling interrupts in order to clear out any residual data or status bits which may be invalid for subsequent operation.

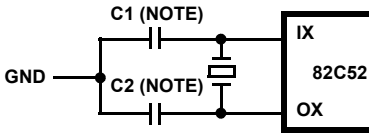
Crystal Operation

The 82C52 crystal oscillator circuitry is designed to operate with a fundamental mode, parallel resonant crystal. This circuit is the same one used in the Intersil 82C84A clock generator/driver. To summarize, Table 3 and Figure 10 show the required crystal parameters and crystal circuit configuration respectively.

When using an external clock source, the IX input is driven and the OX output is left open. Power consumption when using an external clock is typically 50% of that required when using a crystal. This is due to the sinusoidal nature of the drive circuitry when using a crystal.

TABLE 3.

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	1.0 to 16MHz
Type of Operation	Parallel Resonant, Fundamental Mode
Load Capacitance (CL)	20 or 32pF (Typ)
R_{SERIES}(Max)	100Ω (f = 16MHz, CL = 32pF) 200Ω (f = 16MHz, CL = 20pF)



NOTE: C1 = C2 = 20pF For CL = 20pF
C1 = C2 = 47pF For CL = 32pF

FIGURE 10.

82C52 - 80C86 Interfacing

The following example (Figure 11) shows the interface for an 82C52 in an 80C86 system.

Use of the Intersil CMOS Interrupt Controller (82C59A) is optional and necessary only if an interrupt driven system is desired.

By using the Intersil CMOS 82C84A clock generator, the system can be built with a single crystal providing both the processor clock and the clock for the 82C52. The 82C52 has special divider circuitry which is designed to supply industry standard baud rates with a 2.4576MHz input frequency. Using a 15MHz crystal as shown, results in less than a 2% frequency error which is adequate for many applications. For more precise baud rate requirements, a 14.7456MHz crystal will drive the 80C86 at 4.9MHz and provide the 82C52 with the standard baud rate input frequency of 2.4576MHz. If baud rates above 156Kbaud are desired, the OSC output can be used instead of the PCLK (÷6) output for asynchronous baud rates up to 1Mbaud.

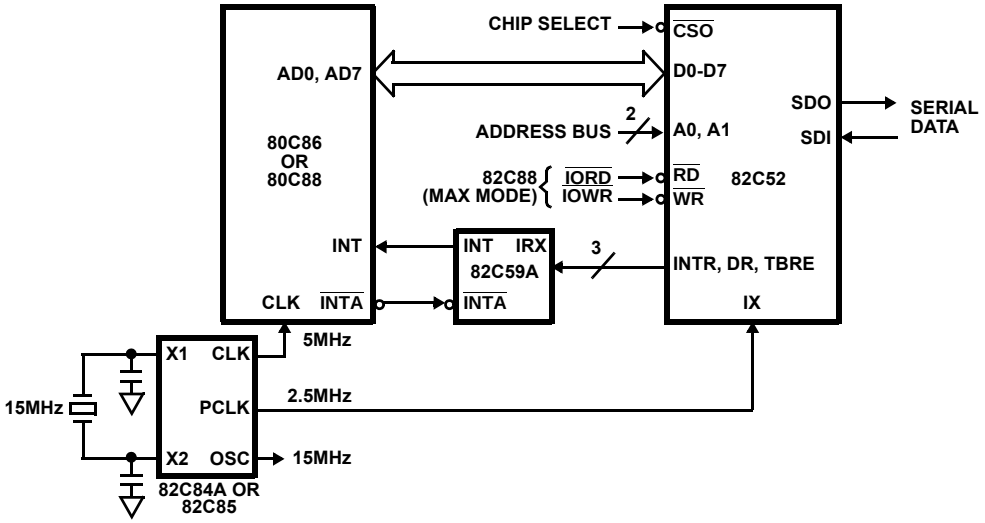


FIGURE 11. 80C86/82C52 INTERFACE

Absolute Maximum Ratings

Supply Voltage . . . . . +8.0V
Input, Output or I/O Voltage . . . . . GND-0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 1

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range
C82C52 . . . . . 0°C to +70°C
I82C52 . . . . . -40°C to +85°C
M82C52 . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	45	8.4
CLCC Package	60	14
PDIP Package	55	N/A
PLCC Package	46	N/A

Maximum Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C
(Lead Tips Only For Surface Mount Packages)

Die Characteristics

Gate Count . . . . . 1500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (C82C52), T_A = -40°C to +85°C (I82C52) T_A = -55°C to +125°C (M82C52)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical One Input Voltage	2.0	-	V	I82C52, C82C52
		2.2	-	V	M82C52
V_{IL}	Logical Zero Input Voltage	-	0.8	V	
VTH	Schmitt Trigger Logic One Input Voltage	V_{CC} -0.5	-	V	Reset Input
VTL	Schmitt Trigger Logic Zero Input Voltage	-	GND +0.5	V	Reset Input
VIH (CLK)	Logical One Clock Input Voltage	V_{CC} -0.5	-	V	External Clock
VIL (CLK)	Logical Zero Clock Input Voltage	-	GND +0.5	V	External Clock
VOH	Output High Voltage	3.0	-	V	I_{OH} = -2.5mA, Except OX
		V_{CC} -0.4	-	V	I_{OH} = -100µA, For OX - I_{OH} = -1.0mA
VOL	Output Low Voltage	-	0.4	V	I_{OL} = +2.5mA
II	Input Leakage Current	-1.0	+1.0	µA	V_{IN} = GND or V_{CC}, DIP Pins 1, 2, 11, 12, 17, 18, 23, 25, 28
IO	Input/Output Leakage Current	-10.0	+10.0	µA	V_O = GND or V_{CC}, DIP Pins 3-10
ICCOP	Operating Power Supply Current (Note 1)	-	4	mA	External Clock F = 2.4576MHz, V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open
ICCSB	Standby Supply Current	-	100	µA	V_{CC} = 5.5V, V_{IN} = V_{CC} or GND, Outputs Open

NOTE:

1. Guaranteed and sampled, but not 100% tested. ICCOP is typically ≤ 1.5mA/MHz.

Capacitance T_A = 25°C

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
CIN	Input Capacitance	12	pF	FREQ = 1MHz, all measurements are referenced to device GND
COUT	Output Capacitance	15	pF	
CI/O	I/O Capacitance	15	pF	

AC Electrical Specifications

V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C (C82C52), T_A = -40°C to +85°C (I82C52)
T_A = -55°C to +125°C (M82C52)

Timing Requirements and Responses

SYMBOL		PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(1)	TSVCTL	Select Setup to Control Leading Edge	30	-	ns	
(2)	TCTHSX	Select Hold from Control Trailing Edge	50	-	ns	
(3)	TCTLCTH	Control Pulse Width	150	-	ns	Control Consists of $\overline{RD}$ or $\overline{WR}$
(4)	TCTHCTL	Control Disable to Control Enable	190	-	ns	
(5)	TRLDV	Read Low to Data Valid	-	120	ns	1, See AC Test Circuit
(6)	TRHDZ	Read Disable	0	60	ns	2, See AC Test Circuit
(7)	TDVWH	Data Setup Time	50	-	ns	
(8)	TWHDX	Data Hold Time	20	-	ns	
(9)	FC	Clock Frequency	0	16	MHz	TCHCL + TCLCH must be ≥ 62.5ns
(10)	TCHCL	Clock High Time	25	-	ns	
(11)	TCLCH	Clock Low Time	25	-	ns	
(12)	TR/TF	IX Input Rise/Fall Time (External Clock)	-	tx	ns	$tx \geq \frac{1}{6FC}$ or 50ns Whichever is smaller
(13)	TFCO	Clock Output Fall Time	-	15	ns	CL = 50pf
(14)	TRCO	Clock Output Rise Time	-	15	ns	CL = 50pf

AC Testing Input, Output Waveforms

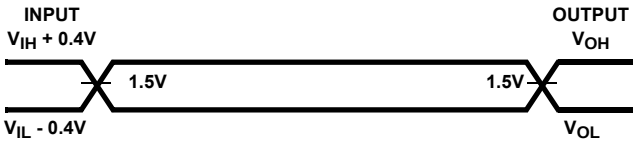


FIGURE 12. PROPAGATION DELAY

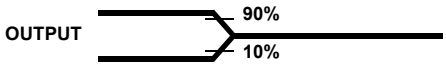


FIGURE 13. ENABLE/DISABLE DELAY

AC TESTING: All input signals (except IX and RST) must switch between V_{IL} -0.4V and V_{IH} +0.4V. Input rise and fall times are driven at 1ns/V.

Timing Waveform

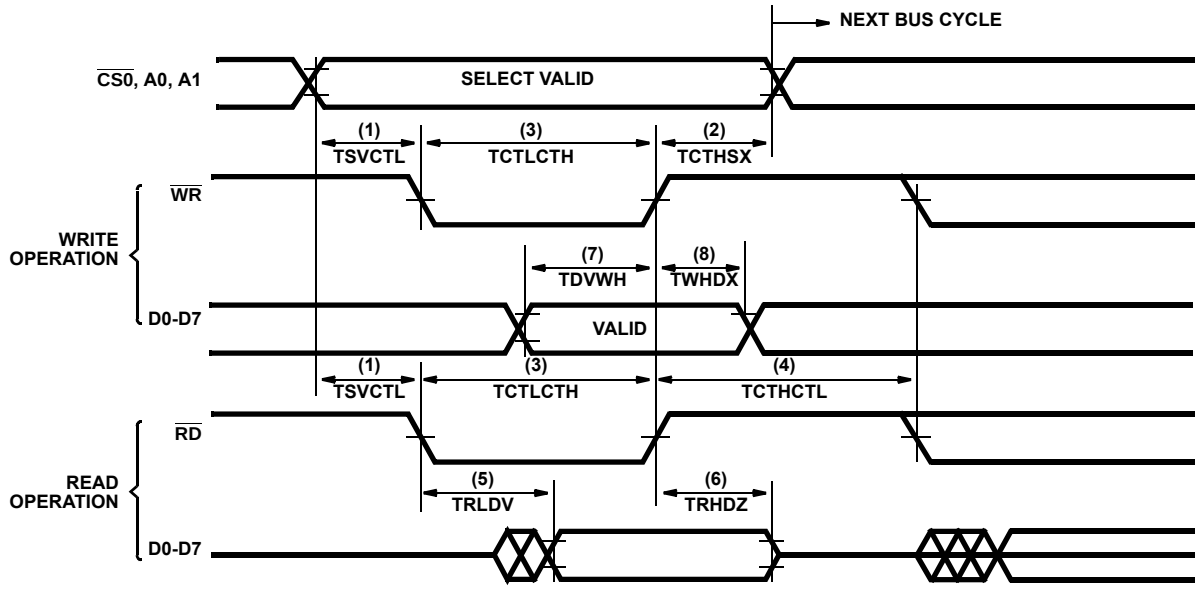
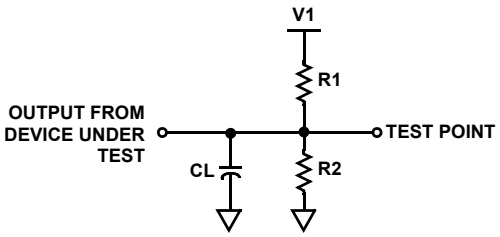


FIGURE 14. BUS OPERATION

AC Test Circuit



TEST CONDITION		V1	R1	R2	CL
1	Propagation Delay	1.7V	520	∞	100pF
2	Disable Delay	V_{CC}	5K	5K	50pF

UART Timing Characterization

All parameters listed in this table were laboratory bench characterized at room temperature on a small sample of parts. No guarantee is implied. The main intent here is to clarify functional operation of the 82C52.

82C52 UART Timing Characterized with IX = External Clock

SYMBOL		PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
(15)	TS1	CO(IX) Delay from IX	-	30	ns	BRSR Bit D7 = 0 (IX Output)
(16)	TS2	CO (BRG) Delay from IX	-	80	ns	BRSR Bit D7 = 1 (BRG Output)
(17)	TCY	CO (BRG) Clock Cycle Time	62.5	-	ns	BRSR Bit D7 = 1 (BRG Output), Note 1
(18)	TDTX	SDO Delay from CO(BRG) Low	-	30	ns	Note 2
(19)	TWLTL	$\overline{WR}$ Low to TBRE Low	-	50	ns	Note 3
(20)	TCLTH	CO (BRG) Low to TBRE HIgh	-	50	ns	Notes 3, 4
(21)	TIHF	INTR High on Flag	-	50	ns	Note 5A, 5B
(22)	TIHM	INTR High on MS	-	50	ns	Note 5
(23)	TRLIL	$\overline{RD}$ Low to INTR Low	-	60	ns	
(24)	TCTHX	$\overline{CTS}$ High to Disable Transmit	4TCY + 10	-	ns	TBR Full, Note 6
(25)	TDRH	CO (BRG) Low to DR High	-	40	ns	Note 7
(26)	TRLDL	$\overline{RD}$ Low to DR Low	-	50	ns	Note 7
(27)	TWHO	$\overline{WR}$ High to $\overline{RTS}$/$\overline{DTR}$ Active	-	50	ns	

NOTES:

1. Prescaler rate of divide by 1, Divisor Select rate of “external” (divide by 1). The Baud Rate Clock (CO-BRG) operates at 16 times the user programmed bit rate. For example, at 1200 baud: TCY = 1/(16 x 1200) = 52.1µs.
2. A. With TR (Transmitter Register) initially empty, TDTX occurs from the 5th falling edge of CO(BRG) after $\overline{WR}$ goes high.
   B. With TR initially full, TDTX occurs from the trailing edge of the 16th CO(BRG) in the last Stop bit provided $\overline{WR}$ went high by the trailing edge of the 12th CO(BRG) in the last Stop bit.
   C. With $\overline{CTS}$ high (disable transmit) and TBR full, TDTX occurs from the 5th falling edge of CO(BRG) after $\overline{CTS}$ goes low.
3. TBRE bit D6 in USR is updated each time TBRE changes state.
4. A. With TR initially empty, TCLTH(TBRE) occurs from the 4th falling edge of CO(BRG) after $\overline{WR}$ goes high.
   B. With TR initially full, TCLTH(TBRE) occurs from the trailing edge of the 15th CO(BRG) in the last Stop bit provided $\overline{WR}$ went high by the trailing edge of the 12th CO(BRG) in the last Stop bit.
   C. With $\overline{CTS}$ high (disable transmit) and TBR full, TCLTH(TBRE) occurs from the 4th falling edge of CO(BRG) after $\overline{CTS}$ goes low.
5. A. <u>INT on TC:</u> INTEN enabled; USR bit D5(TC) is updated at this time regardless of interrupt configuration.
   - INT on TC occurs from the trailing edge of the 11th CO(BRG) in the last Stop bit if TBR empty at that time.

   B. <u>INTR on receive flags OE, FE, PE, and RBRK:</u> INTEN enabled; Respective USR bits updated at this time regardless of interrupt configuration.
   - INT on OE, FE, PE, RBRK occurs from the trailing edge of the 11th CO(BRG) in the last Stop bit. To avoid OE, $\overline{RD}$(RBR) must go low by the trailing edge of the 8th CO(BRG) in the last Stop bit.

   C. <u>INTR on MS:</u> INTEN and MIEN enabled; USR bit D4(MS) is updated at this time regardless of INTEN/MIEN.
   - INTR on MS occurs whenever $\overline{CTS}$ or $\overline{DSR}$ input changes state.
6. TCTHX is time before end of last Stop bit by which $\overline{CTS}$ must be inactive (high) to prevent transmission of the character waiting in TBR.
7. DR bit D7 in USR is updated each time DR changes state. TDRH always from trailing edge of 11th CO(BRG) in last Stop bit.

UART Timing Characterization

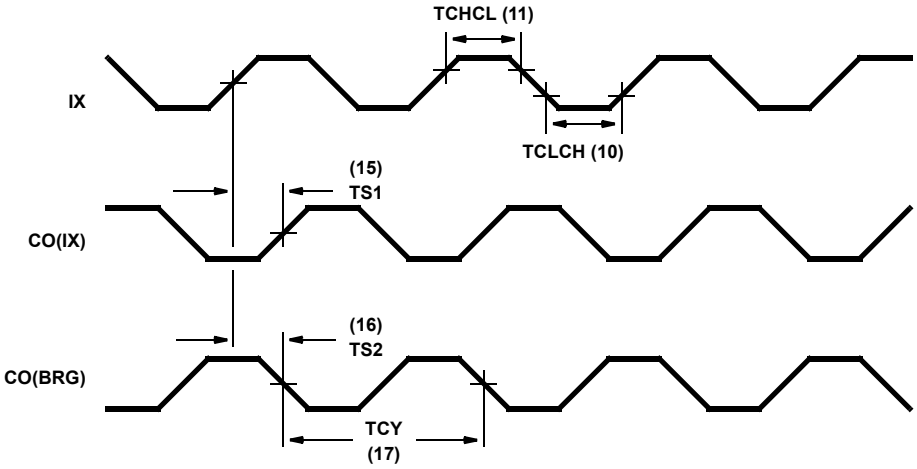


FIGURE 15. CLOCK (IX) AND CO TIMING

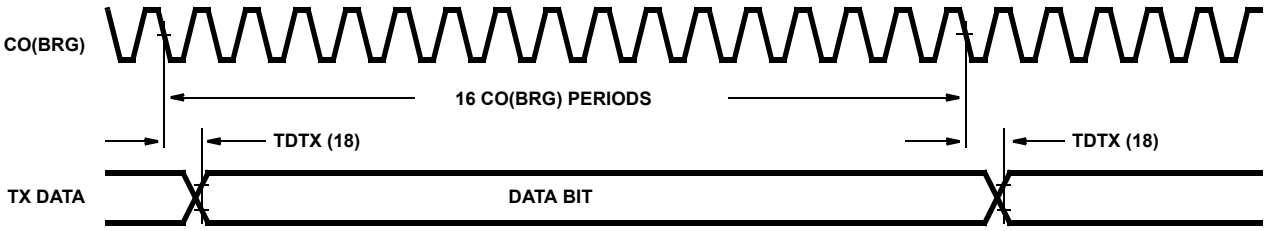


FIGURE 16. TRANSMITTER DATA

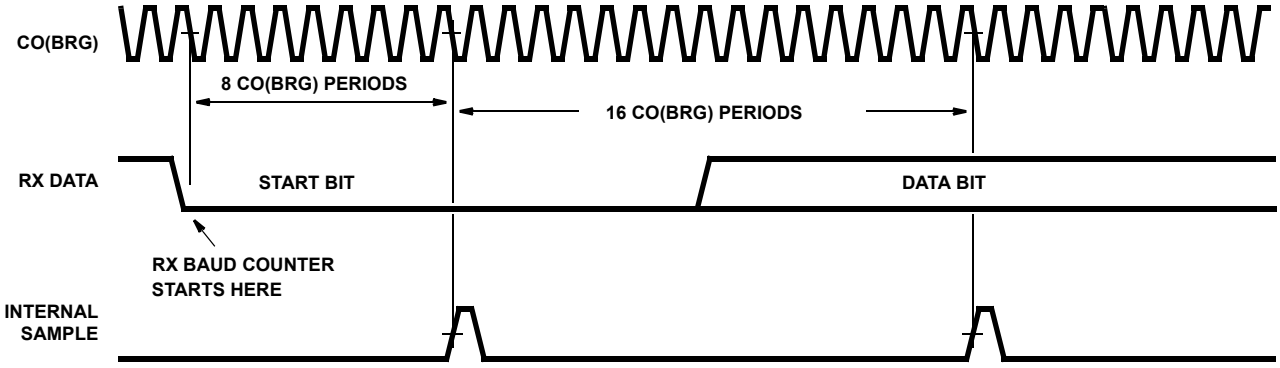


FIGURE 17. RECEIVER DATA

UART Timing Characterization (Continued)

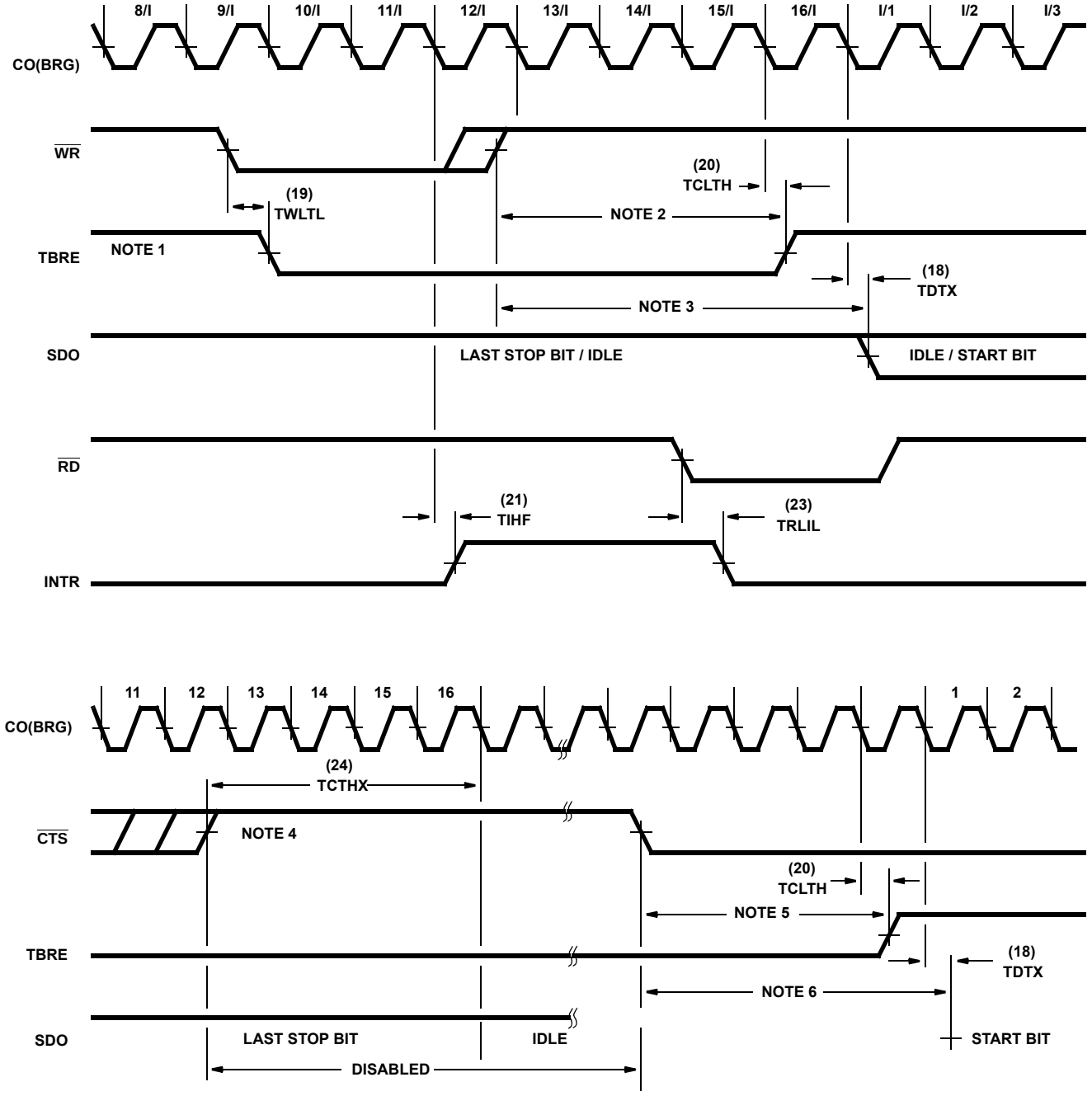


FIGURE 18. TRANSMIT TIMING

UART Timing Characterization (Continued)

NOTES:

1. TBRE bit D6 in USR is updated each time TBRE changes state.
2. A. With TR initially empty, TCLTH(TBRE) occurs from the 4th falling edge of CO(BRG) after $\overline{WR}$ goes high.
   B. With TR initially full, TCLTH(TBRE) occurs from the trailing edge of the 15th CO(BRG) in the last Stop bit provided $\overline{WR}$ went high by the trailing edge of the 12th CO(BRG) in the last Stop bit.
3. A. With TR (Transmitter Register) initially empty, TDTX occurs from the 5th falling edge of CO(BRG) after $\overline{WR}$ goes high.
   B. With TR initially full, TDTX occurs from the trailing edge of the 16th CO(BRG) in the last Stop bit provided $\overline{WR}$ went high by the trailing edge of the 12th CO(BRG) in the last Stop bit.
4. TCTHX is time before end of last Stop bit by which $\overline{CTS}$ must be inactive (high) to prevent transmission of the character waiting in TBR.
5. With $\overline{CTS}$ high (disable transmit) and TBR full, TCLTH(TBRE) occurs from the 4th falling edge of CO(BRG) after $\overline{CTS}$ goes low.
6. With $\overline{CTS}$ high (disable transmit) and TBR full, TDTX occurs from the 5th falling edge of CO(BRG) after $\overline{CTS}$ goes low.

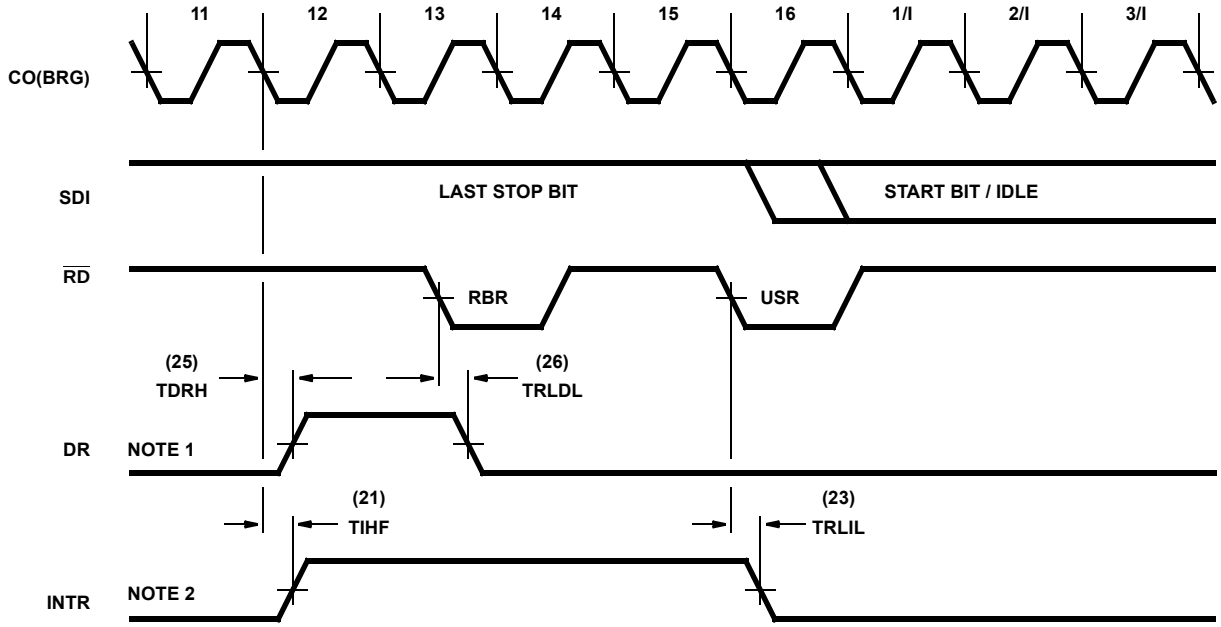


FIGURE 19. RECEIVE TIMING

UART Timing Characterization (Continued)

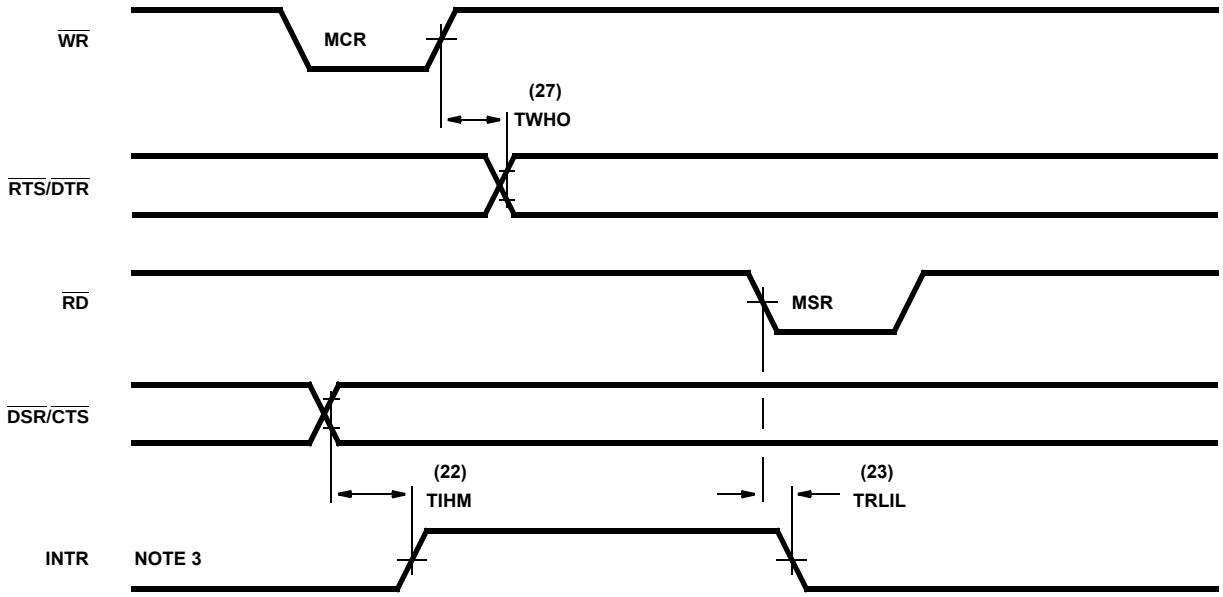


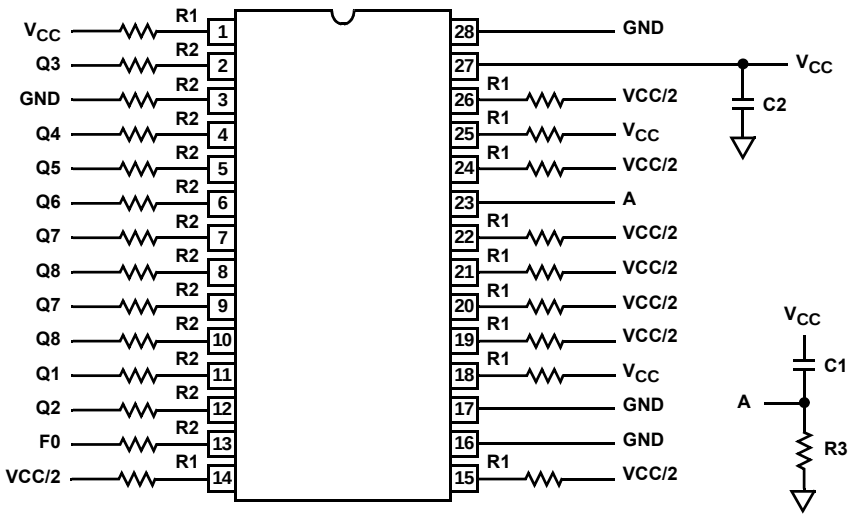
FIGURE 20. OTHER TIMING

NOTES:

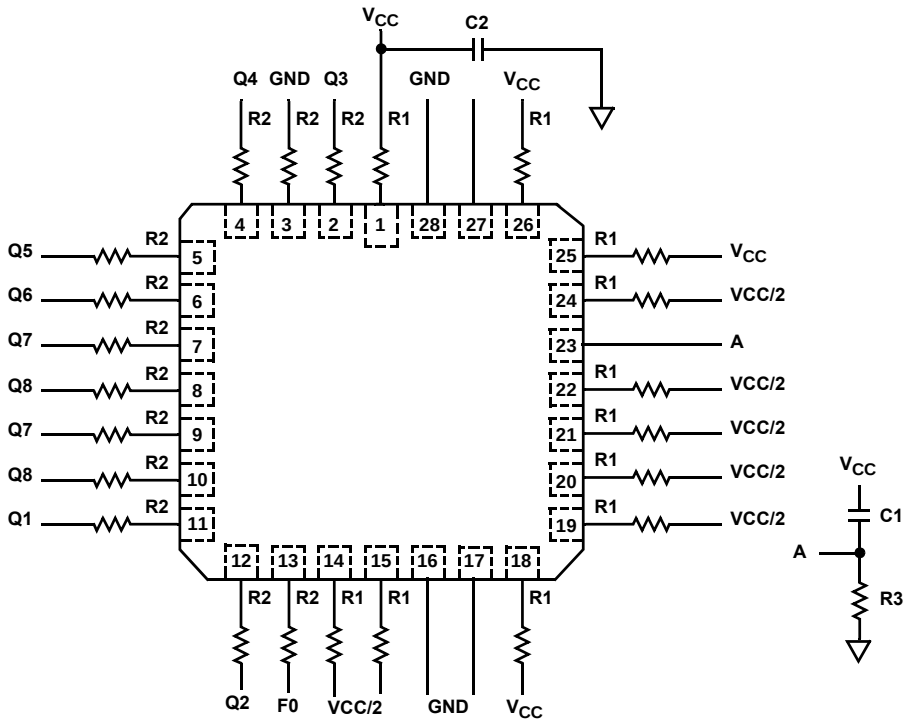
1. DR bit D7 in USR is updated each time DR changes state. TDRH always from trailing edge of 11th CO(BRG) in last Stop bit.
2. INTR on receive flags OE, FE, PE, and RBRK: INTEN enabled; Respective USR bits updated at this time regardless of interrupt configuration.
   - INT on OE, FE, PE, RBRK occurs from the trailing edge of the 11th CO(BRG) in the last Stop bit. To avoid OE, $\overline{RD}$(RBR) must go low by the trailing edge of the 8th CO(BRG) in the last Stop bit.
3. INTR on MS: INTEN and MIEN enabled; USR bit D4(MS) is updated at this time regardless of INTEN/MIEN.
   - INTR on MS occurs whenever $\overline{CTS}$ or $\overline{DSR}$ input changes state.

Burn-In Circuits

MD82C52 CERDIP



MR82C52 CLCC



NOTES:

1. V_{CC} = 5.5V ±0.5V
   GND = 0V
2. V_{IH} = 4.5V ±10%
   V_{IL} = -0.2V to +0.4V
3. Component Values:
   R1 = 1.2KΩ, 1/4W, 5%
   R2 = 47KΩ, 1/4W, 5%
   R3 = 10KΩ, 1/4W, 5%
   C1 = 1.0μF nominal
   C2 = 0.01μF minimum
   F0 = 100KHz ±10%, F1 = F0/2, F2 = F1/2 . . . F12 = F11/2

Die Characteristics

DIE DIMENSIONS:
178.7 x 187.0 x 19 ±1mils

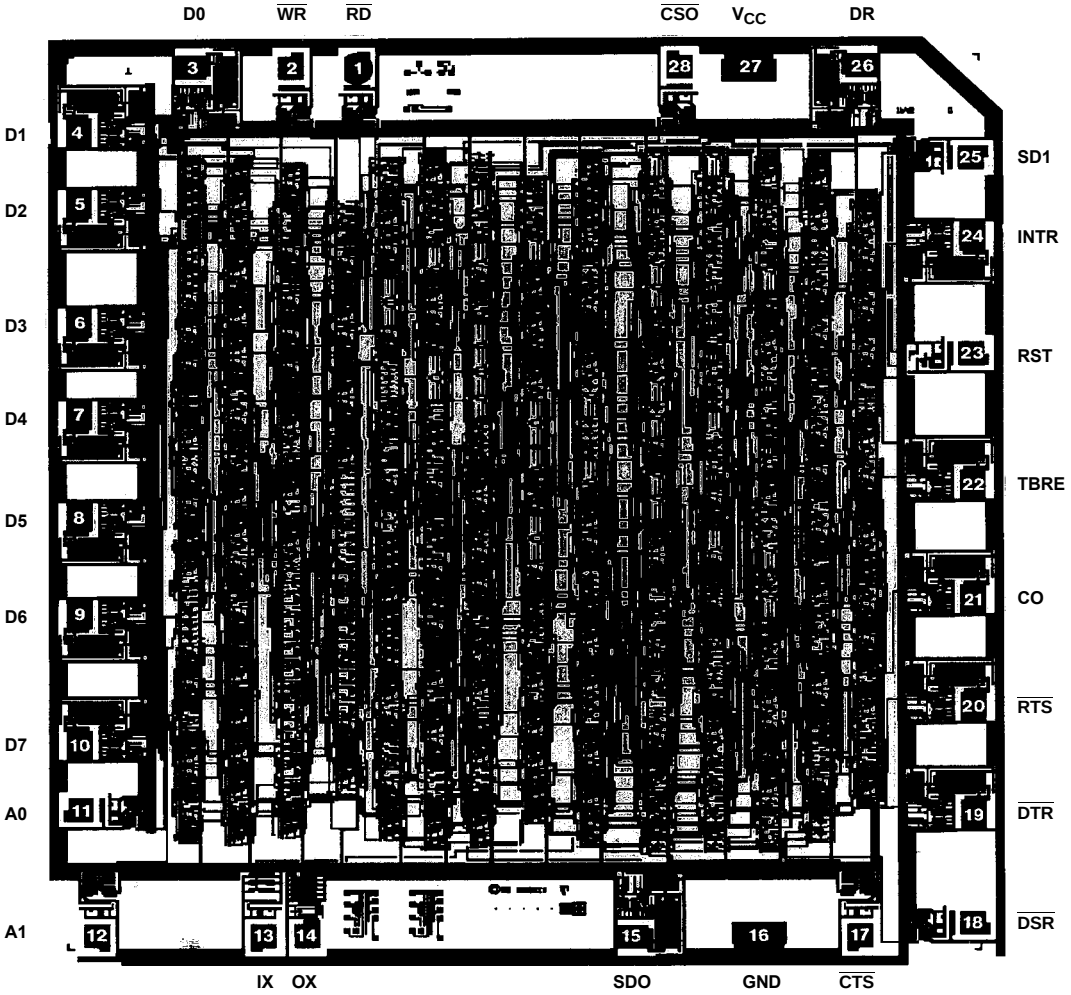
METALLIZATION:
Type: Silicon - Aluminum
Thickness: 11kÅ ±2kÅ

GLASSIVATION:
Type: Nitrox
Thickness: 10kÅ

WORST CASE CURRENT DENSITY:
2.07×10^4 A/cm^2

Metallization Mask Layout

82C52



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