

**FEATURES**

- **Guaranteed AC performance over temperature and voltage:**
  - > 800MHz  $f_{MAX}$  (typical)
  - < 50ps within-device skew
- **Low voltage operation:**
  - LVPECL: +3.3V  $\pm 10\%$
  - LVECL: -3.3V  $\pm 10\%$
- **Internal 75k $\Omega$  pull-down resistors**
- **Guaranteed over industrial temperature range:**  
-40°C to +85°C
- **Pin-for-pin, plug-in replacement for MC100LVE310**
- **Available in 28-pin PLCC package**

**DESCRIPTION**

The SY100E310L is a 3.3V, precision 2:8 ECL/PECL fanout buffer optimized for precision low-skew clock distribution. The SY100E310L features fully differential clock paths to minimize both device and system skew resulting in skew performance of < 50ps. In addition, the device includes a 2:1 multiplexer input for redundant switchover applications.

The SY100E310L is optimized for low voltage +3.3V LVPECL or -3.3V LVECL applications.

Data sheets and support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

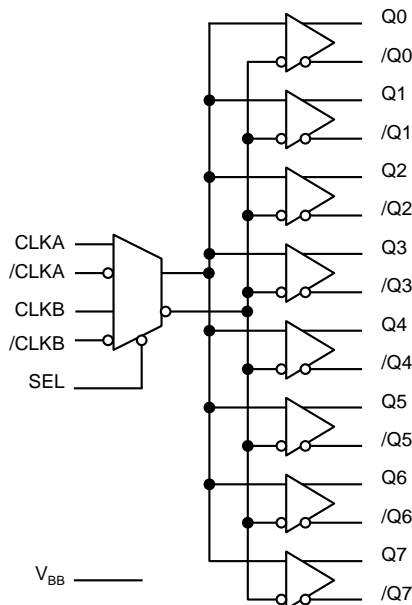
**APPLICATIONS**

- **Communications clock distribution**
- **Redundant clock switchover**
- **High-end server clock distribution**

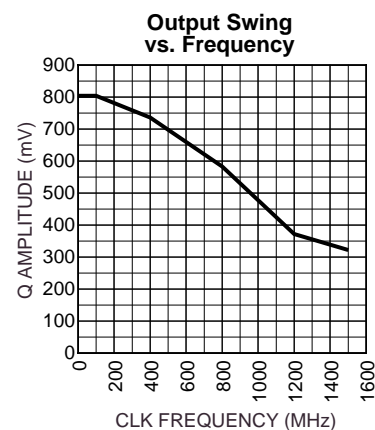
**CROSS REFERENCE TABLE**

Micrel Semiconductor	On Semiconductor
SY100E310LJI	MC100LVE310FN
SY100E310LJITR	MC100LVE310FNR2

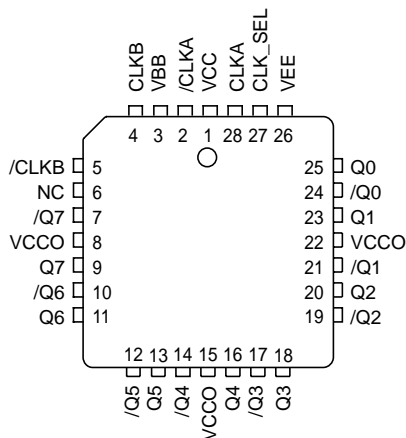
**FUNCTIONAL BLOCK DIAGRAM**



**TYPICAL PERFORMANCE**



**PACKAGE/ORDERING INFORMATION**



**28-Pin PLCC (J28-1)**

**Ordering Information<sup>(1)</sup>**

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100E310LJI	J28-1	Industrial	SY100E310LJI	Sn-Pb
SY100E310LJITR <sup>(2)</sup>	J28-1	Industrial	SY100E310LJI	Sn-Pb
SY100E310LJY <sup>(3)</sup>	J28-1	Industrial	SY100E310LJY with Pb-Free bar-line indicator	Matte-Sn
SY100E310LJYTR <sup>(2, 3)</sup>	J28-1	Industrial	SY100E310LJY with Pb-Free bar-line indicator	Matte-Sn

**Notes:**

1. Contact factory for die availability. Dice are guaranteed at T<sub>A</sub> = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

**PIN DESCRIPTION**

Pin Number	Pin Name	Pin Function
1	VCC	Positive Core Power Supply. Bypass with 0.1μF  0.01μF low ESR capacitors. Not internally connected to V <sub>CCO</sub> . Must be externally connected to V <sub>CCO</sub> on PCB.
28, 2, 4, 5	CLKA, /CLKA CLKB, /CLKB	Differential Inputs: These input pairs are the differential data inputs to the device.
3	VBB	Reference Voltage Output. Used for AC-coupled inputs or single-ended inputs.
6	NC	No Connect.
8, 15, 22	VCCO	Positive Power Supply. Bypass with 0.1μF  0.01μF low ESR capacitors. Not internally connected to V <sub>CC</sub> . Must be externally connected to V <sub>CC</sub> on PCB.
24, 21, 19, 17, 14, 12, 10, 7	/Q0, /Q1, /Q2, /Q3 /Q4, /Q5, /Q6, /Q7	Differential Outputs.
25, 23, 20, 18, 16, 13, 11, 9,	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Differential Outputs.
26	VEE	Negative Supply.
27	CLK_SEL	Single-Ended Clock Select.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{CC}$ ) .....	-0.5V to +4.0V
Input Voltage ( $V_{IN}$ ) .....	-0.5V to $V_{CC}$
Termination Current <sup>(3)</sup>	
Source or sink current on $V_{BB}$ ( $I_{BB}$ ) .....	$\pm 0.5$ mA
Input Current	
Source or sink current	
(CLKA, /CLKA, CLKB, /CLKB, CLK_SEL) .....	$\pm 50$ mA
Lead Temperature (soldering, 20 sec.) .....	+260°C
Storage Temperature ( $T_S$ ) .....	-65°C to +150°C

### Operating Ratings<sup>(2)</sup>

Supply Voltage ( $V_{CC}$ ) .....	+3.0V to +3.6V
Ambient Temperature ( $T_A$ ) .....	-40°C to +85°C
Package Thermal Resistance	
PLCC ( $\theta_{JA}$ )	
Still-Air .....	63.5°C/W
500lfpm .....	43.5°C/W

## DC ELECTRICAL CHARACTERISTICS<sup>(4)</sup>

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply		3.0	3.3	3.6	V

## LVPECL DC ELECTRICAL CHARACTERISTICS<sup>(4, 5)</sup>

$V_{CC} = +3.3\text{V}$ ,  $V_{EE} = 0\text{V}$ ;  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{CC}$	Power Supply Current	No load, max. $V_{CC}$		55	70	mA
$V_{OH}$	Output High Voltage (Q0-Q7, /Q0-/Q7)	$R_L = 50\Omega$ to $V_{CC} - 2\text{V}$	2215	2345	2420	mV
$V_{OL}$	Output Low Voltage (Q0-Q7, /Q0-/Q7)	$R_L = 50\Omega$ to $V_{CC} - 2\text{V}$	1470	1595	1680	mV
$V_{IH}$	Input High Voltage (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)		2135		2420	mV
$V_{IL}$	Input Low Voltage (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)		1490		1825	mV
$V_{IHCMR}$	Input High Voltage Common Mode Range (Differential) (CLKA, / CLKA, CLKB, /CLKB)	<b>Note 6</b>	1.8		2.9	V
$V_{BB}$	Output Reference Voltage		1.92		2.04	V
$I_{IN}$	Input HIGH Current (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)				150	$\mu\text{A}$
$I_{IL}$	Input LOW Current (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)		0.5			$\mu\text{A}$

**Notes:**

1. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Due to the limited drive capability use for input of the same package only.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.3\text{V}$ .
6.  $V_{IHCMR}$  is defined as the range within which the  $V_{IH}$  level may vary with the device still meeting the propagation delay specification. The  $V_{IL}$  level must be such that the peak-to-peak voltage is less than 1.0V and then greater than or equal to  $V_{PP}(\text{min})$ .

**LVNECL DC ELECTRICAL CHARACTERISTICS<sup>(7, 8)</sup>**

$V_{CC} = +3.3V$ ,  $V_{EE} = 0V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ; unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output High Voltage (Q0-Q7, /Q0-/Q7)	$R_L = 50\Omega$ to $V_{CC} - 2V$	-1085	-955	-880	mV
$V_{OL}$	Output Low Voltage (Q0-Q7, /Q0-/Q7)	$R_L = 50\Omega$ to $V_{CC} - 2V$	-1830	-1705	-1620	mV
$V_{IH}$	Input High Voltage (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)		-1165		-880	mV
$V_{IL}$	Input Low Voltage (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)		-1810		-1475	mV
$V_{IHCMR}$	Input High Voltage Common Mode Range (Differential) (CLKA, /CLKA, CLKB, /CLKB)	<b>Note 9</b>	-1.5		-0.4	V
$V_{BB}$	Output Reference Voltage		-1.38		-1.26	V
$I_{IN}$	Input HIGH Current (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)				150	$\mu A$
$I_{IL}$	Input LOW Current (CLKA, /CLKA, CLKB, /CLKB, CLK_SEL)		0.5			$\mu A$

**AC ELECTRICAL CHARACTERISTICS**

$V_{CC} = +3.0$  to  $+3.6V$  and  $V_{EE} = 0V$  or  $V_{CC} = 0V$  and  $V_{EE} = -3.0$  to  $-3.6V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ ; unless noted.

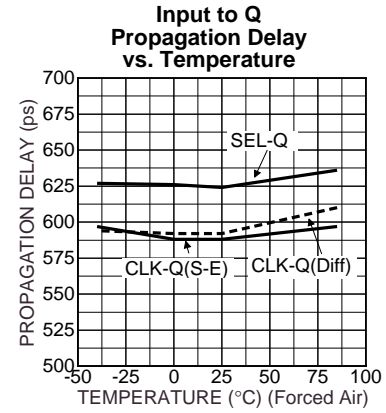
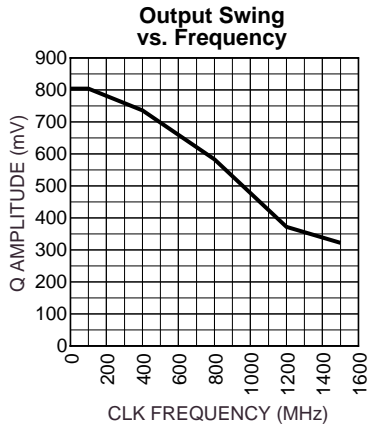
Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	$V_{OUT} = 400mV$		800		MHz
$t_{PD}$	Propagation Delay CLKA-to-Q, CLKB-to-Q (Differential)	<b>Note 10</b>	525		725	ps
	CLKA-to-Q, CLKB-to-Q (Single-ended)	<b>Note 11</b>	500		750	ps
$t_{SKEW}$	Within-Device Skew	<b>Note 12</b>			50	ps
	Part-to-Part Skew (Differential)				200	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter			1	$ps_{RMS}$	
$V_{PP}$	Input Swing	<b>Note 13</b>	500		1000	mV
$t_r, t_f$	Rise / Fall Time (20% to 80%) (Q0-Q7, /Q0-/Q7)		160	375	600	ps

**Notes:**

- The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.3V$ .
- $V_{IHCMR}$  is defined as the range within which the  $V_{IH}$  level may vary with the device still meeting the propagation delay specification. The  $V_{IL}$  level must be such that the peak-to-peak voltage is less than 1.0V and then greater than or equal to  $V_{PP(min)}$ .
- The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
- The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
- The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
- $V_{PP(min)}$  is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The  $V_{PP(min)}$  is AC limited for the E310L as a differential input as low as 50 mV will still produce full ECL levels at the output.

**TYPICAL OPERATING CHARACTERISTICS**

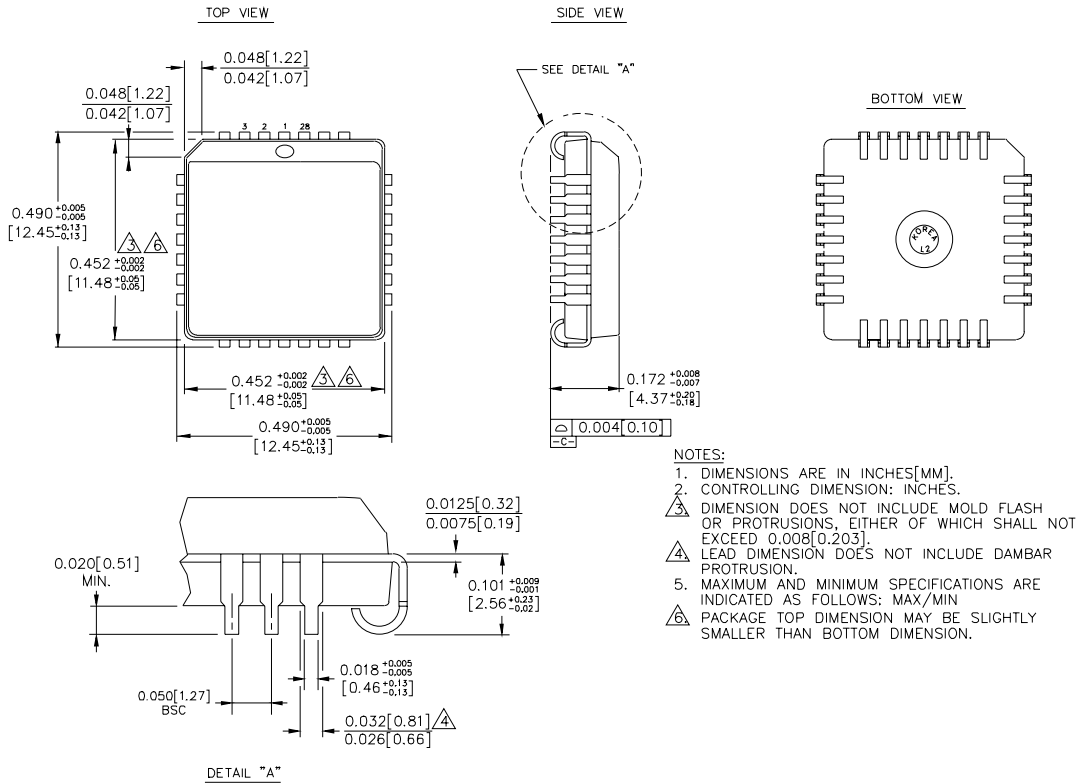
$V_{CC} = 3.3V, T_A = 25^{\circ}C$



**RELATED PRODUCT AND SUPPORT DOCUMENTATION**

Part Number	Function	Data Sheet Link
HBW Solutions	New Products and Applications	<a href="http://www.micrel.com/product-info/products/solutions.shtml">www.micrel.com/product-info/products/solutions.shtml</a>

**28-PIN PLCC (J28-1)**



Rev. 03

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