

Table 11. FSMC pin definition (continued)

Pins	FSMC		64 pins	81 pins	100 pins	144 pins
	LCD/NOR/ PSRAM/SRAM	NOR/PSRAM Mux				
PF1	A1	-	-	-	-	Yes
PF2	A2	-	-	-	-	Yes
PF3	A3	-	-	-	-	Yes
PF4	A4	-	-	-	-	Yes
PF5	A5	-	-	-	-	Yes
PC2	NWE	NWE	Yes	Yes	Yes	Yes
PC3	A0	-	Yes	Yes	Yes	Yes
PA2	D4	DA4	Yes	Yes	Yes	Yes
PA3	D5	DA5	Yes	Yes	Yes	Yes
PA4	D6	DA6	Yes	Yes	Yes	Yes
PA5	D7	DA7	Yes	Yes	Yes	Yes
PC4	NE4	NE4	Yes	Yes	Yes	Yes
PC5	NOE	NOE	Yes	Yes	Yes	Yes
PF12	A6	-	-	-	-	Yes
PF13	A7	-	-	-	-	Yes
PF14	A8	-	-	-	-	Yes
PF15	A9	-	-	-	-	Yes
PG0	A10	-	-	-	-	Yes
PG1	A11	-	-	-	-	Yes
PE7	D4	DA4	-	-	Yes	Yes
PE8	D5	DA5	-	-	Yes	Yes
PE9	D6	DA6	-	Yes	Yes	Yes
PE10	D7	DA7	-	Yes	Yes	Yes
PE11	D8	DA8	-	Yes	Yes	Yes
PE12	D9	DA9	-	Yes	Yes	Yes
PE13	D10	DA10	-	Yes	Yes	Yes
PE14	D11	DA11	-	Yes	Yes	Yes
PE15	D12	DA12	-	Yes	Yes	Yes
PB12	D13	DA13	Yes	Yes	Yes	Yes
PB14	D0	DA0	Yes	Yes	Yes	Yes
PD8	D13	DA13	-	-	-	Yes
PD9	D14	DA14	-	Yes	Yes	Yes
PD10	D15	DA15	-	Yes	Yes	Yes

Table 11. FSMC pin definition (continued)

Pins	FSMC		64 pins	81 pins	100 pins	144 pins
	LCD/NOR/ PSRAM/SRAM	NOR/PSRAM Mux				
PD11	A16	A16	-	-	Yes	Yes
PD12	A17	A17	-	-	Yes	Yes
PD13	A18	A18	-	-	Yes	Yes
PD14	D0	DA0	-	-	Yes	Yes
PD15	D1	DA1	-	-	Yes	Yes
PG2	A12	-	-	-	-	Yes
PG3	A13	-	-	-	-	Yes
PG4	A14	-	-	-	-	Yes
PG5	A15	-	-	-	-	Yes
PC6	D1	DA1	Yes	Yes	Yes	Yes
PC11	D2	DA2	Yes	Yes	Yes	Yes
PC12	D3	DA3	Yes	Yes	Yes	Yes
PD0	D2	DA2	-	Yes	Yes	Yes
PD1	D3	DA3	-	-	Yes	Yes
PD2	NWE	NWE	Yes	Yes	Yes	Yes
PD3	CLK	CLK	-	-	Yes	Yes
PD4	NOE	NOE	-	-	Yes	Yes
PD5	NWE	NWE	-	-	Yes	Yes
PD6	NWAIT	NWAIT	-	-	Yes	Yes
PD7	NE1	NE1	-	-	Yes	Yes
PG9	NE2	NE2	-	-	-	Yes
PG10	NE3	NE3	-	-	-	Yes
PG12	NE4	NE4	-	-	-	Yes
PG13	A24	A24	-	-	-	Yes
PG14	A25	A25	-	-	-	Yes
PB7	NL	NL	Yes	Yes	Yes	Yes
PE0	NBL0	NBL0	-	-	Yes	Yes
PE1	NBL1	NBL1	-	-	Yes	Yes



4.9 Alternate functions

Table 12. STM32F413xG/H alternate functions

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	TIM8_ETR	-	-	-	USART2_CTS	UART4_TX	-	-	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	SPI4_MOSI/I2S4_SD	-	USART2_RTS	UART4_RX	QUADSPI_BK1_IO3	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	I2S2_CKIN	-	USART2_TX	-	-	-	FSMC_D4/ FSMC_DA4	-	-	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-	I2S2_MCK	-	USART2_RX	-	-	SAI1_SD_B	FSMC_D5/ FSMC_DA5	-	-	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART2_CK	DFSDM1_DATIN1	-	-	FSMC_D6/ FSMC_DA6	-	-	EVENT OUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	TIM8_CH1N	-	SPI1_SCK/I2S1_CK	-	-	DFSDM1_CKIN1	-	-	FSMC_D7/ FSMC_DA7	-	-	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	TIM8_BKIN	-	SPI1_MISO	I2S2_MCK	DFSDM2_CKIN1	-	TIM13_CH1	QUADSPI_BK2_IO0	SDIO_CMD	-	-	EVENT OUT
	PA7	-	TIM1_CH1N	TIM3_CH2	TIM8_CH1N	-	SPI1_MOSI/I2S1_SD	-	DFSDM2_DATIN1	-	TIM14_CH1	QUADSPI_BK2_IO1	-	-	-	EVENT OUT
	PA8	MCO_1	TIM1_CH1	-	-	I2C3_SCL	-	DFSDM1_CKOUT	USART1_CK	UART7_RX	-	USB_FS_SOF	CAN3_RX	SDIO_D1	-	EVENT OUT
	PA9	-	TIM1_CH2	-	DFSDM2_CKIN3	I2C3_SMBA	SPI2_SCK/I2S2_CK	-	USART1_TX	-	-	USB_FS_VBUS	-	SDIO_D2	-	EVENT OUT
	PA10	-	TIM1_CH3	-	DFSDM2_DATIN3	-	SPI2_MOSI/I2S2_SD	SPI5_MOSI/I2S5_SD	USART1_RX	-	-	USB_FS_ID	-	-	-	EVENT OUT
	PA11	-	TIM1_CH4	-	DFSDM2_CKIN5	-	SPI2_NSS/I2S2_WS	SPI4_MISO	USART1_CTS	USART6_TX	CAN1_RX	USB_FS_DM	UART4_RX	-	-	EVENT OUT
	PA12	-	TIM1_ETR	-	DFSDM2_DATIN5	-	SPI2_MISO	SPI5_MISO	USART1_RTS	USART6_RX	CAN1_TX	USB_FS_DP	UART4_TX	-	-	EVENT OUT
	PA13	JTMS-SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK-SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_NSS/I2S1_WS	SPI3_NSS/I2S3_WS	USART1_TX	UART7_TX	-	SAI1_MCLK_A	CAN3_TX	-	-	EVENT OUT

Table 12. STM32F413xG/H alternate functions (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	TIM8_CH2N	-	-	SPI5_SCK/I2S5_CK	-	-	-	-	-	-	-	EVENT OUT
	PB1	-	TIM1_CH3N	TIM3_CH4	TIM8_CH3N	-	-	SPI5_NSS/I2S5_WS	-	DFSDM1_DATIN0	QUADSPI_CLK	-	-	-	-	EVENT OUT
	PB2	-	LPTIM1_OUT	-	-	-	-	DFSDM1_CKIN0	-	-	QUADSPI_CLK	-	-	-	-	EVENT OUT
	PB3	JTDO-SWO	TIM2_CH2	-	-	I2CFMP1_SDA	SPI1_SCK/I2S1_CK	SPI3_SCK/I2S3_CK	USART1_RX	UART7_RX	I2C2_SDA	SAI1_SD_A	CAN3_RX	-	-	EVENT OUT
	PB4	JTRST	-	TIM3_CH1	-	-	SPI1_MISO	SPI3_MISO	I2S3ext_SD	UART7_TX	I2C3_SDA	SAI1_SCK_A	CAN3_TX	SDIO_D0	-	EVENT OUT
	PB5	-	LPTIM1_IN1	TIM3_CH2	-	I2C1_SMB	SPI1_MOSI/I2S1_SD	SPI3_MOSI/I2S3_SD	-	-	CAN2_RX	SAI1_FS_A	UART5_RX	SDIO_D3	-	EVENT OUT
	PB6	-	LPTIM1_ETR	TIM4_CH1	-	I2C1_SCL	-	DFSDM2_CKIN7	USART1_TX	-	CAN2_TX	QUADSPI_BK1_NCS	UART5_TX	SDIO_D0	-	EVENT OUT
	PB7	-	LPTIM1_IN2	TIM4_CH2	-	I2C1_SDA	-	DFSDM2_DATIN7	USART1_RX	-	-	-	FSMC_NL	-	-	EVENT OUT
	PB8	-	LPTIM1_OUT	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	SPI5_MOSI/I2S5_SD	DFSDM2_CKIN1	CAN1_RX	I2C3_SDA	-	UART5_RX	SDIO_D4	-	EVENT OUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I2S2_WS	DFSDM2_DATIN1	-	CAN1_TX	I2C2_SDA	-	UART5_TX	SDIO_D5	-	EVENT OUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I2S2_CK	I2S3_MCK	USART3_TX	-	I2CFMP1_SCL	DFSDM2_CKOUT	-	SDIO_D7	-	EVENT OUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	I2S2_CKIN	-	USART3_RX	-	-	-	-	-	-	EVENT OUT
	PB12	-	TIM1_BKIN	-	-	I2C2_SMB	SPI2_NSS/I2S2_WS	SPI4_NSS/I2S4_WS	SPI3_SCK/I2S3_CK	USART3_CK	CAN2_RX	DFSDM1_DATIN1	UART5_RX	FSMC_D13/FSMC_DA13	-	EVENT OUT
	PB13	-	TIM1_CH1N	-	-	I2CFMP1_SMB	SPI2_SCK/I2S2_CK	SPI4_SCK/I2S4_CK	-	USART3_CTS	CAN2_TX	DFSDM1_CKIN1	UART5_TX	-	-	EVENT OUT
	PB14	-	TIM1_CH2N	-	TIM8_CH2N	I2CFMP1_SDA	SPI2_MISO	I2S2ext_SD	USART3_RTS	DFSDM1_DATIN2	TIM12_CH1	FSMC_D0/FSMC_DA0	-	SDIO_D6	-	EVENT OUT
	PB15	RTC_REFIN	TIM1_CH3N	-	TIM8_CH3N	I2CFMP1_SCL	SPI2_MOSI/I2S2_SD	-	-	DFSDM1_CKIN2	TIM12_CH2	-	-	SDIO_CK	-	EVENT OUT



Table 12. STM32F413xG/H alternate functions (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port C	PC0	-	LPTIM1_IN1	-	DFSDM2_CK_IN4	-	-	SAI1_MCLK_B	-	-	-	-	-	-	-	EVENT OUT
	PC1	-	LPTIM1_OUT	-	DFSDM2_DATA_IN4	-	-	SAI1_SD_B	-	-	-	-	-	-	-	EVENT OUT
	PC2	-	LPTIM1_IN2	-	DFSDM2_DATA_IN7	-	SPI2_MISO	I2S2ext_SD	SAI1_SCK_B	DFSDM1_CKOUT	-	-	FSMC_NWE	-	-	EVENT OUT
	PC3	-	LPTIM1_ETR	-	DFSDM2_CK_IN7	-	SPI2_MOSI/I2S2_SD	SAI1_FS_B	-	-	-	-	FSMC_A0	-	-	EVENT OUT
	PC4	-	-	-	DFSDM2_CK_IN2	-	I2S1_MCK	-	-	-	QUADSPI_BK2_IO2	-	FSMC_NE4	-	-	EVENT OUT
	PC5	-	-	-	DFSDM2_DATA_IN2	I2CFMP1_SMBA	-	USART3_RX	-	-	QUADSPI_BK2_IO3	-	FSMC_NOE	-	-	EVENT OUT
	PC6	-	-	TIM3_CH1	TIM8_CH1	I2CFMP1_SCL	I2S2_MCK	DFSDM1_CKIN3	DFSDM2_DATIN6	USART6_TX	FSMC_D1/FSMC_DA1	-	SDIO_D6	-	-	EVENT OUT
	PC7	-	-	TIM3_CH2	TIM8_CH2	I2CFMP1_SDA	SPI2_SCK/I2S2_CK	I2S3_MCK	DFSDM2_CKIN6	USART6_RX	DFSDM1_DATIN3	-	SDIO_D7	-	-	EVENT OUT
	PC8	-	-	TIM3_CH3	TIM8_CH3	-	-	-	DFSDM2_CKIN3	USART6_CK	QUADSPI_BK1_IO2	-	SDIO_D0	-	-	EVENT OUT
	PC9	MCO_2	-	TIM3_CH4	TIM8_CH4	I2C3_SDA	I2S2_CKIN	-	DFSDM2_DATIN3	-	QUADSPI_BK1_IO0	-	SDIO_D1	-	-	EVENT OUT
	PC10	-	-	-	DFSDM2_CKIN5	-	-	SPI3_SCK/I2S3_CK	USART3_TX	-	QUADSPI_BK1_IO1	-	SDIO_D2	-	-	EVENT OUT
	PC11	-	-	-	DFSDM2_DATIN5	-	I2S3ext_SD	SPI3_MISO	USART3_RX	UART4_RX	QUADSPI_BK2_NCS	FSMC_D2/FSMC_DA2	SDIO_D3	-	-	EVENT OUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/I2S3_SD	USART3_CK	UART5_TX	-	FSMC_D3/FSMC_DA3	SDIO_CK	-	-	EVENT OUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 12. STM32F413xG/H alternate functions (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/2/LPTIM1	TIM3/4/5	DFSDM2/TIM8/9/10/11	I2C1/2/3/I2CFMP1	SPI1/I2S1/SPI2/I2S2/SPI3/I2S3/SPI4/I2S4	SPI2/I2S2/SPI3/I2S3/SPI4/I2S4/SPI5/I2S5/DFSDM1/2	SPI3/I2S3/SAI1/DFSDM2/USART1/USART2/USART3	DFSDM1/USART3/4/5/6/7/8/CAN1	I2C2/I2C3/I2CFMP1/CAN1/2/TIM12/13/14/QUADSPI	SAI1/DFSDM1/DFSDM2/QUADSPI/FSMC/OTG1_FS	UART4/UART5/UART9/UART10/CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port D	PD0	-	-	-	DFSDM2_CKIN6	-	-	-	-	CAN1_RX	-	UART4_RX	FSMC_D2/FSMC_DA2	-	-	EVENT OUT
	PD1	-	-	-	DFSDM2_DATIN6	-	-	-	-	CAN1_TX	-	UART4_TX	FSMC_D3/FSMC_DA3	-	-	EVENT OUT
	PD2	-	-	TIM3_ETR	DFSDM2_CKOUT	-	-	-	UART5_RX	-	FSMC_NWE	-	SDIO_CMD	-	-	EVENT OUT
	PD3	TRACE D1	-	-	-	SPI2_SCK/I2S2_CK	DFSDM1_DATIN0	USART2_CTS	-	QUADSPI_CLK	-	-	FSMC_CLK	-	-	EVENT OUT
	PD4	-	-	-	-	-	DFSDM1_CKIN0	USART2_RTS	-	-	-	-	FSMC_NOE	-	-	EVENT OUT
	PD5	-	-	-	DFSDM2_CKOUT	-	-	USART2_TX	-	-	-	-	FSMC_NWE	-	-	EVENT OUT
	PD6	-	-	-	-	SPI3_MOSI/I2S3_SD	DFSDM1_DATIN1	USART2_RX	-	-	-	-	FSMC_NWAIT	-	-	EVENT OUT
	PD7	-	-	-	-	-	DFSDM1_CKIN1	USART2_CK	-	-	-	-	FSMC_NE1	-	-	EVENT OUT
	PD8	-	-	-	-	-	-	USART3_TX	-	-	-	-	FSMC_D13/FSMC_DA13	-	-	EVENT OUT
	PD9	-	-	-	-	-	-	USART3_RX	-	-	-	-	FSMC_D14/FSMC_DA14	-	-	EVENT OUT
	PD10	-	-	-	-	-	-	USART3_CK	UART4_TX	-	-	-	FSMC_D15/FSMC_DA15	-	-	EVENT OUT
	PD11	-	-	-	DFSDM2_DATIN2	I2CFMP1_SMBA	-	USART3_CTS	-	QUADSPI_BK1_IO0	-	-	FSMC_A16	-	-	EVENT OUT
	PD12	-	-	TIM4_CH1	DFSDM2_CKIN2	I2CFMP1_SCL	-	USART3_RTS	-	QUADSPI_BK1_IO1	-	-	FSMC_A17	-	-	EVENT OUT
	PD13	-	-	TIM4_CH2	-	I2CFMP1_SDA	-	-	-	QUADSPI_BK1_IO3	-	-	FSMC_A18	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	I2CFMP1_SCL	-	-	-	-	DFSDM2_CKIN0	UART9_RX	FSMC_D0/FSMC_DA0	-	-	EVENT OUT
	PD15	-	-	TIM4_CH4	-	I2CFMP1_SDA	-	-	-	-	DFSDM2_DATIN0	UART9_TX	FSMC_D1/FSMC_DA1	-	-	EVENT OUT



Table 12. STM32F413xG/H alternate functions (continued)

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
	SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port E	PE0	-	-	TIM4_ETR	DFSDM2_CKIN4	-	-	-	UART8_Rx	-	-	-	FSMC_NBL0	-	-	EVENT OUT
	PE1	-	-	-	DFSDM2_DATIN4	-	-	-	UART8_Tx	-	-	-	FSMC_NBL1	-	-	EVENT OUT
	PE2	TRACE CLK	-	-	-	SPI4_SCK/I2S4_CK	SPI5_SCK/I2S5_CK	SAI1_MCLK_A	-	QUADSPI_BK1_IO2	-	UART10_RX	FSMC_A23	-	-	EVENT OUT
	PE3	TRACE D0	-	-	-	-	-	SAI1_SD_B	-	-	-	UART10_TX	FSMC_A19	-	-	EVENT OUT
	PE4	TRACE D1	-	-	-	SPI4_NSS/I2S4_WS	SPI5_NSS/I2S5_WS	SAI1_SD_A	DFSDM1_DATIN3	-	-	-	FSMC_A20	-	-	EVENT OUT
	PE5	TRACE D2	-	-	TIM9_CH1	-	SPI4_MISO	SPI5_MISO	SAI1_SCK_A	DFSDM1_CKIN3	-	-	FSMC_A21	-	-	EVENT OUT
	PE6	TRACE D3	-	-	TIM9_CH2	-	SPI4_MOSI/I2S4_SD	SPI5_MOSI/I2S5_SD	SAI1_FS_A	-	-	-	FSMC_A22	-	-	EVENT OUT
	PE7	-	TIM1_ETR	-	-	-	DFSDM1_DATIN2	-	UART7_Rx	-	QUADSPI_BK2_IO0	-	FSMC_D4/FSMC_DA4	-	-	EVENT OUT
	PE8	-	TIM1_CH1N	-	-	-	DFSDM1_CKIN2	-	UART7_Tx	-	QUADSPI_BK2_IO1	-	FSMC_D5/FSMC_DA5	-	-	EVENT OUT
	PE9	-	TIM1_CH1	-	-	-	DFSDM1_CKOUT	-	-	-	QUADSPI_BK2_IO2	-	FSMC_D6/FSMC_DA6	-	-	EVENT OUT
	PE10	-	TIM1_CH2N	-	DFSDM2_DATIN0	-	-	-	-	-	QUADSPI_BK2_IO3	-	FSMC_D7/FSMC_DA7	-	-	EVENT OUT
	PE11	-	TIM1_CH2	-	DFSDM2_CKIN0	-	SPI4_NSS/I2S4_WS	SPI5_NSS/I2S5_WS	-	-	-	-	FSMC_D8/FSMC_DA8	-	-	EVENT OUT
	PE12	-	TIM1_CH3N	-	DFSDM2_DATIN7	-	SPI4_SCK/I2S4_CK	SPI5_SCK/I2S5_CK	-	-	-	-	FSMC_D9/FSMC_DA9	-	-	EVENT OUT
	PE13	-	TIM1_CH3	-	DFSDM2_CKIN7	-	SPI4_MISO	SPI5_MISO	-	-	-	-	FSMC_D10/FSMC_DA10	-	-	EVENT OUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI/I2S4_SD	SPI5_MOSI/I2S5_SD	-	-	-	DFSDM2_DATIN1	FSMC_D11/FSMC_DA11	-	-	EVENT OUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	DFSDM2_CKIN1	-	FSMC_D12/FSMC_DA12	-	-	EVENT OUT

Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15	
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF	
Port F	PF0	-	-	-	-	I2C2_SDA	-	-	-	-	-	-	-	FSMC_A0	-	-	EVENT OUT	
	PF1	-	-	-	-	I2C2_SCL	-	-	-	-	-	-	-	FSMC_A1	-	-	EVENT OUT	
	PF2	-	-	-	-	I2C2_SMBA	-	-	-	-	-	-	-	FSMC_A2	-	-	EVENT OUT	
	PF3	-	-	TIM5_CH1	-	-	-	-	-	-	-	-	-	FSMC_A3	-	-	EVENT OUT	
	PF4	-	-	TIM5_CH2	-	-	-	-	-	-	-	-	-	FSMC_A4	-	-	EVENT OUT	
	PF5	-	-	TIM5_CH3	-	-	-	-	-	-	-	-	-	FSMC_A5	-	-	EVENT OUT	
	PF6	TRACE_D0	-	-	TIM10_CH1	-	-	-	SAI1_SD_B	UART7_Rx	QUADSPI_BK1_IO3	-	-	-	-	-	EVENT OUT	
	PF7	TRACE_D1	-	-	TIM11_CH1	-	-	-	SAI1_MCLK_B	UART7_Tx	QUADSPI_BK1_IO2	-	-	-	-	-	EVENT OUT	
	PF8	-	-	-	-	-	-	-	SAI1_SCK_B	UART8_RX	TIM13_CH1	QUADSPI_BK1_IO0	-	-	-	-	EVENT OUT	
	PF9	-	-	-	-	-	-	-	SAI1_FS_B	UART8_TX	TIM14_CH1	QUADSPI_BK1_IO1	-	-	-	-	EVENT OUT	
	PF10	-	TIM1_ETR	TIM5_CH4	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF11	-	-	-	TIM8_ETR	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PF12	-	-	-	TIM8_BKIN	-	-	-	-	-	-	-	-	-	FSMC_A6	-	-	EVENT OUT
	PF13	-	-	-	-	I2CFMP1_SMBA	-	-	-	-	-	-	-	-	FSMC_A7	-	-	EVENT OUT
	PF14	-	-	-	-	I2CFMP1_SCL	-	-	-	-	-	-	-	-	FSMC_A8	-	-	EVENT OUT
	PF15	-	-	-	-	I2CFMP1_SDA	-	-	-	-	-	-	-	-	FSMC_A9	-	-	EVENT OUT



Table 12. STM32F413xG/H alternate functions (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/2/ LPTIM1	TIM3/4/5	DFSDM2/ TIM8/9/10/11	I2C1/2/3/ I2CFMP1	SPI1/I2S1/ SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4	SPI2/I2S2/ SPI3/I2S3/ SPI4/I2S4/ SPI5/I2S5/ DFSDM1/2	SPI3/I2S3/ SAI1/ DFSDM2/ USART1/ USART2/ USART3	DFSDM1/ USART3/4/ 5/6/7/8/ CAN1	I2C2/I2C3/ I2CFMP1/ CAN1/2/ TIM12/13/14/ QUADSPI	SAI1/ DFSDM1/ DFSDM2/ QUADSPI/ FSMC /OTG1_FS	UART4/ UART5/ UART9/ UART10 /CAN3	FSMC /SDIO	-	RNG	SYS_AF
Port G	PG0	-	-	-	-	-	-	-	-	-	CAN1_RX	-	UART9_RX	FSMC_A10	-	-	EVENT OUT
	PG1	-	-	-	-	-	-	-	-	-	CAN1_TX	-	UART9_TX	FSMC_A11	-	-	EVENT OUT
	PG2	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A12	-	-	EVENT OUT
	PG3	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A13	-	-	EVENT OUT
	PG4	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A14	-	-	EVENT OUT
	PG5	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_A15	-	-	EVENT OUT
	PG6	-	-	-	-	-	-	-	-	-	-	QUADSPI_B K1_NCS	-	-	-	-	EVENT OUT
	PG7	-	-	-	-	-	-	-	-	USART6_ CK	-	-	-	-	-	-	EVENT OUT
	PG8	-	-	-	-	-	-	-	-	USART6_ RTS	-	-	-	-	-	-	EVENT OUT
	PG9	-	-	-	-	-	-	-	-	USART6_ RX	QUADSPI_ BK2_IO2	-	-	FSMC_NE2	-	-	EVENT OUT
	PG10	-	-	-	-	-	-	-	-	-	-	-	-	FSMC_NE3	-	-	EVENT OUT
	PG11	-	-	-	-	-	-	-	-	-	CAN2_RX	-	UART10_RX	-	-	-	EVENT OUT
	PG12	-	-	-	-	-	-	-	-	USART6_ RTS	CAN2_TX	-	UART10_TX	FSMC_NE4	-	-	EVENT OUT
	PG13	TRACE D2	-	-	-	-	-	-	-	USART6_ CTS	-	-	-	FSMC_A24	-	-	EVENT OUT
	PG14	TRACE D3	-	-	-	-	-	-	-	USART6_ TX	QUADSPI_ BK2_IO3	-	-	FSMC_A25	-	-	EVENT OUT
	PG15	-	-	-	-	-	-	-	-	USART6_ CTS	-	-	-	-	-	-	EVENT OUT
Port H	PH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PH1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

5 Memory mapping

The memory map is shown in [Figure 18](#).

Figure 18. Memory map

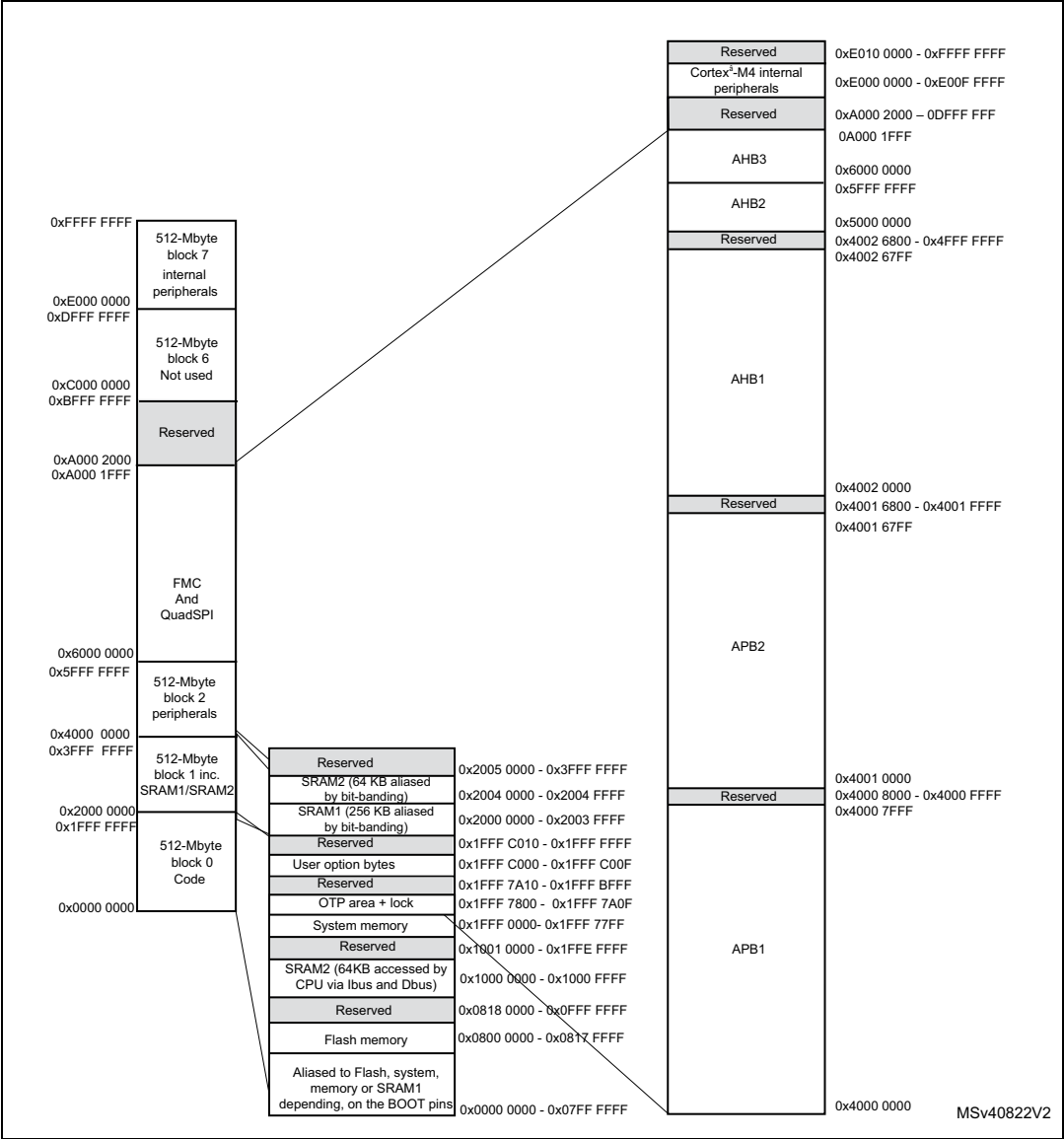


Table 13. STM32F413xG/H register boundary addresses

Bus	Boundary address	Peripheral
	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex [®] -M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
AHB3	0xA000 2000 - 0xDFFF FFFF	Reserved
	0xA000 1000 - 0xA000 1FFF	QuadSPI control register
	0xA000 0000 - 0xA000 0FFF	FSMC control register
	0x9000 0000 - 0x9FFF FFFF	QUADSPI
	0x7000 0000 - 0x08FFF FFFF	Reserved
	0x6000 0000 - 0x6FFF FFFF	FSMC
AHB2	0x5006 0C00 - 0x5FFF FFFF	Reserved
	0x5006 0800 - 0x5006 0BFF	RNG
	0x5004 0000 - 0x5006 07FF	Reserved
	0x5000 0000 - 0x5003 FFFF	USB OTG FS
AHB1	0x4002 6800 - 0x4FFF FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 4000 - 0x4002 5FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2000 - 0x4002 2FFF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1800 - 0x4002 1BFF	GPIOG
	0x4002 1400 - 0x4002 17FF	GPIOF
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GIOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

Table 13. STM32F413xG/H register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 6800 - 0x4001 FFFF	Reserved
	0x4001 6400 - 0x4001 67FF	DFSDM2
	0x4001 6000 - 0x4001 63FF	DFSDM1
	0x4001 5C00 - 0x4001 5FFF	Reserved
	0x4001 5800 - 0x4001 5BFF	SAI1
	0x4001 5400 - 0x4001 57FF	Reserved
	0x4001 5000 - 0x4001 53FF	SPI5/I2S5
	0x4001 4C00 - 0x4001 4FFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1/2/3
	0x4001 1C00 - 0x4001 1FFF	UART10
	0x4001 1800 - 0x4001 1BFF	UART9
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1

Table 13. STM32F413xG/H register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB1	0x4000 8000 - 0x4000 FFFF	Reserved
	0x4000 7C00 - 0x4000 7FFF	UART8
	0x4000 7800 - 0x4000 7BFF	UART7
	0x4000 7400 - 0x4000 77FF	DAC1
	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6C00 - 0x4000 6FFF	CAN3
	0x4000 6800 - 0x4000 6BFF	CAN2
	0x4000 6400 - 0x4000 67FF	CAN1
	0x4000 6000 - 0x4000 63FF	I2CFMP1
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 5000 - 0x4000 53FF	UART5
	0x4000 4C00 - 0x4000 4FFF	UART4
	0x4000 4800 - 0x4000 4BFF	USART3
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 2400 - 0x4000 27FF	LPTIM1
	0x4000 2000 - 0x4000 23FF	TIM14
	0x4000 1C00 - 0x4000 1FFF	TIM13
	0x4000 1800 - 0x4000 1BFF	TIM12
	0x4000 1400 - 0x4000 17FF	TIM7
	0x4000 1000 - 0x4000 13FF	TIM6
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^{\circ}\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 3.3\text{ V}$ (for the $1.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$ voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

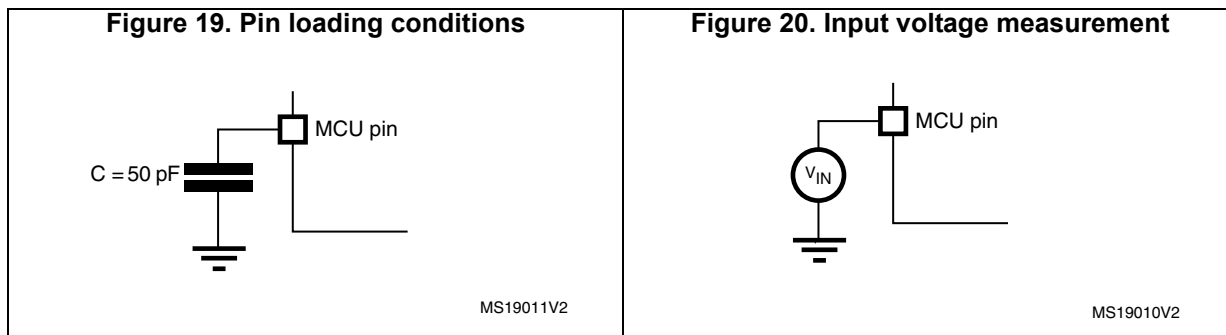
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 19](#).

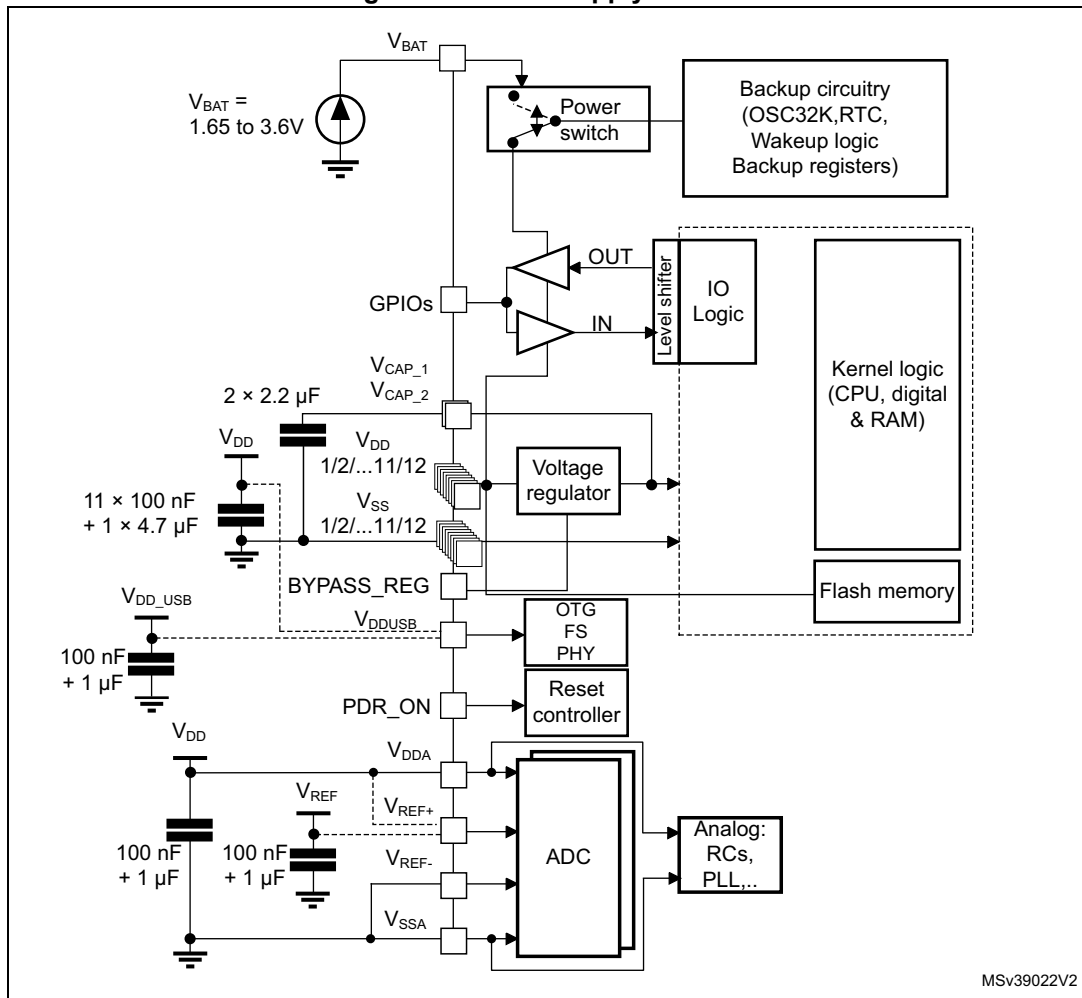
6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 20](#).



6.1.6 Power supply scheme

Figure 21. Power supply scheme

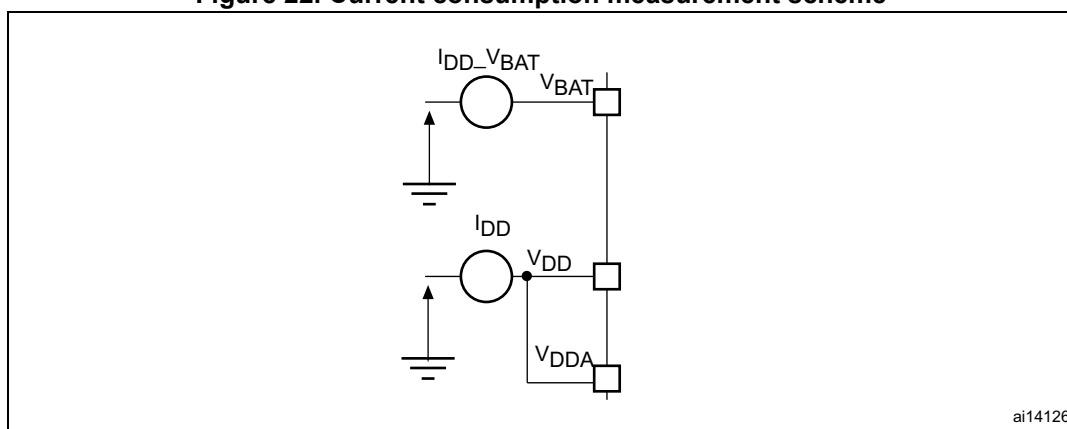


1. To connect PDR_ON pin, refer to Section: Power supply supervisor.
2. The 4.7 μF ceramic capacitor must be connected to one of the V_{DD} pin.
3. VCAP_2 pad is only available on 100-pin and 144-pin packages.
4. $V_{\text{DDA}}=V_{\text{DD}}$ and $V_{\text{SSA}}=V_{\text{SS}}$.
5. V_{DDUSB} is a dedicated independent USB power supply for the on-chip full-speed OTG PHY module and associated DP/DM GPIOs. V_{DDUSB} value does not depend on the V_{DD} and V_{DDA} values, but it must be the last supply to be provided and the first to disappear.

Caution: Each power supply pair (for example V_{DD}/V_{SS} , V_{DDA}/V_{SSA}) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 22. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 14: Voltage characteristics](#), [Table 15: Current characteristics](#), and [Table 16: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} , V_{DD} , V_{DDUSB} and V_{BAT}) ⁽¹⁾	-0.3	4.0	V
V_{IN}	Input voltage on FT and TC pins ⁽²⁾	$V_{SS}-0.3$	$V_{DD}+4.0$	
	Input voltage on TTa pins	$V_{SS}-0.3$	4.0	
	Input voltage on any other pin	$V_{SS}-0.3$	4.0	
	Input voltage for BOOT0	V_{SS}	9.0	
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx}-V_{SS} $	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.14: Absolute maximum ratings (electrical sensitivity)		

1. All main power (V_{DD} , V_{DDA} , V_{DDUSB}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to [Table 15](#) for the values of the maximum allowed injected current.

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source) ⁽¹⁾	180	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink) ⁽¹⁾	-180	
ΣI_{VDDUSB}	Total current into V_{DDUSB} power lines (source)	25	
I_{VDD}	Maximum current into each V_{DD_x} power line (source) ⁽¹⁾	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink) ⁽¹⁾	-100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins ⁽²⁾	120	
	Total output current sunk by sum of all USB I/Os	25	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-120	
$I_{INJ(PIN)}^{(3)}$	Injected current on FT and TC pins ⁽⁴⁾	– 5/ + 0	
	Injected current on NRST and B pins ⁽⁴⁾		
	Injected current on TTa pins ⁽⁵⁾	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	

1. All main power (V_{DD} , V_{DDA} , V_{DDUSB}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins.
3. Negative injection disturbs the analog performance of the device. See note in [Section 6.3.20: 12-bit ADC characteristics](#).
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ in the same time a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 14](#) for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	125	
T_{LEAD}	Maximum lead temperature during soldering (WLCSP81, LQFP64/100/144, UFQFPN48, UFBGA100/144)	see note ⁽¹⁾	

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

6.3 Operating conditions

6.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	64	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
		Power Scale1: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x11	0	-	100	
f_{PCLK1}	Internal APB1 clock frequency	-	0	-	50	MHz
f_{PCLK2}	Internal APB2 clock frequency	-	0	-	100	MHz
V_{DD}	Standard operating voltage	-	1.7 ⁽¹⁾	-	3.6	V
$V_{DDA}^{(2)(3)}$	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as $V_{DD}^{(4)}$	1.7 ⁽¹⁾	-	2.4	V
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{DDUSB}	USB supply voltage (supply voltage for PA11 and PA12 pins)	USB not used	1.7	3.3	3.6	V
		USB used ⁽⁵⁾	3.0	-	3.6	
V_{BAT}	Backup operating voltage	-	1.65	-	3.6	V
V_{12}	Regulator ON: 1.2 V internal voltage on VCAP_1/VCAP_2 pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 64 MHz	1.08 ⁽⁶⁾	1.14	1.20 ⁽⁶⁾	V
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20 ⁽⁶⁾	1.26	1.32 ⁽⁶⁾	
		VOS[1:0] bits in PWR_CR register = 0x11 Max frequency 100 MHz	1.26	1.32	1.38	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on VCAP_1/VCAP_2 pins	Max frequency 64 MHz	1.10	1.14	1.20	V
		Max frequency 84 MHz	1.20	1.26	1.32	
		Max frequency 100 MHz	1.26	1.32	1.38	

Table 17. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage on RST, FT and TC pins ⁽⁷⁾	$2\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	-0.3	-	5.5	V
		$V_{DD} \leq 2\text{ V}$	-0.3	-	5.2	
	Input voltage on TTa pins	-	-0.3	-	$V_{DDA} + 0.3$	
	Input voltage on BOOT0 pin	-	0	-	9	
P_D	Power dissipation at $T_A = 85^\circ\text{C}$ for range 6 or $T_A = 105^\circ\text{C}$ for range 7 ⁽⁸⁾	UFQFPN48	-	-	625	mW
		WLCSP81	-	-	504	
		LQFP64	-	-	426	
		LQFP100	-	-	465	
		LQFP144	-	-	571	
		UFBGA100	-	-	351	
		UFBGA144	-	-	417	
	Power dissipation at $T_A = 125^\circ\text{C}$ for range 3 ⁽⁸⁾	UFQFPN48	-	-	156	
		WLCSP81	-	-	126	
		LQFP64	-	-	106	
		LQFP100	-	-	116	
		LQFP144	-	-	143	
		UFBGA100	-	-	088	
		UFBGA144	-	-	104	
T_A	Ambient temperature for range 6	Maximum power dissipation	-40	-	85	$^\circ\text{C}$
		Low power dissipation ⁽⁹⁾	-40	-	105	
	Ambient temperature for range 7	Maximum power dissipation	-40	-	105	
		Low power dissipation ⁽⁹⁾	-40	-	125	
	Ambient temperature for range 3	Maximum power dissipation	-40	-	125	
		Low power dissipation ⁽⁹⁾	-40	-	130	
T_J	Junction temperature range	Range 6	-40	-	105	
		Range 7	-40	-	125	
		Range 3	-40	-	130	

- V_{DD}/V_{DDA} minimum value of 1.7 V with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).
- When the ADC is used, refer to [Table 75: ADC characteristics](#).
- If V_{REF+} pin is present, it must respect the following condition: $V_{DDA} - V_{REF+} < 1.2\text{ V}$.
- It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and power-down operation.
- Only the DM (P_{A11}) and DP (P_{A12}) pads are supplied through V_{DDUSB} . For application where the V_{BUS} (P_{A9}) is directly connected to the chip, a minimum V_{DD} supply of 2.7V is required. (some application examples are shown in appendix B)
- Guaranteed by test in production
- To sustain a voltage higher than $V_{DD} + 0.3$, the internal Pull-up and Pull-Down resistors must be disabled

8. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} .
9. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} .

Table 18. Features depending on the operating power supply range

Operating power supply range	ADC operation	Maximum Flash memory access frequency with no wait states ($f_{Flashmax}$)	Maximum Flash memory access frequency with wait states ⁽¹⁾⁽²⁾	I/O operation	Clock output frequency on I/O pins ⁽³⁾	Possible Flash memory operations
$V_{DD} = 1.7$ to 2.1 V ⁽⁴⁾	Conversion time up to 1.2 Msps	16 MHz ⁽⁵⁾	100 MHz with 6 wait states	– No I/O compensation	up to 30 MHz	8-bit erase and program operations only
$V_{DD} = 2.1$ to 2.4 V	Conversion time up to 1.2 Msps	18 MHz	100 MHz with 5 wait states	– No I/O compensation	up to 30 MHz	16-bit erase and program operations
$V_{DD} = 2.4$ to 2.7 V	Conversion time up to 2.4 Msps	20 MHz	100 MHz with 4 wait states	– I/O compensation works	up to 50 MHz	16-bit erase and program operations
$V_{DD} = 2.7$ to 3.6 V ⁽⁶⁾	Conversion time up to 2.4 Msps	25 MHz	100 MHz with 3 wait states	– I/O compensation works	– up to 100 MHz when $V_{DD} = 3.0$ to 3.6 V – up to 50 MHz when $V_{DD} = 2.7$ to 3.0 V	32-bit erase and program operations

1. Applicable only when the code is executed from Flash memory. When the code is executed from RAM, no wait state is required.
2. Thanks to the ART accelerator and the 128-bit Flash memory, the number of wait states given here does not impact the execution speed from Flash memory since the ART accelerator allows to achieve a performance equivalent to 0 wait state program execution.
3. Refer to [Table 61: I/O AC characteristics](#) for frequencies vs. external load.
4. V_{DD}/V_{DDA} minimum value of 1.7 V, with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).
5. Prefetch available over the complete VDD supply range.
6. The voltage range for the USB full speed embedded PHY can drop down to 2.7 V. However the electrical characteristics of D- and D+ pins will be degraded between 2.7 and 3 V.

6.3.2 VCAP_1/VCAP_2 external capacitors

Stabilization for the main regulator is achieved by connecting the external capacitor C_{EXT} to the VCAP_1 and VCAP_2 pins. For packages supporting only 1 VCAP pin, the 2 CEXT capacitors are replaced by a single capacitor.

C_{EXT} is specified in [Table 19](#).

Figure 23. External capacitor C_{EXT}



1. Legend: ESR is the equivalent series resistance.

Table 19. VCAP_1/VCAP_2 operating conditions⁽¹⁾

Symbol	Parameter	Conditions
CEXT	Capacitance of external capacitor with the pins VCAP_1 and VCAP_2 available	2.2 μ F
ESR	ESR of external capacitor with the pins VCAP_1 and VCAP_2 available	< 2 Ω
CEXT	Capacitance of external capacitor with a single VCAP pin available	4.7 μ F
ESR	ESR of external capacitor with a single VCAP pin available	< 1 Ω

1. When bypassing the voltage regulator, the two 2.2 μ F V_{CAP} capacitors are not required and should be replaced by two 100 nF decoupling capacitors.

6.3.3 Operating conditions at power-up/power-down (regulator ON)

Subject to general operating conditions for T_A .

Table 20. Operating conditions at power-up / power-down (regulator ON)

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	20	∞	μ s/V
	V_{DD} fall time rate	20	∞	

6.3.4 Operating conditions at power-up / power-down (regulator OFF)

Subject to general operating conditions for T_A .

Table 21. Operating conditions at power-up / power-down (regulator OFF)⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	Power-up	20	∞	$\mu s/V$
	V_{DD} fall time rate	Power-down	20	∞	
t_{VCAP}	V_{CAP_1} and V_{CAP_2} rise time rate	Power-up	20	∞	
	V_{CAP_1} and V_{CAP_2} fall time rate	Power-down	20	∞	

1. To reset the internal logic at power-down, a reset must be applied on pin PA0 when V_{DD} reach below 1.08 V.

Note: This feature is only available for UFBGA100 and UFBGA144 packages.

6.3.5 Embedded reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage @ 3.3V.

Table 22. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.09	2.14	2.19	V
		PLS[2:0]=000 (falling edge)	1.98	2.04	2.08	
		PLS[2:0]=001 (rising edge)	2.23	2.30	2.37	
		PLS[2:0]=001 (falling edge)	2.13	2.19	2.25	
		PLS[2:0]=010 (rising edge)	2.39	2.45	2.51	
		PLS[2:0]=010 (falling edge)	2.29	2.35	2.39	
		PLS[2:0]=011 (rising edge)	2.54	2.60	2.65	
		PLS[2:0]=011 (falling edge)	2.44	2.51	2.56	
		PLS[2:0]=100 (rising edge)	2.70	2.76	2.82	
		PLS[2:0]=100 (falling edge)	2.59	2.66	2.71	
		PLS[2:0]=101 (rising edge)	2.86	2.93	2.99	
		PLS[2:0]=101 (falling edge)	2.65	2.84	3.02	
		PLS[2:0]=110 (rising edge)	2.96	3.03	3.10	
		PLS[2:0]=110 (falling edge)	2.85	2.93	2.99	
		PLS[2:0]=111 (rising edge)	3.07	3.14	3.21	
		PLS[2:0]=111 (falling edge)	2.95	3.03	3.09	
$V_{PVDhyst}^{(2)}$	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power-on/power-down reset threshold	Falling edge	1.60 ⁽¹⁾	1.68	1.76	V
		Rising edge	1.64	1.72	1.80	

Table 22. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{PDRhyst}^{(2)}$	PDR hysteresis	-	-	40	-	mV
V_{BOR1}	Brownout level 1 threshold	Falling edge	2.13	2.19	2.24	V
		Rising edge	2.23	2.29	2.33	
V_{BOR2}	Brownout level 2 threshold	Falling edge	2.44	2.50	2.56	
		Rising edge	2.53	2.59	2.63	
V_{BOR3}	Brownout level 3 threshold	Falling edge	2.75	2.83	2.88	
		Rising edge	2.85	2.92	2.97	
$V_{BORhyst}^{(2)}$	BOR hysteresis	-	-	100	-	mV
$T_{RSTTEMPO}^{(2)(3)}$	POR reset timing	-	0.5	1.5	3.0	ms
$I_{RUSH}^{(2)}$	In-Rush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	160	200	mA
$E_{RUSH}^{(2)}$	In-Rush energy on voltage regulator power-on (POR or wakeup from Standby)	$V_{DD} = 1.7\text{ V}$, $T_A = 125\text{ }^{\circ}\text{C}$, $I_{RUSH} = 171\text{ mA}$ for $31\text{ }\mu\text{s}$	-	-	5.4	μC

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design.
3. The reset timing is measured from the power-on (POR reset or wakeup from V_{BAT}) to the instant when first instruction is fetched by the user application code.

6.3.6 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 22: Current consumption measurement scheme](#).

All the run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to [Table 18: Features depending on the operating power supply range](#)).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
 - Scale 3 for $f_{HCLK} \leq 64$ MHz
 - Scale 2 for $64 \text{ MHz} < f_{HCLK} \leq 84$ MHz
 - Scale 1 for $84 \text{ MHz} < f_{HCLK} \leq 100$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is ON except if it is explicitly mentioned.
- The maximum values are obtained for $V_{DD} = 3.6$ V and a maximum ambient temperature (T_A), and the typical values for $T_A = 25$ °C and $V_{DD} = 3.3$ V unless otherwise specified.

Table 23. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD} = 1.7$ V

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A =85 °C	T _A =105 °C	T _A =125 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON, all peripherals enabled ⁽²⁾⁽³⁾	100	32.9	34.96	35.30	37.21	40.79	mA	
			84	26.5	28.13	28.58	30.50	33.96		
			64	18.3	19.44	20.11	21.76	25.03		
			50	14.4	15.28	16.12	17.95	21.11		
			25	7.5	8.10	9.35	11.09	14.38		
			20	6.4	6.99	8.17	9.96	13.17		
		HSI, PLL off, all peripherals enabled ⁽²⁾⁽³⁾	16	4.6	5.17	6.42	8.28	11.46		
			1	0.7	1.28	2.64	4.30	7.66		
		External clock, PLL ON, all peripherals disabled ⁽³⁾	100	15.4	16.43	17.35	19.17	22.85		
			84	12.4	13.28	14.32	16.12	19.67		
			64	8.7	9.36	10.38	12.06	15.31		
			50	6.9	7.47	8.54	10.36	13.49		
			25	3.7	4.27	5.47	7.17	10.45		
			20	3.2	3.72	5.01	6.67	10.02		
		HSI, PLL off, all peripherals disabled ⁽³⁾	16	2.3	2.80	4.05	5.90	9.07		
			1	0.6	1.14	2.51	4.16	7.51		

1. Guaranteed by characterization results.

2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.

3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

Table 24. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - $V_{DD} = 3.6$ V

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON, all peripherals enabled ⁽²⁾	100	33.3	35.32 ⁽³⁾	35.65	37.65	41.26 ⁽³⁾	mA	
			84	26.8	28.45 ⁽³⁾	28.97	30.82	34.39 ⁽³⁾		
			64	18.6	19.74 ⁽³⁾	20.35	22.11	25.35 ⁽³⁾		
			50	14.6	15.57	16.41	18.21	21.46		
			25	7.8	8.37	9.64	11.32	14.68		
			20	6.7	7.25	8.40	10.25	13.45		
		HSI, PLL OFF ⁽⁴⁾ , all peripherals enabled ⁽²⁾	16	4.6	4.96	6.39	8.20	11.54		
			1	0.8	0.86	2.51	4.34	7.65		
		External clock, PLL ON, all peripherals disabled ⁽²⁾	100	15.7	16.74 ⁽³⁾	17.62	19.50	23.16 ⁽³⁾		
			84	12.7	13.57 ⁽³⁾	14.60	16.38	19.98 ⁽³⁾		
			64	9.0	9.62 ⁽³⁾	10.60	12.37	15.58 ⁽³⁾		
			50	7.1	7.69	8.79	10.63	13.79		
			25	4.0	4.52	5.68	7.44	10.68		
			20	3.4	4.03	5.23	6.90	10.27		
		HSI, PLL OFF, all peripherals disabled ⁽²⁾	16	2.3	2.44	4.00	5.81	9.13		
			1	0.6	0.70	2.35	4.18	7.49		

1. Guaranteed by characterization results.
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
3. Tested in production
4. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- $V_{DD} = 1.7\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON, all peripherals enabled ⁽²⁾⁽³⁾	100	30.2	32.03	32.71	34.69	38.46	mA	
			84	24.3	25.77	26.58	28.47	32.16		
			64	16.8	17.80	18.66	20.53	23.85		
			50	13.2	14.05	15.12	16.85	20.27		
			25	7.1	7.62	8.92	10.81	14.11		
			20	6.1	6.69	7.95	9.72	13.09		
		HSI, PLL OFF, all peripherals enabled ⁽²⁾	16	4.4	4.99	6.28	8.18	11.45		
			1	0.9	1.50	2.88	4.58	8.00		
		External clock, PLL ON ⁽⁴⁾ all peripherals disabled ⁽²⁾	100	12.6	13.46	14.75	16.68	20.54		
			84	10.2	10.90	12.25	14.10	17.84		
			64	7.2	7.70	8.95	10.81	14.14		
			50	5.7	6.26	7.56	9.26	12.72		
			25	3.2	3.77	5.11	6.82	10.26		
			20	2.9	3.41	4.79	6.49	9.92		
		HSI, PLL OFF, all peripherals disabled ⁽²⁾	16	2.1	2.63	3.91	5.80	9.06		
			1	0.8	1.34	2.72	4.42	7.86		

1. Guaranteed by characterization results..

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

4. Refer to [Table 47](#) and RM0383 for the possible PLL VCO setting

Table 26. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - $V_{DD} = 3.6\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON ⁽²⁾ , all peripherals enabled ⁽³⁾	100	30.7	32.85 ⁽⁴⁾	33.30	35.37	39.08	mA	
			84	24.7	26.48	27.15	28.94	32.65		
			64	17.2	18.36	19.14	20.88	24.29		
			50	13.6	14.54	15.45	17.27	20.58		
			25	7.4	7.97	9.23	11.05	14.42		
			20	6.4	6.99	8.18	10.03	13.32		
		HSI, PLL OFF, all peripherals enabled ⁽³⁾	16	4.5	5.04	6.32	8.23	11.50		
			1	1.0	1.50	2.89	4.59	8.01		
		External clock, PLL ON ⁽²⁾ all peripherals disabled ⁽³⁾	100	13.1	14.36	15.33	17.25	20.98		
			84	10.7	11.67	12.73	14.56	18.21		
			64	7.5	8.23	9.40	11.13	14.52		
			50	6.1	6.74	7.89	9.61	12.98		
			25	3.5	4.19	5.37	7.08	10.48		
			20	3.2	3.71	5.02	6.72	10.15		
		HSI, PLL OFF, all peripherals disabled ⁽³⁾	16	2.1	2.67	3.95	5.84	9.10		
			1	0.8	1.35	2.72	4.43	7.87		

1. Guaranteed by characterization results.

2. Refer to [Table 47](#) and RM0383 for the possible PLL VCO setting

3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

4. Tested in production.

Table 27. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD} = 3.6\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON ⁽²⁾ , all peripherals enabled ⁽³⁾	100	39.9	42.46	43.17	45.32	49.19	mA	
			84	32.6	34.71	35.45	37.58	41.24		
			64	24.2	25.86	26.73	28.47	31.96		
			50	19.7	21.01	22.00	23.74	27.26		
			25	10.8	11.55	12.83	14.66	18.03		
			20	9.2	9.82	11.16	13.09	16.36		
		HSI, PLL OFF, all peripherals enabled ⁽³⁾	16	6.8	7.33	8.77	10.69	14.00		
			1	1.2	1.83	3.08	4.83	8.19		
		External clock, PLL ON ⁽²⁾ all peripherals disabled ⁽³⁾	100	22.3	24.11	25.26	27.35	31.11		
			84	18.5	20.00	21.15	23.20	26.87		
			64	14.6	15.81	17.02	18.74	22.20		
			50	12.2	13.14	14.45	16.18	19.66		
			25	7.0	7.52	8.95	10.84	14.19		
			20	6.0	6.58	7.95	9.74	13.07		
		HSI, PLL OFF, all peripherals disabled ⁽³⁾	16	4.5	4.97	6.40	8.30	11.59		
			1	1.0	1.61	2.94	4.65	8.05		

1. Guaranteed by characterization results.

2. Refer to [Table 47](#) and RM0383 for the possible PLL VCO setting

3. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 28. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory - $V_{DD} = 1.7\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON, all peripherals enabled ⁽²⁾⁽³⁾	100	36.1	38.48	39.08	40.91	44.59	mA	
			84	30.6	32.60	33.14	35.10	38.56		
			64	23.9	25.67	26.27	27.94	31.19		
			50	18.9	20.32	21.04	22.85	26.10		
			25	10.8	11.63	12.75	14.56	17.87		
			20	9.2	9.84	11.06	12.98	16.23		
		HSI, PLL OFF, all peripherals enabled ⁽²⁾⁽³⁾	16	7.1	7.69	9.02	10.87	14.25		
			1	1.2	1.84	3.10	4.84	8.20		
		External clock, PLL ON ⁽³⁾ all peripherals disabled	100	18.6	20.33	21.23	23.15	26.71		
			84	16.5	18.09	19.01	20.81	24.29		
			64	14.3	15.76	16.67	18.28	21.50		
			50	11.5	12.57	13.53	15.33	18.49		
			25	7.0	7.67	8.90	10.76	14.05		
			20	6.0	6.68	7.87	9.65	12.96		
		HSI, PLL OFF, all peripherals disabled ⁽³⁾	16	4.8	5.33	6.66	8.49	11.86		
			1	1.0	1.62	2.95	4.66	8.06		

1. Guaranteed by characterization results.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

Table 29. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - $V_{DD} = 3.6\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON, all peripherals enabled ⁽²⁾	100	42.3	45.08	45.76	47.88	51.71	mA	
			84	34.6	36.87	37.58	39.64	43.32		
			64	25.5	27.18	27.93	29.90	33.23		
			50	20.2	21.55	22.50	24.34	27.73		
			25	10.9	11.61	12.87	14.72	18.08		
			20	9.3	9.86	11.20	13.13	16.41		
		HSI, PLL OFF, all peripherals enabled	16	6.9	7.37	8.81	10.72	14.04		
			1	1.2	1.83	3.09	4.83	8.19		
		External clock, PLL ON ⁽²⁾ all peripherals disabled	100	24.7	26.76	27.84	29.93	33.66		
			84	20.5	22.18	23.25	25.33	28.98		
			64	15.9	17.13	18.23	20.18	23.46		
			50	12.7	13.68	14.95	16.71	20.13		
			25	7.1	7.57	9.01	10.88	14.25		
			20	6.1	6.61	7.98	9.80	13.11		
		HSI, PLL OFF, all peripherals disabled	16	4.5	5.00	6.44	8.33	11.63		
			1	1.0	1.61	2.94	4.65	8.06		

1. Guaranteed by characterization results.

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 30. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory - $V_{DD} = 1.7\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Run mode	External clock, PLL ON, all peripherals enabled ⁽²⁾	100	42.9	45.86	45.76	47.88	51.71	mA	
			84	35.4	37.90	38.16	40.01	43.26		
			64	26.2	28.19	28.74	30.37	33.54		
			50	20.7	22.32	22.50	24.34	27.73		
			25	11.1	11.87	12.87	14.72	18.08		
			20	9.4	10.05	11.26	13.16	16.46		
		HSI, PLL OFF, all peripherals enabled	16	7.1	7.72	9.06	10.90	14.29		
			1	1.2	1.84	3.10	4.84	8.20		
		External clock, PLL ON ⁽²⁾ all peripherals disabled	100	25.4	27.83	27.84	29.93	33.66		
			84	21.4	23.44	24.10	25.77	29.04		
			64	16.6	18.31	19.17	20.72	23.86		
			50	13.2	15.10	14.95	16.71	20.13		
			25	7.2	7.90	9.01	10.88	14.25		
			20	6.2	6.83	8.05	9.88	13.15		
		HSI, PLL OFF, all peripherals disabled	16	4.8	5.37	6.70	8.52	11.89		
			1	1.0	1.62	2.96	4.67	8.07		

1. Guaranteed by characterization results.

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 31. Typical and maximum current consumption in Sleep mode - $V_{DD} = 3.6\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Sleep mode	All peripherals enabled ⁽²⁾⁽³⁾ , External clock, PLL ON, Flash deep power down	100	21.6	22.97 ⁽⁴⁾	23.91	25.99	29.72	mA	
			84	17.4	18.50	19.59	21.42	25.09		
			64	12.0	12.81	13.87	15.73	19.00		
			50	9.5	10.15	11.33	13.22	16.44		
			25	5.2	5.79	7.11	8.82	12.18		
			20	4.6	5.17	6.41	8.28	11.48		
		All peripherals enabled ⁽²⁾⁽³⁾ , HSI, PLL OFF, Flash deep power down	16	3.0	3.24	4.78	6.60	9.94		
			1	0.7	0.76	2.41	4.23	7.55		
		All peripherals enabled ⁽²⁾⁽³⁾ , External clock, PLL ON Flash ON	100	22.0	23.42	24.45	26.41	30.24		
			84	17.7	18.91	19.98	21.85	25.56		
			64	12.4	13.17	14.30	16.07	19.48		
			50	9.8	10.48	11.72	13.53	16.90		
			25	5.5	6.05	7.41	9.11	12.55		
			20	4.9	5.42	6.72	8.57	11.89		
		All peripherals enabled ⁽²⁾⁽³⁾ , HSI, PLL ON, Flash ON	16	3.3	3.51	5.06	6.91	10.30		
			1	0.9	1.01	2.67	4.52	7.88		
		All peripherals disabled, External clock, PLL ON ⁽²⁾ , Flash deep power down	100	3.5	4.17	5.56	7.54	11.23		
			84	2.9	3.48	4.94	6.76	10.40		
			64	2.2	2.73	3.94	5.80	8.98		
			50	1.8	2.38	3.57	5.42	8.60		
			25	1.3	1.86	3.11	4.82	8.12		
			20	1.3	1.90	3.13	4.85	8.15		
		All peripherals disabled, HSI, PLL OFF ⁽²⁾ , Flash deep power down	16	0.6	0.68	2.33	4.16	7.47		
			1	0.5	0.59	2.24	4.07	7.38		
		All peripherals disabled, External clock, PLL ON ⁽²⁾ , Flash ON	100	4.0	4.54	5.97	8.09	11.74		
			84	3.3	3.87	5.32	7.19	10.84		
			64	2.5	3.04	4.33	6.15	9.47		
			50	2.2	2.69	3.93	5.82	9.04		
			25	1.6	2.13	3.37	5.20	8.46		
			20	1.6	2.16	3.39	5.22	8.48		
		All peripherals disabled, HSI, PLL OFF ⁽²⁾ , Flash ON	16	0.9	0.96	2.62	4.47	7.82		
			1	0.7	0.85	2.50	4.36	7.71		

1. Guaranteed by characterization results.

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

4. Tested in production.

Table 32. Typical and maximum current consumption in Sleep mode - $V_{DD} = 1.7\text{ V}$

Symbol	Parameter	Conditions	f _{HCLK} (MHz)	Typ	Max ⁽¹⁾					Unit
				T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD}	Supply current in Sleep mode	External clock, PLL ON, Flash deep power down, all peripherals enabled ⁽²⁾	100	21.2	22.64	23.56	25.66	29.30	mA	
			84	17.1	18.20	19.27	21.14	24.75		
			64	11.8	12.53	13.59	15.47	18.66		
			50	9.3	9.88	11.06	12.94	16.11		
			25	5.0	5.52	6.83	8.61	11.88		
			20	4.4	4.93	6.16	8.03	11.19		
		HSI, PLL OFF ⁽²⁾ , Flash deep power down, all peripherals enabled	16	3.0	3.53	4.91	6.57	9.94		
			1	0.6	1.19	2.55	4.21	7.57		
		External clock, PLL ON ⁽²⁾ , all peripherals enabled, Flash ON	100	21.7	23.10	24.09	26.12	29.90		
			84	17.4	18.61	19.72	21.55	25.27		
			64	12.1	12.89	13.98	15.84	19.18		
			50	9.6	10.20	11.43	13.32	16.62		
			25	5.2	5.80	7.19	8.91	12.33		
			20	4.6	5.18	6.47	8.37	11.63		
		HSI, PLL OFF ⁽²⁾ , all peripherals enabled, Flash ON	16	3.2	3.79	5.17	6.88	10.32		
			1	0.9	1.43	2.80	4.50	7.92		
		All peripherals disabled, External clock, PLL ON ⁽²⁾ , Flash deep power down	100	3.3	3.82	5.34	7.25	10.97		
			84	2.7	3.22	4.70	6.54	10.13		
			64	1.9	2.48	3.70	5.55	8.71		
			50	1.6	2.13	3.35	5.15	8.35		
			25	1.0	1.61	2.90	4.57	7.91		
			20	1.1	1.66	2.93	4.59	7.93		
		All peripherals disabled, HSI, PLL OFF ⁽²⁾ , Flash deep power down	16	0.6	1.12	2.49	4.14	7.49		
			1	0.5	1.04	2.40	4.06	7.40		
		All peripherals disabled, External clock, PLL ON ⁽²⁾ , Flash ON	100	3.7	4.28	5.76	7.83	11.49		
			84	3.1	3.60	5.11	6.96	10.64		
			64	2.3	2.80	4.09	5.96	9.23		
			50	1.9	2.44	3.70	5.59	8.82		
			25	1.3	1.89	3.18	4.94	8.27		
			20	1.4	1.92	3.20	4.97	8.29		
		All peripherals disabled, HSI, PLL OFF ⁽²⁾ , Flash ON	16	0.8	1.38	2.75	4.44	7.87		
			1	0.7	1.25	2.65	4.34	7.77		

1. Guaranteed by characterization results.

2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).

Table 33. Typical and maximum current consumptions in Stop mode - $V_{DD} = 1.7\text{ V}$

Symbol	Conditions	Parameter	Typ ⁽¹⁾	Max ⁽¹⁾					Unit
			T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	111.7	157.9	713.7	1323.5	2315.1	μA	
		Low power regulator usage	42.3	80.1	594.1	1167.6	2097.6		
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	77.9	113.1	568.3	1073.6	1883.7		
		Low power regulator usage	19.7	55.8	561.3	1123.2	2026.0		
		Low power low voltage regulator usage	15.3	46.3	490.8	991.3	1793.9		

1. Guaranteed by characterization results.

Table 34. Typical and maximum current consumption in Stop mode - $V_{DD}=3.6\text{ V}$

Symbol	Conditions	Parameter	Typ	Max ⁽¹⁾					Unit
			T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD_STOP}	Flash in Stop mode, all oscillators OFF, no independent watchdog	Main regulator usage	114.4	161.6 ⁽²⁾	723.0	1339.0	2342.7 ⁽²⁾	µA	
		Low power regulator usage	44.1	82.5 ⁽²⁾	600.6	1179.3	2119.1		
	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	Main regulator usage	80.6	116.7	572.3	1079.2	1896.3		
		Low power regulator usage	21.4	58.9	567.9	1134.5	2049.6		
		Low power low voltage regulator usage	17.0	49.0 ⁽²⁾	497.4	1003.6	1817.0 ⁽²⁾		

1. Guaranteed by characterization results.
2. Tested in production.

Table 35. Typical and maximum current consumption in Standby mode - $V_{DD}= 1.7\text{ V}$

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽²⁾					Unit
			T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	2.3	3.7	15.9	32.5	76.8	µA	
		Low-speed oscillator (LSE in high drive mode) and RTC ON	2.9	4.3	16.5	33.1	77.4		
		RTC and LSE OFF	1.1	2.5	14.7	31.3	75.6		

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 μA .
2. Guaranteed by characterization results.

Table 36. Typical and maximum current consumption in Standby mode - $V_{DD} = 3.6\text{ V}$

Symbol	Parameter	Conditions	Typ ⁽¹⁾	Max ⁽²⁾					Unit
			T _A = 25 °C	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	T _A = 125 °C		
I _{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE in low drive mode) and RTC ON	3.7	5.2	20.6	40.5	82.7	μA	
		Low-speed oscillator (LSE in high drive mode) and RTC ON	4.5	6.0	21.4	41.3	83.5		
		RTC and LSE OFF	2.5	4.0	19.4	39.3	81.5 ⁽³⁾		

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 μA .

2. Guaranteed by characterization, not tested in production unless otherwise specified.

3. Tested in production.

Table 37. Typical and maximum current consumptions in V_{BAT} mode

Symbol	Parameter	Conditions ⁽¹⁾	Typ				Max ⁽²⁾			Unit
			T _A = 25 °C				T _A = 85 °C	T _A = 105 °C	T _A = 125 °C	
			V _{BAT} = 1.7 V	V _{BAT} = 2.4 V	V _{BAT} = 3.3 V	V _{BAT} = 3.6 V	V _{BAT} = 3.6 V			
I _{DD_VBAT}	Backup domain supply current	Low-speed oscillator (LSE in low-drive mode) and RTC ON	0.74	0.84	1.04	1.24	3.00	5.00	10.00	µA
		Low-speed oscillator (LSE in high-drive mode) and RTC ON	1.51	1.64	1.89	2.00	3.80	5.80	11.60	
		RTC and LSE OFF	0.03	0.03	0.04	0.04	2.00	4.00	8.00	

1. Crystal used: Abracon ABS07-120-32.768 kHz-T with a C_L of 6 pF for typical values.

2. Guaranteed by characterization results.

Figure 24. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator “low power” mode selection)

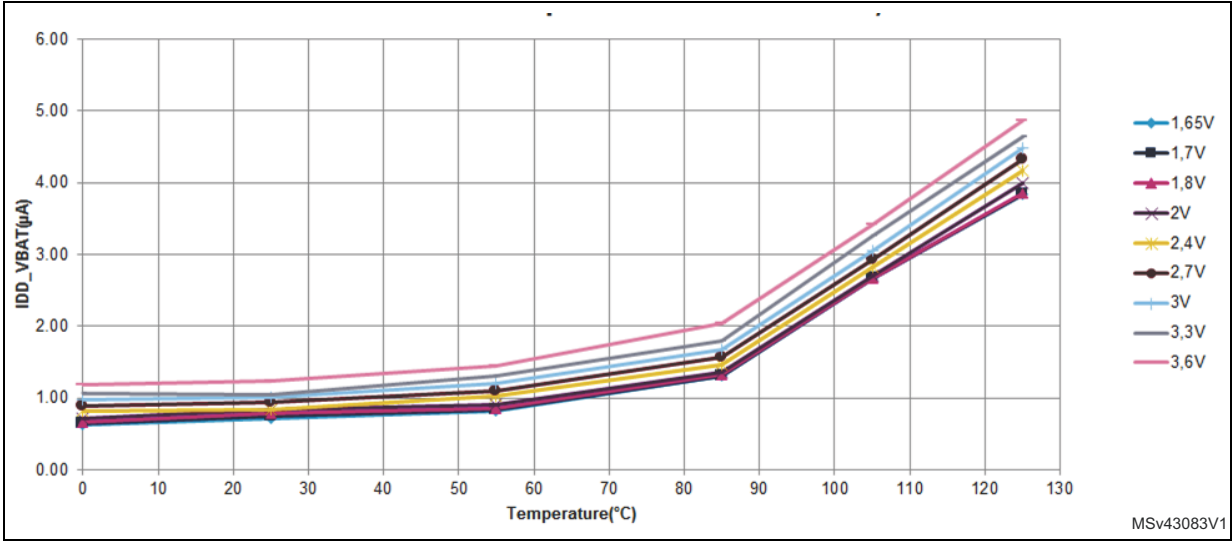
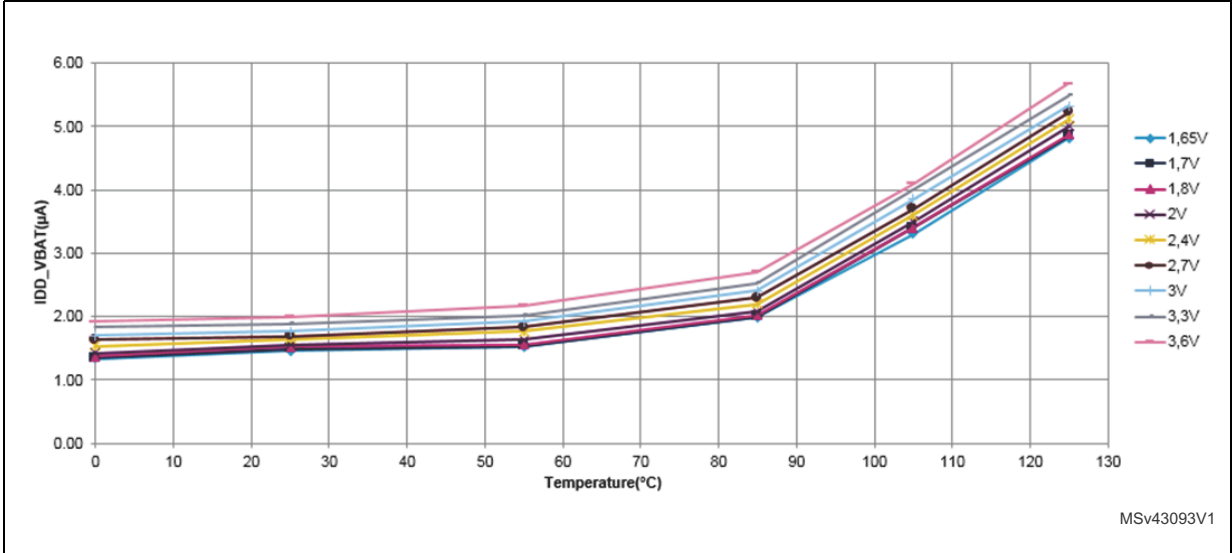


Figure 25. Typical V_{BAT} current consumption (LSE and RTC ON/LSE oscillator “high drive” mode selection)



I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 59: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see [Table 39: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 38. Switching output I/O current consumption

Symbol	Parameter	Conditions ⁽¹⁾	I/O toggling frequency (f _{sw})	Typ	Unit
IDDIO	I/O switching current	$V_{DD} = 3.3\text{ V}$ $C = C_{INT}$	2 MHz	0.05	mA
			8 MHz	0.15	
			25 MHz	0.45	
			50 MHz	0.85	
			60 MHz	1.00	
			84 MHz	1.40	
			90 MHz	1.67	
		$V_{DD} = 3.3\text{ V}$ $C_{EXT} = 0\text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.10	
			8 MHz	0.35	
			25 MHz	1.05	
			50 MHz	2.20	
			60 MHz	2.40	
			84 MHz	3.55	
			90 MHz	4.23	
		$V_{DD} = 3.3\text{ V}$ $C_{EXT} = 10\text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.20	
			8 MHz	0.65	
			25 MHz	1.85	
			50 MHz	2.45	
			60 MHz	4.70	
			84 MHz	8.80	
			90 MHz	10.47	
		$V_{DD} = 3.3\text{ V}$ $C_{EXT} = 22\text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.25	
			8 MHz	1.00	
			25 MHz	3.45	
			50 MHz	7.15	
			60 MHz	11.55	
		$V_{DD} = 3.3\text{ V}$ $C_{EXT} = 33\text{ pF}$ $C = C_{INT} + C_{EXT} + C_S$	2 MHz	0.32	
			8 MHz	1.27	
			25 MHz	3.88	
			50 MHz	12.34	

1. CS is the PCB board capacitance including the pad pin. CS = 7 pF (estimated value).

On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The ART accelerator is ON.
- Voltage Scale 2 mode selected, internal digital voltage V12 = 1.26 V.
- HCLK is the system clock at 100 MHz. $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
The given value is calculated by measuring the difference of current consumption
 - with all peripherals clocked off,
 - with only one peripheral clocked on,
 - scale 1 with $f_{HCLK} = 100$ MHz,
 - scale 2 with $f_{HCLK} = 84$ MHz,
 - scale 3 with $f_{HCLK} = 64$ MHz.
- Ambient operating temperature is 25 °C and $V_{DD}=3.3$ V.

Table 39. Peripheral current consumption

Peripheral		I _{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
AHB1	GPIOA	1.89	1.82	1.64	μA/MHz
	GPIOB	1.75	1.68	1.52	
	GPIOC	1.70	1.64	1.48	
	GPIOD	1.72	1.65	1.48	
	GPIOE	1.78	1.71	1.55	
	GPIOF	1.68	1.62	1.45	
	GPIOG	1.66	1.61	1.44	
	GPIOH	0.72	0.69	0.63	
	CRC	0.30	0.30	0.28	
	DMA1 ⁽¹⁾	1.75N + 3.14	1.66N + 3.00	1.49N + 2.70	
	DMA2 ⁽¹⁾	1.79N + 3.29	1.71N + 3.14	1.53N + 2.82	
AHB2	RNG	0.72	0.70	0.63	μA/MHz
	USB_OTG_FS	19.26	18.37	16.47	
AHB3	FSMC	5.42	5.18	4.64	μA/MHz
	QSPI	10.33	9.86	8.84	

Table 39. Peripheral current consumption (continued)

Peripheral		I _{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB1	AHB-APB1 bridge	0.90	0.88	0.81	μA/MHz
	TIM2	13.08	12.48	11.16	
	TIM3	9.98	9.50	8.50	
	TIM4	9.88	9.43	8.44	
	TIM5	13.14	12.52	11.19	
	TIM6	1.94	1.86	1.66	
	TIM7	1.86	1.79	1.56	
	TIM12	5.56	5.29	4.72	
	TIM13	3.44	3.29	2.94	
	TIM14	3.66	3.48	3.09	
	LPTIM1	7.34	7.00	6.25	
	WWDG	0.64	0.62	0.53	
	SPI2/I2S2	3.02	2.88	2.56	
	SPI3/I2S3	3.06	2.90	2.59	
	USART2	3.30	3.14	2.81	
	USART3	3.32	3.14	2.81	
	UART4	3.18	3.02	2.69	
	UART5	3.26	3.10	2.75	
	I2C1	3.20	3.05	2.72	
	I2C2	3.30	3.14	2.81	
	I2C3	3.26	3.10	2.78	
	I2CFMP1	5.22	4.98	4.44	
	CAN1	5.58	5.31	4.75	
	CAN2	5.14	4.88	4.38	
	CAN3	5.70	5.43	4.84	
	PWR	0.90	0.86	0.75	
	DAC1	2.14	2.05	1.81	
	UART7	3.08	2.93	2.59	
	UART8	3.10	2.95	2.63	

Table 39. Peripheral current consumption (continued)

Peripheral		I _{DD} (Typ)			Unit
		Scale 1	Scale 2	Scale 3	
APB2	AHB-APB2 bridge	0.10	0.11	0.09	μA/MHz
	TIM1	6.78	6.46	5.80	
	TIM8	6.94	6.62	5.94	
	USART1	3.14	3.00	2.69	
	USART6	3.12	2.98	2.67	
	UART9	2.89	1.98	1.75	
	UART10	2.91	2.00	1.77	
	ADC1	3.45	3.29	2.95	
	SDIO	3.54	3.37	3.03	
	SPI1	1.52	1.46	1.31	
	SPI4	1.50	1.43	1.28	
	SYSCFG	0.58	0.55	0.50	
	EXT1	0.91	0.86	0.78	
	TIM9	2.95	2.81	2.53	
	TIM10	1.88	1.79	1.61	
	TIM11	1.86	1.77	1.59	
	SPI5	1.50	1.43	1.30	
	SAI	2.89	2.75	2.47	
	DFSDM1	4.43	4.21	3.80	
	DFSDM2	7.08	6.76	6.05	
Bus Matrix		4.06	3.87	3.45	

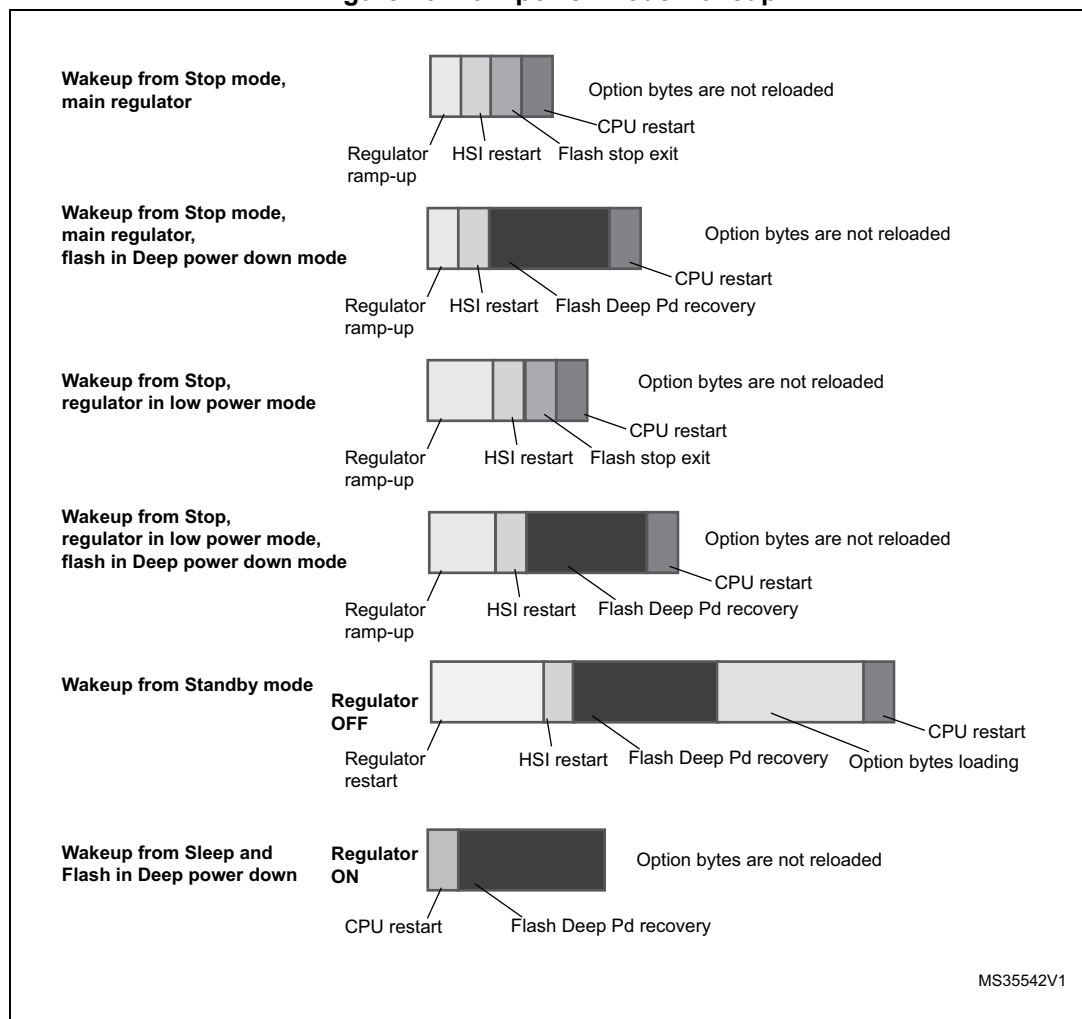
1. N is the number of stream enable (1...8).

6.3.7 Wakeup time from low-power modes

The wakeup times given in [Table 40](#) are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0/PC0/PC1) pins are used to wakeup from Standby, Stop and Sleep modes.

Figure 26. Low-power mode wakeup



All timings are derived from tests performed under ambient temperature and $V_{DD}=3.3$ V.

Table 40. Low-power mode wakeup timings⁽¹⁾

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ ⁽¹⁾	Max ⁽¹⁾	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	-	4	6	clk cycles
$t_{WUSLEEPFDSM}$		Flash memory in Deep power down mode	-	-	50.0	μs
t_{WUSTOP}	Wakeup from STOP mode Code execution on Flash	Main regulator	-	12.7	15.0	
		Main regulator, Flash memory in Deep power down mode	-	104.1	120.0	
		Wakeup from Stop mode, regulator in low power mode ⁽²⁾	-	20.9	28.0	
		Regulator in low power mode, Flash memory in Deep power down mode ⁽²⁾	-	112.5	130.0	
		Regulator in low power mode low voltage, Flash memory in Deep power down mode	-	112.5	130.0	
t_{WUSTOP}	Wakeup from STOP mode code execution on RAM ⁽³⁾	Main regulator with Flash in Stop mode or Deep power down ⁽²⁾	-	4.2	7.0	
		Wakeup from Stop mode, regulator in low power mode and Flash in Stop mode or Deep power down	-	12.6	20.0	
$t_{WUSTDBY}$	Wakeup from Standby mode	-	-	328.2	400.0	
$t_{WUFLASH}$	Wakeup of Flash	From Flash_Stop mode	-	-	11.0	
		From Flash Deep power down mode	-	-	40.0	

1. Guaranteed by characterization results.

2. The specification is valid for wakeup from regulator in low power mode or low power low voltage mode, since the timing difference is negligible.

3. For the faster wakeup time for code execution on RAM, the Flash must be in STOP or DeepPower Down mode (see reference manual RM0430).

6.3.8 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 59](#). However, the recommended clock input waveform is shown in [Figure 27](#).

The characteristics given in [Table 41](#) result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions

summarized in [Table 17](#).

Table 41. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	External user clock source frequency ⁽¹⁾		1	-	50	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{f(HSE)}$	OSC_IN high or low time ⁽¹⁾		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time ⁽¹⁾		-	-	10	
$C_{in(HSE)}$	OSC_IN input capacitance ⁽¹⁾		-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle		45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the [Table 59](#). However, the recommended clock input waveform is shown in [Figure 28](#).

The characteristics given in [Table 42](#) result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in [Table 17](#).

Table 42. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency ⁽¹⁾		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time ⁽¹⁾		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time ⁽¹⁾		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance ⁽¹⁾		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA

1. Guaranteed by design.

Figure 27. High-speed external clock source AC timing diagram

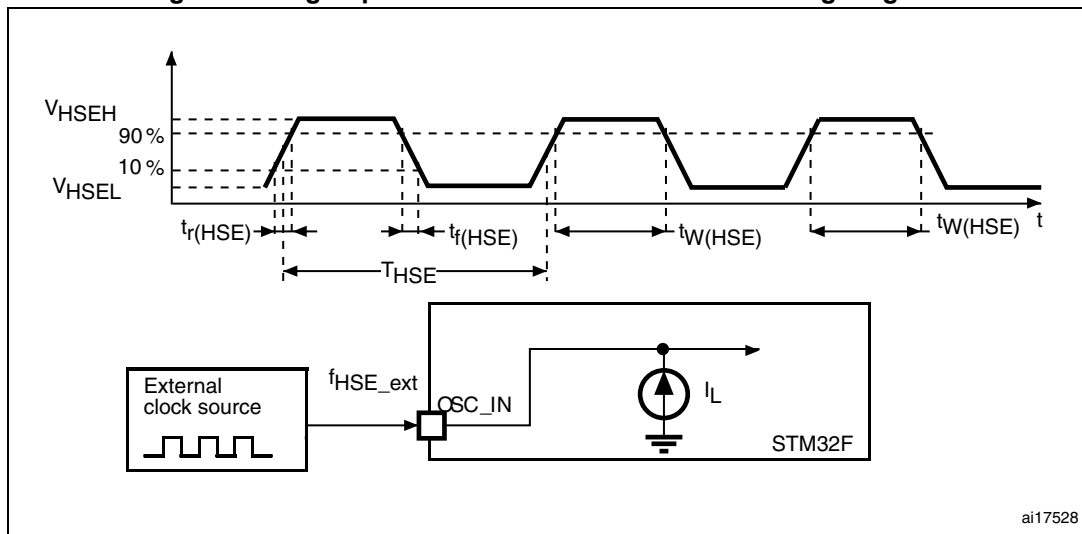
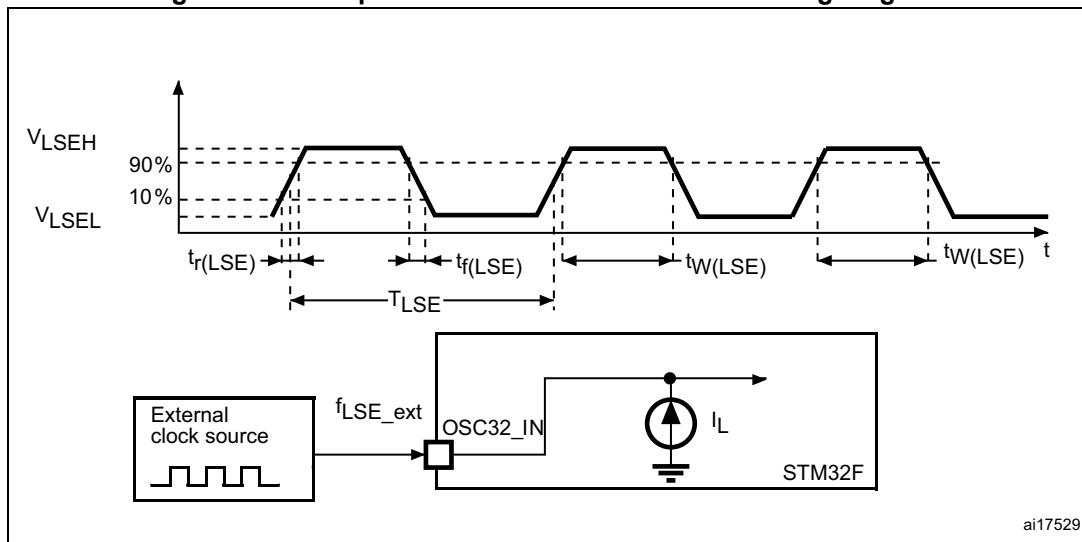


Figure 28. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 43](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 43. HSE 4-26 MHz oscillator characteristics⁽¹⁾

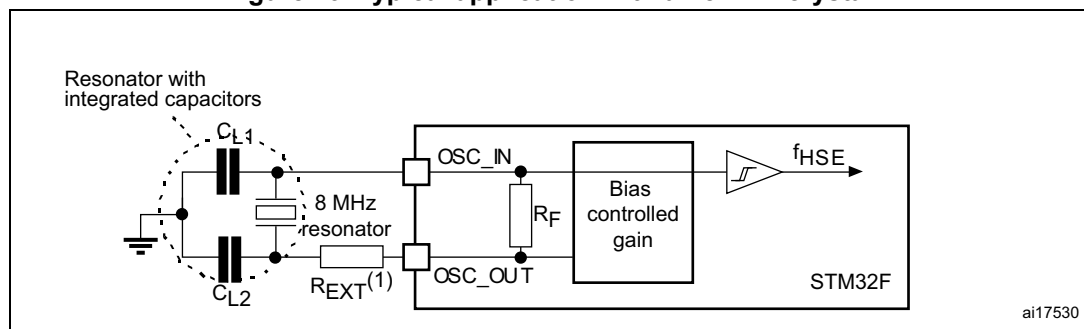
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	-	26	MHz
R_F	Feedback resistor		-	200	-	k Ω
I_{DD}	HSE current consumption	$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=5\text{ pF @25 MHz}$	-	450	-	μA
		$V_{DD}=3.3\text{ V}$, ESR= 30 Ω , $C_L=10\text{ pF @25 MHz}$	-	530	-	
$ACC_{HSE}^{(2)}$	HSE accuracy	-	-500	-	500	ppm
$G_{m_crit_max}$	Maximum critical crystal g_m	Startup	-	-	1	mA/V
$t_{SU(HSE)}^{(3)}$	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. This parameter depends on the crystal used in the application. The minimum and maximum values must be respected to comply with USB standard specifications.
3. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 29](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 29. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 44](#). In the application, the resonator and the load capacitors have to be placed as close as

possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

The LSE high-power mode allows to cover a wider range of possible crystals but with a cost of higher power consumption.

Table 44. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz) ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor	-	-	18.4	-	M Ω
I_{DD}	LSE current consumption	Low-power mode (default)	-	-	1	μ A
		High-drive mode	-	-	3	
$ACC_{LSE}^{(2)}$	LSE accuracy	-	-500	-	500	ppm
$G_{m_crit_max}$	Maximum critical crystal g_m	Startup, low-power mode	-	-	0.56	μ A/V
		Startup, high-drive mode	-	-	1.50	
$t_{SU(LSE)}^{(3)}$	startup time	V_{DD} is stabilized	-	2	-	s

1. Guaranteed by design.

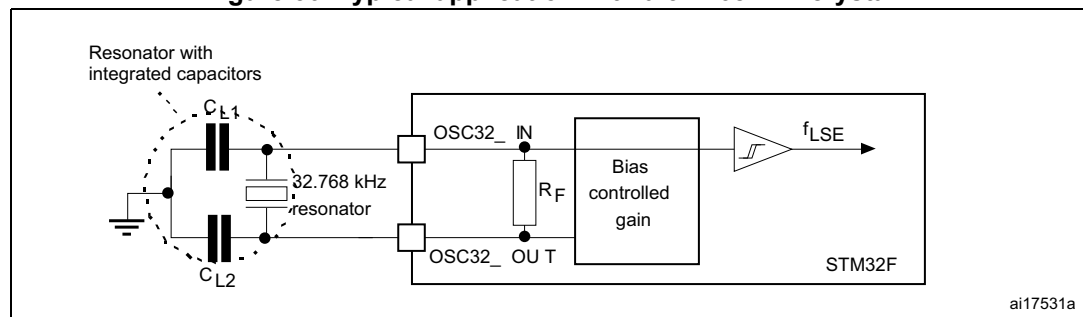
2. This parameter depends on the crystal used in the application. Refer to the application note AN2867.

3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is guaranteed by characterization and not tested in production. It is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

For information about the LSE high-power mode, refer to the reference manual RM0383.

Figure 30. Typical application with a 32.768 kHz crystal



6.3.9 Internal clock source characteristics

The parameters given in [Table 45](#) and [Table 46](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

High-speed internal (HSI) RC oscillator

Table 45. HSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	16	-	MHz
ACC_{HSI}	HSI user trimming step ⁽²⁾	-	-	-	1	%
	Accuracy of the HSI oscillator	$T_A = -40$ to 125 °C ⁽³⁾	-8	-	6.75	%
		$T_A = -40$ to 105 °C ⁽³⁾	-8	-	4.5	%
		$T_A = -10$ to 85 °C ⁽³⁾	-4	-	4	%
		$T_A = 25$ °C ⁽⁴⁾	-1	-	1	%
$t_{su(HSI)}$ ⁽²⁾	HSI oscillator startup time	-	-	2.2	4	μs
$I_{DD(HSI)}$ ⁽²⁾	HSI oscillator power consumption	-	-	60	80	μA

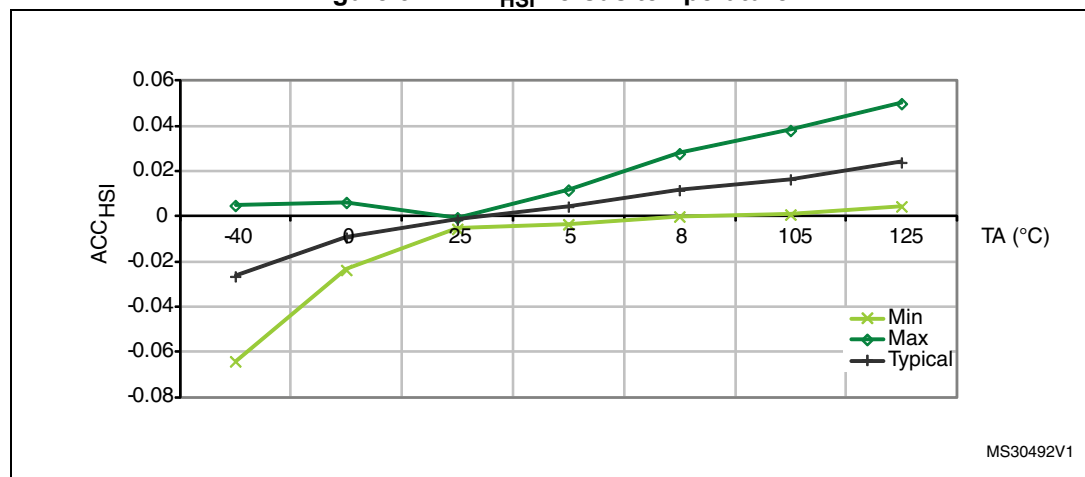
1. $V_{DD} = 3.3$ V, $T_A = -40$ to 125 °C unless otherwise specified.

2. Guaranteed by design

3. Based on characterization

4. Factory calibrated, parts not soldered.

Figure 31. ACC_{HSI} versus temperature



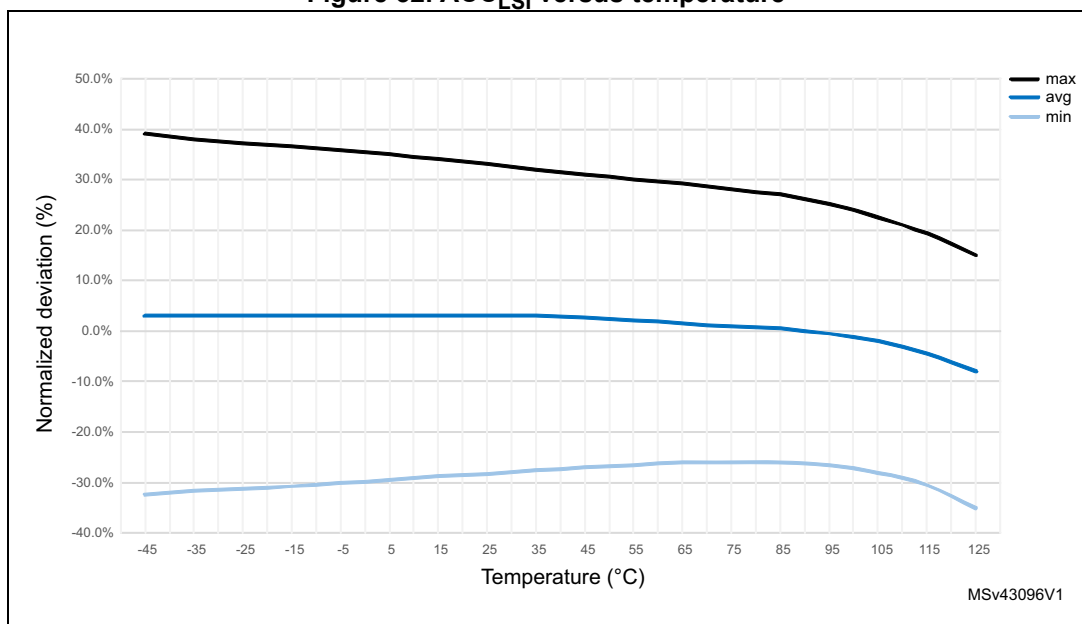
1. Guaranteed by characterization results.

Low-speed internal (LSI) RC oscillator

Table 46. LSI oscillator characteristics ⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
$f_{\text{LSI}}^{(2)}$	Frequency	16.1	32.0	47.0	kHz
$t_{\text{su(LSI)}}^{(3)}$	LSI oscillator startup time	-	15.0	40.0	μs
$I_{\text{DD(LSI)}}^{(3)}$	LSI oscillator power consumption	-	0.4	0.6	μA

- $V_{\text{DD}} = 3 \text{ V}$, $T_{\text{A}} = -40$ to $125 \text{ }^{\circ}\text{C}$ unless otherwise specified.
- Guaranteed by characterization results.
- Guaranteed by design.

Figure 32. ACC_{LSI} versus temperature

6.3.10 PLL characteristics

The parameters given in [Table 47](#) and [Table 48](#) are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 47. Main PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock ⁽¹⁾	-	0.95 ⁽²⁾	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock	-	24	-	100	
f_{PLLQ_OUT}	48 MHz PLLQ multiplier output clock	-	-	48	75	
f_{PLLR_OUT}	PLLR multiplier output clock for I2S and SAI	-	-	-	216	
f_{VCO_OUT}	PLL VCO output	-	100	-	432	
t_{LOCK}	PLL lock time	VCO freq = 100 MHz	75	-	200	μs
		VCO freq = 432 MHz	100	-	300	
Jitter ⁽³⁾	Cycle-to-cycle jitter	System clock 100 MHz	RMS	-	25	ps
			peak to peak	-	± 150	
	Period Jitter		RMS	-	15	
			peak to peak	-	± 200	
	Bit Time CAN jitter	Cycle to cycle at 1 MHz on 1000 samples.	-	330	-	
$I_{DD(PLL)}^{(4)}$	PLL power consumption on VDD	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLL)}^{(4)}$	PLL power consumption on VDDA	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to obtain the specified PLL input clock values. The M factor is shared between PLL and PLLI2S.
2. Guaranteed by design.
3. The use of two PLLs in parallel could degraded the Jitter up to +30%.
4. Guaranteed by characterization results.

Table 48. PLLI2S (audio PLL) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock ⁽¹⁾	-	0.95 ⁽²⁾	1	2.10	MHz
$f_{PLLI2SQ_OUT}$	48 MHz PLLI2SQ multiplier output clock	-	-	48	75	
$f_{PLLI2SR_OUT}$	PLLI2SR multiplier output clock for I2S and SAI	-	-	-	216	
f_{VCO_OUT}	PLLI2S VCO output	-	100	-	432	
t_{LOCK}	PLLI2S lock time	VCO freq = 100 MHz	75	-	200	μs
		VCO freq = 432 MHz	100	-	300	
Jitter ⁽³⁾	Master I2S clock jitter	Cycle to cycle at 12.288 MHz on 48 kHz period, N=432, R=5	RMS	-	90	-
			peak to peak	-	± 280	-
		Average frequency of 12.288 MHz N = 432, R = 5 on 1000 samples	-	90	-	ps
	WS I2S clock jitter	Cycle to cycle at 48 KHz on 1000 samples	-	400	-	
$I_{DD(PLLI2S)}^{(4)}$	PLLI2S power consumption on V_{DD}	VCO freq = 100 MHz VCO freq = 432 MHz	0.15 0.45	-	0.40 0.75	mA
$I_{DDA(PLLI2S)}^{(4)}$	PLLI2S power consumption on V_{DDA}	VCO freq = 100 MHz VCO freq = 432 MHz	0.30 0.55	-	0.40 0.85	

1. Take care of using the appropriate division factor M to have the specified PLL input clock values.

2. Guaranteed by design.

3. Value given with main PLL running.

4. Guaranteed by characterization results.

6.3.11 PLL spread spectrum clock generation (SSCG) characteristics

The spread spectrum clock generation (SSCG) feature allows to reduce electromagnetic interferences (see [Table 55: EMI characteristics for LQFP144](#)). It is available only on the main PLL.

Table 49. SSCG parameter constraints

Symbol	Parameter	Min	Typ	Max ⁽¹⁾	Unit
f_{Mod}	Modulation frequency	-	-	10	kHz
md	Peak modulation depth	0.25	-	2	%
MODEPER * INCSTEP	(Modulation period) * (Increment Step)	-	-	$2^{15}-1$	-

1. Guaranteed by design.

Equation 1

The frequency modulation period (MODEPER) is given by the equation below:

$$MODEPER = \text{round}[f_{PLL_IN} / (4 \times f_{Mod})]$$

f_{PLL_IN} and f_{Mod} must be expressed in Hz.

As an example:

If $f_{PLL_IN} = 1$ MHz, and $f_{MOD} = 1$ kHz, the modulation depth (MODEPER) is given by equation 1:

$$MODEPER = \text{round}[10^6 / (4 \times 10^3)] = 250$$

Equation 2

Equation 2 allows to calculate the increment step (INCSTEP):

$$INCSTEP = \text{round}[(2^{15} - 1) \times md \times PLLN] / (100 \times 5 \times MODEPER)$$

f_{VCO_OUT} must be expressed in MHz.

With a modulation depth (md) = $\pm 2\%$ (4 % peak to peak), and PLLN = 240 (in MHz):

$$INCSTEP = \text{round}[(2^{15} - 1) \times 2 \times 240] / (100 \times 5 \times 250) = 126md(\text{quantitized})\%$$

An amplitude quantization error may be generated because the linear modulation profile is obtained by taking the quantized values (rounded to the nearest integer) of MODPER and INCSTEP. As a result, the achieved modulation depth is quantized. The percentage quantized modulation depth is given by the following formula:

$$md_{\text{quantized}}\% = (MODEPER \times INCSTEP \times 100 \times 5) / ((2^{15} - 1) \times PLLN)$$

As a result:

$$md_{\text{quantized}}\% = (250 \times 126 \times 100 \times 5) / ((2^{15} - 1) \times 240) = 2.002\%(\text{peak})$$

Figure 33 and Figure 34 show the main PLL output clock waveforms in center spread and down spread modes, where:

- F0 is f_{PLL_OUT} nominal.
- T_{mode} is the modulation period.
- md is the modulation depth.

Figure 33. PLL output clock waveforms in center spread mode

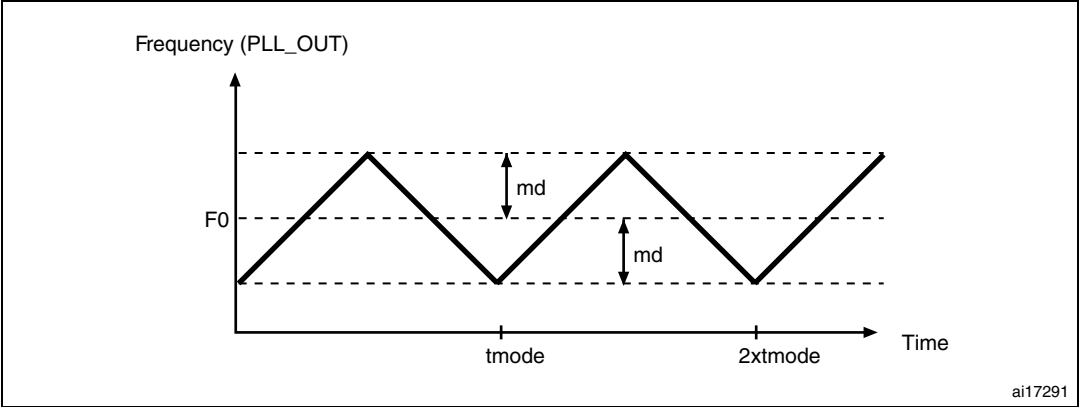
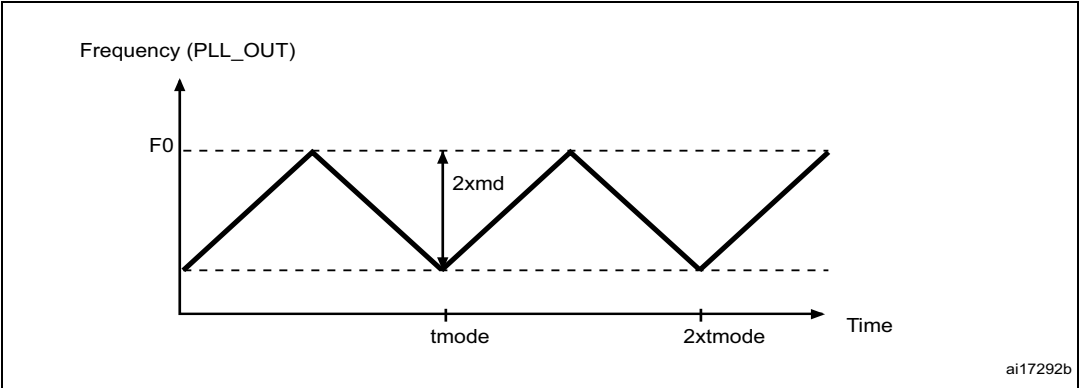


Figure 34. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to $125\text{ }^{\circ}\text{C}$ unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 50. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, $V_{DD} = 1.7\text{ V}$	-	5	-	mA
		Write / Erase 16-bit mode, $V_{DD} = 2.1\text{ V}$	-	8	-	
		Write / Erase 32-bit mode, $V_{DD} = 3.3\text{ V}$	-	12	-	

Table 51. Flash memory programming

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t_{prog}	Word programming time	Program/erase parallelism (PSIZE) = x 8/16/32	-	16	100 ⁽²⁾	μs
$t_{\text{ERASE16KB}}$	Sector (16 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	400	800	ms
		Program/erase parallelism (PSIZE) = x 16	-	300	600	
		Program/erase parallelism (PSIZE) = x 32	-	250	500	
$t_{\text{ERASE64KB}}$	Sector (64 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	1200	2400	ms
		Program/erase parallelism (PSIZE) = x 16	-	700	1400	
		Program/erase parallelism (PSIZE) = x 32	-	550	1100	
$t_{\text{ERASE128KB}}$	Sector (128 KB) erase time	Program/erase parallelism (PSIZE) = x 8	-	2	4	s
		Program/erase parallelism (PSIZE) = x 16	-	1.3	2.6	
		Program/erase parallelism (PSIZE) = x 32	-	1	2	
t_{ME}	Mass erase time	Program/erase parallelism (PSIZE) = x 8	-	24	48	s
		Program/erase parallelism (PSIZE) = x 16	-	15	30	
		Program/erase parallelism (PSIZE) = x 32	-	11	22	
V_{prog}	Programming voltage	32-bit program operation	2.7	-	3.6	V
		16-bit program operation	2.1	-	3.6	V
		8-bit program operation	1.7	-	3.6	V

1. Guaranteed by characterization results.

2. The maximum programming time is measured after 100K erase operations.

Table 52. Flash memory programming with V_{PP} voltage

Symbol	Parameter	Conditions	Min ⁽¹⁾	Typ	Max ⁽¹⁾	Unit
t_{prog}	Double word programming	$T_A = 0 \text{ to } +40 \text{ }^\circ\text{C}$ $V_{DD} = 3.3 \text{ V}$ $V_{PP} = 8.5 \text{ V}$	-	16	100 ⁽²⁾	μs
$t_{ERASE16KB}$	Sector (16 KB) erase time		-	230	-	ms
$t_{ERASE64KB}$	Sector (64 KB) erase time		-	490	-	
$t_{ERASE128KB}$	Sector (128 KB) erase time		-	875	-	
t_{ME}	Mass erase time		-	9.8	-	s
V_{prog}	Programming voltage	-	2.7	-	3.6	V
V_{PP}	V_{PP} voltage range	-	7	-	9	V
I_{PP}	Minimum current sunk on the V_{PP} pin	-	10	-	-	mA
$t_{VPP}^{(3)}$	Cumulative time during which V_{PP} is applied	-	-	-	1	hour

1. Guaranteed by design.
2. The maximum programming time is measured after 100K erase operations.
3. V_{PP} should only be connected during programming/erasing.

Table 53. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min ⁽¹⁾	
N_{END}	Endurance	$T_A = -40 \text{ to } +85 \text{ }^\circ\text{C}$ (temp. range 6) $T_A = -40 \text{ to } +105 \text{ }^\circ\text{C}$ (temp. range 7) $T_A = -40 \text{ to } +125 \text{ }^\circ\text{C}$ (temp. range 3)	10	kcycles
t_{RET}	Data retention	1 kcycle ⁽²⁾ at $T_A = 85 \text{ }^\circ\text{C}$	30	Years
		1 kcycle ⁽²⁾ at $T_A = 105 \text{ }^\circ\text{C}$	10	
		1 kcycle ⁽²⁾ at $T_A = 125 \text{ }^\circ\text{C}$	3	
		10 kcycle ⁽²⁾ at $T_A = 55 \text{ }^\circ\text{C}$	20	

1. Guaranteed by characterization results.
2. Cycling performed over the whole temperature range.

6.3.13 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 55](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 54. EMS characteristics for LQFP144 package

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, LQFP144 $T_A = +25\text{ }^{\circ}\text{C}$, $f_{HCLK} = 100\text{ MHz}$, conforms to IEC 61000-4-2	1B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	$V_{DD} = 3.3\text{ V}$, LQFP144 $T_A = +25\text{ }^{\circ}\text{C}$, $f_{HCLK} = 100\text{ MHz}$, conforms to IEC 61000-4-4	3B

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP144 packages and PDR_ON on WLCSP81.

As a consequence, it is recommended to add a serial resistor (1 k Ω maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with IEC61967-2 standard which specifies the test board and the pin loading.

Table 55. EMI characteristics for LQFP144

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. $[f_{HSE}/f_{CPU}]$	Unit
				8/100 MHz	
S_{EMI}	Peak level	$V_{DD} = 3.6\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, LQFP144 package, conforming to IEC 61967-2, EEMBC, ART ON, all peripheral clocks enabled, clock dithering disabled.	0.1 to 30 MHz	13	dB μ V
			30 to 130 MHz	21	
			130 MHz to 1 GHz	25	
			1 GHz to 2 GHz	19	
			EMI Level	4	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts $\times$ (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 56. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value ⁽¹⁾	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25\text{ °C}$ conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25\text{ °C}$ conforming to ANSI/ESD STM5.3.1, UFBGA144, UFBGA100, LQFP144, LQFP100, WLCSP81, LQFP64	3	250	
		$T_A = +25\text{ °C}$ conforming to ANSI/ESD STM5.3.1, UFQFPN48	4	500	

1. Guaranteed by characterization results.

Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latchup standard.

Table 57. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +125\text{ °C}$ conforming to JESD78A	II level A

6.3.15 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$ range), or other functional failure (for example reset, oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

The test results are given in [Table 58](#).

Table 58. I/O current injection susceptibility⁽¹⁾

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on BOOT0, PDR_ON, BYPASS_REG	- 0	0	mA
	Injected current on NRST	- 0	NA	
	Injected current on PE6, PC13, PC14, PC15, PF0, PF1, PF2, PC0, PC1, PC2, PC3	- 0	NA	
	Injected current on any other FT and FTf pins	- 5	NA	
	Injected current on any other pins	- 5	+ 5	

1. NA = not applicable.

Note: *It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.*

6.3.16 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 59](#) are derived from tests performed under the conditions summarized in [Table 17](#). All I/Os are CMOS and TTL compliant.

Table 59. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IL}	FT, TTa, TC and NRST I/O input low level voltage	1.7 V≤V _{DD} ≤3.6 V	-	-	0.3V _{DD} ⁽¹⁾	V
	BOOT0 I/O input low level voltage	1.75 V≤V _{DD} ≤3.6 V, -40 °C≤T _A ≤125 °C	-	-	0.1V _{DD} +0.1 ⁽²⁾	
		1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤125 °C	-	-		
V _{IH}	FT, TTa, TC and NRST I/O input high level voltage ⁽⁶⁾	1.7 V≤V _{DD} ≤3.6 V	0.7V _{DD} ⁽¹⁾	-	-	V
	BOOT0 I/O input high level voltage	1.75 V≤V _{DD} ≤3.6 V, -40 °C≤T _A ≤125 °C	0.17V _{DD} +0.7 ⁽²⁾	-	-	
		1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤125 °C				
V _{HYS} ⁽³⁾	FT, TTa, TC and NRST I/O input hysteresis	1.7 V≤V _{DD} ≤3.6 V	10% V _{DD} ⁽²⁾⁽⁴⁾	-	-	V
	BOOT0 I/O input hysteresis	1.75 V≤V _{DD} ≤3.6 V, -40 °C≤T _A ≤125 °C	0.1	-	-	
		1.7 V≤V _{DD} ≤3.6 V, 0 °C≤T _A ≤125 °C				

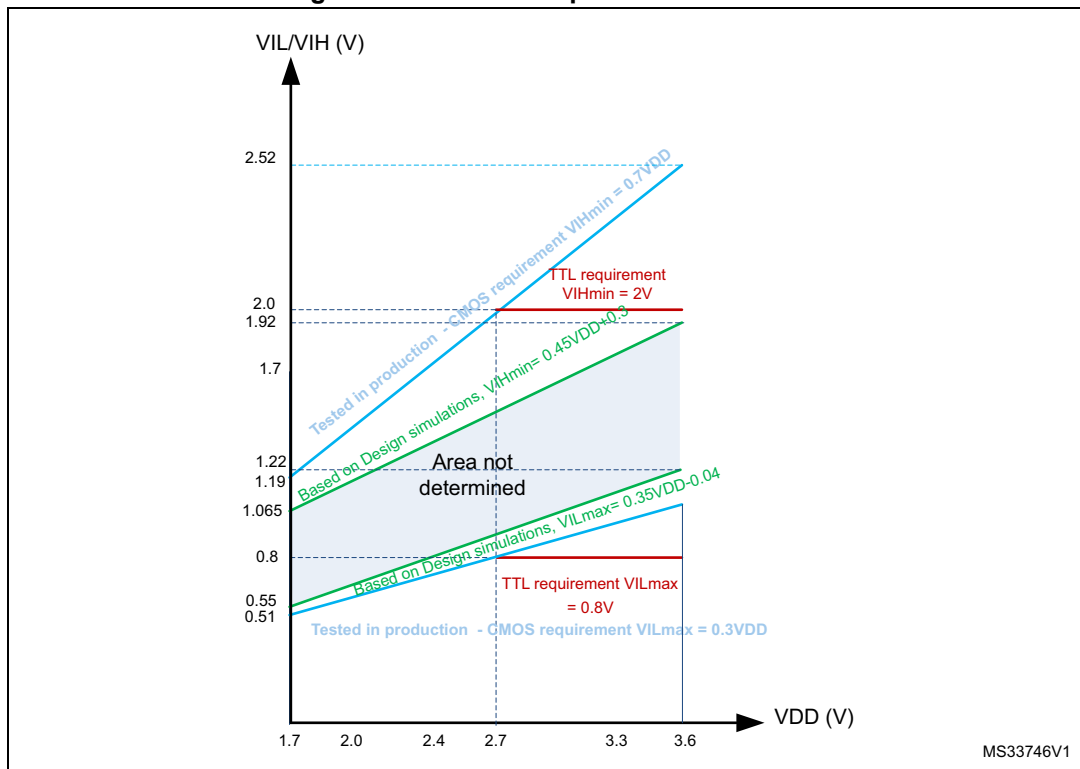
Table 59. I/O static characteristics (continued)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
I_{lkg}	I/O input leakage current ⁽⁵⁾		$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	± 1	μA
	I/O FT/TC input leakage current ⁽⁶⁾		$V_{IN} = 5 V$	-	-	3	
R_{PU}	Weak pull-up equivalent resistor ⁽⁷⁾	All pins except for PA10 (OTG_FS_ID)	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
		PA10 (OTG_FS_ID)	-	7	10	14	
R_{PD}	Weak pull-down equivalent resistor ⁽⁸⁾	All pins except for PA10 (OTG_FS_ID)	$V_{IN} = V_{DD}$	30	40	50	
		PA10 (OTG_FS_ID)	-	7	10	14	
C_{IO}	I/O pin capacitance		-	-	5	-	pF

1. Guaranteed by test in production.
2. Guaranteed by design.
3. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results.
4. With a minimum of 200 mV.
5. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 58: I/O current injection susceptibility](#)
6. To sustain a voltage higher than $V_{DD} + 0.3 V$, the internal pull-up/pull-down resistors must be disabled. Leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 58: I/O current injection susceptibility](#)
7. Pull-up resistors are designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimum (~10% order).
8. Pull-down resistors are designed with a true resistance in series with a switchable NMOS. This NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT and TC I/Os is shown in [Figure 35](#).

Figure 35. FT/TC I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#). In particular:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 15](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 15](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 60](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#). All I/Os are CMOS and TTL compliant.

Table 60. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$1.3^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-1.3^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(5)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4^{(5)}$	-	
$V_{OLFM}^{(1)}$	Output low level voltage for an FTf I/O pin in FM+ mode	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OLFM}^{(1)}$	Output low level voltage for an FTf I/O pin in FM+ mode	$I_{IO} = +10 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 15](#), and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 15](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Guaranteed by characterization results.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 36](#) and [Table 61](#), respectively.

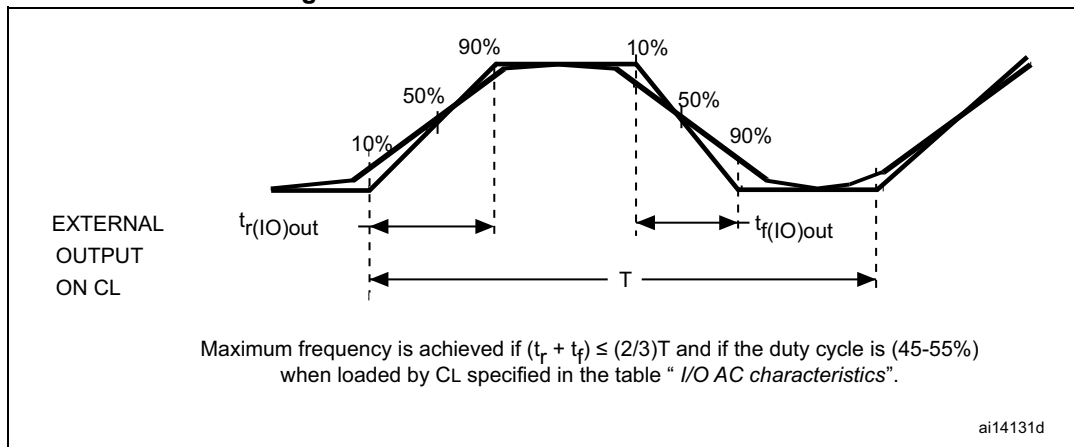
Unless otherwise specified, the parameters given in [Table 61](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 61. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	4	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} = 1.7 \text{ V to } 3.6 \text{ V}$	-	-	100	ns
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	25	MHz
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	12.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	50	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	20	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}, V_{DD} \geq 2.7 \text{ V}$	-	-	10	ns
			$C_L = 50 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	20	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	6	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10	
10	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 40 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	50 ⁽⁴⁾	MHz
			$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	25	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	100 ⁽⁴⁾	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	50 ⁽⁴⁾	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 40 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	6	ns
			$C_L = 40 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	10	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	4	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	6	
11	$F_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	100 ⁽⁴⁾	MHz
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	50 ⁽⁴⁾	
	$t_{f(\text{IO})\text{out}}/$ $t_{r(\text{IO})\text{out}}$	Output high to low level fall time and output low to high level rise time	$C_L = 30 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	4	ns
			$C_L = 30 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	6	
			$C_L = 10 \text{ pF}, V_{DD} \geq 2.70 \text{ V}$	-	-	2.5	
			$C_L = 10 \text{ pF}, V_{DD} \geq 1.7 \text{ V}$	-	-	4	
FM+	Fmax	Maximum frequency	$C_L = 50 \text{ pF}, 1.6 \leq V_{DD} \leq 3.6 \text{ V}$	-	-	1	MHz
	Tf	Output high to low level fall time		-	-	5	ns
-	$t_{\text{EXTI}pw}$	Pulse width of external signals detected by the EXTI controller	-	10	-	-	ns

1. Guaranteed by characterization results.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in [Figure 36](#).
4. For maximum frequencies above 50 MHz and $V_{DD} > 2.4$ V, the compensation cell should be used.

Figure 36. I/O AC characteristics definition



6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 59](#)).

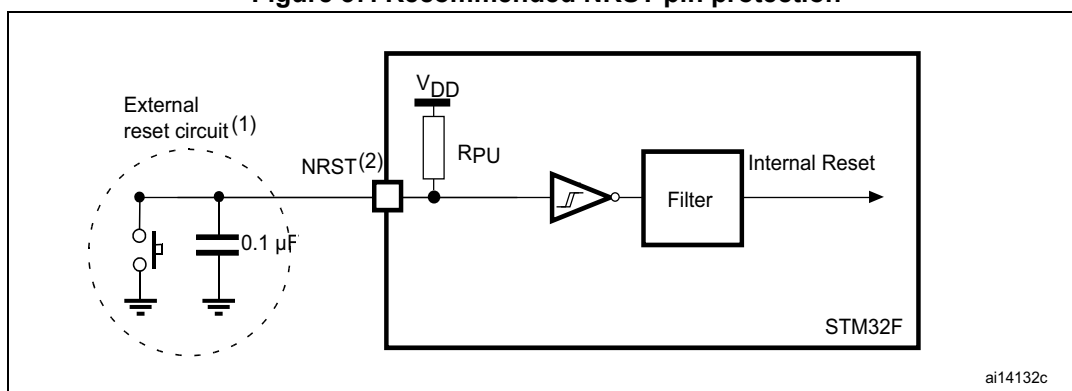
Unless otherwise specified, the parameters given in [Table 62](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#). Refer to [Table 59: I/O static characteristics](#) for the values of V_{IH} and V_{IL} for NRST pin.

Table 62. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor ⁽¹⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}^{(2)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(2)}$	NRST Input not filtered pulse	$V_{DD} > 2.7$ V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	μ s

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Figure 37. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 62](#). Otherwise the reset is not taken into account by the device.

6.3.18 TIM timer characteristics

The parameters given in [Table 63](#) are guaranteed by design.

Refer to [Section 6.3.16: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 63. TIMx characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions ⁽³⁾	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK} = 100\text{ MHz}$	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APBx prescaler>4, $f_{TIMxCLK} = 100\text{ MHz}$	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK} = 100\text{ MHz}$	0	$f_{TIMxCLK}/2$	MHz
			0	50	MHz
Res_{TIM}			-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	$f_{TIMxCLK} = 100\text{ MHz}$	0.0119	780	μs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 100\text{ MHz}$	-	51.1	S

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 is 50 MHz and on APB2 is up to 100 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then $TIMxCLK = HCLK$, otherwise $TIMxCLK \geq 4 \times PCLKx$.

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

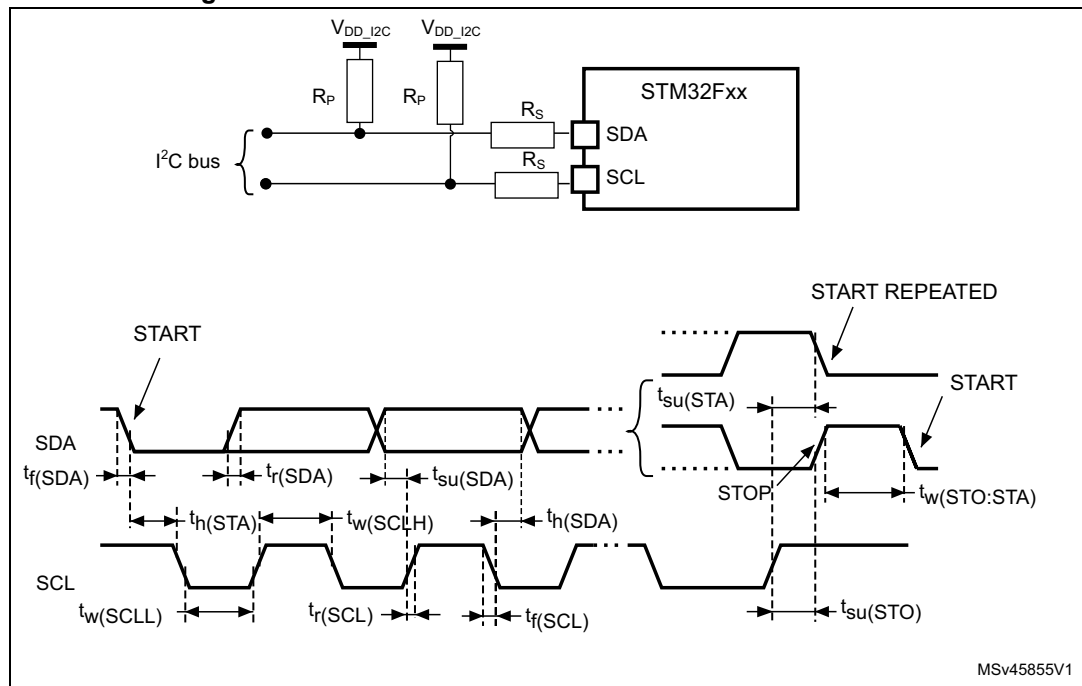
The I²C characteristics are described in [Table 64](#). Refer also to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, contact your local ST sales representative.

Table 64. I²C characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾⁽²⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
t _{w(SCLL)}	SCL clock low time	4.70	-	1.30	-	μs
t _{w(SCLH)}	SCL clock high time	4.0	-	0.60	-	
t _{su(SDA)}	SDA setup time	0.25	-	0.10	-	
t _{h(SDA)}	SDA data hold time	0	-	0	-	
t _{v(SDA,ACK)}	SDA data hold time	-	3.45 ⁽³⁾	-	0.90 ⁽⁴⁾	
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time	-	0.100	-	0.30	
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time	-	0.30	-	0.30	
t _{h(STA)}	Start condition hold time	4	-	0.6	-	
t _{su(STA)}	Repeated Start condition setup time	4.7	-	0.6	-	
t _{su(STO)}	Stop condition setup time	4	-	0.60	-	
t _{w(STO:STA)}	Stop to Start condition time (bus free)	4.70	-	1.3	-	
t _{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	-	-	0.05	0.10 ⁽⁵⁾	
C _b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
4. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
5. The minimum width of the spikes filtered by the analog filter is above t_{SP} (max)

Figure 38. I²C bus AC waveforms and measurement circuit

1. R_S = series protection resistor.
2. R_P = external pull-up resistor.
3. V_{DD_I2C} is the I²C bus power supply.

Table 65. SCL frequency ($f_{PCLK1} = 50$ MHz, $V_{DD} = V_{DD_I2C} = 3.3$ V)⁽¹⁾⁽²⁾

f_{SCL} (kHz)	I2C_CCR value
	$R_P = 4.7$ k Ω
400	0x8019
300	0x8021
200	0x8032
100	0x0096
50	0x012C
20	0x02EE

1. R_P = External pull-up resistance, f_{SCL} = I²C speed
2. For speeds around 200 kHz, the tolerance on the achieved speed is of $\pm 5\%$. For other speed ranges, the tolerance on the achieved speed is $\pm 2\%$. These variations depend on the accuracy of the external components used to design the application.

FMPI²C characteristics

The following table presents FMPI²C characteristics.

Refer also to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output function characteristics (SDA and SCL).

Table 66. FMPI²C characteristics⁽¹⁾

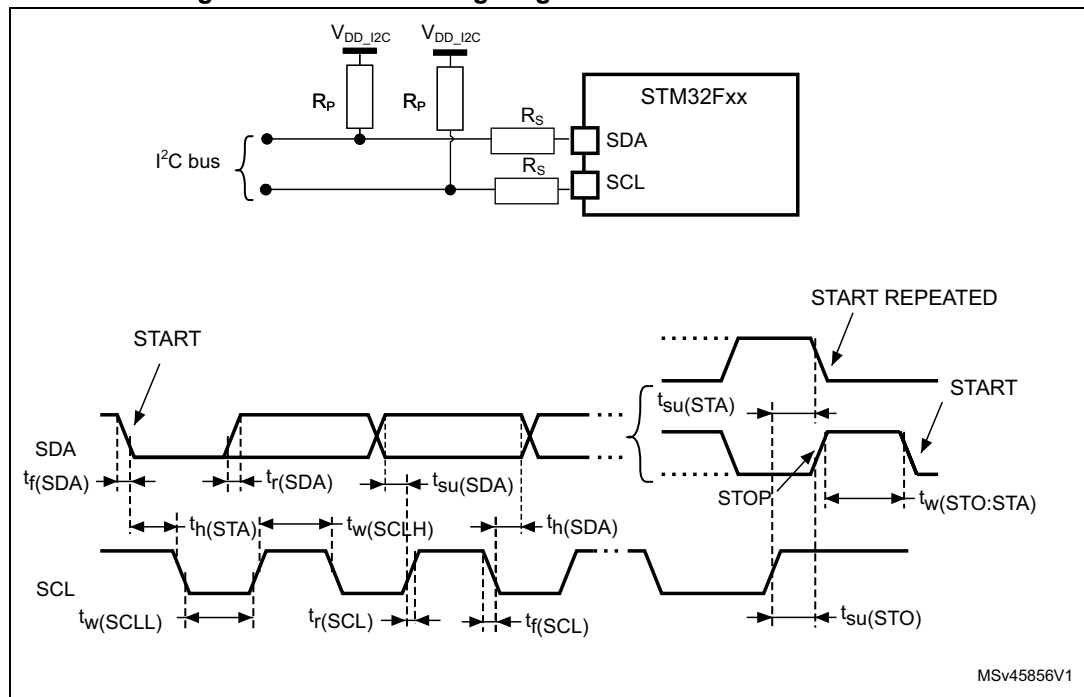
	Parameter	Standard mode		Fast mode		Fast+ mode		Unit
		Min	Max	Min	Max	Min	Max	
f _{FMPI2CC}	FMPI2CCCLK frequency	2	-	8	-	18	-	μs
t _w (SCLL)	SCL clock low time	4.7	-	1.3	-	0.5	-	
t _w (SCLH)	SCL clock high time	4.0	-	0.6	-	0.26	-	
t _{su} (SDA)	SDA setup time	0.25	-	0.10	-	0.05	-	
t _H (SDA)	SDA data hold time	0	-	0	-	0	-	
t _v (SDA,ACK)	Data, ACK valid time	-	3.45	-	0.9	-	0.45	
t _r (SDA) t _r (SCL)	SDA and SCL rise time	-	1.0	-	0.30	-	0.12	
t _f (SDA) t _f (SCL)	SDA and SCL fall time	-	0.30	-	0.30	-0	0.12	
t _H (STA)	Start condition hold time	4	-	0.6	-	0.26	-	
t _{su} (STA)	Repeated Start condition setup time	4.7	-	0.6	-	0.26	-	
t _{su} (STO)	Stop condition setup time	4	-	0.6	-	0.26	-	pF
t _w (STO:STA)	Stop to Start condition time (bus free)	4.7	-	1.3	-	0.5	-	
t _{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode	-	-	0.05	0.1	0.05	0.1	
C _b	Capacitive load for each bus Line	-	400	-	400	-	550 ⁽²⁾	pF

1. Based on characterization results.

2. Can be limited. Maximum supported value can be retrieved by referring to the following formulas:

$$t_{r(SDA/SCL)} = 0.8473 \times R_p \times C_{load}$$

$$R_{p(min)} = (V_{DD} - V_{OL(max)}) / I_{OL(max)}$$

Figure 39. FMPI²C timing diagram and measurement circuit

SPI interface characteristics

Unless otherwise specified, the parameters given in [Table 67](#) for the SPI interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30\text{ pF}$
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 67. SPI dynamic characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode, SPI1,4,5 $3.0\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	50	MHz
		Master mode, SPI1,4,5 $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	42	
		Master mode SPI1,4,5 $1.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	25	
		Master transmitter mode SPI1,4,5 $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	50	
		Slave receiver mode SPI1,4,5 $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	50	
		Slave mode transmitter/full duplex SPI1,4,5 $2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	40 ⁽²⁾	
		Slave mode transmitter/full duplex SPI1,4,5 $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	26	
		Master & Slave mode, SPI2/3 $1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	-	25	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI presc = 2	$4 \cdot T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI presc = 2	$2 \cdot T_{PCLK}$	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	$T_{PCLK} - 2$	T_{PCLK}	$T_{PCLK} + 2$	ns
$t_{su(MI)}$	Data input setup time	Master mode	2.5	-	-	ns
$t_{su(SI)}$		Slave mode	4.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	5	-	-	ns
$t_{h(SI)}$		Slave mode	2	-	-	

Table 67. SPI dynamic characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{a(SO)}$	Data output access time	Slave mode	7	-	21	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	12	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge), 2.7 V < V_{DD} < 3.6 V	-	7	12.5	ns
		Slave mode (after enable edge), 1.71 V < V_{DD} < 3.6 V	-	7	19	
$t_{v(MO)}$		Master mode	-	2	3	
$t_{h(SO)}$	Data output hold time	Slave mode 1.71 V < V_{DD} < 3.6 V	6	-	-	ns
$t_{h(MO)}$		Master mode	1.5	-	-	

1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)} = 0$ while Duty(SCK) = 50%

Figure 40. SPI timing diagram - slave mode and CPHA = 0

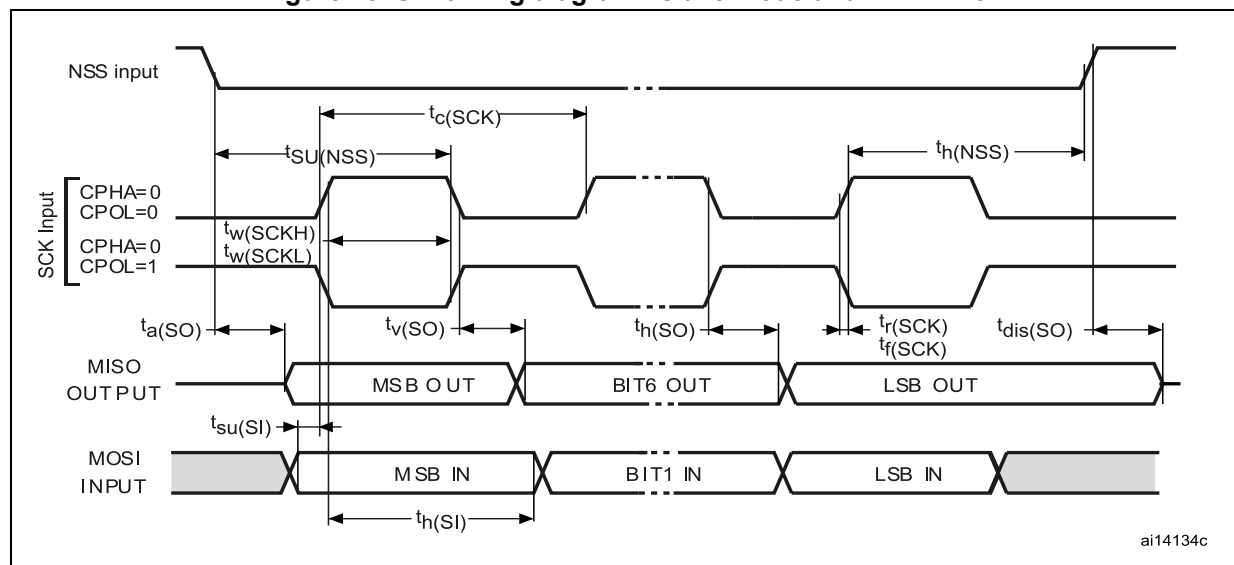


Figure 41. SPI timing diagram - slave mode and CPHA = 1

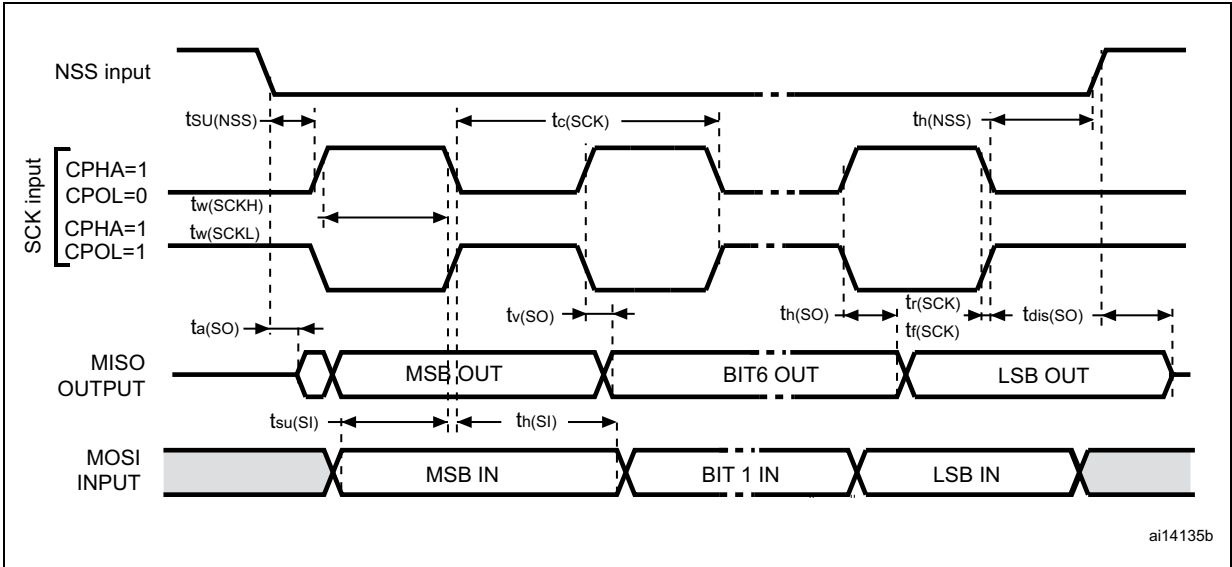
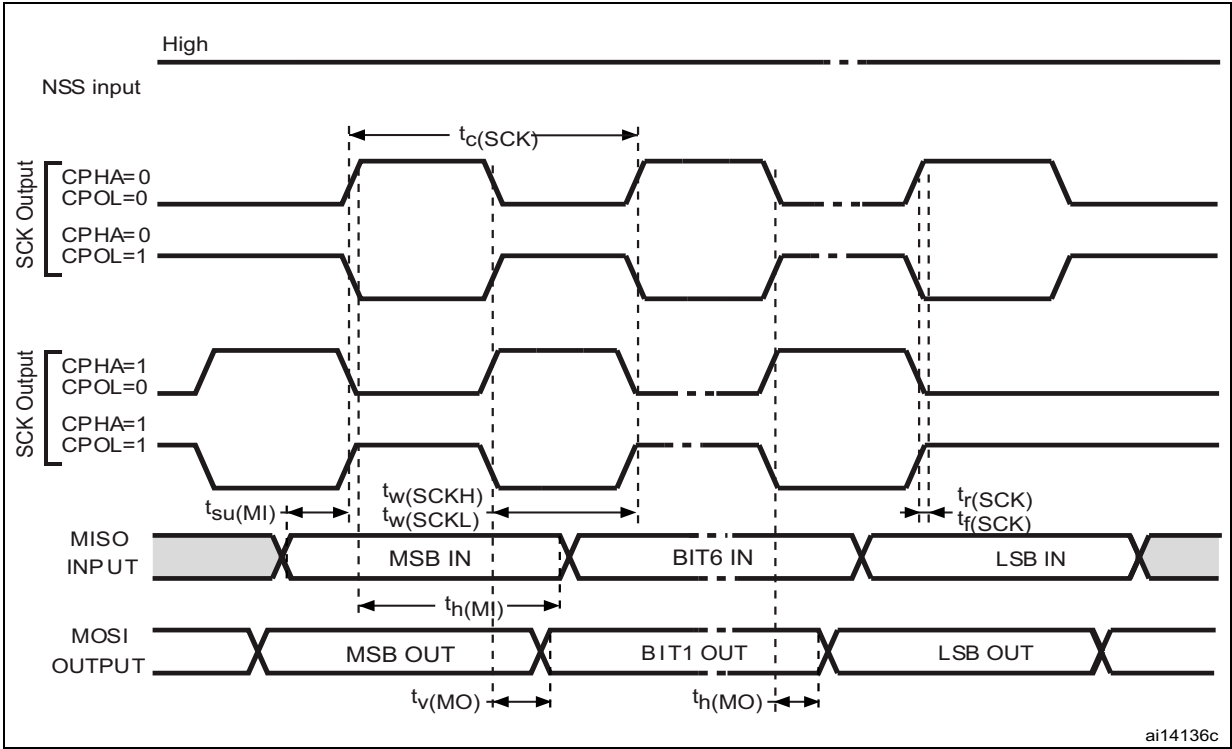


Figure 42. SPI timing diagram - master mode



I²S interface characteristics

Unless otherwise specified, the parameters given in [Table 68](#) for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 68. I²S dynamic characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256 * 8K	256 * $F_S^{(2)}$	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64 * F_S	MHz
		Slave data: 32 bits	-	64 * F_S	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	-	3.5	ns
$t_{h(WS)}$	WS hold time	Master mode	1.5	-	
$t_{su(WS)}$	WS setup time	Slave mode	2.5	-	
$t_{h(WS)}$	WS hold time	Slave mode	0.5	-	
$t_{su(SD_MR)}$	Data input setup time	Master receiver	3	-	
$t_{su(SD_SR)}$		Slave receiver	2.5	-	
$t_{h(SD_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD_SR)}$		Slave receiver	1.5	-	
$t_{v(SD_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	15	
$t_{v(SD_MT)}$		Master transmitter (after enable edge)	-	6	
$t_{h(SD_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3.5	-	
$t_{h(SD_MT)}$		Master transmitter (after enable edge)	1.5	-	

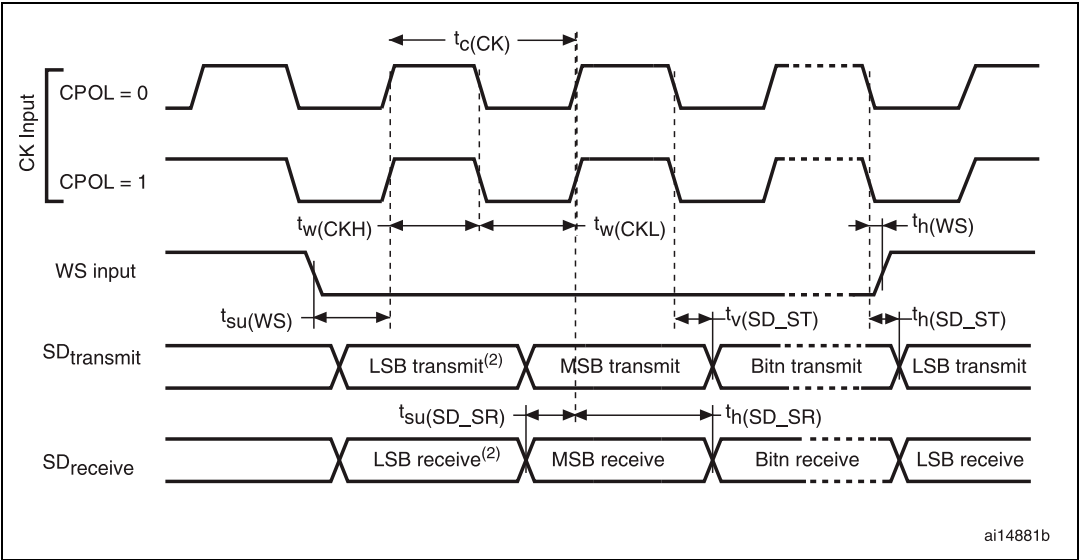
1. Guaranteed by characterization results.

2. The maximum value of 256x F_S is 50 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of RM0430 reference manual for more details on the sampling frequency (F_S).

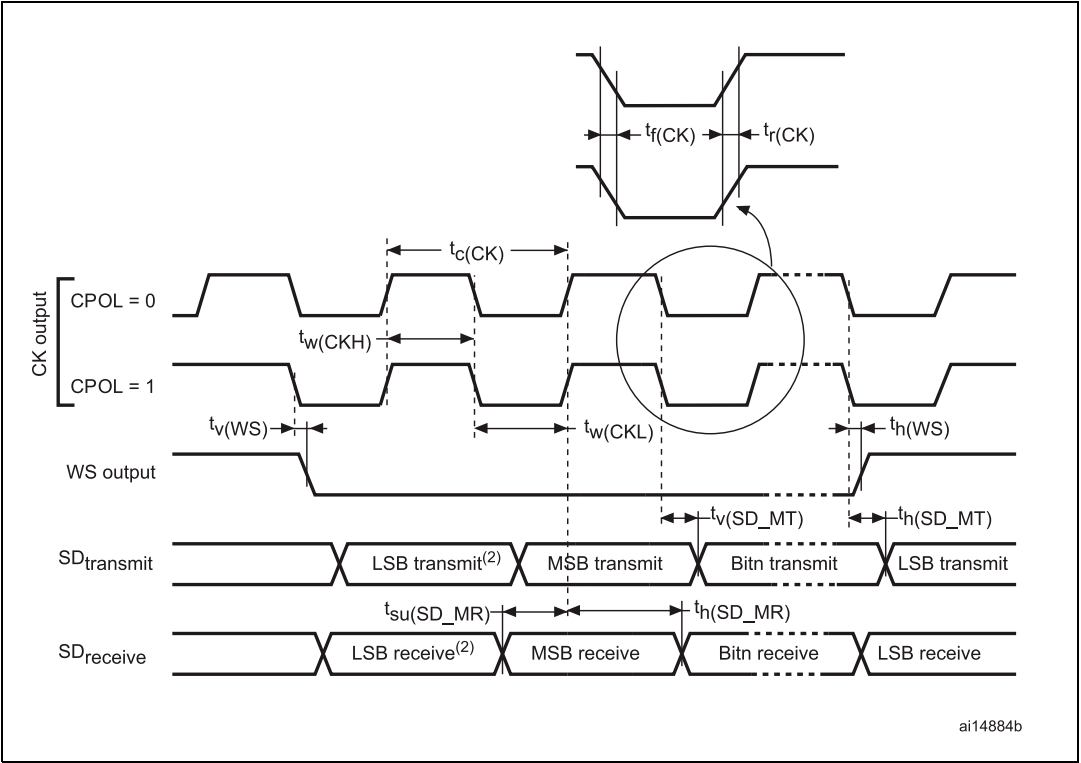
f_{MCK} , f_{CK} , and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of $(I2SDIV/(2*I2SDIV+ODD))$ and a maximum value of $(I2SDIV+ODD)/(2*I2SDIV+ODD)$. F_S maximum value is supported for each mode/condition.

Figure 43. I²S slave timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 44. I²S master timing diagram (Philips protocol)



1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

SAI characteristics

Unless otherwise specified, the parameters given in [Table 69](#) for SAI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and VDD supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C=30 pF
- Measurement points are performed at CMOS levels: 0.5V_{DD}

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SCK,SD,WS).

Table 69. SAI characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCKL}	SAI Main clock output	-	256 * 8K	256 * F _s ⁽²⁾	MHz
F_{SCK}	SAI clock frequency	Master data: 32 bits	-	128 * F _s	MHz
		Slave data: 32 bits	-	128 * F _s	
$t_{v(FS)}$	FS valid time	Master mode 2.7 V ≤ V _{DD} ≤ 3.6 V	-	19	ns
		Master mode 1.71 V ≤ V _{DD} ≤ 3.6 V	-	28	
$t_{h(FS)}$	FS hold time	Master mode	13	-	
		Slave mode	0	-	
$t_{su(FS)}$	FS setup time	Slave mode	3	-	
$t_{su(SD_A_MR)}$	Data input setup time	Master receiver	0.5	-	
$t_{su(SD_B_SR)}$		Slave receiver	1.5	-	
$t_{h(SD_A_MR)}$	Data input hold time	Master receiver	5	-	
$t_{h(SD_B_SR)}$		Slave receiver	2.5	-	
$t_{v(SD_B_ST)}$	Data output valid time	Slave transmitter (after enable edge) 2.7 V ≤ V _{DD} ≤ 3.6 V	-	15	
		Slave transmitter (after enable edge) 1.71 V ≤ V _{DD} ≤ 3.6 V	-	28	
$t_{h(SD_B_ST)}$	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD_A_MT)}$	Data output valid time	Master transmitter (after enable edge) 2.7 V ≤ V _{DD} ≤ 3.6 V	-	15	
		Master transmitter (after enable edge) 1.71 V ≤ V _{DD} ≤ 3.6 V	-	29	
$t_{h(SD_A_MT)}$	Data output hold time	Master transmitter (after enable edge)	13	-	

1. Guaranteed by characterization results.

2. 256 * F_s maximum corresponds to 45 MHz (APB2 maximum frequency)

Figure 45. SAI master timing waveforms

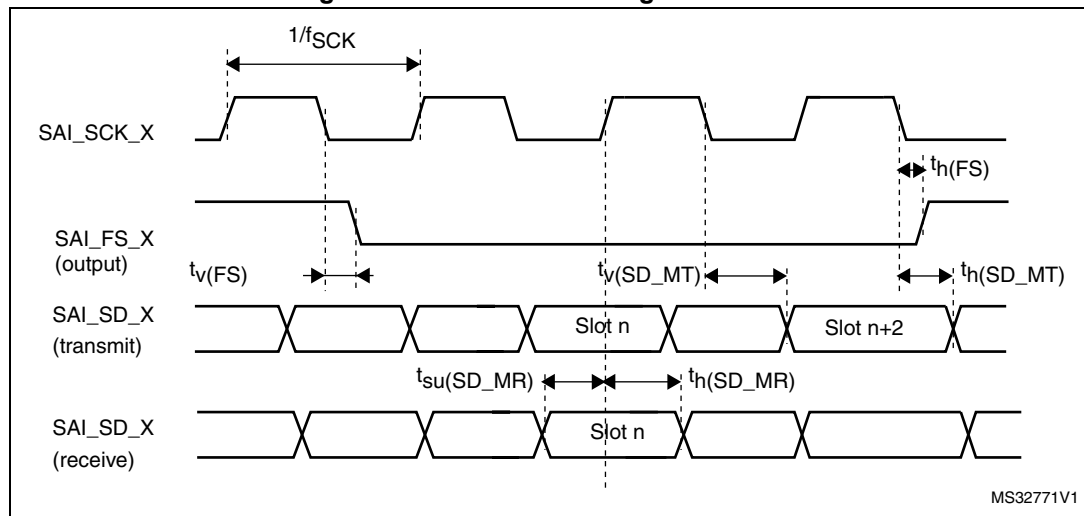
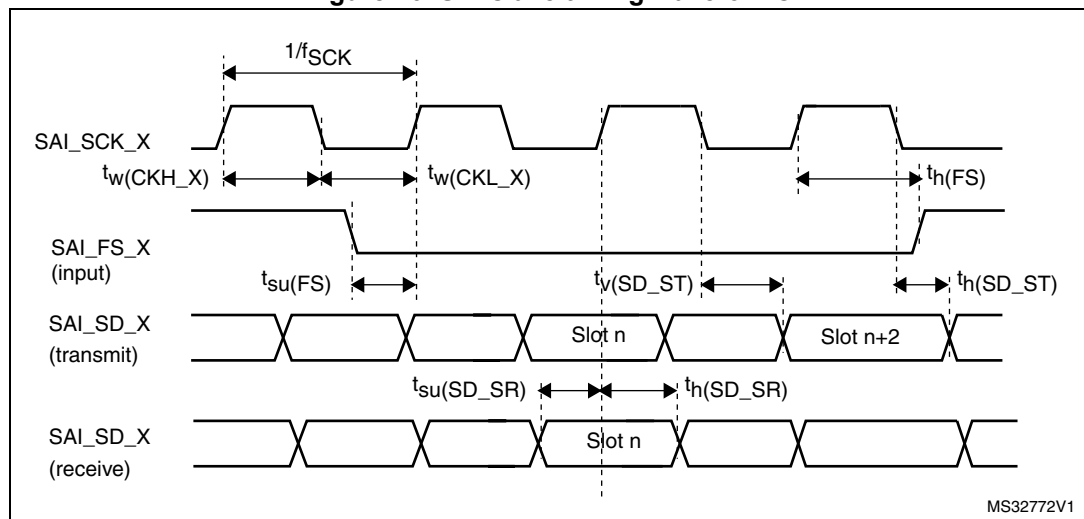


Figure 46. SAI slave timing waveforms



QSPI interface characteristics

Unless otherwise specified, the parameters given in the following tables for QSPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load $C = 20\text{pF}$
- Measurement points are done at CMOS levels: 0.5VDD

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics.

Table 70. QSPI dynamic characteristics in SDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{\text{c(SCK)}}$	QSPI clock frequency	$2.7\text{ V} < V_{\text{DD}} < 3.6\text{ V}$ $C_{\text{load}} = 20\text{ pF}$	-	-	100	MHz
		$1.71\text{ V} < V_{\text{DD}} < 3.6\text{ V}$ $C_{\text{load}} = 15\text{ pF}$	-	-	80	
$t_{\text{w(CKH)}}$	QSPI clock high and low	-	$t_{\text{(CK)}} / 2 - 1$	-	$t_{\text{(CK)}} / 2$	ns
$t_{\text{w(CKL)}}$			$t_{\text{(CK)}} / 2$	-	$t_{\text{(CK)}} / 2 + 1$	
$t_{\text{s(IN)}}$	Data input setup time	-	1.5	-	-	
$t_{\text{h(IN)}}$	Data input hold time	-	3	-	-	
$t_{\text{v(OUT)}}$	Data output valid time	$2.7\text{ V} < V_{\text{DD}} < 3.6\text{ V}$	-	0.5	1	
		$1.71\text{ V} < V_{\text{DD}} < 3.6\text{ V}$	-	0.5	3	
$t_{\text{h(OUT)}}$	Data output hold time	-	0	-	0	

1. Guaranteed by characterization results.

Table 71. QSPI dynamic characteristics in DDR mode⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{\text{c(SCK)}}$	QSPI clock frequency	$2.7\text{ V} < V_{\text{DD}} < 3.6\text{ V}$ $C_{\text{load}} = 20\text{ pF}$	-	-	80	MHz
		$1.71\text{ V} < V_{\text{DD}} < 3.6\text{ V}$ $C_{\text{load}} = 15\text{ pF}$	-	-	70	

Table 71. QSPI dynamic characteristics in DDR mode⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(CKH)}$	QSPI clock high and low time	-	$t_{(CK)} / 2 - 1$	-	$t_{(CK)} / 2$	ns
$t_{w(CKL)}$			$t_{(CK)} / 2$	-	$t_{(CK)} / 2 + 1$	
$t_{sr(IN)}$, $t_{sf(IN)}$	Data input setup time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	0.5	-	-	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	0.5	-	-	
$t_{hr(IN)}$, $t_{hf(IN)}$	Data input hold time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	2	-	-	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	2	-	-	
$t_{vr(OUT)}$, $t_{vf(OUT)}$	Data output valid time	$2.7\text{ V} < V_{DD} < 3.6\text{ V}$	-	8.5	9	
		$1.71\text{ V} < V_{DD} < 3.6\text{ V}$	-	8.5	11.5	
$t_{hr(OUT)}$, $t_{hf(OUT)}$	Data output hold time	-	7.5	-	-	

1. Guaranteed by characterization results.

USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

Table 72. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}^{(1)}$	USB OTG FS transceiver startup time	1	μs

1. Guaranteed by design.

Table 73. USB OTG FS DC electrical characteristics

Symbol	Parameter	Conditions	Min. ⁽¹⁾	Typ.	Max. ⁽¹⁾	Unit
Input levels	V_{DD}	USB OTG FS operating voltage	3.0 ⁽²⁾	-	3.6	V
	$V_{DI}^{(3)}$	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	V
	$V_{CM}^{(3)}$	Differential common mode range	Includes V_{DI} range	0.8	-	
	$V_{SE}^{(3)}$	Single ended receiver threshold		1.3	-	
Output levels	V_{OL}	Static output level low	R_L of 1.5 k Ω to 3.6 V ⁽⁴⁾	-	-	V
	V_{OH}	Static output level high	R_L of 15 k Ω to $V_{SS}^{(4)}$	2.8	-	
R_{PD}	PA11, PA12 (USB_FS_DM/DP)	$V_{IN} = V_{DD}$	17	21	24	k Ω
	PA9 (OTG_FS_VBUS)		0.65	1.1	2.0	
R_{PU}	PA11, PA12 (USB_FS_DM/DP)	$V_{IN} = V_{SS}$	1.5	1.8	2.1	
	PA9 (OTG_FS_VBUS)	$V_{IN} = V_{SS}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.

2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 μ A current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Figure 47. USB OTG FS timings: definition of data signal rise and fall time

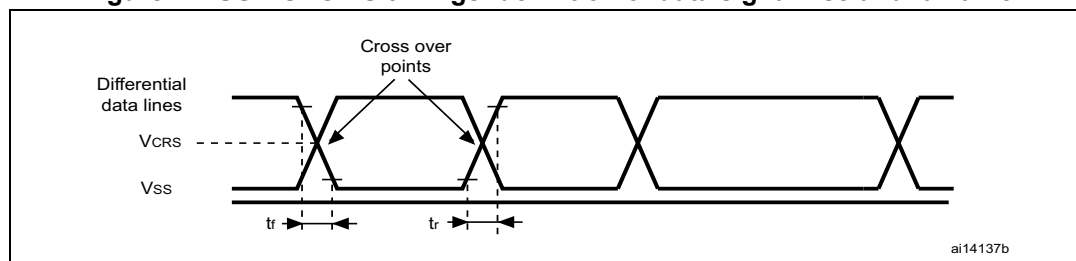


Table 74. USB OTG FS electrical characteristics⁽¹⁾

Driver characteristics					
Symbol	Parameter	Conditions	Min	Max	Unit
t_r	Rise time ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_f	Fall time ⁽²⁾	$C_L = 50$ pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, refer to USB Specification - Chapter 7 (version 2.0).

CAN (controller area network) interface

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CANx_TX and CANx_RX).

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 75](#) are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in [Table 17](#).

Table 75. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	$V_{DDA} - V_{REF+} < 1.2\text{ V}$	1.7 ⁽¹⁾	-	3.6	V
V_{REF+}	Positive reference voltage		1.7 ⁽¹⁾	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	$V_{DDA} = 1.7^{(1)}\text{ to }2.4\text{ V}$	0.6	15	18	MHz
		$V_{DDA} = 2.4\text{ to }3.6\text{ V}$	0.6	30	36	MHz
$f_{TRIG}^{(2)}$	External trigger frequency	$f_{ADC} = 30\text{ MHz}$, 12-bit resolution	-	-	1764	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range ⁽³⁾	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
$R_{AIN}^{(2)}$	External input impedance	See Equation 1 for details	-	-	50	k Ω
$R_{ADC}^{(2)(4)}$	Sampling switch resistance	-	-	-	6	k Ω
$C_{ADC}^{(2)}$	Internal sample and hold capacitor	-	-	4	7	pF
$t_{lat}^{(2)}$	Injection trigger conversion latency	$f_{ADC} = 30\text{ MHz}$	-	-	0.100	μs
		-	-	-	3 ⁽⁵⁾	$1/f_{ADC}$
$t_{latr}^{(2)}$	Regular trigger conversion latency	$f_{ADC} = 30\text{ MHz}$	-	-	0.067	μs
		-	-	-	2 ⁽⁵⁾	$1/f_{ADC}$
$t_S^{(2)}$	Sampling time	$f_{ADC} = 30\text{ MHz}$	0.100	-	16	μs
		-	3	-	480	$1/f_{ADC}$
$t_{STAB}^{(2)}$	Power-up time	-	-	2	3	μs
$t_{CONV}^{(2)}$	Total conversion time (including sampling time)	$f_{ADC} = 30\text{ MHz}$ 12-bit resolution	0.50	-	16.40	μs
		$f_{ADC} = 30\text{ MHz}$ 10-bit resolution	0.43	-	16.34	μs
		$f_{ADC} = 30\text{ MHz}$ 8-bit resolution	0.37	-	16.27	μs
		$f_{ADC} = 30\text{ MHz}$ 6-bit resolution	0.30	-	16.20	μs
		9 to 492 (t_S for sampling + n-bit resolution for successive approximation)				$1/f_{ADC}$

Table 75. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_S^{(2)}$	Sampling rate ($f_{ADC} = 30$ MHz, and $t_S = 3$ ADC cycles)	12-bit resolution Single ADC	-	-	2	Msp/s
$I_{VREF+}^{(2)}$	ADC V_{REF} DC current consumption in conversion mode	-	-	300	500	μA
$I_{VDDA}^{(2)}$	ADC V_{DDA} DC current consumption in conversion mode	-	-	1.6	1.8	mA

- V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).
- Guaranteed by characterization results.
- V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA} .
- R_{ADC} maximum value is given for $V_{DD}=1.7$ V, and minimum value for $V_{DD}=3.3$ V.
- For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in [Table 75](#).

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. $N = 12$ (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 76. ADC accuracy at $f_{ADC} = 18$ MHz⁽¹⁾

Symbol	Parameter	Test conditions	Typ	Max ⁽²⁾	Unit
ET	Total unadjusted error	$f_{ADC} = 18$ MHz $V_{DDA} = 1.7$ to 3.6 V $V_{REF} = 1.7$ to 3.6 V $V_{DDA} - V_{REF} < 1.2$ V	± 3	± 4	LSB
EO	Offset error		± 2	± 3	
EG	Gain error		± 1	± 3	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 2	± 3	

- Better performance could be achieved in restricted V_{DD} , frequency and temperature ranges.
- Guaranteed by characterization results.

Table 77. ADC accuracy at $f_{\text{ADC}} = 30 \text{ MHz}^{(1)}$

Symbol	Parameter	Test conditions	Typ	Max ⁽²⁾	Unit
ET	Total unadjusted error	$f_{\text{ADC}} = 30 \text{ MHz}$, $R_{\text{AIN}} < 10 \text{ k}\Omega$, $V_{\text{DDA}} = 2.4 \text{ to } 3.6 \text{ V}$, $V_{\text{REF}} = 1.7 \text{ to } 3.6 \text{ V}$, $V_{\text{DDA}} - V_{\text{REF}} < 1.2 \text{ V}$	± 2	± 5	LSB
EO	Offset error		± 1.5	± 2.5	
EG	Gain error		± 1.5	± 4	
ED	Differential linearity error		± 1	± 2	
EL	Integral linearity error		± 1.5	± 3	

1. Better performance could be achieved in restricted V_{DD} , frequency and temperature ranges.
2. Guaranteed by characterization results.

Table 78. ADC accuracy at $f_{\text{ADC}} = 36 \text{ MHz}^{(1)}$

Symbol	Parameter	Test conditions	Typ	Max ⁽²⁾	Unit
ET	Total unadjusted error	$f_{\text{ADC}} = 36 \text{ MHz}$, $V_{\text{DDA}} = 2.4 \text{ to } 3.6 \text{ V}$, $V_{\text{REF}} = 1.7 \text{ to } 3.6 \text{ V}$, $V_{\text{DDA}} - V_{\text{REF}} < 1.2 \text{ V}$	± 4	± 7	LSB
EO	Offset error		± 2	± 3	
EG	Gain error		± 3	± 6	
ED	Differential linearity error		± 2	± 3	
EL	Integral linearity error		± 3	± 6	

1. Better performance could be achieved in restricted V_{DD} , frequency and temperature ranges.
2. Guaranteed by characterization results.

Table 79. ADC dynamic accuracy at $f_{\text{ADC}} = 18 \text{ MHz}$ - limited test conditions⁽¹⁾

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{\text{ADC}} = 18 \text{ MHz}$ $V_{\text{DDA}} = V_{\text{REF}+} = 1.7 \text{ V}$ Input Frequency = 20 kHz Temperature = 25 °C	10.3	10.4	-	bits
SINAD	Signal-to-noise and distortion ratio		64	64.2	-	dB
SNR	Signal-to-noise ratio		64	65	-	
THD	Total harmonic distortion		-	-72	-67	

1. Guaranteed by characterization results.

Table 80. ADC dynamic accuracy at $f_{\text{ADC}} = 36 \text{ MHz}$ - limited test conditions⁽¹⁾

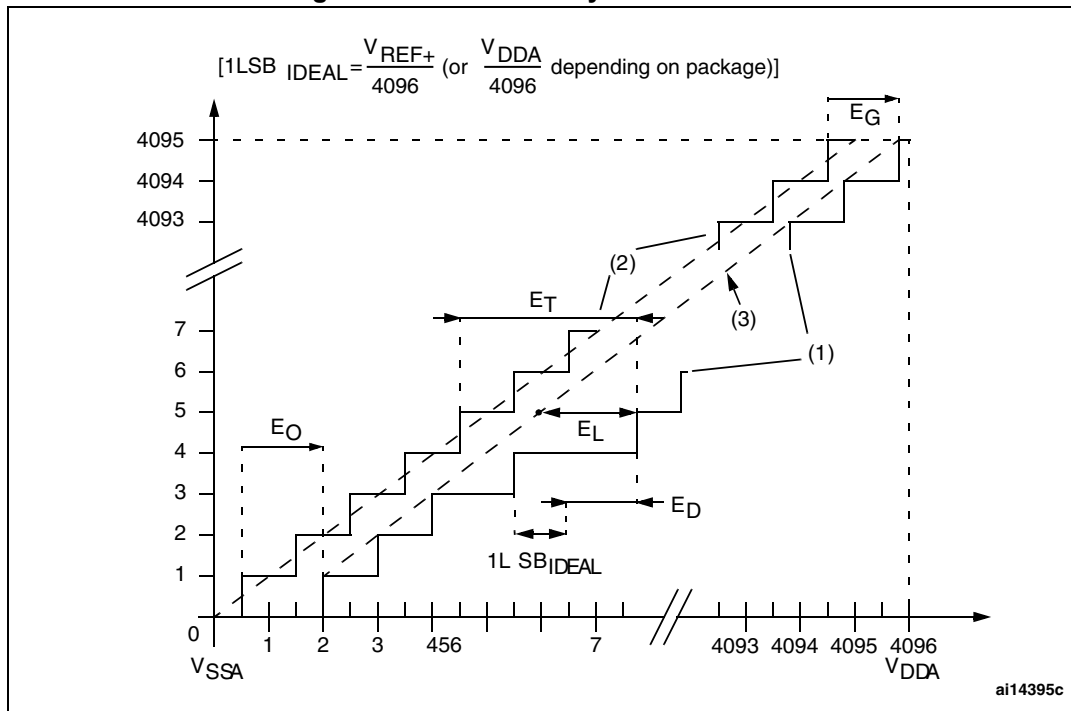
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ENOB	Effective number of bits	$f_{\text{ADC}} = 36 \text{ MHz}$ $V_{\text{DDA}} = V_{\text{REF}+} = 3.3 \text{ V}$ Input Frequency = 20 kHz Temperature = 25 °C	10.6	10.8	-	bits
SINAD	Signal-to noise and distortion ratio		66	67	-	dB
SNR	Signal-to noise ratio		64	68	-	
THD	Total harmonic distortion		-	-72	-70	

1. Guaranteed by characterization results.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

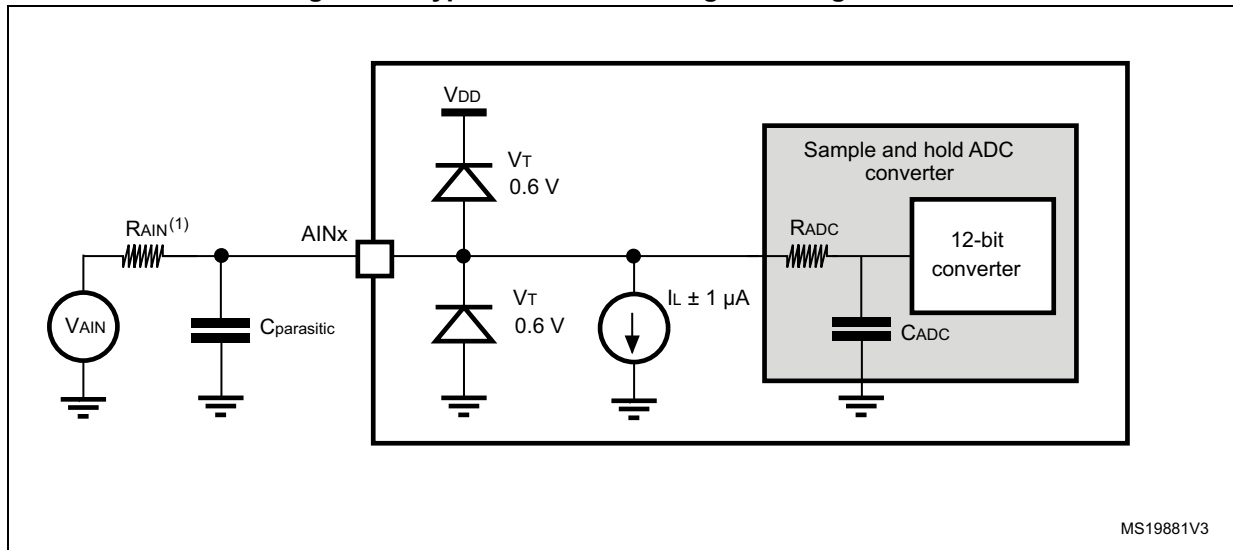
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in [Section 6.3.16](#) does not affect the ADC accuracy.

Figure 48. ADC accuracy characteristics



1. See also [Table 77](#).
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
 E_O = Offset Error: deviation between the first actual transition and the first ideal one.
 E_G = Gain Error: deviation between the last ideal transition and the last actual one.
 E_D = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
 E_L = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Figure 49. Typical connection diagram using the ADC

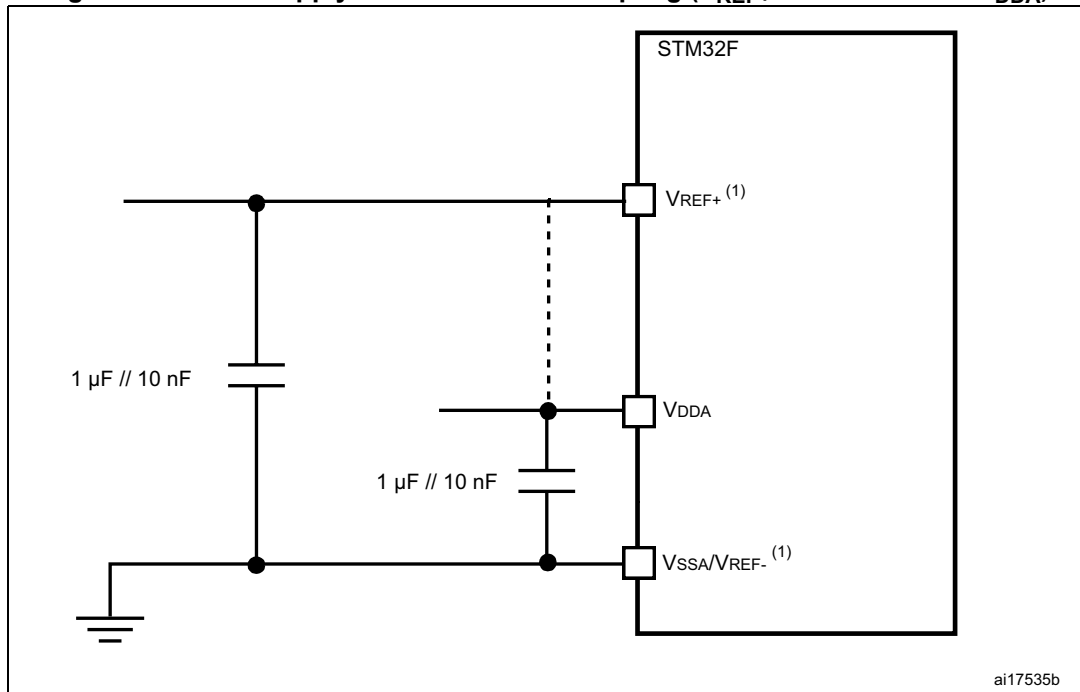


1. Refer to [Table 75](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

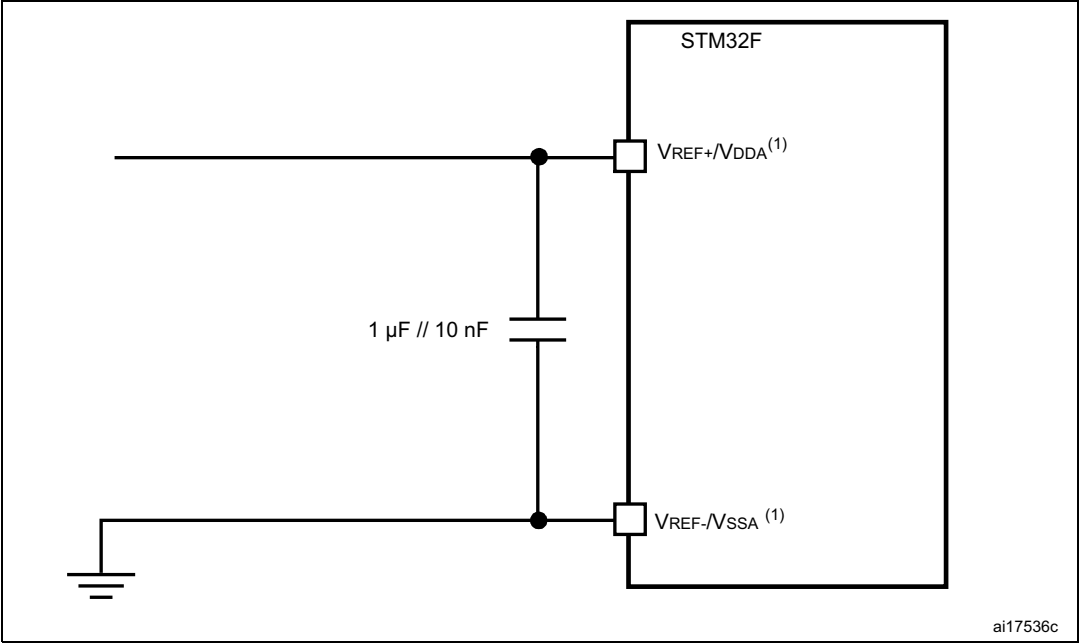
Power supply decoupling should be performed as shown in [Figure 50](#) or [Figure 51](#), depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

Figure 50. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

Figure 51. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA} .

6.3.21 Temperature sensor characteristics

Table 81. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_L^{(1)}$	V_{SENSE} linearity with temperature	-	± 1	± 2	$^{\circ}\text{C}$
Avg_Slope ⁽¹⁾	Average slope	-	2.5	-	mV/ $^{\circ}\text{C}$
$V_{25}^{(1)}$	Voltage at 25 $^{\circ}\text{C}$	-	0.76	-	V
$t_{START}^{(2)}$	Startup time	-	6	10	μs
$T_{S_temp}^{(2)}$	ADC sampling time when reading the temperature (1 $^{\circ}\text{C}$ accuracy)	10	-	-	μs

- Guaranteed by characterization results.
- Guaranteed by design.

Table 82. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 $^{\circ}\text{C}$, V_{DDA} = 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 $^{\circ}\text{C}$, V_{DDA} = 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

6.3.22 V_{BAT} monitoring characteristics

Table 83. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	K Ω
Q	Ratio on V_{BAT} measurement	-	4	-	
$E_r^{(1)}$	Error on Q	-1	-	+1	%
$T_{S_vbat}^{(2)(2)}$	ADC sampling time when reading the V_{BAT} 1 mV accuracy	5	-	-	μ s

1. Guaranteed by design.
2. Shortest sampling time can be determined in the application by multiple iterations.

6.3.23 Embedded reference voltage

The parameters given in [Table 84](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 17](#).

Table 84. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +125\text{ }^{\circ}\text{C}$	1.18	1.21	1.24	V
$T_{S_vrefint}^{(1)}$	ADC sampling time when reading the internal reference voltage	-	10	-	-	μ s
$V_{RERINT_s}^{(2)}$	Internal reference voltage spread over the temperature range	$V_{DD} = 3V \pm 10\text{mV}$	-	3	5	mV
$T_{Coeff}^{(2)}$	Temperature coefficient	-	-	30	50	ppm/ $^{\circ}\text{C}$
$t_{START}^{(2)}$	Startup time	-	-	6	10	μ s

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design

Table 85. Internal reference voltage calibration values

Symbol	Parameter	Memory address
V_{REFIN_CAL}	Raw data acquired at temperature of 30 $^{\circ}\text{C}$ $V_{DDA} = 3.3\text{ V}$	0x1FFF 7A2A - 0x1FFF 7A2B

6.3.24 DAC electrical characteristics

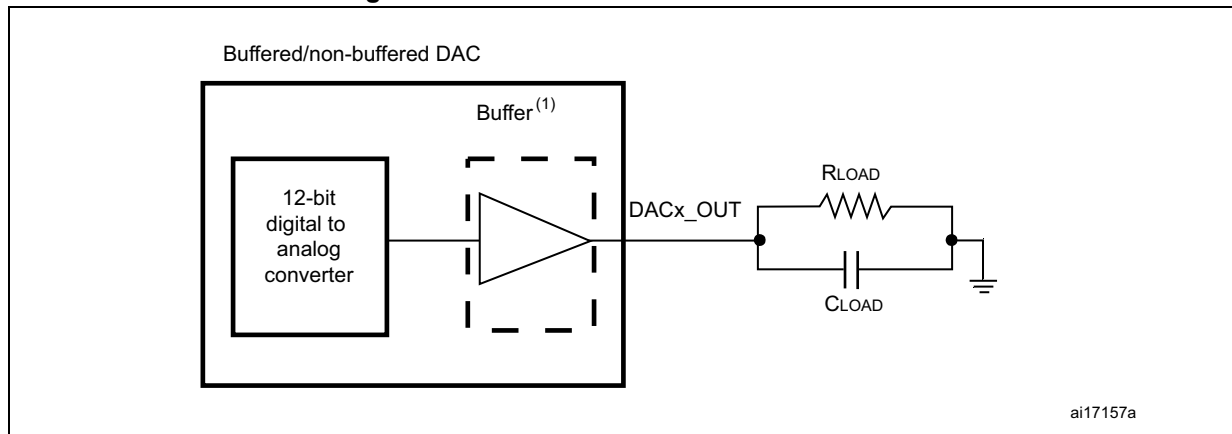
Table 86. DAC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit	Comments
V _{DDA}	Analog supply voltage	-		1.7 ⁽¹⁾	-	3.6	V	
V _{REF+}	Reference supply voltage	-		1.7 ⁽¹⁾	-	3.6	V	V _{REF+} ≤ V _{DDA}
V _{SSA}	Ground	-		0	-	0	V	-
R _{LOAD} ⁽²⁾	Resistive load	DAC output buffer ON	R _{LOAD} connected to V _{SSA}	5	-	-	kΩ	-
			R _{LOAD} connected to V _{DDA}	25	-	-	kΩ	-
R _O ⁽²⁾	Impedance output with buffer OFF	-		-	-	15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V _{SS} to have a 1% accuracy is 1.5 MΩ
C _{LOAD} ⁽²⁾	Capacitive load	-		-	-	50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT _{min} ⁽²⁾	Lower DAC_OUT voltage with buffer ON	-		0.2	-	-	V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V _{REF+} = 3.6 V and (0x1C7) to (0xE38) at V _{REF+} = 1.7 V
DAC_OUT _{max} ⁽²⁾	Higher DAC_OUT voltage with buffer ON	-		-	-	V _{DDA} – 0.2	V	
DAC_OUT _{min} ⁽²⁾	Lower DAC_OUT voltage with buffer OFF	-		-	0.5	-	mV	It gives the maximum output excursion of the DAC.
DAC_OUT _{max} ⁽²⁾	Higher DAC_OUT voltage with buffer OFF	-		-	-	V _{REF+} – 1LSB	V	
I _{VREF+} ⁽⁴⁾	DAC DC V _{REF} current consumption in quiescent mode (Standby mode)	-		-	170	240	μA	With no load, worst code (0x800) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs
		-		-	50	75		With no load, worst code (0xF1C) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs
I _{DDA} ⁽⁴⁾	DAC DC V _{DDA} current consumption in quiescent mode ⁽³⁾	-		-	280	380	μA	With no load, middle code (0x800) on the inputs
		-		-	475	625	μA	With no load, worst code (0xF1C) at V _{REF+} = 3.6 V in terms of DC consumption on the inputs

Table 86. DAC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Comments
DNL ⁽⁴⁾	Differential non linearity Difference between two consecutive code-1LSB)	-	-	-	±0.5	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±2	LSB	Given for the DAC in 12-bit configuration.
INL ⁽⁴⁾	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	-	±1	LSB	Given for the DAC in 10-bit configuration.
		-	-	-	±4	LSB	Given for the DAC in 12-bit configuration.
Offset ⁽⁴⁾	Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{REF+}/2$)	-	-	-	±10	mV	Given for the DAC in 12-bit configuration
		-	-	-	±3	LSB	Given for the DAC in 10-bit at $V_{REF+} = 3.6$ V
		-	-	-	±12	LSB	Given for the DAC in 12-bit at $V_{REF+} = 3.6$ V
Gain error ⁽⁴⁾	Gain error	-	-	-	±0.5	%	Given for the DAC in 12-bit configuration
$t_{SETTLING}^{(4)}$	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±4LSB)	-	-	3	6	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
THD ⁽⁴⁾	Total Harmonic Distortion Buffer ON	-	-	-	-	dB	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
Update rate ⁽²⁾	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	-	1	MS/s	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ
$t_{WAKEUP}^{(4)}$	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	-	6.5	10	µs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ input code between lowest and highest possible ones.
PSRR+ ⁽²⁾	Power supply rejection ratio (to V_{DDA}) (static DC measurement)	-	-	-67	-40	dB	No R_{LOAD} , $C_{LOAD} = 50$ pF

1. V_{DDA} minimum value of 1.7 V is obtained with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)).
2. Guaranteed by design.
3. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
4. Guaranteed by characterization results.

Figure 52. 12-bit buffered /non-buffered DAC

1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.25 DFSDM characteristics

Unless otherwise specified, the parameters given in [Table 87](#) for DFSDM are derived from tests performed under the ambient temperature, f_{APB2} frequency and V_{DD} supply voltage conditions summarized in [Table 17: General operating conditions](#).

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5 * V_{DD}$

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (DFSDM_CKINy, DFSDM_DATINy, DFSDM_CKOUT for DFSDM).

Table 87. DFSDM characteristics⁽¹⁾

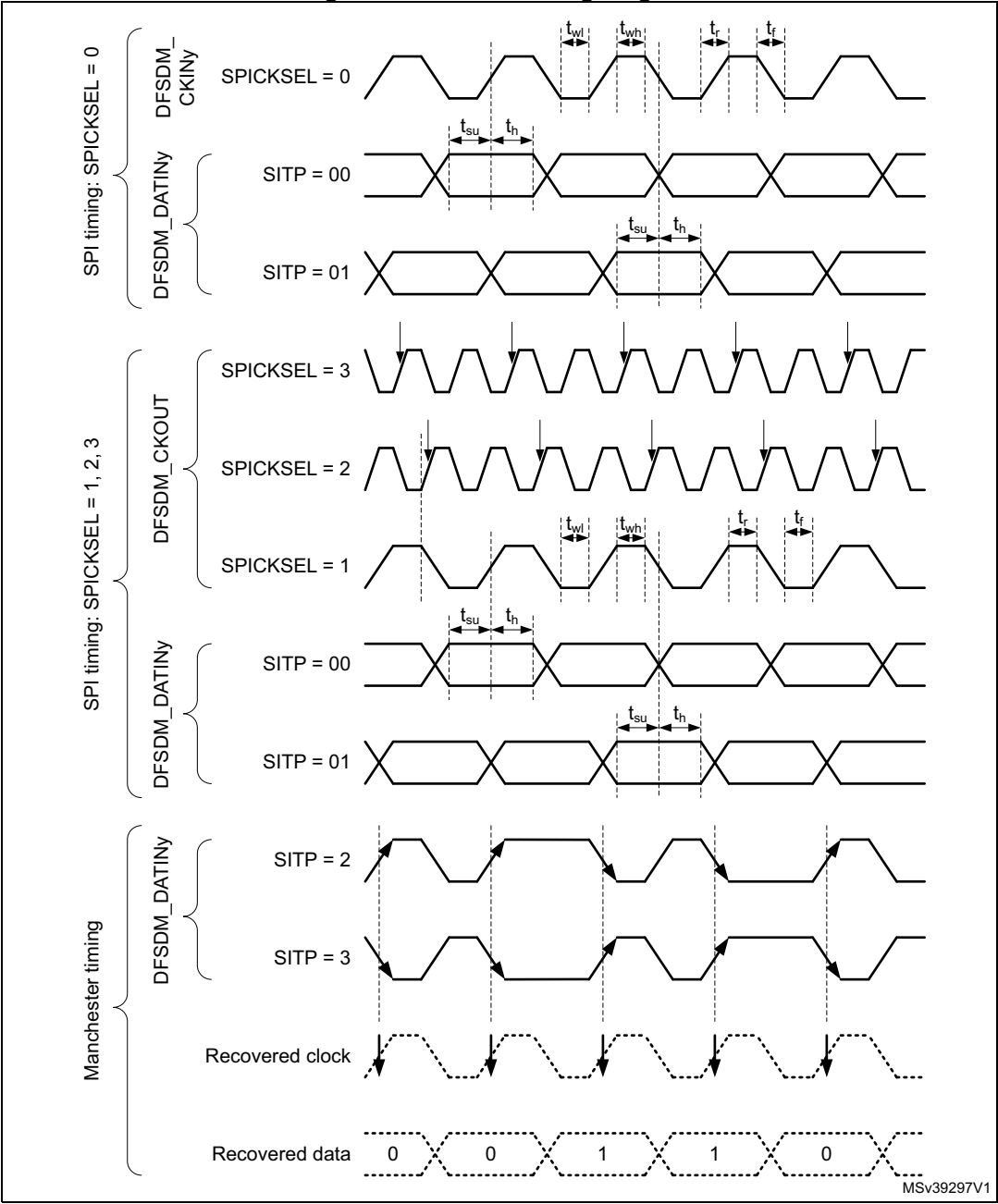
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{DFSDMCLK}$	DFSDM clock	$1.71 < V_{DD} < 3.6$ V	-	-	f_{SYSCLK}	
f_{CKIN} ($1/T_{CKIN}$)	Input clock frequency	SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0, $1.71 < V_{DD} < 3.6$ V	-	-	20 ($f_{DFBDMCLK} / 4$)	MHz
		SPI mode (SITP[1:0] = 0,1), External clock mode (SPICKSEL[1:0] = 0, $2.7 < V_{DD} < 3.6$ V	-	-	20 ($f_{DFBDMCLK} / 4$)	
		SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] ≠ 0, $1.71 < V_{DD} < 3.6$ V	-	-	20 ($f_{DFBDMCLK} / 4$)	
		SPI mode (SITP[1:0] = 0,1), Internal clock mode (SPICKSEL[1:0] ≠ 0, $2.7 < V_{DD} < 3.6$ V	-	-	20 ($f_{DFBDMCLK} / 4$)	
f_{CKOUT}	Output clock frequency	$1.71 < V_{DD} < 3.6$ V	-	-	20	
$DuCy_{CKOUT}$	Output clock frequency duty cycle	$1.71 < V_{DD} < 3.6$ V	45	50	55	%

Table 87. DFSDM characteristics⁽¹⁾ (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{wh}(CKIN)$ $t_{wl}(CKIN)$	Input clock high and low time	SPI mode (SITP[1:0] = 01), External clock mode (SPICKSEL[1:0] = 0) $1.71 < V_{DD} < 3.6 \text{ V}$	$t_{CKIN} / 2 - 0.5$	$t_{CKIN} / 2$	-	ns
t_{su}	Data input setup time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0) $1.71 < V_{DD} < 3.6 \text{ V}$	3.5	-	-	
t_h	Data input hold time	SPI mode (SITP[1:0]=01), External clock mode (SPICKSEL[1:0] = 0) $1.71 < V_{DD} < 3.6 \text{ V}$	2.5	-	-	
$T_{Manchester}$	Manchester data period (recovered clock period)	Manchester mode (SITP[1:0] = 10 or 11), Internal clock mode (SPICKSEL[1:0] $\neq$ 0) $1.71 < V_{DD} < 3.6 \text{ V}$	$(CKOUTDIV + 1) * t_{DFBDMCLK}$	-	$(2 * CKOUTDIV) * t_{DFBDMCLK}$	

1. Data based on characterization results.

Figure 16: DFSDM timing diagram



6.3.26 FSMC characteristics

Unless otherwise specified, the parameters given in [Table 88](#) to [Table 95](#) for the FSMC interface are derived from tests performed under the ambient temperature, f_{HCLK} frequency and V_{DD} supply voltage conditions summarized in [Table 16](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitance load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5 \cdot V_{DD}$

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output characteristics.

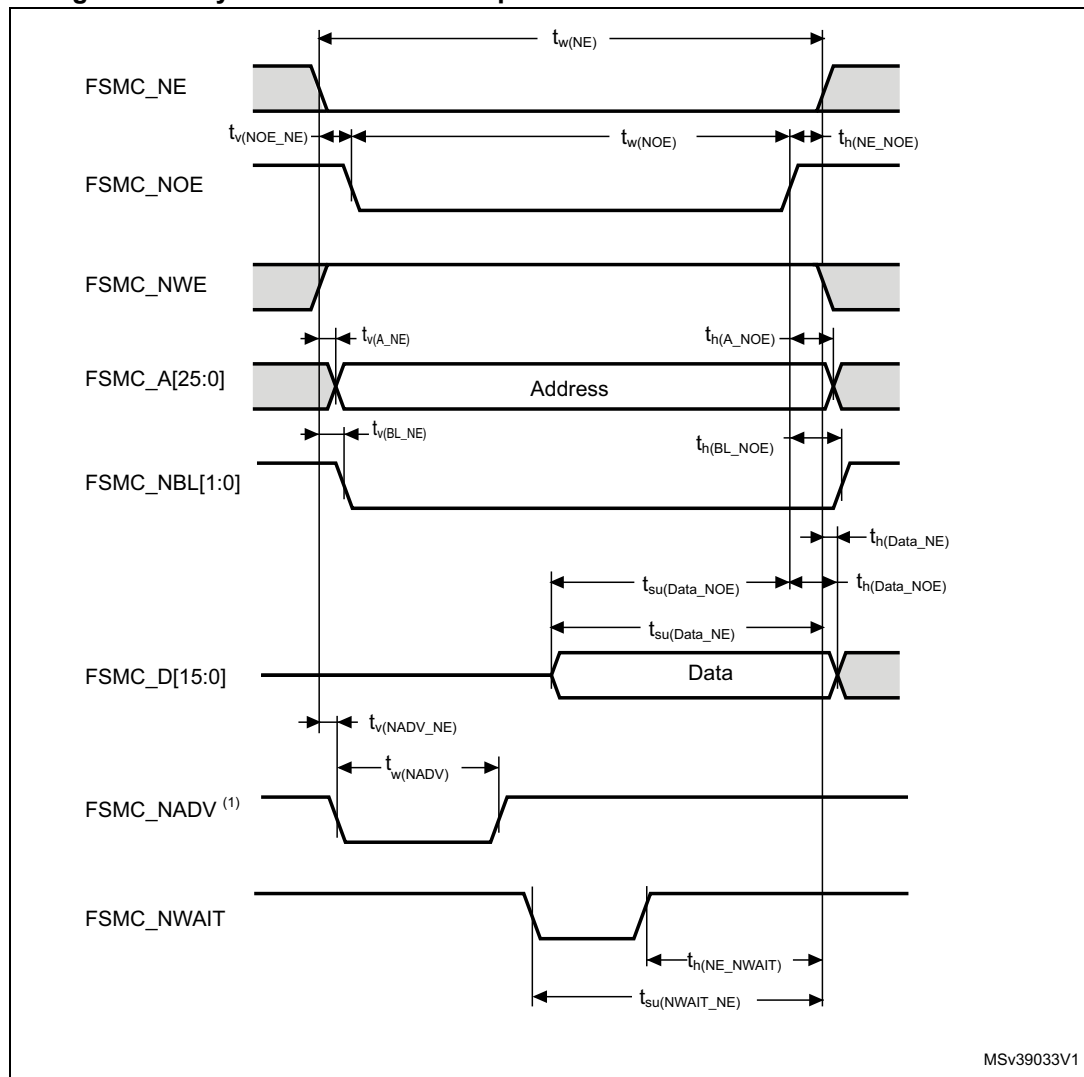
Asynchronous waveforms and timings

[Figure 53](#) through [Figure 56](#) represent asynchronous waveforms and [Table 88](#) through [Table 95](#) provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode, DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0

In all timing tables, the T_{HCLK} is the HCLK clock period.

Figure 53. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 88. Asynchronous non-multiplexed SRAM/PSRAM/NOR - read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$2 * t_{HCLK} - 1$	$2 * t_{HCLK} + 1$	ns
$t_{v(NOE_NE)}$	FSMC_NEx low to FSMC_NOE low	0	0.5	
$t_{w(NOE)}$	FSMC_NOE low time	$2 * t_{HCLK} - 1$	$2 * t_{HCLK} + 1$	
$t_{h(NE_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	0.5	
$t_{h(A_NOE)}$	Address hold time after FSMC_NOE high	0	-	
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{h(BL_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0	-	
$t_{su(Data_NE)}$	Data to FSMC_NEx high setup time	$t_{HCLK} - 2$	-	
$t_{su(Data_NOE)}$	Data to FSMC_NOEx high setup time	$t_{HCLK} - 2$	-	
$t_{h(Data_NOE)}$	Data hold time after FSMC_NOE high	0	-	
$t_{h(Data_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	-	0	
$t_{w(NADV)}$	FSMC_NADV low time	-	$t_{HCLK} + 1$	

1. $C_L = 30$ pF.

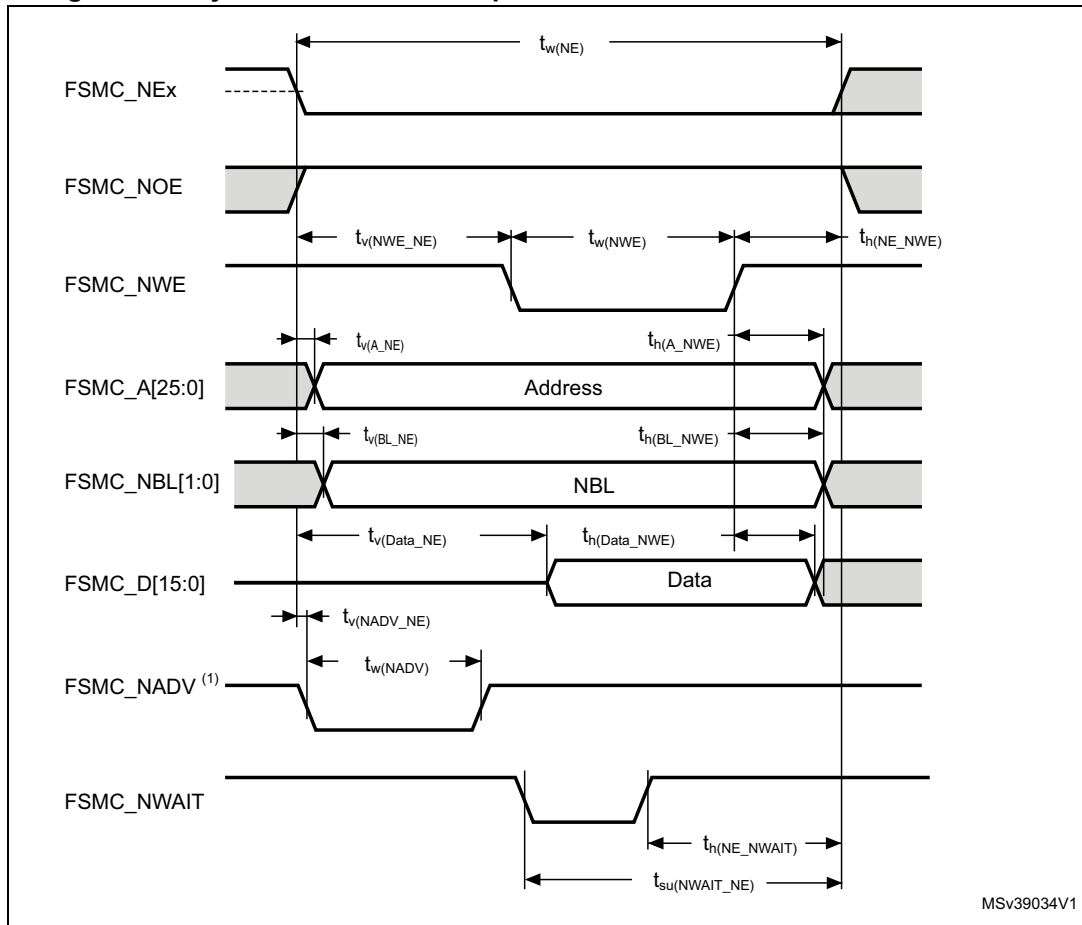
2. Based on characterization.

Table 89. Asynchronous non-multiplexed SRAM/PSRAM/NOR read - NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7 * t_{HCLK} + 1$	$7 * t_{HCLK} + 1$	ns
$t_{w(NOE)}$	FSMC_NWE low time	$5 * t_{HCLK} - 1$	$5 * t_{HCLK} + 1$	
$t_{w(NWAIT)}$	FSMC_NWAIT low time	$t_{HCLK} - 0.5$	-	
$t_{su(NWAIT_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$5 * t_{HCLK} + 1.5$	-	
$t_{h(NE_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4 * t_{HCLK} + 1$	-	

1. $C_L = 30$ pF.

2. Based on characterization.

Figure 54. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms

1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 90. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NEx low time	$3 * t_{HCLK} - 1$	$3 * t_{HCLK} - 1$	ns
$t_{v(NWE_NE)}$	FSMC_NEx low to FSMC_NWE low	$t_{HCLK} - 1$	$t_{HCLK} + 0.5$	
$t_{w(NWE)}$	FSMC_NWE low time	$t_{HCLK} - 1.5$	$t_{HCLK} + 0.5$	
$t_{h(NE_NWE)}$	FSMC_NWE high to FSMC_NEx high hold time	t_{HCLK}	-	
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	
$t_{h(A_NWE)}$	Address hold time after FSMC_NWE high	$t_{HCLK} - 0.5$	-	
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_NBL valid	-	0.5	
$t_{h(BL_NWE)}$	FSMC_NBL hold time after FSMC_NWE high	$t_{HCLK} - 0.5$	-	
$t_{v(Data_NE)}$	Data to FSMC_NEx low to Data valid	-	$t_{HCLK} + 2.5$	
$t_{h(Data_NWE)}$	Data hold time after FSMC_NWE high	t_{HCLK}	-	
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	-	0	
$t_{w(NADV)}$	FSMC_NADV low time	-	$t_{HCLK} + 1$	

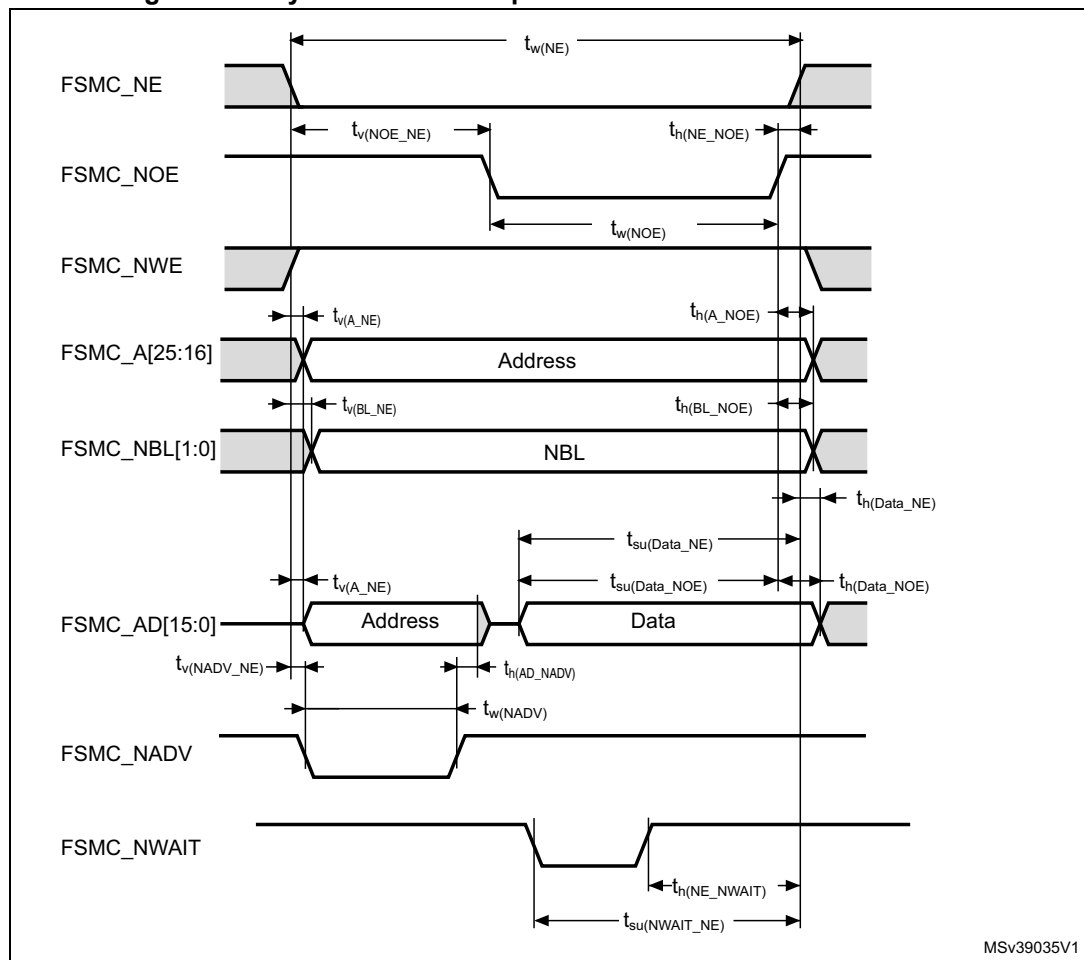
1. $C_L = 30$ pF.
2. Based on characterization.

Table 91. Asynchronous non-multiplexed SRAM/PSRAM/NOR write - NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$8 * t_{HCLK} - 1$	$8 * t_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$6 * t_{HCLK} - 1.5$	$6 * t_{HCLK} + 0.5$	
$t_{su(NWAIT_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$6 * t_{HCLK} - 1$	-	
$t_{h(NE_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4 * t_{HCLK} + 2$	-	

1. $C_L = 30$ pF.
2. Based on characterization.

Figure 55. Asynchronous multiplexed PSRAM/NOR read waveforms



MSv39035V1

Table 92. Asynchronous multiplexed PSRAM/NOR read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3 * t_{HCLK} - 1$	$3 * t_{HCLK} + 1$	ns
$t_{v(NOE_NE)}$	FSMC_NEx low to FSMC_NOE low	$2 * t_{HCLK}$	$2 * t_{HCLK} + 0.5$	
$t_{w(NOE)}$	FSMC_NOE low time	$t_{HCLK} - 1$	$t_{HCLK} + 1$	
$t_{h(NE_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	0.5	
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	0	0.5	
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} - 0.5$	$t_{HCLK} + 1$	
$t_{h(AD_NADV)}$	FSMC_AD(address) valid hold time after FSMC_NADV high	$t_{HCLK} + 0.5$	-	
$t_{h(A_NOE)}$	Address hold time after FSMC_NOE high	$t_{HCLK} - 0.5$	-	
$t_{h(BL_NOE)}$	FSMC_BL time after FSMC_NOE high	0	-	
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{su(Data_NE)}$	Data to FSMC_NEx high setup time	$t_{HCLK} - 2$	-	
$t_{su(Data_NOE)}$	Data to FSMC_NOE high setup time	$t_{HCLK} - 2$	-	
$t_{h(Data_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{h(Data_NOE)}$	Data hold time after FSMC_NOE high	0	-	

1. $C_L = 30$ pF.

2. Based on characterization.

Table 93. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$8 * t_{HCLK} - 1$	$8 * t_{HCLK} + 1$	ns
$t_{w(NOE)}$	FSMC_NWE low time	$5 * t_{HCLK} - 1.5$	$5 * t_{HCLK} + 0.5$	
$t_{su(NWAIT_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$5 * t_{HCLK} + 1.5$	-	
$t_{h(NE_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4 * t_{HCLK} + 1$	-	

1. $C_L = 30$ pF.

2. Based on characterization.

Figure 56. Asynchronous multiplexed PSRAM/NOR write waveforms

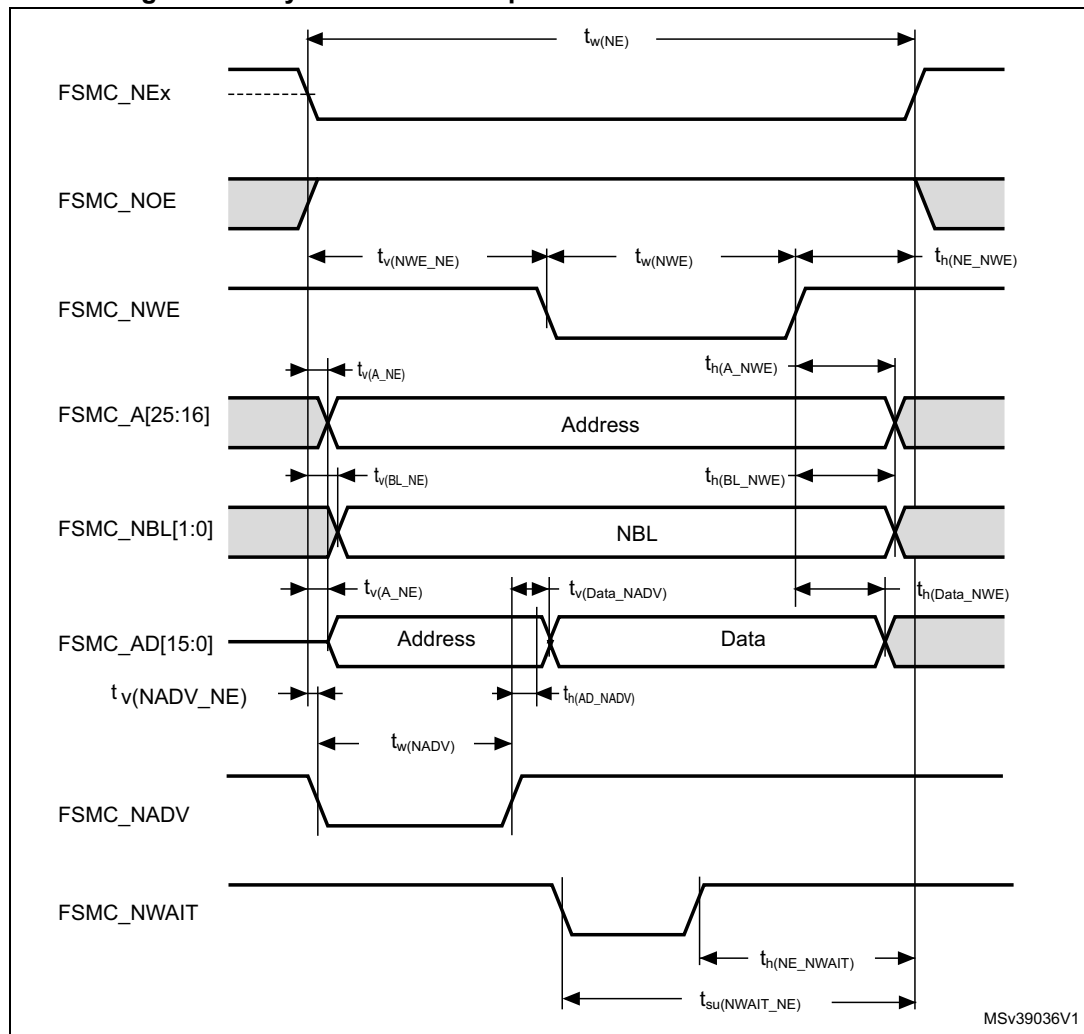


Table 94. Asynchronous multiplexed PSRAM/NOR write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$4 * T_{HCLK} - 1$	$4 * T_{HCLK} + 1$	ns
$t_{v(NWE_NE)}$	FSMC_NEx low to FSMC_NWE low	$T_{HCLK} - 1$	$T_{HCLK} + 0.5$	
$t_{w(NWE)}$	FSMC_NWE low time	$2 * T_{HCLK} - 0.5$	$2 * T_{HCLK} - 0.5$	
$t_{h(NE_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	$T_{HCLK} - 0.5$	-	
$t_{v(A_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	
$t_{v(NADV_NE)}$	FSMC_NEx low to FSMC_NADV low	0	0.5	
$t_{w(NADV)}$	FSMC_NADV low time	T_{HCLK}	$T_{HCLK} + 1$	
$t_{h(AD_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	$T_{HCLK} + 0.5$	-	
$t_{h(A_NWE)}$	Address hold time after FSMC_NWE high	$T_{HCLK} + 0.5$	-	
$t_{h(BL_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$T_{HCLK} - 0.5$	-	
$t_{v(BL_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	
$t_{v(Data_NADV)}$	FSMC_NADV high to Data valid	-	$T_{HCLK} + 2.5$	
$t_{h(Data_NWE)}$	Data hold time after FSMC_NWE high	T_{HCLK}	-	

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Table 95. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$9 * T_{HCLK} - 1$	$9 * T_{HCLK} + 1$	ns
$t_{w(NWE)}$	FSMC_NWE low time	$7 * T_{HCLK} - 0.5$	$7 * T_{HCLK} + 0.5$	
$t_{su(NWAIT_NE)}$	FSMC_NWAIT valid before FSMC_NEx high	$6 * T_{HCLK} + 2$	-	
$t_{h(NE_NWAIT)}$	FSMC_NEx hold time after FSMC_NWAIT invalid	$4 * T_{HCLK} - 1$	-	

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Synchronous waveforms and timings

[Figure 57](#) through [Figure 60](#) represent synchronous waveforms and [Table 96](#) through [Table 99](#) provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F446 reference manual: RM0390)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 57. Synchronous multiplexed NOR/PSRAM read timings

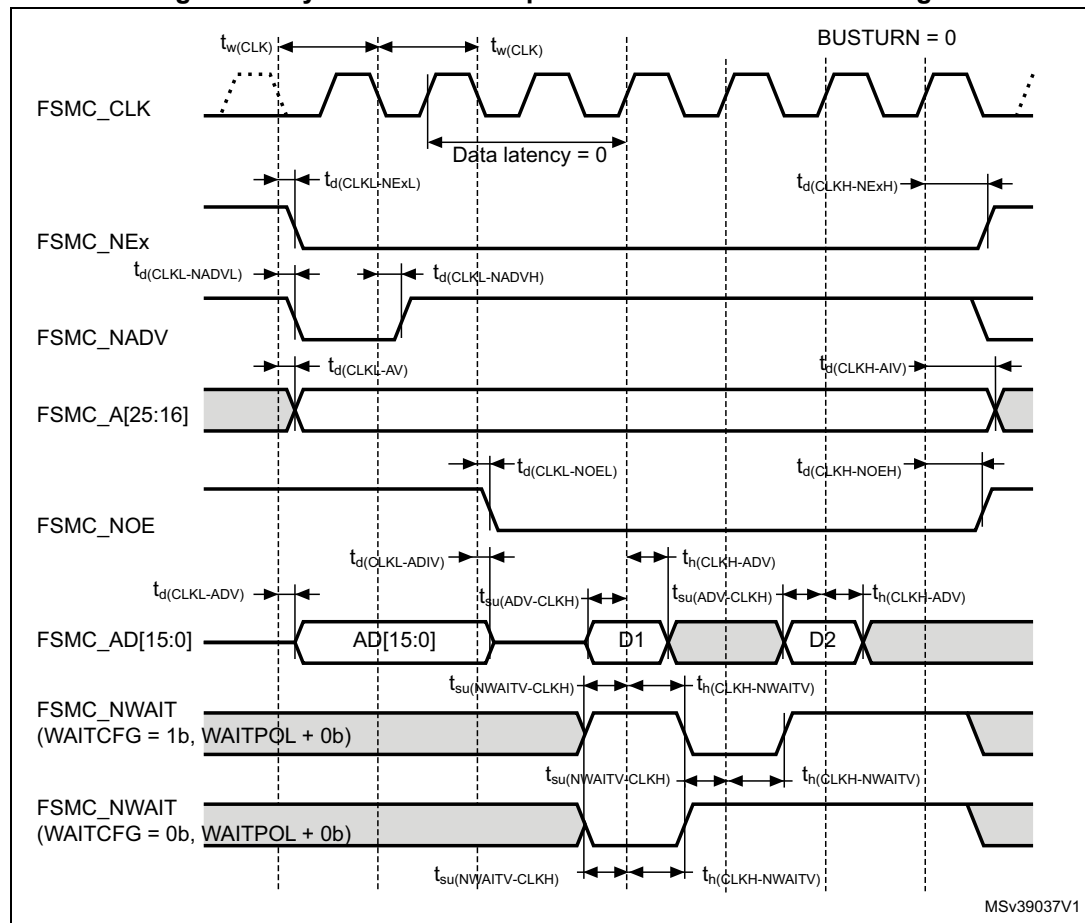


Table 96. Synchronous multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	$2 * T_{HCLK} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x=0..2)	-	2	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high (x= 0...2)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-NADV_L)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADV_H)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x=16...25)	-	2.5	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid (x=16...25)	T_{HCLK}	-	
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{d(CLKH-NOEH)}$	FSMC_CLK high to FSMC_NOE high	$T_{HCLK} - 0.5$	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{su(ADV-CLKH)}$	FSMC_A/D[15:0] valid data before FSMC_CLK high	1.5	-	
$t_h(CLKH-ADV)$	FSMC_A/D[15:0] valid data after FSMC_CLK high	3.5	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2.5	-	
$t_h(CLKH-NWAIT)$	FSMC_NWAIT valid after FSMC_CLK high	3.5	-	

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Figure 58. Synchronous multiplexed PSRAM write timings

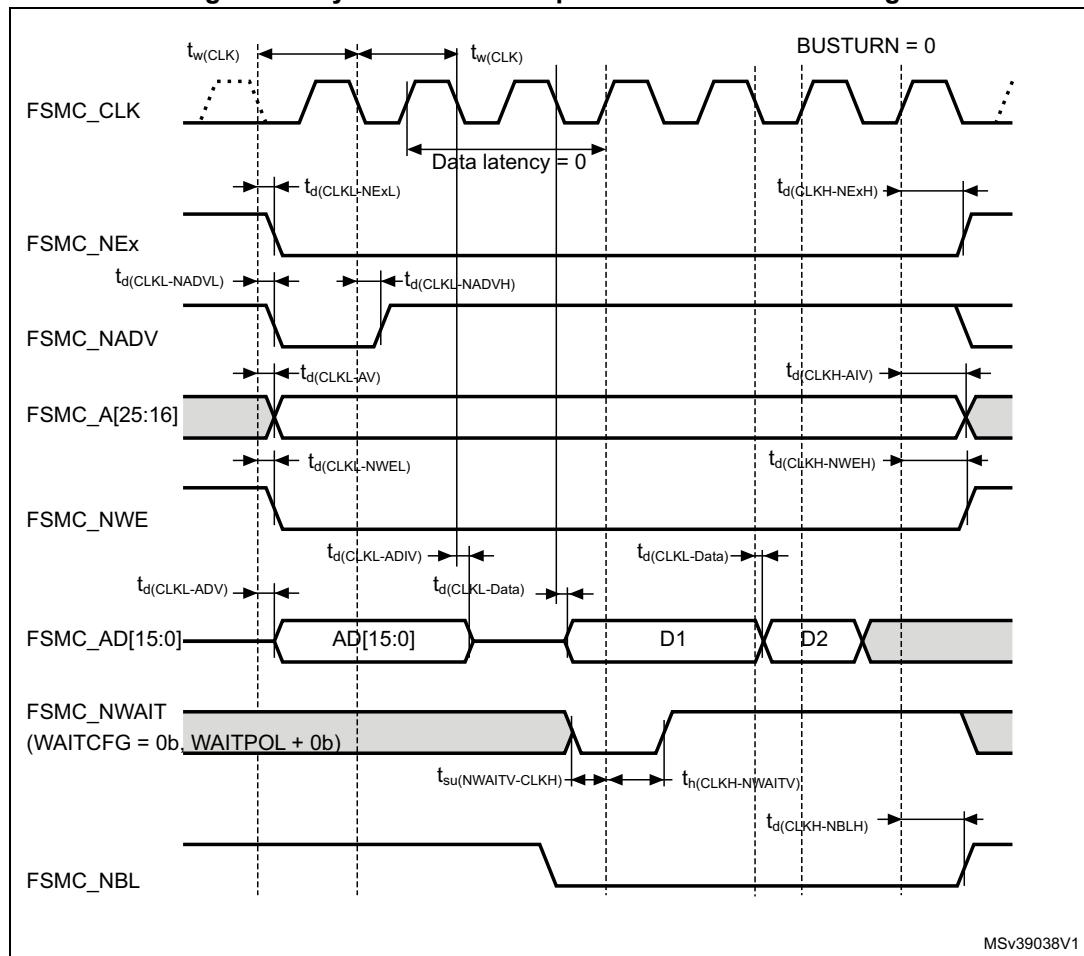


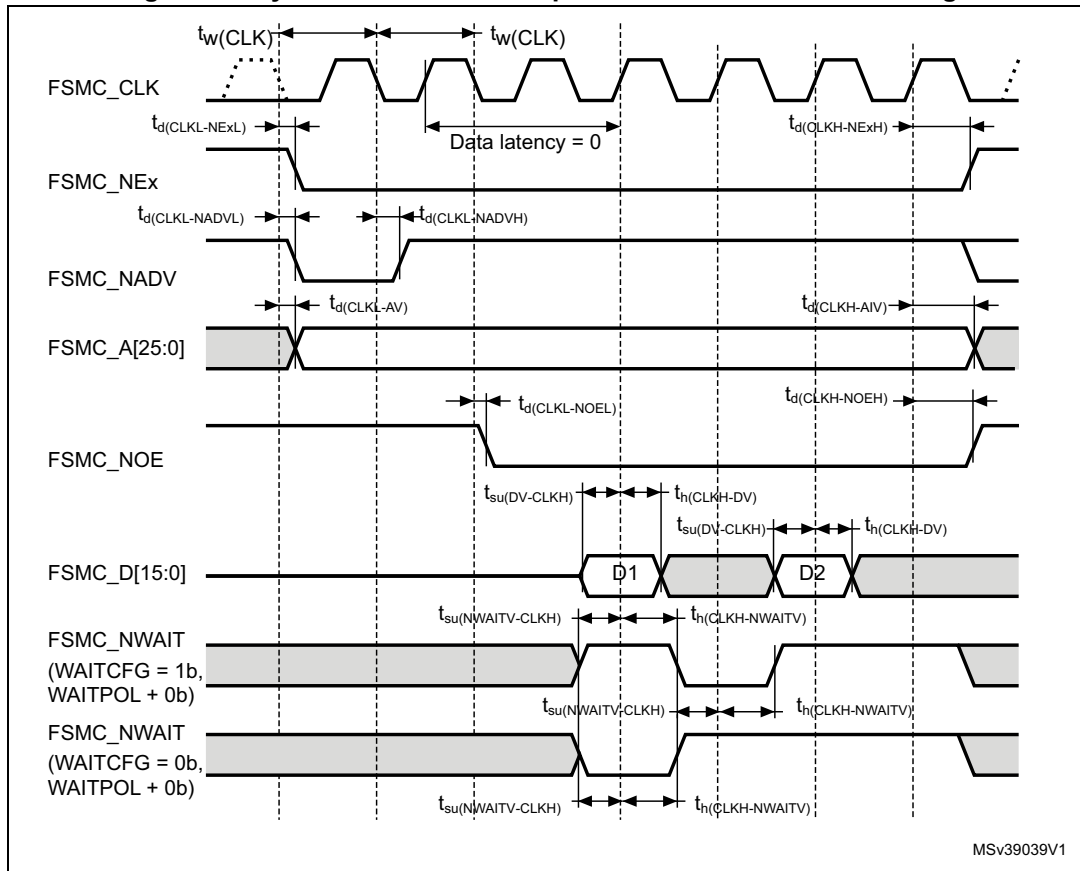
Table 97. Synchronous multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period, V_{DD} range= 2.7 to 3.6 V	$2 * T_{HCLK} - 0.5$	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low ($x= 0...2$)	-	2	
$t_{d(CLKH-NExH)}$	FSMC_CLK high to FSMC_NEx high ($x= 0...2$)	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-NADV_L)}$	FSMC_CLK low to FSMC_NADV low	-	1	
$t_{d(CLKL-NADV_H)}$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid ($x=16...25$)	-	2.5	
$t_{d(CLKH-AIV)}$	FSMC_CLK high to FSMC_Ax invalid ($x=16...25$)	T_{HCLK}	-	
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_{d(CLKH-NWEH)}$	FSMC_CLK high to FSMC_NWE high	$T_{HCLK} + 0.5$	-	
$t_{d(CLKL-ADV)}$	FSMC_CLK low to FSMC_AD[15:0] valid	-	3	
$t_{d(CLKL-ADIV)}$	FSMC_CLK low to FSMC_AD[15:0] invalid	0	-	
$t_{d(CLKL-DATA)}$	FSMC_A/D[15:0] valid data after FSMC_CLK low	-	4	
$t_{d(CLKL-NBLL)}$	FSMC_CLK low to FSMC_NBL low	0	2	
$t_{d(CLKH-NBLH)}$	FSMC_CLK high to FSMC_NBL high	$T_{HCLK} + 0.5$	-	
$t_{su(NWAIT-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_h(CLKH-NWAIT)$	FSMC_NWAIT valid after FSMC_CLK high	3.5	-	

1. $C_L = 30$ pF.

2. Guaranteed by characterization results.

Figure 59. Synchronous non-multiplexed NOR/PSRAM read timings

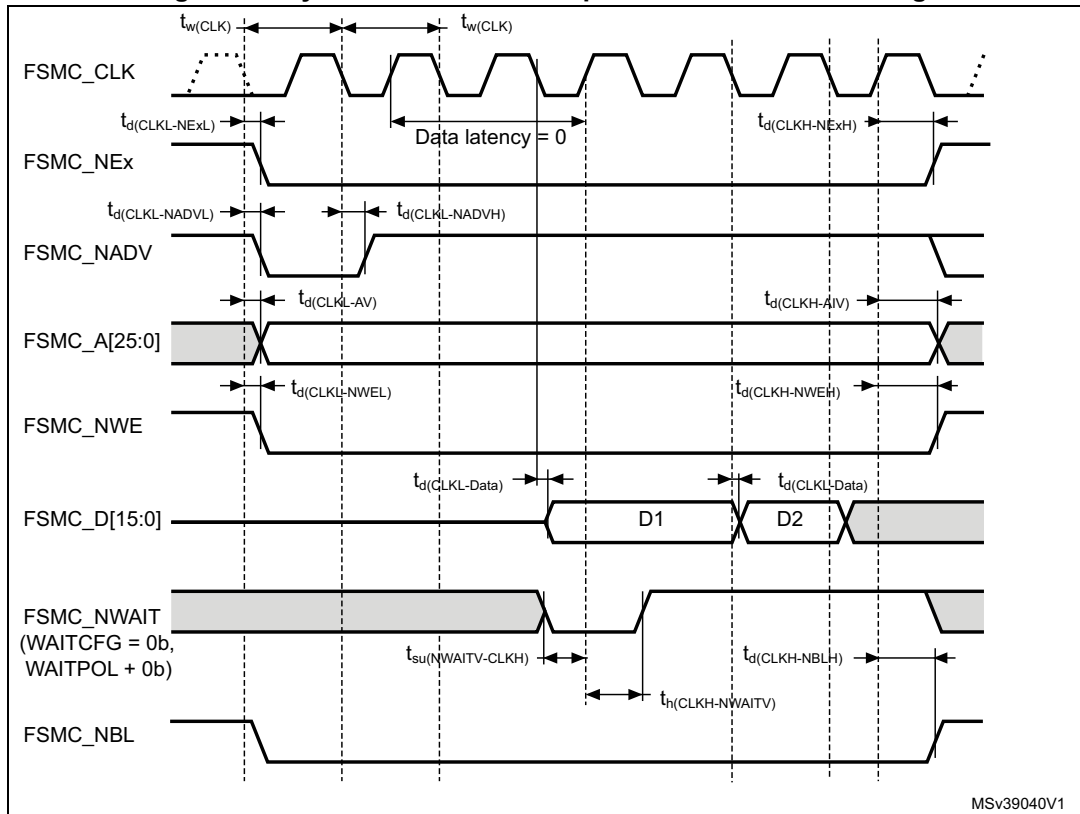
Table 98. Synchronous non-multiplexed NOR/PSRAM read timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FSMC_CLK period	$2T_{\text{HCLK}} - 0.5$	-	ns
$t_{\text{d}}(\text{CLKL-NExL})$	FSMC_CLK low to FSMC_NEx low ($x=0..2$)	-	2	
$t_{\text{d}}(\text{CLKH-NExH})$	FSMC_CLK high to FSMC_NEx high ($x=0..2$)	$T_{\text{HCLK}} + 0.5$	-	
$t_{\text{d}}(\text{CLKL-NADVL})$	FSMC_CLK low to FSMC_NADV low	-	0.5	
$t_{\text{d}}(\text{CLKL-NADVH})$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_{\text{d}}(\text{CLKL-AV})$	FSMC_CLK low to FSMC_Ax valid ($x=16..25$)	-	2.5	
$t_{\text{d}}(\text{CLKH-AIV})$	FSMC_CLK high to FSMC_Ax invalid ($x=16..25$)	T_{HCLK}	-	
$t_{\text{d}}(\text{CLKL-NOEL})$	FSMC_CLK low to FSMC_NOE low	-	1.5	
$t_{\text{d}}(\text{CLKH-NOEH})$	FSMC_CLK high to FSMC_NOE high	$T_{\text{HCLK}} - 0.5$	-	
$t_{\text{su}}(\text{DV-CLKH})$	FSMC_D[15:0] valid data before FSMC_CLK high	1.5	-	
$t_{\text{h}}(\text{CLKH-DV})$	FSMC_D[15:0] valid data after FSMC_CLK high	3.5	-	
$t_{\text{su}}(\text{NWAIT-CLKH})$	FSMC_NWAIT valid before FSMC_CLK high	2.5	-	
$t_{\text{h}}(\text{CLKH-NWAIT})$	FSMC_NWAIT valid after FSMC_CLK high	3.5	-	

1. $C_L = 30 \text{ pF}$.

2. Guaranteed by characterization results.

Figure 60. Synchronous non-multiplexed PSRAM write timings

Table 99. Synchronous non-multiplexed PSRAM write timings⁽¹⁾⁽²⁾

Symbol	Parameter	Min	Max	Unit
$t_w(\text{CLK})$	FSMC_CLK period	$2 * T_{\text{HCLK}} - 0.5$	-	ns
$t_d(\text{CLKL-NExL})$	FSMC_CLK low to FSMC_NEx low ($x=0..2$)	-	2	
$t_d(\text{CLKH-NExH})$	FSMC_CLK high to FSMC_NEx high ($x=0..2$)	$T_{\text{HCLK}} + 0.5$	-	
$t_d(\text{CLKL-NADVL})$	FSMC_CLK low to FSMC_NADV low	-	0.5	
$t_d(\text{CLKL-NADVH})$	FSMC_CLK low to FSMC_NADV high	0	-	
$t_d(\text{CLKL-AV})$	FSMC_CLK low to FSMC_Ax valid ($x=16..25$)	-	2.5	
$t_d(\text{CLKH-AIV})$	FSMC_CLK high to FSMC_Ax invalid ($x=16..25$)	T_{HCLK}	-	
$t_d(\text{CLKL-NWEL})$	FSMC_CLK low to FSMC_NWE low	-	1.5	
$t_d(\text{CLKH-NWEH})$	FSMC_CLK high to FSMC_NWE high	$T_{\text{HCLK}} + 1$	-	
$t_d(\text{CLKL-Data})$	FSMC_D[15:0] valid data after FSMC_CLK low	-	4	
$t_d(\text{CLKL-NBL})$	FSMC_CLK low to FSMC_NBL low	-	2	
$t_d(\text{CLKH-NBLH})$	FSMC_CLK high to FSMC_NBL high	$T_{\text{HCLK}} + 1$	-	
$t_{su}(\text{NWAIT-CLKH})$	FSMC_NWAIT valid before FSMC_CLK high	2	-	
$t_h(\text{CLKH-NWAIT})$	FSMC_NWAIT valid after FSMC_CLK high	3.5	-	

1. $C_L = 30 \text{ pF}$.

2. Guaranteed by characterization results.

6.3.27 SD/SDIO MMC/eMMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in [Table 100](#) for the SDIO are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DD} supply voltage conditions summarized in [Table 17](#), with the following configuration:

- Output speed is set to $OSPEEDRy[1:0] = 10$
- Capacitive load $C = 30$ pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output characteristics.

Figure 61. SDIO high-speed mode

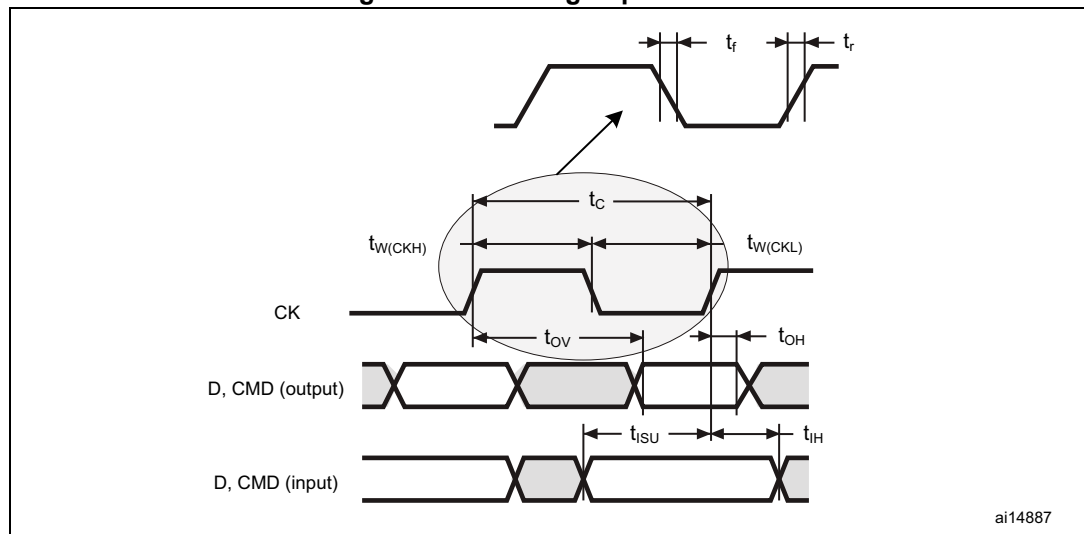


Figure 62. SD default mode

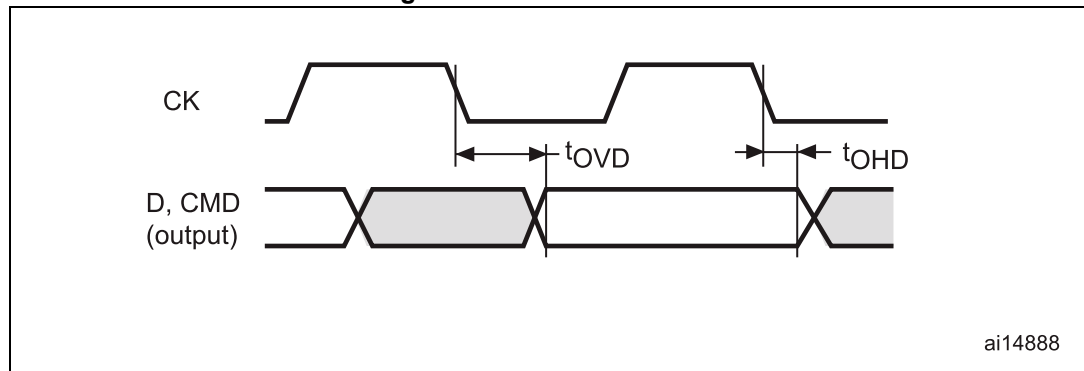


Table 100. SD / MMC characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8 / 3	-
t _{W(CKL)}	Clock low time	fpp =50MHz	9.5	10.5	-	ns
t _{W(CKH)}	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t _{ISU}	Input setup time HS	fpp =50MHz	5	-	-	ns
t _{IH}	Input hold time HS	fpp =50MHz	1	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t _{OV}	Output valid time HS	fpp =50MHz	-	12	13.5	ns
t _{OH}	Output hold time HS	fpp =50MHz	10.5	-	-	
CMD, D inputs (referenced to CK) in SD default mode						
t _{ISUD}	Input setup time SD	fpp =25MHz	5	-	-	ns
t _{IHD}	Input hold time SD	fpp =25MHz	1	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t _{OVD}	Output valid default time SD	fpp =25 MHz	-	2	3	ns
t _{OHD}	Output hold default time SD	fpp =25 MHz	1	-	-	

1. Guaranteed by characterization results.

2. V_{DD} = 2.7 to 3.6 V.Table 101. eMMC characteristics V_{DD} = 1.7 V to 1.9 V⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	8 / 3	-
t _{W(CKL)}	Clock low time	fpp =50MHz	9.5	10.5	-	ns
t _{W(CKH)}	Clock high time	fpp =50MHz	8.5	9.5	-	
CMD, D inputs (referenced to CK) in eMMC mode						
t _{ISU}	Input setup time HS	fpp =50MHz	3	-	-	ns
t _{IH}	Input hold time HS	fpp =50MHz	2.5	-	-	
CMD, D outputs (referenced to CK) in eMMC mode						
t _{OV}	Output valid time HS	fpp =50MHz	-	15	15.5	ns
t _{OH}	Output hold time HS	fpp =50MHz	13	-	-	

1. Guaranteed by characterization results.

2. C_{LOAD} = 20 pF.

6.3.28 RTC characteristics

Table 102. RTC characteristics

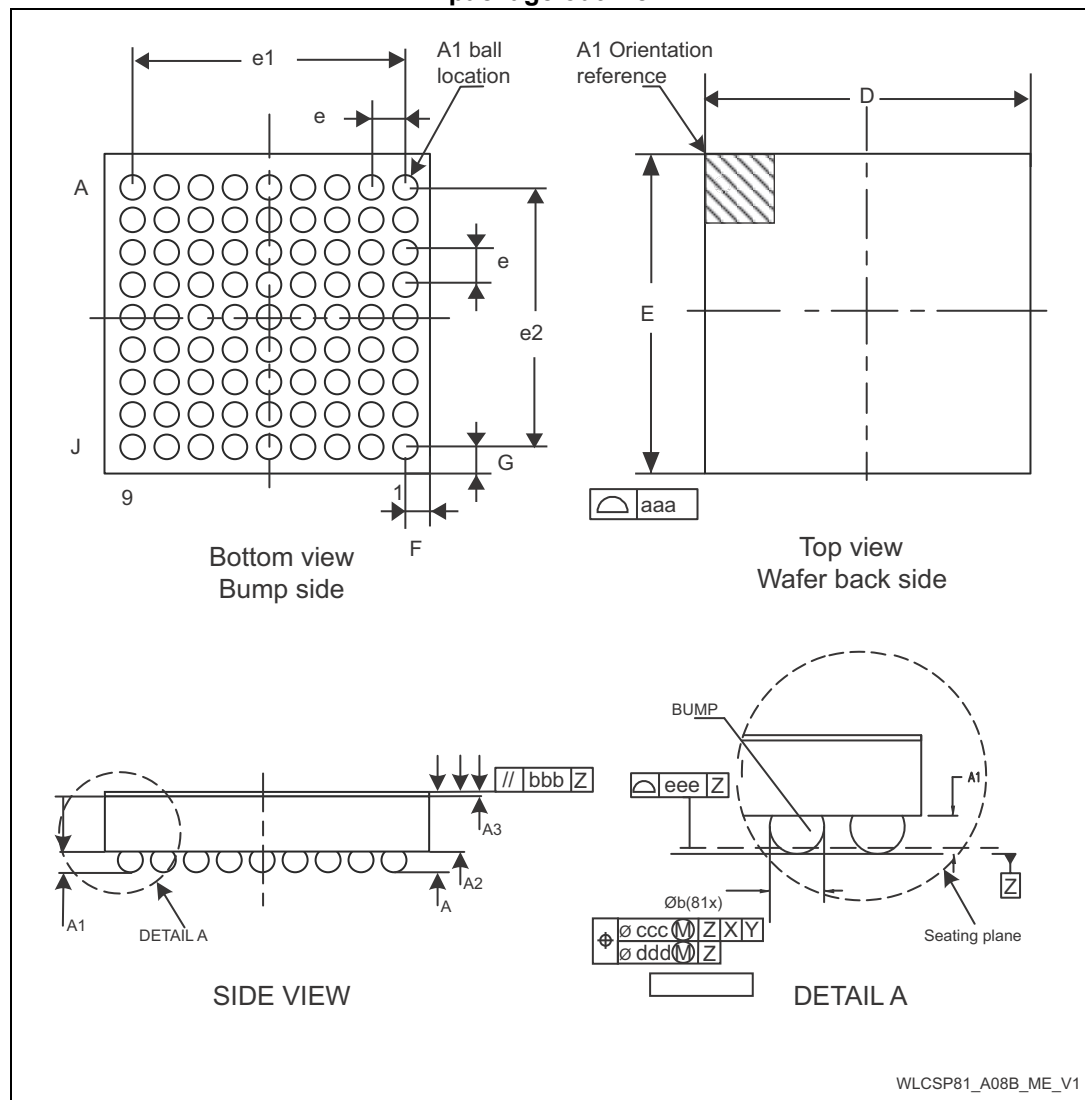
Symbol	Parameter	Conditions	Min	Max
-	$f_{PCLK1}/RTCCLK$ frequency ratio	Any read/write operation from/to an RTC register	4	-

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

7.1 WLCSP81 package information

Figure 63. WLCSP81 - 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 103. WLCSP81 - 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
Ø b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	4.004	4.039	4.074	0.1576	0.1590	0.1604
E	3.916	3.951	3.986	0.1542	0.1556	0.1569
e	-	0.400	-	-	0.0157	-
e1	-	3.200	-	-	0.1260	-
e2	-	3.200	-	-	0.1260	-
F	-	0.4195	-	-	0.0165	-
G	-	0.3755	-	-	0.0148	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 64. WLCSP81- 81-ball, 4.039 x 3.951 mm, 0.4 mm pitch wafer level chip scale package recommended footprint

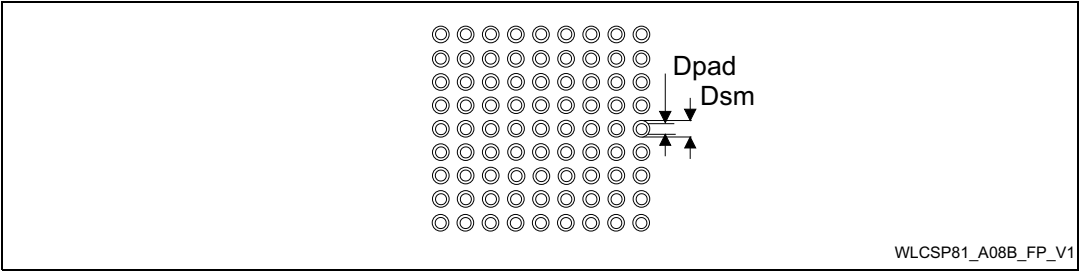


Table 104. WLCSP81 recommended PCB design rules (0.4 mm pitch)

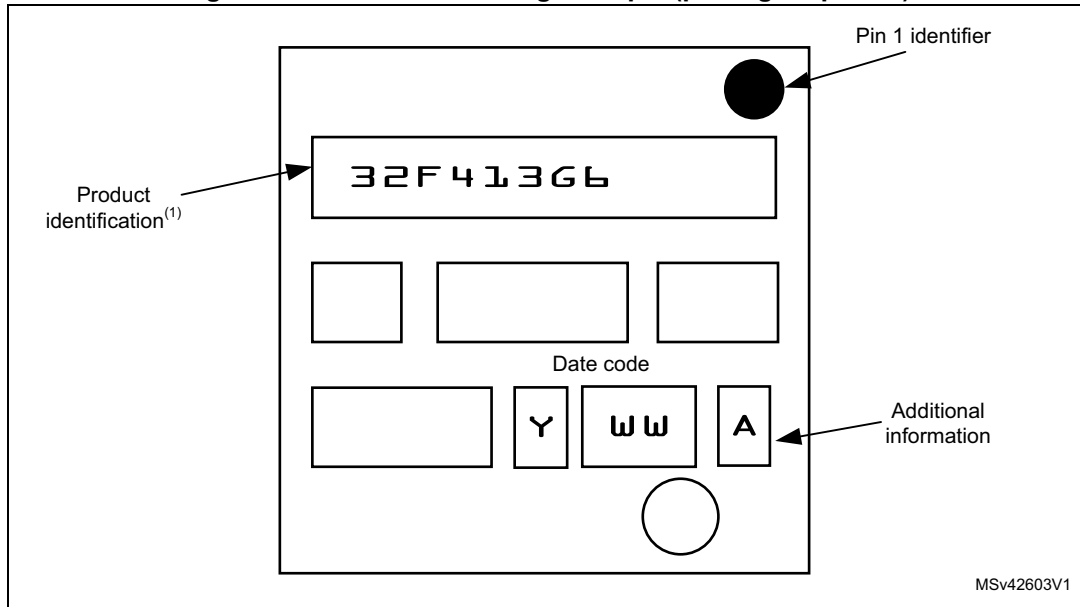
Dimension	Recommended values
Pitch	0.4 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Device marking for WLCSP81

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

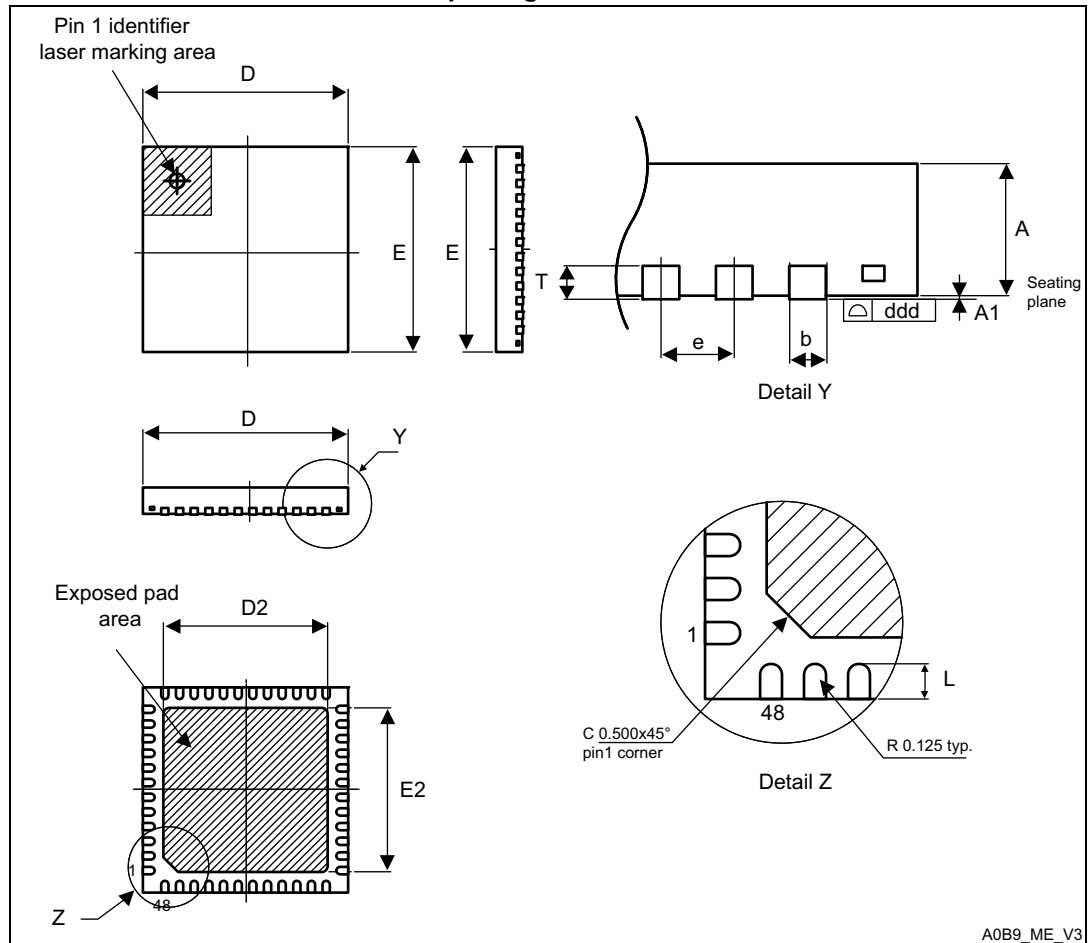
Figure 65. WLCSP81 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.2 UFQFPN48 package information

Figure 66. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline

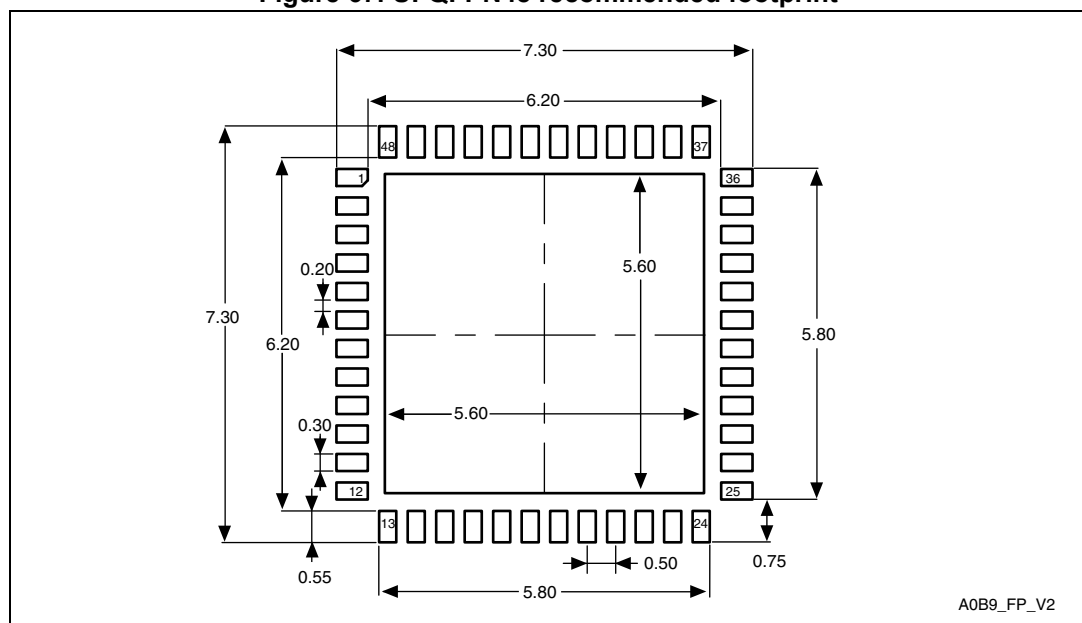


1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 105. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 67. UFQFPN48 recommended footprint

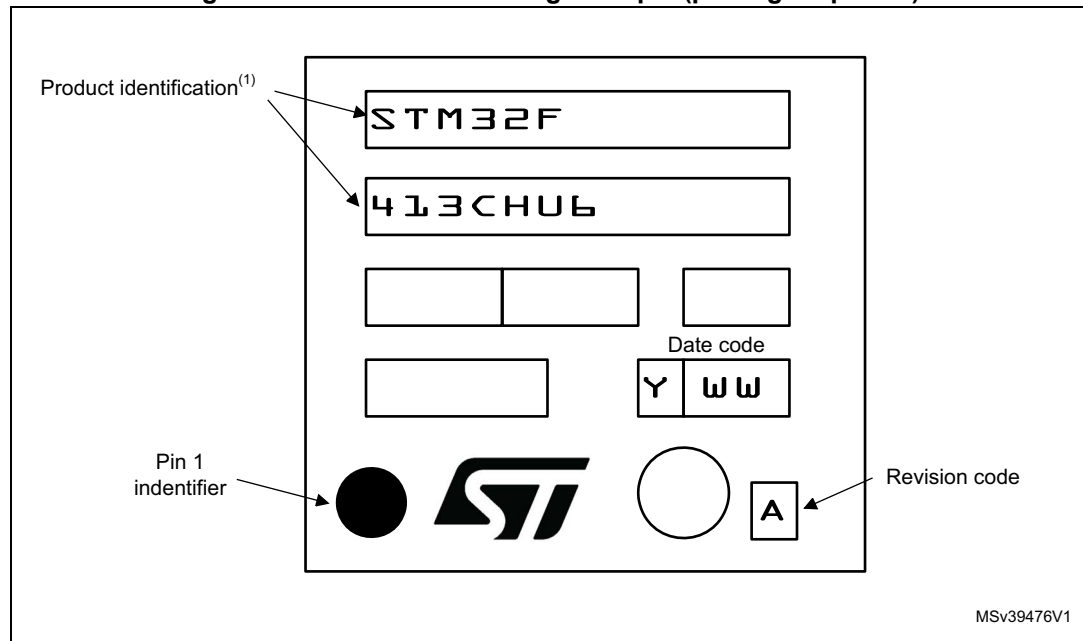
1. Dimensions are in millimeters.

Device marking for UFQFPN48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

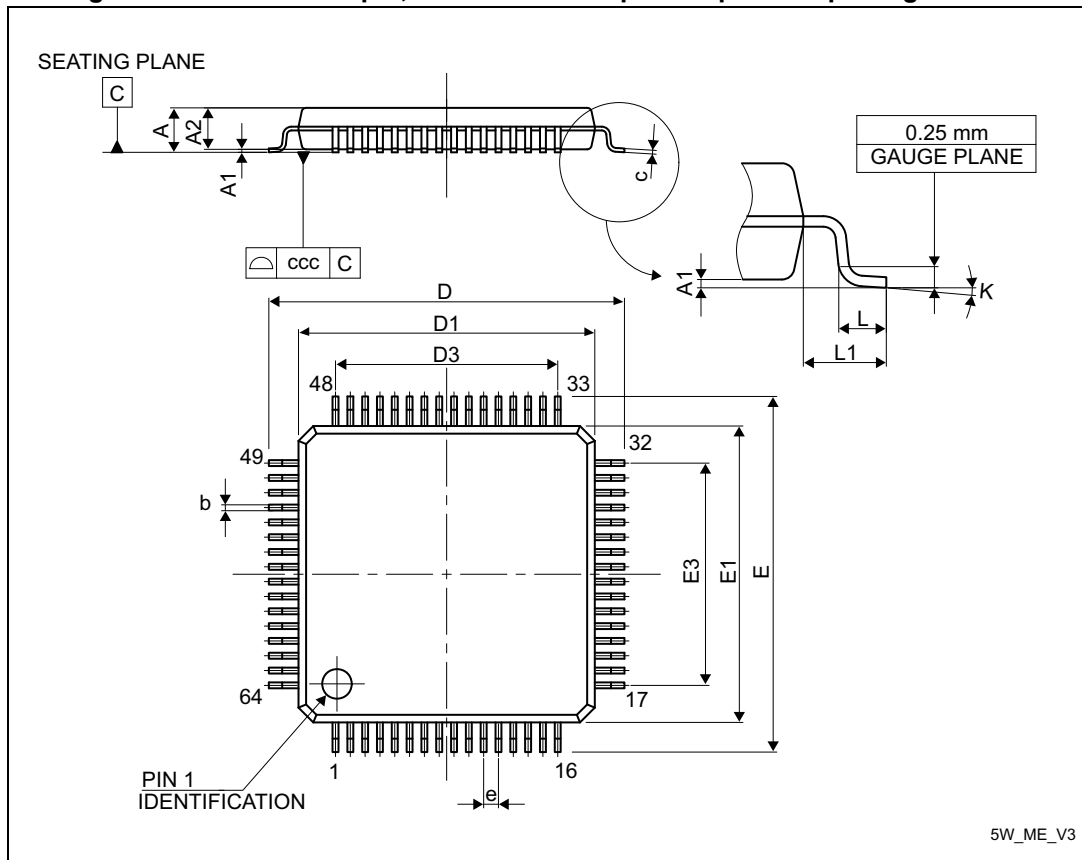
Figure 68. UFQFPN48 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.3 LQFP64 package information

Figure 69. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 106. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

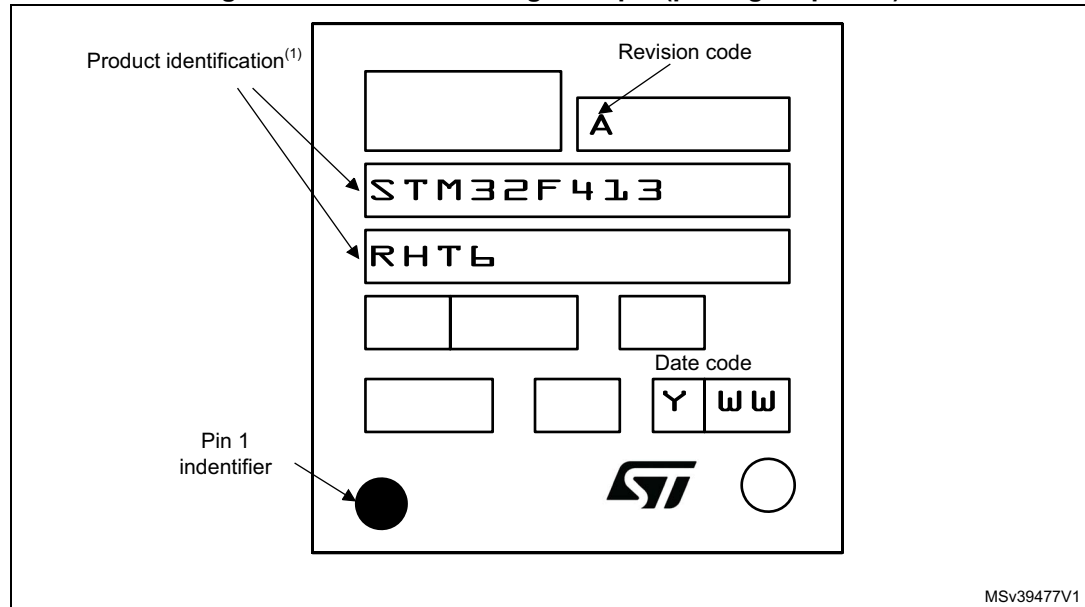
[illegible]

Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

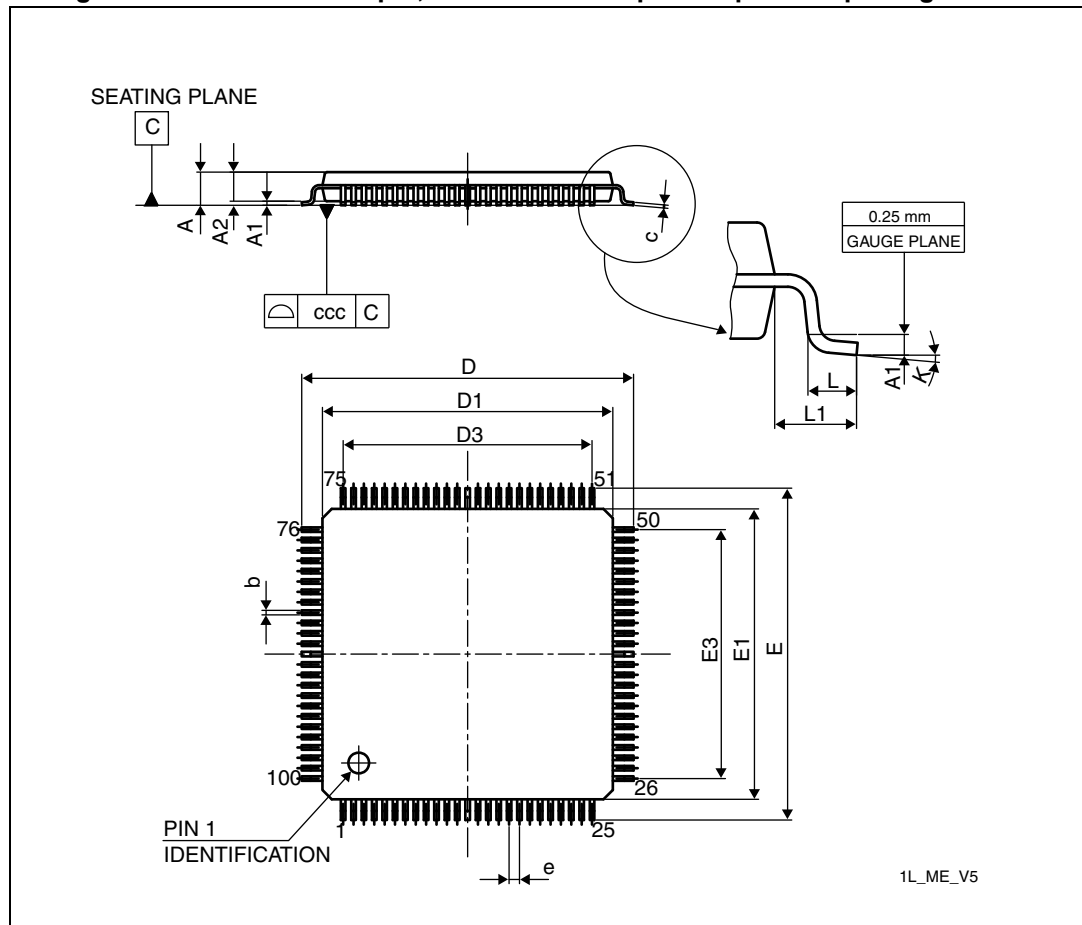
Figure 71. LQFP64 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.4 LQFP100 package information

Figure 72. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat package outline



1. Drawing is not to scale. Dimensions are in millimeters.

Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data

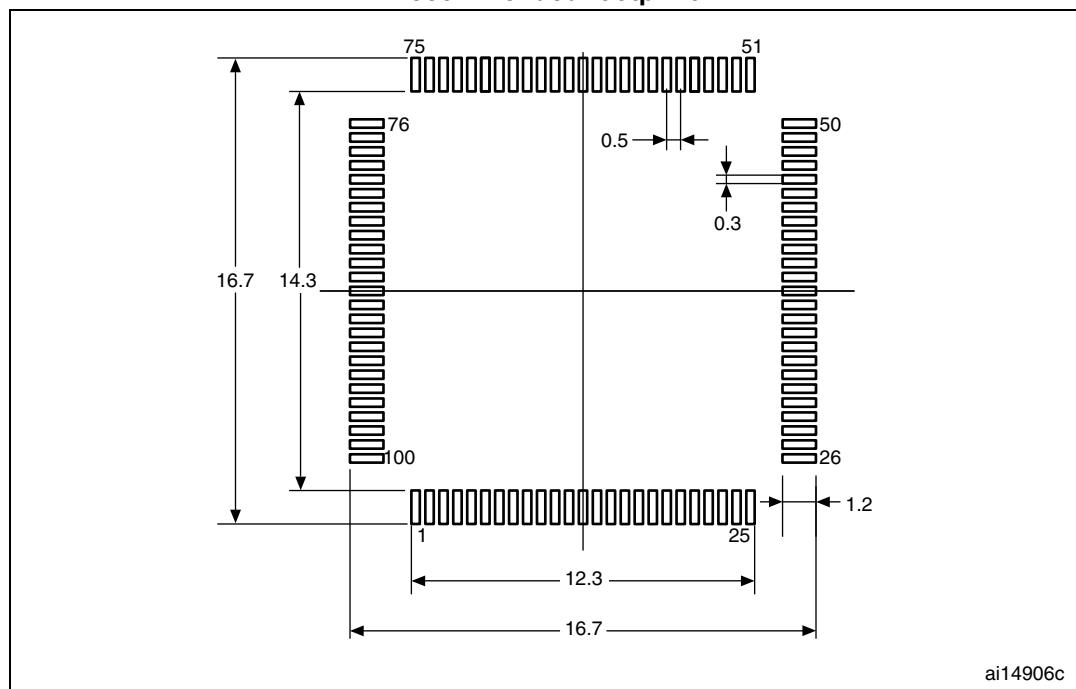
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378

Table 107. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 73. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint



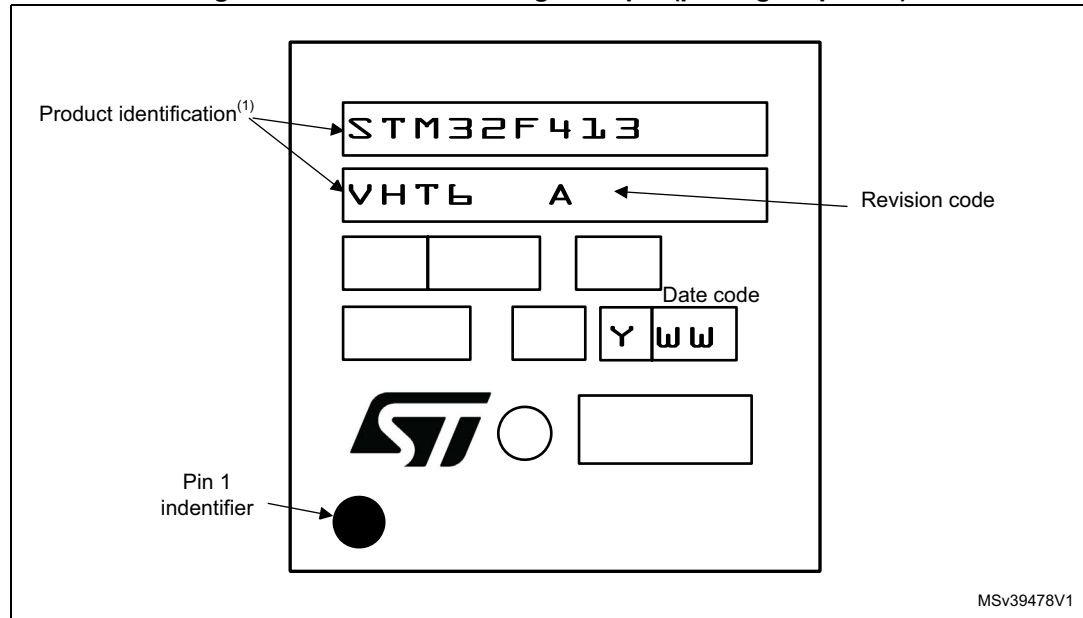
1. Dimensions are in millimeters.

Device marking for LQFP100

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

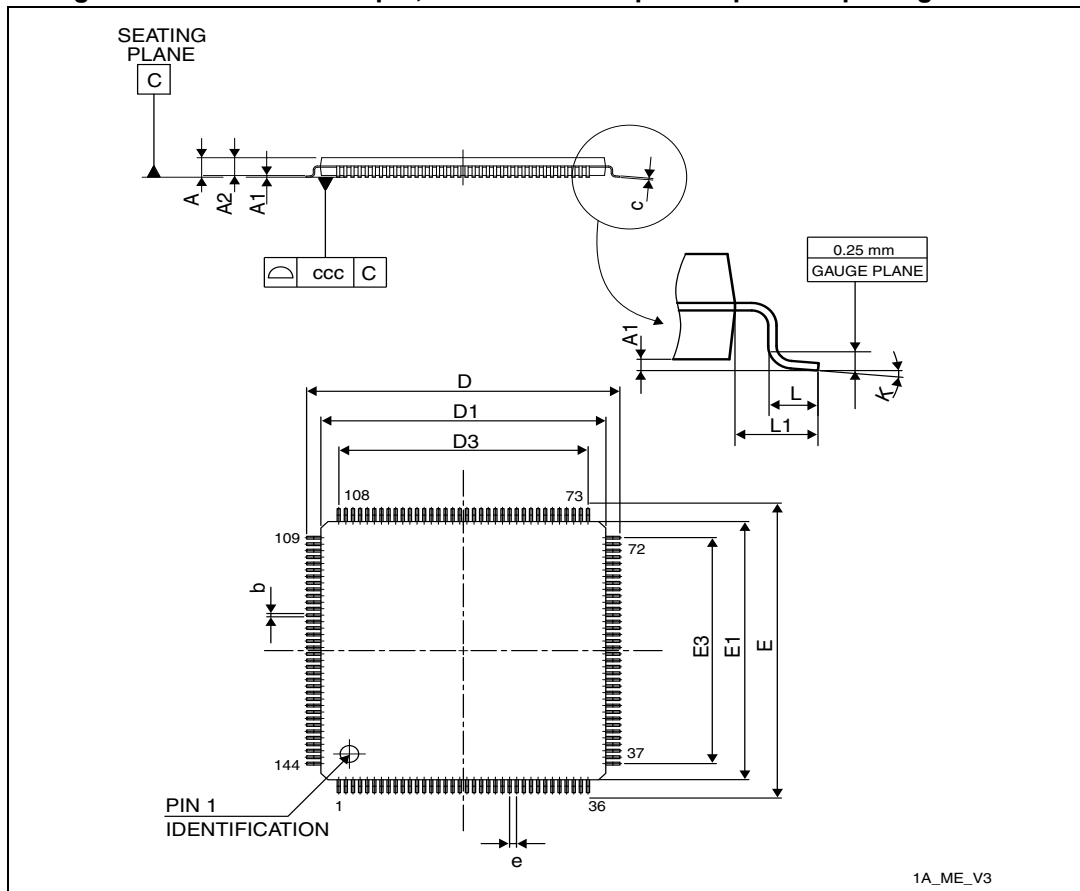
Figure 74. LQFP100 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.5 LQFP144 package information

Figure 75. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 108. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

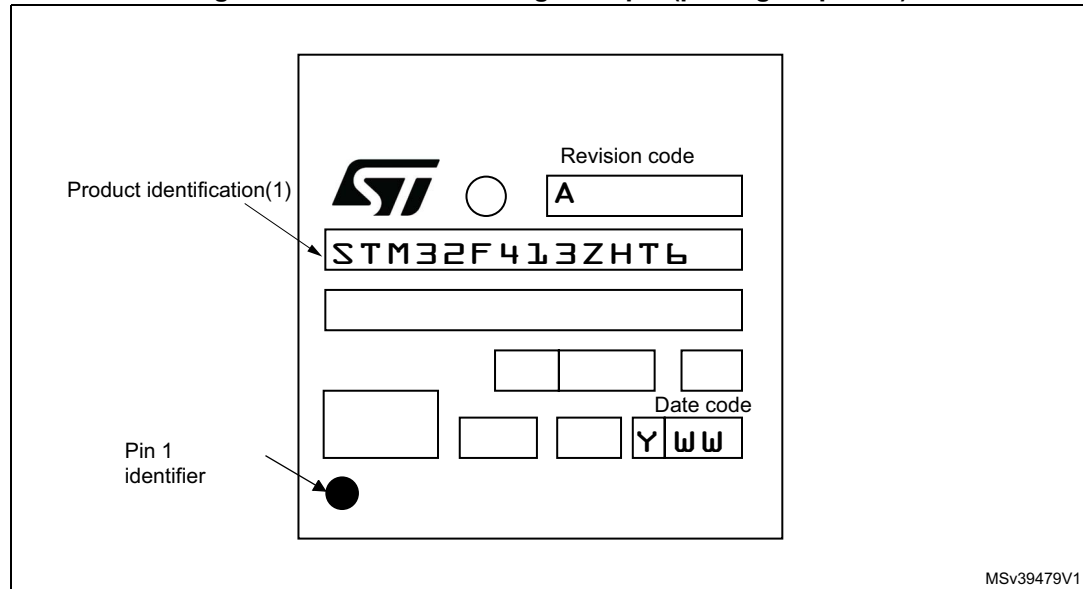
1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking for LQFP144

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

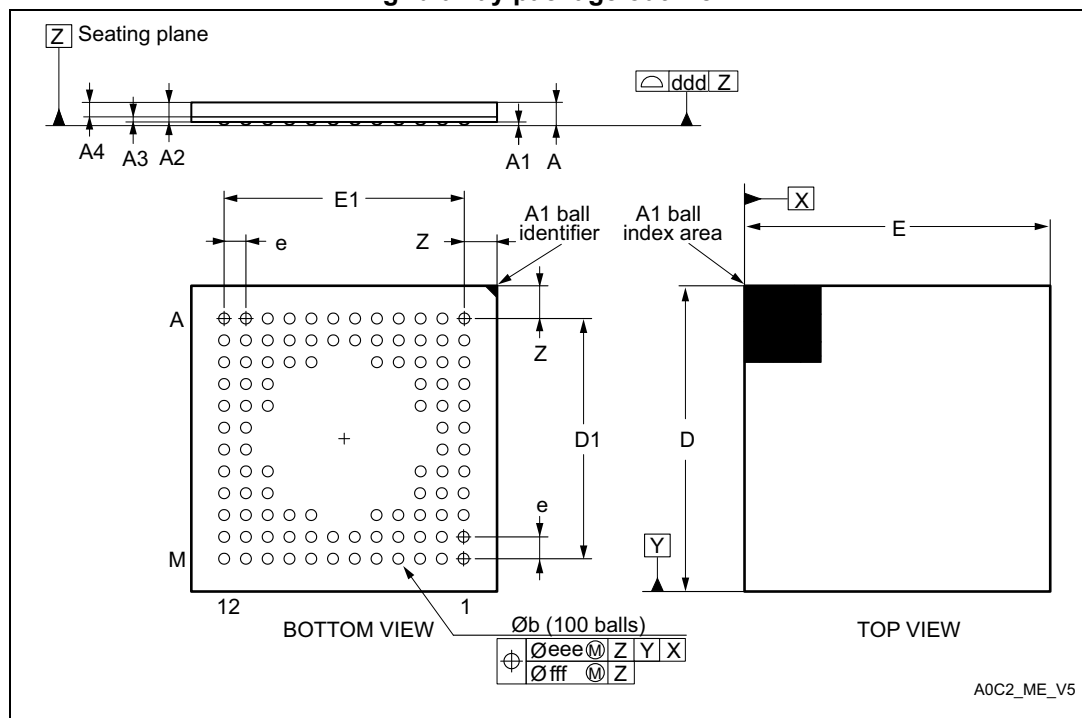
Figure 77. LQFP144 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.6 UFBGA100 package information

Figure 78. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 109. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	0.600	-	-	0.0236
A1	-	-	0.110	-	-	0.0043
A2	-	0.450	-	-	0.0177	-
A3	-	0.130	-	-	0.0051	0.0094
A4	-	0.320	-	-	0.0126	-
b	0.240	0.290	0.340	0.0094	0.0114	0.0134
D	6.850	7.000	7.150	0.2697	0.2756	0.2815
D1	-	5.500	-	-	0.2165	-
E	6.850	7.000	7.150	0.2697	0.2756	0.2815
E1	-	5.500	-	-	0.2165	-
e	-	0.500	-	-	0.0197	-
Z	-	0.750	-	-	0.0295	-

Table 109. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.080	-	-	0.0031
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 79. UFBGA100 - 100-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

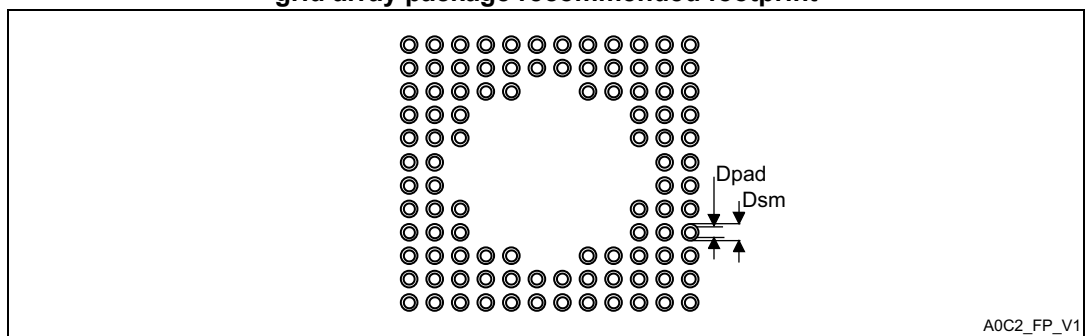


Table 110. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

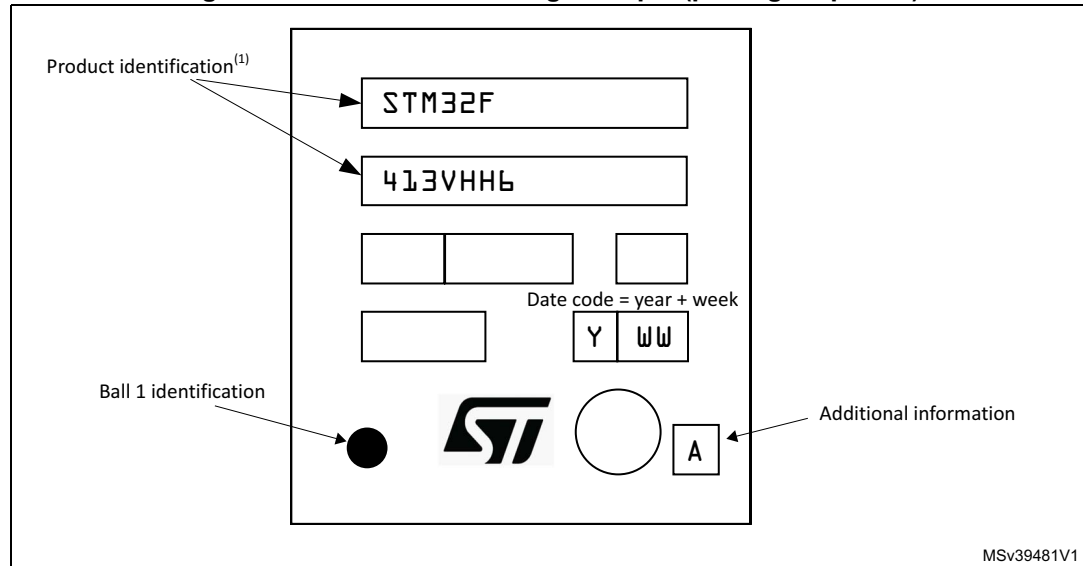
Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Device marking for UFBGA100

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

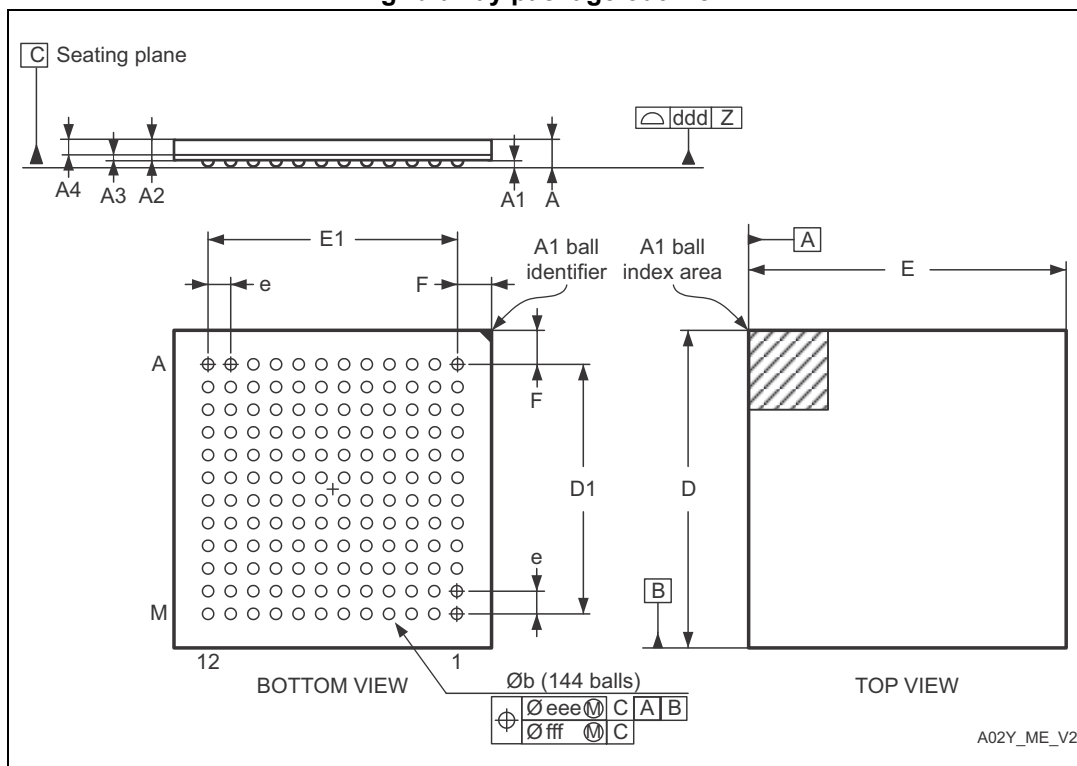
Figure 80. UFBGA100 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.7 UFBGA144 package information

Figure 81. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline



1. Drawing is not to scale.

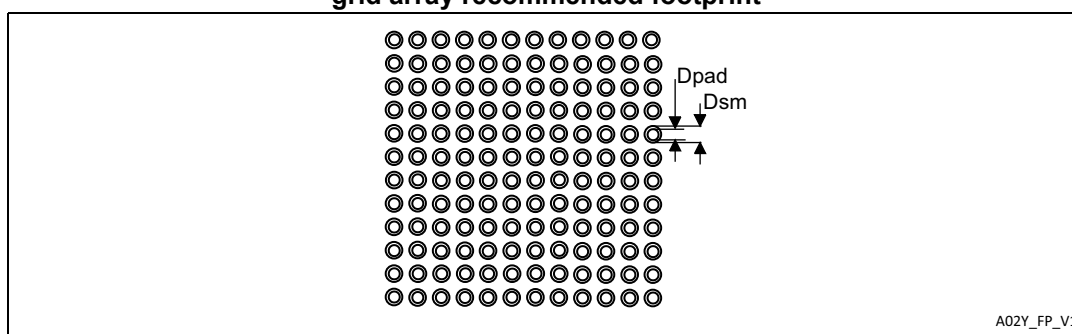
Table 111. UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.460	0.530	0.600	0.0181	0.0209	0.0236
A1	0.050	0.080	0.110	0.0020	0.0031	0.0043
A2	0.400	0.450	0.500	0.0157	0.0177	0.0197
A3	-	0.130	-	-	0.0051	-
A4	-	0.320	-	-	0.0126	-
b	0.360	0.400	0.440	0.0091	0.0110	0.0130
D	9.950	10.000	10.050	0.2736	0.2756	0.2776
D1	8.750	8.800	8.850	0.2343	0.2362	0.2382
E	9.950	10.000	10.050	0.2736	0.2756	0.2776
E1	8.750	8.800	8.850	0.2343	0.2362	0.2382
e	0.750	0.800	0.850	-	0.0197	-

Table 111. UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
F	0.550	0.600	0.650	0.0177	0.0197	0.0217
ddd	-	-	0.080	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 82. UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array recommended footprint**Table 112. UFBGA144 recommended PCB design rules (0.80 mm pitch BGA)**

Dimension	Recommended values
Pitch	0.80 mm
Dpad	0.400 mm
Dsm	0.550 mm typ. (depends on the soldermask registration tolerance)

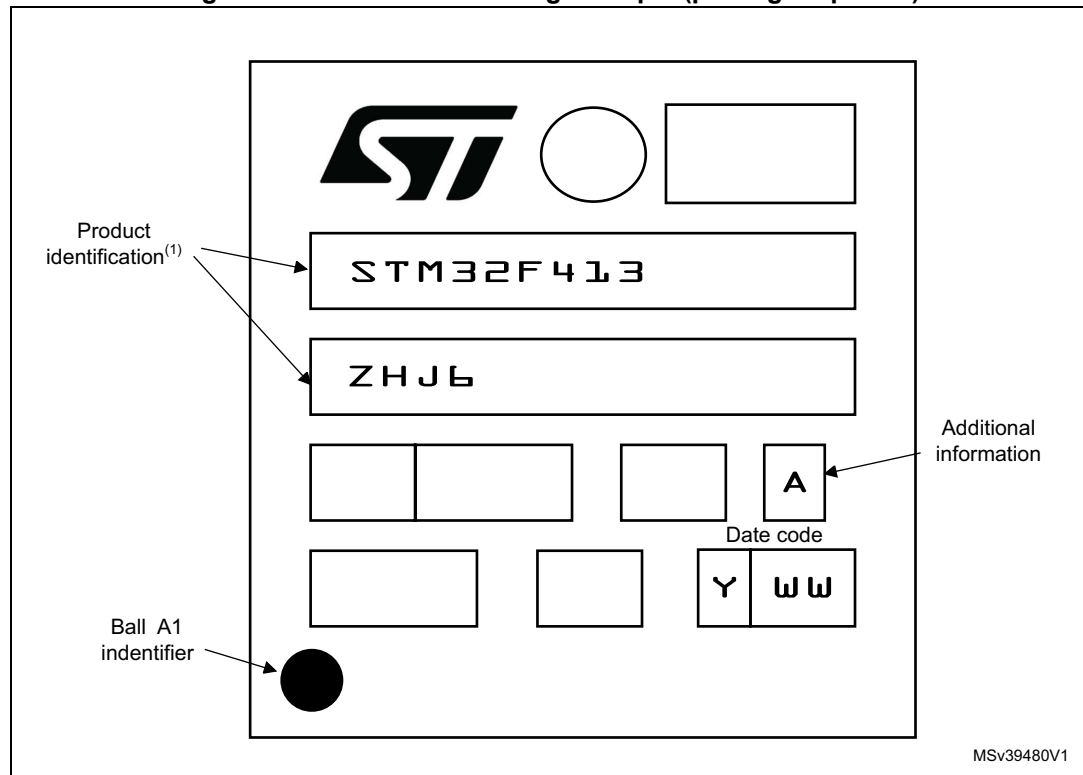
Note: *Non solder mask defined (NSMD) pads are recommended.
 4 to 6 mils solder paste screen printing process.
 Stencil opening is 0.400 mm.
 Stencil thickness is between 0.100 mm and 0.125 mm.
 Pad trace width is 0.120 mm.*

Device marking for UFBGA144

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 83. UFBGA144 marking example (package top view)



1. Parts marked as ES or E or accompanied by an Engineering Sample notification letter are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST's Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

7.8 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 17: General operating conditions](#).

The maximum chip-junction temperature, T_J max., in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (PD \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- PD max is the sum of P_{INT} max and $P_{I/O}$ max ($PD \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma (V_{DD} - V_{OH}) \times I_{OH},$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 113. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP144 - 20 x 20 mm	35	°C/W
	Thermal resistance junction-ambient LQFP100 - 14 x 14 mm	43	
	Thermal resistance junction-ambient LQFP64 - 10 x 10 mm	47	
	Thermal resistance junction-ambient UFBGA144 - 10 x 10 mm / 0.8 mm pitch	48	
	Thermal resistance junction-ambient UFBGA100 - 7 x 7 mm	57	
	Thermal resistance junction-ambient WLCSP81 - 4.039 x 3.951 mm	39.7	
	Thermal resistance junction-ambient UFQFPN48 - 7 x 7 mm	32	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

8 Ordering information

Table 114. Ordering information scheme

Example:	STM32	F	413	C	H	T	6	TR
Device family								
STM32 = Arm®-based 32-bit microcontroller								
Product type								
F = General-purpose								
Device subfamily								
413 = 413 line								
Pin count								
C = 48 pins								
R = 64 pins								
M = 81 pins								
V = 100 pins								
Z = 144 pins								
Flash memory size								
G = 1024 Kbytes of Flash memory								
H = 1536 Kbytes of Flash memory								
Package								
H = UFBGA 7 x 7 mm								
J = UFBGA 10 x 10 mm								
T = LQFP								
U = UFQFPN								
Y = WLCSP								
Temperature range								
6 = Industrial temperature range, – 40 to 85 °C								
3 = Industrial temperature range, – 40 to 125 °C								
Packing								
TR = tape and reel								
No character = tray or tube								

Appendix A Recommendations when using the internal reset OFF

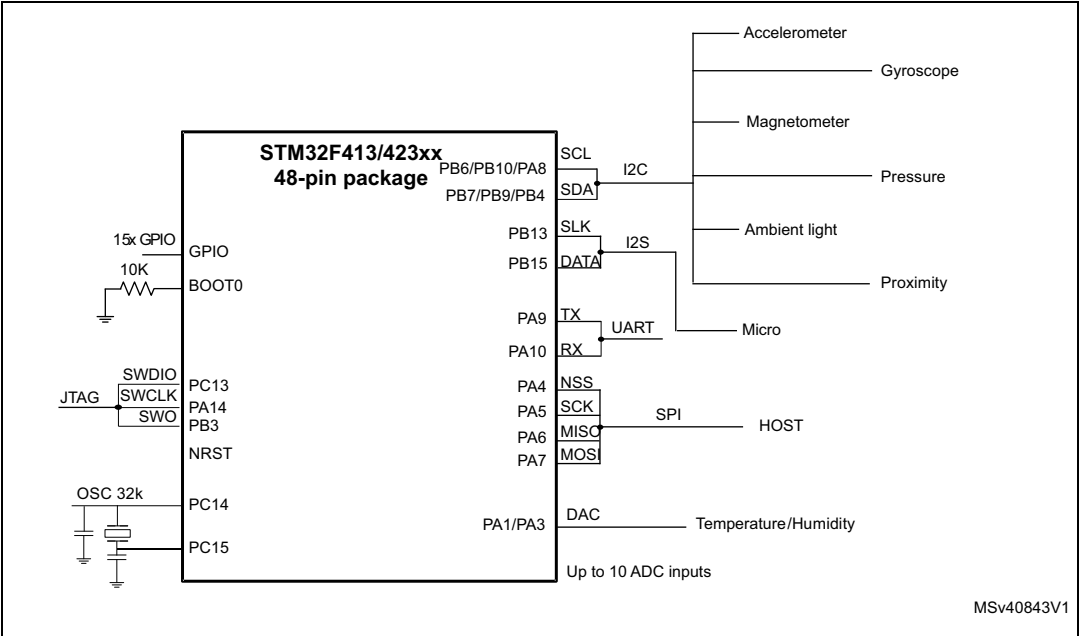
When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on-reset (POR)/power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled. By default BOR is OFF.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD} .

Appendix B Application block diagrams

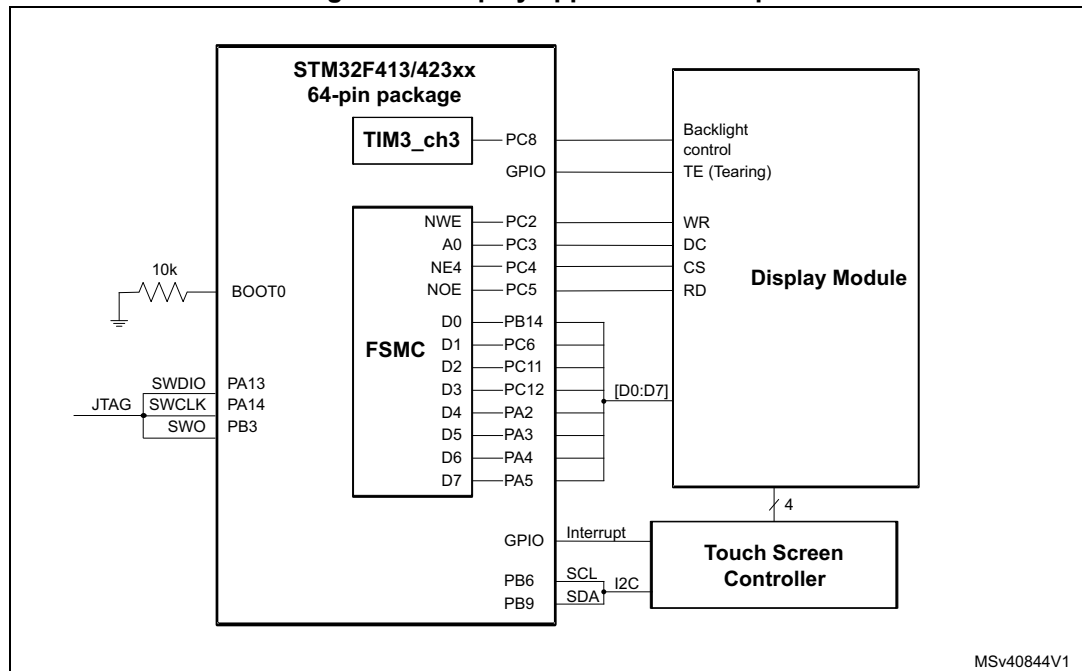
B.1 Sensor Hub application example

Figure 84. Sensor Hub application example



B.2 Display application example

Figure 85. Display application example

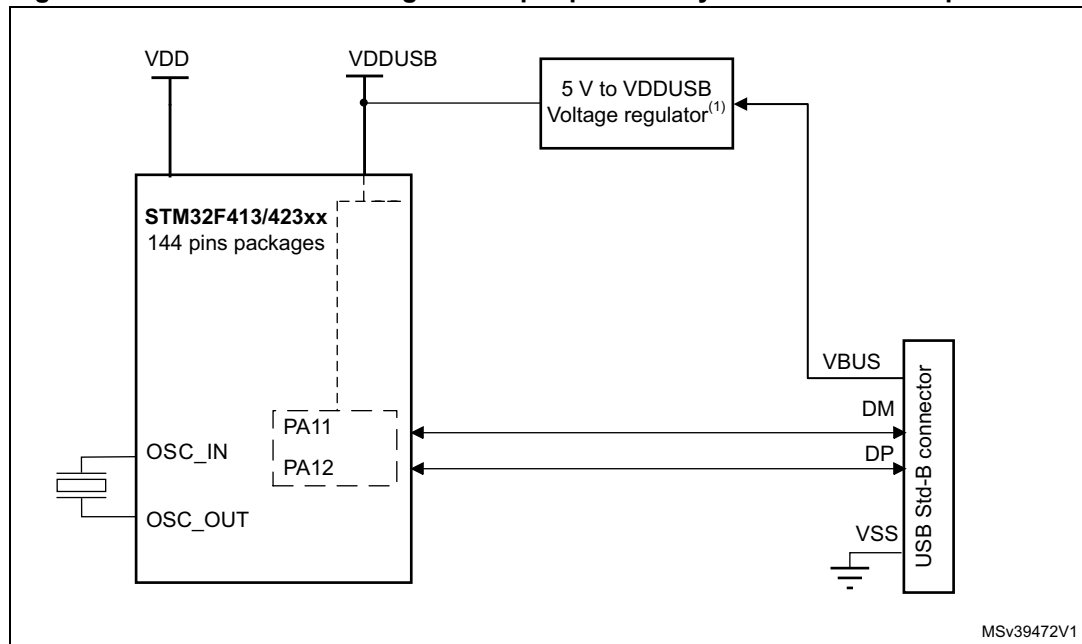


Note: 16 bit displays interfaces can be addressed with 100 and 144 pins packages.

MSv40843

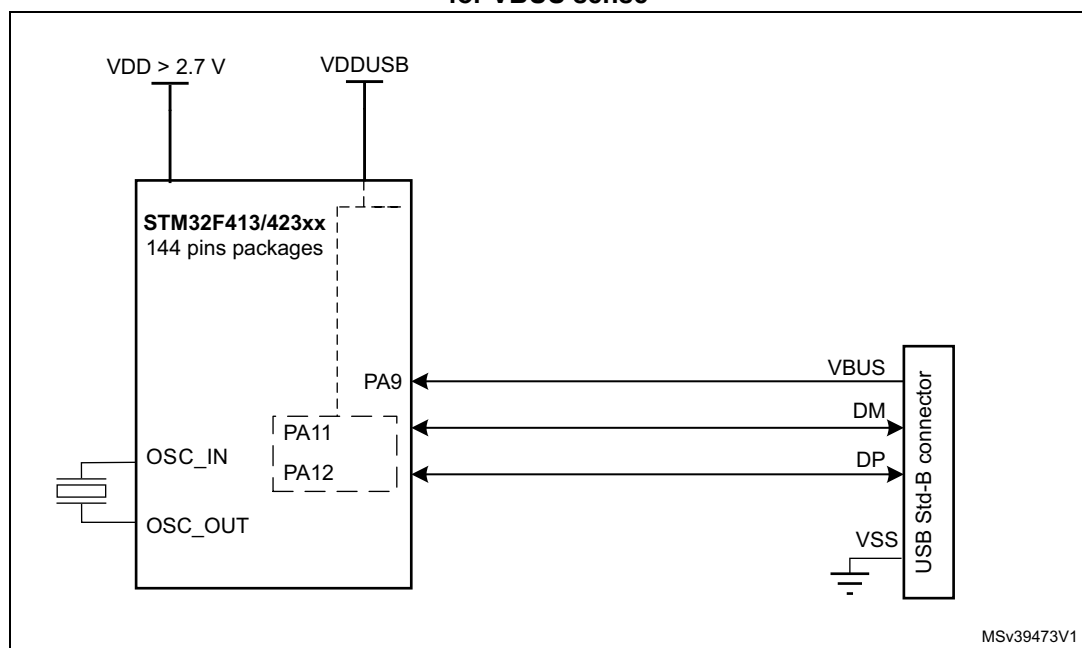
B.3 USB OTG full speed (FS) interface solutions

Figure 86. USB controller configured as peripheral-only and used in Full speed mode

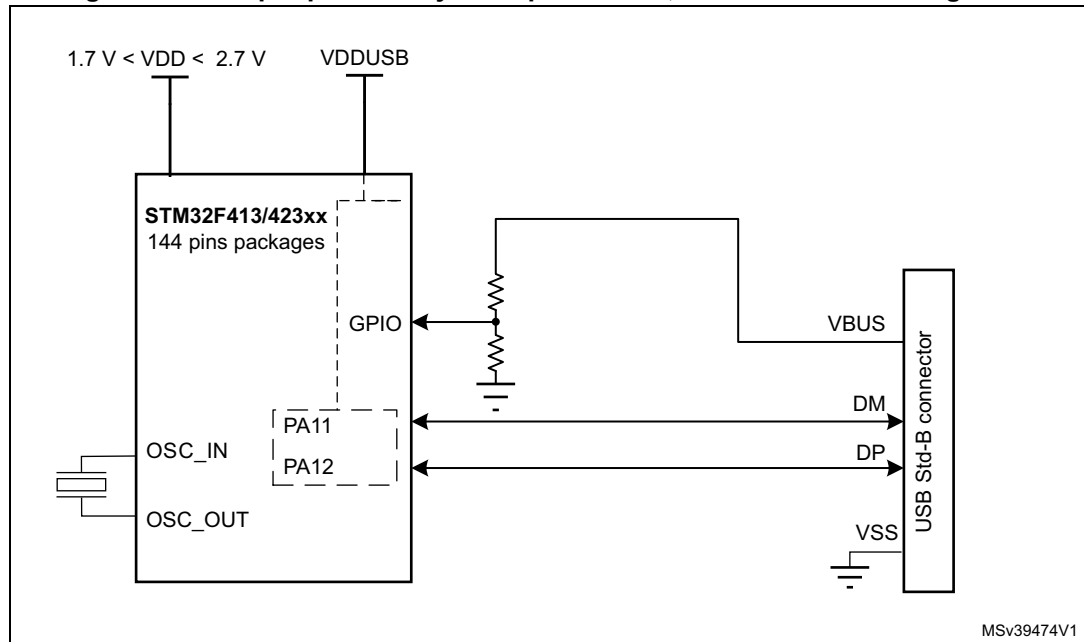


1. External voltage regulator only needed when building a V_{BUS} powered device.

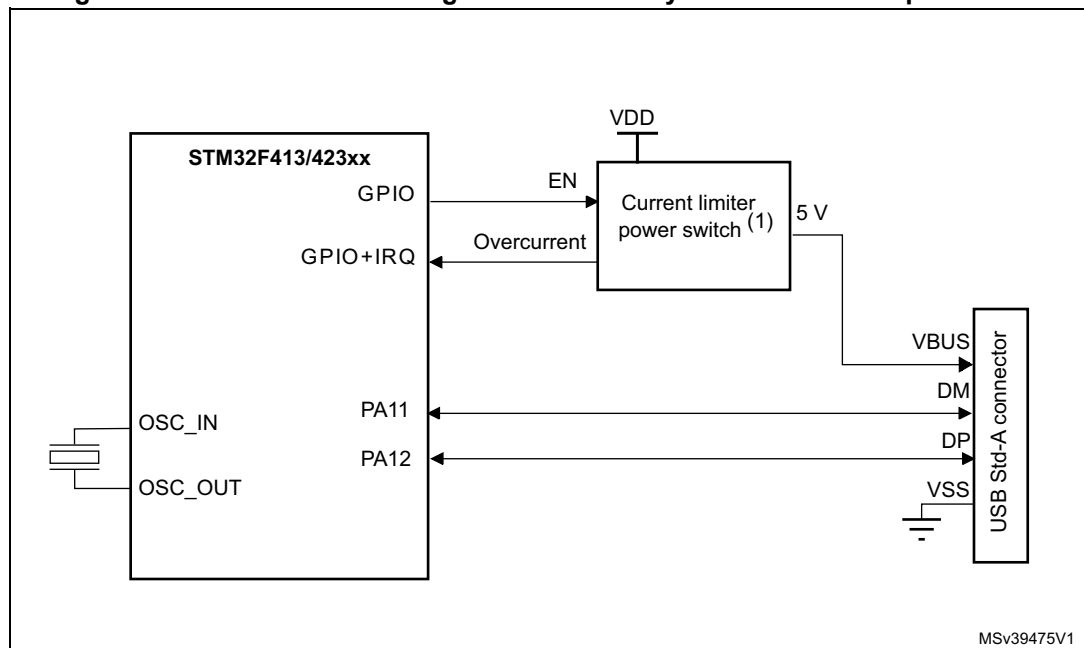
Figure 87. USB peripheral-only Full speed mode with direct connection for VBUS sense



1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 88. USB peripheral-only Full speed mode, VBUS detection using GPIO

1. External voltage regulator only needed when building a V_{BUS} powered device.

Figure 89. USB controller configured as host-only and used in full speed mode

2. The current limiter is required only if the application has to support a V_{BUS} powered device. A basic power switch can be used if 5 V are available on the application board.

Revision history

Table 115. Document revision history

Date	Revision	Changes
29-Aug-2016	1	Initial release.
21-Oct-2016	2	Updated: – Table 10: STM32F413xG/H pin definition – Section 7: Package information – Figure 65: WLCSP81 marking example (package top view)
13-Dec-2016	3	Updated: – Table 39: Peripheral current consumption – Table 55: EMI characteristics for LQFP144 – Table 56: ESD absolute maximum ratings – Table 70: QSPI dynamic characteristics in SDR mode – Table 111: UFBGA144 - 144-ball, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package mechanical data – Figure 81: UFBGA144 - 144-pin, 10 x 10 mm, 0.80 mm pitch, ultra fine pitch ball grid array package outline
09-Mar-2017	4	Updated: – Table 2: STM32F413xG/H features and peripheral counts – Table 12: STM32F413xG/H alternate functions Added: – Table 11: FSMC pin definition

Table 115. Document revision history

Date	Revision	Changes
14-Jun-2017	5	Added: – Section 4.1: WLCSP81 pinout description – Section 4.2: UFQFPN48 pinout description – Section 4.3: LQFP64 pinout description – Section 4.4: LQFP100 pinout description – Section 4.5: LQFP144 pinout description – Section 4.6: UFBGA100 pinout description – Section 4.7: UFBGA144 pinout description – Section 4.8: Pins definition – Section 4.9: Alternate functions Updated: – Table 10: STM32F413xG/H pin definition – Table 11: FSMC pin definition – Table 38: Switching output I/O current consumption – Table 39: Peripheral current consumption
19-Sep-2017	6	Updated: – Section 3.29: Digital filter for sigma-delta modulators (DFSDM) – Table 53: Flash memory endurance and data retention – Table 59: I/O static characteristics – Table 75: ADC characteristics

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