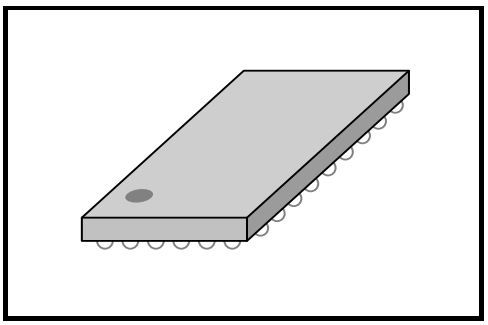
TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB6860WBG

Qi compliant wireless power receiver and charger IC

1. Outline

The TB6860WBG is Qi compliant wireless power receiver (Rx) IC. The TB6860WBG includes a bridge rectifier circuit, a modulation circuit, and a step-down DCDC converter. The wireless power system is constructed easily by combining with the TB6865FG which is a wireless power transmitter (Tx) IC. Charge mode and feed mode can be selected because the step-down DCDC converter has two operating modes. It expands usage flexibility.



S-WFBGA39-0305-0.40A01

2. Applications

Mobile devices (Smartphone, tablet), Battery pack, Mobile accessory etc.

3. Features

- Input voltage : PVDD2 = 3.4V to 12V
- Maximum output current : Step-down DCDC converter ... 1.2A
  3.3V-LDO output (VDD33) 60mA
- Synchronous rectification step-down DCDC converter : Selectable modes (feed mode or charge mode)
  Switching frequency 3MHz
- I^2C communication (Slave/Fast mode)
- WPC v1.0.3 compliant modulation
- Under voltage lockout (UVLO)
- Over voltage lockout(OVLO)
- Over current limit protection (OCL)
- Thermal shutdown protection (TSD)
- Package : WCSP (4.25mm×2.65mm)

This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

4. Block diagram

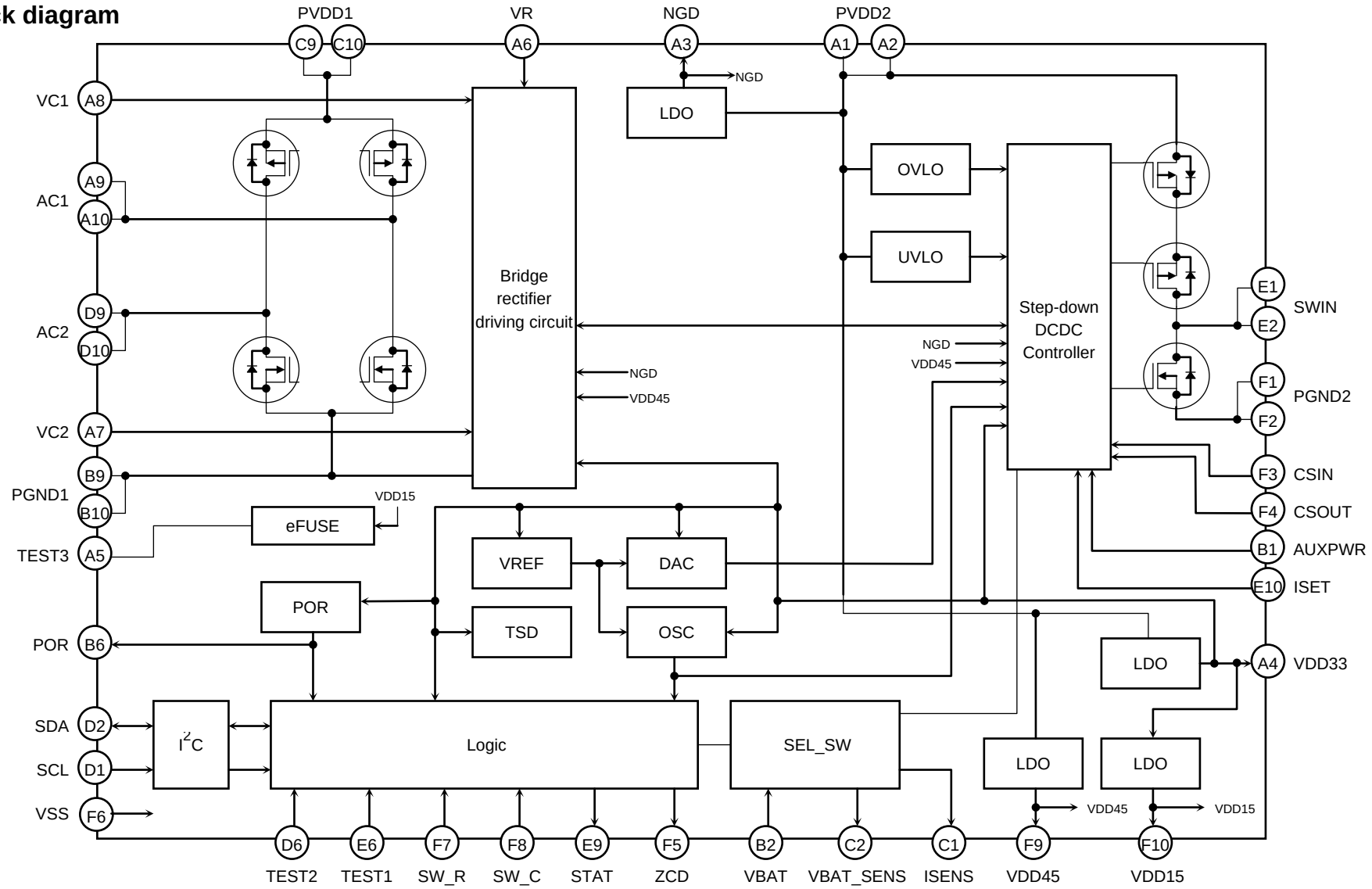


Figure 4.1 Block diagram

5. Pin Assignment

	A	B	C	D	E	F
10	AC1	PGND1	PVDD1	AC2	ISET	VDD15
9	AC1	PGND1	PVDD1	AC2	STAT	VDD45
8	VC1					SW_C
7	VC2					SW_R
6	VR	POR		TEST2	TEST1	VSS
5	TEST3					ZCD
4	VDD33					CSOUT
3	NGD					CSIN
2	PVDD2	VBAT	VBAT_SENS	SDA	SWIN	PGND2
1	PVDD2	AUXPWR	ISENS	SCL	SWIN	PGND2

(Top View)

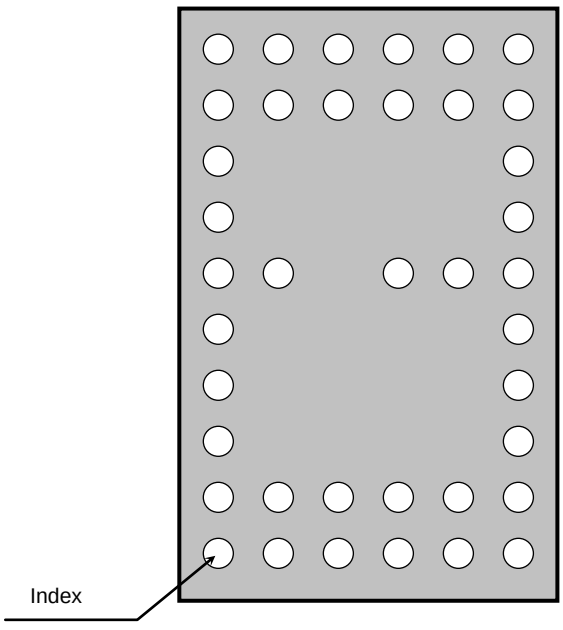


Figure 5.1 Pin Assignment

Note: The pin configuration figure is indicated that package ball side is located on the back and indicating pins from the surface view

6. Pin function

Table 6.1 Pin function

Pin Number	Pin symbol	I/O	Description
C9, C10	PVDD1	O	Bridge rectifier voltage output Connect smoothing ceramic capacitor between PVDD1 and GND. And connect PVDD1 with PVDD2.
A9, A10	AC1	I/O	Antenna terminals for receiver
D9, D10	AC2	I/O	
B9, B10	PGND1	-	Power ground 1 Connect to common ground (GND).
F5	ZCD	O	Test terminal 4 Keep open condition.
B6	POR	O	Power On Reset
D2	SDA	I/O	DATA terminal for I^2C (Note) Connect to pull-up resistor because it is an open drain terminal.
D1	SCL	I	CLK input terminal for I^2C (Note)
F6	VSS	-	Analog ground terminal Connect to common ground (GND)
E6	TEST1	I	Test terminal 1 Connect to GND
D6	TEST2	I	Test terminal 2 Connect to GND
A5	TEST3	I	Test terminal 3 Connect to VDD33
F7	SW_R	I	Input terminal for resistance load ASK modulation control This terminal is available by setting internal resister. When it's not in use, connect to GND.
F8	SW_C	I	Input terminal for capacitive load ASK modulation control This terminal is available by setting internal resister. When it's not in use, connect to GND.
E9	STAT	O	Status signal output terminal STAT="L" : Step-down DCDC converter is on. STAT="H" : Step-down DCDC converter is off.
C2	VBAT_SENS	O	Monitor terminal for battery voltage One third of VBAT input voltage is output.
C1	ISENS	O	Monitor terminal for output current It's possible to monitor following three kinds of voltages by setting internal resister. 1) Output current voltage 2) The voltage of VBAT×1/3 (VBAT_SENS output) 3) The voltage of PVDD2×1/8.
A8	VC1	O	Capacitor connection terminal 1 for capacitive load ASK modulation This terminal is open drain. When using this function, connect capacitor between VC1 and AC1. When it's not in use, connect to GNO or keep open condition.
A7	VC2	O	Capacitor connection terminal 2 for capacitive load ASK modulation This terminal is open drain. When using this function, connect capacitor between VC2 and AC2. When it's not in use, connect to GNO or keep open condition.

Note: The SDA and SCL pins have ESD protection diodes to VDD33.
TB6862WBG cannot share the I^2C bus with other peripheral IC.

Table 6.2 Pin function

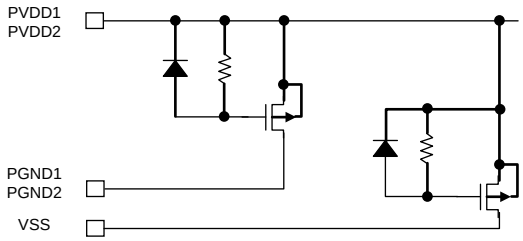
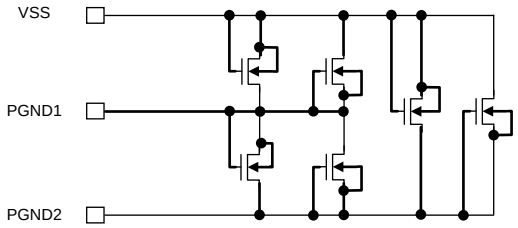
Pin Number	Pin symbol	I/O	Description
A1, A2	PVDD2	-	Power supply terminal This terminal supplies power to internal LDOs and step-down DCDC converter. Connect capacitor between PVDD2 and GND.
E1, E2	SWIN	O	Step-down DCDC converter output terminal Connect inductor between SWIN and CSIN.
F1, F2	PGND2	-	Power ground 2 Connect to common ground (GND).
F3	CSIN	I	Current sense input terminal (+) Connect resistor for current detection of 68mΩ between CSIN and CSOUT.
F4	CSOUT	I	Current sense input terminal (-) Connect resistor for current detection of 68mΩ between CSIN and CSOUT.
B1	AUXPWR	I	Voltage feedback input
F9	VDD45	O	4.5V-LDO output terminal for internal circuit It is impossible to supply power to external parts. Connect capacitor between VDD45 and GND.
A4	VDD33	O	3.3V-LDO output terminal Connect capacitor between VDD33 and GND.
F10	VDD15	O	1.5V-LDO output terminal for internal circuit. It is impossible to supply power to external parts. Connect capacitor between VDD15 and GND.
A3	NGD	O	PVDD2-4.5V output terminal for internal circuit. It is impossible to supply power to external parts. Connect capacitor between NGD and PVDD2.
B2	VBAT	I	Battery voltage input terminal In charge mode, input output voltage of external battery.
E10	ISET	I	Test terminal 5 Connect to GND
A6	VR	O	Resistor connect terminal for resistance load ASK modulation control This terminal is open drain terminal. When using this function, connect resistor between VR and PVDD1. When it’s not in use, connect to GNO or keep open condition.

7. Equivalent circuits for input/output/power supply terminals

7.1 Power supply terminal

Table 7.1 Equivalent circuits for power supply terminals

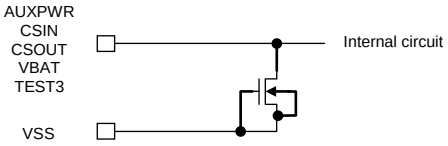
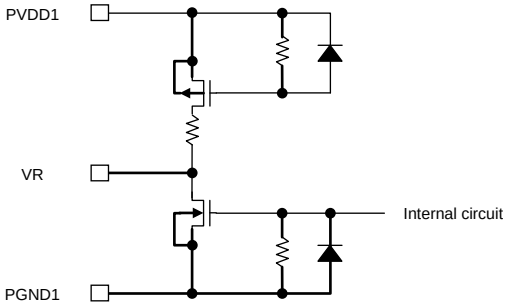
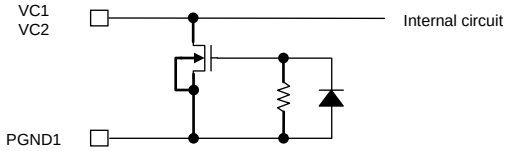
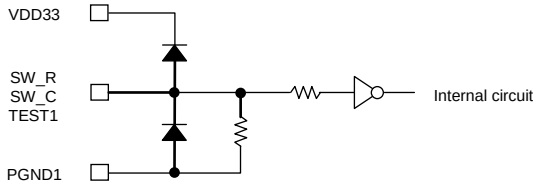
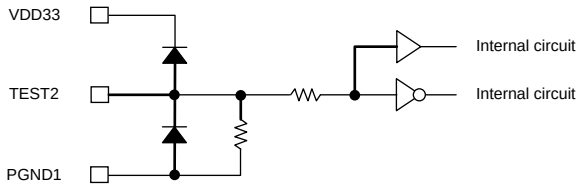
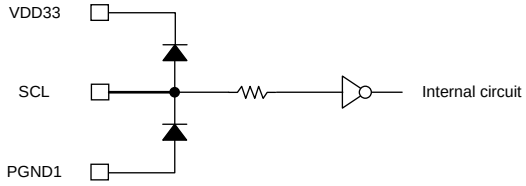
Note: Equivalent circuits may be simplified to illustrate circuits.

Pin name	Equivalent circuit
PVDD1/2-PGND1/2 PVDD1/2-VSS	
VSS-PGND1/2 PGND1-PGND2	

7.2 Input terminal

Table 7.2 Equivalent circuits for input terminals

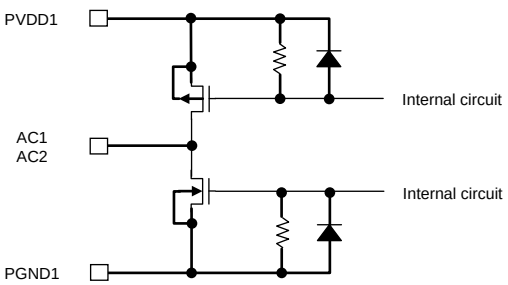
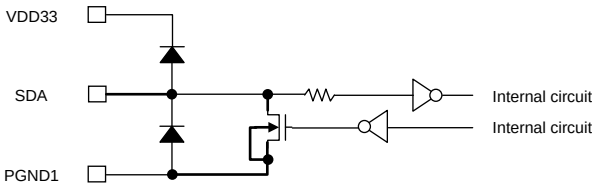
Note: Equivalent circuits may be simplified to illustrate circuits.

Pin name	Equivalent circuit
AUXPWR CSIN CSOUT VBAT TEST3	
VR	
VC1 VC2	
SW_R SW_C TEST1	
TEST2	
SCL	

7.3 Input/output terminal

Table 7.3 Equivalent circuits for Input/output terminals

Note: Equivalent circuits may be simplified to illustrate circuits.

Pin name	Equivalent circuit
AC1 AC2	
SDA	

7.4 Output terminal

Table 7.4 Equivalent circuits for output terminals

Note: Equivalent circuits may be simplified to illustrate circuits.

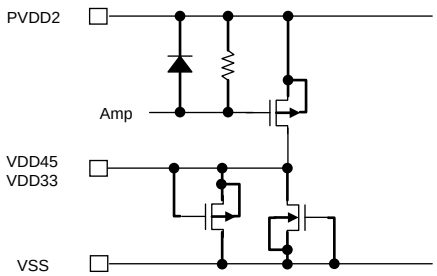
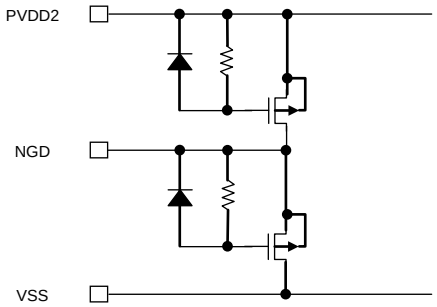
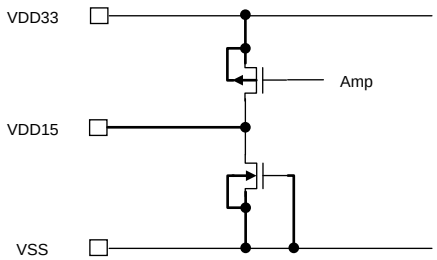
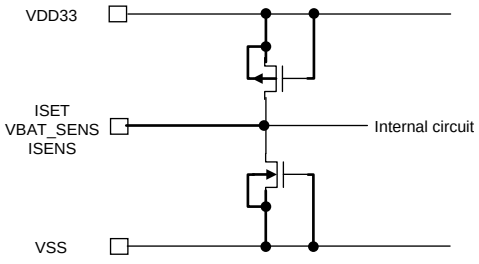
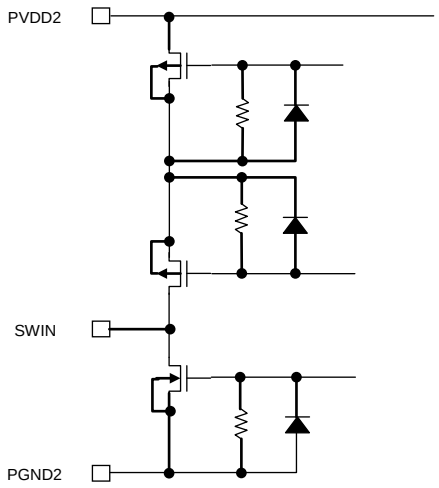
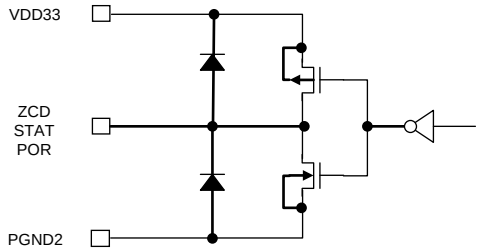
Pin name	Equivalent circuit
VDD45 VDD33	
NGD	
VDD15	
ISET VBAT_SENS ISENS	

Table 7.5 Equivalent circuits for output terminals

Note: Equivalent circuits may be simplified to illustrate circuits.

Pin name	Equivalent circuit
SWIN	
ZCD STAT POR	

8. Function

The TB6860WBG is Qi compliant wireless power receiver (Rx) IC. Qi compliant wireless power system transfers power by adjoining coils of transmitter (Tx) and receiver (Rx). The TB6860WBG includes a bridge rectifier circuit which rectifies AC power received by a coil (Rx), a modulation circuit for communicating from Rx to Tx side, and a step-down DCDC converter for supplying power to the load. The step-down DCDC converter makes possible to operate the driver in two modes of charge mode and feed mode. Select the operating mode depending on the method of power feed to the system. Construction of the circuit when the TB6860WBG charges battery directly (charge mode) is shown in Figure 8.1. And the Figure 8.2 indicates the construction of the circuit when the TB6860WBG feeds power to the battery charging circuit (feed mode). It is possible to feed power to the load with high efficiency by adopting step-down DCDC converter.

(1) Charging the battery directly

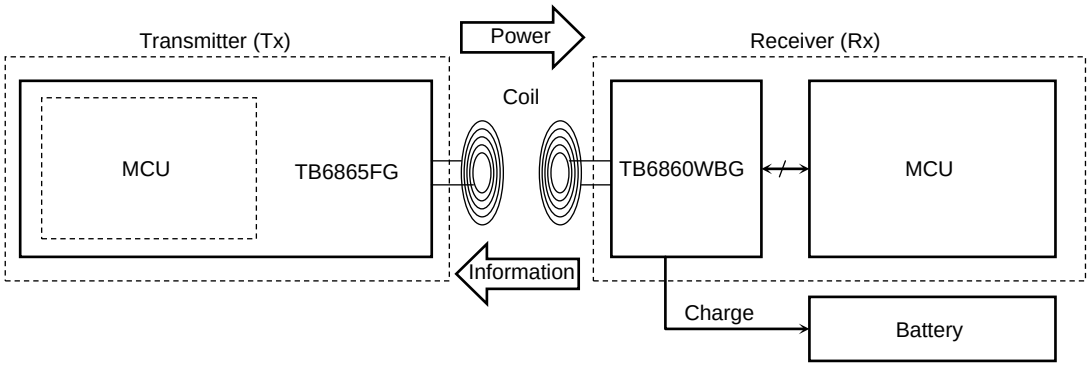


Figure 8.1 Charge mode

(2) Charging the battery through feeding power to the external PMIC

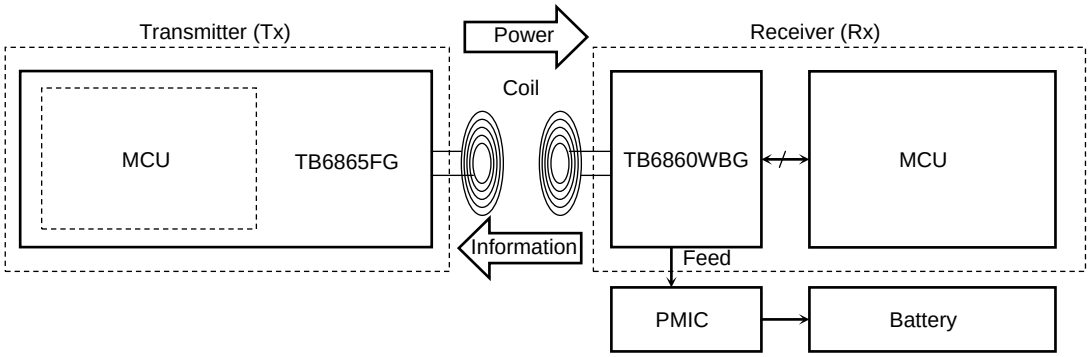


Figure 8.2 Feed mode

Communication from Rx to Tx is necessary to construct wireless feed system. Rx should monitor receiving power and return communication signal according to Qi standard. The TB6860WBG includes a modulation circuit and a power circuit (VDD33) which drives MCU. The communication signal between Rx and Tx should be input from MCU to the TB6860WBG. And it should be controlled by I^2C interface to enable each function which is fed power from the TB6860WBG. Construct the system by combining the MCU which includes AD converter, I^2C interface, and GPIO. Connecting description is shown in the Figure 8.3.

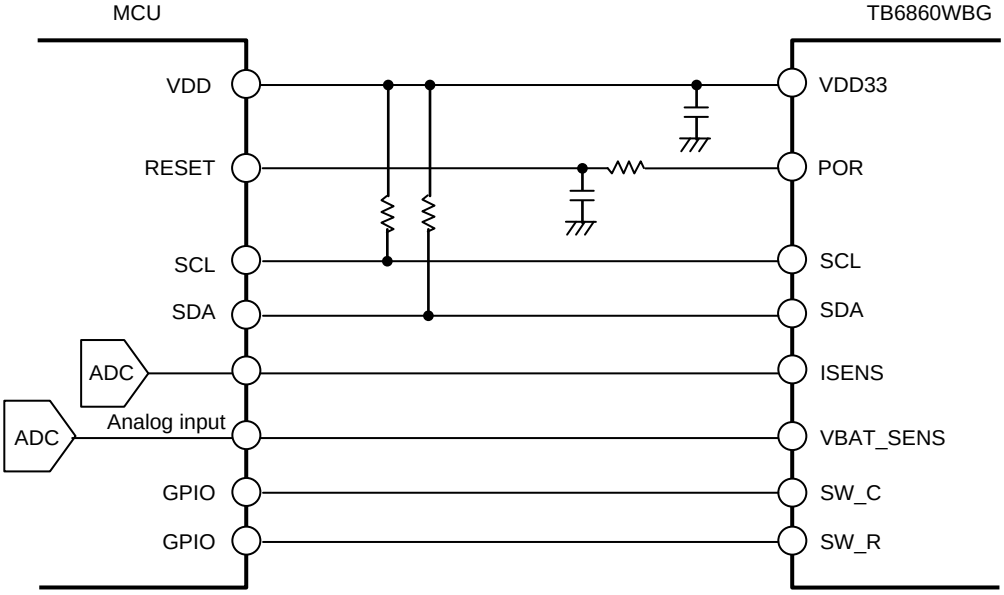


Figure 8.3 Example of connection with MCU

The TB6860WBG drives modulated operation, which is necessary to communicate between Rx and Tx by inputting data to SW_C terminal or SW_R terminal from MCU. The TB6860WBG supports two ASK modulations of capacitive load and resistance load. In case of ASK modulation by capacitive load, connect the capacitor to VC1 and VC2 terminals and input data to SW_C terminal. In case of ASK modulation by resistance load, connect the resistor between VR terminal and PVDD1 terminal and input data to SW_R terminal. It is possible to drive modulated operation without inputting data to SW_C terminal and SW_R terminal by using I^2C interface. In this case, EN_CAP register and EN_RES register are re-written by I^2C interface.

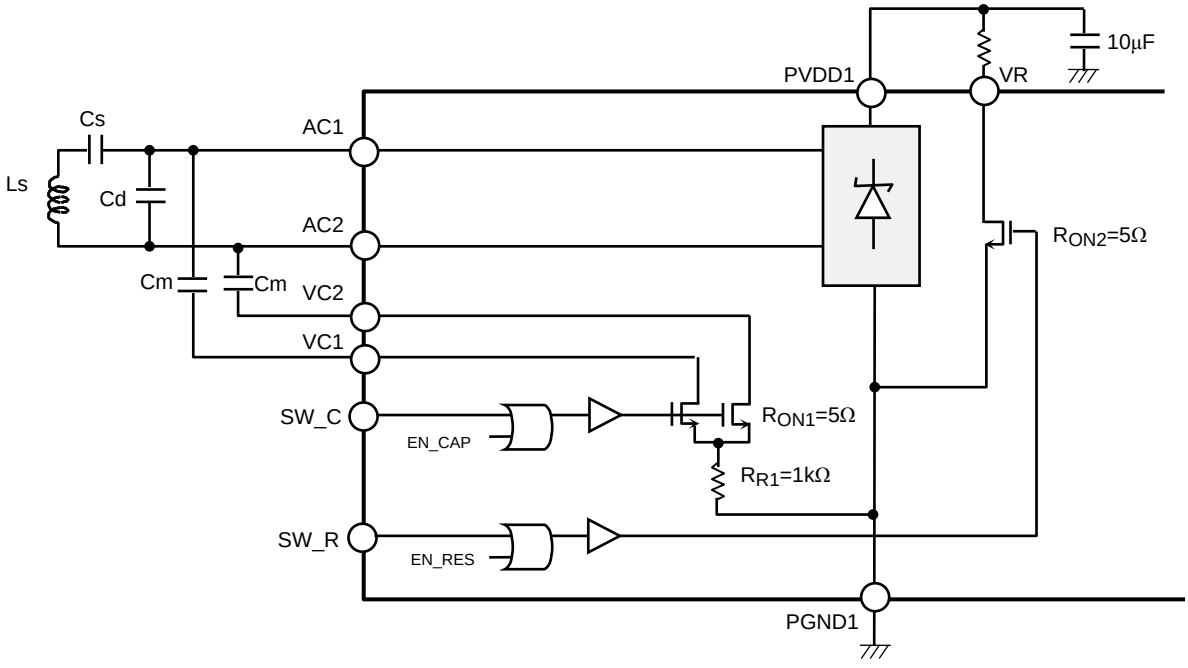


Figure 8.4 Example of modulation connection of capacitive load and resistance load

8.1 Step-down DCDC converter charge/feed mode

Step-down DCDC converter operates with switching frequency of 3MHz (typ.). Step-down DCDC converter has two operation modes of charge mode and feed mode. Operation mode is configured by CH_DC register. Step-down DCDC converter is turned on and off by EN_DCDC register. When step-down DCDC converter turns on, STAT outputs ”L”, and when it turns off, STAT outputs ”H”.

8.1.1 Waiting mode

When EN_DCDC is set ”0”, the step-down DCDC converter is turned off and the operation moves to waiting mode. When EN_DCDC is set ”1”, the step-down DCDC converter starts operation with charge mode or feed mode according to the CH_DC register set. Make sure to configure the related registers before turning on the step-down DCDC converter. EN_DCDC register is rewritten to ”0” automatically and the operation moves to the waiting mode in following two cases; operation of the step-down DCDC converter stops by protection circuits and charging is completed in the charge mode.

8.1.2 Charge mode

It is possible to charge the battery directly by setting CH_DC ”0” and operates the step-down DCDC converter in charge mode. Charge mode has the constant current (CC) charge modes (trickle charge, pre-charge, and fast charge) and the constant voltage (CV) charge mode (taper charge). Control, switch, and charge completion of these modes are detected by monitoring battery voltage by AUXPWR terminal and monitoring charging current by the voltage between CSIN terminal and CSOUT terminal.

(1) Trickle charge mode

It detects charge of the over discharged battery and abnormal operation. The trickle charge can be turned on and off by the EN_TRKL register. When the step-down DCDC converter is set on (EN_DCDC=”1”) while the trickle charge is on (EN_TRKL=”1”), the voltage of the battery is detected. When the voltage of the battery is detected 2.1 V or less, the trickle charge starts. The charge current of the trickle charge mode is 40mA (typ.). When the step-down DCDC converter is set on (EN_DCDC=”1”) while the trickle charge is off (EN_TRKL=”0”), the operation moves to the pre charge mode regardless of the voltage of the battery. When the voltage of the battery reaches 2.1 V during the trickle charge mode, it moves to the pre charge mode.

(2) Pre charge mode

It charges the over discharged battery. When the voltage of the battery reaches 2.1 V while the trickle charge is on (EN_TRKL=”1”), the pre charge starts. When the step-down DCDC converter is set on (EN_DCDC=”1”) while the trickle charge is off (EN_TRKL=”0”), the pre charge also starts. The charge current in the pre charge mode can be set in the range of 0mA to 400mA by the PRCC2-0 register. When the voltage of the battery reaches the voltage configured by FSTV3-0 register during the pre charge mode, the operation moves to the fast charge mode.

(3) Fast charge mode

It is a rapid charge mode. When the voltage of the battery reaches the voltage configured by FSTV3-0 register during the pre charge mode, the operation moves to the fast charge mode. The charge current of the fast charge mode can be set in the range of 0mA to 1,200mA by CCLT4-0 register. When the voltage of the battery reaches the voltage set by CVF7-0 register during the fast charge mode, the operation moves to the taper charge mode.

(4) Taper charge mode

It is the charge mode of the constant voltage. When the voltage of the battery reaches the voltage set by CVF7-0 register during the fast charge mode, the taper charge starts. The charge voltage of the taper charge mode can be set by CVF7-0 register in the range of 3.0V to 5.55V. In the taper charge mode, the detection of charge completion can be set on or off by the EN_TERM register. When the charge completion detection is on (EN_TERM=”1”), the charge is judged completed in the case the charge current decreases to the current value set by TERMC1-0 register. When charge completion is detected, the step-down DCDC converter is turned off (EN_DCDC=”0”) and the operation moves to the waiting mode. The current of termination can be set by TERMC1-0 register in the range of 50mA to 200mA. When the charge completion detection is turned off (EN_DCDC=”0”), this detection is invalid and setting of EN_DCDC register should be set ”0” to stop charging.

Table 8.1 Charge mode

Charge mode	Control	Charge current	Starting condition	Finishing condition	Remarks
Trickle charge	CC	40mA	EN_TRKL="1" & Battery voltage<2.1V	EN_TRKL="1" & Battery voltage≥2.1V	ON or OFF setting of the trickle charge is possible by EN_TRKL register
Pre charge	CC	50mA to 400mA	EN_TRKL="0" or Battery voltage≥2.1V	Battery voltage≥FSVT3-0 (2.1V to 3.6V)	
Fast charge	CC	1,200mA (max)	Battery voltage≥ FSVT3-0 (2.1V to 3.6V)	Battery voltage≥CVF7-0 (3.0V to 5.55V)	
Taper charge	CV	50mA to 200mA	Battery voltage≥CVF7-0 (3.0V to 5.55V)	Charge current ≤ TERMC1-0 (50mA to 200mA)	ON or OFF setting of the charge completion detection is possible by EN_TERM register

Note: Make sure to set CVF7-0 voltage > FSVT3-0 voltage.

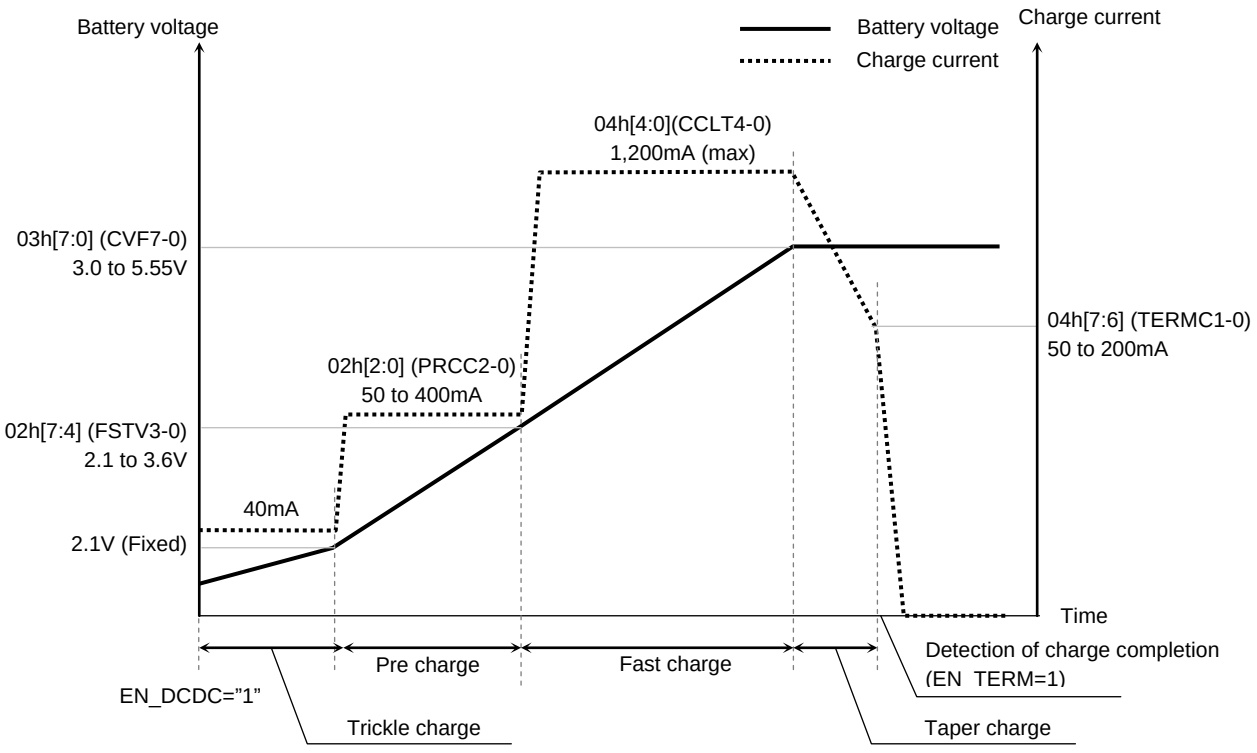


Figure 8.5 Output of charge mode

8.1.3 Feed mode

The step-down DCDC converter operates in feed mode by setting CH_DC="1". The constant voltage is supplied in this mode. Feed mode has soft start and CV mode. These modes are switched by internal counter automatically. The output voltage can be set in the range of 3.0V to 5.55V by CVF7-0 register. The over current limit value is different between the soft start mode and CV mode.

(1) Soft start

It avoids rush current which is generated just after startup. Soft start starts by setting the step-down DCDC converter on (EN_DCDC="1"). The over current limit value changes three steps as follows;

For 170μs just after soft start starting: 300mA

170μs to 340μs: 600mA

340μs to 510μs: 900mA

The operation moves to the feed mode after 510μs of starting soft start.

(2) CV mode

It supplies constant voltage. The over current limit value is 2.4A in this mode

Table 8.2 Feed mode

Feed mode	Allowable current (typ.)	Over current limit (typ.)	Setting voltage (typ.)	Remarks
CV	1.2A	2.4A	3.0V to 5.55V (CVF7-0)	CCLT4-0 setting is not valid.

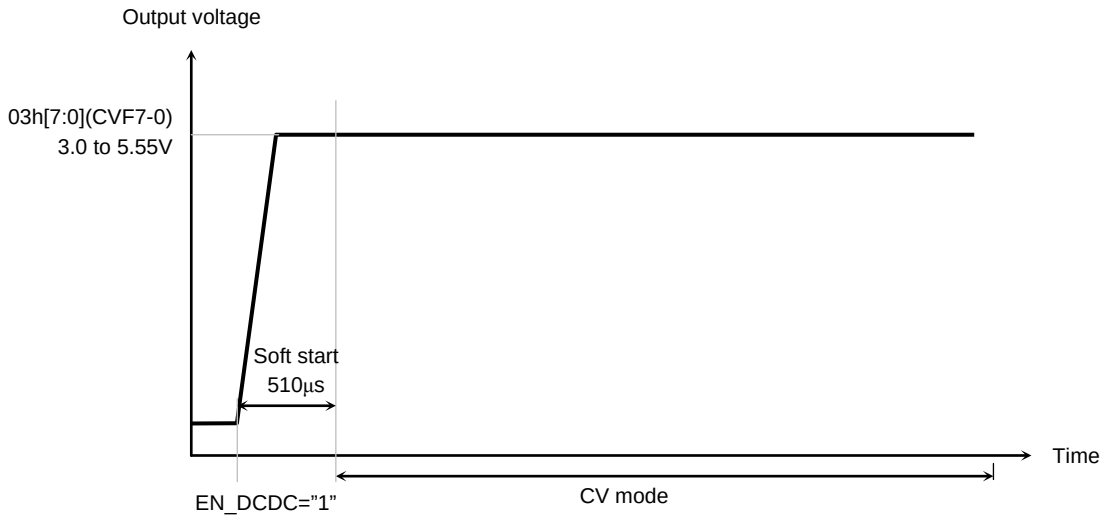


Figure 8.6 Output of feed mode

8.2 Circuit state in each operation mode

Table 8.3 Circuit in each mode

Mode		Rectifier circuit, Modulation circuit, LDO	Step-down DCDC converter	UVLO, OVLO(Note1), TSD	Safety timer (Note2)	OCL	I^2C	Writable register
Waiting mode		Enable	Disable	Enable	Disable	Disable	Access enable	All address
Charge mode	Trickle charge	Enable	Enable	Enable	Enable	Enable	Access enable	00h (Note3)
	Pre charge	Enable	Enable	Enable	Enable	Enable	Access enable	00h (Note3)
	Fast charge	Enable	Enable	Enable	Enable	Enable	Access enable	00h (Note3)
	Taper charge	Enable	Enable	Enable	Enable	Enable	Access enable	00h (Note3)
Feed mode	Soft start	Enable	Enable	Enable	Disable	Enable	Access enable	00h (Note3)
	CV	Enable	Enable	Enable	Disable	Enable	Access enable	00h (Note3)

Note 1: It is possible to turn OVLO function on or off by setting of 00h[7] resister, (EN_OVLO).

Note 2: It is possible to turn safety timer on or off by setting of 01h[3] resister, (BTMSD).

Note 3: No writing any resisters except 00h resister at Charge mode and Feed mode.

8.3 Interface

Each function of the TB6860WBG is configured by I^2C interface. It supports the sleeve function (I^2C standard) and the fast mode (400 kHz). Single writing, continuous writing, single reading, and continuous reading are possible. The sleeve address of the TB6860WBG is fixed 0b1001101.As for description of writing and reading; refer to below Figure 8.7 to Figure 8.10.

Table 8.4 Description of I^2C interface

Symbol	Description
S	Start condition
Sr	Repeat start condition
Slave Address	Sleeve address (7bit)
R	Read mode (R/W=1)
W	Write mode (R/W=0)
A	Acknowledge signal (output L level)
NA	Non acknowledge signal (output HiZ)
P	Stop condition

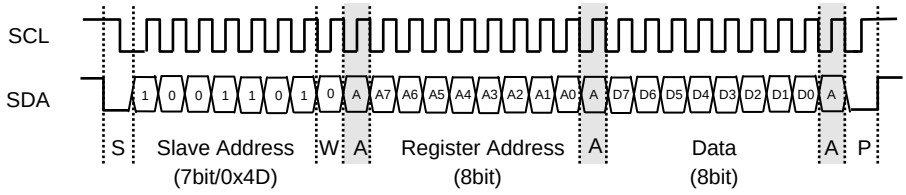


Figure 8.7 Single writing mode

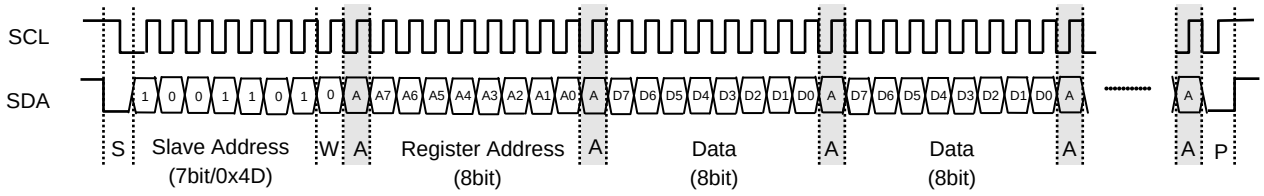


Figure 8.8 Continuous writing mode

Note 1: In continuous writing, return ACK without writing data to register 06h.

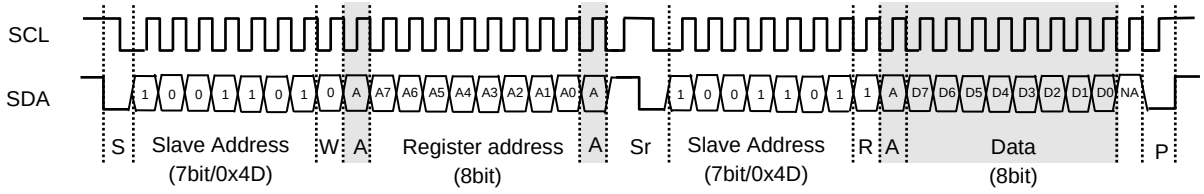


Figure 8.9 Single reading mode

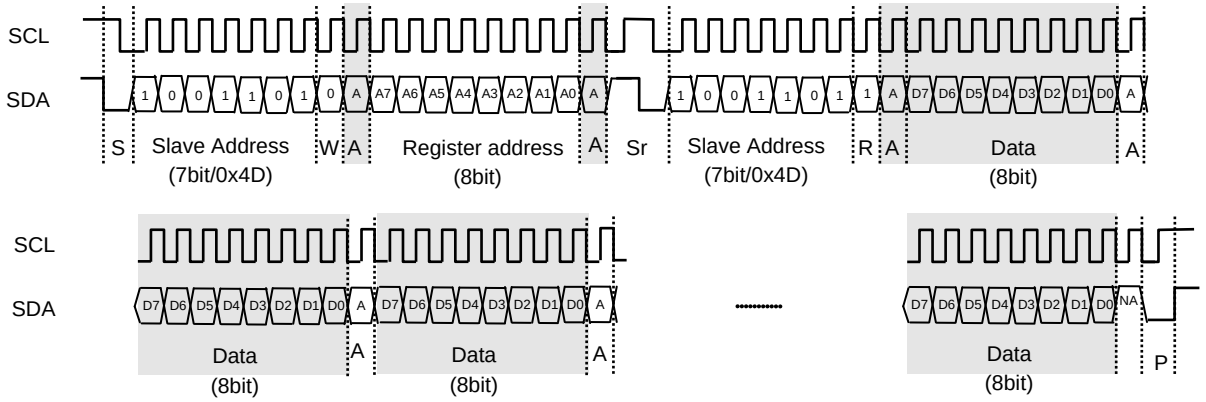


Figure 8.10 Continuous reading mode

Note 1: When ACK="1", the command of stop condition should be input to MCU.

Note 2: When stop condition is recognized, the TB6860WBG opens SDA to wait for the start condition. In case the data is under accessed, transferred data is not executed. Clock count is initialized.

Note 3: When the command is interrupted on the way, the command before interrupted is reflected. And the interrupted command is not executed. Please set the command again to reflect the command.

9. Detail description of functions

9.1 Register

The TB6860WBG can change the operation mode arbitrarily by changing the register by I^2C interface. The content of register is described in below table.

Table 9.1 Description of register

Address	Command	Write/Read	Functions
00h	Operation set	W/R	Operation mode set
01h	Charge function set	W/R	Charge function set
02h	Charge voltage/current set	W/R	Threshold set between pre charge and fast charge voltage. Pre charge current set.
03h	Output voltage level set	W/R	Output voltage set
04h	Termination current set /Charge current set	W/R	Termination current set, Fast charge current set
05h	Input over current limit/ Current sense output mode set	W/R	Input over current limit set, output mode of ISENS terminal set
06h	Charge information read	R	Charge mode information read, status of error read
07h	Test mode 1	W/R	Toshiba test mode. Do not access.
10h	Test mode 2	R	Toshiba test mode. Do not access.

Connected host side (MCU) controls the register. Under managed by the host side, the TB6860WBG changes the operation mode.

Table 9.2 Operation set: 00h

Address		7	6	5	4	3	2	1	0
	Bit Symbol	EN_OVLO	EN_DCDC	-	-	-	EN_CAP	EN_RES	-
00h	Write/Read	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R
	Default	1	0	1	1	1	0	0	1
	Function	OVLO Enable	DCDC Enable	-	-	-	Capacitive Load Enable	Resistance Load Enable	-
		0:Disable 1:Enable	0:Disable 1:Enable	1	1	0	0:Terminal (SW_C) 1:FET enable	0:Terminal (SW_R) 1:FET enable	1

Table 9.3 Charge function set: 01h

Address		7	6	5	4	3	2	1	0
	Bit Symbol	EN_TRKL	EN_TERM	-	WDTE	BTMSD	-	-	CH_DC
01h	Write/Read	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R
	Default	1	1	0	1	1	1	0	0
	Function	Trickle Charge Enable	End Charge Cycle Enable	-	Watch-Dog Timer Enable	Battery Missing Detector	-	-	Charge/ Feed Mode Set
		0:Disable 1:Enable	0:Disable 1:Enable	0	0:Disbale 1:Enable	0:Disbale 1:Enable	1	0	0:Charge Mode 1:Feed Mode

Table 9.4 Charge voltage/current set: 02h

Address		7	6	5	4	3	2	1	0
	Bit Symbol	FSTV3	FSTV2	FSTV1	FSTV0	-	PRCC2	PRCC1	PRCC0
02h	Write/Read	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R
	Default	0	0	0	0	0	0	0	0
	Function	Threshold Set between Pre-charge and Fast-charge change voltage				-	Pre-charge Current Set		
		0h: 2.1V 1h: 2.2V 2h: 2.3V 3h: 2.4V	4h: 2.5V 5h: 2.6V 6h: 2.7V 7h: 2.8V	8h: 2.9V 9h: 3.0V Ah: 3.1V Bh: 3.2V	Ch: 3.3V Dh: 3.4V Eh: 3.5V Fh: 3.6V	0	000: 50mA 001: 100mA 010: 150mA 011: 200mA		100: 250mA 101: 300mA 110: 350mA 111: 400mA

Table 9.5 Output voltage level set: 03h

Address		7	6	5	4	3	2	1	0
	Bit Symbol	CVF7	CVF6	CVF5	CVF4	CVF3	CVF2	CVF1	CVF0
03h	Write/Read	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R
	Default	0	0	0	0	0	0	0	0
	Function	CV Mode Output Voltage Set							
		00h:3.000V 01h:3.010V 02h:3.020V			Voltage Step = 10mV/bit		FDh:5.530V FEh:5.540V FFh:5.550V		

Table 9.6 Termination/charge current set: 04h

Address		7	6	5	4	3	2	1	0
	Bit Symbol	TERMC1	TERMC0	-	CCLT4	CCLT3	CCLT2	CCLT1	CCLT0
04h	Write/Read	W/R	W/R	-	W/R	W/R	W/R	W/R	W/R
	Default	0	0	-	0	0	0	0	0
	Function	Termination Current Set			Charge Current Limit Set				
		00: 50mA 01:100mA	10:150mA 11:200mA	Don't care	00h:0mA 01h:50mA 02h:100mA 03h:150mA		Current step=50mA/bit		15h:1050mA 16h:1100mA 17h:1150mA 18h:1200mA 19h to 1Fh: Prohibit

Table 9.7 Input over current limit/current sense output mode set: 05h

Address		7	6	5	4	3	2	1	0
	Bit Symbol	ISNOS1	ISNOS0	-	AICLT4	AICLT3	AICLT2	AICLT1	AICLT0
05h	Write/Read	W/R	W/R	-	W/R	W/R	W/R	W/R	W/R
	Default	0	0	-	0	0	0	0	0
	Function	ISENS Output Select			Input Current Limit Set				
		00: DCDC converter output current 01: VBAT×1/3 10: PVDD2×1/8 11: Prohibit		Don't care	00h:0mA 01h:100mA 02h:200mA 03h:300mA		Current step=100mA/bit		15h:2100mA 16h:2200mA 17h:2300mA 18h:2400mA 19h to 1Fh: Prohibit

Table 9.8 Charge information read: 06h

Address		7	6	5	4	3	2	1	0
	Bit Symbol	TRC	PRC	FST	TPC	UV_OVLO	TSD	NBAT	WDTD
06h	Write/Read	R	R	R	R	R	R	R	R
	Default	0	0	0	0	0	0	0	0
	Function	Charge Status				Voltage Detect	TSD Detect	Battery Connection Error Detect	Watch-dog Timer Detect
		0:Nop* 1:Trickle Charge	0:Nop* 1:Pre Charge	0:Nop* 1:Fast Charge	0:Nop* 1:Taper Charge	0:Nop* 1:UVLO/OVLO Detect	0:Nop* 1:TSD Detect	0:Nop* 1: Battery Connection Error Detect	0:Nop* 1:Watch-dog Timer Detect

* Nop: Non-operation

Table 9.9 Test mode 1/2: 07h/10h

Address		7	6	5	4	3	2	1	0
	Bit Symbol	TEST Mode							
07h, 10h	Function	Toshiba test mode (Do not access)							

9.2 Detail description of register

9.2.1 Operation set (00h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	EN_OVLO	EN_DCDC	1	1	0	EN_CAP	EN_RES	1
Initial value	1	0	1	1	1	0	0	1

This register sets operation mode. It sets the on and off modes of each circuit.

EN_OVLO (bit7) : ON/OFF setting of the over voltage lockout (OVLO) mode.

Table 9.10 EN_OVLO set

EN_OVLO	Function	
0	Disable	
1	Enable	(Initial value)

EN_DCDC (bit6) : ON/OFF setting of the step-down DCDC converter.

Table 9.11 EN_DCDC set

EN_DCDC	Function	
0	Disable	(Initial value)
1	Enable	

EN_CAP (bit2) : Selecting input of capacitive load modulation operation.

Table 9.12 EN_CAP set

EN_CAP	Function	
0	SW_C terminal	(Initial value)
1	Internal FET ON	

EN_RES (bit1) : Selecting input of resistance load modulation operation.

Table 9.13 EN_RES set

EN_RES	Function	
0	SW_R terminal	(Initial value)
1	Internal FET ON	

Note 1: Bit5, bit4, and bit0 must be fixed "1".

9.2.2 Charge function set (01h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
01h	EN_TRKL	EN_TERM	0	WDTE	BTMSD	1	0	CH_DC
Initial value	1	1	0	1	1	1	0	0

This register sets conditions and on/off of charge function.

EN_TRKL (bit7) : Setting ON/OFF of the trickle charge mode.

Table 9.14 EN_TRKL set

EN_TRKL	Function	
0	Disable	
1	Enable	(Initial value)

EN_TREM (bit6) : Setting ON/OFF of the charge completion of the taper charge mode.

Table 9.15 EN_TREM set

EN_TREM	Function	
0	Disable	
1	Enable	(Initial value)

WDTE (bit4) : Setting ON/OFF of the watch dog timer.

Table 9.16 WDTE set

WDTE	Function	
0	Disable	
1	Enable	(Initial value)

BTMSD (bit3) : Setting ON/OFF of the battery connection error detection

Table 9.17 BTMSD set

BTMSD	Function	
0	Disable	
1	Enable	(Initial value)

CH_DC (bit0) : Switching the charge and feed modes.

Table 9.18 CH_DC set

CH_DC	Function	
0	Charge mode	(Initial value)
1	Feed mode	

Note 1: Bit5 and bit1 must be fixed "0".

Note 2: Bit2 must be fixed "1".

9.2.3 Charge voltage/current set (02h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
02h	FSTV3	FSTV2	FSTV1	FSTV0	-	PRCC2	PRCC1	PRCC0
Initial value	0	0	0	0	0	0	0	0

This register sets the threshold voltage between the pre charge and the fast charge modes in charging and sets the current of the pre charge.

FSTV3-0(bit7-4) : Selecting the threshold voltage between the pre charge and the fast charge modes.

Table 9.19 FSTV3-0 set

FSTV3	FSTV2	FSTV1	FSTV0	Threshold voltage	
0	0	0	0	2.1V	(Initial value)
0	0	0	1	2.2V	
0	0	1	0	2.3V	
0	0	1	1	2.4V	
0	1	0	0	2.5V	
0	1	0	1	2.6V	
0	1	1	0	2.7V	
0	1	1	1	2.8V	
1	0	0	0	2.9V	
1	0	0	1	3.0V	
1	0	1	0	3.1V	
1	0	1	1	3.2V	
1	1	0	0	3.3V	
1	1	0	1	3.4V	
1	1	1	0	3.5V	
1	1	1	1	3.6V	

PRCC2-0(bit2-0) : Selecting the current of the pre charge.

Table 9.20 PRCC2-0 set

PRCC2	PRCC1	PRCC0	Pre charge current	
0	0	0	50mA	(Initial value)
0	0	1	100mA	
0	1	0	150mA	
0	1	1	200mA	
1	0	0	250mA	
1	0	1	300mA	
1	1	0	350mA	
1	1	1	400mA	

Note 1: Bit3 must be fixed "0".

9.2.4 Output voltage level set (03h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
03h	CVF7	CVF6	CVF5	CVF4	CVF3	CVF2	CVF1	CVF0
Initial value	0	0	0	0	0	0	0	0

This register sets output voltage of constant voltage (CV) mode. Output voltage can be changed with a step of 10mV.

CVF7-0(bit7-0) : Selecting output voltage in the CV mode.

Table 9.21 CVF7-0 set

CVF7-0(bin)	Output voltage of CV mode	
00000000	3.000V	(Initial value)
00000001	3.010V	
00000010	3.020V	
00000011	3.030V	
:	:	
01111110	4.260V	
01111111	4.270V	
10000000	4.280V	
10000001	4.290V	
:	:	
11111100	5.520V	
11111101	5.530V	
11111110	5.540V	
11111111	5.550V	

9.2.5 Termination current/charge current set (04h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
04h	TERMC1	TERMC0	-	CCLT4	CCLT3	CCLT2	CCLT1	CCLT0
Initial value	0	0	-	0	0	0	0	0

This register sets the current of the termination and the fast charge.

TERMC1-0(bit7-6): Selecting the current of the termination.

Table 9.22 TERMC1-0 set

TERMC1	TERMC0	Current of termination	
0	0	50mA	(Initial value)
0	1	100mA	
1	0	150mA	
1	1	200mA	

CCLT4-0(bit4-0) : Selecting the current of the fast charge.
The current can be changed with a step of 50mA.

Table 9.23 CCLT4-0 set

CCLT4	CCLT3	CCLT2	CCLT1	CCLT0	Current of fast charge	
0	0	0	0	0	0mA	(Initial value)
0	0	0	0	1	50mA	
0	0	0	1	0	100mA	
0	0	0	1	1	150mA	
:	:	:	:	:	:	
1	0	1	1	0	1,100mA	
1	0	1	1	1	1,150mA	
1	1	0	0	0	1,200mA	
1	1	0	0	1	Forbidden to set	
1	1	0	1	0	Forbidden to set	
:	:	:	:	:	:	
1	1	1	1	0	Forbidden to set	
1	1	1	1	1	Forbidden to set	

Note 1: Do not set CCLT4-0 from 0b11001 to 0b11111.

9.2.6 Input over current limit set/ISENS output mode set (05h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
05h	ISNOS1	ISNOS0	-	AICLT4	AICLT3	AICLT2	AICLT1	AICLT0
Initial value	0	0	-	0	0	0	0	0

This register sets output mode of ISEN terminal and input over current limit.

ISNOS1-0(bit7-6): Selecting output mode of ISENS terminal.

Table 9.24 ISNOS1-0 set

ISNOS1	ISNOS0	Output mode	
0	0	Output Current voltage	(Initial value)
0	1	VBAT×1/3	
1	0	PVDD2×1/8	
1	1	Forbidden to set	

AICLT4-0(bit4-0) : Selecting the input over current limit.
Limit value can be changed with a step of 100mA.
This configured value is valid in the CC mode. Set it including an operation margin for the charge current.

Table 9.25 AICLT4-0 set

AICLT4	AICLT3	AICLT2	AICLT1	AICLT0	Over current limit	
0	0	0	0	0	0mA	(Initial value)
0	0	0	0	1	100mA	
0	0	0	1	0	200mA	
0	0	0	1	1	300mA	
:	:	:	:	:	:	
1	0	1	1	0	2,200mA	
1	0	1	1	1	2,300mA	
1	1	0	0	0	2,400mA	
1	1	0	0	1	Forbidden to set	
1	1	0	1	0	Forbidden to set	
:	:	:	:	:	:	
1	1	1	1	0	Forbidden to set	
1	1	1	1	1	Forbidden to set	

Note 1: Do not set AICLT4-0 from 0b11001 to 0b11111.

9.2.7 Charge information read (06h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
06h	TRC	PRC	FST	TPC	UV_OVLO	TSD	NBAT	WDTD
Initial value	0	0	0	0	0	0	0	0

This register confirms the state in the chip. When the register data which is read is ”1”, it indicates active. This register is only for reading. Make sure that when data is written to this register, transferred command is invalid. State information of each bit is shown below. The Bit3-0 automatically are initialized when DCDC converter start to works (EN_DCDC=”1”).

Table 9.26 Charge information read

Command name	bit	Description	Data=0	Data=1
TRC	bit7	Read whether the state is in the trickle charge or not.	Non active	Active
PRC	bit6	Read whether the state is in the pre charge or not.	Non active	Active
FST	Bit5	Read whether the state is in the fast charge or not.	Non active	Active
TPC	bit4	Read whether the state is in the taper charge or not.	Non active	Active
UV_OVLO	bit3	Read detection result of over voltage/under voltage circuits.	Non detection	Detection
TSD	bit2	Read detection result of thermal shutdown circuit.	Non detection	Detection
NBAT	bit1	Read detection result of battery connecting error.	Non detection	Detection
WDTD	bit0	Read detection of watch-dog timer error.	Non detection	Detection

9.2.8 Test mode (07h/10h)

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Initial value
07h	Test mode 1(8bit)								00h
10h	Test mode 2(8bit)								00h

This register is for Toshiba test mode. Do not access to 07h and 10h registers.

9.3 Detection and protection function

The TB6860WBG has two voltage detections and two protection functions.

9.3.1 Under voltage lockout (UVLO) function

UVLO function avoids malfunction when the voltage of PVDD2 terminal is low. The detection condition is that the voltage of PVDD2 terminal drops below 3.2V (typ.). UVLO is deactivated when the voltage of PVDD2 terminal rises over 3.46V (typ.). UVLO turns off the step-down DCDC converter (EN_DCDC="0") and outputs high signal for STAT which corresponds to wait mode. The error flag which indicates abnormal input voltage is configured UV_OVLO="1". To re-start the step-down DCDC converter, the step-down DCDC converter should be set on (EN_DCDC="1") again. The error flag keeps the flag until the step-down DCDC converter is set on (EN_DCDC="1") or POR starts operation.

9.3.2 Over voltage lockout (OVLO) function

OVLO function avoids malfunction when the voltage of PVDD2 terminal is high. OVLO is activated when EN_OVLO="1". The detection condition is that the voltage of PVDD2 terminal rises over 17V (typ.).OVLO is deactivated when the voltage of PVDD2 terminal drops below 16V. OVLO turns off the step-down DCDC converter (EN_DCDC="0") and outputs high signal for STAT which corresponds to wait mode. The error flag which indicates abnormal input voltage is configured UV_OVLO="1". To re-start the step-down DCDC converter, the step-down DCDC converter should be set on (EN_DCDC="1") again. The error flag keeps the flag until the step-down DCDC converter is set on (EN_DCDC="1") or POR starts operation.

9.3.3 Thermal shutdown protection (TSD) function

TSD function protects the IC from internal temperature rise. The detection condition is that the internal temperature rises over 150°C (typ.). TSD is deactivated when the internal temperature drops below 130°C (typ.). TSD turns off the step-down DCDC converter (EN_DCDC="0") and outputs high signal for STAT which corresponds to wait mode. The error flag which indicates abnormal internal temperature is configured TSD="1". To re-start the step-down DCDC converter, the step-down DCDC converter should be set on (EN_DCDC="1") again. The error flag keeps the flag until the step-down DCDC converter is set on (EN_DCDC="1") or POR starts operation.

9.3.4 Over current limit protection (OCL) function

OCL function protects the IC from overcurrent of the step-down DCDC converter. The detection condition is that the value of current which flows in MOSFET (high side) of the step-down DCDC converter reaches the specified value. Setting method of the detection current depends on the operation mode of the step-down DCDC converter. When the step-down DCDC converter drives in charge mode, OCL detection current can be set in the range from 0 mA to 2.4 A by the register of AICLT4-0. When it drives in feed mode, OCL detection current is fixed depending on each mode. When OCL detects over current, MOSFET (high side) of the step-down DCDC converter is turned off and MOSFET (low side) is turned on. OCL function operates every switching cycle. So, OCL is deactivated in the next switching cycle automatically and the normal operation is returned.

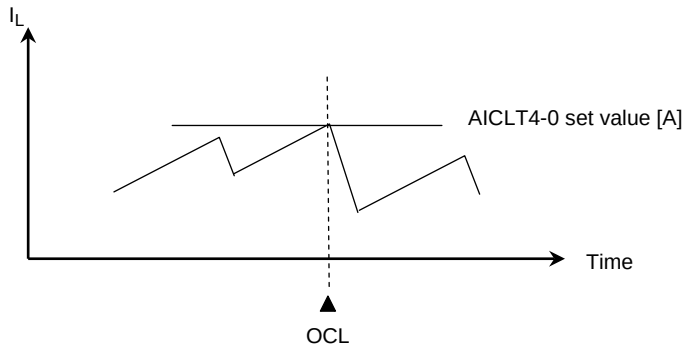


Figure 9.1 Description of OCL function

9.4 Battery missing detection

Battery missing detection avoids malfunction of charge caused by error of battery connection. It operates when the step-down DCDC converter drives in charge mode (CH_DC="0"). BTMSD register sets ON and OFF of this detection. Trickle charge function is valid. And the battery missing detection starts monitoring when the voltage of AUXPWR terminal is 2.1V or less in charge start. Battery missing detection has two error detections. First detection is activated in charge start. The safety timer starts counting when charge starts. And it continues counting during trickle charge mode and judges it battery missing after a lapse of 36 minutes. Second detection is activated in transition from trickle charge mode to pre charge mode. The safety timer re-starts counting when the mode moves from trickle charge mode to pre charge mode. The detection judges it battery missing when the voltage of AUXPWR terminal rises over 3.6V within 87ms after the operation moves to taper charge mode. When battery missing is detected, the step-down DCDC converter is set off (EN_DCDC="0") and outputs high level for STAT which corresponds to wait mode. The error flag which indicates battery missing is configured NBAT="1". Description of operation is shown in Figure 9.2. To re-start the step-down DCDC converter, the step-down DCDC converter should be set on (EN_DCDC="1") again. The error flag keeps the flag until the step-down DCDC converter is set on (EN_DCDC="1") or POR starts operating.

9.5 Watch-dog timer

The TB6860WBG includes watch-dog timer. It is configured on and off by WDTE register. It operates when the step-down DCDC converter is set on (EN_DCDC="1"). Its monitoring time is 42s. And it is reset by ACK signal of I^2C interface. When watch-dog timer is time out, the step-down DCDC converter is set off (EN_DCDC="0") and outputs high signal for STAT which corresponds to wait mode. The error flag which indicates watch-dog time out is set WDTD="1". The step-down DCDC converter should be set on (EN_DCDC="1") again to re-start the operation of the step-down DCDC converter. The error flag keeps the flag until the step-down DCDC converter is set on (EN_DCDC="1") or POR start operating.

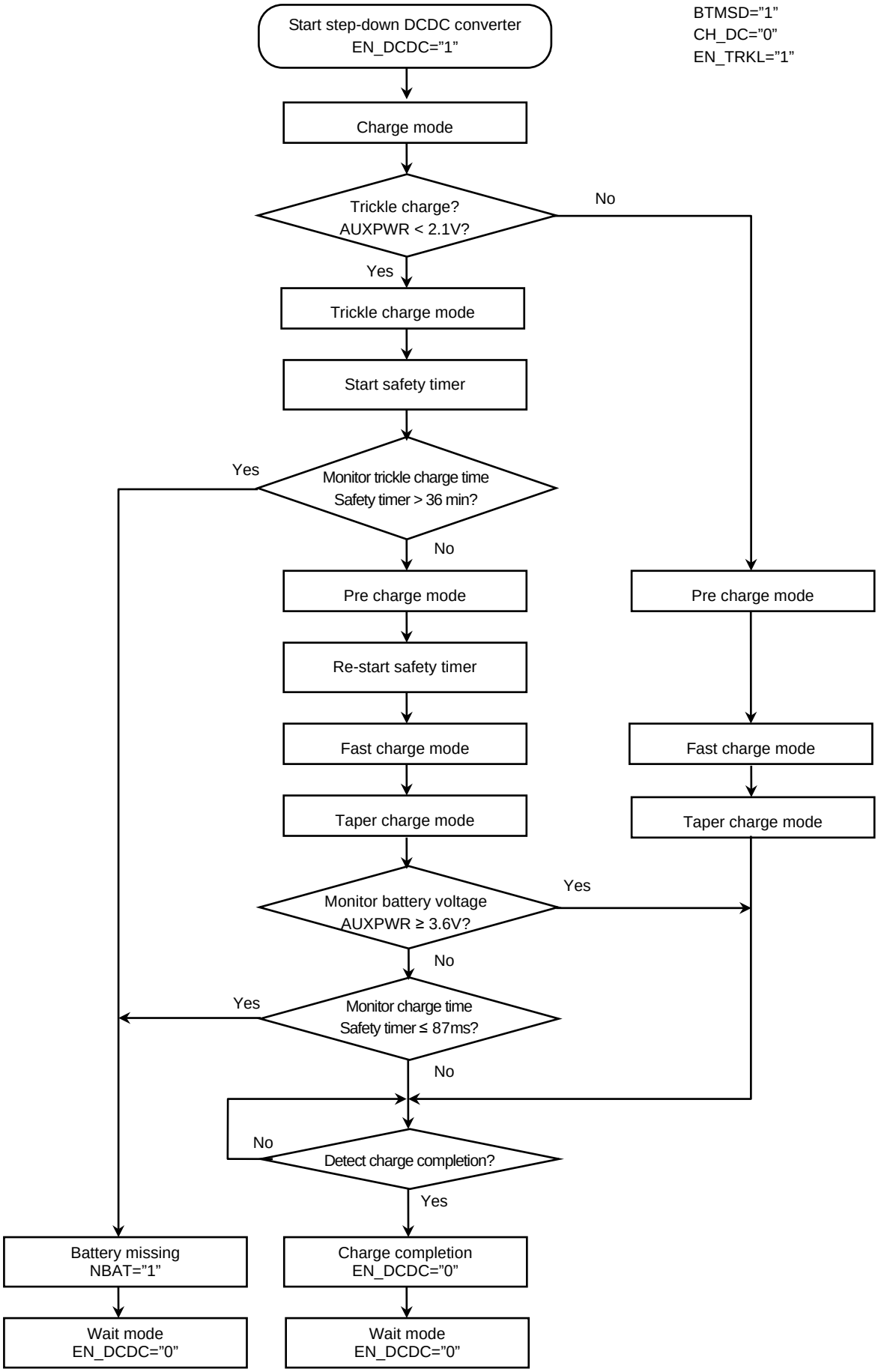


Figure 9.2 Description of battery missing detection

9.6 Function of terminals

9.6.1 STAT terminal

STAT terminal outputs the operation state of the step-down DCDC converter. STAT output corresponds to CMOS output which refers VDD33 and VSS. It outputs low level when the step-down DCDC converter is operating (Charge mode or feed mode). When the step-down DCDC converter is turned off (wait mode), it outputs high level.

9.6.2 VBAT_SENS terminal and ISENS terminal

VBAT_SENS terminal and ISENS terminal are analog output terminals which monitor input and output voltage and output current of the step-down DCDC converter by MCU.
VBAT_SENS terminal outputs 1/3 of the voltage of VBAT terminal.
ISENS terminal outputs different signal depending on the setting of ISONS1-0 registers. Relation of setting of ISNOS1-0 registers and output of ISENS terminal is shown in Table 9.27. In case that ISENS terminal is used in output current monitor mode, offset voltage is added. Measure the voltage when the DCDC converter is no load, and use the terminal after offset correction.

Table 9.27 Output mode of ISENS terminal

ISNOS1	ISNOS0	ISENS terminal output mode	Output reduction formula of ISENS	Output reduction formula
0	0	Output current (I_{OUT})	(V_{CSIN}-V_{CSOUT}) × 24+Offset (Note)	(V_{ISENS}-Offset)/24/ R_{SENSE} (Note)
0	1	Voltage of VBAT terminal	VBAT × 1/3	V_{ISENS} × 3
1	0	Voltage of PVDD2 terminal	PVDD2 × 1/8	V_{ISENS} × 8
1	1	Set forbidden	-	-

Offset : Output voltage of ISEN terminal when the step-down DCDC converter is no load during output current monitor mode.
V_{ISENS} : Output voltage of ISENS terminal
V_{CSIN} : Voltage of CSIN terminal
V_{CSOUT} : Voltage of CSOUT terminal
R_{SENSE} : Resistance of current detection which is connected between CSIN and CSOUT terminals (Recommended value: 0.068Ω)
VBAT : Voltage of VBAT terminal
PVDD2 : Voltage of PVDD2 terminal

Note: In case ISENS terminal is used in the output current monitor mode, the voltage of ISENS terminal under the condition that the DCDC converter is no load (I_{OUT}=0V) must be measured to correct offset.

10. Start sequence

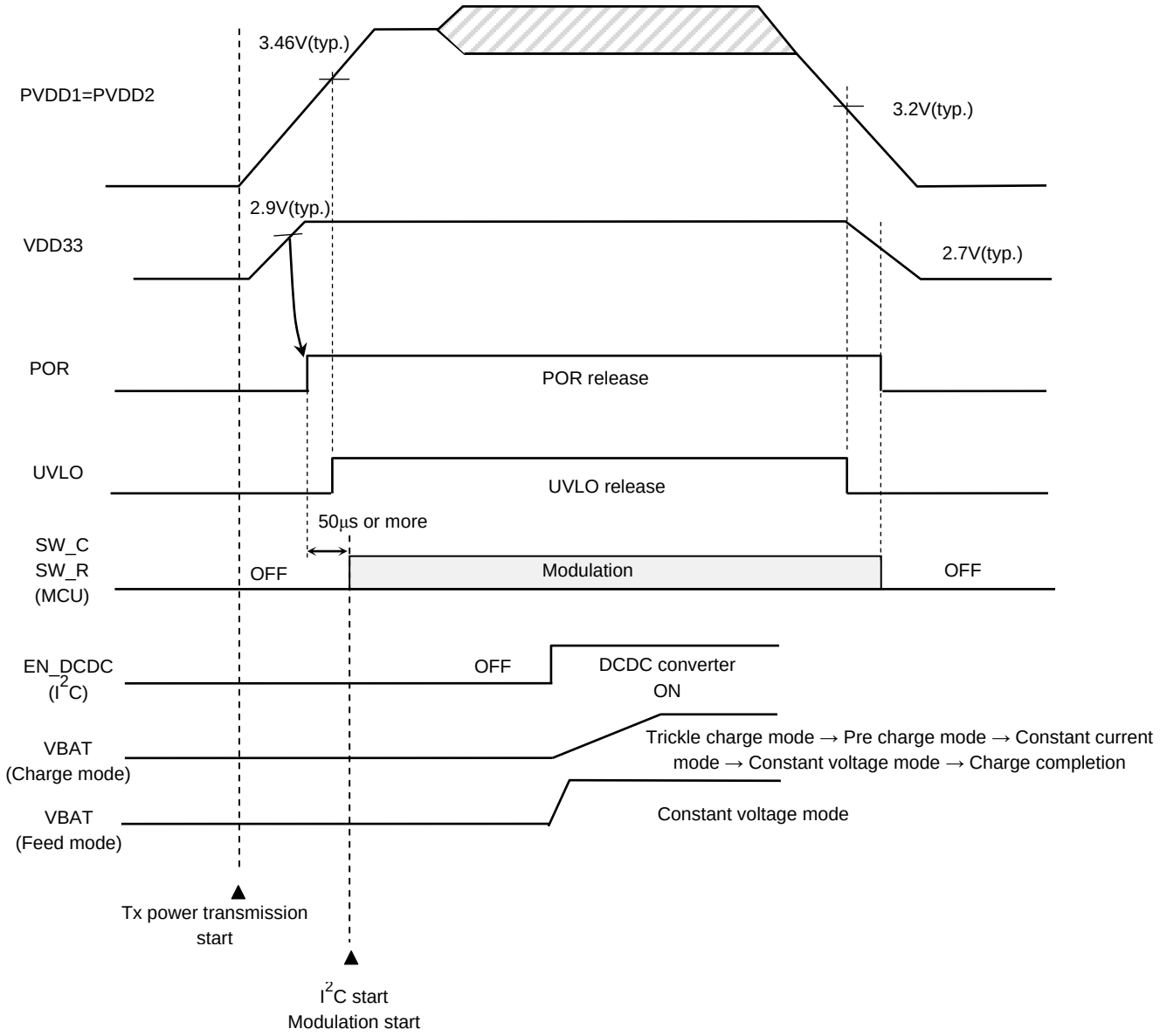


Figure 10.1 Start sequence

11. Absolute Maximum Ratings (Ta = 25°C)

Table 11.1 Absolute Maximum Ratings

Characteristics	Symbol	Rating	Unit	Remarks
Supply voltage	$PVDD_{MAX}$	- 0.3 to 20	V	(Note 1)
Input voltage 1	V_{I1}	- 0.3 to 20	V	(Note 2)
Input voltage 2	V_{I2}	- 0.3 to VOUT33 + 0.3	V	(Note 3)
Input voltage 3	V_{I3}	- 0.3 to min(5.6, PVDD + 0.3) (Note 5)	V	(Note 4)
Operating temperature	T_{opr}	- 40 to 85	°C	
Junction temperature	T_j	150	°C	
Storage temperature	T_{stg}	- 55 to 155	°C	

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
Please use the IC within the specified operating ranges.

Note: PGND1=PGND2=VSS=0V

Note 1: Apply to PVDD1 and PVDD2 terminals.

Note 2: Apply to AC1, AC2, VC1, VC2, VR, and SWIN terminals.

Note 3: Apply to SW_R, SW_C, SCL, SDA, POR, VBAT_SENS, TEST1, TEST2, and TEST3 terminals.

Note 4: Apply to CSIN, CSOUT, AUXPWR, and VBAT terminals.

Note 5: min (a, b): Smaller value is reflected by comparing a with b.

12. Electrical Characteristics

12.1 DC characteristics 1

Table 12.1 DC characteristics 1

(Unless otherwise specified, PVDD1 = PVDD2 = 5.0V, PGND1=PGND2=VSS=0V, Ta = 25°C)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit	Terminal
Power supply voltage		PVDD		3.4	—	12	V	PVDD2
Input voltage	High level	V_{IH}		0.7×V_{OUT33}	—	V_{OUT33}	V	SCL, SDA SW_R, SW_C
	Low level	V_{IL}		VSS	—	0.3×V_{OUT33}		
Input current 1	High level	I_{IH1}	V_{IH1}=V_{OUT33}	40	66	110	μA	SW_R, SW_C
	Low level	I_{IL1}	V_{IL1}=GND	-10	0	10		
Input current 2	High level	I_{IH2}	V_{IH2}=V_{OUT33}	-10	0	10	μA	SCL, SDA
	Low level	I_{IL2}	V_{IL2}=GND	-10	0	10		
Output voltage 1	Low level	V_{OL1}	I_{SINK}=3mA, N-ch open Drain	VSS	—	0.4	V	SDA
Output voltage 2	High level	V_{OH2}	I_{OUT}=-1mA	0.8×V_{OUT33}	—	V_{OUT33}	V	STAT, POR
	Low level	V_{OL2}	I_{OUT}=4mA	VSS	—	0.2×V_{OUT33}	V	
VDD33 output voltage		V_{OUT33}	I_{OUT33}=0 to 60mA	2.7	3.3	3.6	V	VDD33
VDD33 maximum output current		$I_{OUT33MAX}$		60	—	—	mA	VDD33
POR voltage		V_{POR}	Voltage of VDD33 rises from GND to “H”.	2.6	—	2.8	V	VDD33
POR hysteresis voltage		V_{PORHYS}		—	0.2	—	V	VDD33

12.2 DC characteristics 2

Table 12.2 DC characteristics 2

(Unless otherwise specified, PVDD1 = PVDD2 = 5.0V, PGND1=PGND2=VSS=0V, Ta = 25°C)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit	Terminal
Maximum output voltage of rectified step		V_{OUTMAX}		15	—	—	V	PVDD1
On resistance of rectified step 1	High side	R_{ONH_AC1}	I_{OUT}=100mA	—	150	300	mΩ	AC1
	Low side	R_{ONL_AC1}	I_{OUT}=-100mA	—	150	300		
On resistance of rectified step 2	High side	R_{ONH_AC2}	I_{OUT}=100mA	—	150	300	mΩ	AC2
	Low side	R_{ONL_AC2}	I_{OUT}=-100mA	—	150	300		
Internal resistance for adjusting rectified step 1		R_{R1}	SW_C="H"	0.85	1	1.15	kΩ	VC1, VC2
Internal resistance for adjusting rectified step 2		R_{ON2}	SW_R="H"	—	—	10	Ω	VR

12.3 DC characteristics 3

Table 12.3 DC characteristics 3

(Unless otherwise specified, PVDD1 = PVDD2 = 5.0V, PGND1=PGND2=VSS=0V, Ta = 25°C)

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit	Terminal
Judging voltage of trickle charge		V_{TRC}		1.9	2.1	2.3	V	AUXPWR
Trickle charge current		I_{TRC}	AUXPWR=2.0V	10	40	60	mA	
Accuracy of judging voltage of fast charge		$AccV_{FST}$		-3.5	—	3.5	%	AUXPWR
Accuracy of pre charge current		$AccI_{PRC}$	FSTV3-0=Fh (Setting 3.6V)	-50	—	55	mA	
Accuracy of fast charge current		$AccI_{FST}$	CVF7-0=78h (Setting 4.2V)	-105	—	80	mA	
Accuracy of termination current		$AccI_{TERM}$	CVF7-0=78h (Setting 4.2V)	-50	—	80	mA	
Accuracy of output voltage (in CV operation)		$AccV_{OUT}$		-1	—	1	%	
MOSFET On resistance	High side	R_{ONH_SW}	I_{OUT}=100mA	—	270	350	mΩ	SWIN
	Low side	R_{ONL_SW}	I_{OUT}=-100mA	—	180	250	mΩ	SWIN
Maximum output current		I_{OUTMAX}		1.2	—	—	A	
Switching frequency		f_{PWM}		2.4	3	3.6	MHz	SWIN

12.4 DC characteristics 4

Table 12.4 DC characteristics 4

(Unless otherwise specified, PVDD1 = PVDD2 = 5.0V, PGND1=PGND2=VSS=0V, Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit	Terminal
UVLO operation voltage	V_{UVLO}		3.1	3.2	3.4	V	PVDD2
UVLO hysteresis voltage	$V_{UVLOHYS}$		—	0.26	—	V	PVDD2
OVLO voltage	V_{OVLO}		15	17	20	V	PVDD2
OVLO hysteresis voltage	$V_{OVLOHYS}$		—	1	—	V	PVDD2
TSD operation temperature	T_{TSD}		120	150	—	°C	
TSD hysteresis temperature	T_{TSDHYS}		—	20	—	°C	
OCL current	I_{OCL}	CH_DC=0h AICLT4-0=0Ch (Setting 1.2A)	1.08	1.2	1.32	A	PVDD2

12.5 AC characteristics

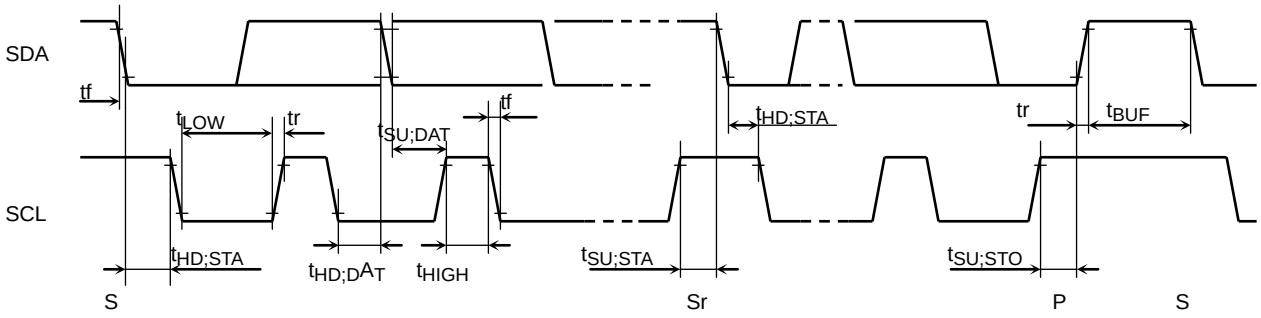


Table 12.5 AC characteristics

(Unless otherwise specified, PVDD1 = PVDD2 = 5.0V, PGND1=PGND2=VSS=0V, Ta = 25°C)

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Operation clock frequency	f_{SCL}		—	—	400	kHz
Hold time of repeated start	$t_{HD:STA}$		0.6	—	—	μs
Setup time of repeated start	$t_{SU:STA}$		0.6	—	—	μs
Data hold time	$t_{HD;DAT}$		0	—	0.9	μs
Data setup time	$t_{SU;DAT}$		100	—	—	ns
Low term of SCL signal	t_{LOW}		1.3	—	—	μs
High term of SCL signal	t_{HIGH}		0.6	—	—	μs

13. Application Circuit

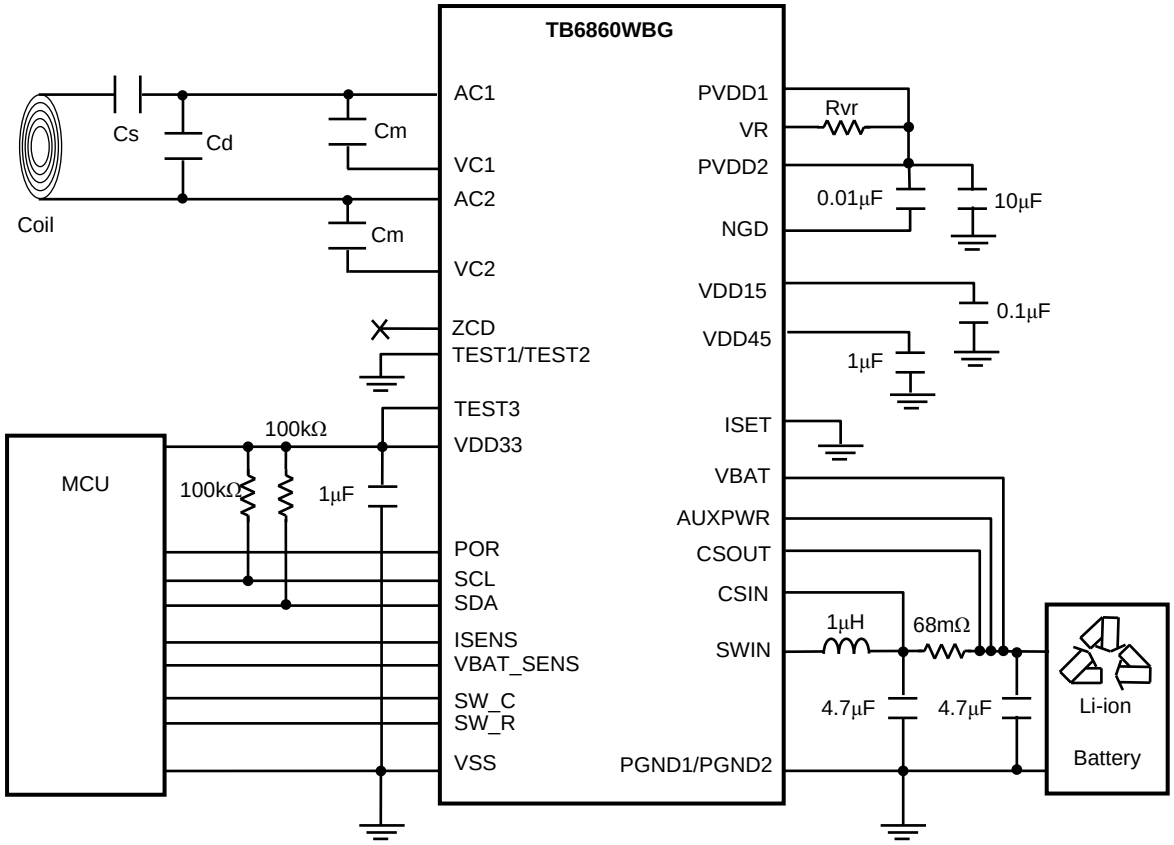


Figure 13.1 Charger mode

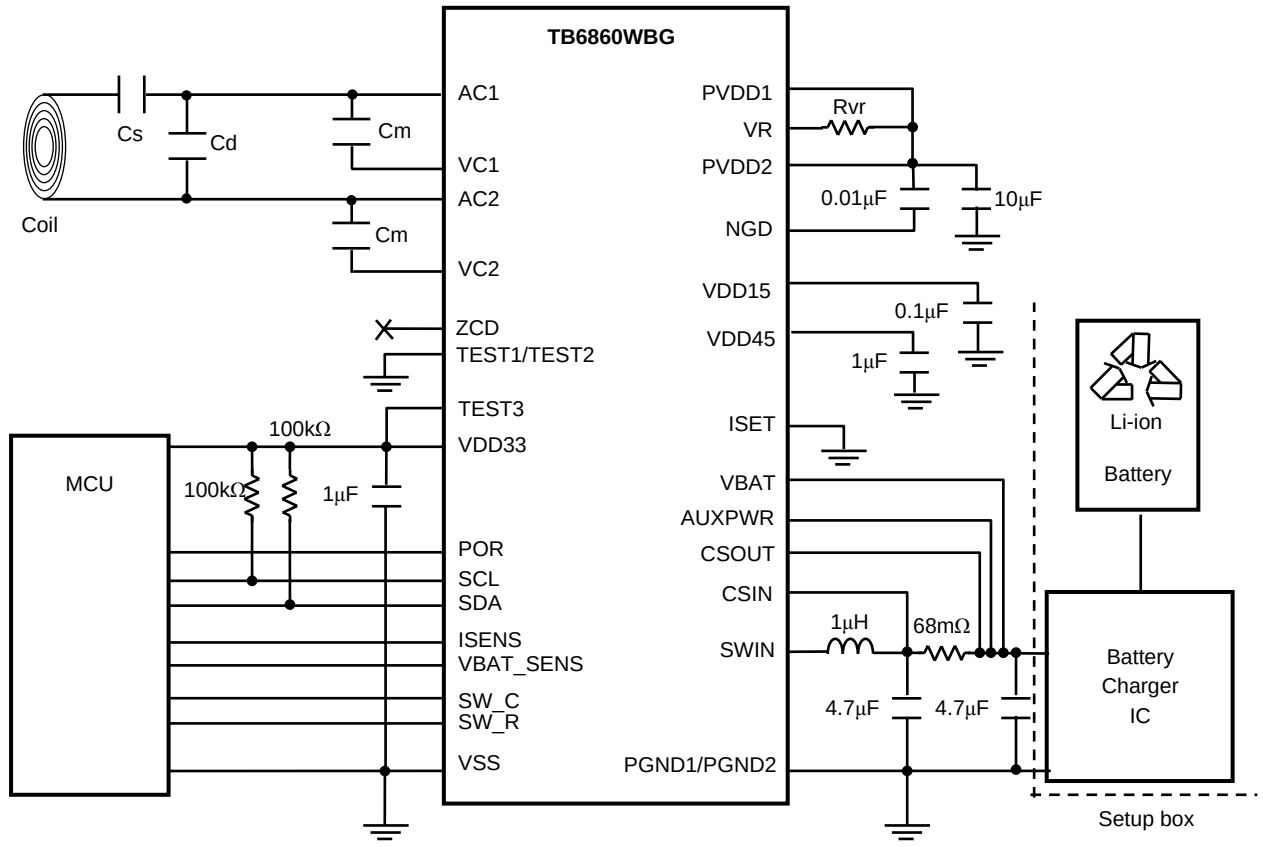
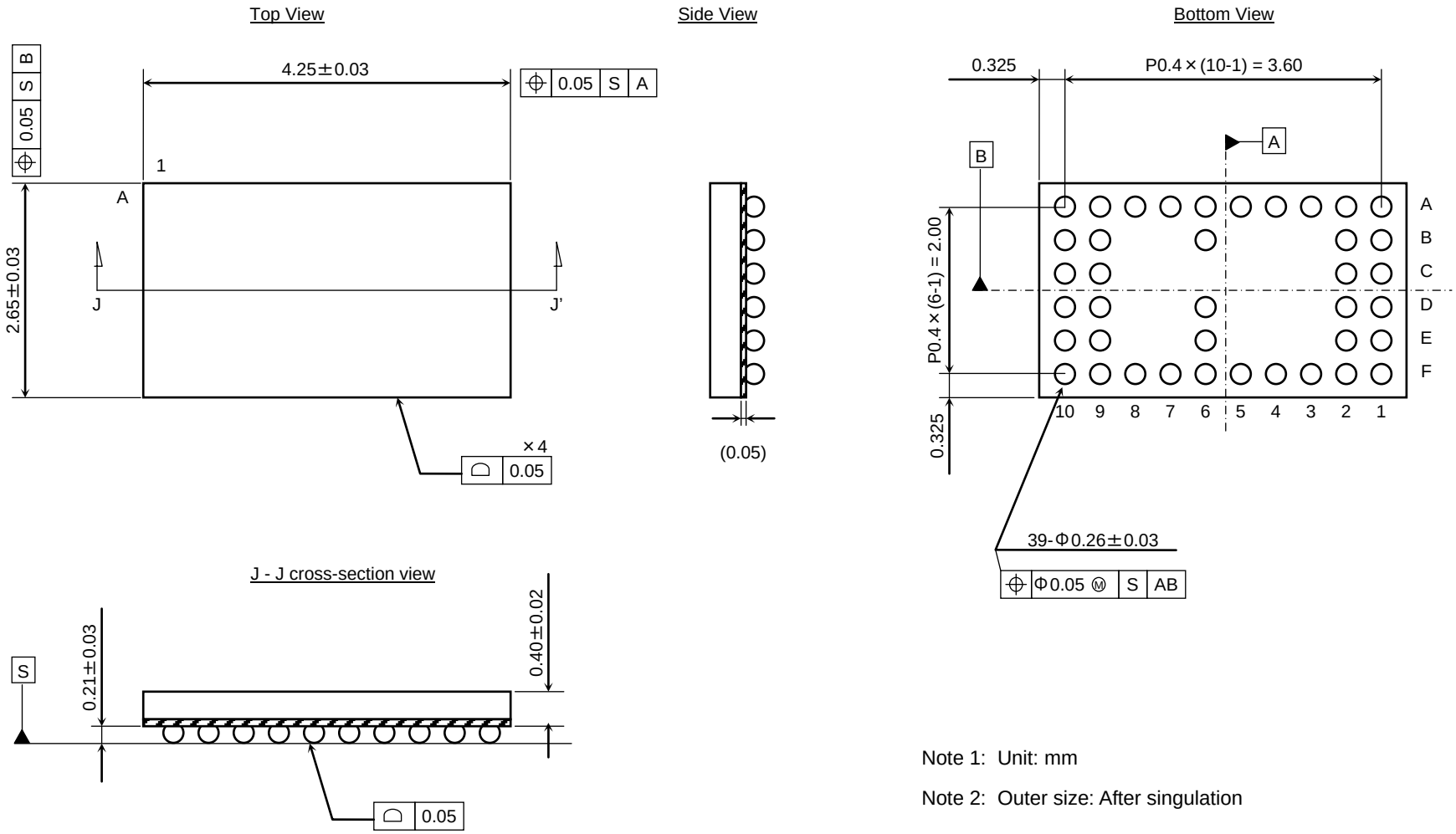


Figure 13.2 Feed mode

14. Package dimensions



Note 1: Unit: mm

Note 2: Outer size: After singulation

Weight: 13mg (Typ.)

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