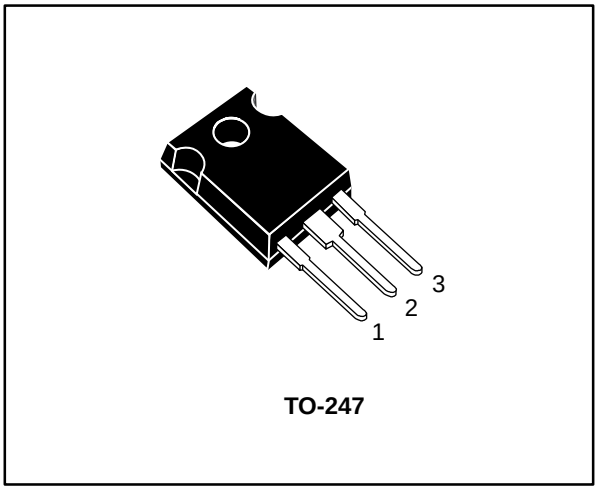
STW240N10F7

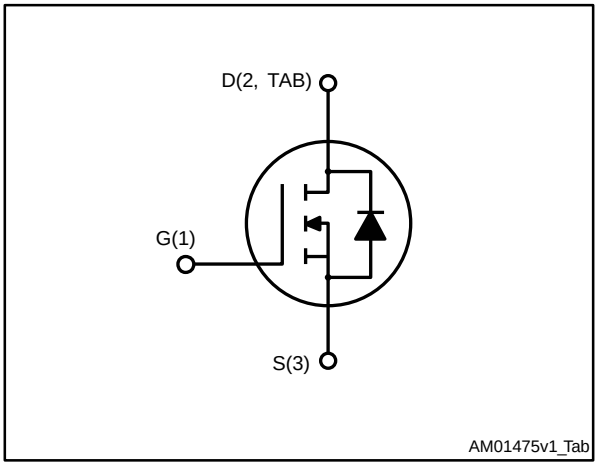
N-channel 100 V, 2.6 mΩ typ., 180 A, STripFET™ F7 Power MOSFET in a TO-247 package

Datasheet - production data



TO-247

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW240N10F7	100 V	3.0 mΩ	180 A

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STW240N10F7	240N10F7	TO-247	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	180	A
	Drain current (continuous) at T_C = 100 °C	160	A
I_D(2)	Drain current (pulsed)	720	A
P_{TOT}	Total dissipation at T_C = 25 °C	300	W
E_{AS}(3)	Single pulse avalanche energy	500	mJ
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		°C

Notes:

(1)Current limited by package

(2)Pulse width limited by safe operating area

(3)Starting T_J = 25 °C, I_D = 45 A, V_{DD} = 50 V

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	50	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 100 V			1	µA
		V_{GS} = 0, V_{DS} = 100 V; T_C = 125 °C(1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 90 A		2.6	3.0	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	-	11550	-	pF
C_{oss}	Output capacitance			2950		pF
C_{rss}	Reverse transfer capacitance			217		pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 180 A V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)		160		nC
Q_{gs}	Gate-source charge			48		nC
Q_{gd}	Gate-drain charge			38		nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 90 A, R_G = 4.7 Ω, V_{GS}= 10 V (see *Figure 13: "Test circuit for resistive load switching times"*)	-	49	-	ns
t_r	Rise time			139		ns
$t_{d(off)}$	Turn-off delay time			110		ns
t_f	Fall time			112		ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	I_{SD} = 180 A, V_{GS} = 0			1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 180 A, di/dt = 100 A/µs, V_{DD} = 80 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)		108		ns
Q_{rr}	Reverse recovery charge			315		nC
I_{RRM}	Reverse recovery current			5.8		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

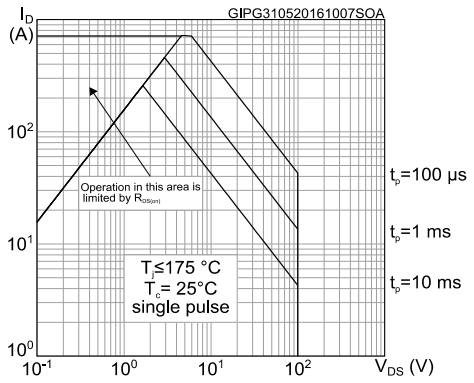


Figure 3: Thermal impedance

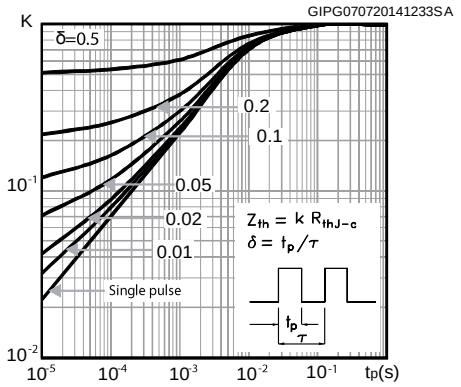


Figure 4: Output characteristics

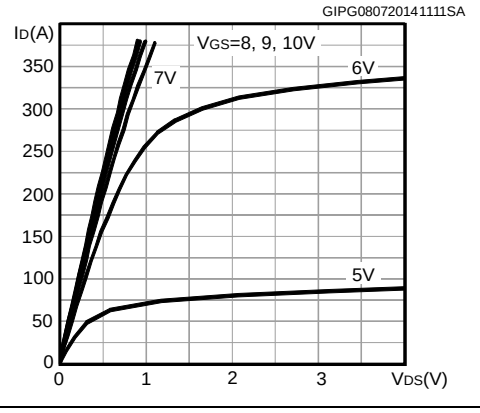


Figure 5: Transfer characteristics

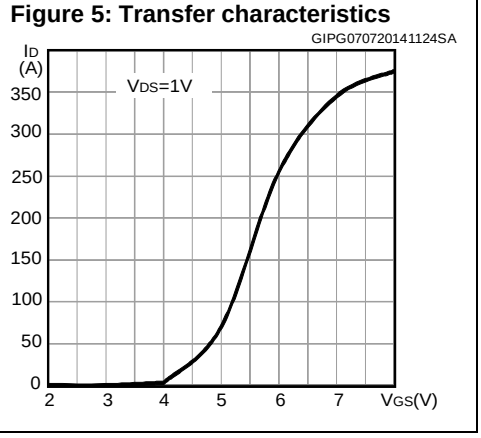


Figure 6: Gate charge vs gate-source voltage

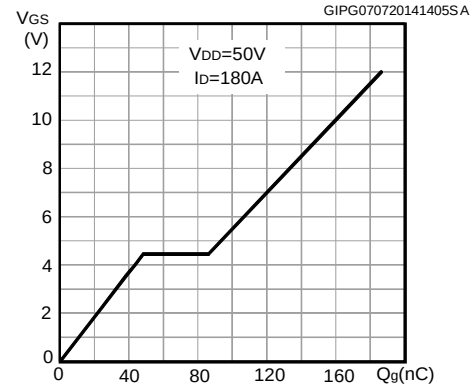


Figure 7: Static drain-source on-resistance

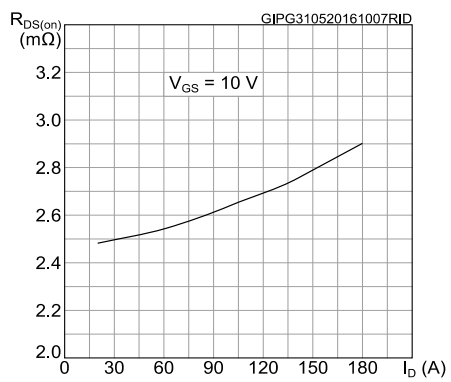


Figure 8: Normalized V(BR)DSS vs temperature

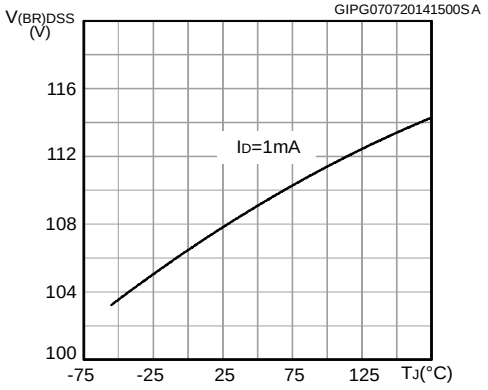


Figure 9: Capacitance variations

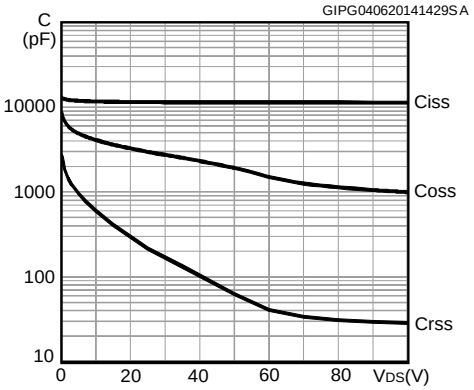


Figure 10: Source-drain diode forward characteristics

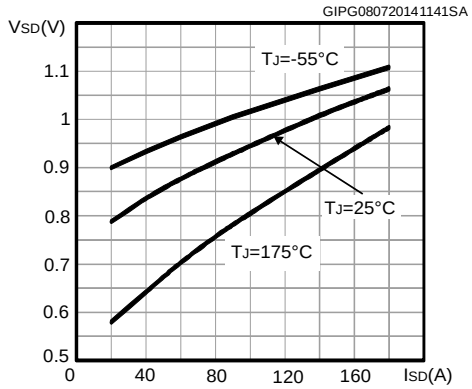


Figure 11: Normalized gate threshold voltage vs temperature

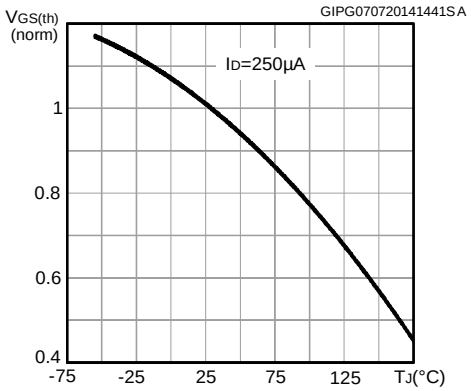
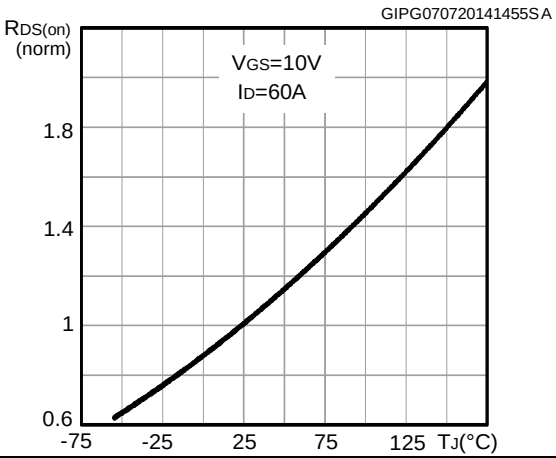


Figure 12: Normalized on-resistance vs temperature



3 Test circuits

Figure 13: Test circuit for resistive load switching times

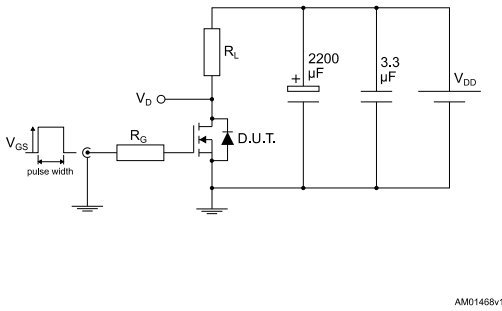


Figure 14: Test circuit for gate charge behavior

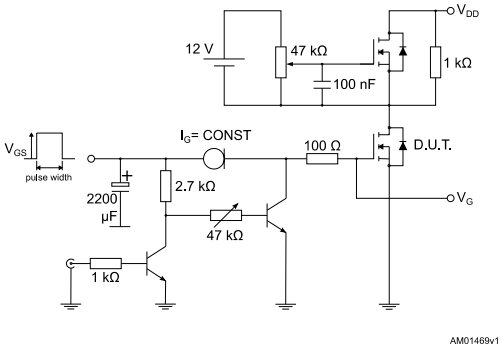


Figure 15: Test circuit for inductive load switching and diode recovery times

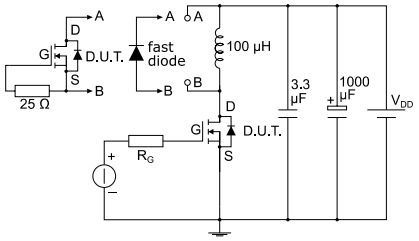


Figure 16: Unclamped inductive load test circuit

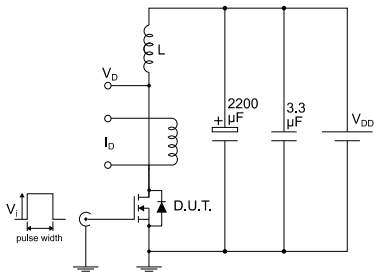


Figure 17: Unclamped inductive waveform

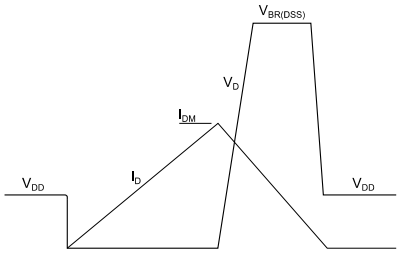
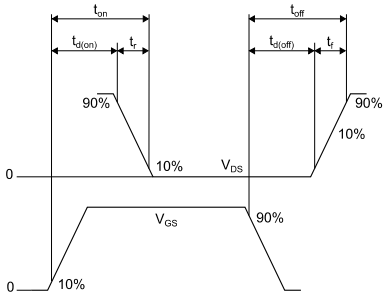


Figure 18: Switching time waveform



4 Package information

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4.1 TO-247 package information

Figure 19: TO-247 package outline

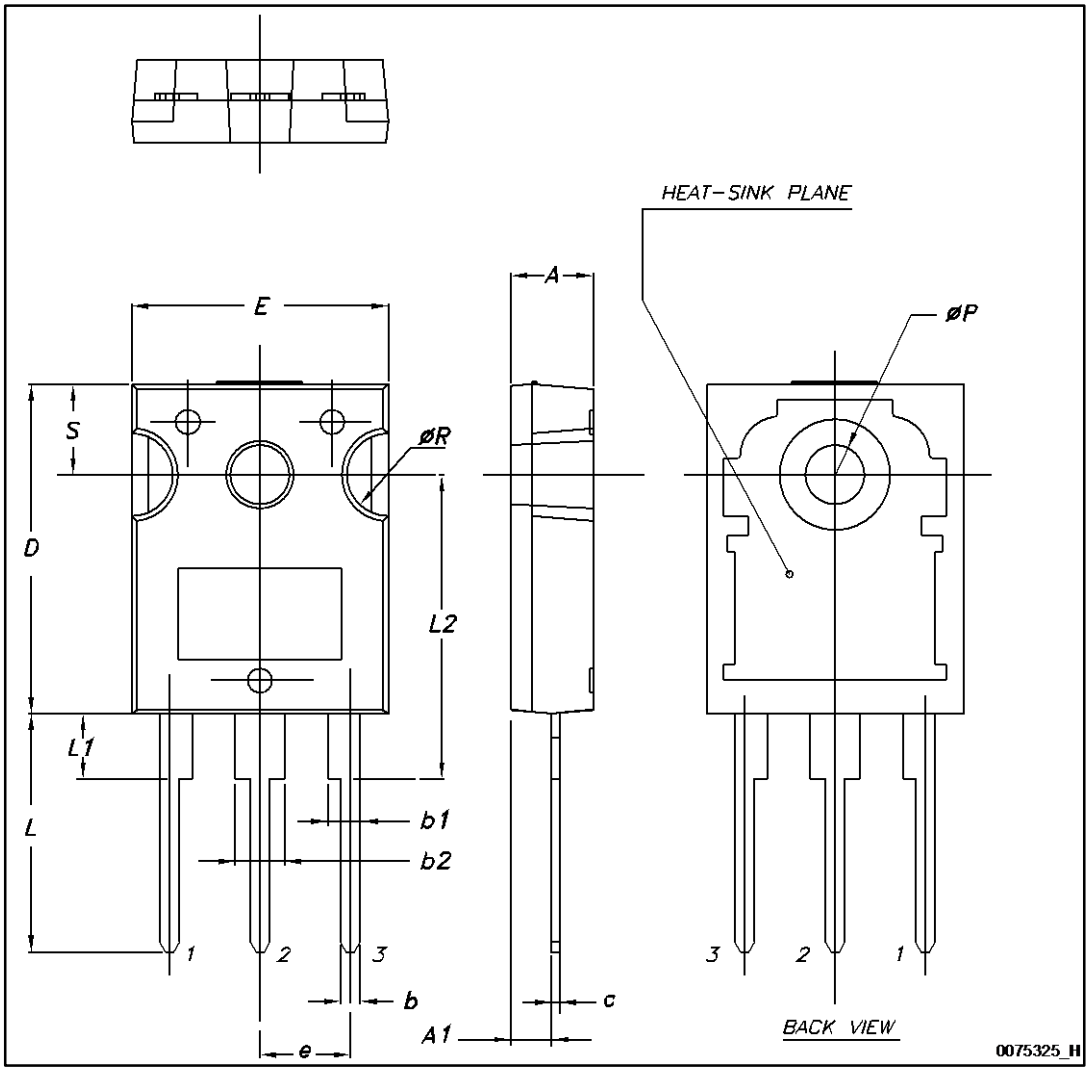

Table 8: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
06-Jun-2016	1	Initial release.
08-Jul-2016	2	Document status promoted from preliminary to production data.

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Тел: +7 (812) 336 43 04 (многоканальный)
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www.lifeelectronics.ru