

Technical Note

Hi-performance Regulator IC Series for PCs PGOOD IC for PC

No.09030EBT18

RoHS

Description

BD4140HFV

BD4140HFV is 1ch reset IC for watching the voltage. The detected voltage is 0.5V, and it is available to several kinds of voltage with additional external resistance. For the independent supply voltage (Vcc), the "L" level of voltage is guaranteed in case the watching input voltage is also low.

Features

- 1) Open drain output type
- 2) Built in Under Voltage LockOut (UVLO) circuit
- 3) HVSOF5 package : 1.6 × 1.6 × 0.6(mm)

Applications

Laptop PC, Desktop PC, LCD-TV, Printer, STV, Digital appliances

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	BD4140HFV	Unit	
Terminal voltage	Vcc, IN, DLY, PGOOD	6 ^{*1}	V	
Power Dissipation	Pd	0.67 *2	W	
PGOOD Capacity Current	IPGOOD	5	mA	
Operating temperature range	Topr	-10~+100	°C	
Storage temperature range	Tstg	-55~+150	°C	
Junction Temperature	Tjmax	+150	°C	

*1 Do not however exceed Pd.

*2 Reduced by θ_{ja} = 186.6°CW for increase in Ta of 1°C over 25°C.

(when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB which has 1 layer. (copper foil density :2%))

*3 Reduced by θ_{ja} = 185.2°CW for increase in Ta of 1°C over 25°C

(when mounted on a board 70.0mm × 70mm × 1.6mm Glass-epoxy PCB which has 1 layer.)

Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Max.	Unit
	Vcc	3.0	5.5	V
Terminal valtage	IN	-0.3	V _{CC} -2	V
Terminal voltage	PGOOD	-0.3	5.5	V
	DLY	-0.3	V _{CC}	V

●ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta=25°C, VCC=5V)

Devementer	Currente e l	Limits Unit Conditions	Limits			
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Bias Current	lcc	-	5	10	μA	-
Detected Voltage	Vdet	491	500	509	mV	IN sweep up
Hysteresis Voltage	VHYS	-	10	-	mV	IN sweep down
Delay Current	Idly	150	250	350	nA	IN=0.6V
PGOOD Output ON Resistance	RVout	-	100	200	Ω	IN=0V
PGOODOutput Leak Current	Ιουτ	-	0	5	μA	IN=0.6V

Block Diagram



Pin Layout



Pin Function Table

PIN No.	PIN Name	PIN Function
1	PGOOD Reset Output Pin (Power Good Signal	
2	GND	Ground Pin
3	Vcc	Power Supply Input Pin
4	IN	Watching Voltage Input Pin
5	DLY	Capacitor connected pin for setting delay time
Bottom	FIN	Substrate

Explanation of Operation

BD4140HFV is 1ch reset IC with independent supply voltage.

The following voltage is available to input VCC voltage before the watching input voltage. (Input-output voltage characteristic)



(Detected delay time setting)



TDELAY is calculated with formula below.

TDELAY [sec] = $\frac{\text{CEXT} [\mu \text{ F}] \times 0.5}{0.25 [\mu \text{ A}]}$ $= 2 \times \text{C}_{\text{EXT}}[\text{pF}] \times 10^{-6}$

 $CEXT[pF] = TDELAY[sec] / (2 \times 10^{-6})$

(Example) When using the 4700pF capacitor,

TDELAY [sec] = $2 \times 4700 \text{ [pF]} \times 10^{-6}$ = $9400 \times 10^{-6} = 9.4 \text{ [ms]}$

(Example) When setting 2ms Delay,

 $CEXT = 2 [ms] \times 0.25 [uA] / 0.5$ $= \frac{2 \times 10^{-3} \times 0.25 \times 10^{-6}}{0.5}$ $= 1 \times 10^{-9}$ = 1000[pF]

<VCC starting>

- When VCC is below the minimum operation voltage, PGOOD pin will be at H level. (The meaning of the minimum operation voltage is : When the starting of VCC, PGOOD output voltage become within 10% of VCC voltage, and the value will be around 0.8VTYP(RPGOOD=100k Ω) and 1.0VTYP(RPGOOD=10k Ω). But note that this value is reference.)
- ② If VCC value exceeds the minimum operation voltage, by the VCC reached UVLO cancellation voltage (2.5V TYP), PGOOD output become at L level.
- ③ If VCC exceeds UVLO cancellation voltage, when the input voltage of IN pin is over the detected voltage, PGOOD pin will be at H level, and when the input voltage of IN pin is below the detected voltage, PGOOD pin will be at L level.

(PGOOD=OK)



(PGOOD=NG)



Evaluation Board Circuit



BD4140HFV Evaluation Board Standard Component List (at detecting 0.5V)

Component	Rating	Manufacturer	Product Name	Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD4140HFV	R1	100kΩ	ROHM	
C1	-	-	-	R2	0Ω	-	jumper
C2	1000pF	murata	GRM1552C1H102JA01	R3	-	-	-
C3	-	-	-	R4	0Ω	-	jumper
C4	-	-	-				

BD4140HFV Evaluation Board Layout

Silk screen (Top)



TOP Layer

Bottom Layer





Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Power supply lines

Please add a protection diode when a large inductance component is connected to the output terminal, and reverse-polarity power is possible at startup or in output OFF condition.



3. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

4. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

5. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

7. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



Power Dissipation Characteristics ØHVSOF5



BD4140HFV

Ordering part number



HVSOF5



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