Si4770/77-A20

HIGH-PERFORMANCE CONSUMER ELECTRONICS BROADCAST RADIO RECEIVER AND HD RADIO TUNER

Features

- Worldwide FM band support (64–108 MHz)
- Worldwide AM band support (520–1710 kHz)
- AM/FM HD Radio support (Si4777 only)
- Comprehensive signal quality metrics: RSSI, SNR, multipath interference, frequency offset, adjacent channel RSSI, frequency deviation, and image RSSI
- Advanced patented RDS soft-decision decoder
- Advanced, patented FM channel equalizer for multipath interference
- Dynamic AM/FM channel bandwidth control
- Programmable AM/FM soft mute
- FM stereo-mono blend
- FM hi-blend control
- AM/FM hi-cut control
- AM lo-cut filter
- L/R analog and digital (I^2S) audio outputs
- Digital Low-IF architecture
- Frequency synthesizer with fully integrated PLL-VCO
- Fully integrated AM/FM front-end including high performance LNA, AGC with integrated resistor and capacitor banks, and RF and IF peak detectors
- Integrated crystal oscillator
- Digital (I^2S) Zero-IF AM/FM I/Q outputs (Si4777 only)
- 1.2 to 5 V power supplies
- QFN 40-pin, 6x6x0.85 mm
  - Pb-free/RoHS compliant

Applications

- Audio/video receivers
- Consumer electronics
- Boom boxes
- Home theater systems

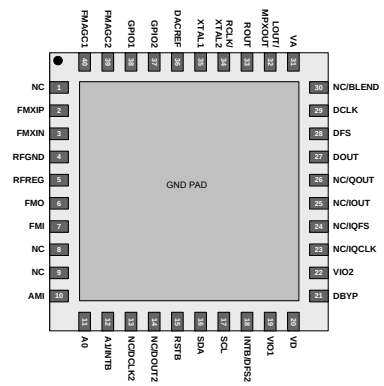
Description

The Si4770/77-A20 broadcast receiver and HD Radio tuner (Si4777 only) employs an advanced, proven digital low-IF architecture to bring outstanding receiver performance to high-performance consumer electronics.

Ordering Information:
See page 49.

Pin Assignments

Si4770/77-A20



Patents pending

Functional Block Diagram

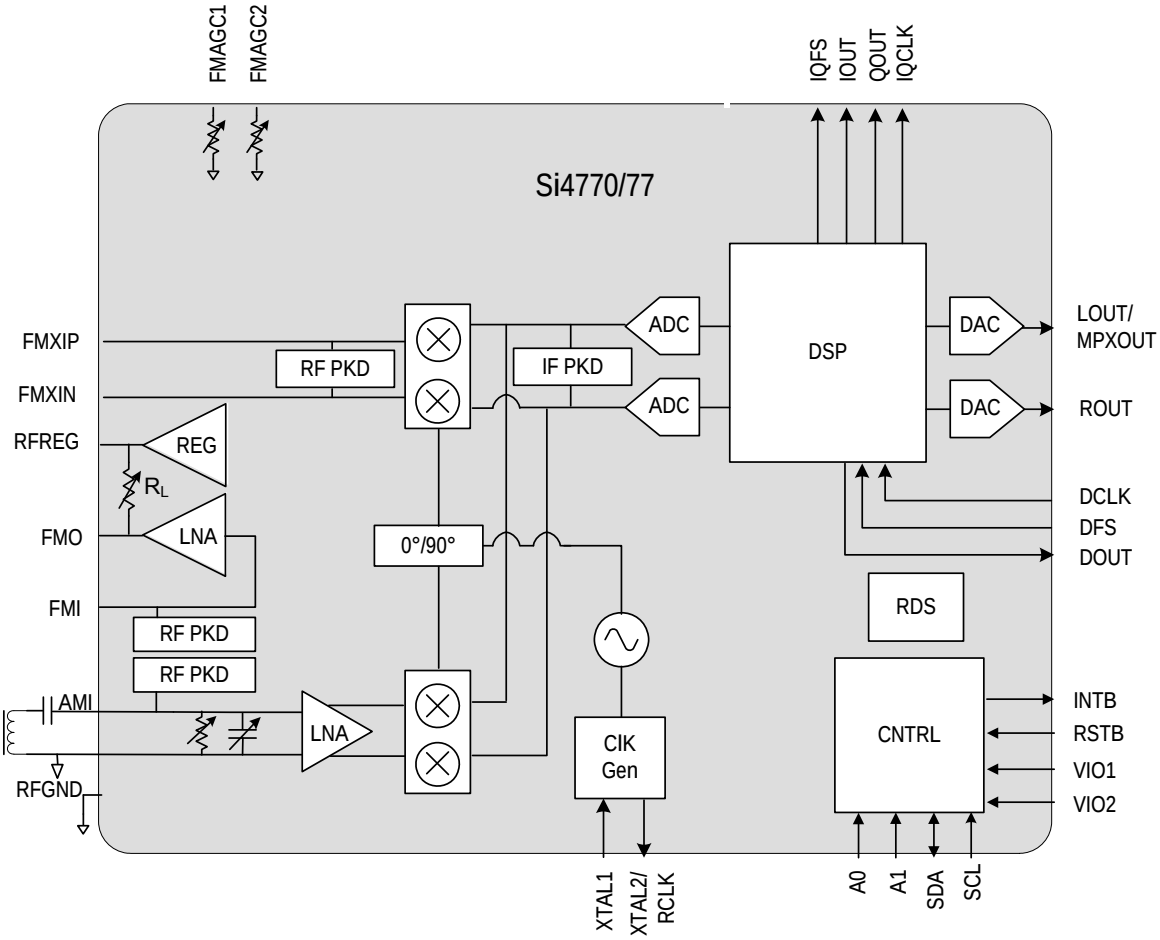


TABLE OF CONTENTS

Section **Page**

1. Electrical Specifications

Table 1. Recommended Operation Conditions*

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog Supply Voltage	V_A	—	4.5	5	5.5	V
Digital Supply Voltage	V_D	—	2.7	3.3	3.6	V
Interface Supply Voltage	V_{IO1}	—	1.7	3.3	3.6	V
	V_{IO2}	—	1.2	3.3	3.6	V

***Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at V_D = 3.3 V, V_{IO1} = 3.3 V, V_{IO2} = 3.3 V, V_A = 5 V, and 25 °C unless otherwise stated. Parameters are tested in production unless otherwise stated.

Table 2. DC Characteristics

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FM Mode						
Total Supply Power			671	850	1049	mW
V_A Supply Current	I_{VA}		121	130	139	mA
V_D Supply Current	I_{VD}		47	60	79	mA
V_A Supply Power Down Current	I_{VA}		20	90	170	µA
V_D Supply Power Down Current	I_{VD}		5	20	50	µA
AM Mode						
Total Supply Power			707	900	1100	mW
V_A Supply Current	I_{VA}		129	140	147	mA
V_D Supply Current	I_{VD}		47	60	81	mA
V_A Supply Power Down Current	I_{VA}		20	90	170	µA
V_D Supply Power Down Current	I_{VD}		5	20	50	µA

***Note:** See "7. I2C Control Bus" on page 44.

Table 2. DC Characteristics (Continued)

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Interface Supplies						
V_{IO1} Supply Current	I_{VIO1}		0.1	0.5	0.82	mA
V_{IO2} Supply Current	I_{VIO2}		0.1	0.2	0.5	mA
V_{IO1} Supply Power Down Current*	I_{PD}		150	250	420	µA
V_{IO2} Supply Power Down Current*	I_{PD}		5	20	150	µA
Inputs Pins SCL, SDA, RSTB, A0, A1						
High Level Input Voltage	V_{IH}		0.7 x V_{IO1}	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3xV_{IO1}	V
High Level Input Current	I_{IH}	V_{IN} = V_{I01} = 3.6 V	–10	—	10	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 = V, V_{I01} = 3.6 V	–10	—	10	µA
Input Pins DCLK, DFS						
High Level Input Voltage	V_{IH}		0.7 x V_{IO2}	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.3 x V_{IO2}	V
High Level Input Current	I_{IH}	V_{IN} = V_{I02} = 3.6 V	–10	—	10	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 V, V_{I02} = 3.6 V	–10	—	10	µA
Input Pins GPIO1, GPIO2						
High Level Input Voltage	V_{IH}	GPIO1 and GPIO2 are internally regulated at 3.6 V	2.52	—	—	V
Low Level Input Voltage	V_{IL}		—	—	1.08	V
High Level Input Current	I_{IH}	V_{IN} = 3.6 V	–10	—	10	µA
Low Level Input Current	I_{IL}	V_{IN} = 0 V	–10	—	10	µA
Output Pins INTB						
High Level Output Voltage	V_{OH}	Output is common drain output with internal 10 kΩ pull-up to V_{IO1}	0.8xV_{IO1}	—	—	V
Low Level Output Voltage	V_{OL}	I_{OUT} = –500 µA	—	—	0.2xV_{IO1}	V

***Note:** See "7. I2C Control Bus" on page 44.

Table 2. DC Characteristics (Continued)

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pins SDA						
High Level Output Voltage	V_{OH}	Output is common drain output with external 4.7 kΩ pull-up to V_{IO1}	$0.8xV_{IO1}$	—	—	V
Low Level Output Voltage	V_{OL}	I_{OUT} = –500 µA	—	—	$0.2xV_{IO1}$	V
Output Pins GPIO1, GPIO2						
High Level Output Voltage	V_{OH}	GPIO1 and GPIO2 are internally regulated at 3.6 V, IOUT = +500 µA	2.88	—	—	V
Low Level Output Voltage	V_{OL}	I_{OUT} = –500 µA	—	—	0.72	V
Output Pins IQCLK, IQFS, IOUT, QOUT, DFS, DCLK, DOUT						
High Level Output Voltage	V_{OH}	I_{OUT} = 500 µA	$0.8 \times V_{IO2}$	—	—	V
Low Level Output Voltage	V_{OL}	I_{OUT} = –500 µA	—	—	$0.2 \times V_{IO2}$	V
***Note:** See "7. I2C Control Bus" on page 44.						

Table 3. Digital Audio Interface Characteristics*

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DCLK Input Cycle Time	$t_{CYC:\ DCLK}$		70	—	—	ns
DCLK Input Pulse Width High	$t_{HI:\ DCLK}$		0.4 x $t_{CYC:DCLK}$	—	0.6 x $t_{CYC:DCLK}$	ns
DCLK Input Pulse Width Low	$t_{LO:\ DCLK}$		0.4 x $t_{CYC:DCLK}$	—	0.6 x $t_{CYC:DCLK}$	ns
DFS Setup Time	$t_{SU:DFS}$		10	—	—	ns
DFS Hold Time	$t_{HD:DFS}$		5	—	—	ns
DOUT ouTput Delay	$t_{PD:DOUT}$		0	—	35	ns
Capacitive Loading	C_B	$VIO_2 \leq 1.33$ V	—	—	10	pF
		$VIO_2 > 1.33$ V	—	—	15	

***Note:** Guaranteed by characterization.

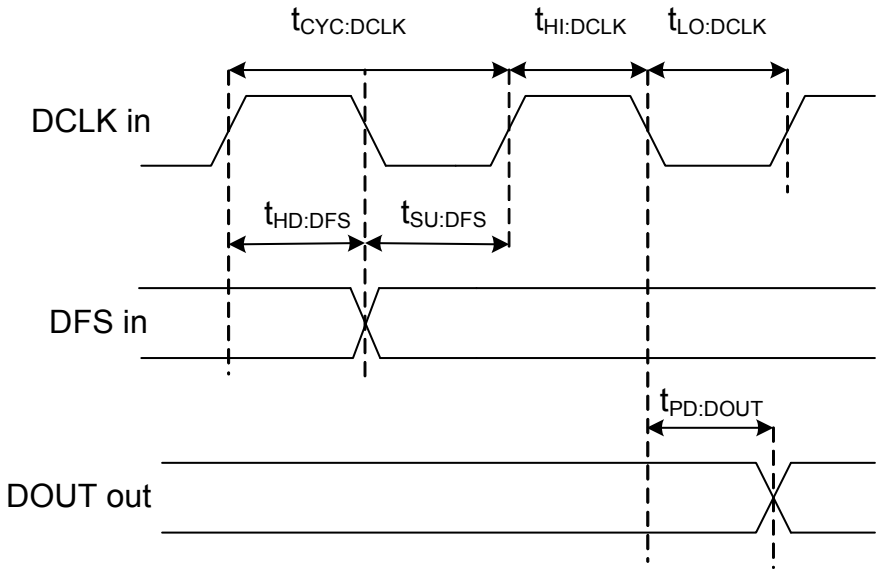


Figure 1. Digital Audio

Table 4. Digital Zero-IF I/Q Interface Characteristics (Si4777 Only)[1]

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
IQCLK Output Cycle Time	$t_{CYC:IQCLK}$		0.8 x per	per[2]	1.2 x per	ns
IQCLK Output Pulse Width High	$t_{HI:IQCLK}$		0.22 x per	—	0.59 x per	ns
IQCLK Output Pulse Width Low	$t_{LO:IQCLK}$		0.41 x per	—	0.78 x per	ns
IQFS Output Delay	$t_{PD:IQFS}$		0	—	(0.5 x per) + 18	ns
IQFS Output Setup to IQCLK Rise[3]	$t_{SU:IQFS}$		(0.5 x per) – 18	—	—	ns
IOUT Output Delay	$t_{PD:IOUT}$		0	—	(0.5 x per) + 18	ns
QOUT Output Delay	$t_{PD:QOUT}$		0	—	(0.5 x per) + 18	ns
IOUT Output Setup to IQCLK rise[3]	$t_{SU:IOUT}$		(0.5 x per) – 18	—	—	ns
QOUT Output Setup to IQCLK Rise[3]	$t_{SU:QOUT}$		(0.5 x per) – 18	—	—	ns

Notes:
1. Guaranteed by characterization.
2. per is the IQCLK I/Q bit clock period. Refer to Table 15 on page 35 for IQCLK bit clock frequencies.
3. Minimum time the Si4770/77-A20 will produce between valid output and the next rising edge of IQCLK

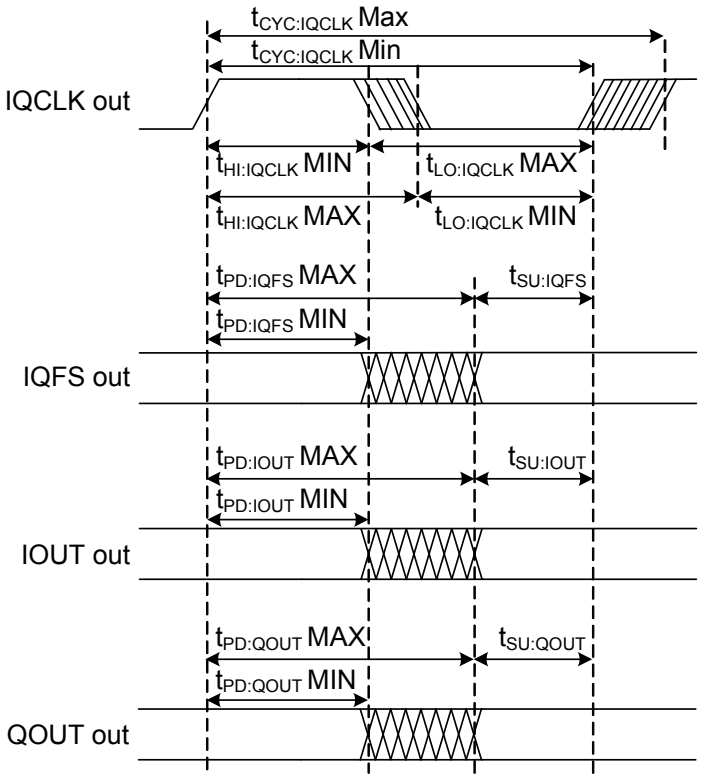


Figure 2. Digital Zero-IF I/Q

Table 5. Reference Clock and Crystal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reference Clock, Pin RCLK						
RCLK Supported Frequencies			—	36.4 37.8 37.209375	—	MHz
RCLK Frequency Tolerance			–100	—	100	ppm
RCLK = 36.4 MHz, 37.8 MHz, 37.209375 MHz						
Phase Noise		100 Hz offset	—	—	–86	dBc/Hz
		1 kHz offset	—	—	–101	dBc/Hz
		10 kHz offset	—	—	–108	dBc/Hz
		≥ 100 kHz offset	—	—	–122	dBc/Hz
Input Capacitance			—	7	—	pF
Input Voltage		AC coupling capacitor = 1 µF Square wave input			400	mV_{PP}
		AC coupling capacitor = 1 µF Sine wave input	300	—	900	mV_{PP}
Crystal Oscillator, Pins XTAL1, XTAL2						
Crystal Frequency			—	36.4 37.8 37.209375	—	MHz
Crystal Frequency Tolerance			–100	—	100	ppm
Load Capacitance, Programmable, Each Pin to GND			5	—	21.8	pF

Table 6. I²C Control Interface Characteristics

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Pins SCL, SDA						
SCL Frequency	f_{SCL}		0	—	400	kHz
SCL Low Time	t_{LOW}		1.3	—	—	µs
SCL High Time	t_{HIGH}		0.6	—	—	µs
SCL Input to SDA ↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCL Input from SDA ↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDA Input to SCL ↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDA Input from SCL ↓ Hold	$t_{HD:DAT}$		0	—	900	ns
SDA Output Delay	$t_{PD:DAT}$		300	—	900	ns
SCL Input to SDA ↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDA Output Fall Time	$t_{f:OUT}$		$20 + 0.1\frac{C_B}{1pF}$	—	250	ns
SDA Input, SCL Rise/Fall Time	$t_{f:IN}$, $t_{r:IN}$		$20 + 0.1\frac{C_B}{1pF}$	—	300	ns
Capacitive Loading	C_B		—	—	50	pF
Pulse Width Rejected by Input Filter	t_{SP}		—	—	50	ns

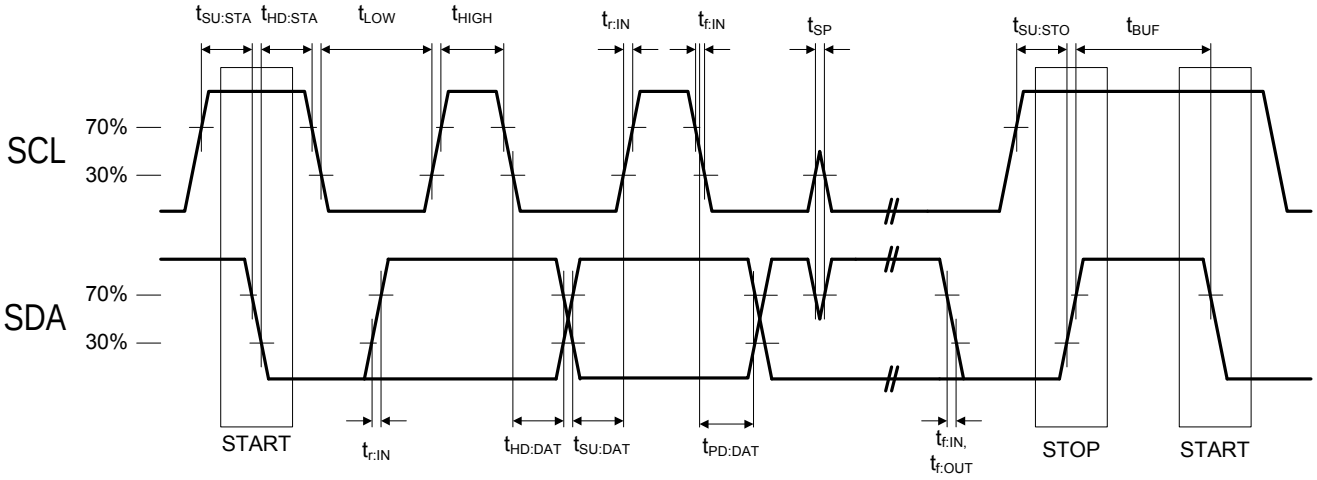


Figure 3. I²C Control Interface Read and Write Timing Parameters

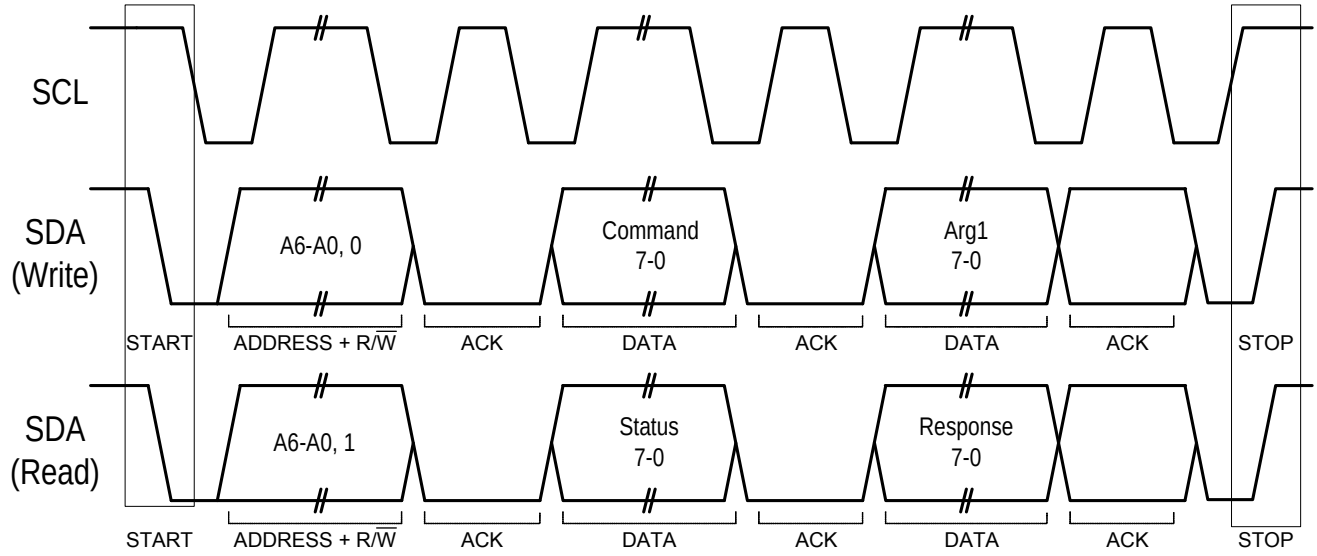


Figure 4. I²C Control Interface Read and Write Timing Diagram

Table 7. FM Receiver Characteristics

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V. Typical values measured at T_{AMB} = 25 °C, FM modulation (L = R), F_{MOD} = 1 kHz, F_{DEV} = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and F_{RF} = 98 MHz in application circuit unless otherwise specified)

Parameter	Test Condition	Min	Typ	Max	Unit
Input Frequency		64	—	108	MHz
Frequency Step Resolution		10	—	200	kHz
Powerup Time[1,2]	RCLK or Crystal = 36.4 MHz, 37.8 MHz, 37.209375 MHz	—	—	100	ms
Tune time[1]		—	1.5	—	ms
Seek Time/Channel[1]	At LOUT and ROUT pins	—	20	—	ms
Max Frequency Deviation[1]	Audio THD <1%, over-deviation handling enabled	—	150	—	kHz
RF AGC Range		—	40	—	dB
AGC Gain Resolution[3]		—	2	—	dB
RF AGC Threshold Accuracy[3]			2	—	dB
IF AGC Threshold Accuracy[3]			1	—	dB
Following FM Receiver Specifications Refer to Si4770/77-A20 Application Circuit Input					
IP3[6]	Blockers at 400/800 kHz offset AGC disabled (Max RF gain)	115	117	—	dBµV
Sensitivity[6]	Audio SINAD = 26 dB AGC disabled (Max RF gain)	—	–3.5	–2	dBµV
Image Rejection[1]	Deviation = 22.5 kHz	65	70	—	dB
Adjacent Channel Rejection[1,6]	Audio SINAD = 26 dB Desired = 40dBµV, F_{MOD} = 1 kHz, F_{DEV} = 22.5 kHz Undesired at ±100 kHz offset, F_{MOD} = 400 Hz, F_{DEV} = 22.5 kHz	63	65	—	dB

Notes:

1. Guaranteed by characterization.
2. Measured at T_{AMB} = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

Table 7. FM Receiver Characteristics (Continued)

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V. Typical values measured at T_{AMB} = 25 °C, FM modulation (L = R), F_{MOD} = 1 kHz, F_{DEV} = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and F_{RF} = 98 MHz in application circuit unless otherwise specified)

Parameter	Test Condition	Min	Typ	Max	Unit
Alternate Channel Rejection[6]	Audio SINAD = 26 dB Desired = 40 dBµV, F_{MOD} = 1 kHz, F_{DEV} = 22.5 kHz Undesired at ±200 kHz offset, F_{MOD} = 400 Hz, F_{DEV} = 22.5 kHz	65	72	—	dB
THD	F_{DEV} = 75 kHz	—	0.05	0.1	%
Mono (S+N)/N[6]		66	75	—	dB
Stereo (S+N)/N[6]	Stereo modulation (L = 1, R = 0), deviation = 67.5 kHz, pilot deviation = 6.75 kHz	64	70	—	dB
AM Suppression[1]	AM: m = 0.3/Fmod = 1 kHz, RF level = 60 dBµV	50	55	—	dB
De-Emphasis Time Constant[3]		70	75	80	µsec
		45	50	54	µsec
L/R Imbalance	Deviation = 75 kHz	–1	—	1	dB
Stereo Separation	Stereo modulation (L = 1, R = 0), Deviation = 67.5 kHz, pilot deviation = 6.75 kHz	40	43	—	dB
Stereo THD	Stereo modulation (L = 1, R = 0), Deviation = 67.5 kHz, pilot deviation = 6.75 kHz	—	0.1	0.2	%
Pilot Signal Rejection[1]	Stereo modulation (L = 1, R = 0), Deviation = 67.5 kHz, pilot deviation = 6.75 kHz	—	55	—	dB
RDS Sensitivity[1]	∆f = 2 kHz, RDS BLER < 5%	—	13	14.5	dBµV
RDS Synchronization Time[1]	∆f = 2 kHz RF input = 60 dBµV	—	70	—	ms
RDS PI Lock Time[1]	∆f = 2 kHz RF input = 60 dBµV	—	85	—	ms

Notes:

1. Guaranteed by characterization.
2. Measured at T_{AMB} = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

Table 7. FM Receiver Characteristics (Continued)

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V. Typical values measured at T_{AMB} = 25 °C, FM modulation (L = R), F_{MOD} = 1 kHz, F_{DEV} = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and F_{RF} = 98 MHz in application circuit unless otherwise specified)

Parameter	Test Condition	Min	Typ	Max	Unit
FM Mixer Inputs: Pins FMXIP, FMXIN					
Maximum RF Input Voltage[3]	1 dB compression point of mixer	—	112	—	dBµV
Mixer Input Resistance[3]		—	8	—	kΩ
Mixer Input Capacitance[3]		—	6	—	pF
IP3[4,5,6]	Blockers at 400/800 kHz offset, Max Gain (AGC disabled)	—	123	—	dBµV
Sensitivity[5,6]	Audio SINAD = 26 dB Max Gain (AGC disabled)	—	3.5	—	dBµV
FM Resistor Banks: FMAGC1, FMAGC2					
FMAGC1 Min		—	2.5	—	Ω
FMAGC1 Max		—	800	—	Ω
FMAGC1 Step Size	Maximum parallel resistance change	—	800	—	Ω
FMAGC2 Min		—	2.5	—	Ω
FMAGC2 Max		—	800	—	Ω
FMAGC2 Step Size	Maximum parallel resistance change	—	800	—	Ω
FM LNA: Pins FMI, FMO					
Single Receiver Mode					
FMI Input Resistance[3,7]		—	50	—	Ω
FMI Input Capacitance[3]		—	2	—	pF
FMI Return Loss[3]	64 MHz < F < 108 MHz	—	15	—	dB
FMI Input Referred Noise[3]		—	0.73	—	$nV/\sqrt{Hz}$
FMI LNA IP3[3,8]	Blockers at 400/800 kHz offset, Max Gain	—	128	—	dBµV

Notes:

1. Guaranteed by characterization.
2. Measured at T_{AMB} = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

Table 7. FM Receiver Characteristics (Continued)

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V. Typical values measured at T_{AMB} = 25 °C, FM modulation (L = R), F_{MOD} = 1 kHz, F_{DEV} = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and F_{RF} = 98 MHz in application circuit unless otherwise specified)

Parameter	Test Condition	Min	Typ	Max	Unit
FMO Output Resistance[3]	Nominal FMI to FMO gain = 8 dB, Source load = 50 Ω	—	125	—	Ω
FMO Output Capacitance[3]		—	2	—	pF
Dual Receiver Mode					
FMI Input Resistance[7,3]		—	100	—	Ω
FMI Input Capacitance[3]		—	1.5	—	pF
FMI Return Loss[3]	64 MHz < F < 108 MHz	—	15	—	dB
FMI Input Referred Noise[3]		—	1.20	—	nV/$\sqrt{\text{Hz}}$
FMI LNA IP3[3,8]	Blockers at 400/800 kHz offset, Max Gain	—	126	—	dBµV
FMO Output Resistance[3]	Nominal FMI to FMO gain = 8dB, Source load = 50 Ω	—	250	—	Ω
FMO Output Capacitance[3]		—	2	—	pF
Audio Outputs: Pins LOUT and ROUT					
Audio Frequency Response Low[1,2]	±3 dB	—	—	30	Hz
Audio Frequency Response High[1,2]	±3 dB	15	—	—	kHz
Output Load Resistance[3]	At LOUT and ROUT pins	10 k	—	—	Ω
Output Load Capacitance[3]	At LOUT and ROUT pins	—	—	50	pF
Output Voltage	Deviation = 22.5 kHz	99	112	125	mVRMS
Power Supply Rejection Ratio (PSRR)[3]	100 Hz ripple on power supply lines. Ripple voltage = 100 mV_{PP} of power supply voltage	—	45	—	dB

Notes:

1. Guaranteed by characterization.
2. Measured at T_{AMB} = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

Table 7. FM Receiver Characteristics (Continued)

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V. Typical values measured at T_{AMB} = 25 °C, FM modulation (L = R), F_{MOD} = 1 kHz, F_{DEV} = 22.5 kHz, Deemphasis = 75 µsec, RF level = 60 dBµV, and F_{RF} = 98 MHz in application circuit unless otherwise specified)

Parameter	Test Condition	Min	Typ	Max	Unit
FM MPX Output: Pins MPXOUT					
Output Voltage[1]	F_{RF} = 83 MHz, RF level = 65 dBµV, F_{DEV} = 3 kHz, F_{MOD} = 76 kHz unless otherwise noted	14	16	—	mVRMS
Output Load Resistance[3]		—	10	—	kΩ
Output Load Capacitance[3]		—	50	—	pF
PSRR[3]	100 Hz ripple on power supply lines. Ripple voltage = 100 mV_{PP} of power supply voltage	—	45	—	dB
Bandwidth[1]		110	—	—	kHz
Following FM MPX Specifications Refer to Si4770/77-A20 Application Circuit					
(S+N)/N[1,11]	F_{RF} = 83 MHz, RF level = 65 dBµV, F_{DEV} = 3 kHz, F_{MOD} = 76 kHz unless otherwise noted	25	30	—	dB
Sensitivity[1,11]	F_{RF} = 83 MHz, F_{DEV} = 3 kHz, F_{MOD} = 76 kHz unless otherwise noted, SINAD = 5 dB	—	19	25	dBµV

Notes:

1. Guaranteed by characterization.
2. Measured at T_{AMB} = 25 °C.
3. Guaranteed by design.
4. IP3 measured at the FMXIP and FMXIN pins reflects IP3 for mixer stage and all subsequent downstream blocks.
5. Refer to FM test circuit in Figure 5.
6. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
7. Input resistance is software configurable.
8. IP3 measured at the FMI input pin reflects IP3 for FMI LNA stage.
9. RDS Synchronization Persistence is the minimum RF level at which the tuner loses synchronization to the RDS PI code as the RF level decreases from high to low levels.
10. RDS Synchronization Stability is the minimum RF level at which the tuner achieves synchronization to the RDS PI code as the RF level increases from low to high levels.
11. Noise integrated from 30 Hz to 120 kHz for audio SINAD and SNR measurements.

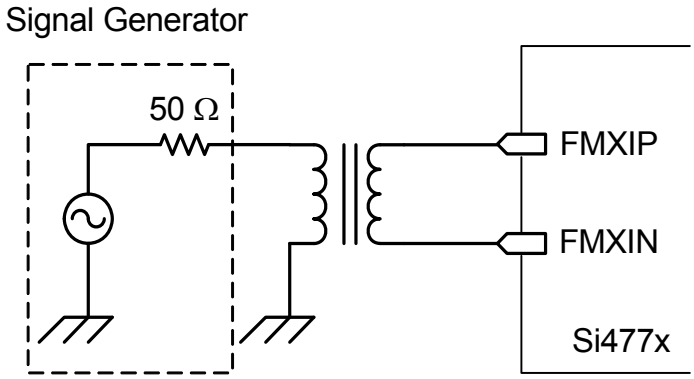


Figure 5. FM Test Circuit for Mixer Input IP3 and Sensitivity Measurement

Table 8. AM Receiver Characteristics

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V. Typical values measured at T_{AMB} = 25 °C, AM modulation = 30%, F_{MOD} = 1 kHz, RF level = 74 dBµV, and F_{RF} = 1 MHz unless otherwise specified)

Parameter	Test Condition	Min	Typ	Max	Unit
Input Frequency		520	—	1710	kHz
Frequency Step Resolution		1	—	10	kHz
Powerup Time[1,2]	RCLK or Crystal = 36.4 MHz, 37.8 MHz, 37.209375 MHz	—	—	100	ms
Tune Time[1]		—	15	—	ms
Seek Time/Channel[1]	At LOUT and ROUT pins	—	55	—	ms
Maximum RF Input Voltage[1,2]	Mod = 90%, Fmod = 1 kHz, SINAD = 57 dB	—	93	—	dBµV
Image Rejection[1,3]		68	72	—	dB
Adjacent Channel Rejection[1,3]	SINAD = 20 dB Desired = 40 dBµV, F_{MOD} = 1 kHz, MOD = 30% Undesired at ±9 kHz offset, F_{MOD} = 400 Hz, MOD = 30%	57	62	—	dB
Alternate Channel Rejection[1,3]	SINAD = 20 dB Desired = 40dBµV, F_{MOD} = 1 kHz, MOD = 30% Undesired at ±18 kHz offset, F_{MOD} = 400 Hz, MOD = 30%	59	62	—	dB
IP3[1,3]	Blockers at 40/80 kHz, AGC disabled (Max gain)	110	120	—	dBµV

Notes:
1. Guaranteed by characterization.
2. Measured at T_{AMB} = 25 °C.
3. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
4. Guaranteed by design.

Table 8. AM Receiver Characteristics (Continued)

(T_{AMB} = –40 to 85 °C, V_A = 4.5 to 5.5 V, V_D = 2.7 to 3.6 V, V_{IO1} = 1.7 to 3.6 V, V_{IO2} = 1.2 to 3.6 V. Typical values measured at T_{AMB} = 25 °C, AM modulation = 30%, F_{MOD} = 1 kHz, RF level = 74 dBµV, and F_{RF} = 1 MHz unless otherwise specified)

Parameter	Test Condition	Min	Typ	Max	Unit
IP2[1,3]	Desired = 700 kHz, Undesired = 1000 kHz, 1700 kHz AGC disabled (Max gain)	142	146	—	dBµV
RF AGC Range		—	50	—	dB
AGC Step Resolution			2		dB
RF AGC Threshold Accuracy[4]		—	2	—	dB
IF AGC Threshold Accuracy[4]		—	2	—	dB
Sensitivity[1,3]	SINAD = 20 dB, AGC Disabled (Max RF Gain)	—	14	17	dBµV EMF
THD[1,3]	Mod = 30%	—	0.1	—	%
	Mod = 90%	—	0.2	—	%
Audio SNR[1,3]	Mod = 30%	60	65	—	dB
Antenna Inductance[3]		180	—	540	µH
Audio Outputs: Pins LOUT and ROUT					
Audio Output Resistance Load[4]		10k	—	—	Ω
Audio Output Capacitance Load[4]	Single Ended	—	—	50	pF
Audio Output Voltage		96	108	121	mVRMS
PSRR at Audio Output Pins[4]	Ripple test should be for 100 Hz ripple on power supply lines Ripple voltage = 100 mV_{PP} of power supply voltage	—	45	—	dB

Notes:
1. Guaranteed by characterization.
2. Measured at T_{AMB} = 25 °C.
3. No A-weighting. Noise integrated from 30 Hz to 15 kHz for audio SINAD and SNR measurements.
4. Guaranteed by design.

Table 9. Thermal Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Ambient Temperature	T_{AMB}	—	–40	25	85	°C
Junction Temperature	T_J	—	—	—	115	°C
Delta from Junction to Ambient*	θ_{JA}	—	—	27	—	°C/W

***Note:** The θ_{JA} is layout-dependent, and, therefore, PCB layout must provide adequate heat-sink capability. The θ_{JA} is specified assuming adequate ground plane.

Table 10. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Analog Supply Voltage	V_A	–0.5	5.9	V
Digital Supply Voltage	V_D	–0.5	3.9	V
I/O 1 Supply Voltage	V_{IO1}	–0.5	3.9	V
I/O 2 Supply Voltage	V_{IO2}	–0.5	3.9	V
I/O 1 Input Current[2]	I_{IN1}	–10	10	µA
I/O 1 Input Voltage[2]	V_{IN1}	–0.3	V_{I01} + 0.3	V
I/O 2 Input Current[3]	I_{IN2}	–10	10	µA
I/O 2 Input Voltage[3]	V_{IN2}	–0.3	V_{I02} + 0.3	V
Operating Temperature	T_{OP}	–40	95	°C
Storage Temperature	T_{STG}	–55	150	°C
AM RF Input Level[4]	V_{RFIN}	–1	V_A + 1	V
AM RF Input Current[4]	I_{RFIN}	–100	100	mA
FM RF Input Level[5]	V_{RFIN}	–1	1	V
FM RF Input Current[5]	I_{RFIN}	–100	100	mA
HBM ESD	V_{HBM}	–2	2	kV
MM ESD	V_{MM}	–200	200	V
CDM ESD[6]	V_{CDM}	–500	500	V
CDM ESD[7]	V_{CDM}	–750	750	V

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. For input pins SCL, SDA, RSTB, A0, A1, GPIO1, GPIO2.
3. For input pins DCLK and DFS.
4. At RF input pins AM1.
5. At RF input pins FMXIN, FMXIP, FMI, FMAGC1, FMAGC2.
6. All pins.
7. Corner pins.

2. Typical Application Schematic

Figure 6 shows the proposed application schematic.

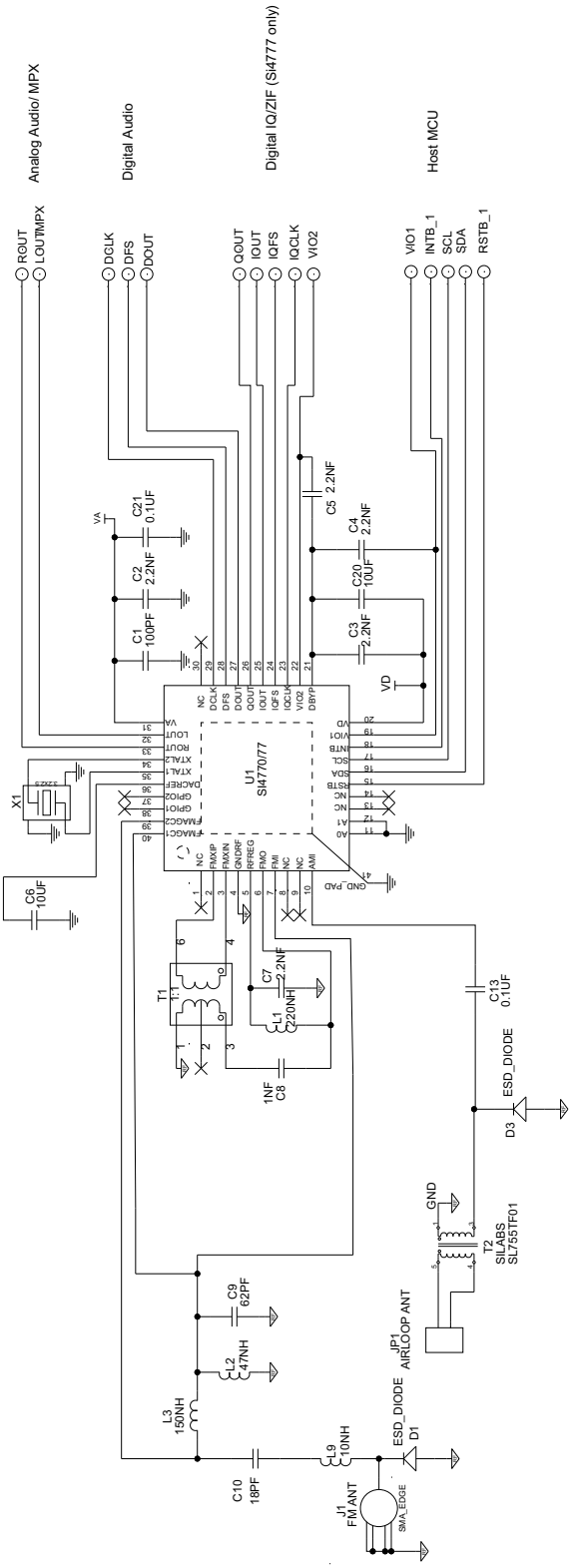


Figure 6. Application Circuit

3. Bill of Materials

Table 11. Si4770/77-A20 Bill of Materials

Item	Qty	Ref	Package	Value	Mfr	Part Number
1	1	T2	Transformer, Thru-hole		Silicon Laboratories	SL755TF01
2	1	T1	BALUN, 1:1, Toko		Toko	458PT1566
3	2	C13, C21	CAP, SM, 0402	0.1 µF	Murata	GRM155R71A204KA01D
5	1	C1	CAP, SM, 0402	100 pF	Murata	GRM1555C1H101JZ01
6	1	C10	CAP, SM, 0402	18 pF	Murata	GRM1555C1H180JZ01
7	1	C8	CAP, SM, 0402	1 nF	Murata	GRM155R61H102KA01
8	5	C2, C3, C4, C5, C7	CAP, SM, 0402	2.2 nF	Murata	GRM155R71H222KA01
9	1	C9	CAP, SM, 0402	62 pF	Murata	GRM1555C1H620JD01
10	2	C6, C20	CAP, SM, 0603	10 µF	Digikey	490-3896-2-ND
11	1	J1	CONN, SMA, Edgemount		AEP Connectors	
12	1	JP1	CONN, TH, HEADER, .100 PITCH,1X2		Samtec	HTSW-101-07-G-D
13	2	D1, D3	ESD Protector, SM		TE Connectivity	PESD0402-140
14	1	U1	IC, SM, Si4770/77-A20, QFN40		Silicon Laboratories	Si4770/77
15	1	L9	IND, SM, 0603	10 nH	Murata	
16	1	L3	IND, SM, 0603	150 nH	Murata	LQW18ANR15G00
17	1	L1	IND, SM, 0603	220 nH	Murata	LQW18ANR22G00
18	1	L2	IND, SM, 0603	47 nH	Murata	LQW18AN47NG00
21	1	X1	XTAL, SM, 3.2 x 2.5 mm	See Table 12	See Table 12	See Table 12

Table 12. Crystal Options

Frequency (MHz)	Mfr	Series	P/N
36.400000	NDK	NX3225SA	EXS00A-CS02420
37.800000	NDK	NX3225SA	EXS00A-CS02421
37.209375	NDK	NX3225SA	EXS00A-CS02422
36.400000	TaiSaw	SMD 3.2x2.5 36.4 MHz Crystal Unit	TZ1514A
37.800000	TaiSaw	SMD 3.2x2.5 37.8 MHz Crystal Unit	TZ1517A
37.209375	TaiSaw	SMD 3.2x2.5 37.209375 MHz Crystal Unit	TZ1522A
36.400000	Jauch	JXE115	Q36,40-JAS32P4-12-10/20-T1-LF
37.800000	Jauch	JXE115	Q37,80-JAS32P4-12-10/20-T1-LF
37.209375	Jauch	JXE115	Q37,209375-JAS32P4-12-10/20-T1-LF
36.400000	Epson Toyocom	TSX-3225	OUTD-2B-0541
37.800000	Epson Toyocom	TSX-3225	OUTD-2B-0541
37.209375	Epson Toyocom	TSX-3225	OUTD-2B-0541

4. Functional Description

4.1. Overview

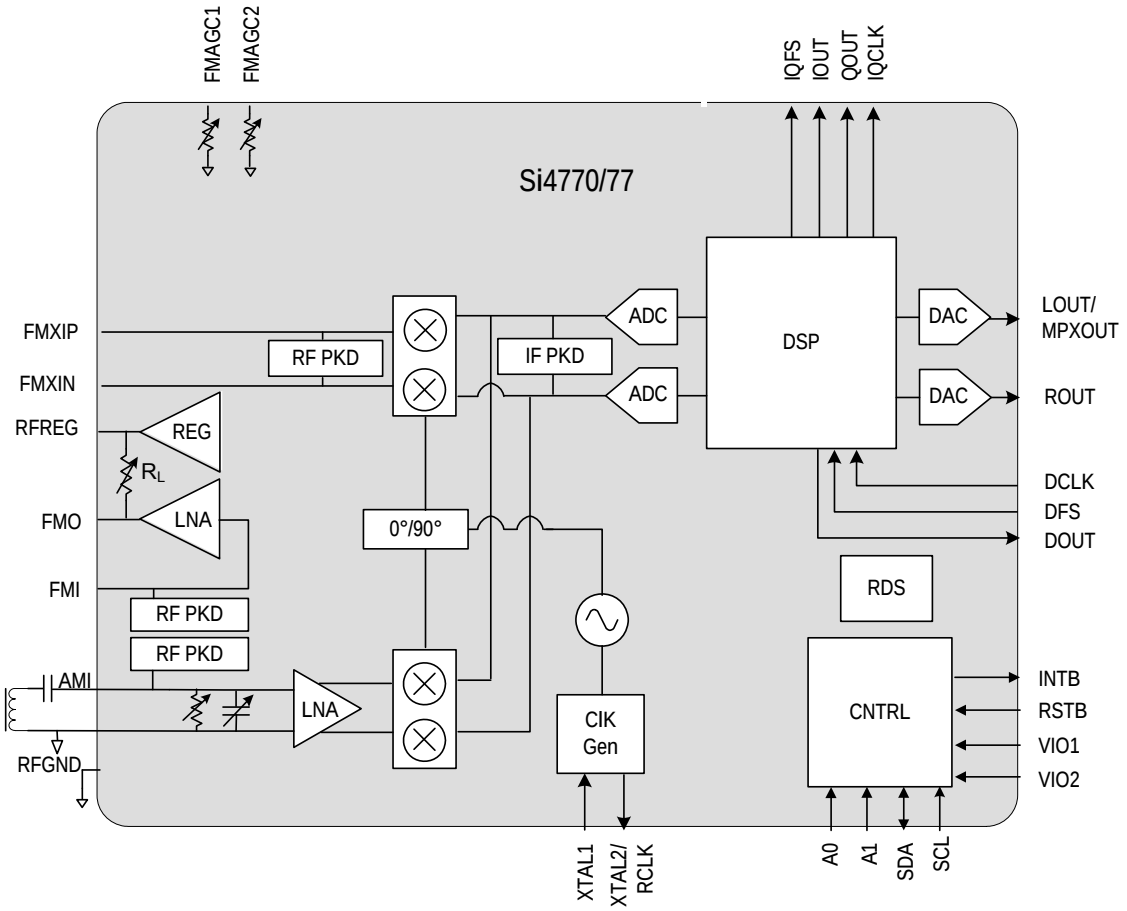


Figure 7. Si4770/77-A20 Block Diagram

The Si4770/77-A20 radio receiver family employs 100% RF CMOS technology to bring outstanding receiver performance to the consumer electronics industry. The Si4770/77-A20 receiver family supports worldwide radio reception. The Si4770/77-A20 incorporates a digital pre-processor for the European Radio Data System (RDS) and the North American Radio Broadcast Data System (RBDS) including all required symbol decoding, block synchronization, error detection, and error correction functions. The Si4777 supports AM/FM HD radio channel reception with digital (I^2S) Zero-IF (ZIF) I/Q outputs for interface to an HD radio processor.

The family leverages Silicon Laboratories' patented low-IF digital architecture, delivering superior RF performance and interference rejection. The low-IF architecture delivers superior performance while integrating the great majority of external components required by competing solutions.

The proven digital techniques provide excellent sensitivity in weak signal environments and superb selectivity and intermodulation immunity in strong signal environments. The solution offers dynamic AM/FM channel bandwidth control, auto-calibrated digital tuning, and proven AM/FM seek functionality based on multiple signal quality and band parameters. The family offers highly flexible and advanced audio processing including programmable softmute, FM stereo-mono blend, dynamic AM/FM channel bandwidth, AM/FM hi-cut, FM hi-blend, and AM lo-cut filters. In addition, the Si4770/77-A20 provides an integrated clock oscillator or accepts a reference clock and an I^2C-compatible, 2-wire control interface. The Si4770/77-A20 receiver system specifies a minimal bill of materials, resulting in a small board space requirement and making the solution ideal for any consumer electronics application from single tuner radios to multiple tuner radios.

Table 13. Part Number Descriptions

Part Number	Description	FM (64–108 MHz)	MW (520–1710 kHz)	RDS	Analog MPX (VICS/DARC)	IBOC Blend	Digital ZIF (HD/DRM)	Channel EQ	IR Cal
Si4770	AM/FM RDS, VICS	✓	✓	✓	✓			✓	✓
Si4777	AM/FM RDS, VICS, HD Tuner	✓	✓	✓	✓	✓	✓	✓	✓

4.2. Clocking

The Si4770/77-A20 generates all internal clocking from an external crystal using an on-chip oscillator or an external programmable reference clock. The reference clock of Si4770/77-A20 is a sinusoidal or rectangular clock provided by an external source on pin RCLK. The supported crystal and external clock source frequencies are selected frequencies in the 36–38 MHz range.

The power up command enables the selection of an external crystal or reference clock. The reference clock and/or crystal accuracy should be ±100 ppm. In a multi-receiver system, a single crystal can be shared between all Si4770/77-A20 receivers. The Si4770/77-A20 family features programmable loading capacitors for the on-chip crystal oscillator, eliminating external loading capacitors.

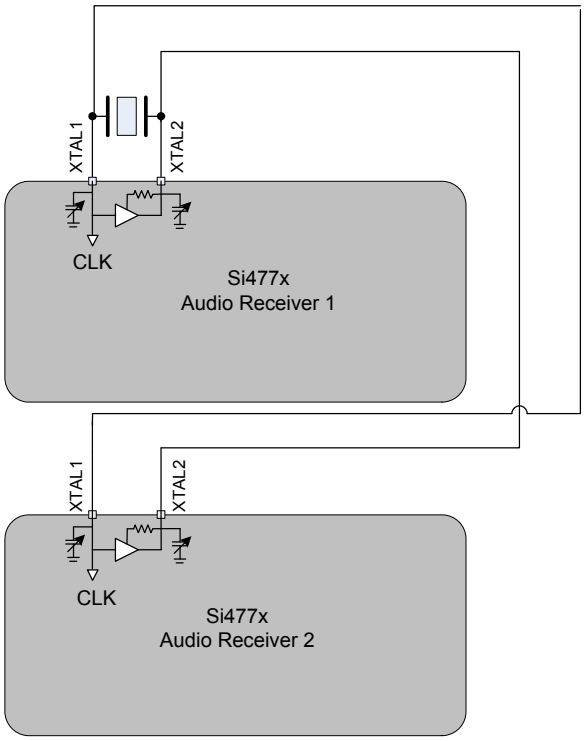


Figure 8. Xtal Share between Two Tuners

4.3. Tuning

The Si4770/77-A20 includes a complete on-chip PLL-VCO frequency synthesizer to generate the quadrature LO input to the image-reject AM and FM mixers. The Si4770/77-A20 employs a single-conversion mix (down conversion) to a fixed low IF center frequency. An innovative high-performance image reject mixer architecture allows for IF center frequencies below 300 kHz, thereby eliminating ceramic filters required in 10.7 MHz IF tuner architectures. The tune command automatically programs the LO frequency to the center of the desired channel plus (minus) the output center IF frequency when using a high-side (low-side) mix. The Si4770/77-A20 supports 50, 100, or 200 kHz channel spacing for FM, 9 or 10 kHz for AM.

4.4. FM Receiver Front-End

The Si4770/77-A20 provides a very flexible front-end interface to accommodate a wide range of applications from cost-sensitive to high-performance.

An advanced AGC on the Si4770/77-A20 is implemented with the use of internal RF peak and IF peak detectors with programmable thresholds (trip points). The AGC adjusts the resistor values automatically. Attack and release rates for the AGC are programmable, providing flexible fast attack and slow release AGC performance.

For cost-effective performance and superior FM sensitivity, the antenna output can be received on the FMI pin (Figure 9). The FM band can be received on the FMI pin via an input coupling network. This input coupling network isolates the FM band for best performance. An internal LNA provides gain for the signal. The LNA output is routed externally to the FM mixer input pins. The LNA gain is regulated with an internal voltage regulator supply via an internal resistor bank, R_L. The AGC circuit automatically controls the LNA gain, resistor banks FMAGC1, FMAGC2, and R_L to optimize sensitivity and strong signal handling.

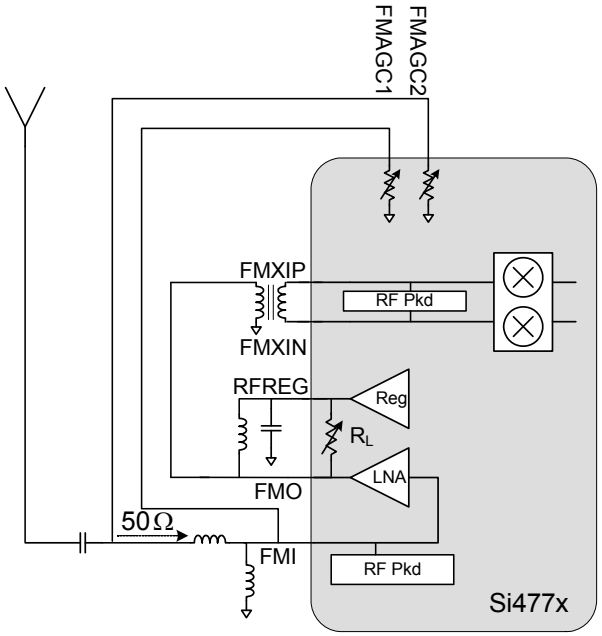


Figure 9. Conceptual Illustration of the Use of the FMI LNA for Cost-Optimized and Superior FM Sensitivity Performance

Cost can be further reduced by eliminating the 1:1 balun and directly interfacing the signal to the FM mixer by programming the mixer for single-ended input mode (Figure 10). The trade-off is a drop in linearity of 6 dBµV in IP3.

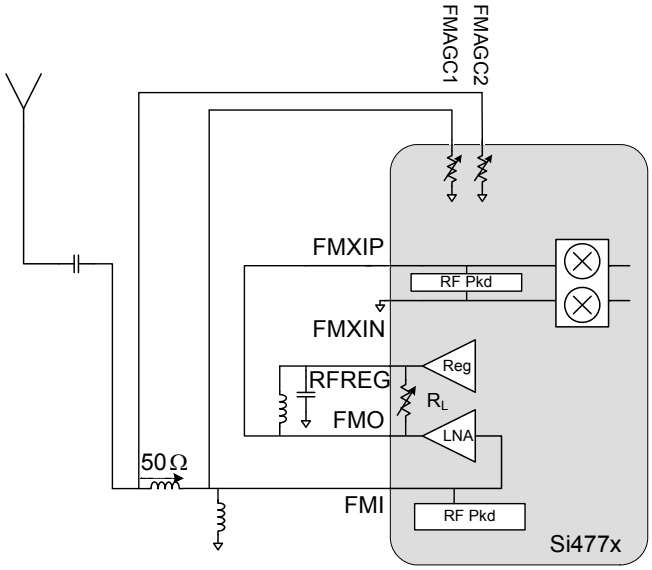


Figure 10. Conceptual Illustration of the Lowest-Cost Configuration

4.4.1. FMI LNA for FM Loop-Through Usage

In dual receiver applications, two receivers (Figure 11) can be attached to a single antenna. The dual receiver solution allows for independent radio station listening in different rooms.

The FMI LNA input impedance is software-configurable and provides two options: 50 Ω and 100 Ω. Configuring the input impedance for 100 Ω facilitates a Si4770/77-A20 receiver 1 and the Si4770/77-A20 receiver 2 to be interfaced to the antenna output in parallel, providing a matched 50 Ω input impedance. AGC is coordinated between both receivers whereby the resistor banks, FMAGC1, FMAGC2, and R_L, from one receiver are used to optimize sensitivity and strong signal handling.

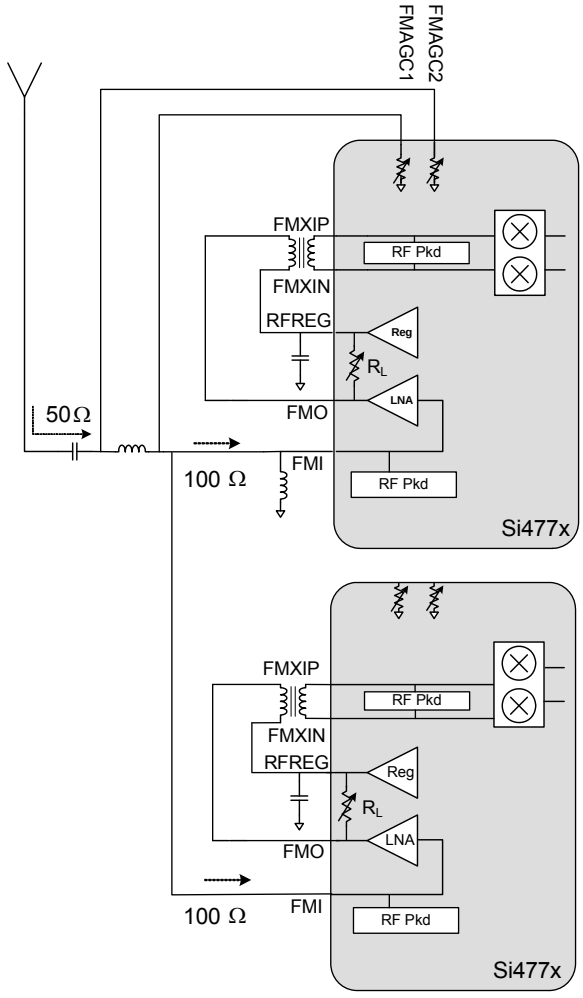


Figure 11. Conceptual Illustration of Si4770/77-A20 Receivers Interfaced to a Single Antenna Using the FMI LNA in Loop-Through Mode

4.5. AM Receiver Front-End

The Si4770/77-A20 contains an integrated LNA, providing an AM receive chain from antenna to audio out. There are few external components and no manual alignment required. The AM signal is received on the AMI pin. An advanced AGC on the Si4770/77-A20 is implemented with the use of internal RF peak and IF peak detectors with programmable thresholds (trip points). Attack and release rates for the AGC are programmable providing flexible fast attack and slow release AGC performance.

The Si4770/77-A20 provides highly-accurate digital AM tuning without factory adjustments. To offer maximum flexibility, the receiver supports a wide range of ferrite loop sticks from 180~688 µH. An air loop antenna is supported by using a transformer to increase the effective inductance of the air loop. Using a 1:5 turn ratio inductor, the inductance is increased by 25 times and easily supports all typical AM air loop antennas which generally vary between 10 and 20 µH.

4.6. Received Signal Qualifiers

A tuned signal's quality can vary with the environmental conditions, time of day, and geographical location among many other factors. To adequately manage the audio output and avoid unpleasant audible effects to the end-user, the Si4770/77-A20 monitors and provides indicators of signal quality, allowing the on-chip DSP and host processor (if required) to perform signal processing. The Si4770/77-A20 monitors and reports a set of industry-standard signal quality metrics including on-channel RSSI, adjacent channel RSSI (100 kHz and 200 kHz), image RSSI, SNR, multi-path interference on FM signal, ultra-sonic noise, and FM pilot detection. As with other Si4770/77-A20 features, how these variables are used to improve audio performance can be left to the Silicon Labs on-chip algorithms (recommended), or they can be brought out for host-processor instructions.

4.7. Digital Audio Interface

The digital audio 3-pin interface consists of data serial lines containing audio data, a bit clock, and a word frame for left and right channel data. The digital audio interface operates in slave mode and supports five different audio data formats:

- I^2S Audio
- Left-Justified Audio
- Right-Justified Audio
- DSP Audio
- DSP Left-Justified Audio

4.7.1. Audio Data Formats

In I^2S format, by default the MSB is captured on the second rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is low, and the right channel is transferred when the DFS is high.

In Left-Justified format, by default, the MSB is captured on the first rising edge of DCLK following each DFS transition. The remaining bits of the word are sent in order, down to the LSB. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In Right-Justified format, by default, the LSB is captured on the last rising edge of DCLK in each valid DFS interval. The left channel is transferred first when the DFS is high, and the right channel is transferred when the DFS is low.

In DSP format, the DFS becomes a pulse with a width of one DCLK period. The left channel is transferred first, followed right away by the right channel. There are two options in transferring the digital audio data in DSP format; the MSB of the left channel can be transferred on the first rising edge of DCLK following the DFS pulse (left-justified DSP format) or on the second rising edge.

In all audio formats, depending on the word size, DCLK frequency, and sample rates, there may be unused DCLK cycles after the LSB of each word before the next DFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of DCLK via properties. The number of audio bits can be configured for 8, 16, 20, or 24 bits.

4.7.2. Audio Sample Rates

The device supports a number of industry-standard sampling rates including 32, 40, 44.1, and 48 kHz.

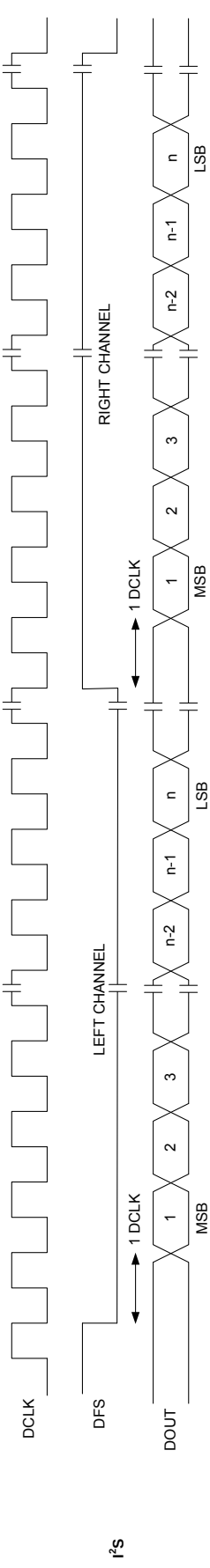


Figure 12. I²S Audio Format

Figure 13. Left-Justified Audio Format

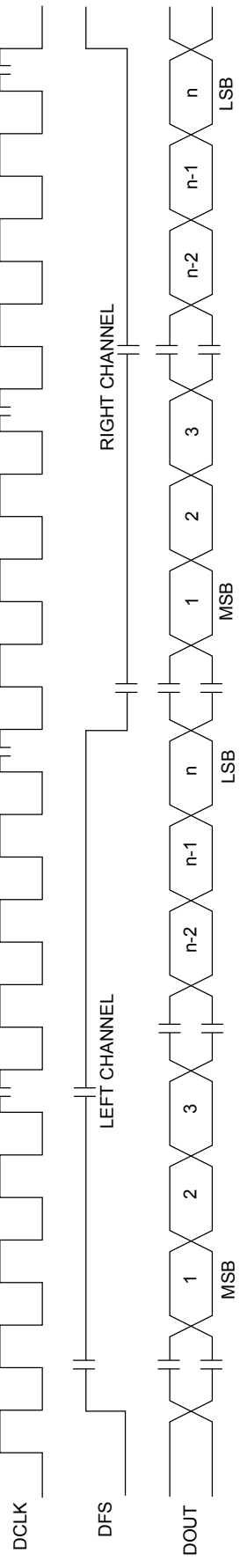


Figure 14. Right-Justified Audio Format

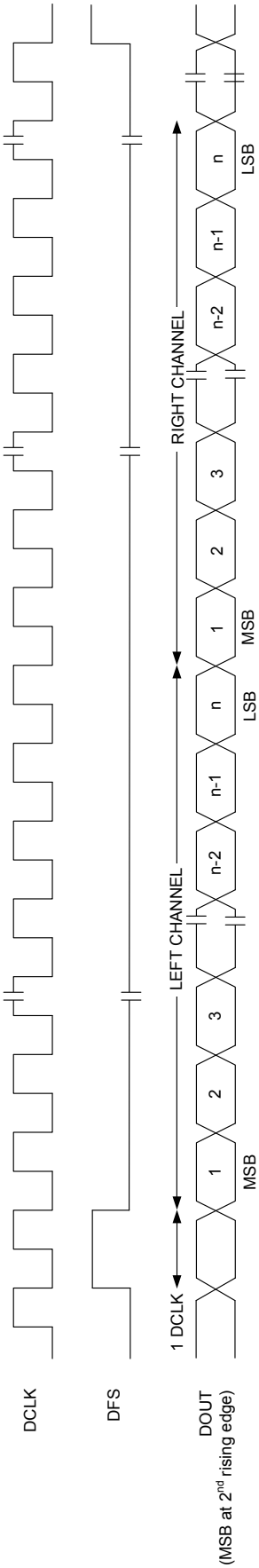


Figure 15. DSP Audio Format

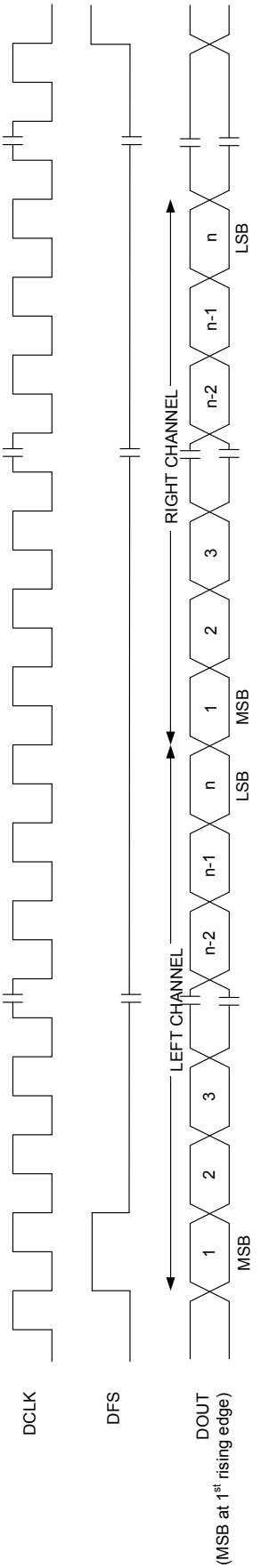


Figure 16. DSP Left-Justified Audio Format

4.8. Channel Equalizer

The Si4770/77-A20 supports advanced FM multi-path channel equalization. Multi-path interference results in fading of the FM signal at the receiver. Frequency selective fading causes different frequencies of an input signal to be attenuated and phase shifted differently in a channel. Frequency selective fading gives rise to notches in the frequency response of the channel. The Si4770/77-A20 channel equalizer performs blind equalization utilizing proprietary constant modulus algorithm (CMA) to restore the flat response of the channel.

4.9. Digital ZIF I/Q Interface (Si4777 Only)

The digital ZIF I/Q output can provide the down converted channelized AM/FM signal at baseband to a third-party processor for AM/FM HD radio processor for IBOC signal processing. The Si4777 provide a 500 kHz BW signal for FM IBOC signal processing and a 30 kHz BW signal for AM IBOC signal processing. The ZIF I/Q 4-pin interface consists of two data serial lines containing I and Q data, a bit clock, and a word frame for each data sample. The interface operates in master mode and supports five different data formats:

- I^2S ZIF
- Left-Justified ZIF
- Right-Justified ZIF
- DSP ZIF
- DSP Left-Justified ZIF

Table 14. ZIF I/Q Interface Description

Pin	Description
IOUT	16-bit baseband I word
QOUT	16-bit baseband Q word
IQFS	Word frame sync for I and Q words
IQCLK	Bit clock for I and Q data

4.9.1. ZIF I/Q Data Formats

In I^2S format, by default, the MSB is captured on the second rising edge of IQCLK following each IQFS transition. The remaining bits of the word are sent in order, down to the LSB.

In Left-Justified format, by default, the MSB is captured on the first rising edge of IQCLK following each IQFS transition. The remaining bits of the word are sent in order, down to the LSB.

In Right-Justified format, by default, the LSB is captured on the last rising edge of IQCLK in each valid IQFS interval.

In DSP format, the IQFS becomes a pulse with a width of 1 IQCLK period. There are two options in transferring the digital baseband I/Q data in DSP format: the MSB of I and Q data can be transferred on the first rising edge of IQCLK following the IQFS pulse (left-justified DSP format) or on the second rising edge.

In all data formats, depending on the word size, IQCLK frequency, and sample rates, there may be unused IQCLK cycles after the LSB of each word before the next IQFS transition and MSB of the next word. In addition, if preferred, the user can configure the MSB to be captured on the falling edge of IQCLK via properties. The number of baseband I/Q bits is configured for 16 bits.

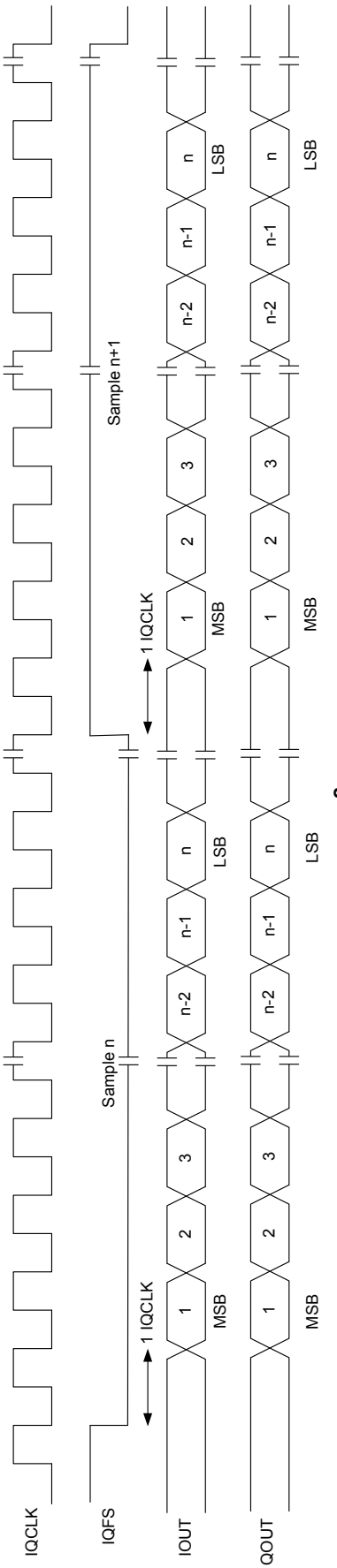


Figure 17. I²S ZIF Format

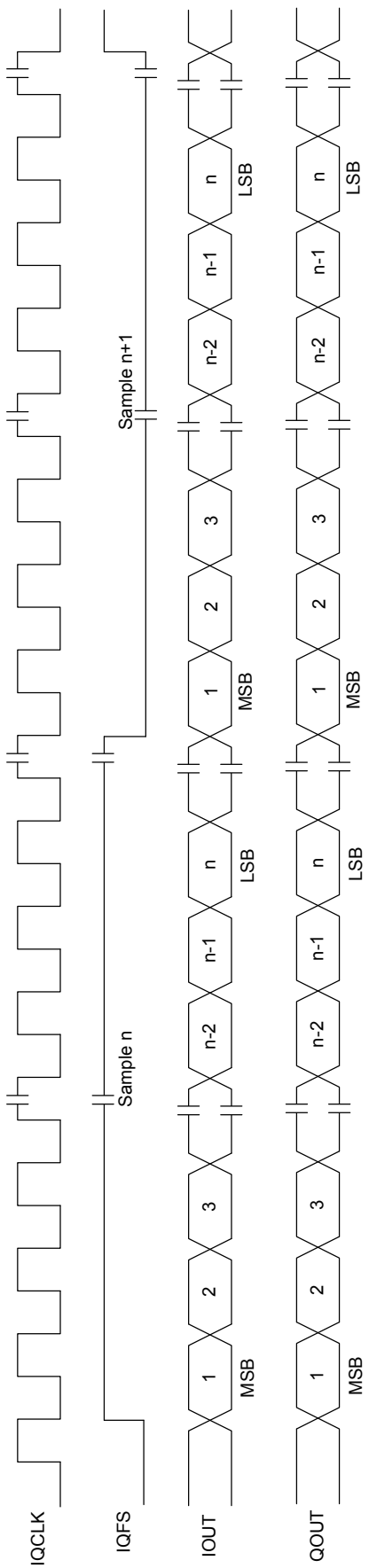


Figure 18. Left-Justified ZIF Format

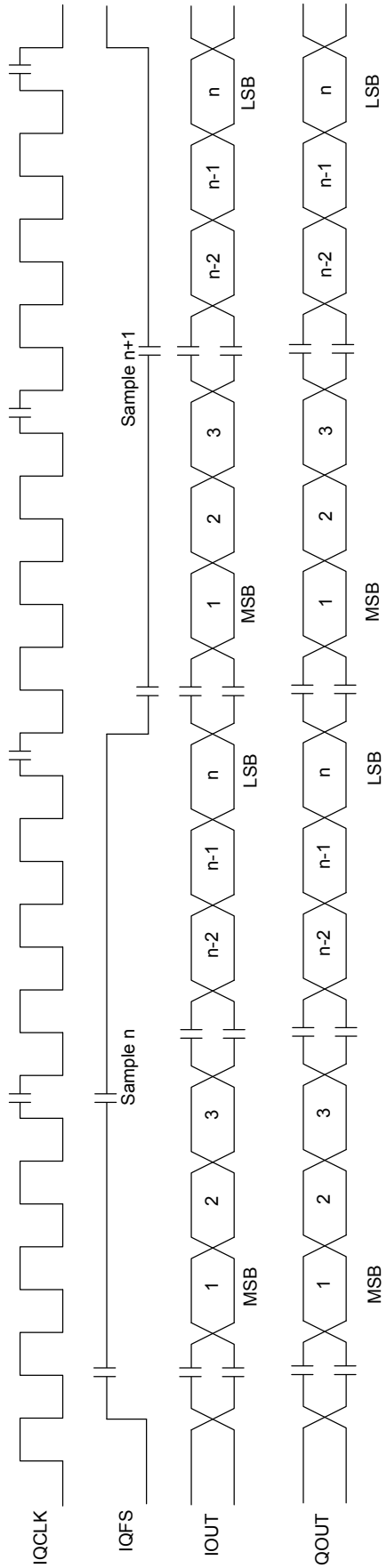


Figure 19. Right-Justified ZIF Format

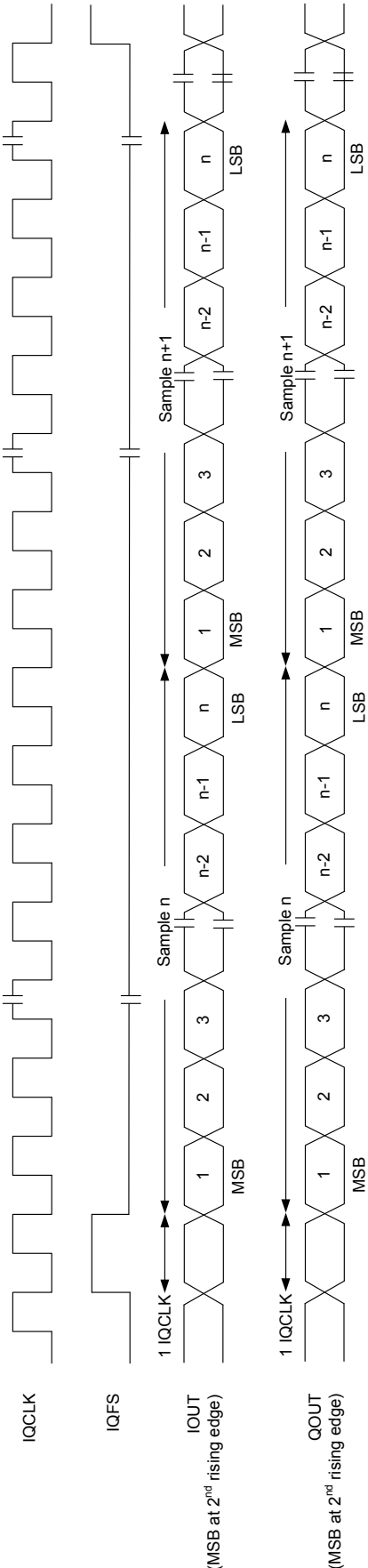


Figure 20. DSP ZIF Format

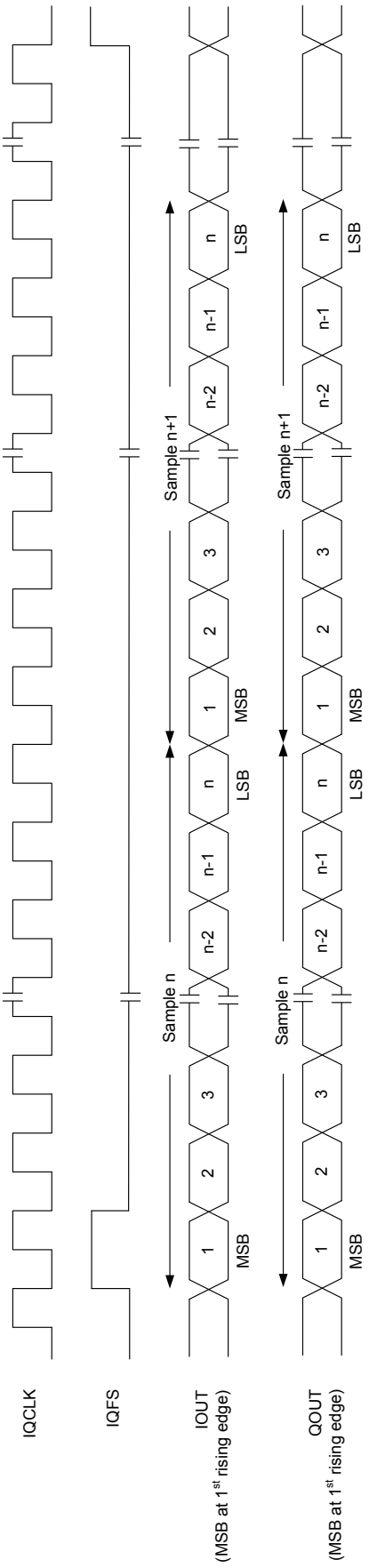


Figure 21. DSP Left-Justified ZIF Format

4.9.2. ZIF I/Q Sample Rates and Clocking Requirements

The device supports a number of industry-standard sampling rates including 650, 675, and 744.1875 kHz.

The external crystal and/or reference clock frequency must be the following to support the following ZIF I/Q samples rates for interface to an HD radio demodulator/decoder or DSP.

Table 15. Crystal/Reference Clock Frequency Requirements for the ZIF I/Q Sample Rates and Bit Clock Rates Supported

RCLK/XTAL Frequency (MHz)	IQFS ZIF I/Q Sample Rate (kHz)	IQCLK I/Q Bit Clock (MHz)	Broadcast Reception Modes
36.4000	650.0000	10.4000	AM/FM HD-Radio
	325.0000	5.2000	FM Analog
	40.6250	2.2750	AM Analog/HD-Radio
37.8000	675.0000	10.8000	AM/FM HD-Radio
	337.5000	5.4000	FM Analog
	42.1875	2.3625	AM Analog/HD-Radio
37.209375	744.1875	14.88375	AM/FM HD-Radio
	372.0938	7.4419	FM Analog
	46.5117	1.8605	AM Analog/HD-Radio

4.10. IBOC Blend Mode for HD Radio (Si4777 Only)

For HD-Radio reception IBOC blend is supported on the Si4777. This feature supports the ability to blend between analog and digital audio. When the bit error rate (BER) of the HD-Radio digital signal falls below a predefined threshold (set by the HD-Radio demodulator) and the digital audio fades out, the analog audio is blended in. This prevents the received audio from muting when the digital signal is lost. The audio will "blend to digital" upon reacquisition of the digital signal. Figure 22 illustrates the system implementation with a third party HD-Radio demodulator. ZIF I/Q data is output to the HD-Radio demodulator. The HD-Radio demodulator demodulates and decodes the received HD-Radio signal. It outputs digital audio (I^2S three-wire mode) to the Si4777 where the IBOC blend is performed. An on-chip asynchronous resampling converter (ASRC) allows the Si4777 to be slaved to the HD-Radio demodulator digital audio output at any sample rate from 32 kHz to 48 kHz.

The HD-R demodulator sends a 1-bit "BLEND" signal to the Silicon Labs tuner. When this signal is "1", the Si4777 initiates a crossover from full AM/FM analog audio into full HD-R audio following a time ramp at a programmable ramp rate. This process continues until HD-R audio is fully blended to analog or until the BLEND bit becomes a "0". When the BLEND bit is "0", the reverse crossover occurs (crossover from HD-R to AM/FM analog following a programmable ramp rate). This process continues until AM/FM is fully blended or until BLEND becomes "1".

The blended audio can be output on the analog output pins, LOUT and ROUT and/or a digital audio port to a third party audio DSP.

An on-chip asynchronous re-sampling converter (ASRC) allows the Si4777 to be slaved to the Audio DSP's digital frame sync and bit clock from 32 kHz to 48 kHz.

Audio level alignment and calibration is implemented in the Si4777 by multiplying the input HD-R audio signal by a scaling constant (determined at manufacturing time in the factory) and a dynamic constant that is HD-R station-dependent. The dynamic constant is determined by the HD-R demodulator during reception and is relayed to the Si4777 by the host controller for the blend.

4.10.1. IBOC Blend and I^2C Device Address Selection

In applications not requiring HD-Radio reception and IBOC blend, with the Si4777, two I^2C device addresses, A0 and A1 (pins 11 and 12), are available, allowing up to four Si4777 receivers to share the same I^2C bus (see "7. I2C Control Bus" on page 44). However in utilizing IBOC blend for HD-radio reception on the Si4777, only one device address A0 (pin 11) is available. Pin 12 is repurposed for the Interrupt output INTB, whilst Pin 18 is repurposed for the digital audio clock input DFS2.

The 7-bit device address consists of a fixed part (6 MSBs), followed by a programmable 1-bit part. The LSB of the device address signals whether a read or write I^2C operation occurs. The voltage on the A0 pin is used to set the programmable 1-bit part of the device address. The A0 pin is tied to ground and or is left to float for address selection. The various I^2C device addresses can be selected as summarized in Table 16.

Table 16. I^2C Device Address Selection in IBOC Blend Mode for Si4777

Device Address [6…1]	Device Address [0]	A0 Voltage (Pin connection)
110001	1	VIO1
110001	0	GND

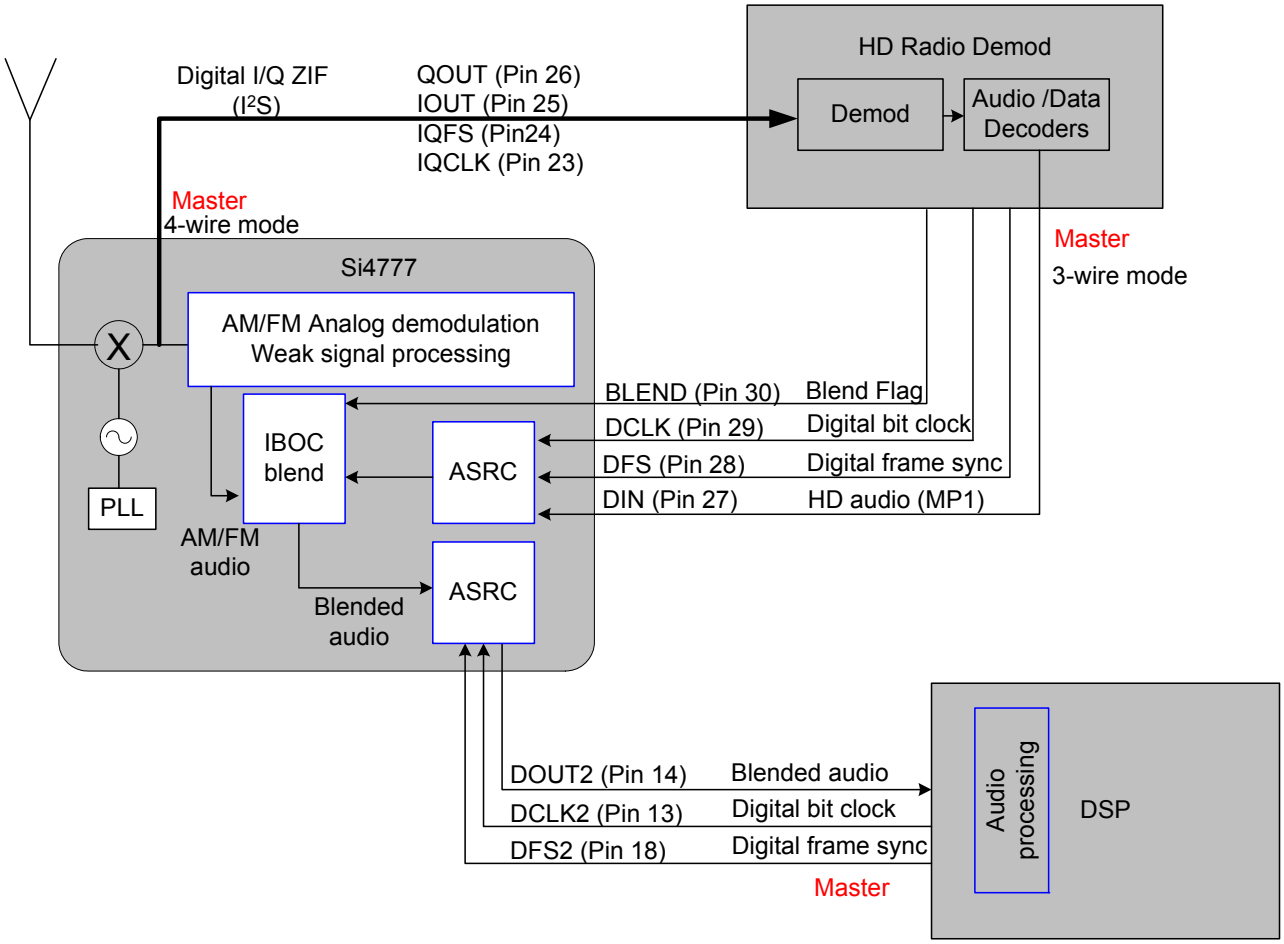


Figure 22. System Implementation of HD-Radio Reception with IBOC Blend on the Si4777

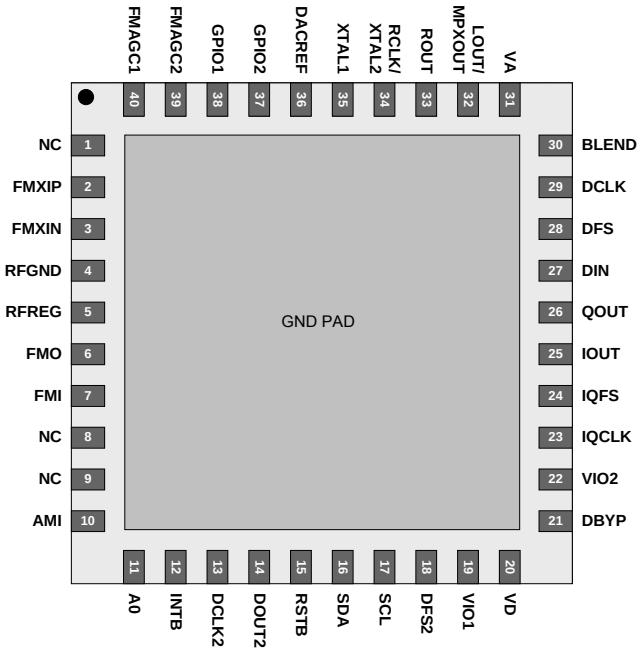


Figure 23. Si4777 Pin Descriptions for IBOC Blend Mode

Table 17. Pin Descriptions for Si4777 for IBOC Blend Mode

Pin Number	Name	I/O	Description
1	NC	I	No connect: Leave floating
2	FMXIP	I	Balanced input to FM mixer (positive)
3	FMXIN	I	Balanced input to FM mixer (negative)
4	RFGND		RF Ground
5	RFREG	O	FM LNA regulator
6	FMO	O	FM LNA output
7	FMI	I	FM LNA input
8	NC		No connect: Leave floating
9	NC		No connect: Leave floating
10	AMI	I	AM single-ended input
11	A0	I	I^2C Address 0
12	INTB	O	Interrupt active low (Si4777 for IBOC blend mode)
13	DCLK2	I	Digital audio bit clock input (Si4777 for IBOC blend mode)
14	DOUT2	O	Digital audio output (Si4777 for IBOC blend mode)

Table 17. Pin Descriptions for Si4777 for IBOC Blend Mode (Continued)

Pin Number	Name	I/O	Description
15	RSTB	I	Global Chip Reset
16	SDA	I/O	I^2C Data input/output
17	SCL	I	I^2C clock
18	DFS2	I	Digital audio bit clock input (Si4777 for IBOC blend mode)
19	VIO1	S	Host I/O Supply Voltage (all pads except digital audio and I/Q)
20	VD	S	Digital Voltage Supply
21	DBYP	I	Digital bypass to Ground
22	VIO2	S	Digital audio and I/Q interface supply voltage
23	IQCLK	O	ZIF I/Q bit clock output (Si4777)
24	IQFS	O	ZIF I/Q frame sync output (Si4777)
25	IOUT	O	ZIF I data output (Si4777)
26	QOUT	O	ZIF Q data output (Si4777)
27	DIN	I	Digital audio data input (Si4777 for IBOC blend mode)
28	DFS	I	Digital audio frame sync input
29	DCLK	I	Digital audio bit clock input
30	BLEND	I	Blend Flag Control
31	VA	S	Analog Voltage Supply
32	LOUT/ MPXOUT	O	Left audio line out / FM MPX output
33	ROUT	O	Right audio line out
34	XTAL2/RCLK	I	Crystal oscillator input/Reference clock input
35	XTAL1	O	Crystal oscillator output
36	DACREF	I	Voltage Reference for analog outputs
37	GPIO2	I/O	General-purpose input/output
38	GPIO1	I/O	General-purpose input/output
39	FMAGC2	I	FM automatic gain control 2
40	FMAGC1	I	FM automatic gain control 1
PDL	GND PAD	I	Ground. Reference ground

4.11. Stereo Audio Processing

The output of the FM demodulator is a stereo multiplexed (MPX) signal. The MPX standard was developed in 1961, and is used worldwide. Today's MPX signal format consists of left + right (L+R) audio, left – right (L–R) audio, a 19 kHz pilot tone, and RDS/RBDS data as shown in Figure 24.

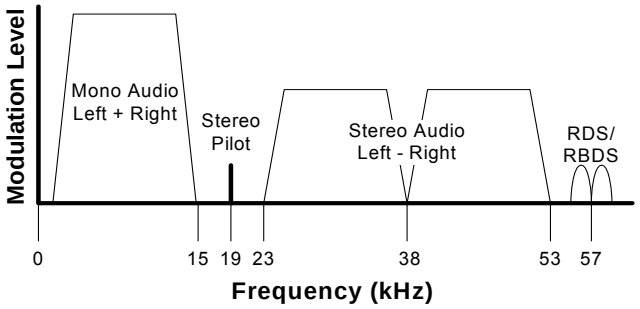


Figure 24. MPX Signal Spectrum

4.11.1. Stereo Decoder

The Si4770/77-A20's integrated stereo decoder automatically decodes the MPX signal using DSP techniques. The 0 to 15 kHz (L+R) signal is the mono output of the FM tuner. Stereo is generated from the (L+R), (L–R), and a 19 kHz pilot tone. The pilot tone is used as a reference to recover the (L–R) signal. Output left and right channels are obtained by adding and subtracting the (L+R) and (L–R) signals respectively.

4.11.2. Stereo-Mono Blending

Adaptive noise suppression is employed to gradually combine the stereo left and right audio channels to a mono (L+R) audio signal as the signal quality degrades to maintain optimum sound fidelity under varying reception conditions. Signal metrics such as on-channel RSSI, ultra-sonic noise (USN), and multi-path interference are monitored simultaneously in forcing a blend from stereo to mono. The metric, reflecting the poorest signal quality, takes priority and the stereo signal is blended appropriately. The thresholds for activating stereo-mono blend are programmable, as are the levels for a fully blended state. The attack and decay rates for each metric are programmable. The pilot detection metric is additionally available for read-out.

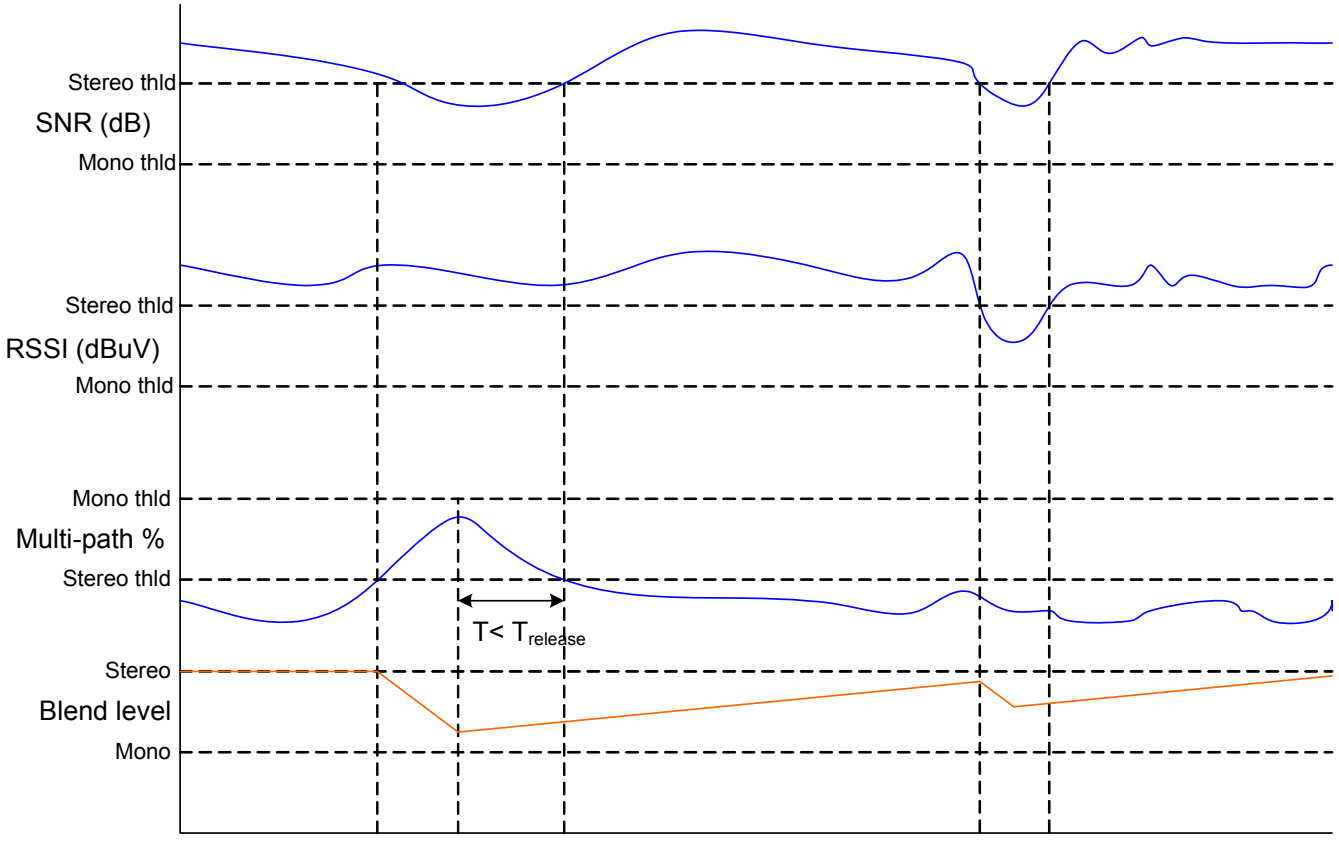


Figure 25. Conceptual Illustration of Stereo-Mono Blend

4.12. De-emphasis

Pre-emphasis and de-emphasis is a technique used by FM broadcasters to improve the signal-to-noise ratio of FM receivers by reducing the effects of high-frequency interference and noise. When the FM signal is transmitted, a pre-emphasis filter is applied to accentuate the high audio frequencies. The Si4770/77-A20 incorporate a de-emphasis filter which attenuates high frequencies to restore a flat frequency response. Two time constants are used in various regions. The de-emphasis time constant is programmable to 50 or 75 µs.

4.13. Analog Audio and FM MPX

High-fidelity digital-to-analog converters (DACs) drive analog audio signals or the FM MPX signal onto the LOUT/MPXOUT and ROUT pins. At powerup time the user can configure the analog outputs for either audio or MPX output. In applications where MPX and audio outputs are required simultaneously, the analog MPX signal can be driven onto the MPXOUT pin and the audio signals can be sourced from the digital audio interface.

The audio output may be muted. Volume is adjusted digitally. It is necessary that the volume be maintained at maximum levels to ensure the highest dynamic range audio outputs to the external audio processing stage in a car radio.

4.14. Soft Mute

The soft mute feature is available to attenuate the audio outputs and minimize audible noise in compromised signal conditions. The Si4770/77-A20 triggers soft mute by monitoring signal metrics such as on-channel RSSI or SNR. The thresholds for activating soft mute are programmable, as are soft mute attenuation levels and attack and decay rates. The Si4770/77-A20 provides the soft mute feature in FM and AM bands.

4.15. AM/FM Dynamic Bandwidth Control

The AM/FM IF channel bandwidth is dynamically optimized according to on-channel RSSI, and with the aid of the adjacent and alternate channel RSSI metric.

4.16. Seek and Valid Station Qualification

The seek function will search up or down the selected frequency band for a valid channel. A valid channel is qualified according to a series of programmable signal indicators and thresholds. The seek function can be made to stop at the band edge and provide an interrupt, or wrap the band and continue seeking until arriving at the original departure frequency. The device sets interrupts with found valid stations or, if the seek results in zero found valid stations, the device indicates failure and again sets an interrupt.

The Si4770/77-A20 seek functionality is performed completely on-chip or can be brought out to a companion processor. The Si4770/77-A20 can provide base values for signal quality variables to a companion processor for qualification or can further process the base values to qualify valid or invalid stations.

The Si4770/77-A20 uses RSSI, SNR, and frequency offset to qualify stations. These variables have programmable thresholds to tailor the seek function to the subjective tastes of customers.

RSSI is employed first to screen all possible candidate stations. SNR and frequency offset are subsequently used in screening the RSSI qualified stations. The more thresholds the system engages, the higher the confidence that any found stations will indeed be valid broadcast stations; however, the more challenging levels the thresholds are set to, the longer the overall seek time as more stations and more qualifiers will be assessed.

It is recommended that RSSI be set to a midlevel threshold in conjunction with an SNR threshold set to a level delivering acceptable audio performance. This trade-off will eliminate very low RSSI stations whilst keeping the seek time to acceptable levels. Generally, the time to auto-scan and store valid channels for an entire AM or FM band with all thresholds engaged is very short depending on the band content.

Seek is initiated using the AM and FM seek commands. The RSSI and SNR threshold settings are adjustable using properties.

4.17. AM Hi-Cut Control

AM hi-cut control is employed on AM audio outputs with degradation of signal quality. Signal metrics such as SNR or on-channel RSSI activate the hi-cut filter. Programmable minimum and maximum thresholds are available for all metrics. Attack and release rates for hi-cut are programmable for all metrics.

The level of hi-cut applied can be monitored with the received signal quality command. Hi-cut can be disabled by setting the hi-cut filter setting to the default audio bandwidth for AM. Further information is provided in the Programming Guide.

4.18. FM Hi-Cut Control

FM hi-cut control applies a low-pass filter on the (L+R) audio upon degradation of received signal quality. Signal metrics, such as USN, on-channel RSSI, and multipath interference, activate the hi-cut filter. Programmable minimum and maximum thresholds are available for all metrics. Attack and release rates are also programmable for all metrics. The level of hi-cut applied can be monitored with the received signal quality command. Further information is provided in the Programming Guide.

4.19. FM Hi-Blend

FM hi-blend control applies a low-pass filter on the (L-R) audio upon degradation of received signal quality. Signal metrics, such as USN, on-channel RSSI, and multipath interference, activate the hi-blend filter. Programmable minimum and maximum thresholds are available for all metrics. Attack and release rates for are also programmable for all metrics. The level of hi-blend applied can be monitored with the received signal quality command. Further information is provided in the Programming Guide.

4.20. AM Lo-Cut

AM lo-cut is employed on audio outputs for rejection of power-supply 50/60 Hz interference. AM lo-cut is a high pass filter. Lo-cut is enabled by default and can be disabled by programming the filter to being switched off.

5. RDS/RBDS Advanced Processor

The Si4770/77-A20 implements an advanced, patented, high-performance RDS processor for demodulation, symbol decoding, block synchronization, error detection, and error correction. The RDS decoder applies advanced decoding and statistical decision

techniques to provide high-performance synchronization at very noisy signal levels, and excellent sensitivity at industry-standard block error rate (BLER) levels (5%).

The Si4770/77-A20's strong synchronization performance in very noisy/low SNR environments minimizes the number of instances of lost synchronization. Other less robust tuners must attempt to resynchronize in low SNR environments, resulting in lost data and lengthy delays in reestablishing data reception. The Si4770/77-A20 maintains synchronization to the RDS transmission, despite high BLER. This results in fewer dropped connections, minimal resynchronization time, and greater data reliability in low SNR environments.

The Si4770/77-A20 reports RDS decoder synchronization status and detailed bit errors for each RDS block. The range of reportable bit errors detected and corrected are 0, 1-2, 3-5, and "not correctable." More than five errors indicate that the corresponding block information word is non-correctable.

The Si4770/77-A20 also provides highly configurable interrupts based on RDS-driven events and conditions. The default settings provide an interrupt when RDS is synchronized and when RDS group data has been received. The configurable interrupts can be set to provide frequent interrupts down to a single received block with BLER. The configurable interrupts also can be set to provide very infrequent interrupts, buffering up to 25 complete RDS groups (100 blocks) with BLER information by block in the on-chip FIFO. The Si4770/77-A20 also provides configurable interrupts on changes or receipt of the key RDS blocks A and B. This flexibility allows adopters to either conduct extensive RDS data processing on the host or reserve the host processor in power-saving modes with minimal RDS interrupts, allowing the Si4770/77-A20 to perform RDS processing on-chip.

6. Programming Section

To ease development time and offer maximum customization, the Si4770/77-A20 provides a simple and powerful software command protocol in addition to the 2-wire I^2C serial interface to communicate with the host processor.The device is programmed using commands, arguments, properties, and responses. To perform an action, the user writes a command byte and associated arguments, causing the chip to execute the given command. Commands control actions such as powerup, powerdown, or tune to a station. Arguments are specific to a given command and are used to modify the command. Properties are a special command + argument used to modify the default chip operation and are generally configured immediately after powerup. Examples of properties are de-emphasis level, RSSI seek threshold, and soft mute attenuation threshold. Responses provide information and are echoed after a command + argument is issued and processed. All commands provide a one-byte status update indicating interrupt and clear-to-send status information.

7. I²C Control Bus

A serial port slave interface is provided, which allows an external controller to send commands and receive responses from the Si4770/77-A20.

7.1. I²C Device Address Selection

Two device I²C addresses are available, allowing up to four Si4770/77-A20 receivers to share the same I²C bus. The 7-bit device address consists of a fixed part (5 MSBs), followed by a programmable 2-bit part. The LSB of the device address signals whether a read or write I²C operation occurs. The voltage on the A0 and A1 pins are used to set the programmable 2-bit part of the device address. The A0 and A1 pins are tied to ground and are left to float for address selection. The various I²C device addresses can be selected as summarized in Table 18.

7.2. I²C Standard Operation

The I²C bus interface is provided for configuration and monitoring of all internal registers. The Si4770/77-A20 supports a 7-bit device addressing procedure and is capable of operating at clock rates up to 400 kHz. Individual data transfers to and from the device are eight bits. The I²C bus consists of two wires: a serial clock line (SCL) and a serial data line (SDA). The device always operates as a bus slave. In order to be active, the I²C block requires that VIO1 and VD supplies be turned on.

A transaction begins with the START condition, which occurs when SDA falls while SCL is high. Next, the user drives an 8-bit control byte serially on SDA, which is captured by the device on rising edges of SCL. The control byte consists of a 7-bit device address followed by a read/write bit (read = 1, write = 0). The Si4770/77-A20 acknowledges the control word by driving SDA low on the next falling edge of SCL.

Read and write operations are performed in accordance with the I²C bus specification. For write operations, the host sends an 8-bit data byte on SDA, which is captured by the device on rising edges of SCL. The Si4770/77-A20 acknowledges each data byte by driving SDA low for one cycle, after the next falling edge of SCL. The host may write any number of data bytes in a single two-wire transaction. The first byte is a command, and the next bytes are arguments.

For read operations, after the Si4770/77-A20 has acknowledged the control byte, it drives an 8-bit data byte on SDA, changing the state of SDA after the falling edge of SCL. The host acknowledges each data byte by driving SDA low for one cycle, after the next falling edge of SCL. If a data byte is not acknowledged, the transaction ends. The host may read any number of data bytes in a single two-wire transaction. These bytes contain the response data from the Si4770/77-A20. A 2-wire transaction ends with the STOP condition, which occurs when SDA rises while SCL is high.

Table 18. I²C Device Address Selection

Device Address [6…2]	Device Address [1:0]	A1 Voltage (Pin Connection)	A0 Voltage (Pin Connection)
11000	11	Floating	Floating
11000	10	Floating	GND
11000	01	GND	Floating
11000	00	GND	GND

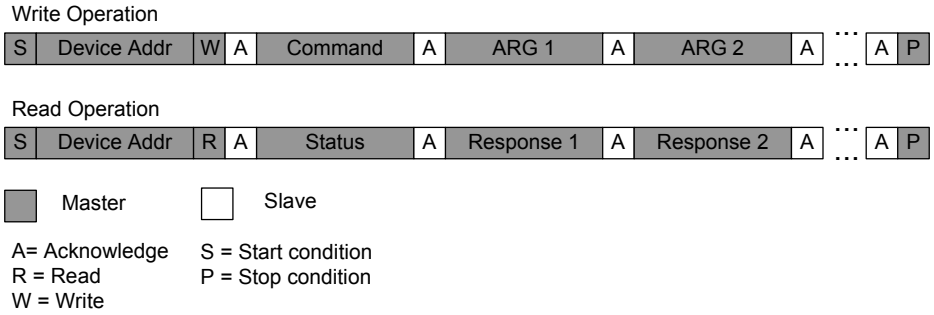


Figure 26. I²C Command/Response Protocol

8. Reset, Powerup, and Powerdown

Setting the RSTB pin low will disable analog and digital circuitry, reset the registers to their default settings, and disable the bus. Setting the RSTB pin high will bring the device out of reset.

The powerup mode powers up the device and provides mode selection. Mode selections include the following:

- AM, FM reception (Si4770/77-A20 only).
- Crystal oscillator or reference clock input

A powerdown mode is available to reduce power consumption when the part is idle. Putting the device in powerdown mode will disable analog and digital circuitry while keeping the bus active.

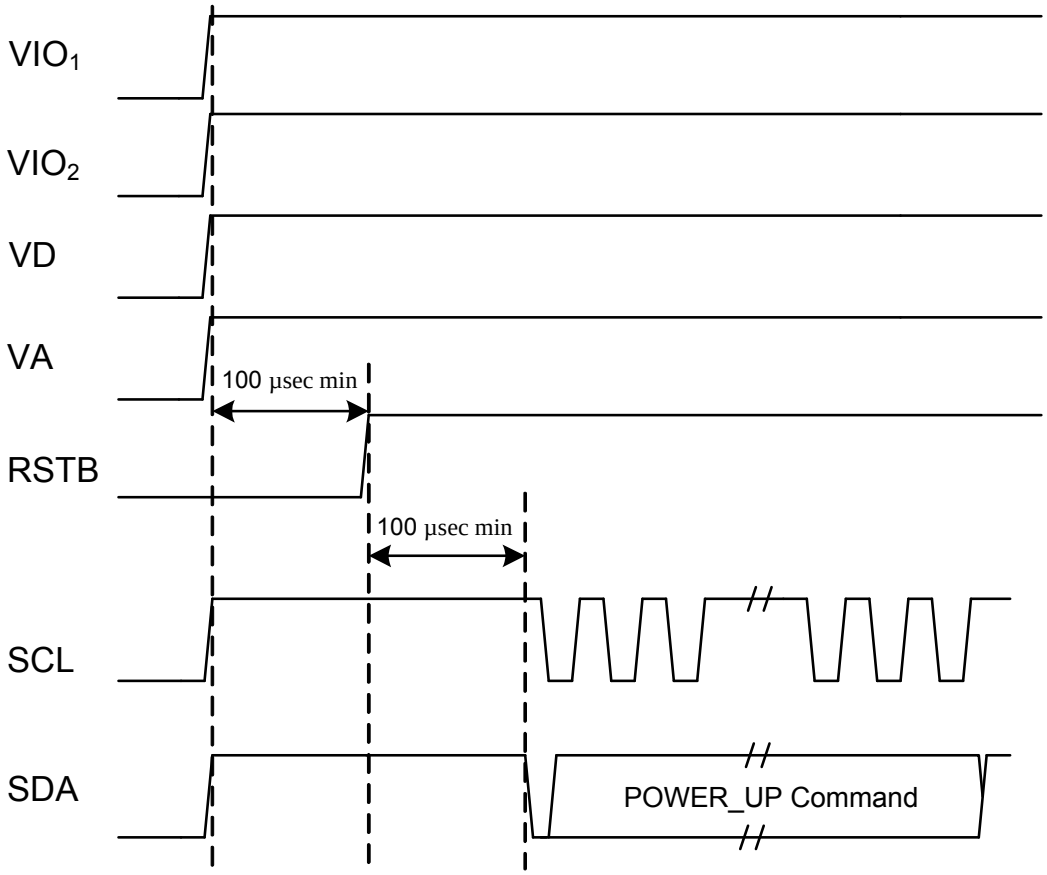


Figure 27. Startup Timing

9. Pin Descriptions: Si4770/77-A20

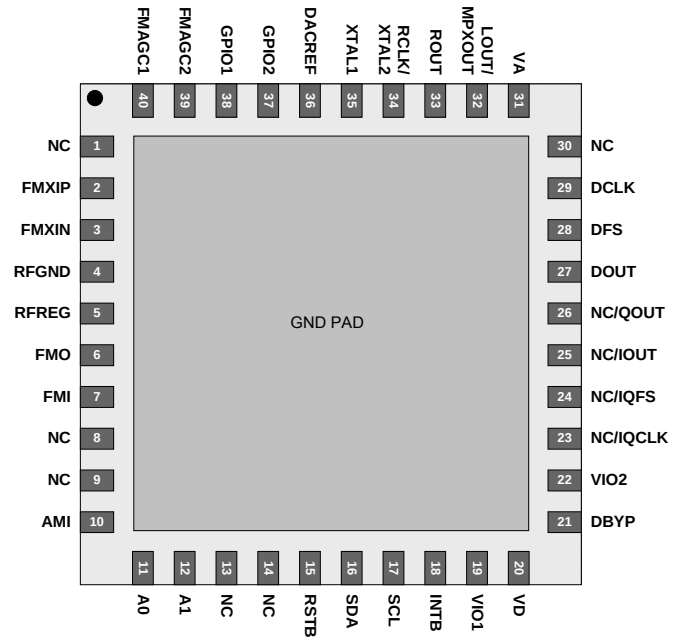


Figure 28. Si4770/77 Pin Descriptions

Table 19. Pin Descriptions for Si4770/77

Pin Number	Name	I/O	Description
1	NC	I	No connect: Leave floating
2	FMXIP	I	Balanced input to FM mixer (positive)
3	FMXIN	I	Balanced input to FM mixer (negative)
4	RFGND		RF Ground
5	RFREG	O	FM LNA regulator
6	FMO	O	FM LNA output
7	FMI	I	FM LNA input
8	NC		No connect: Leave floating
9	NC		No connect: Leave floating
10	AMI	I	AM single-ended input
11	A0	I	I^2C Address 0
12	A1	I	I^2C Address 1
13	NC		No connect: Leave floating

Table 19. Pin Descriptions for Si4770/77 (Continued)

Pin Number	Name	I/O	Description
14	NC		No connect: Leave floating
15	RSTB	I	Global Chip Reset
16	SDA	I/O	I^2C Data input/output
17	SCL	I	I^2C clock
18	INTB	O	Interrupt, Active Low
19	VIO1	S	Host I/O Supply Voltage (all pads except digital audio and I/Q)
20	VD	S	Digital Voltage Supply
21	DBYP	I	Digital bypass to Ground
22	VIO2	S	Digital audio and I/Q interface supply voltage
23	NC/IQCLK	O	No Connect: Leave floating (Si4770); ZIF I/Q bit clock output (Si4777)
24	NC/IQFS	O	No Connect: Leave floating (Si4770); ZIF I/Q frame sync output (Si4777)
25	NC/IOUT	O	No Connect: Leave floating (Si4770); ZIF I data output (Si4777)
26	NC/QOUT	O	No Connect: Leave floating (Si4770); ZIF Q data output (Si4777)
27	DOUT	O	Digital audio data output
28	DFS	I	Digital audio frame sync input
29	DCLK	I	Digital audio bit clock input
30	NC		No Connect: Leave floating
31	VA	S	Analog Voltage Supply
32	LOUT/ MPXOUT	O	Left audio line out / FM MPX output
33	ROUT	O	Right audio line out
34	XTAL2/RCLK	I	Crystal oscillator input/Reference clock input
35	XTAL1	O	Crystal oscillator output
36	DACREF	I	Voltage Reference for analog outputs
37	GPIO2	I/O	General-purpose input/output
38	GPIO1	I/O	General-purpose input/output
39	FMAGC2	I	FM automatic gain control 2
40	FMAGC1	I	FM automatic gain control 1
PDL	GND PAD	I	Ground. Reference ground

10. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si4770-A20-GM	AM/FM RDS Broadcast Radio Receiver	6 x 6 40-pin QFN Pb-Free	–40 to 85 °C
Si4777-A20-GM	AM/FM RDS Broadcast Radio Receiver and HD Radio Tuner	6 x 6 40-pin QFN Pb-Free	–40 to 85 °C
***Note:** Add an “(R)” at the end of the device part number to denote tape and reel option.			

11. Package Outline

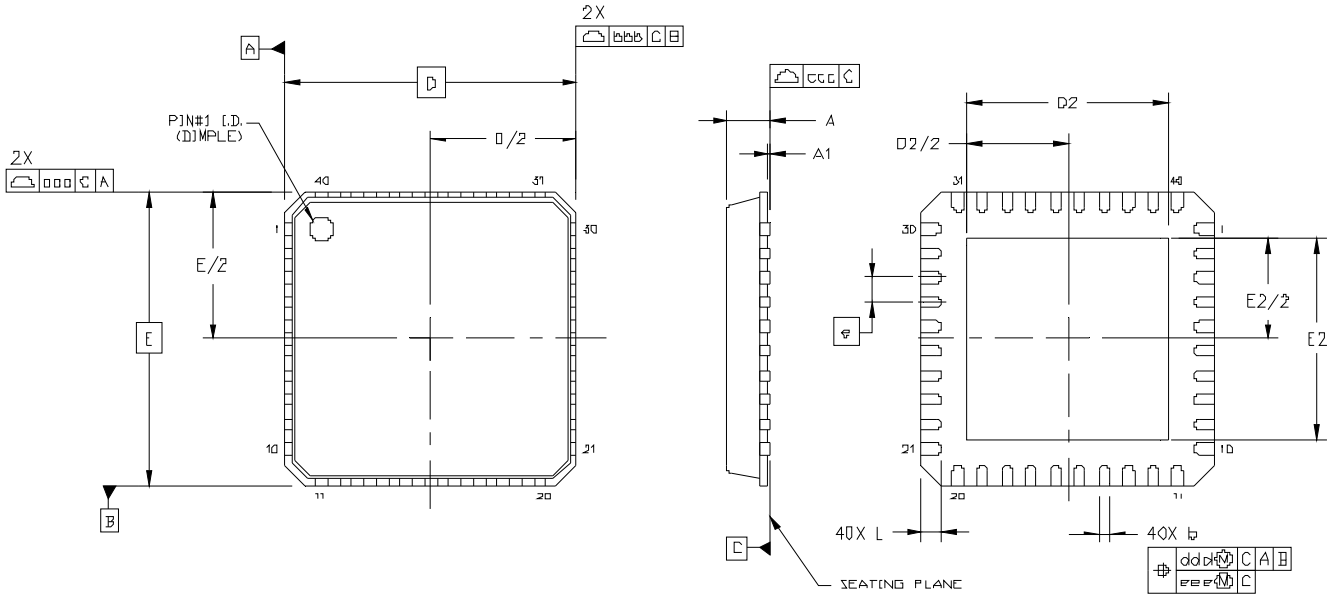


Figure 29. 40-Pin Quad Flat No-Lead (QFN)

Table 20. Package Dimensions

Dimensions	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC.	
D2	3.95	4.10	4.25
e		0.50 BSC.	
E		6.00 BSC.	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, Variation VJJD-2.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

12. PCB Land Pattern

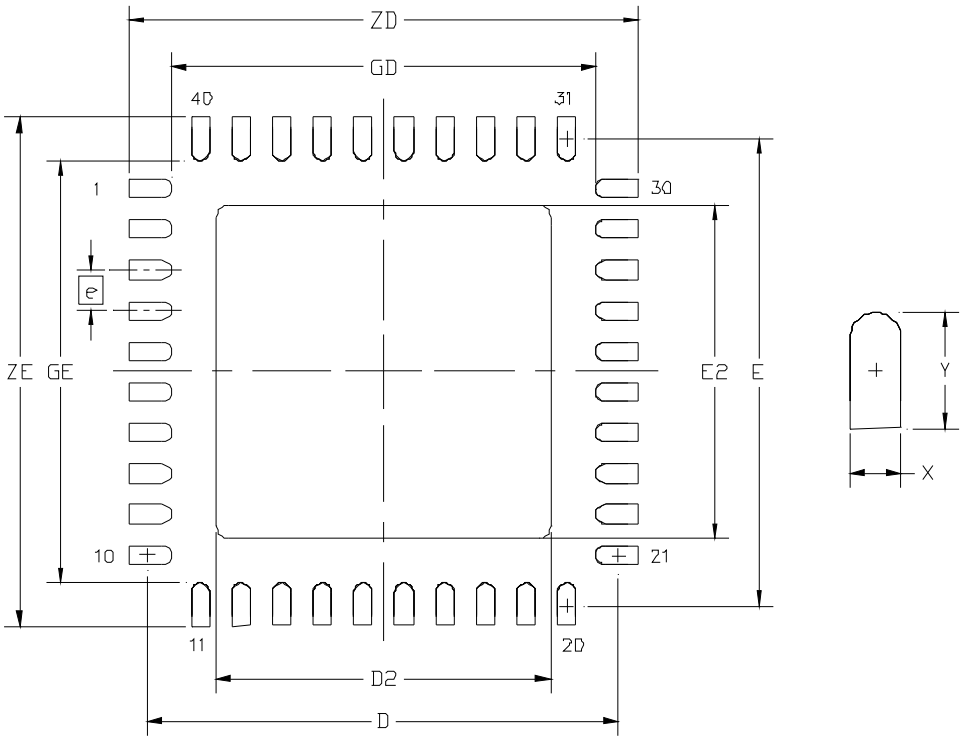


Figure 30. PCB Land Pattern

Table 21. PCB Land Pattern Dimensions

Dimensions	Min	Max
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

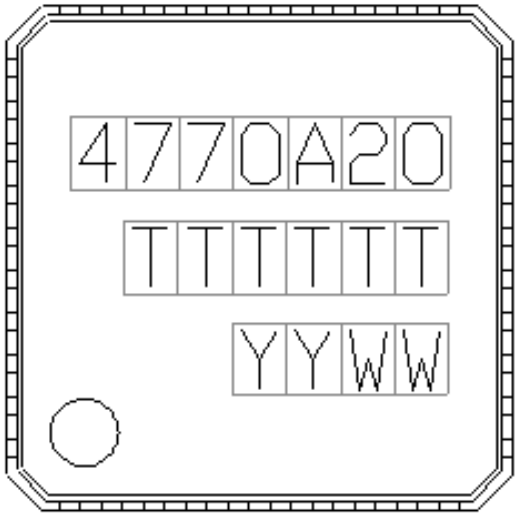
6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4 x4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

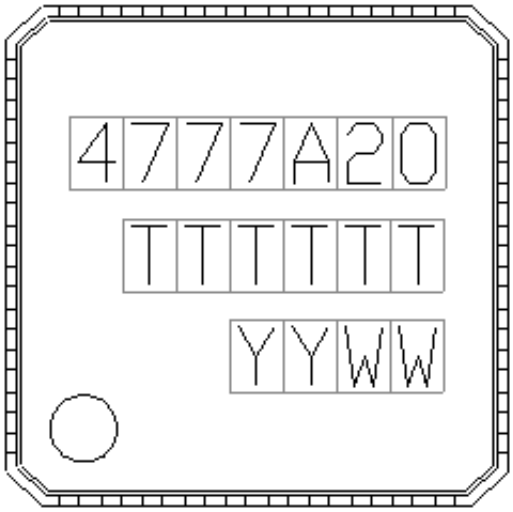
Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

13. Top Marking

13.1. Si4770/77-A20 Top Marking





13.2. Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Circle = 0.90 mm diameter (Bottom-Left-Justified)	
Font Size:	0.70 mm Right-Justified	
Line 1 Mark Format:	Device Number	4770 = Si4770 4777 = Si4777 A = Part Revision A 20 = Firmware Revision 2.0
Line 2 Mark Format:	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order Form.
Line 3 Mark Format:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly date.

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