AT9932

Automotive Boost-Buck LED Lamp Driver IC

Features

- Constant Output Current
- Steps Output Voltage Up or Down
- Very Low Susceptibility to Input Voltage Transients
- Frequency Jitter
- Externally Programmable Fixed Switching Frequency
- Temperature Foldback with External NTC Resistor
- Internal 40V Voltage Regulator
- +/–1A MOSFET Gate Driver
- Short LED Protection
- Open LED Protection
- Input Undervoltage Lockout Protection
- Enable and PWM Dimming
- ±3% Accurate Trimmed Reference
- AEC-Q100 Compliant

Applications

- Automobile Lighting
- Battery-Powered LED Lamps
- Other Low-Voltage AC/DC or DC/DC LED Drivers

General Description

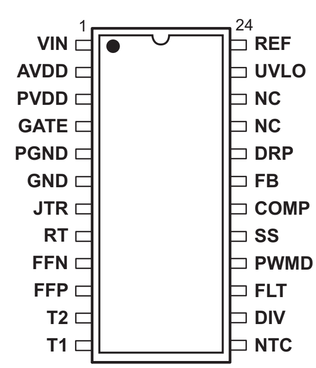
The AT9932 is an advanced fixed-frequency PWM controller IC designed to control an LED lamp driver using a boost-buck topology that can step the input voltage up or down automatically. The IC provides fast output current transient response and very low susceptibility to input voltage transients. This allows the lamp driver to pass the rigorous electrical transient requirements of SAE J1455 or ISO 7637-2, making the AT9932 an ultimate solution for automobile lighting. Capacitive isolation protects the LED Lamp from failure of the switching MOSFET.

The AT9932 features a unique feed-forward current control scheme, differential output current sensing, soft start and protection from short or open LED load. Switching frequency can be programmed with a single external resistor.

The AT9932 includes a temperature foldback of the output current using an external NTC resistor. This feature allows optimization of the light output of the LED load for safe operation over the entire operating temperature range.

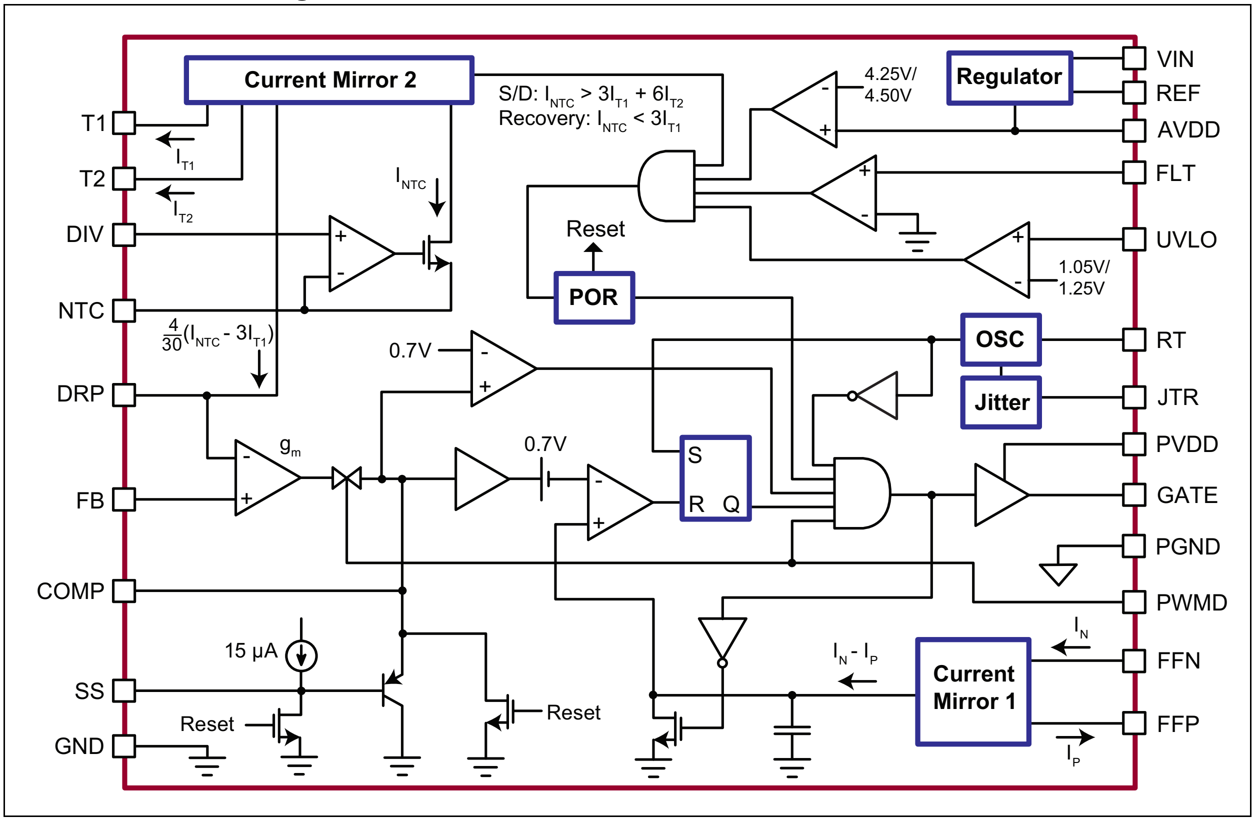
Package Type

24-lead TSSOP
(Top view)

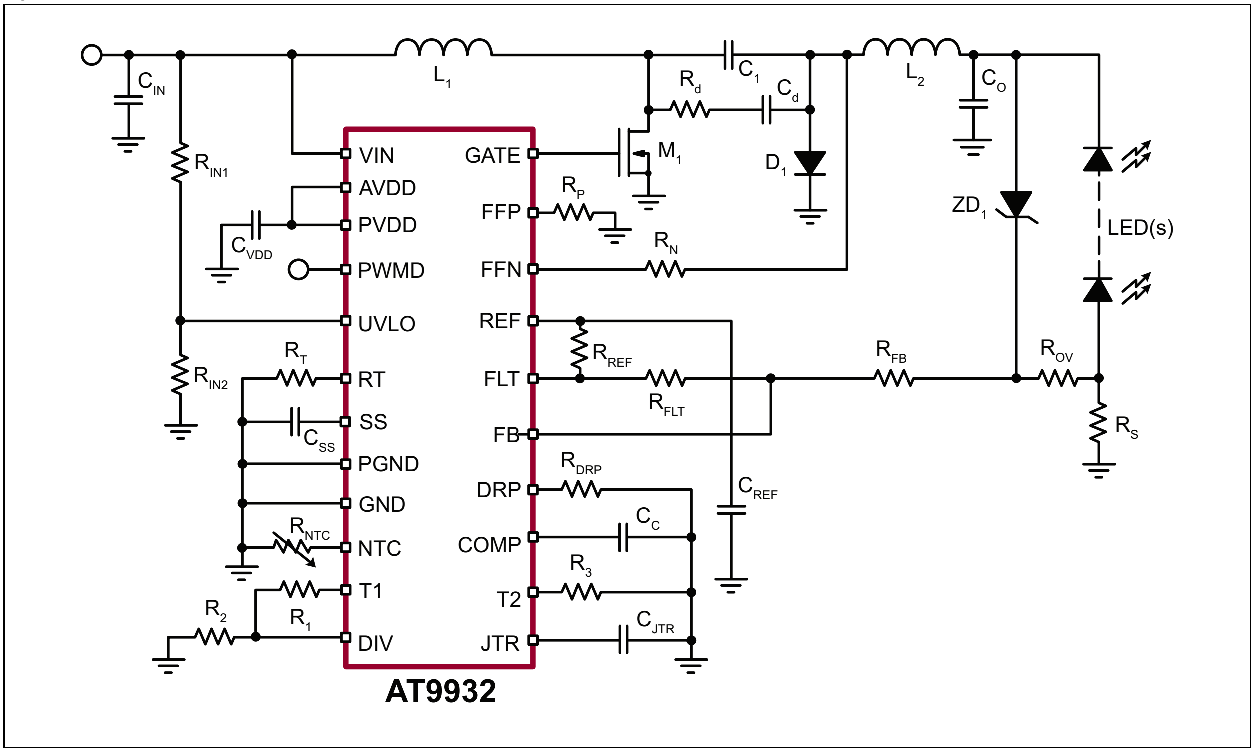


See Table 2-1 for pin information.

Functional Block Diagram



Typical Application Circuit



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

V_{IN} to GND .... –0.5V to +45V
PVDD and AVDD to GND .... –0.3V to +6V
Gate to GND Voltage .... –0.3V to (PVDD +0.3V)
All other pins to GND Voltage .... –0.3V to (AVDD +0.3V)
FFN, FFP Current .... 2 mA
REF Current .... 5 mA
Junction Temperature, T_J .... –40°C to +150°C
Storage Temperature, T_S .... –65°C to +150°C
Continuous Power Dissipation (T_A = +25°C):
24-lead TSSOP (**Note 1**) .... 1000 mW

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: $R_{\theta JA}$ = 125°C/W

ELECTRICAL CHARACTERISTICS

Electrical Specifications: Specifications are at T_A = 25°C, V_{IN} = 12V, $V_{PWMD} = V_{UVLO} = V_{AVDD} = V_{PVDD}$, Gate open, R_T = 200 kΩ, C_{REF} = 0.1 µF, $C_{AVDD} = C_{PVDD}$ = 1 µF, $I_{T1} = I_{T2}$ = 100 µA unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
INPUT						
Input DC Supply Voltage Range	V_{IN}	5.3	—	40	V	
Input Supply Current	I_{INEN}	—	—	2	mA	$V_{PWMD} = V_{GND}$ (**Note 1**)
Input Current, UVLO Mode	I_{INDIS}	—	—	100	µA	$V_{UVLO} = V_{PWMD} = V_{GND}$ (**Note 1**)
INTERNAL REGULATOR						
Regulated Output Voltage	V_{DD}	4.65	5	5.35	V	I_{DD} = 0 mA–20 mA, V_{IN} = 6V–40V, $V_{PWMD} = V_{GND}$ (**Note 1**)
V_{DD} UVLO Upper Threshold	$V_{DDUV, R}$	4.25	4.5	4.85	V	V_{DD} rising (**Note 1**)
V_{DD} UVLO Hysteresis	ΔV_{DDUV}	—	250	—	mV	V_{DD} falling
REFERENCE						
Reference Output Voltage	V_{REF}	1.21	1.25	1.29	V	I_{REF} = 0 mA (**Note 1**)
Reference Output Voltage, UVLO Mode	$V_{REF, DIS}$	—	0	—	mV	$V_{UVLO} = V_{GND}$
Load Regulation	ΔV_{REF}	0	—	2	mV	I_{REF} = 0 mA–1 mA
GATE OUTPUT						
Gate Output Rise Time	t_r	—	20	35	ns	C_{GATE} = 4 nF, $V_{IN} = V_{AVDD} = V_{PVDD}$ = 5V
Gate Output Fall Time	t_f	—	20	35	ns	
Maximum Duty Cycle	D_{MAX}	87	90	93	%	(**Note 1**)
FEED-FORWARD RAMP GENERATOR						
Minimum Gate On-Time	$t_{ON(MIN)}$	250	—	400	ns	I_{FFN} = 500 µA, I_{FFP} = 0 µA, V_{COMP} = 3.5V (**Note 1**)
Maximum Gate On-Time	$t_{ON(MAX)}$	6	—	13	µs	I_{FFN} = 10 µA, I_{FFP} = 0 µA, V_{COMP} = 3.5V (**Note 1**)
Gate On-Time	t_{ON}	1	—	2	µs	I_{FFN} = 110 µA, I_{FFP} = 10 µA, V_{COMP} = 3.5V (**Note 1**)
FFN/FFP Current Balancing	$\Delta t_{ON}/t_{ON}$	–3	—	3	%	I_{FFN} = 100 µA, I_{FFP} = 0 µA, V_{COMP} = 3.5V (**Note 2**)

Note 1: Specifications apply over the full operating ambient temperature range of –40ºC < T_A < +125ºC.
2: Specifications are obtained by characterization and are not 100% tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Specifications are at T_A = 25°C, V_{IN} = 12V, V_{PWMD} = V_{UVLO} = V_{AVDD} = V_{PVDD}, Gate open, R_T = 200 kΩ, C_{REF} = 0.1 µF, C_{AVDD} = C_{PVDD} = 1 µF, I_{T1} = I_{T2} = 100 µA unless otherwise noted.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TRANSCONDUCTANCE OPERATION AMPLIFIER						
Input Common Mode Range	V_{FB}, V_{DRP}	–0.3	—	3	V	(**Note 2**)
Input Offset Voltage	V_{OS}	–9	—	9	mV	(**Note 1**)
Transconductance	g_m	—	0.95	—	mA/V	
Open-Loop Voltage Gain	A_V	65	—	—	dB	COMP open
Gain Bandwidth Product	GBW	1	—	—	MHz	C_{COMP} = 150 pF (**Note 2**)
COMP Sink Current	I_{COMP}	0.2	—	—	mA	V_{FB} = 0.1V, V_{COMP} = V_{GND} (**Note 2**)
COMP Source Current		–0.2	—	—	mA	V_{FB} = –0.1V, V_{COMP} = V_{AVDD} (**Note 2**)
Input Bias Current	$I_{BIAS, AMP}$	—	0.5	1	nA	(**Note 2**)
Output Voltage Range	V_{COMP}	0.7	—	V_{DD}	V	(**Note 2**)
COMP Hiccup Threshold	$V_{COMP, HT}$	—	700	—	mV	
Output Leakage Current	I_{LEAK}	—	0.5	1	nA	V_{PWMD} = V_{GND} (**Note 2**)
OSCILLATOR						
Output Frequency	f_{OSC1}	90	105	120	kHz	R_T = 1 MΩ (**Note 1**)
	f_{OSC2}	427	505	583	kHz	R_T = 200 kΩ (**Note 1**)
Output Frequency Range	f_{OSC}	100	—	800	kHz	**Note 2**
JITTER						
Jitter Frequency	F_{JTR}	—	50	—	Hz	C_{JTR} = 0.1 µF
		—	500	—	Hz	C_{JTR} = 0.01 µF
Change in Switching Frequency	ΔF	±4.5	—	—	kHz	
TEMPERATURE FOLDBACK CIRCUIT						
NTC Source Current Range	I_{NTC}	—	—	1	mA	**Note 2**
DRP to NTC Current Gain	N_{NTC}	—	0.13	—	—	I_{NTC} = 0.5 mA
NTC to T1 Current Gain	N_{T1}	—	3	—	—	I_{NTC} = 0.5 mA
NTC to T2 Current Gain	N_{T2}	—	6	—	—	I_{NTC} = 0.5 mA
T1 and T2 Reference Voltage	V_{T1}, V_{T2}	—	3.5	—	V	
SOFT START						
Charging Current	$I_{SS, CHG}$	10	—	25	µA	
Discharging Current	$I_{SS, DIS}$	1	—	—	mA	V_{SS} = 5V
Reset Voltage	$V_{SS, RST}$	—	—	100	mV	
FAULT DETECT COMPARATOR						
Trip Voltage	V_{FLT}	–20	—	20	mV	
Input Bias Current	$I_{BIAS, FLT}$	—	0.5	1	nA	**Note 2**
INPUT UNDERVOLTAGE LOCKOUT						
Undervoltage Lockout Upper Threshold	$V_{UVLO, R}$	1.15	1.25	1.4	V	V_{UVLO} rising (**Note 1**)
Undervoltage Lockout Hysteresis	ΔV_{UVLO}	—	200	—	mV	V_{UVLO} falling
Input Bias Current	$I_{BIAS, UV}$	—	0.5	1	nA	**Note 2**
PWM DIMMING						
Enable Voltage Level	$V_{PWMD(HI)}$	2	—	—	V	**Note 1**
Disable Voltage Level	$V_{PWMD(LO)}$	—	—	0.8	V	**Note 1**
Pull-Down Resistor	R_{PWMD}	120	—	280	kΩ	

Note 1: Specifications apply over the full operating ambient temperature range of –40°C < T_A < +125°C.

2: Specifications are obtained by characterization and are not 100% tested.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+125	°C	
Maximum Junction Temperature	T_J	—	—	+150	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
24-lead TSSOP	θ_{JA}	—	125	—	°C/W	Note 1

Note 1: Mounted on an FR-4 board, 25 mm x 25 mm x 1.57 mm

2.0 PIN DESCRIPTION

The details on the pins of AT9932 are listed on Table 2-1. Refer to **Package Type** for the location of the pins.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VIN	This pin is the input of a 40V high-voltage regulator.
2	AVDD	This is a power supply pin for all internal circuits. It must be bypassed with a low-ESR capacitor to GND (at least 0.1 µF).
3	PVDD	This is the power supply pin for the gate driver. It should be connected externally to AVDD and bypassed with a low-ESR capacitor to PGND (at least 0.1 µF).
4	GATE	This pin is the output of gate driver for driving an external logic level N-channel power MOSFET.
5	PGND	Ground return for the gate drive circuitry
6	GND	Ground return for all the low-power analog internal circuitry. This pin must be connected to the return path from the input.
7	JTR	This pin programs the jitter of the clock by a capacitor connected from this pin to GND.
8	RT	Connecting an external resistor from this pin to GND sets the frequency of the oscillator circuit.
9	FFN	Connecting a resistor between this pin and the negative terminal of the coupling capacitor in the boost-buck converter programs positive PWM ramp signal. The slew rate is proportional to the current sunk from this pin. When the ramp voltage exceeds the voltage at COMP, the gate signal is terminated.
10	FFP	Connecting a resistor between this pin and GND cancels the FFN current error due to non-zero voltage at FFN. The FFN and FFP current mirrors are internally matched.
11	T2	Connecting a resistor from this current source pin to GND programs the overtemperature shutdown threshold temperature detected by an external NTC resistor.
12	T1	Connecting a resistor from this current source pin to GND programs the temperature threshold beyond which the LED current is reduced.
13	NTC	Connect an external NTC resistor from this current source pin to GND for temperature foldback of the output current and overtemperature shutdown.
14	DIV	This is the reference input that programs the voltage at the NTC pin.
15	FLT	This pin is an input of the fault comparator. This comparator is used for open and short LED protection. The IC shuts down and restarts after a POR delay when this comparator is triggered.
16	PWMD	When this pin is pulled to GND (or left open), the gate output is disabled. The COMP pin becomes high-impedance and holds its voltage level. When this pin is logic-high, the switching of gate resumes.
17	SS	Connecting a capacitor from this pin to GND programs the soft-start time of the LED driver.
18	COMP	This pin is the output of the error amplifier. Stable closed-loop control of the output LED current can be achieved by connecting a compensation network between COMP and GND. This pin is pulled to GND internally upon a startup or detection of a Fault condition.
19	FB	This pin is the high-impedance non-inverting input of the error amplifier. The output LED current sense voltage is programmed by connecting a resistor divider between REF and the negative terminal of the current sense resistor.
20	DRP	This is the output current sense reference voltage input at the error amplifier. Connect this pin to GND when no NTC derating is used. Connect a resistor from this pin to GND to program the droop of the LED current at temperature foldback.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
21	NC	No Connection
22	NC	
23	UVLO	This pin provides input undervoltage lockout protection. When voltage at this pin falls below its lower threshold, AT9932 halts switching, and the soft-start capacitor is discharged rapidly. The voltage at the REF pin becomes 0V, and the entire IC consumes quiescent current of less than 100 µA. The switching resumes when the UVLO pin voltage exceeds the upper threshold. Hysteresis is provided between the two thresholds.
24	REF	This pin provides accurate reference voltage. It must be bypassed with a 0.01 µF to 0.1 µF capacitor to GND.

3.0 FUNCTIONAL DESCRIPTION

3.1 Power Topology

The AT9932 is optimized to drive a Continuous Conduction Mode (CCM) boost-buck DC/DC converter topology commonly referred to as the Ćuk converter. (Refer to **Typical Application Circuit**.) This power converter topology offers numerous advantages useful for driving high-brightness light-emitting diodes (HB LED). These advantages include step-up or step-down voltage conversion ratio and low input and output current ripple. The output load is decoupled from the input voltage with a capacitor, making the driver inherently failure-safe for the output load.

The AT9932 features an optimal control method for use with a boost-buck LED driver. This method achieves very low susceptibility to input voltage transients, which makes it indispensable for automotive LED lighting applications. The AT9932 can maintain constant output current even under vigorous input transient conditions. Its output current control loop is inherently stable and can be compensated using a single capacitor with the appropriate damping at the coupling capacitor.

3.2 Regulator (V_{IN}, AVDD) and Gate Driver (Gate, PVDD)

The AT9932 can be powered directly from its V_{IN} pin that takes a voltage up to 40V. When V_{IN} voltage is applied, the AT9932 seeks to maintain constant voltage at the AVDD pin. When the undervoltage upper threshold is exceeded at AVDD, the gate driver is enabled after a 100 µs power-on reset (POR) delay. The output of the gate driver (GATE) controls the gate of an external N-channel power MOSFET. The maximum duty cycle of the gate signal is limited to 0.9 (typical). The undervoltage protection comparator disables the gate driver when the voltage at AVDD falls below the undervoltage lower threshold.

A separate PVDD input is provided to power the gate output to decouple the high switching currents of the gate driver from AVDD. Both pins (AVDD, PVDD) must be wired together on the printed circuit board (PCB). AVDD needs to be bypassed to GND by a low-ESR capacitor (≥0.1 µF). PVDD needs to be bypassed to PGND by a low-ESR capacitor (≥0.1 µF).

The input current drawn from the external power supply (or V_{IN} pin) is a sum of the 2 mA maximum current drawn by the all the internal circuitry and the current drawn by the gate driver which in turn depends on the switching frequency and the gate charge of the external FET. Refer to Equation 3-1.

EQUATION 3-1:

$$I_{IN} = 2mA + Q_G \times f_S$$

In Equation 3-1, f_S is the switching frequency, and Q_G is the gate charge of the external FET which can be obtained from the FET data sheet.

3.3 Timing Resistor (R_T)

The switching frequency f_S is programmed by selecting an external timing resistor, R_T. The resistance value can be computed as shown in Equation 3-2:

EQUATION 3-2:

$$R_T = \frac{1}{F_S \times C_T}$$

Where C_T = 9.5 pF

3.4 Jitter (JTR)

Clock frequency can be modulated by an externally programmed saw-tooth wave signal to reduce conducted electro-magnetic emission (EMI) from the LED driver. The deviation of the oscillator frequency is set internally to ±5 kHz. The modulation frequency is programmed by connecting a capacitor from JTR to GND. The value of the capacitor required for the jitter frequency is calculated with Equation 3-3.

EQUATION 3-3:

$$C_{JTR} = \frac{5\mu F}{F_{JTR}(Hz)}$$

Note that the jitter frequency must be chosen to be significantly lower than the crossover frequency of the closed-loop control. If not, the controller will not be able to reject the jitter frequency, and the LED current will have a current ripple at the jitter frequency.

3.5 Reference Voltage (REF)

The AT9932 provides a 1.25V reference voltage at the REF pin. This voltage is used to derive the various internal voltages required by the IC and is also used to set the LED current externally. It should be bypassed with a low-impedance capacitor (0.01 µF–0.1 µF).

3.6 Internal 1 MHz Transconductance Amplifier

The AT9932 includes a 1 MHz transconductance amplifier, which can be used to close the LED current feedback loop. The output state of the amplifier is controlled by the signal applied to the PWMD pin. When PWMD is high, the output of the amplifier is connected to the COMP pin and the gate drive is enabled. When PWMD is low, COMP is left open and the gate drive is disabled. This enables the integrating capacitor at the COMP pin to hold its charge when the PWMD signal has turned off the gate drive. When the gate drive is resumed, the voltage at COMP will be positioned for the converter to return to its Steady State condition.

When the voltage at COMP falls below 700 mV, the gate output is disabled. This feature reduces power dissipation in the Zener diode ZD_1 during Open LED string condition.

3.7 Soft Start (SS)

The soft-start feature can determine the initial ramp-up of the error voltage at the COMP pin. Connecting a single capacitor between SS to GND can program the soft-start time. Upon the first application of voltage to the AVDD pin, a current of 15 µA is supplied from the SS pin, gradually charging the soft-start capacitor. The COMP voltage tracks the voltage at the SS pin until regulation of the output current is reached. When the voltage at AVDD pin (V_{DD}) falls below the undervoltage lower threshold, the soft-start capacitor is discharged rapidly.

3.8 Feed-Forward Ramp Generator (FFP, FFN) and PWM Comparator

The heart of the AT9932 is the feed-forward circuit having two inputs: FFN and FFP. This circuit generates a voltage ramp proportional to the difference between the FFN and FFP currents.

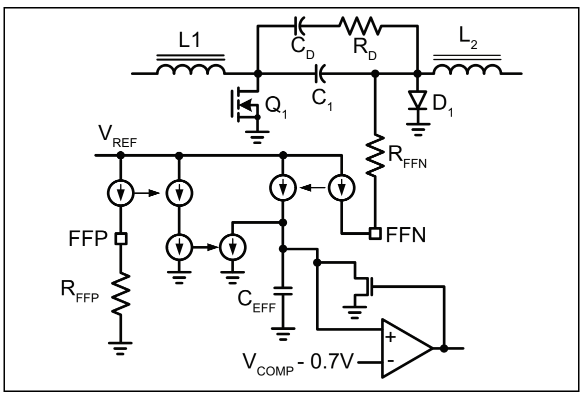


FIGURE 3-1: Feed-Forward Ramp Generator.

As shown in Figure 3-1, the resistor R_{FFN} is connected between FFN and the negative terminal of the coupling capacitor C_1. The resistor R_{FFP} of the same value ($R_{FFP} = R_{FFN}$) is connected between FFP and GND. The on-time of the gate output can be computed as shown in Equation 3-4.

EQUATION 3-4:

$$t_{ON} = \frac{R_{FFN} \times C_{EFF} \times (V_{COMP} - 0.7V)}{V_{C1}}$$

Where C_{EFF} = 50 pF ±40%, V_{COMP} is the COMP voltage, and V_{C1} is the voltage across the coupling capacitor C_1.

The duty cycle of a Continuous Conduction mode boost-buck converter is given as illustrated in Equation 3-5.

EQUATION 3-5:

$$D = t_{ON} \times f_S = \frac{V_{OUT}}{V_{C1}} = \frac{V_{OUT}}{V_{OUT} + V_{IN}}$$

Where V_{IN} is the input supply voltage, and V_{OUT} is the forward voltage of the LED string.

Since the output voltage at COMP is limited to $V_{COMP} = V_{DD}$, the feed-forward resistors must be selected in accordance with Equation 3-6.

EQUATION 3-6:

$$R_{FFN} = R_{FFP} \geq \frac{V_{OUT}}{C_{EFF} \times f_S \times (V_{DD} - 0.7V)}$$

Otherwise, the steady-state Duty Cycle D will not be reached, and the LED driver will be unable to develop the desired current.

The feed-forward loop provides instantaneous response to any transient at C_1 and therefore achieves excellent rejection of the input voltage transients along the supply line. It is inherently stable with proper selection of the damping network R_d and C_d. Optimal selection of R_d and C_d is complex. However, the worst case design of the damping circuit can be performed under the assumption that $V_{OUT(MAX)} >> V_{IN(MIN)}$ for most automotive applications of the AT9932. The simplified equations given below produce excellent results under this assumption. See Equation 3-7 and Equation 3-8.

EQUATION 3-7:

$$C_d = \frac{9D_{MAX}}{(1 - D_{MAX})} \times \frac{L_1 \times I_O^2}{V_{IN(MIN)}}$$

EQUATION 3-8:

$$R_d = \frac{V_{IN(MIN)}}{3D_{MAX}I_O}$$

In cases where the above assumption is not valid, the equations for R_d and C_d could still be used. However, they may produce conservative results. Power dissipation in the damping resistor R_d can be computed as shown in Equation 3-9.

EQUATION 3-9:

$$P_{Rd} = \frac{\Delta V_{C1}^{2}}{12 \times R_d}$$

Where:

$$\Delta V_{C1} = \frac{I_{OUT} \times D}{f_S \times C_1}$$

is the peak-to-peak voltage ripple at the coupling capacitor.

3.9 Output Overvoltage Protection

The AT9932 LED lamp driver supplies constant current to the load. Therefore, an output circuit protection is needed to prevent dramatic failures when the output load fails to open. A simple addition of a Zener diode (ZD_1 in the **Typical Application Circuit**) will limit the output voltage when the output LED connection is lost.

3.10 Programming LED Current and Temperature Foldback

The AT9932 offers a temperature foldback feature that allows the programming of output current in accordance with the temperature derating characteristics provided by the LED manufacturers. A typical derating curve is shown in Figure 3-2.

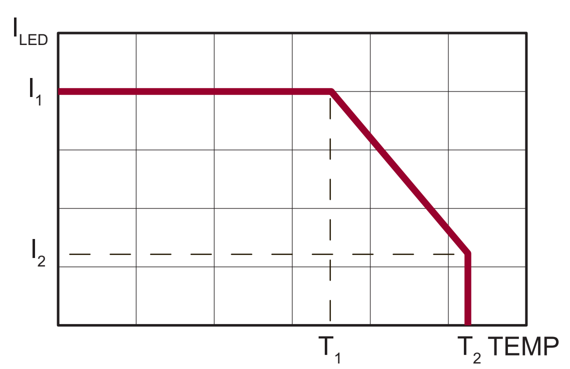


FIGURE 3-2: Temperature Derating Curve of LED Current.

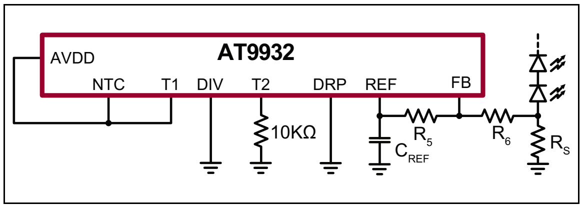


FIGURE 3-3: Output Current Feedback without Temperature Foldback.

When no temperature foldback is required, NTC and T1 should be connected to AVDD. In addition, DIV and DRP should be connected to GND. T2 still requires a resistor to GND (10 kΩ–100 kΩ). No pins should be left floating as shown in Figure 3-3. In this case, the output current of the AT9932 LED driver is programmed using Equation 3-10:

EQUATION 3-10:

$$I_1 = \frac{V_{REF}}{R_S} \times \frac{R_6}{R_5}$$

Where V_{REF} is voltage at the REF pin (V_{REF} = 1.25V).

When temperature foldback is required, the Equation 3-10 is also used to calculate LED current I_1 at temperature below T_1.

When an external NTC resistor is connected (See Figure 3-4.), both temperatures T_1 and T_2, as well as the current I_2 can be accurately programmed to safely regulate the light output of the LED lamp at the higher temperature range between T_1 and T_2.

The ratio of the resistor divider $R_2 /(R_1 + R_2)$ programs the voltage at the NTC pin. The voltage at T1 is approximately 3.5V. The currents sourced by NTC and T1 pins are mirrored into DRP in accordance with Equation 3-11.

EQUATION 3-11:

$$I_{DRP} = \frac{4}{30}(I_{NTC} - 3I_{T1}) > 0$$

No current is sourced from DRP when I_{NTC} < 3 x I_{T1}.

Temperature T_1 is programmed by selecting R_2 such that (See Equation 3-12.):

EQUATION 3-12:

$$R_2 = 3R_{NTC(T1)}$$

Where $R_{NTC(T1)}$ is the resistance of the NTC resistor at temperature T_1.

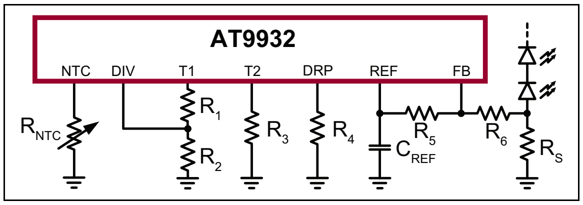


FIGURE 3-4: Output Current Feedback with Temperature Foldback.

At temperature higher than T_1, further reduction of the NTC resistance R_{NTC} will create a proportional offset of the current feedback reference voltage at DRP, and will therefore decrease the LED current. To program the desired LED current I_2 at the temperature T_2, the resistor R_4 at DRP can be calculated as shown in Equation 3-13.

EQUATION 3-13:

$$R_4 = (I_1 - I_2) \times R_S \times \frac{30 R_{NTC(T2)}(R_1 + R_2)}{4 V_{T1}(R_2 - 3 R_{NTC(T2)})} \times \frac{R_5}{R_5 + R_6}$$

Where $R_{NTC(T2)}$ is the resistance of the NTC resistor at the temperature T_2, and V_{T1} is the voltage at the T1 pin ($V_{T1} \approx 3.5V$).

When the current from the NTC pin exceeds 3 x I_{T1} + 6 x I_{T2}, overtemperature shutdown is triggered. The voltage at T2 is approximately equal to the voltage at T1. Selecting resistance of R_3 at the T2 pin programs the desired shutdown temperature T_2. Refer to Equation 3-14.

EQUATION 3-14:

$$R_3 = \frac{6 R_{NTC(T2)} \times (R_1 + R_2)}{R_2 - 3 R_{NTC(T2)}}$$

The overtemperature recovery threshold is independent of the current at T2 pin. The AT9932 recovers from thermal shutdown at the break temperature T_1, where $I_{NTC} < 3 \times I_{T1}$.

3.11 Input Undervoltage Lockout (UVLO) Protection

To protect the AT9932 against excessive input current at low input supply voltage, the undervoltage lockout protection comparator input is provided. Connecting a resistor divider between V_{IN} and GND programs the V_{IN} start and V_{IN} stop thresholds as indicated in Equation 3-15 and Equation 3-16.

EQUATION 3-15:

$$V_{IN(START)} = \frac{(R_{IN1} + R_{IN2}) \times 1.25V}{R_{IN2}}$$

EQUATION 3-16:

$$V_{IN(STOP)} = 0.84 \times V_{IN(START)}$$

The hysteresis is provided to prevent oscillation.

The AT9932 becomes disabled and draws less than 100 µA of current from V_{IN} or V_{DD} when the UVLO pin voltage falls below the UVLO lower threshold. The 1.25V reference at the REF pin becomes 0V at this condition. Hence, the UVLO input can also be used as a low stand-by power disable input.

3.12 Fault Comparator (FLT)

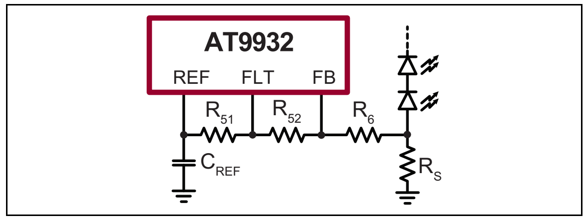


FIGURE 3-5: Output Short-circuit Protection.

The AT9932 also provides an internal protection comparator that can be used for protection against short and open LED string conditions. When the voltage at the FLT input falls below the GND potential, the AT9932 shuts down. The soft-start capacitor at SS is discharged. Switching resumes automatically after a POR delay.

Configuring the FLT input to protect against a short LED string is illustrated in Figure 3-5. The short-circuit current can be calculated as shown in Equation 3-17.

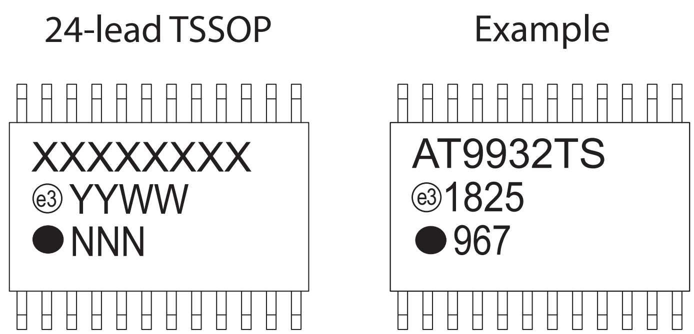
EQUATION 3-17:

$$I_{SHORT} = \frac{V_{REF}}{R_S} \times \frac{R_6 + R_{52}}{R_{51}}$$

The same resistor divider can be used to protect the LED driver from the open LED string condition, as shown in the **Typical Application Circuit**. The addition of a Zener diode ZD_1 causes the FLT comparator to trip when $V_{OUT} > V_Z$.

4.0 PACKAGING INFORMATION

4.1 Package Marking Information

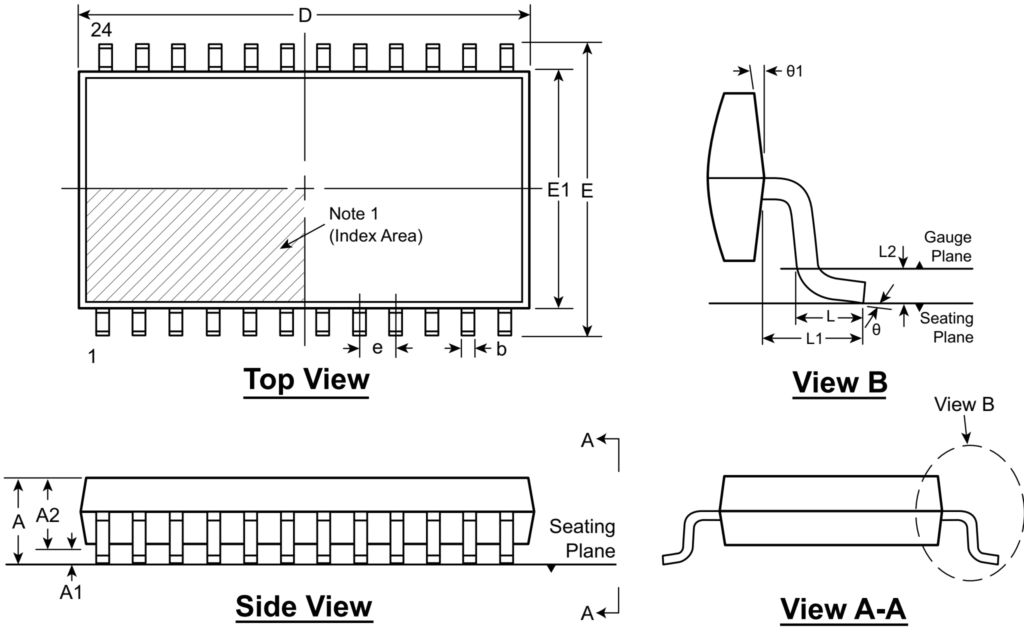


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

24-Lead TSSOP Package Outline (TS)

7.80x4.40mm body, 1.20mm height (max), 0.65mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	$\theta 1$
Dimension (mm)	MIN	0.85*	0.05	0.80	0.19	7.70	6.20*	4.30	0.65 BSC	0.45	1.00 REF	0.25 BSC	0°	12° REF
	NOM	-	-	1.00	-	7.80	6.40	4.40		0.60			-	
	MAX	1.20	0.15	1.15†	0.30	7.90	6.60*	4.50		0.75			8°	

JEDEC Registration MS-153, Variation AD, Issue F, May 2001.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (May 2018)

- Converted Supertex Doc# DSFP-AT9932 to Microchip DS20005789A
- Changed the package marking format
- Changed the quantity of the 24-lead TSSOP TS package from 3000/Reel to 2500/Reel
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	AT9932	=	Automotive Boost-Buck LED Lamp Driver IC
Package:	TS	=	24-lead TSSOP
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	2500/Reel for a TS Package

Example:

a) AT9932TS-G: Automotive Boost-Buck LED Lamp Driver IC, 24-lead TSSOP, 2500/Reel

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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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