4 CML Output, Low Jitter Clock Generator with an Integrated 5.4 GHz VCO

Data Sheet **AD9530**

FEATURES

- Fully integrated, ultralow noise phase-locked loop (PLL)
- 4 differential, 2.7 GHz common-mode logic (CML) outputs
- 2 differential reference inputs with programmable internal termination options
- <232 fs rms absolute jitter (12 kHz to 20 MHz) with a non-ideal reference and 8 kHz loop bandwidth
- <100 fs rms absolute jitter (12 kHz to 20 MHz) with an 80 kHz loop bandwidth and low jitter input reference clock
- Supports low loop bandwidths for jitter attenuation
- Manual switchover
- Single 2.5 V typical supply voltage
- 48-lead, 7 mm × 7 mm LFCSP

APPLICATIONS

- 40 Gbps/100 Gbps optical transport network (OTN) line side clocking
- Clocking of high speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs)
- Data communications

GENERAL DESCRIPTION

The AD9530 is a fully integrated PLL and distribution supporting, clock cleanup, and frequency translation device for 40 Gbps/ 100 Gbps OTN applications. The internal PLL can lock to one of two reference frequencies to generate four discrete output frequencies up to 2.7 GHz.

The AD9530 features an internal 5.11 GHz to 5.4 GHz, ultralow noise voltage controlled oscillator (VCO). All four outputs are individually divided down from the internal VCO using two high speed VCO dividers (the Mx dividers) and four individual 8-bit channel dividers (the Dx dividers). The high speed VCO dividers offer fixed divisions of 2, 2.5, 3, and 3.5 for wide coverage of possible output frequencies. The AD9530 is configurable for loop bandwidths <15 kHz to attenuate reference noise.

The AD9530 is available in a 48-lead LFCSP and operates from a single 2.5 V typical supply voltage.

The AD9530 operates over the extended industrial temperature range of −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

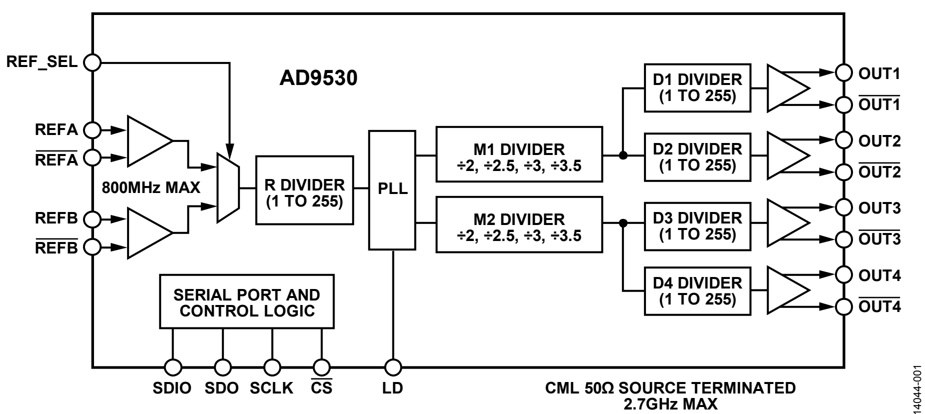

Figure 1.

Rev. 0 Document Feedback

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REVISION HISTORY

4/16—Revision 0: Initial Version

SPECIFICATIONS

Typical values are given for V_{DD} = 2.5 V ± 5%, T_A = 25°C, unless otherwise noted. Minimum and maximum values are given over the full V_{DD} range and T_A (−40°C to +85°C) variations listed in Table 1.

SUPPLY VOLTAGE AND TEMPERATURE RANGE SPECIFICATIONS

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY VOLTAGE	V_{DD}	2.375	2.5	2.625	V	2.5 V ± 5%
TEMPERATURE						
Ambient Temperature Range	T_A	−40	+25	+85	°C	
Junction Temperature[1]	T_J			115	°C	

[1] The is the maximum junction temperature for which device performance is guaranteed. Note that the Absolute Maximum Ratings section may have a higher maximum junction temperature, but device operation or performance is not guaranteed above the number that appears here. To calculate the junction temperature, see the Power Dissipation and Thermal Considerations section.

SUPPLY CURRENT SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT OTHER THAN CLOCK THE DISTRIBUTION CHANNEL					Current listed in the Typ column is at nominal V_{DD} at 25°C; current listed in the Max column is at maximum V_{DD} and worst case temperature
Typical Operation 1					f_{RTWO} = 5300.16 MHz; VCO mode = low power; REFA enabled at 110.42 MHz; REFB disabled; R divider = 1; M1 and M3 divider = 3; M2 divider = powered down; phase frequency detector (PFD) = 110.42 MHz; OUT1 CML output at 1766.72 MHz; OUT2, OUT3, and OUT4 outputs and dividers powered down; single-ended output swing level = 800 mV; outputs terminated externally with 50 Ω to V_{DD}
Reference Input VDD (Pin 3 and Pin 7)		8.2	10.7	mA	Combined current of Pin 3 and Pin 7
PLL VDD (Pin 12)		18.2	24	mA	
Rotary Travelling Wave Oscillator (RTWO) VDD (Pin 20 to Pin 23)		747	860	mA	Combined current of Pin 20 to Pin 23
SUPPLY CURRENT FOR AN INDIVIDUAL CLOCK DISTRIBUTION CHANNEL					Each output channel has a dedicated VDD pin; all current values are listed for a single driver supply pin operating at 1766.72 MHz; output terminated externally, 50 Ω to VDD; these specifications include the current required for the external load resistors
CML					
Internal Termination Disabled					
800 mV		28.8	35.5	mA	
900 mV		30.7	37.6	mA	
1000 mV		32.6	39.8	mA	
1100 mV		34.5	41.8	mA	
Internal Termination Enabled					
800 mV		47.6	57.2	mA	
900 mV		51.5	61.5	mA	
1000 mV		55.3	65.8	mA	
1100 mV		59.0	70.1	mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT DELTAS, INDIVIDUAL FUNCTIONS					Current delta when a function is enabled/disabled from Typical Operation 1
VCO High Performance Mode Enabled		133.5	160.0	mA	Current increase when the VCO mode is changed from low power mode to high performance mode; combined current delta of Pin 20 to Pin 23
REFx/$\overline{\text{REFx}}$ Receiver[1]		2.5	3.3	mA	Current increase when REFB is enabled with a 110.42 MHz reference input; combined current delta of Pin 3 and Pin 7
Reference Divider	−0.55	−0.39		mA	Delta from bypassing reference divider to using reference divider = 2; total feedback division doubled to preserve lock; combined current delta of Pin 3 and Pin 7
Output Channel		28.4	33.3	mA	One output channel enabled by powering up M2 divider = 3; D3 and D4 divider = 1; OUT3 and OUT4 enabled to 800 mV; no internal termination; associated low-dropout regulators (LDOs) enabled; includes the current required by the external termination; both outputs at 1766.72 MHz
Mx Divider On/Off		33.2	36.2	mA	This is the current consumption delta between an Mx (where x is 0, 1, or 2) divider powered up and powered down; these dividers are a part of the RTWO VDD (Pin 20 to Pin 23) power domain
Single Output Plus Associated Channel Divider (OUT1: Pin 31, OUT2: Pin 35, OUT3: Pin 41, OUT4: Pin 45)		28.4	33.4	mA	One output driver enabled by powering up the driver and channel divider (does not include power on the extra M2 divider); includes the current required by the external termination; output = 1766.72 MHz

[1] Where x is either A or B.

POWER DISSIPATION SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TOTAL POWER DISSIPATION					Does not include power dissipated in external resistors; all CML outputs terminated with 50 Ω to VDD; internal output termination is disabled; output amplitude set to 1.0 V; reference inputs set to ac-coupled mode
Power-On Default		2.284	2.750	W	
Power-Down Mode		0.338	0.480	W	
Typical Operation 2		2.344	2.82	W	f_{RTWO} = 5302.5 MHz; VCO mode = high performance; REFA enabled at 101 MHz, ac-coupled; REFB disabled; R divider = 1; M1 divider and M3 divider = 2.5; PFD = 101 MHz; OUT1 and OUT2 CML outputs at 2121 MHz; OUT3 and OUT4 disabled; output swing level = 800 mV; outputs terminated externally to 50 Ω to VDD and internal termination disabled; M2 divider and LDO powered down; D3 and D4 dividers and associated LDOs disabled
All Blocks Running					f_{RTWO} = 5400 MHz; VCO mode = high performance; REFA and REFB enabled at 100 MHz; ac-coupled mode; R divider = 1; M divider = 2; PFD = 100 MHz; four CML outputs at 2700 MHz
800 mV Output Swing, Without Internal Output Termination		2.536	3.02	W	Single-ended output swing level = 800 mV and internal termination off
1100 mV Output Swing with Internal Output Termination		2.796	3.326	W	Single-ended output swing level = 1100 mV and internal termination on

REFA/$\overline{REFA}$ AND REFB/$\overline{REFB}$ INPUT CHARACTERISTICS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC-COUPLED LVDS MODE (REFA, $\overline{REFA}$; REFB, $\overline{REFB}$)					DC-coupled LVDS mode (REFx_TERM_SEL = 00); includes an internal 100 Ω differential termination; inputs are not self biased in this setting
Input Frequency	6		800	MHz	Assumes a minimum of 494 mV p-p differential amplitude as measured with a differential probe at the REFx input pins
Input Sensitivity	494			mV p-p	Peak-to-peak differential voltage swing across the pins to ensure switching between logic levels as measured with a differential probe
Common-Mode Input Voltage	0.4		1.4	V	Allowable common-mode voltage for dc coupling
Differential Input Resistance		110		Ω	Differential input resistance measured across the REFx and $\overline{REFx}$ pins
Input Capacitance		3		pF	Input capacitance measured from each REFx pin to GND
DC-COUPLED CML MODE (REFA, $\overline{REFA}$, REFB, $\overline{REFB}$)					DC-coupled (REFx_TERM_SEL = 01); includes an internal termination of 50 Ω from each REFx input to GND; inputs are not self biased in this setting
Input Frequency	6		800	MHz	Assumes a minimum of 494 mV p-p differential amplitude as measured with a differential probe at the REFx input pins
Input Sensitivity	494			mV p-p	Peak-to-peak differential voltage swing across pins to ensure switching between logic levels as measured with a differential probe
Common-Mode Input Voltage	0.3		0.4	V	Allowable common-mode voltage for dc coupling
Single-Ended Input Resistance		55		Ω	Input resistance measured from each REFx pin to GND
Input Capacitance		3		pF	Input capacitance measured from each REFx pin to GND
AC-COUPLED CML MODE (REFA, $\overline{REFA}$, REFB, $\overline{REFB}$)					AC-coupled mode (REFx_TERM_SEL = 10); includes an internal termination of 50 Ω from each REFx input to a nominal dc bias of 0.35 V
Input Frequency	6		800	MHz	Assumes a minimum of 494 mV p-p differential amplitude as measured with a differential probe at the REFx input pins
Input Sensitivity	494			mV p-p	Peak-to-peak differential voltage swing across pins to ensure switching between logic levels as measured with a differential probe
Input Self Bias Voltage (VTT) (Internally Generated)	0.32	0.355	0.39	V	Self bias voltage of the REFx and $\overline{REFx}$ inputs in ac-coupled mode (REFx_TERM_SEL = 10)
Differential Input Resistance		105		Ω	Differential input resistance measured across the REFx and $\overline{REFx}$ pins
Input Capacitance		3		pF	Input capacitance measured from each REFx pin to GND
DC-COUPLED HIGH-Z MODE (REFA, $\overline{REFA}$, REFB, $\overline{REFB}$)					DC-coupled high-Z mode (REFx_TERM_SEL = 11) places the REFx inputs into a high impedance state; inputs are not self biased in this setting
Input Frequency	6		800	MHz	Assumes a minimum of 500 mV p-p differential amplitude as measured with a differential probe at the REFx input pins
Input Sensitivity	494			mV p-p	Peak-to-peak differential voltage swing across pins to ensure switching between logic levels as measured with a differential probe
Common-Mode Input Voltage	0.4		1.4	V	
Differential Input Resistance		10.3		kΩ	Differential input resistance measured across the REFx and $\overline{REFx}$ pins
Input Capacitance		3		pF	Input capacitance measured from each REFx pin to GND

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DUTY CYCLE					Duty cycle bounds are set by pulse width high and pulse width low
Pulse Width					
Low	600			ps	
High	600			ps	

PLL CHARACTERISTICS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RTWO					
Frequency Range	5.11		5.4	GHz	
VCO Gain (K_{VCO})		180		MHz/V	
PHASE FREQUENCY DETECTOR (PFD)					
PFD Input Frequency	6		800	MHz	Antibacklash pulse width disabled (Register 0x026, Bit 1 = 0)
	6		500	MHz	Antibacklash pulse width enabled (Register 0x026, Bit 1 = 1)
CHARGE PUMP (CP)					
Sink/Source Current (I_{CP})	0.05		2.6	mA	Register 0x025, Bits[5:0] controls the charge pump current (see Table 56)
LOOP FILTER					
External Loop Filter Capacitor			3.2	µF	Maximum value for the C2 capacitor in Figure 16; using a loop filter capacitor value larger than the maximum may affect device functionality
POWER-ON RESET (POR) TIMER					
Internal Wait Time	2			sec	Minimum wait time implemented before issuing the first RTWO calibration after a POR

PLL DIGITAL LOCK DETECT SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PLL DIGITAL LOCK DETECT WINDOW[1]					Signal available at the LD pin and in Register 0x01F, Bit 2
Lock Threshold	±0.020		±300	ppm	Lock threshold is selected by Register 0x01D, Bits[3:1], which is the threshold for transitioning from unlock to lock and vice versa

[1] For reliable operation of the digital lock detect, the period of the PFD frequency must be greater than the lock detector update interval (see Table 48).

CLOCK OUTPUTS (INTERNAL TERMINATION DISABLED) SPECIFICATIONS

Table 7.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML MODE					All outputs are externally terminated with 50 Ω to VDD
800 mV					
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		78	107	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	51	54	%	Mx divider = 2, output divider = 1
	45	51	57	%	Mx divider = 2.5, output divider = 1
	48	50	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	600	845	1090	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.82	2.075	2.32	V	Measured with output driver static

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
900 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		77	98	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	51	54	%	Mx divider = 2, output divider = 1
	45	51	57	%	Mx divider = 2.5, output divider = 1
	49	51	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	675	950	1340	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.76	2.03	2.29	V	Measured with output driver static
1000 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		76	105	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	51	54	%	Mx divider = 2, output divider = 1
	45	51	57	%	Mx divider = 2.5, output divider = 1
	49	51	52	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	730	1040	1340	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.69	1.97	2.25	V	
1100 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		76	104	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	51	54	%	Mx divider = 2, output divider = 1
	45	51	57	%	Mx divider = 2.5, output divider = 1
	49	50	52	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	815	1140	1480	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.61	1.92	2.22	V	Measured with output driver static

CLOCK OUTPUTS (INTERNAL TERMINATION ENABLED) SPECIFICATIONS

Table 8.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML MODE					All outputs are externally terminated with 50 Ω to VDD
800 mV					
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		55	75	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	52	56	%	Mx divider = 2, output divider = 1
	43	51	60	%	Mx divider = 2.5, output divider = 1
	48	51	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	590	830	1070	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.9	2.08	2.26	V	Measured with output driver static

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
900 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		53	70	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	48	52	56	%	Mx divider = 2, output divider = 1
	43	51	60	%	Mx divider = 2.5, output divider = 1
	48	51	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	660	930	1200	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.83	2.03	2.23	V	Measured with output driver static
1000 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		53	71	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	47	52	56	%	Mx divider = 2, output divider = 1
	43	52	60	%	Mx divider = 2.5, output divider = 1
	48	51	53	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	735	1025	1335	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.83	2.03	2.23	V	Measured with output driver static
1100 mV					All outputs are externally terminated with 50 Ω to VDD
Output Frequency	5.725		2700	MHz	
Rise Time/Fall Time (20% to 80%)		53	72	ps	
Duty Cycle	47		53	%	Any Mx divider, output divider ≠ 1
	47	52	56	%	Mx divider = 2, output divider = 1
	43	52	60	%	Mx divider = 2.5, output divider = 1
	48	51	54	%	Mx divider = 3, output divider = 1
Output Differential Voltage, Magnitude	810	1125	1455	mV	Voltage difference between the output pins; output driver is static; in normal operation, the peak-to-peak amplitude is approximately 2× this value if measured with a differential probe
Common-Mode Output Voltage	1.71	1.93	2.23	V	Measured with output driver static
INTERNAL OUTPUT TERMINATION RESISTANCE		53.7		Ω	Measured with output driver static

CLOCK OUTPUT ABSOLUTE TIME JITTER (LOW LOOP BANDWIDTH) SPECIFICATIONS

Table 9.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML OUTPUT ABSOLUTE TIME JITTER					REFA enabled and ac-coupled; R divider = 1; Mx divider value varies; loop bandwidth = 8 kHz; output divider bypassed unless otherwise noted; single-ended output swing level = 1000 mV; no internal termination; VCO in high power mode, integration bandwidth = 12 kHz to 20 MHz
f_{OUT} = 2700 MHz		219		fs rms	Reference frequency = 100 MHz, Mx divider = 2
f_{OUT} = 2100 MHz		220		fs rms	Reference frequency = 100 MHz, Mx divider = 2.5
f_{OUT} = 2050 MHz		214		fs rms	Reference frequency = 102.5 MHz, Mx divider = 2.5
f_{OUT} = 1768 MHz		219		fs rms	Reference frequency = 104 MHz, Mx divider = 3
f_{OUT} = 1500 MHz		210		fs rms	Reference frequency = 100 MHz, Mx divider = 3.5
f_{OUT} = 100 MHz		232		fs rms	Reference frequency = 100 MHz, Mx divider = 3, output divider (Dx divider) = 17

CLOCK OUTPUT ABSOLUTE TIME JITTER (HIGH LOOP BANDWIDTH) SPECIFICATIONS

Table 10.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CML OUTPUT ABSOLUTE TIME JITTER		93		fs rms	REFA enabled and ac-coupled; R divider = 1; Mx divider value = 2; loop bandwidth = 80 kHz; output divider bypassed; single-ended output swing level = 1000 mV; no internal termination; VCO in high power mode; reference frequency = 860 MHz; output frequency = 2.58 GHz; integration bandwidth = 12 kHz to 20 MHz; absolute jitter value also depends on the noise of the input clock in the 12 kHz to 80 kHz range

$\overline{\text{RESET}}$ AND REF_SEL PINS SPECIFICATIONS

Table 11.

Parameter	Min	Typ	Max	Unit
INPUT CHARACTERISTICS				
Voltage				
Logic 1	V_{DD} − 0.5		V_{DD}	V
Logic 0			0.5	V
Current				
Logic 1		1		µA
Logic 0		36		µA
Capacitance		3		pF
RESET TIMING				
Pulse Width Low	100			ns
$\overline{\text{RESET}}$ Inactive to Start of Register Programming	50			ms

LD PIN SPECIFICATIONS

Table 12.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS						1 mA output load
Output Voltage						
High	V_{OH}	V_{DD} − 0.5			V	
Low	V_{OL}			0.5	V	

SERIAL CONTROL PORT SPECIFICATIONS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$\overline{\text{CS}}$ (INPUT)						$\overline{\text{CS}}$ has an internal 75 kΩ pull-up resistor
Input Voltage						
Logic 1		V_{DD} − 0.4			V	
Logic 0				0.4	V	
Input Current						
Logic 1			1		µA	
Logic 0			32		µA	
Input Capacitance			3		pF	
SCLK (INPUT)						SCLK has an internal 75 kΩ pull-down resistor
Input Voltage						
Logic 1		V_{DD} − 0.4			V	
Logic 0				0.4	V	
Input Current						
Logic 1			45		µA	
Logic 0			1		µA	
Input Capacitance			3		pF	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SDIO (INPUT)						
Input Voltage						
Logic 1		V_{DD} − 0.4			V	
Logic 0				0.4	V	
Input Current						
Logic 1			1		µA	
Logic 0			1		µA	
Input Capacitance			3		pF	
SDIO, SDO (OUTPUTS)						1 mA load current
Output Voltage						
Logic 1		V_{DD} − 0.2			V	
Logic 0				0.2	V	
TIMING						See Figure 26 through Figure 30 and Table 21
Clock Rate (SCLK)	$1/t_{SCLK}$			40	MHz	
Pulse Width High	t_{HIGH}	6			ns	
Pulse Width Low	t_{LOW}	6			ns	
SDIO to SCLK Setup	t_{DS}	1.8			ns	
SCLK to SDIO Hold	t_{DH}	0.6			ns	
SCLK to Valid SDIO and SDO	t_{DV}			10	ns	
$\overline{CS}$ to SCLK Setup	t_S	0.6			ns	
$\overline{CS}$ to SCLK Hold	t_H	3.5			ns	
$\overline{CS}$ Minimum Pulse Width High	t_{PWH}	1.5			ns	

ABSOLUTE MAXIMUM RATINGS

Table 14.

Parameter	Rating
VDD, BP_CAP_1, BP_CAP_2, BP_CAP_3, REFA, $\overline{\text{REFA}}$, REFB, $\overline{\text{REFB}}$, SCLK, SDIO, SDO, $\overline{\text{CS}}$, OUT1, $\overline{\text{OUT1}}$, OUT2, $\overline{\text{OUT2}}$, OUT3, $\overline{\text{OUT3}}$, OUT4, $\overline{\text{OUT4}}$, $\overline{\text{RESET}}$, and REF_SEL to GND	2.625 V
Junction Temperature[1]	150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (10 sec)	300°C

[1] See Table 15 for θ_{JA}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 15. Thermal Resistance (Simulated)

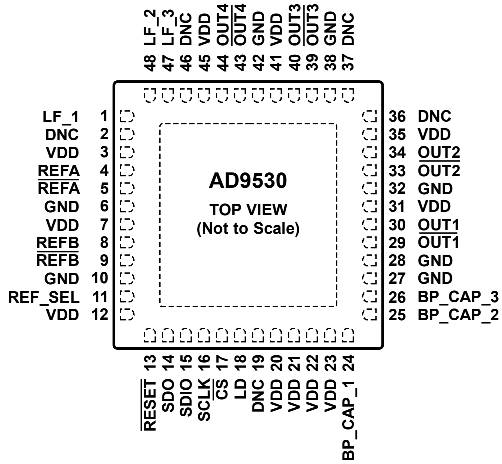
Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3,4]	θ_{JB}[1,4,5]	Ψ_{JT}[1,2,4]	Unit
48-Lead LFCSP	0	25.8	2.8	7.5	0.20	°C/W
	1.0	22.2	N/A	N/A	N/A	°C/W
	2.5	19.7	N/A	N/A	N/A	°C/W

[1] Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] N/A means not applicable.
[5] Per JEDEC JESD51-8 (still air).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT TO THESE PINS.
2. THE EXPOSED PAD IS A GROUND CONNECTION ON THE CHIP THAT MUST BE SOLDERED TO THE ANALOG GROUND OF THE PCB TO ENSURE PROPER FUNCTIONALITY AND HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

14044-003

Figure 2. Pin Configuration

Table 16. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	LF_1	O	Loop Filter Connection, Negative Output Side of the Active Loop Filter Op Amp. Connect the PLL active loop filter components (R1, C1, and C2) to this pin and LF_2 (Pin 48).
2, 19, 36, 37, 46	DNC	N/A	Do Not Connect. Do not connect to this pin.
3	VDD	P	Power Supply for REFA.
4	REFA	I	Reference Clock Input A. This pin, along with $\overline{\text{REFA}}$, is the first differential reference input for the PLL.
5	$\overline{\text{REFA}}$	I	Complimentary Reference Clock Input A. This pin, along with REFA, is the first differential reference input for the PLL.
6	GND	GND	Ground for the REFA Power Supply. Connect this pin to ground.
7	VDD	P	Power Supply for REFB.
8	REFB	I	Reference Clock Input B. This pin, along with $\overline{\text{REFB}}$, is the second differential reference input for the PLL.
9	$\overline{\text{REFB}}$	I	Complimentary Reference Clock Input B. This pin, along with REFB, is the second differential reference input for the PLL.
10	GND	GND	Ground for the REFB Power Supply. Connect this pin to ground.
11	REF_SEL	I	Reference Input Select. This pin is the digital input to select REFA or REFB as the active reference to the PLL. This pin has an internal 75 kΩ pull-up resistor. Logic high (default) selects REFA. Logic low selects REFB.
12	VDD	P	Power Supply for the Serial Port Interface (SPI) and the PFD.
13	$\overline{\text{RESET}}$	I	Chip Reset, Active Low. This pin has an internal 75 kΩ pull-up resistor.
14	SDO	O	Serial Control Port Unidirectional Serial Data Output. This pin is high impedance during 3-wire SPI mode.
15	SDIO	I/O	Serial Control Port Bidirectional Serial Data Input/Output.
16	SCLK	I	Serial Control Port Clock Signal. This pin has an internal 75 kΩ pull-down resistor.
17	$\overline{\text{CS}}$	I	Serial Control Port Chip Select, Active Low. This pin has an internal 75 kΩ pull-up resistor.
18	LD	O	PLL Lock Detect Output.
20 to 23	VDD	P	2.5 V Power Supply for the RTWO Internal LDO.
24	BP_CAP_1	O	RTWO LDO Op Amp Bypass Capacitor. Connect an external 0.01 μF capacitor from this pin to GND.
25	BP_CAP_2	O	RTWO LDO Bypass Capacitor. Connect an external 1 μF capacitor from this pin to GND.
26	BP_CAP_3	O	RTWO Bias Supply Bypass Capacitor. This pin can be left unconnected (floating).
27	GND	GND	Ground for RTWO Power Supply. Connect this pin to ground.
28	GND	GND	Ground for OUT1 Power Supply. Connect this pin to ground.

Pin No.	Mnemonic	Type[1]	Description
29	$\overline{\text{OUT1}}$	O	CML Complementary Output 1. This pin requires a 50 Ω to VDD termination even if the output is unused. See the CML Output Drivers section for more information.
30	OUT1	O	CML Output 1. This pin requires a 50 Ω termination to VDD, even if the output is unused. See the CML Output Drivers section for more information.
31	VDD	P	Power Supply for OUT1.
32	GND	GND	Ground for OUT2 Power Supply. Connect this pin to ground.
33	$\overline{\text{OUT2}}$	O	CML Complementary Output 2.
34	OUT2	O	CML Output 2.
35	VDD	P	Power Supply for OUT2.
38	GND	GND	Ground for OUT3 Power Supply. Connect this pin to ground.
39	$\overline{\text{OUT3}}$	O	CML Complementary Output 3.
40	OUT3	O	CML Output 3.
41	VDD	P	Power Supply for OUT3.
42	GND	GND	Ground for OUT4 Power Supply. Connect this pin to ground.
43	$\overline{\text{OUT4}}$	O	CML Complementary Output 4.
44	OUT4	O	CML Output 4.
45	VDD	P	Power Supply for OUT4.
47	LF_3	O	Loop Filter Connection. Connect an external capacitor (C_A) between this pin and ground.
48	LF_2	O	Loop Filter Connection. This pin is the output side of the active loop filter op amp. Connect the PLL active loop filter components (R1, C1, and C2) to this pin and LF_1 (Pin 1).
	EP	GND	Exposed Pad. The exposed pad is a ground connection on the chip that must be soldered to the analog ground of the printed circuit board (PCB) to ensure proper functionality and heat dissipation, noise, and mechanical strength benefits.

[1] O means output, N/A means not applicable, P means power, I means input, GND means ground, and I/O means input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

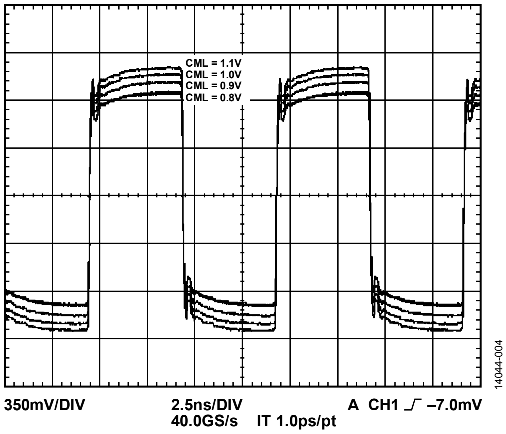


Figure 3. CML Output Waveform (Differential) at 101 MHz, Internal Termination Disabled

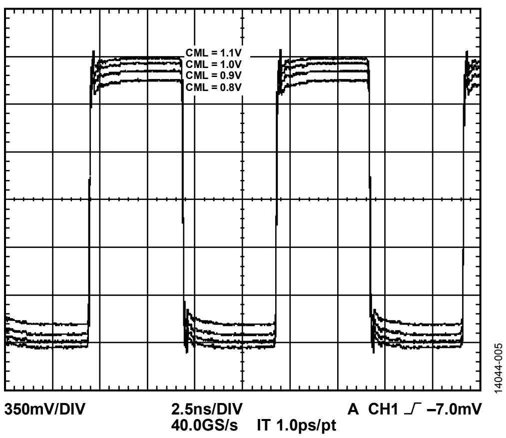


Figure 4. CML Output Waveform (Differential) at 101 MHz, Internal Termination Enabled

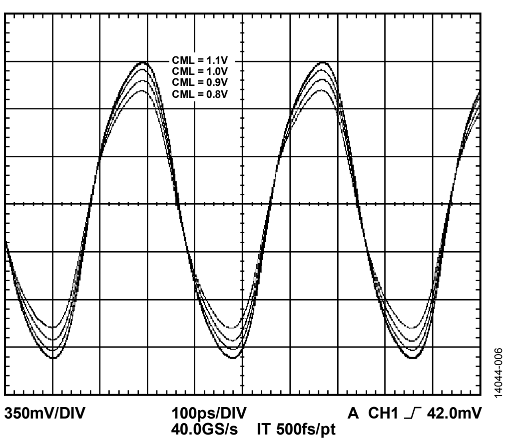


Figure 5. CML Output Waveform (Differential) at 2650 MHz, Internal Termination Disabled

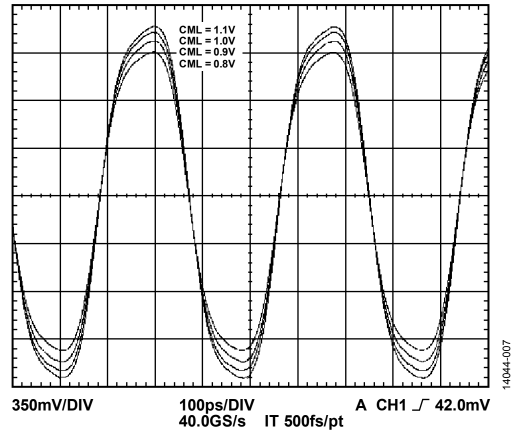


Figure 6. CML Output Waveform (Differential) at 2650 MHz, Internal Termination Enabled

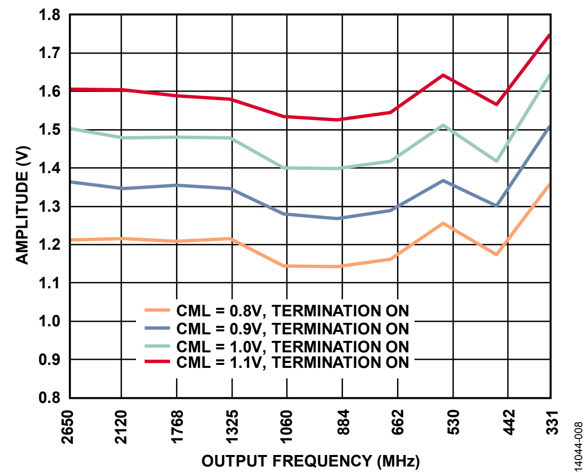


Figure 7. Differential Voltage Amplitude vs. Output Frequency, Internal Termination Enabled

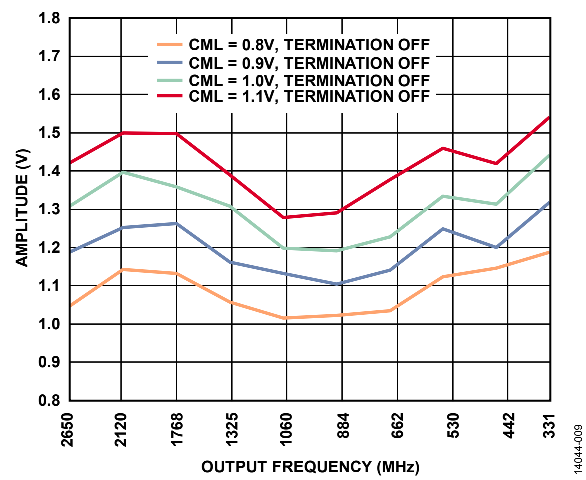


Figure 8. Differential Voltage Amplitude vs. Output Frequency, Internal Termination Disabled

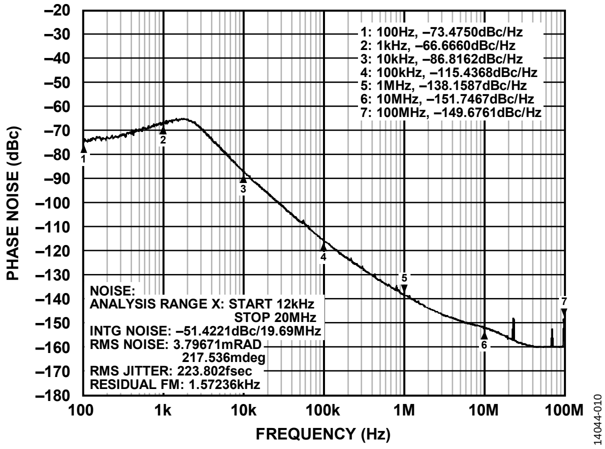


Figure 9. Phase Noise, f_{OUT} = 2.7 GHz, Loop Bandwidth = 8 kHz

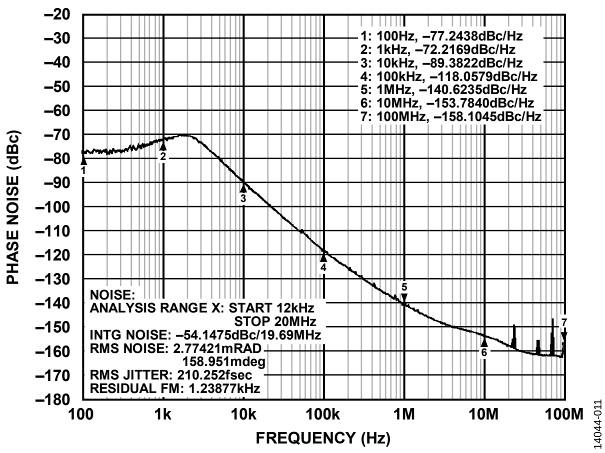


Figure 10. Phase Noise, f_{OUT} = 2.1 GHz, Loop Bandwidth = 8 kHz

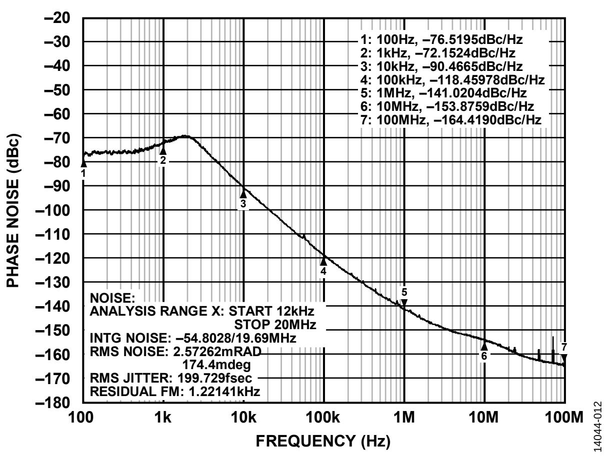


Figure 11. Phase Noise, f_{OUT} = 2.05 GHz, Loop Bandwidth = 8 kHz

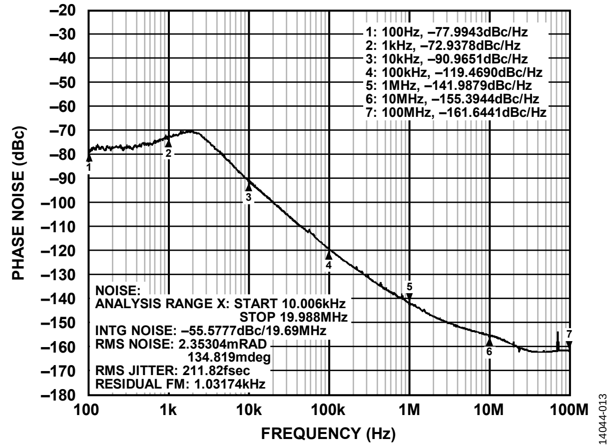


Figure 12. Phase Noise, f_{OUT} = 1.768 GHz, Loop Bandwidth = 8 kHz

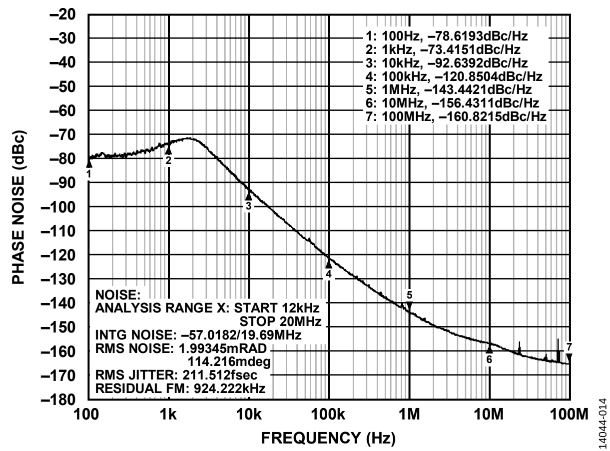


Figure 13. Phase Noise, f_{OUT} = 1.5 GHz, Loop Bandwidth = 8 kHz, High Performance Mode

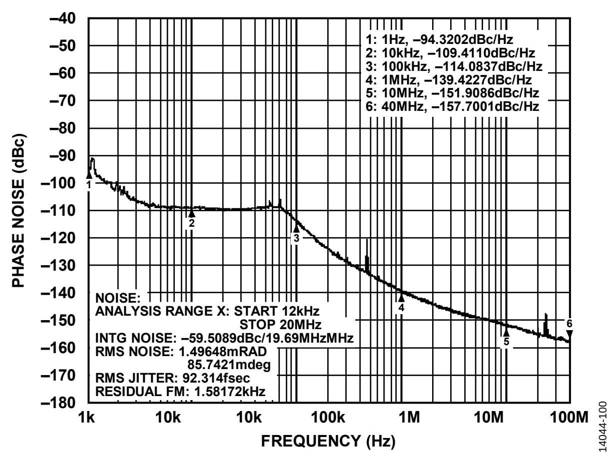


Figure 14. Phase Noise, f_{IN} = 860 MHz, f_{OUT} = 2.58 GHz, Loop Bandwidth = 80 kHz, I_{CP} = 2.4 mA, High Performance Mode

TERMINOLOGY

Phase Jitter

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time, and this phenomenon is called phase jitter. Although many factors can contribute to phase jitter, one major factor is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

Phase jitter leads to a spreading out of the energy of the sine wave in the frequency domain, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Absolute Phase Noise

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is called the integrated phase noise over that frequency offset interval; it is related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways. Absolute phase noise is the actual measured noise from the AD9530, and includes the input reference and power supply noise.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that can be attributed to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted, making it possible to predict the degree to which the device impacts the total system phase noise when used in conjunction with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that can be attributed to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is not a part of this jitter number. This makes it possible to predict the degree to which the device impacts the total system time jitter when used in conjunction with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

DETAILED FUNCTIONAL BLOCK DIAGRAM

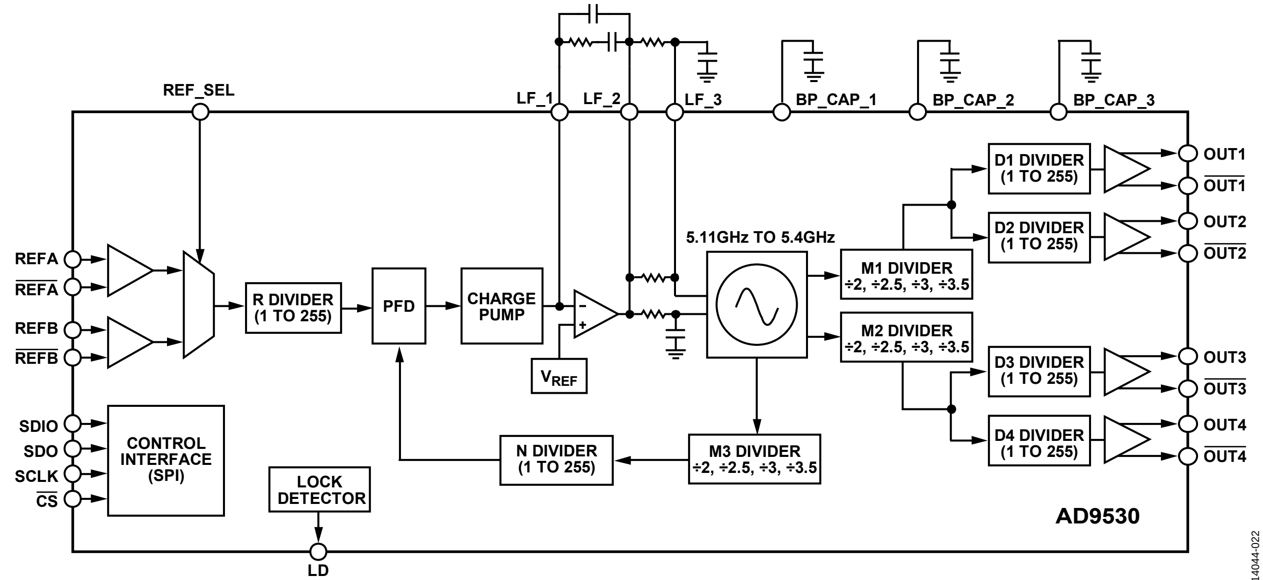


Figure 15. Detailed Functional Block Diagram

OVERVIEW

The AD9530 is a fully integrated, integer-N PLL with an ultralow noise, internal 5.11 GHz to 5.4 GHz RTWO capable of generating <232 fs rms, (12 kHz to 20 MHz) jitter clocking signals with a nonideal reference. The AD9530 is tailored for 40 Gbps and 100 Gbps OTN applications with stringent converter and ASIC clocking specifications.

The AD9530 includes an on-chip PLL, an internal RTWO, and four output channels with integrated dividers and CML drivers. The PLL contains a partially internal active loop filter, which requires a small number of external components to obtain loop bandwidths lower than 15 kHz for reference phase noise attenuation.

The four outputs of the AD9530 feature individual dividers to generate four separate frequencies up to 2.7 GHz.

CONFIGURATION OF THE PLL

Configuration of the PLL is accomplished by programming the various settings for the R divider, N divider, M3 divider, charge pump current, and a calibration of the RTWO. The combination of these settings and the loop filter determine the PLL loop bandwidth and stability.

Successful PLL operation and satisfactory PLL loop performance are highly dependent on proper configuration of the internal PLL settings and loop filter. ADIsimCLK™ is a free program that helps the design and exploration of the capabilities and features of the AD9530, including the design of the PLL loop filter.

Phase Frequency Detector (PFD)

The PFD takes inputs from the R divider output and the feedback divider path to produce an output proportional to the phase and frequency difference between them. The PFD includes an adjustable delay element that controls the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and minimizes phase noise and reference spurs.

The maximum allowable input frequency into the PFD is specified in the PFD parameter in Table 5.

Charge Pump (CP)

The CP is controlled by the PFD. The PFD monitors the phase and frequency relationship between its two inputs and causes the CP to pump up or pump down to charge or discharge, respectively, the integrating node, which is part of the loop filter. The integrated and filtered CP current is transformed into a voltage that drives the tuning node of the RTWO to move the RTWO frequency up or down. The CP current is programmable in 52 steps, where each step corresponds to a current increase of 50 µA. Calculate the CP current (I_{CP}) by

$$I_{CP}\ (\mu A) = 50 \times (1 + x)$$

where x is the value written to Register 0x025, Bits[5:0].

PLL Active Loop Filter

The AD9530 active loop filter consists of an internal op amp, internal passive components, and external passive components. Proper loop filter configuration is application dependent. An example of a second-order loop filter is shown in Figure 16.

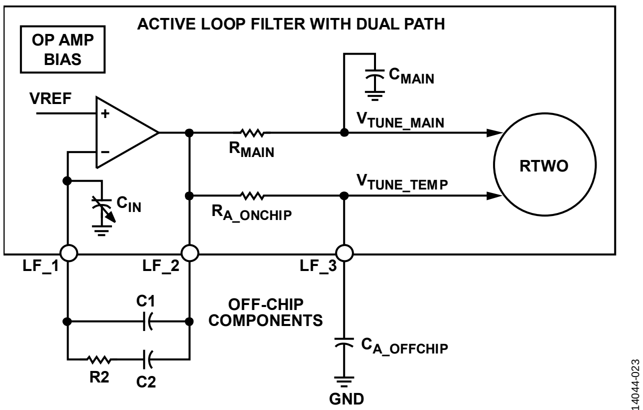


Figure 16. External Second-Order Loop Filer Configuration

C1, C2, $C_{A\_OFFCHIP}$, and R2 are external components required for proper loop filter operation. All internal loop filter components (R_{MAIN}, R_{A_ONCHIP}, C_{MAIN}) are fixed with the exception of C_{IN}, which has available settings of 5 pF to 192.5 pF by programming Register 0x027, Bits[5:2]. This capacitance setting alters the bandwidth of the loop filter op amp. C_{IN} is composed of a fixed 5 pF capacitor and a bank of 15 selectable 12.5 pF capacitors. Calculate the C_{IN} value by

$$C_{IN} = 5\text{ pF} + 12.5\text{ pF} \times \textit{Register 0x027, Bits[5:2]}$$

Note that R_{MAIN} and C_{MAIN} in Figure 16 form a pole at approximately 2 MHz.

Table 17 shows the typical loop filter component values and CP settings for an 8 kHz loop bandwidth.

The maximum allowable capacitance value for the external loop filter design is shown in Table 5. Exceeding this value may cause various functions of the AD9530 to become unstable.

Use the ADIsimCLK design tool to design and simulate loop filters with varying bandwidths.

PLL Reference Inputs

The AD9530 features two fully differential PLL reference inputs that are routed through a 2:1 mux to a common R divider. The differential reference input receiver has four internal termination/biasing options to accommodate many input logic types. A functional diagram of the reference input receiver is shown in Figure 17. Table 18 details the four possible reference input termination and common-mode settings achievable by writing to Register 0x012, Bits[3:2] and Register 0x013, Bits[3:2]. The input frequency specifications for the reference inputs are listed in Table 4.

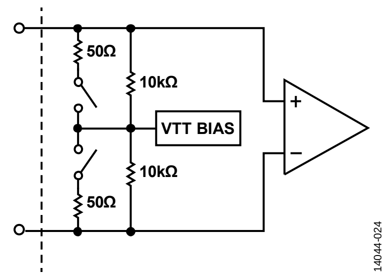


Figure 17. Reference Input Receiver Functional Diagram

Each REFx/$\overline{\text{REFx}}$ receiver can be disabled by setting the associated reference enable bit to 0.

RTWO

The internal RTWO tunes from 5.11 GHz to 5.4 GHz and is powered by the VDD supply pins (Pin 20 to Pin 23). The RTWO has two modes: high performance mode and low power mode. These modes are set by Register 0x01C, Bit 0. These modes enable optimization between the phase noise performance and power consumption. See the Power Supply Recommendations section for a recommended power supply configuration for Pin 20 to Pin 23.

Table 17. Typical Loop Filter Components and I_{CP} Settings for 8 kHz Loop Bandwidth

Reference (MHz)	R Divider	Feedback Divider (N × M3)	C1 (nF)	C2 (µF)	R2 (Ω)	$C_{A\_OFFCHIP}$ (µF)	I_{CP} (mA)
181.5	÷1	÷30	10	0.47	255	0.1	0.3

Table 18. Possible Reference Input Termination Settings

Mode Name	REFx/$\overline{\text{REFx}}$ Input Termination Select Settings	On-Chip Termination	Common-Mode Bias
DC-Coupled LVDS	00	100 Ω differential	High-Z
DC-Coupled, Internally Biased	01 (default)	50 Ω to GND	GND
AC-Coupled	10	50 Ω to 0.35 V	0.35 V
DC-Coupled High-Z	11	10 kΩ to GND	GND

RTWO Calibration

The RTWO calibration function selects the appropriate RTWO frequency band for a given configuration. A calibration is performed by toggling Register 0x001, Bit 2 from 0 to 1. The command sequence to issue a VCO calibration is as follows:

1. Write the desired AD9530 configuration, including the divider and output driver settings.
2. Set Register 0x001, Bit 2 = 0 (CALIBRATE VCO bit). Note that this is a self clearing bit.

A calibration is required after initial power-up, after subsequent resets, and after any changes to the input reference frequency or the divide settings that affect the RTWO operating frequency. A 2 sec wait timer is activated at power-up to gate the first calibration. This wait time is not enforced for subsequent calibrations after power-on. See the CML Output Drivers section for more details. The PLL reference must be active and stable and the PLL must be configured to a valid operational state prior to issuing a calibration. After a calibration, all of the internal dividers are synchronized automatically to ensure proper phase alignment of the PLL and distribution.

Reference Switchover

The AD9530 supports two separate differential reference inputs. Manual switchover is performed between these inputs by either writing to Register 0x011, Bit 2 and Bit 1, or by using the REF_SEL pin. Register 0x011, Bit 2 sets whether the REF_SEL pin or the reference select register controls the reference input mux. Default operation ignores the REF_SEL pin setting and uses the value of Register 0x011, Bit 1.

Dividers (R, Mx, N, and Dx)

The AD9530 contains multiple dividers that configure the PLL for a given frequency plan. Each divider has an associated reset bit that is self clearing. Resetting a divider is required every time the divide value of that driver is changed. Issuing a reset of a single divider does not clear the current divide value.

Reference Divider (R Divider)

The reference inputs are routed through a 2:1 mux into a common 8-bit R divider. R can be set to any value from 1 to 255 (Register 0x010, Bits[7:0]). Setting Register 0x010 = 0x0A is equivalent to an R divider setting of 10.

The frequency out of the R divider must not exceed the maximum allowable frequency of the PFD listed in Table 5.

The R divider has its own reset located in Register 0x011. This reset bit is self clearing.

M3 and N Feedback Dividers

The total feedback division from the RTWO to the PFD is the product of the M3 and N dividers. The N divider (Register 0x023, Bits[7:0]) functions identically to the R divider described in the Reference Divider (R Divider) section. The M3 divider (Register 0x022, Bits[3:2]) is limited to fixed divide values of 2, 2.5, 3, and 3.5 and acts as a prescaler to the N divider. The M3 and N dividers have individual resets located at Register 0x022, Bit 0, and Register 0x024, Bit 0, respectively.

M1 and M2 Dividers (M1 and M2)

The M1 and M2 dividers (Register 0x020, Bits[4:3] and Register 0x021, Bits[4:3], respectively) have fixed divide values of 2, 2.5, 3, and 3.5.

The M1 and M2 dividers provide frequency division between the RTWO output and the clock distribution channel dividers (Dx).

The M1 and M2 dividers have individual resets located at Register 0x020, Bit 0, and Register 0x021, Bit 0, respectively.

Channel Dividers (Dx)

The AD9530 has four 8-bit channel dividers (Dx) which are identical to the R and N dividers. Dx can be set to any value from 1 to 255. Setting the divide value for D1 through D4 is accomplished by writing Register 0x014, Register 0x016, Register 0x018, and Register 0x01A, respectively. The D1 through D4 reset bits that reset D1 through D4 are located in Bit 0 of Register 0x015, Register 0x017, Register 0x019, and Register 0x01B, respectively. A setting of 0 disables the divider.

Dividers Sync

Use a sync to phase align all of the AD9530 internal dividers to a common point in time. A global sync of all dividers is performed after a VCO calibration. To perform a VCO calibration, write a 1 to Bit 2 of Register 0x001. A VCO calibration must be performed after power up, as well as any time a different VCO frequency is selected.

To sync all of the dividers after programming them, without the VCO frequency, write a 1 to Bit 1 of Register 0x001.

Lock Detector

The AD9530 features a frequency lock detect signal that corresponds to whether the PLL reference and feedback edges are within a certain frequency of one another. The exact frequency lock threshold to indicate a PLL lock is user programmable in Register 0x01D, Bits[3:1]. The three register bits allow the frequency lock threshold to span ±20 ppb to ±300 ppm.

If the frequency error between the reference and feedback edges is lower than the specified lock threshold, the LD pin goes high and the PLL_LOCKED bit = 1. The LD pin and the PLL_LOCKED bit go low when the error between the reference and feedback edges is greater than the frequency lock threshold.

The lock detector also outputs an 11-bit word located in Register 0x01E, Bits[7:0] and Register 0x01F, Bits[1:0]. Bit 10 through Bit 0 contain a binary value representative of the measured frequency lock error, and Bit 11 indicates whether the 10-bit value is expressed in ppm (parts per million) or ppb (parts per billion). Note that this 11^{th} bit is found in Register 0x01F, Bit 3.

CML Output Drivers

The AD9530 has four CML output drivers that are operable up to 2.7 GHz. Each output driver must be externally terminated as shown in the Input/Output Termination Recommendations section. The output voltage swing, internal termination, and power-down of each CML driver are configurable by writing to the appropriate registers. An initial calibration of the internal termination and voltage swing is performed after a POR event. This calibration requires that OUT1 is terminated, regardless of whether the driver is needed in a specific design. A functional diagram of the output driver is shown in Figure 18.

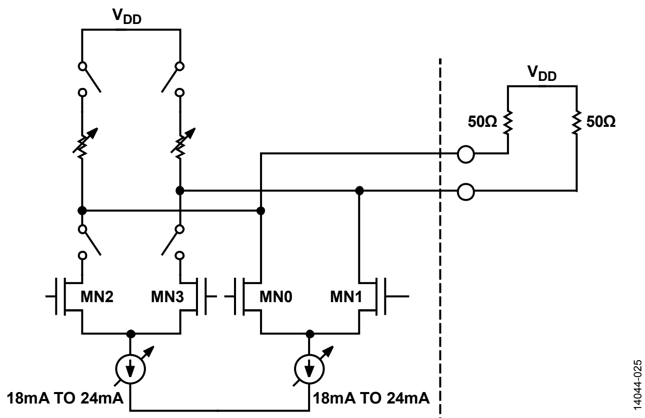


Figure 18. CML Output Simplified Equivalent Circuit

The CML differential voltage (V_{OD}) is selectable from 0.8 V to 1.1 V via Bits[5:4] of Register 0x015, Register 0x017, Register 0x019, and Register 0x01B.

The AD9530 has optional internal termination for cases where transmission line impedance mismatch between the CML output and the receiver causes increased reflections at high output frequencies. These terminations improve impedance match traces at high frequency at the expense of drawing twice as much current as the default operating condition.

For Register 0x015 (for OUT1), Register 0x017 (for OUT2), Register 0x019 (for OUT3), and Register 0x01B (for OUT4), setting the OUTx_TERM_EN (Bit 3) = 1 enables the on-chip termination and is configurable for each driver.

Each CML output can be enabled as needed by altering the appropriate OUTx_ENABLE bit.

RESET MODES

The AD9530 has a POR and several other ways to apply a reset condition to the chip.

Power-On Reset (POR)

During chip power-up, a POR pulse is issued when VDD reaches ~2 V and restores the chip to the default on-chip setting. At this point, a 2 sec counter is started to allow all the user device settings to load and the RTWO to stabilize. After the 2 sec counter finishes, the user can issue a VCO calibration and outputs begin toggling ~500 ns later.

2 sec Wait Timer

The 2 sec wait timer ensures that all internal supplies are stable before allowing the user to issue a VCO calibration. This timer only starts after a POR. The user may program all the necessary registers during this time, including the VCO calibration bit. After the timer times out and a reference input is applied, the calibration issues, allowing the PLL to lock and the outputs to toggle. The maximum internal wait time is shown in Table 5.

Hardware Reset via the $\overline{\text{RESET}}$ Pin

Driving the $\overline{\text{RESET}}$ pin to a Logic 0 and then back to a Logic 1 restores the chip to the on-chip default register settings.

Soft Reset via the Serial Port

The serial port control register allows a soft reset by setting Register 0x000, Bit 7 and Bit 1. When these bits are set, the chip restores to the on-chip default settings, except for Register 0x000 and Register 0x001. Register 0x000 and Register 0x001 retain the values prior to reset, except for the self clearing bits. However, the self clearing operation does not complete until an additional serial port SCLK cycle occurs; the AD9530 is held in reset until this additional SCLK cycle.

Individual Divider Reset via the Serial Port

Every divider in the AD9530 has the ability to reset individually by using the appropriate reset bit. This reset does not clear the value written in the specific divider register but restarts the divider count to 0, which results in a phase adjustment. See the associated divider section or the register map for the location of these bits.

POWER-DOWN MODES

Sleep Mode via the Serial Port

Place the AD9530 in sleep mode by writing Register 0x002, Bits[1:0] = 11. This mode powers down the following blocks:

- All OUTx drivers
- All REFx inputs
- All Mx dividers
- RTWO power set to minimum
- CP current set to minimum
- PFD
- Loop filter op amp

Individual Clock Input and Output Power-Down

Power down any of the reference inputs or clock distribution outputs by individually writing to the appropriate registers. The register map details the individual power-down settings for each input and output.

INPUT/OUTPUT TERMINATION RECOMMENDATIONS

Figure 19 through Figure 24 illustrate the recommended input and output connections for connecting the AD9530 to other devices.

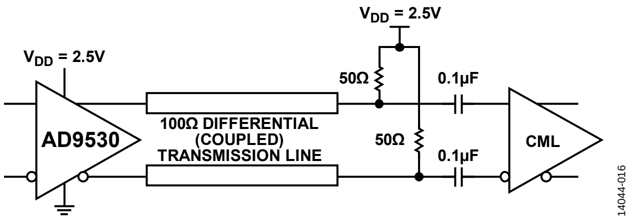


Figure 19. CML AC-Coupled Output Driver (External Termination Required When Using the Internal Termination Option)

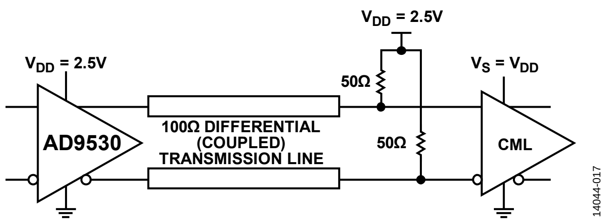


Figure 20. CML DC-Coupled Output Driver (External Termination Required When Using the Internal Termination Option)

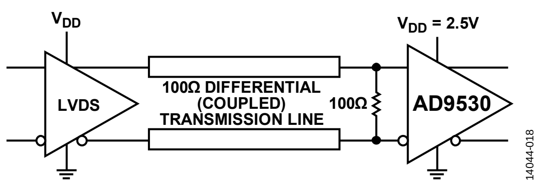


Figure 21. REFx Input Termination Recommendation for LVDS Drivers

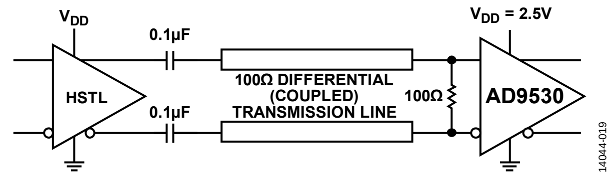


Figure 22. REFx Input Termination Recommendation for High Speed Transceiver Logic (HSTL) Drivers

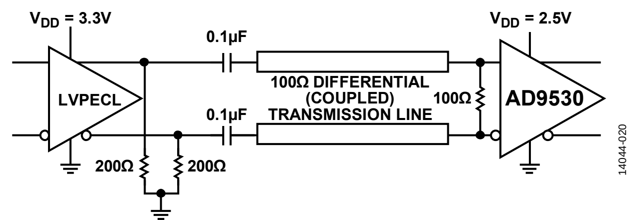


Figure 23. REFx Input Termination Recommendation for 3.3V LVPECL Drivers

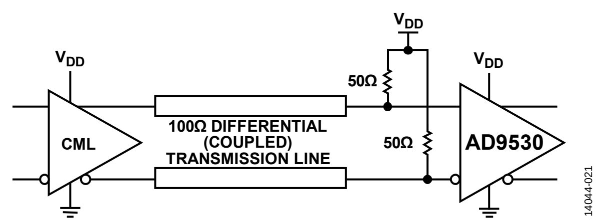


Figure 24. REFx Input Termination Recommendation for 2.5V CML Drivers

SERIAL CONTROL PORT

The AD9530 serial control port is a flexible, synchronous serial communications port that provides a convenient interface to many industry-standard microcontrollers and microprocessors. The serial control port allows read/write access to the AD9530 register map.

The AD9530 uses the Analog Devices, Inc., unified SPI protocol. The unified SPI protocol guarantees that all new Analog Devices products using the unified protocol have consistent serial port characteristics. The SPI port configuration is programmable via Register 0x0000. This register is a part of the SPI control logic rather than in the register map.

SPI SERIAL PORT OPERATION

Pin Descriptions

The SCLK (serial clock) pin serves as the serial shift clock. This pin is an input. SCLK synchronizes serial control port read and write operations. The rising edge SCLK registers write data bits, and the falling edge registers read data bits. The SCLK pin supports a maximum clock rate of 40 MHz.

The SPI port supports both 3-wire (bidirectional) and 4-wire (unidirectional) hardware configurations and both MSB-first and LSB-first data formats. Both the hardware configuration and data format features are programmable. The 3-wire mode uses the SDIO (serial data input/output) pin for transferring data in both directions. The 4-wire mode uses the SDIO pin for transferring data to the AD9530, and the SDO pin for transferring data from the AD9530.

The $\overline{CS}$ (chip select) pin is an active low control that gates read and write operations. Assertion (active low) of the $\overline{CS}$ pin initiates a write or read operation to theAD9530 SPI port. Any number of data bytes can be transferred in a continuous stream. The register address is automatically incremented or decremented based on the setting of the address ascension bit (Register 0x0000). $\overline{CS}$ must be deasserted at the end of the last byte transferred, thereby ending the stream mode. This pin is internally connected to a 10 kΩ pull-up resistor. When $\overline{CS}$ is high, the SDIO and SDO pins go into a high impedance state.

Implementation Specific Details

A detailed description of the unified SPI protocol can be found at www.analog.com/ADISPI, which covers items such as timing, command format, and addressing.

The following product specific items are defined in the unified SPI protocol:

- Analog Devices unified SPI protocol Revision: 1.0.
- Chip type: 0x05 (0x05 indicates a clock chip).
- Product ID: 10011b (in this case) uniquely identifies the device as AD9530. No other Analog Devices clock IC supporting unified SPI has this identifier.
- Physical layer: 3-wire and 4-wire supported and 2.5 V operation supported.
- Optional single-byte instruction mode: not supported.
- Data link: not used.
- Control: not used.

Communication Cycle—Instruction Plus Data

The unified SPI protocol consists of a two part communication cycle. The first part is a 16-bit instruction word that is coincident with the first 16 SCLK rising edges and a payload. The instruction word provides the AD9530 serial control port with information regarding the payload. The instruction word includes the R/$\overline{W}$ bit that indicates the direction of the payload transfer (that is, a read or write operation). The instruction word also indicates the starting register address of the first payload byte.

Write

If the instruction word indicates a write operation, the payload is written into the serial control port buffer of the AD9530. Data bits are registered on the rising edge of SCLK. Generally, it does not matter what data is written to blank registers; however, it is customary to use 0s. Note that there may be reserved registers with default values not equal to 0x00; however, every effort was made to avoid this.

Most of the serial port registers are buffered (see the Buffered/Active Registers section for details on the difference between buffered and active registers). Therefore, data written into buffered registers does not take effect immediately. An additional operation is needed to transfer buffered serial control port contents to the registers that actually control the device. This transfer is accomplished with an IO_UPDATE operation, which is performed in one of two ways. One method is to write a Logic 1 to Register 0x00F, Bit 0 (this bit is an autoclearing bit). The user can change as many register bits as desired before executing an IO_UPDATE command. The IO_UPDATE operation transfers the buffer register contents to their active register counterparts.

Read

If the instruction word indicates a read operation, the next N × 8 SCLK cycles clock out the data starting from the address specified in the instruction word. N is the number of data bytes read. The readback data is driven to the pin on the falling edge and must be latched on the rising edge of SCLK. Blank registers are not skipped over during readback.

A readback operation takes data from either the serial control port buffer registers or the active registers, as determined by Register 0x001, Bit 5.

SPI Instruction Word (16 Bits)

The MSB of the 16-bit instruction word is R/$\overline{W}$, which indicates whether the instruction is a read or a write. The next 15 bits are the register address (A14 to A0), which indicates the starting register address of the read/write operation (see Table 20). Note that, because there are no registers that require more than 13 address bits, A14 and A13 are ignored and treated as zeros.

SPI MSB/LSB First Transfers

The AD9530 instruction word and payload can be MSB first or LSB first. The default for the AD9530 is MSB first. The LSB first mode can be set by writing a 1 to Register 0x000, Bit 6 and Bit 1. Immediately after the LSB first bit is set, subsequent serial control port operations are LSB first.

Address Ascension

If the address ascension bit (Register 0x000, Bit 5 and Bit 2) = 0, the serial control port register address decrements from the specified starting address toward Address 0x0000.

If the address ascension bit (Register 0x0000, Bit 5 and Bit 2) = 1, the serial control port register address increments from the starting address toward Address 0x0FF. Reserved addresses are not skipped during multibyte input/output operations; therefore, write the default value to a reserved register and 0s to unmapped registers. Note that it is more efficient to issue a new write command than to write the default value to more than two consecutive reserved (or unmapped) registers.

Table 19. Streaming Mode (No Addresses Skipped)

Address Ascension	Stop Sequence
Increment	0x0000 … 0x1FFF
Decrement	0x1FFF … 0x0000

Table 20. Serial Control Port, 16-Bit Instruction Word

MSB															LSB
I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
R/$\overline{W}$	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

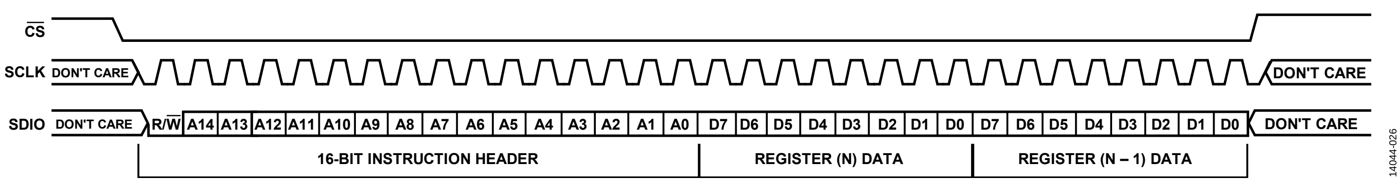


Figure 25. Serial Control Port Write—MSB First, Address Decrement, Two Bytes of Data

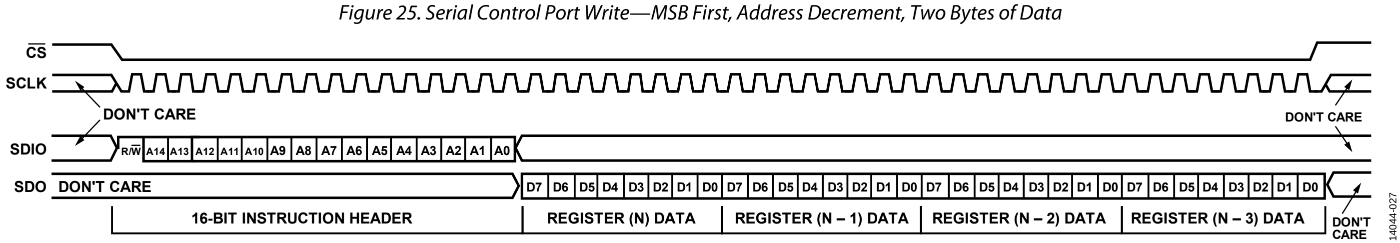


Figure 26. Serial Control Port Read—MSB First, Address Decrement, Four Bytes of Data

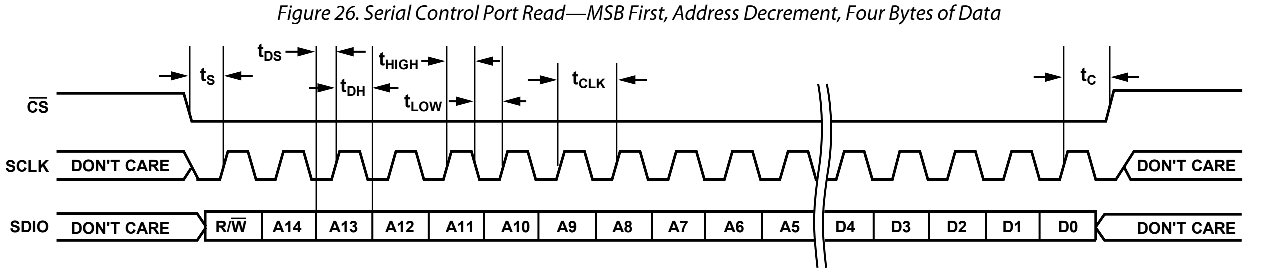


Figure 27. Timing Diagram for Serial Control Port Write—MSB First

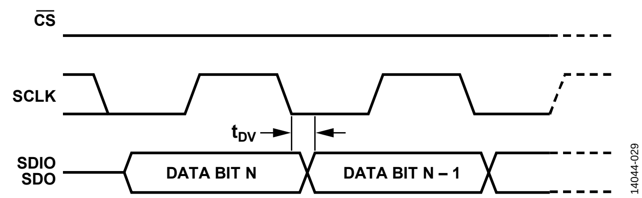


Figure 28. Timing Diagram for Serial Control Port Register Read—MSB First

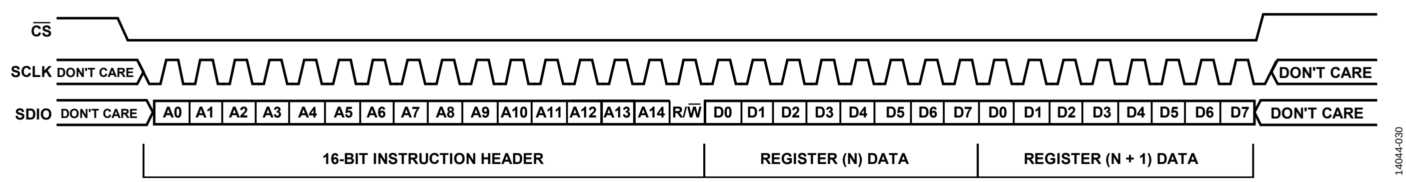


Figure 29. Serial Control Port Write—LSB First, Address Increment, Two Bytes of Data

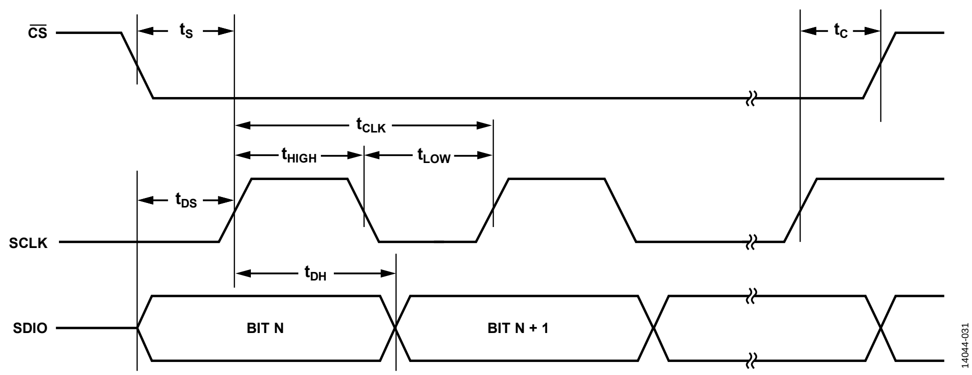


Figure 30. Serial Control Port Timing—Write

Table 21. Serial Control Port Timing

Parameter	Description
t_{DS}	Setup time between data and the rising edge of SCLK (see Figure 27 and Figure 30)
t_{DH}	Hold time between data and the rising edge of SCLK (see Figure 27 and Figure 30)
t_{CLK}	Period of the clock (see Figure 27 and Figure 30)
t_S	Setup time between the $\overline{CS}$ falling edge and the SCLK rising edge (start of the communication cycle) (see Figure 27 and Figure 30)
t_C	Setup time between the SCLK rising edge and $\overline{CS}$ rising edge (end of the communication cycle) (see Figure 27 and Figure 30)
t_{HIGH}	Minimum period that SCLK is in a logic high state (see Figure 27 and Figure 30)
t_{LOW}	Minimum period that SCLK is in a logic low state (see Figure 27 and Figure 30)
t_{DV}	SCLK to valid SDIO (see Figure 28)

POWER DISSIPATION AND THERMAL CONSIDERATIONS

The AD9530 is a multifunctional, high speed device that targets a wide variety of clock applications. The numerous innovative features contained in the device each consume incremental power. If all outputs are enabled in the maximum frequency and mode that have the highest power, the safe thermal operating conditions of the device may be exceeded. Careful analysis and consideration of power dissipation and thermal management are critical elements in the successful application of the AD9530.

The AD9530 is specified to operate within the industrial temperature range of −40°C to +85°C. This specification is conditional, such that the absolute maximum junction temperature is not exceeded (as specified in Table 14). At high operating temperatures, extreme care must be taken when operating the device to avoid exceeding the junction temperature and potentially damaging the device.

Many variables contribute to the operating junction temperature within the device, including

- Selected driver mode of operation
- Output clock speed
- Supply voltage
- Ambient temperature

The combination of these variables determines the junction temperature within the AD9530 for a given set of operating conditions.

The AD9530 is specified for an ambient temperature (T_A). To ensure that T_A is not exceeded, use an airflow source.

Use the following equation to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times PD)$$

where:
T_J is the junction temperature (°C).
T_{CASE} is the case temperature (°C) measured at the top center of the package.
Ψ_{JT} is the value from Table 14.
PD is the power dissipation of the AD9530.

Values of θ_{JA} are provided for package comparison and PCB design considerations. θ_{JA} can be used for a first-order approximation of T_J by the equation

$$T_J = T_A + (\theta_{JA} \times PD)$$

where T_A is the ambient temperature (°C).

Values of θ_{JC} are provided for package comparison and PCB design considerations when an external heat sink is required.

Values of Ψ_{JB} are provided for package comparison and PCB design considerations.

CLOCK SPEED AND DRIVER MODE

Clock speed directly and linearly influences the total power dissipation of the device and, therefore, the junction temperature. Table 3 lists the currents required by the driver for a single output frequency. If using the current vs. frequency graphs provided in the Typical Performance Characteristics section, subtract the power into the load using the following equation:

$$P_{LOAD} = (\textit{Differential Output Voltage Swing}^2/50\ \Omega)$$

EVALUATION OF OPERATING CONDITIONS

The first step in evaluating the operating conditions is to determine the AD9530 maximum power consumption for the user configuration by referring to the values in Table 2. The maximum PD excludes power dissipated in the load resistors of the drivers because such power is external to the device. Use the current dissipation specifications listed in Table 2, as well as the power dissipation numbers in Table 3 to calculate the total power dissipated for the desired configuration.

The second step in evaluating the operating conditions is to multiply the power dissipated by the thermal impedance to determine the maximum power gradient. For this example, a thermal impedance of θ_{JA} = 21.1°C/W is used.

Example 1

Example 1 is as follows:

$$(1358\text{ mW} \times 21.1°\text{C/W}) = 29°\text{C}$$

With an ambient temperature of 85°C, the junction temperature is

$$T_J = 85°\text{C} + 29°\text{C} = 114°\text{C}$$

This junction temperature is below the maximum allowable temperature.

Example 2

Example 2 is as follows:

$$(1630\text{ mW} \times 21.1°\text{C/W}) = 34°\text{C}$$

With an ambient temperature of 85°C, the junction temperature is

$$T_J = 85°\text{C} + 34°\text{C} = 119°\text{C}$$

This junction temperature is greater than the maximum allowable temperature. The ambient temperature must be lowered by 4°C to operate in the condition of Example 2.

THERMALLY ENHANCED PACKAGE MOUNTING GUIDELINES

See the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, for more information about mounting devices with an exposed pad.

APPLICATIONS INFORMATION

POWER SUPPLY RECOMMENDATIONS

The AD9530 only requires 2.5 V for operation, but proper isolation between power domains is beneficial for performance. Figure 31 shows the recommended Analog Devices power solutions for the best possible performance of the AD9530. These devices are also featured on the evaluation board.

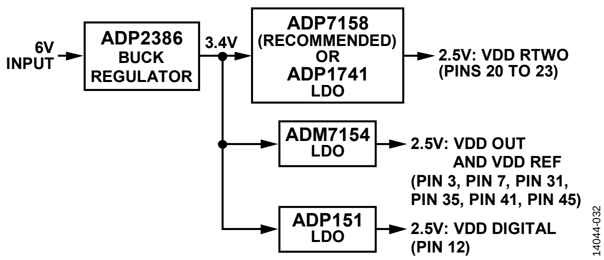


Figure 31. Power Supply Recommendation

USING THE AD9530 OUTPUTS FOR ADC CLOCK APPLICATIONS

Any high speed ADC is extremely sensitive to the quality of the sampling clock of the AD9530. An ADC can be thought of as a sampling mixer, and any noise, distortion, or time jitter on the clock is combined with the desired signal at the analog-to-digital output. Clock integrity requirements scale with the analog input frequency and resolution, with higher analog input frequency applications at ≥14-bit resolution being the most stringent. The theoretical SNR of an ADC is limited by the ADC resolution and the jitter on the sampling clock. Considering an ideal ADC of infinite resolution, where the step size and quantization error can be ignored, the available SNR can be expressed approximately by

$$SNR(\text{dB}) = 20\log\left(\frac{1}{2\pi f_A t_J}\right)$$

where:
f_A is the highest analog frequency being digitized.
t_J is the rms jitter on the sampling clock.

Figure 32 shows the required sampling clock jitter as a function of the analog frequency and effective number of bits (ENOB).

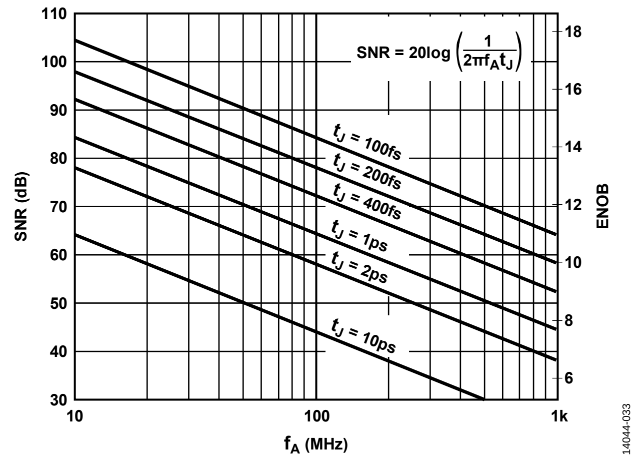


Figure 32. SNR and ENOB vs. Analog Input Frequency (f_A)

For more information, see the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, and the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance.*

Many high performance ADCs feature differential clock inputs to simplify the task of providing the required low jitter clock on a noisy PCB. Distributing a single-ended clock on a noisy PCB can result in coupled noise on the sampling clock. Differential distribution has inherent common-mode rejection that can provide superior clock performance in a noisy environment. The differential CML outputs of the AD9530 enable clock solutions that maximize converter SNR performance.

Consider the input requirements of the ADC (differential or single-ended, logic level termination) when selecting the best clocking/converter solution.

TYPICAL APPLICATION BLOCK DIAGRAM

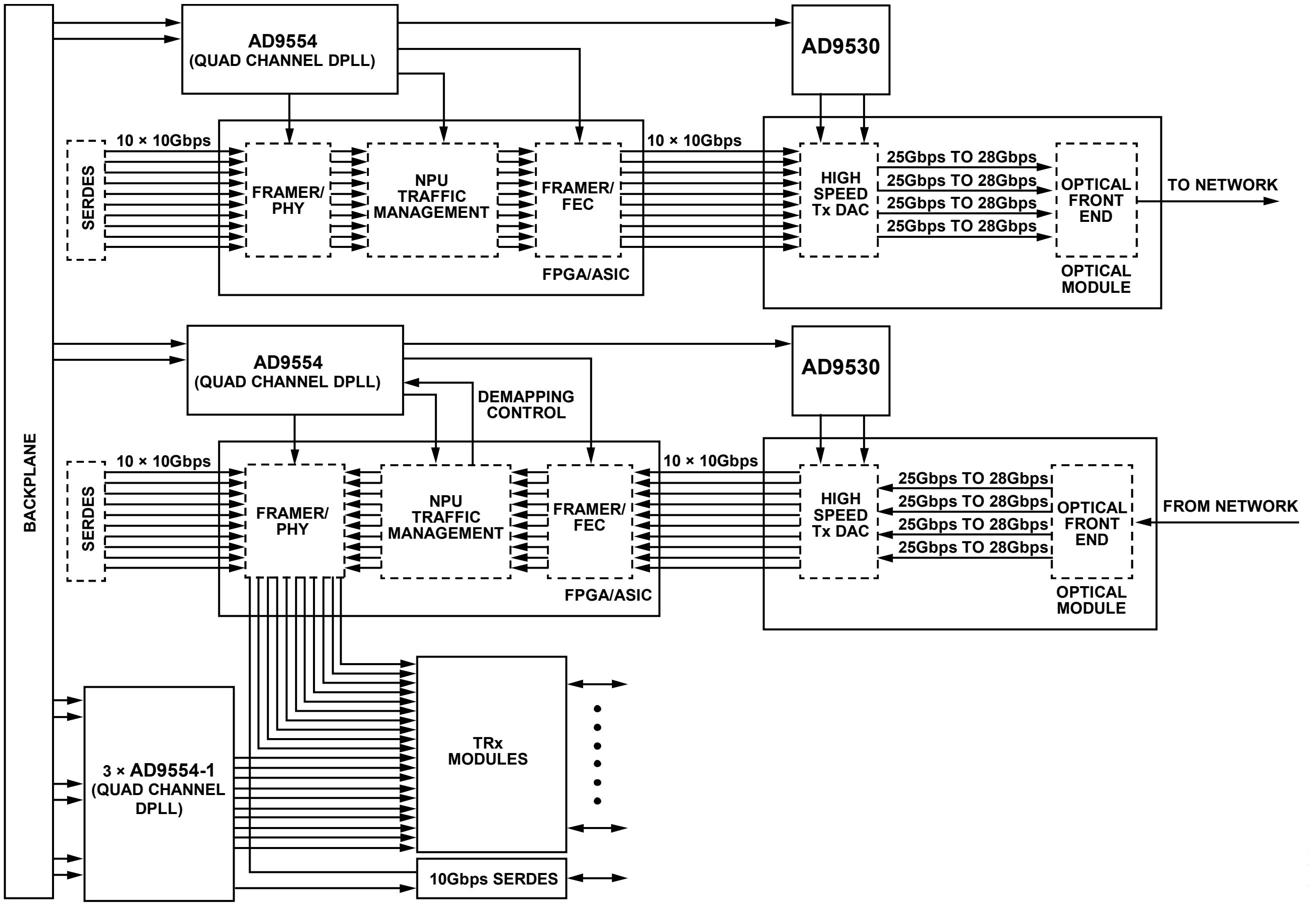


Figure 33. Typical Application Block Diagram, 100 Gbps Muxponder with the AD9530

CONTROL REGISTERS

CONTROL REGISTER MAP OVERVIEW

Register addresses that are not listed in Table 22 are not used and writing to those registers has no effect. Registers that are marked as reserved must never have their values changed.

When writing to registers with bits that are marked reserved, take care to always write the default value for the reserved bits.

Unused and reserved registers are in the control register map but are not in the control register description tables.

Table 22. Control Register Map

Reg. Addr. (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
0x000	SPI_CONFIGA	SOFT_RESET	LSB_FIRST	ADDRESS_ASCEND	SDO_ACTIVE		ADDRESS_ASCEND	LSB_FIRST	SOFT_RESET	0x00
0x001	SPI_CONFIGB	SINGLE_INSTRUCTION	RESERVED	READ_BUFFER	RESERVED		CALIBRATE VCO	DIVIDER_RESET	RESERVED	0x00
0x002	STATUS	PLL_LOCKED	SIGNAL_PRESENT	FEEDBACK_OK	REFERENCE_OK	RESERVED		SLEEP		Varies
0x003	CHIP_TYPE	RESERVED				CHIP_TYPE, Bits[3:0]				0x05
0x004	PRODUCT_ID[11:0]	PRODUCT_ID, Bits[3:0]				RESERVED				0x3F
0x005		PRODUCT_ID, Bits[11:4]								0x01
0x006	PART_VERSION	PART VERSION								0x14
0x007	RESERVED	RESERVED								0x00
0x008	RESERVED	RESERVED								0x00
0x009	RESERVED	RESERVED								0x00
0x00A	USER_SCRATCHPAD1	USER_SCRATCHPAD1, Bits[7:0]								0x00
0x00B	SPI_VERSION	SPI_VERSION, Bits[7:0]								0x00
0x00C	VENDOR_ID	VENDOR_ID, Bits[7:0]								0x56
0x00D	VENDOR_ID	VENDOR_ID, Bits[15:8]								0x04
0x00E	RESERVED	RESERVED								0x00
0x00F	IO_UPDATE	RESERVED							IO_UPDATE	0x00
0x010	R_DIVIDER	R_DIVIDER, Bits[7:0]								0x01
0x011	R_DIVIDER_CTRL	RESERVED					REFIN_OVERRIDE_PIN_SEL	REFIN_INPUT_SEL	REFIN_DIV_RESET	0x06
0x012	REF_A	RESERVED				REFA_TERM_SEL		REFA_LDO_EN	REFA_EN	0x07
0x013	REF_B	RESERVED				REFB_TERM_SEL		REFB_LDO_EN	REFB_EN	0x06
0x014	OUT1_DIVIDER	OUT1_DIVIDER, Bits[7:0]								0x01
0x015	OUT1_DRIVER_CONTROL	RESERVED		OUT1_AMP_TRIM		OUT1_TERM_EN	OUT1_LDO_EN	OUT1_EN	OUT1_DIVIDER_RESET	0x24
0x016	OUT2_DIVIDER	OUT2_DIVIDER, Bits[7:0]								0x01
0x017	OUT2_DRIVER_CONTROL	RESERVED		OUT2_AMP_TRIM		OUT2_TERM_EN	OUT2_LDO_EN	OUT2_EN	OUT2_DIVIDER_RESET	0x24
0x018	OUT3_DIVIDER	OUT3_DIVIDER, Bits[7:0]								0x01
0x019	OUT3_DRIVER_CONTROL	RESERVED		OUT3_AMP_TRIM		OUT3_TERM_EN	OUT3_LDO_EN	OUT3_EN	OUT3_DIVIDER_RESET	0x24
0x01A	OUT4_DIVIDER	OUT4_DIVIDER, Bits[7:0]								0x01
0x01B	OUT4_DRIVER_CONTROL	RESERVED		OUT4_AMP_TRIM		OUT4_TERM_EN	OUT4_LDO_EN	OUT4_EN	OUT4_DIVIDER_RESET	0x24
0x01C	VCO_POWER	RESERVED						VCO_LDO_WAIT_OVERRIDE	VCO_POWER	0x01
0x01D	PLL_LOCKDET_CONTROL	RESERVED			PLL_LOCK_DET_START	PLL_LOCK_DET_ERR_THRESHOLD, Bits[2:0]			PLL_LOCK_DET_RESET	0x0C
0x01E	PLL_LOCKDET_READBACK1	PLL_LOCK_DET_ERROR, Bits[7:0]								Varies
0x01F	PLL_LOCKDET_READBACK2	RESERVED			PLL_LOCK_DET_DONE	PLL_LOCK_DET_RANGE	PLL_LOCKED	PLL_LOCK_DET_ERROR, Bits[9:8]		Varies
0x020	M1_DIVIDER	RESERVED			M1_DIVIDER		M1_LDO_EN	M1_EN	M1_DIVIDER_RESET	0x16
0x021	M2_DIVIDER	RESERVED			M2_DIVIDER		M2_LDO_EN	M2_EN	M2_DIVIDER_RESET	0x16
0x022	M3_DIVIDER	RESERVED				M3_DIVIDER		M3_EN	M3_DIVIDER_RESET	0x02
0x023	N_DIVIDER	N_DIVIDER								0x0A

Reg. Addr. (Hex)	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	(LSB) Bit 0	Default Value (Hex)
0x024	N_DIVIDER_ CTRL	RESERVED							N_DIVIDER_ RESET	0x00
0x025	CHARGE_PUMP	RESERVED		CP_CURRENT						0x07
0x026	PHASE_ FREQUENCY_ DETECTOR	RESERVED						PFD_EN_ ANTIBACKLASH	PFD_ENABLE	0x01
0x027	LOOP_FILTER	RESERVED		LOOP_FILTER_CAP				LOOP_FILTER_ BIAS_EN	LOOP_FILTER_ AMP_EN	0x13
0x028	VCO_READBACK	RESERVED			VCO_FREQ_AUTOCAL					0x00
0x0FC	RESERVED	RESERVED								0x00
0x0FD	RESERVED	RESERVED								0x00
0x0FE	USER_ SCRATCHPAD2	USER_SCRATCHPAD2, Bits[7:0]								0x00
0x0FF	USER_ SCRATCHPAD3	USER_SCRATCHPAD3, Bits[7:0]								0x00

CONTROL REGISTER MAP DESCRIPTIONS

Table 23 through Table 61 provide detailed descriptions for each of the control register functions. The registers are listed by hexadecimal address. Bit fields noted as live indicate that the register write takes effect immediately. Bit fields that are not noted as live only take effect after an IO_UPDATE is issued by writing 0x01 to Register 0x00F.

SPI CONFIGURATION (REGISTER 0x000 AND REGISTER 0x001)

Table 23. Bit Descriptions for SPI_CONFIGA (Default: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
7	SOFT_RESET		Master SPI reset. Setting this self clearing bit to 1 resets the AD9530. This bit is live.	0b	W
6	LSB_FIRST		Selects SPI LSB first mode. This bit is live.	0b	RW
		0	MSB first SPI access.		
		1	LSB first SPI access.		
5	ADDRESS_ASCEND		Selects SPI address ascend mode. This bit is live.	0b	RW
		0	SPI streaming mode addresses decrement (default).		
		1	SPI streaming mode addresses increment.		
[4:3]	SDO_ACTIVE		Selects SPI 4-pin mode, which enables the SDO pin. This bit is live.	0b	RW
		0	SPI 3-pin mode. The SDIO pin is bidirectional (default).		
		1	SPI 4-pin mode. The SDI and SDO pins are unidirectional.		
2	ADDRESS_ASCEND		Selects SPI address ascend mode. This bit is live.	0b	RW
		0	SPI streaming mode addresses decrement (default).		
		1	SPI streaming mode addresses increment.		
1	LSB_FIRST		Selects SPI LSB first mode. This bit is live.	0b	RW
		0	MSB first SPI access (default).		
		1	LSB first SPI access.		
0	SOFT_RESET		Master SPI reset. Setting this self clearing bit to 1 resets the AD9530. This bit is live.	0b	W

Table 24. Bit Descriptions for SPI_CONFIGB (Default: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
7	SINGLE_INSTRUCTION		Single instruction mode. This bit is live.	0b	RW
		0	SPI streaming mode (default).		
		1	SPI single instruction mode.		
6	RESERVED	0	When writing to Register 0x001, this bit must be 0b.	0b	W
5	READ_BUFFER		For buffered registers, this bit controls whether the value read from the serial port is from the actual (active) registers or the buffered copy.	0b	RW
		0	Reads values currently applied to the internal logic of the device (default).		
		1	Reads buffered values that take effect on the next assertion of IO_UPDATE.		
[4:3]	RESERVED	00	When writing to Register 0x001, these bits must be 00b.	00b	W
2	CALIBRATE VCO		VCO calibration. Setting this self clearing bit performs a VCO calibration, which must be performed at startup as well as any time the VCO frequency is changed. A VCO calibration also automatically performs a divider reset (Bit 1 in this register). This bit is live.	0b	W
1	DIVIDER_RESET		Divider reset. Writing a 1 to this self clearing register stalls the outputs, reset all dividers, and reenable the outputs. A divider reset must be performed any time the divider values are changed. Note that if the divider value change results in a different VCO frequency, the CALIBRATE VCO bit (Bit 2 in this register) must be used instead. This bit is live.	0b	W
0	RESERVED	0	When writing to Register 0x001, this bit must be 0b.	0	W

STATUS (REGISTER 0x002)

Table 25. Bit Descriptions for STATUS (Default: Varies[1])

Bits	Bit Name	Settings	Description	Reset	Access
7	PLL_LOCKED		PLL lock detect status readback	Varies	R
		0	PLL unlocked		
		1	PLL locked		
6	SIGNAL_PRESENT		Reference signal present	Varies	R
		0	Reference input signal not detected		
		1	Reference input signal detected		
5	FEEDBACK_OK		Feedback signal valid from N divider	Varies	R
		0	Feedback signal from N divider not detected		
		1	Feedback signal from N divider detected		
4	REFERENCE_OK		Logical AND of reference input signal and feedback signal	Varies	R
		0	Either the reference input clock is not detected or the feedback signal is not detected, or neither are detected		
		1	Reference input signal and feedback signal both detected		
[3:2]	RESERVED	00	When writing to Register 0x002, these bits must be 00b	00b	W
[1:0]	SLEEP		Sleep mode	00b	RW
		00	Normal operation (default)		
		01	Undefined		
		10	Undefined		
		11	Sleep mode		

[1] The default value reads 0xF0 under normal operation if the PLL is locked.

CHIP TYPE (REGISTER 0x003)

Table 26. Bit Descriptions for CHIP_TYPE (Default: 0x05)

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
[3:0]	CHIP_TYPE, Bits[3:0]		The Analog Devices unified SPI protocol reserves this read only register location for identifying the type of device. The default value of 0x05 identifies the AD9530 as a clock IC.	0x5	R

PRODUCT ID (REGISTER 0x004 AND REGISTER 0x005)

Table 27. Bit Descriptions for PRODUCT_ID[3:0] (Default: 0x3F)

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	PRODUCT_ID, Bits[3:0]		The Analog Devices unified SPI protocol reserves this read only register location as the lower four bits of the clock part serial ID that (along with Register 0x005) uniquely identifies the AD9530 within the Analog Devices clock chip family. No other Analog Devices chip that adheres to the Analog Devices unified SPI has these values for Register 0x003, Register 0x004, and Register 0x005.	0x3	R
[3:0]	RESERVED		Reserved.	0xF	R

Table 28. Bit Descriptions for PRODUCT_ID[11:4] (Default: 0x01)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PRODUCT_ID, Bits[11:4]		The Analog Devices unified SPI protocol reserves this read only register location as the upper eight bits of the clock part serial ID that (along with Register 0x004) uniquely identifies the AD9530 within the Analog Devices clock chip family. No other Analog Devices chip that adheres to the Analog Devices unified SPI has these values for Register 0x003, Register 0x004, and Register 0x005.	0x01	R

PART VERSION (REGISTER 0x006)

Table 29. Bit Descriptions for PART_VERSION (Default: 0x14)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PART VERSION		The Analog Devices unified SPI protocol reserves this read only register location for identifying the die revision.	0x00	R

USER SCRATCH PAD 1 (REGISTER 0x00A)

Table 30. Bit Descriptions for USER_SCRATCHPAD1 (Default: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	USER_SCRATCHPAD1, Bits[7:0]	0x00 to 0xFF	This register has no effect on device operation. It is available for serial port debugging or register setting revision control. There are two additional user scratch pad registers at Address 0x0FE and Address 0x0FF.	0x00	RW

SPI VERSION (REGISTER 0x00B)

Table 31. Bit Descriptions for SPI_VERSION (Default: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	SPI_VERSION, Bits[7:0]		The Analog Devices unified SPI protocol reserves this read only register location for identifying the version of the unified SPI protocol.	0x00	R

VENDOR ID (REGISTER 0x00C AND REGISTER 0x00D)

Table 32. Bit Descriptions for VENDOR ID (Default: 0x56)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID, Bits[7:0]		The Analog Devices unified SPI protocol reserves this read only register location for identifying Analog Devices as the chip vendor of this device. All Analog Devices parts adhering to the unified serial port specification have the same value in this register.	0x56	R

Table 33. Bit Descriptions for VENDOR_ID (Default: 0x04)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR_ID, Bits[15:8]		The Analog Devices unified SPI protocol reserves this read only register location for identifying Analog Devices as the chip vendor of this part. All Analog Devices parts adhering to the unified serial port specification have the same value in this register.	0x04	R

IO_UPDATE (REGISTER 0x00F)

Table 34. Bit Descriptions for IO_UPDATE (Default: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED	0x00	When writing to Register 0x00F, these bits must be 0x0.	0x00	W
0	IO_UPDATE		Writing a 1 to this bit transfers the data in the serial input/output buffer registers to the internal control registers of the device. This is a live and autoclearing bit.	0b	W

R DIVIDER—REFERENCE INPUT DIVIDER (REGISTER 0x010)

Table 35. Bit Descriptions for R_DIVIDER (Default: 0x01)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	R_DIVIDER, Bits[7:0]	0x01 to 0xFF	PLL reference divider. These bits control the divide ratio of the R divider. Divide ratio goes from ÷1 (by writing 0x01) to ÷255 (by writing 0xFF).	0x01	RW

R DIVIDER CONTROL (REGISTER 0x011)

Table 36. Bit Descriptions for R_DIVIDER_CTRL (Default: 0x06)

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	RESERVED	00000b	When writing to Register 0x011, these bits must be 00000b.	00000b	RW
2	REFIN_OVERRIDE_PIN_SEL		Reference input override pin selection.	1b	RW
		0	REFIN_INPUT_SEL bit (in this register) controls reference input selection.		
		1	REF_SEL pin controls reference input selection. REFA is selected if the REF_SEL pin is high. REFB is selected if the REF_SEL pin is low.		
1	REFIN_INPUT_SEL		Reference input selection.	1b	RW
		0	Select REFB input if REFIN_OVERRIDE_PIN_SEL = 0.		
		1	Select REFA input if REFIN_OVERRIDE_PIN_SEL = 0.		
0	REFIN_DIV_RESET		Reference input divider reset (autoclearing). Setting this (self clearing) bit resets the R divider. This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

REFERENCE INPUT A (REGISTER 0x012)

Table 37. Bit Descriptions for REF_A (Default: 0x07)

Bits	Bit Name	Settings	Description	Default	Access
[7:4]	RESERVED	00	When writing to Register 0x012, these bits must be 0x0	0x0	W
[3:2]	REFA_TERM_SEL		Reference A input termination select	01b	RW
		00	LVDS mode (100 Ω across the inputs)		
		01	DC-coupled mode (50 Ω to ground) (default)		
		10	AC-coupled mode (50 Ω to 0.35 V, internal)		
		11	DC-coupled high-Z mode		
1	REFA_LDO_EN		Reference A enable LDO	1b	RW
		0	Disabled		
		1	Enabled (default)		
0	REFA_EN		Reference A enable	1b	RW
		0	Disabled		
		1	Enabled (default)		

REFERENCE INPUT B (REGISTER 0x013)

Table 38. Bit Descriptions for REF_B (Default: 0x06)

Bits	Bit Name	Settings	Description	Default	Access
[7:4]	RESERVED	00	When writing to Register 0x013, these bits must be 0x0	0x0	W
[3:2]	REFB_TERM_SEL		Reference B input termination select	01b	RW
		00	LVDS mode (100 Ω across the inputs)		
		01	DC-coupled mode (50 Ω to ground) (default)		
		10	AC-coupled mode (50 Ω to 0.35 V, internal)		
		11	DC-coupled high-Z mode		
1	REFB_LDO_EN		Reference B enable LDO	1b	RW
		0	Disabled		
		1	Enabled (default)		
0	REFB_EN		Reference B enable	0b	RW
		0	Disabled (default)		
		1	Enabled		

OUT1 DIVIDER (REGISTER 0x014)

Table 39. Bit Descriptions for OUT1_DIVIDER (Default: 0x01)

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	OUT1_DIVIDER, Bits[7:0]	0x00 to 0xFF	Output 1 divider. These bits control the divide ratio of the output divider. Divide ratio goes from ÷1 (by writing 0x01) to ÷255 (by writing 0xFF). Writing 0x00 disables the divider.	0x01	RW

OUT1 DRIVER CONTROL REGISTER (REGISTER 0x015)

Table 40. Bit Descriptions for OUT1_DRIVER_CONTROL (Default: 0x24)

Bits	Bit Name	Settings	Description	Default	Access
[7:6]	RESERVED	00	When writing to Register 0x015, these bits must be 00b.	00b	W
[5:4]	OUT1_AMP_TRIM		Output 1 amplitude voltage trim.	10b	RW
		00	0.8 V.		
		01	0.9 V.		
		10	1.0 V (default).		
		11	1.1 V.		
3	OUT1_TERM_EN		Output 1 on-chip termination.	0b	RW
		0	Disabled (default).		
		1	Enabled.		
2	OUT1_LDO_EN		Output 1 enable LDO.	1b	RW
		0	Disabled.		
		1	Enabled (default).		
1	OUT1_EN		Output 1 enable.	0b	RW
		0	Disabled (default).		
		1	Enabled.		
0	OUT1_DIVIDER_RESET		Setting this (self clearing) bit resets the Output 1 divider. This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

OUT2 DIVIDER (REGISTER 0x016)

Table 41. Bit Descriptions for OUT2_DIVIDER (Default: 0x01)

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	OUT2_DIVIDER, Bits[7:0]	0x00 to 0xFF	Output 2 divider. These bits control the divide ratio of the output divider. Divide ratio goes from ÷1 (by writing 0x01) to ÷255 (by writing 0xFF). Writing 0x00 disables the divider.	0x01	RW

OUT2 DRIVER CONTROL (REGISTER 0x017)

Table 42. Bit Descriptions for OUT2_DRIVER_CONTROL (Default: 0x24)

Bits	Bit Name	Settings	Description	Default	Access
[7:6]	RESERVED	00	When writing to Register 0x017, these bits must be 00b.	00	W
[5:4]	OUT2_AMP_TRIM		Output 2 amplitude voltage trim.	10b	RW
		00	0.8 V.		
		01	0.9 V.		
		10	1.0 V (default).		
		11	1.1 V.		
3	OUT2_TERM_EN		Output 2 on-chip termination.	0b	RW
		0	Disabled (default).		
		1	Enabled.		
2	OUT2_LDO_EN		Output 2 enable LDO.	1b	RW
		0	Disabled.		
		1	Enabled (default).		
1	OUT2_EN		Output 2 enable.	0b	RW
		0	Disabled (default).		
		1	Enabled.		

Bits	Bit Name	Settings	Description	Default	Access
0	OUT2_DIVIDER_RESET		Setting this (self clearing) bit resets the Output 2 divider. This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

OUT3 DIVIDER (REGISTER 0x018)

Table 43. Bit Descriptions for OUT3_DIVIDER (Default: 0x01)

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	OUT3_DIVIDER, Bits[7:0]	0x00 to 0xFF	Output 3 divider. These bits control the divide ratio of the output divider. Divide ratio goes from ÷1 (by writing 0x01) to ÷255 by writing 0xFF. Writing 0x00 disables the divider.	0x01	RW

OUT3 DRIVER CONTROL (REGISTER 0x019)

Table 44. Bit Descriptions for OUT3_DRIVER_CONTROL (Default: 0x24)

Bits	Bit Name	Settings	Description	Default	Access
[7:6]	RESERVED		When writing to Register 0x019, these bits must be 00b.	00b	N/A
[5:4]	OUT3_AMP_TRIM		Output 3 amplitude voltage trim.	10b	RW
		00	0.8 V.		
		01	0.9 V.		
		10	1.0 V (default).		
		11	1.1 V.		
3	OUT3_TERM_EN		Output 3 on-chip termination.	0b	RW
		0	Disabled (default).		
		1	Enabled.		
2	OUT3_LDO_EN		Output 3 enable LDO.	1b	RW
		0	Disabled.		
		1	Enabled (default).		
1	OUT3_EN		Output 3 enable.	0b	RW
		0	Disabled (default).		
		1	Enabled.		
0	OUT3_DIVIDER_RESET		Setting this (self clearing) bit resets the Output 3 divider. This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

OUT4 DIVIDER (REGISTER 0x01A)

Table 45. Bit Descriptions for OUT4_DIVIDER (Default: 0x01)

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	OUT4_DIVIDER, Bits[7:0]	0x00 to 0xFF	Output 4 divider. These bits control the divide ratio of the output divider. Divide ratio goes from ÷1 (by writing 0x01) to ÷255 by writing 0xFF. Writing 0x00 disables the divider.	0x01	RW

OUT4 DRIVER CONTROL (REGISTER 0x01B)

Table 46. Bit Descriptions for OUT4_DRIVER_CONTROL (Default: 0x24)

Bits	Bit Name	Settings	Description	Default	Access
[7:6]	RESERVED	00	When writing to Register 0x01B, these bits must be 00b.	00b	W
[5:4]	OUT4_AMP_TRIM		Output 4 amplitude voltage trim.	10b	RW
		00	0.8 V.		
		01	0.9 V.		
		10	1.0 V (default).		
		11	1.1 V.		
3	OUT4_TERM_EN		Output 4 on-chip termination.	0b	RW
		0	Disabled (default).		
		1	Enabled.		

Bits	Bit Name	Settings	Description	Default	Access
2	OUT4_LDO_EN		Output 4 enable LDO.	1b	RW
		0	Disabled.		
		1	Enabled (default).		
1	OUT4_EN		Output 4 enable.	0b	RW
		0	Disabled (default).		
		1	Enabled.		
0	OUT4_DIVIDER_RESET		Setting this (self clearing) bit resets the Output 4 divider. This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

VCO POWER (REGISTER 0x01C)

Table 47. Bit Descriptions for VCO_POWER (Default: 0x01)

Bits	Bit Name	Settings	Description	Default	Access
[7:2]	RESERVED	000000b	When writing to Register 0x01C, these bits must be 00b	000000b	W
1	VCO_LDO_WAIT_OVERRIDE		VCO LDO wait state override	0b	RW
		0	Wait 2 sec on startup for VCO LDO stability (default)		
		1	Do not wait for VCO LDO stability		
0	VCO_POWER		VCO power mode	1b	RW
		0	Low power mode		
		1	High power mode (lower jitter) (default)		

PLL LOCK DETECT CONTROL (REGISTER 0x01D)

Table 48. Bit Descriptions for PLL_LOCKDET_CONTROL (Default: 0x0C)

Bits	Bit Name	Settings	Description	Default	Access
[7:5]	RESERVED	000b	When writing to Register 0x01D, these bits must be 000b.	000b	W
4	PLL_LOCK_DET_START		PLL lock detect start measurement. This live bit enables the lock detector.	0b	RW
		0	PLL lock detector disabled (default).		
		1	PLL lock detector enabled.		
[3:1]	PLL_LOCK_DET_ERR_ THRESHOLD, Bits[2:0]	000b to 111b	PLL lock detect frequency error threshold (ppb is parts per billion and ppm is parts per million).The frequency accuracy of the lock detector is ±25% of the lock detect setting. For example, for the 15 ppb setting, the actual accuracy of the lock detector is 11 ppb to 19 ppb.	010b	RW
		000b	Threshold: ±15 ppb. Update interval: 670 ms.		
		001b	Threshold: ±60 ppb. Update interval: 170 ms.		
		010b	Threshold: ±238 ppb. Update interval: 42 ms (default).		
		011b	Threshold: ±954 ppb. Update interval: 10 ms.		
		100b	Threshold: ±3.8 ppm. Update interval: 2.6 ms.		
		101b	Threshold: ±15 ppm. Update interval: 660 μs.		
		110b	Threshold: ±61 ppm. Update interval: 160 μs.		
		111b	Threshold: ±244 ppm. Update interval: 41 μs.		
0	PLL_LOCK_DET_RESET		PLL lock detect disable.	0b	RW
		0	PLL lock detector enabled (default).		
		1	PLL lock detector disabled.		

PLL LOCK DETECT READBACK (REGISTER 0x01E AND REGISTER 0x01F)

Table 49. Bit Descriptions for PLL_LOCKDET_READBACK1 (Read Only; No Default Value)

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	PLL_LOCK_DET_ERROR, Bits[7:0]		PLL lock detect error, Bits[7:0]. This read only register, along with Bits[1:0] of Register 0x01F, form a 10-bit number that allows the user to read back the magnitude of the frequency error at the phase frequency detector. Bit 3 in Register 0x01F indicates whether the phase error measurement is in parts per million (ppm) or parts per billion (ppb).	Varies	R

Table 50. Bit Descriptions for PLL_LOCKDET_READBACK2 (Read Only; No Default Value)

Bits	Bit Name	Settings	Description	Default	Access
[7:5]	RESERVED	000b	When writing to Register 0x01F, these bits must be 000b.	000b	R
4	PLL_LOCK_DET_DONE		PLL lock detect measurement done.	Varies	R
3	PLL_LOCK_DET_RANGE		PLL lock detect error range.	Varies	R
		0	The read back error is expressed in ppb (parts per billion).		
		1	The read back error is expressed in ppm (parts per million).		
2	PLL_LOCKED		PLL lock detect status readback.	Varies	R
		0	PLL unlocked.		
		1	PLL locked.		
[1:0]	PLL_LOCK_DET_ERROR, Bits[9:8]		PLL lock detect error, Bits[9:8]. These read only register bits, along with Bits[7:0] Register 0x01E, form a 10-bit number that allows the user to read back the magnitude of the frequency error at the phase frequency detector. Bit 3 in Register 0x01F indicates whether the phase error measurement is in parts per million (ppm) or parts per billion (ppb).	Varies	R

M1, M2, M3 DIVIDERS (REGISTER 0x020 AND REGISTER 0x022)

Table 51. Bit Descriptions for M1_DIVIDER (Default 0x16)

Bits	Bit Name	Settings	Description	Default	Access
[7:5]	RESERVED	000b	When writing to Register 0x020, these bits must be 000b.	000b	W
[4:3]	M1_DIVIDER		These bits control the divide ratio for the M1 divider that feeds the D1 and D2 dividers.	10b	RW
		00	Divide by 2.		
		01	Divide by 2.5.		
		10	Divide by 3 (default).		
		11	Divide by 3.5.		
2	M1_LDO_EN		M1 divider enable LDO.	1b	RW
		0	Disabled.		
		1	Enabled (default).		
1	M1_EN		M1 divider enable.	1b	RW
		0	Disabled.		
		1	Enabled (default).		
0	M1_DIVIDER_RESET		Setting this (self clearing) bit resets the M1 divider. This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

Table 52. Bit Descriptions for M2_DIVIDER (Default: 0x16)

Bits	Bit Name	Settings	Description	Default	Access
[7:5]	RESERVED	000b	When writing to Register 0x021, these bits must be 000b.	000b	W
[4:3]	M2_DIVIDER		These bits control the divide ratio for the M2 divider that feeds the D3 and D4 dividers.	10b	RW
		00	Divide by 2.		
		01	Divide by 2.5.		
		10	Divide by 3 (default).		
		11	Divide by 3.5		
2	M2_LDO_EN		M2 divider enable LDO.	1b	RW
		0	Disabled.		
		1	Enabled (default).		
1	M2_EN		M2 divider enable.	1b	RW
		0	Disabled.		
		1	Enabled.		
0	M2_DIVIDER_RESET		Setting this (self clearing) bit resets the M2 divider. This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

M3 DIVIDER (REGISTER 0x022)

Table 53. Bit Descriptions for M3_DIVIDER (Default: 0x02)

Bits	Bit Name	Settings	Description	Default	Access
[7:4]	RESERVED	0x0	When writing to Register 0x01F, these bits must be 0x0.	0x0	W
[3:2]	M3_DIVIDER		These bits control the divide ratio for the M3 divider.	00b	RW
		00	Divide by 2 (default).		
		01	Divide by 2.5.		
		10	Divide by 3.		
		11	Divide by 3.5.		
1	M3_EN		M3 divider enable.	1b	RW
		0	Disabled.		
		1	Enabled (default).		
0	M3_DIVIDER_RESET		Setting this (self clearing) bit resets the M3 divider. This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

N DIVIDER (REGISTER 0x023)

Table 54. Bit Descriptions for N_DIVIDER (Default: 0x0A)

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	N_DIVIDER	0x01 to 0xFF	PLL feedback divider. These bits control the divide ratio of the PLL feedback divider. The divide ratio ranges from ÷1 (by writing 0x01) to ÷255 by writing 0xFF. Writing 0x00 disables the divider.	0x0A	RW

N DIVIDER CONTROL (REGISTER 0x024)

Table 55. Bit Descriptions for N_DIVIDER_CTRL (Default:0x00)

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	RESERVED	0000000b	When writing to Register 0x024, these bits must be 0x00.	0000000b	W
0	N_DIVIDER_RESET		Setting this (self clearing) bit resets the N divider (also called the feedback divider). This bit is live, meaning IO_UPDATE is not needed for it to take effect.	0b	W

CHARGE PUMP (REGISTER 0x025)

Table 56. Bit Descriptions for CHARGE_PUMP (Default: 0x07)

Bits	Bit Name	Settings	Description	Default	Access
[7:6]	RESERVED	00b	When writing to Register 0x025, these bits must be 0x0.	00b	W
[5:0]	CP_CURRENT		Charge pump current. Charge pump current, I_{CP}, is equal to: (1 + CP_CURRENT) × 50 μA. The allowable range is 50 μA to 2.6 mA. Higher register settings result in I_{CP} = 2.6 mA.	0x07	RW
		000000b	50 μA.		
		000001b	100 μA.		
		…			
		000111b	400 μA (default).		
		…			
		110010b	2.55 mA.		
		110011	2.6 mA (maximum).		

PHASE FREQUENCY DECTECTOR (REGISTER 0x026)

Table 57. Bit Descriptions for PHASE_FREQUENCY_DETECTOR (Default: 0x01)

Bits	Bit Name	Settings	Description	Default	Access
[7:2]	RESERVED	000000b	When writing to Register 0x026, these bits must be 0x00.	000000b	W
1	PFD_EN_ANTIBACKLASH		PFD antibacklash enable.	0b	RW
		0	Normal antibacklash pulse width (default).		
		1	Elongated antibacklash pulse width.		

Bits	Bit Name	Settings	Description	Default	Access
0	PFD_ENABLE		PFD enable. This bit enables the phase frequency detector.	1b	RW
		0	Disabled.		
		1	Enabled (default).		

LOOP FILTER (REGISTER 0x027)

Table 58. Bit Descriptions for LOOP_FILTER (Default: 0x13)

Bits	Bit Name	Settings	Description	Default	Access
[7:6]	RESERVED	00b	When writing to Register 0x027, these bits must be 00b	00b	W
[5:2]	LOOP_FILTER_CAP		Loop filter capacitance select (C_{IN} in Figure 16)	0x4	RW
		0000	5 pF		
		0001	17.5 pF		
		0010	30 pF		
		0011	42.5 pF		
		0100	55 pF (default)		
		0101	67.5 pF		
		0110	80 pF		
		0111	92.5 pF		
		1000	105 pF		
		1001	117.5 pF		
		1010	130 pF		
		1011	142.5 pF		
		1100	155 pF		
		1101	167.5 pF		
		1110	180 pF		
		1111	192.5 pF		
1	LOOP_FILTER_BIAS_EN		Loop filter enable bias	1b	RW
		0	Disabled		
		1	Enabled (default)		
0	LOOP_FILTER_AMP_EN		Loop filter enable amplifier	1b	RW
		0	Disabled		
		1	Enabled (default)		

VCO FREQUENCY (REGISTER 0x028)

Table 59. Bit Descriptions for VCO_READBACK (Default: 0x00)

Bits	Bit Name	Settings	Description	Default	Access
[7:5]	RESERVED		Reserved	000b	R
[4:0]	VCO_FREQ_AUTOCAL		Read only VCO autocalibrated frequency band. This is a diagnostic bit and the user normally does not need to access this register.	Varies	R

USER SCRATCH PAD 2 (REGISTER 0x0FE)

Table 60. Bit Descriptions for USER_SCRATCHPAD2 (Default: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	USER_SCRATCHPAD2, Bits[7:0]	0x00 to 0xFF	This register has no effect on device operation. It is available for serial port debugging or register setting revision control. There are two additional user scratch pad registers at Address 0x00A and Address 0x0FF.	0x00	RW

USER SCRATCH PAD 3 (REGISTER 0x0FF)

Table 61. Bit Descriptions for USER_SCRATCHPAD3 (Default: 0x00)

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	USER_SCRATCHPAD3, Bits[7:0]	0x00 to 0xFF	This register has no effect on device operation. It is available for serial port debugging or register setting revision control. There are two additional user scratch pad registers at Address 0x00A and Address 0x0FE.	0x00	RW

OUTLINE DIMENSIONS

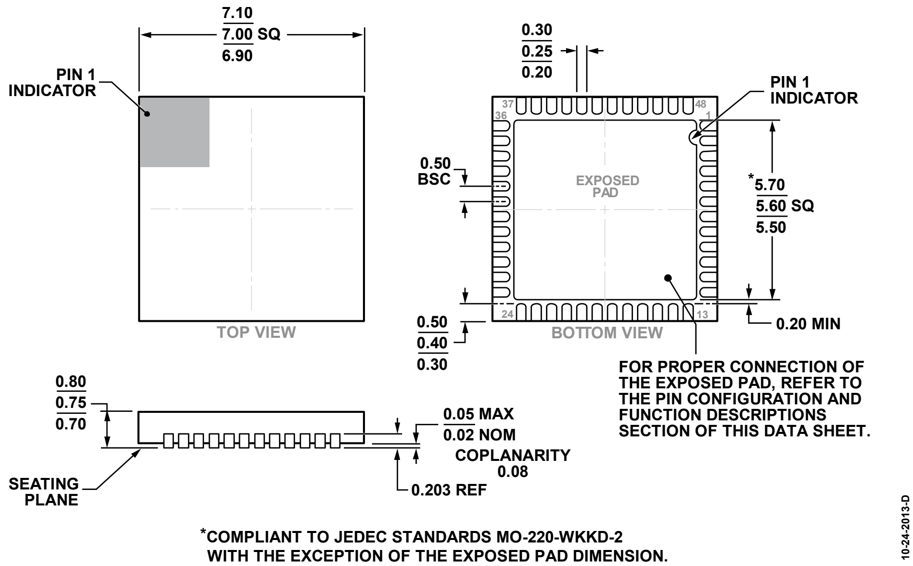


Figure 34. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9530BCPZ	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-13
AD9530BCPZ-REEL7	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	CP-48-13
AD9530/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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D14044-0-4/16(0)

LifeElectronics
Живое партнерство

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