MCP79410/MCP79411/MCP79412

Battery-Backed I²C™ Real-Time Clock/Calendar with EEPROM and Unique ID

Device Selection Table

Part Number	Unique ID
MCP79410	Unprogrammed
MCP79411	EUI-48™
MCP79412	EUI-64™

Timekeeping Features:

- Real-Time Clock/Calendar (RTCC):
  - Hours, Minutes, Seconds, Day of Week, Day, Month, Year
  - Leap year compensated to 2099
  - 12/24 hour modes
- Oscillator for 32,768 kHz Crystals:
  - Optimized for 6-9 pF crystals
- On-Chip Digital Trimming/Calibration:
  - 1 PPM resolution
  - +/- 129 PPM
- Dual Programmable Alarms
- Multifunction Output Pin:
  - Clock out with selectable frequency
  - Alarm output
  - Programmable operation
- Power-Fail Time-Stamp:
  - Time logged on Power-up/down

Low-Power Features:

- Wide Operating Voltage:
  - V_{CC}: 1.8V to 5.5V
  - V_{BAT}: 1.3V to 5.5V
- Low Typical Operating Current:
  - V_{CC} Standby: 5 µA
  - V_{BAT} Standby: 700 nA
- Automatic Battery Switchover

User Memory:

- 64-byte Battery-Backed SRAM
- 1 Kbit EEPROM Memory:
  - Software write-protect
  - Page write up to 8 bytes
  - Endurance: 1M Erase/Write cycles
- 64-bit Protected EEPROM Memory Area:
  - Robust write unlock sequence
  - EUI-48™ MAC address
  - EUI-64™ MAC address
  - Custom specified

Operating Ranges:

- 2-Wire Serial Interface, I²C™ Compatible
  - I²C Clock Rate up to 400 kHz
- Temperature Range:
  - Industrial (I): -40°C to +85°C

Packages:

- 8-Lead SOIC, MSOP, TSSOP and 2x3 TDFN

General Description:

The MCP7941X Real-Time Clock/Calendar (RTCC) tracks time using internal counters for hours, minutes, seconds, days, months, years and day of week. Alarms can be configured on all counters up to and including months. For usage and configuration, the MCP7941X supports I²C communications up to 400 kHz.

The open collector, multifunctional output can be configured to assert on an alarm match, on modification of an internal register or to output a selectable frequency square wave.

The MCP7941X is designed to operate using a 32,768 kHz tuning fork crystal with external crystal load capacitors. On-chip digital trimming can be used to adjust for frequency variance caused by crystal tolerance and temperature.

SRAM and timekeeping circuitry are powered from the back-up supply allowing the device to maintain accurate time and the SRAM contents when the main supply is unavailable. The time when the device switches over to the back-up supply and returns to main power is logged by the power-fail time-stamp.

The MCP7941X features 1 Kbit of internal nonvolatile EEPROM with software write-protectable regions. There is an additional 64 bits of nonvolatile memory, referred to as the unique ID space, which is only writable after an unlock sequence. The MCP7941X device is available with the unique ID space pre-programmed with EUI-48 or EUI-64 unique MAC ID's or unprogrammed.

Package Types

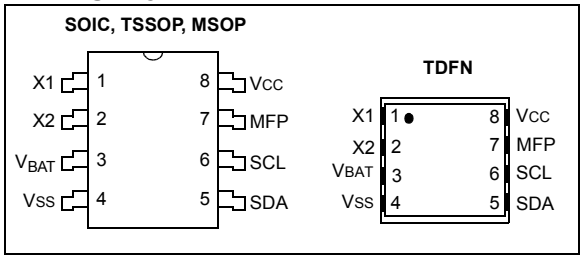


FIGURE 1-1: SCHEMATIC

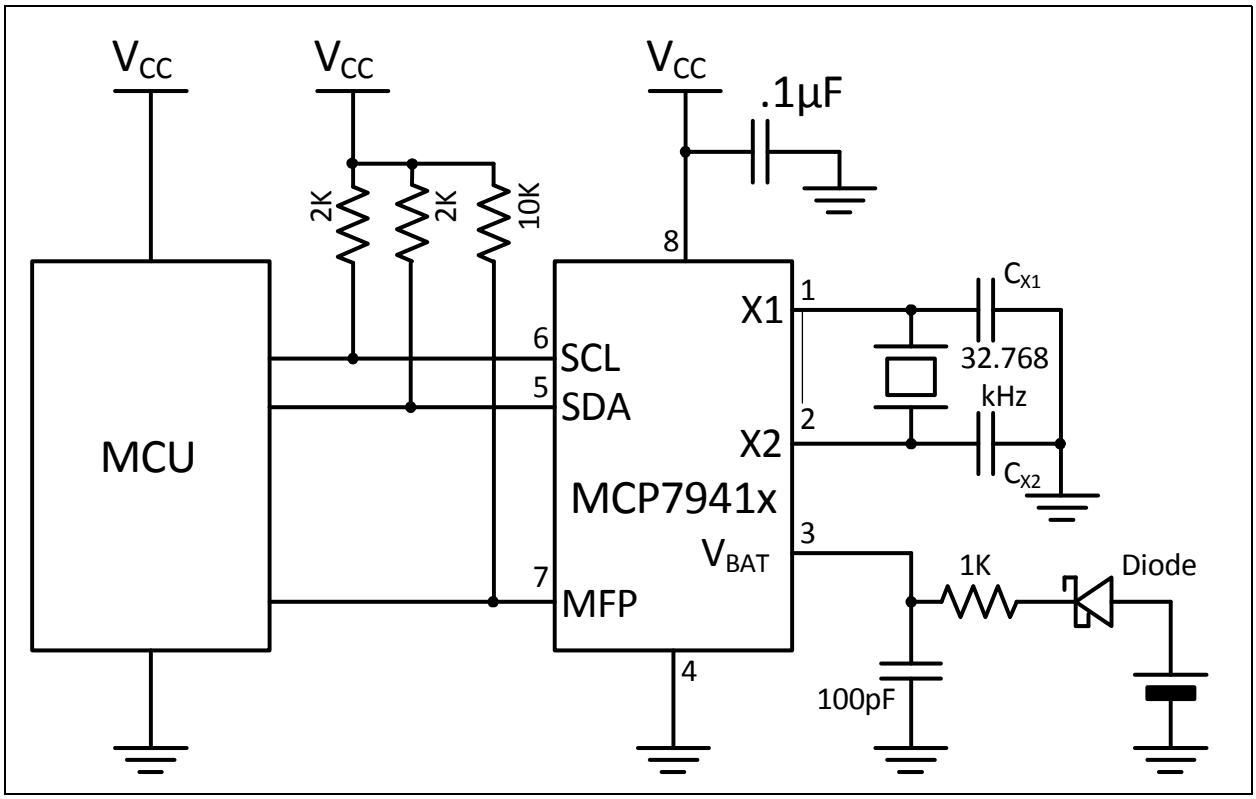
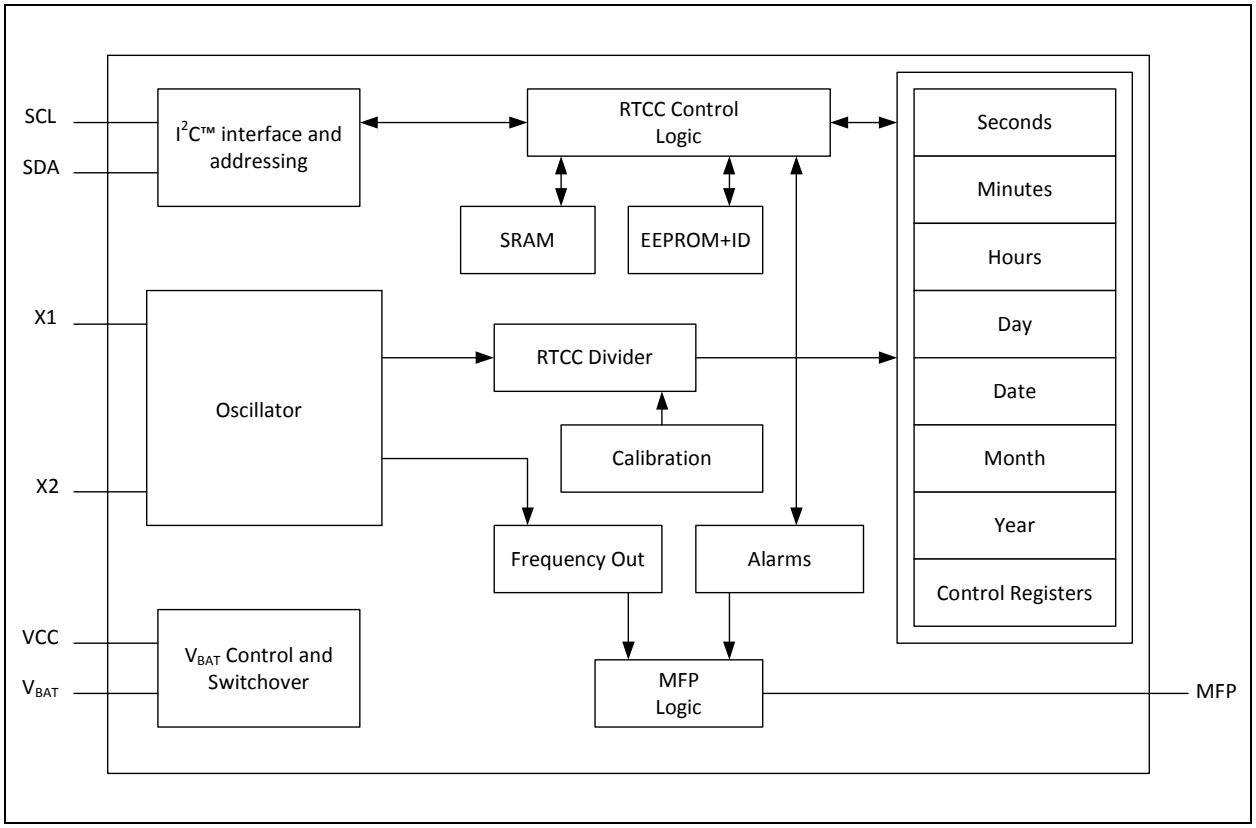


FIGURE 1-2: BLOCK DIAGRAM



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

Maximum voltage on SDA and SCL.....6.5V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
	—	**SCL, SDA pins**	—		—	—	—
D1	VIH	High-level input voltage	0.7 VCC		—	V	—
D2	VIL	Low-level input voltage	—		0.3 VCC 0.2 VCC	V	VCC = 2.5V to 5.5V
D3	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC		—	V	**(Note 1)**
D4	VOL	Low-level output voltage (MFP, SDA)	—		0.40	V	IOL = 3.0 ma @ VCC = 4.5V IOL = 2.1 ma @ VCC = 2.5V
D5	ILI	Input leakage current	—		±1	µA	VIN = VSS or VCC
D6	ILO	Output leakage current	—		±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin capacitance (SDA, SCL and MFP)	—		10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, f = 400 kHz
D8	ICC Read	Operating current EEPROM	—		400	µA	VCC = 5.5V, SCL = 400 kHz
	ICC Write		—		3	mA	VCC = 5.5V
D9	ICC Read	Operating current SRAM	—		300	µA	VCC = 5.5V, SCL = 400 kHz
	ICC Write		—		400	µA	VCC = 5.5V, SCL = 400 kHz
D10	ICCS	Standby current	—		1	µA	VCC = 5.5V, SCL = SDA = VCC **(Note 3)**
	IVCC		—	5	—	µA	VCC = 3.6V @ 25°C, Figure 2-2 **(Note 2)**
D11	VTRIP	VBAT Change Over	1.3	1.5	1.7	V	Typical at TAMB = 25°C
D12	VBAT	VBAT Voltage Range	1.3		5.5	V	**(Note 1)**
D13	IBAT	Operating current, Figure 2-1	— — —	700	1150 1800 5300	nA	VBAT = 1.8V @ 25°C, **(Note 2)** VBAT = 3.0V @ 25°C, **(Note 2)** VBAT = 5.0V @ 25°C, **(Note 2)**
D14	COSC	Oscillator Pin Capacitance	—	3	—	pF	**(Note 1)**

Note 1: This parameter is periodically sampled and not 100% tested.

2: Standby with oscillator running.

3: Standby with oscillator not running.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C			
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
1	FCLK	Clock frequency	— —	100 400	kHz	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
2	THIGH	Clock high time	4000 600	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
3	TLOW	Clock low time	4700 1300	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
4	TR	SDA and SCL rise time **(Note 1)**	— —	1000 300	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
5	TF	SDA and SCL fall time **(Note 1)**	— —	1000 300	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
6	THD:STA	Start condition hold time	4000 600	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
7	TSU:STA	Start condition setup time	4700 600	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
8	THD:DAT	Data input hold time	0	—	ns	**(Note 4)**
9	TSU:DAT	Data input setup time	250 100	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
10	TSU:STO	Stop condition setup time	4000 600	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
11	TAA	Output valid from clock	— —	3500 900	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
12	TBUF	Bus free time: Time the bus must be free before a new transmission can start	4700 1300	— —	ns	1.8V ≤ VCC < 2.5V 2.5V ≤ VCC ≤ 5.5V
13	TSP	Input filter spike suppression (SDA and SCL pins)	—	50	ns	**(Note 1 and Note 2)**
14	TWC	Write cycle time (byte or page)	—	5	ms	—
15	—	Endurance	1M	—	cycles	25°C, VCC = 5.5V Page mode **(Note 3)**
16	TOSF	OSCON Time out	1		ms	**(Note 5)**
17	TFVCC	VCC Fall Time	300		µs	From VTRIP (max) to VTRIP (min) **(Note 1)**
18	TRVCC	VCC Rise Time	0		µs	From VTRIP (min) to VTRIP (max) **(Note 1)**
19	FXTAL	Crystal Frequency		32.768	kHz	

Note 1: Not 100% tested.

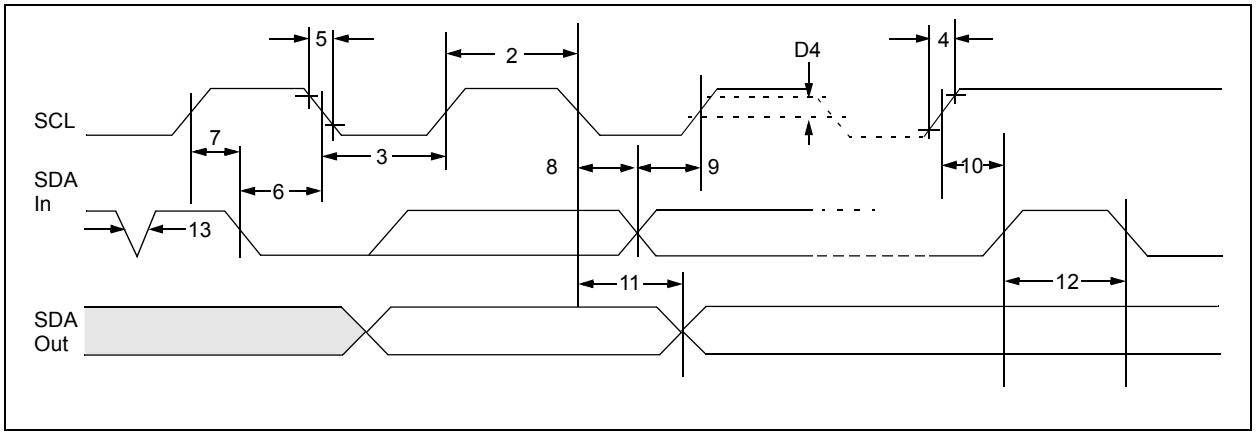
2: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs, which provide improved noise spike suppression.

3: This parameter is not tested but ensured by characterization.

4: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300ns) of the falling edge of the SCL to avoid unintended generation of Start or Stop conditions.

5: Parameter is not tested, ensured by characterization.

FIGURE 1-3: I²C BUS TIMING DATA



2.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

FIGURE 2-1: TYPICAL IBAT VS. VBAT ACROSS TEMPERATURE

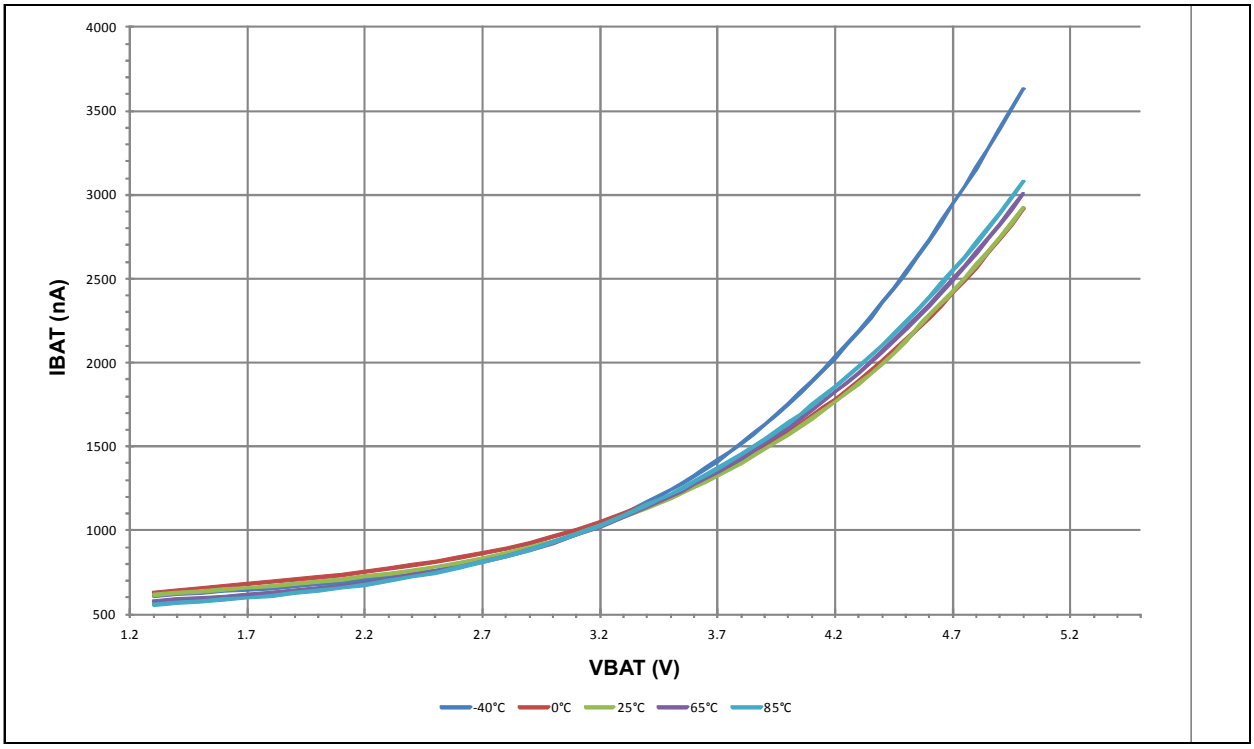
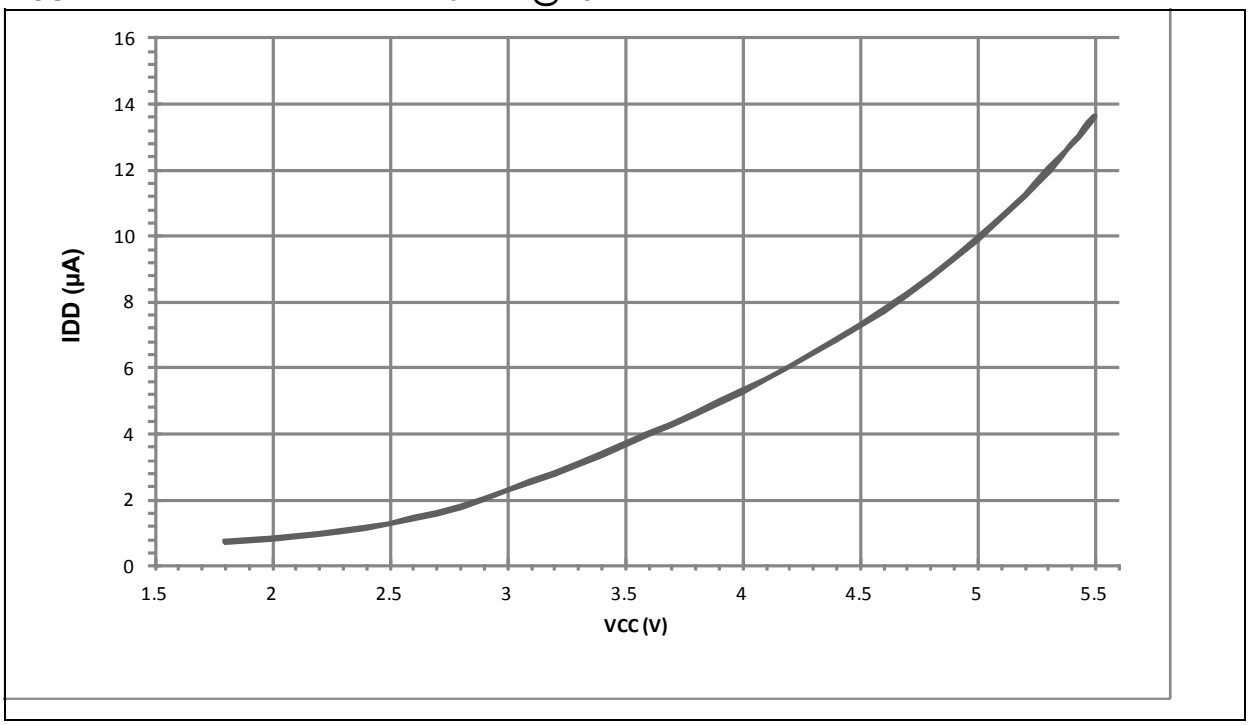


FIGURE 2-2: TYPICAL IVCC VS. VCC @ 25°C



3.0 PIN DESCRIPTIONS

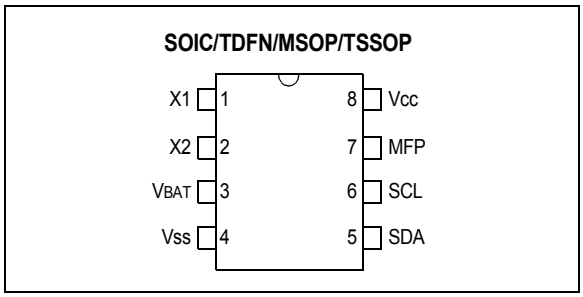
The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN DESCRIPTIONS

Pin Name	Pin Function	Pin Number
X1	Xtal Input, External Oscillator Input	1
X2	Xtal Output	2
VBAT	Battery Backup Input	3
Vss	Ground	4
SDA	Bidirectional Serial Data (I^2C™)	5
SCL	Serial Clock (I^2C)	6
MFP	Multifunction Pin	7
Vcc	Power Supply	8

Note: Exposed pad on TFDN can be connected to Vss or left floating.

FIGURE 3-1: DEVICE PINOUTS



3.1 Serial Data (SDA)

This is a bidirectional pin used to transfer addresses and data into and out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typically 10 kΩ for 100 kHz, 2 kΩ for 400 kHz). For normal data transfer, SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

3.2 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

3.3 X1, X2

External crystal pins for 32.768 kHz crystal and load capacitors.

X1 = Oscillator input, also external oscillator input

X2 = Oscillator output

3.4 MFP (Multifunction Pin)

Open drain pin used for alarm and clock-out, additionally the state of this pin may be changed using the OUT bit. This pin is also controlled by the oscillator bit. See **Section 8.5 "Multifunction PIN (MFP)"** for more details. This pin may be left floating if not used.

3.5 VBAT

Input for backup supply to maintain RTCC and SRAM during the time when VCC is below VTRIP. See **Section 8.6 "Battery Backed Operation"** for more details.

4.0 RTCC FUNCTIONALITY

The MCP7941X family is a highly integrated RTCC. On- board time and date counters are driven from a low-power oscillator to maintain the time and date. An integrated VCC switch enables the device to maintain the time and date, and also the contents of the SRAM during a VCC power failure if an external supply is connected to the VBAT pin and configured.

4.1 Crystal oscillator

The crystal oscillator built into the MCP7941X has been designed to operate with a standard 32.768 kHz tuning fork crystal.

The MCP7941X family of devices require both an external crystal and matching external load capacitors. Capacitors are not included on-chip.

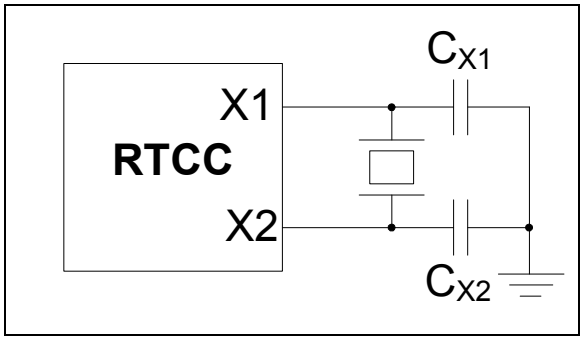
Suitable crystals have a load capacitance (C_L) of 6-9 pF. We do not recommend using crystals with a load capacitance (C_L) of 12.5 pF.

Figure 9.1 shows the required external oscillator components. C_{X1} and C_{X2} pin capacitance and stray capacitance form the crystal load. This is calculated using the equation below:

EQUATION 4-1: CL CALCULATION

$$C_L = \frac{C_{x2} \times C_{x1}}{C_{x2} + C_{x1}} + C_{stray}$$

FIGURE 4-1: OSCILLATOR SCHEMATIC



For a list of tested and recommended crystals, please refer to AN1519, *"Recommended Crystals for Microchip Stand-Alone Real-Time Clock Calendar Devices"*. This document provides a reference for suitable crystals and recommended load capacitors.

For information on suggested board layout, please refer to AN1365, *"Recommended Usage of Microchip Serial RTCC Devices"*.

It is recommended that the final application should be tested with the chosen crystal and capacitor combinations across all operating and environmental conditions. Please also consult the crystal specification to observe correct handling and reflow conditions during assembly.

4.2 RTCC Memory Map

The RTCC registers are contained in addresses 0x00-0x1f. 64 bytes of user-accessible SRAM are located in the address range 0x20-0x5f. The SRAM memory is a separate block from the RTCC Control and Configuration registers. All SRAM locations are battery-backed-up during a VCC power fail. Unused locations are not accessible, MCP7941X will noACK after the address byte if the address is out of range, as shown in the shaded region of the memory map in Figure 4-2.

- Addresses 0x00-0x06 are the RTCC Time and Date registers.

Note: These are Read/Write registers. Care must be taken when writing to these registers with the oscillator running. Incorrect data can appear in the Time and Date registers if a write is attempted during the time frame where these internal registers are being incremented. The user can minimize the likelihood of data corruption by ensuring that any writes to the Time and Date registers occur before the contents of the second register reach a value of 0x59.

- Addresses 0x07-0x09 are the device Configuration, Calibration and ID Unlock registers.
- Addresses 0x0A-0x10 are the Alarm 0 registers. These are used to set up the Alarm 0, the Interrupt polarity and the Alarm 0 Compare.
- Addresses 0x11-0x17 are the same as 0x0Bh-0x11h but are used for Alarm 1.
- Addresses 0x18-0x1F are used for the timestamp feature.

The detailed memory map is shown in Table 4-1.

No error checking is provided when loading Time and Date registers.

FIGURE 4-2: MEMORY MAP

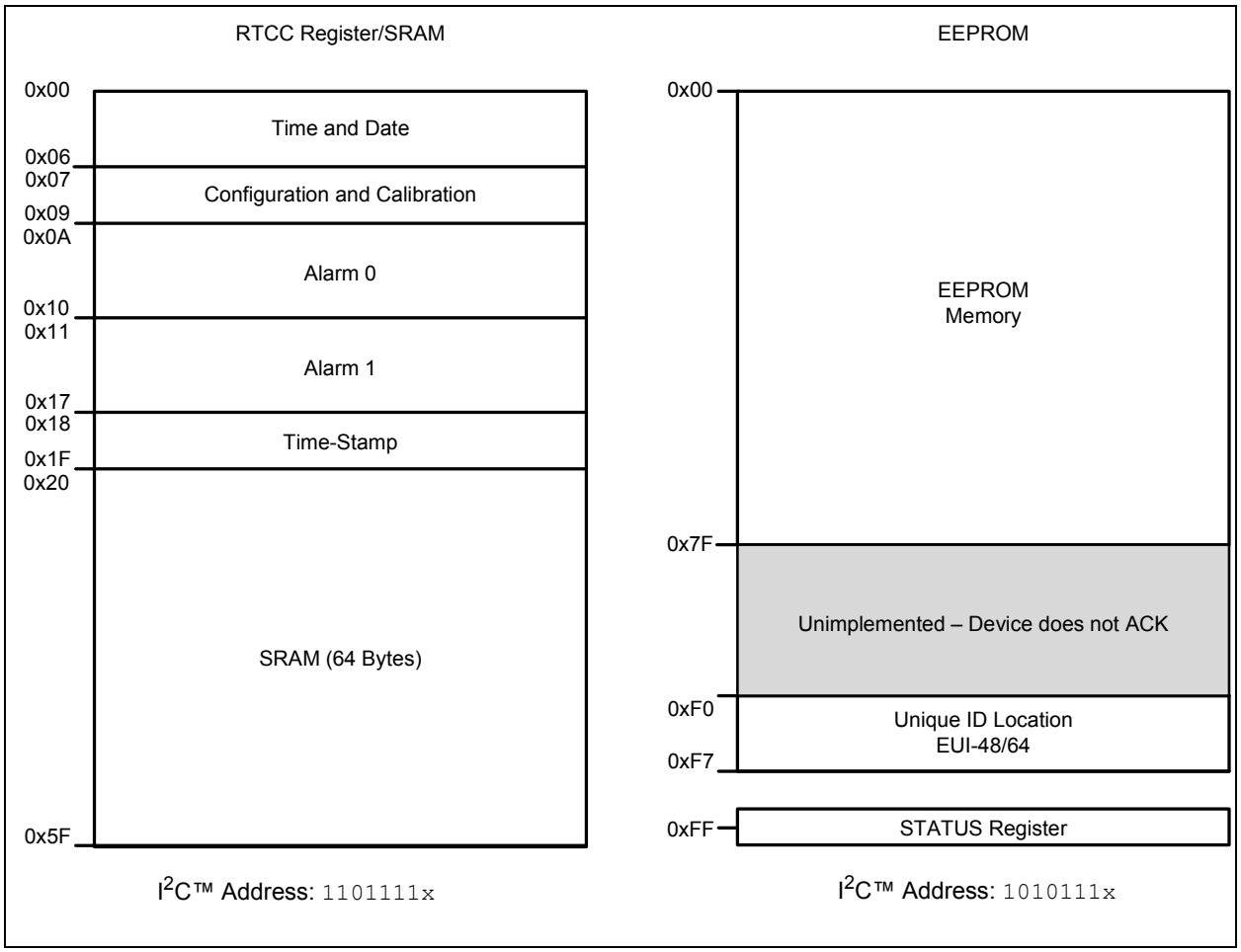


TABLE 4-1: DETAILED RTCC MEMORY MAP

Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Function
Section 5.0 "Time and Date Registers"									
00h	ST	10 Seconds			Seconds				Seconds
01h		10 Minutes			Minutes				Minutes
02h		12/$\overline{24}$	10 Hour AM/PM	10 Hour	Hour				Hours
03h			OSCON	VBAT	VBATEN	Day			Day
04h			10 Date		Date				Date
05h			LP	10 Month	Month				Month
06h	10 Year				Year				Year
07h	OUT	SQWE	ALM1	ALM0	EXTOSC	RS2	RS1	RS0	Control Reg.
08h	CALIBRATION								Calibration
09h	UNIQUE ID UNLOCK								Unlock ID
Section 7.0 "Alarm Registers"									
0Ah		10 Seconds			Seconds				Seconds
0Bh		10 Minutes			Minutes				Minutes
0Ch		12/$\overline{24}$	10 Hour AM/PM	10 Hours	Hour				Hours
0Dh	ALM0POL	ALM0C2	ALM0C1	ALM0C0	ALM0IF	Day			Day
0Eh			10 Date		Date				Date
0Fh				10 Month	Month				Month
10h	Reserved – Do not use								Reserved
Section 7.0 "Alarm Registers"									
11h		10 Seconds			Seconds				Seconds
12h		10 Minutes			Minutes				Minutes
13h		12/$\overline{24}$	10 Hour AM/PM	10 Hours	Hour				Hours
14h	ALM1POL	ALM1C2	ALM1C1	ALM1C0	ALM1IF	Day			Day
15h			10 Date		Date				Date
16h				10 Month	Month				Month
17h	Reserved – Do not use								Reserved
Section 8.6.1 "Power-Down Time-Stamp Registers"									
18h		10 Minutes			Minutes				Power-Down Minutes
19h		12/$\overline{24}$	10 Hour AM/PM	10 Hours	Hour				Power-Down Hours
1Ah			10 Date		Date				Power-Down Date
1Bh	Day			10 Month	Month				Power-Down Day/Month
Section 8.6.2 "Power-Up Time-Stamp Registers"									
1Ch		10 Minutes			Minutes				Power-Up Minutes
1Dh		12/$\overline{24}$	10 Hour AM/PM	10 Hours	Hour				Power-Up Hours
1Eh			10 Date		Date				Power-Up Date
1Fh	Day			10 Month	Month				Power-Up Day/ Month

Note: Grey areas are unimplemented.

5.0 TIME AND DATE REGISTERS

The MCP7941X Serial Real-Time Clock/Calendar uses a low-power external 32.768 kHz crystal to maintain the time and date in a system.

The Real-Time Clock using an external oscillator tracks the time and date with separate registers for hours, minutes, seconds. The MCP7941X also has separate calendar registers for date, month, year and day of the week. The calendar adjusts automatically for months with less than 31 days and also calculates the leap year until 2099.

The Time and Date registers store the current time and date as BCD. Using an external backup supply, the time can be maintained during a VCC power-fail.

REGISTER 5-1: SECONDS 0x00

R/W-0	R/W-0	R/W-0
ST	10 Seconds	Seconds
bit 7	bit 6 bit 4	bit 3 bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **ST:** Start Oscillator bit
1 = Oscillator enabled
0 = Oscillator disabled; The oscillator should be disabled before setting the Time registers.

bit 6-4 **10 SECONDS <6:4>:** Binary-Coded Decimal Value of Second’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONDS<3:0>:** Binary-Coded Decimal Value of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-2: MINUTES 0x01

U-0	R/W-0	R/W-0
—	10 Minutes	Minutes
bit 7	bit 6 bit 4	bit 3 bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **10 MINUTES<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINUTES<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-3: HOUR 0x02

U-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **12/$\overline{24}$:** 12 or 24 Hour Time Format
0 = 24-hour format
1 = 12-hour format

bit 5 **10 HOUR,** AM/$\overline{PM}$

24-Hour format. This is the Ten’s Hour. Bits 5:4 contain the binary-coded decimal of the Ten’s Hour. Contains a value 0 to 2

12-Hour format. This bit contains the AM/PM indicator

0 = PM
1 = AM

bit 4 **10 HOUR**

bit 3-0 **HOUR<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 5

REGISTER 5-4: DAY 0x03

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	
—	—	OSCON	VBAT	VBATEN	Day	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **OSCON:** Oscillator Status bit
Not used in timekeeping (See **Section 8.1 "Oscillator Failure Status"**)

bit 4 **VBAT:** Power-Fail Cycle Status Flag bit
Not used in timekeeping (See **Section 8.6.1 "Power-Down Time-Stamp Registers"**)

bit 3 **VBATEN:** External Battery Enable bit
Not used in timekeeping (See **Section 8.6 "Battery Backed Operation"**)

bit 2-0 **DAY<2:0>:** Undefined, device does not put any limitations on how the day is represented. Binary-Coded Decimal value of day. Contains a value from 1 to 7.

REGISTER 5-5: DATE 0x04

U-0	U-0	R/W-0		R/W-1	
—	—	10 Date		Date	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **10 DATE<1:0>:** Binary-Coded Decimal Value of Dates’s Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATE<3:0>:** Binary-Coded Decimal Value of Dates’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-6: MONTH 0x05

U-0	U-0	R-0	R/W-0	R/W-1	
—	—	LP	10 Month	Month	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **LP:** Leap Year, Set During a Leap Year and is Read-Only
1 = Year is a leap year
0 = Year is not a leap year

bit 4 **10 MONTH:** Binary-Coded Decimal Value of Month’s Tens Digit
Contains a value of 0 or 1

bit 3-0 **MONTH<3:0>:** Binary-Coded Decimal Value of Month’s Ones Digit
Contains a value from 0 to 9

REGISTER 5-7: YEAR 0x06

R/W-0		R/W-1	
10 Year		Year	
bit 7	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7-4 **10 YEAR<3:0>:** Binary-Coded Decimal Value of Year’s Tens Digit
Contains a value from 0 to 9

bit 3-0 **YEAR<3:0>:** Binary-Coded Decimal Value of Year’s Ones Digit
Contains a value from 0 to 9

6.0 CONTROL REGISTER

The Control register is used to enable additional features of the RTCC, such as Alarms and MFP square wave divider. This register also contains bits that can be used to toggle the MFP pin and also allow the RTCC to be driven by an external CMOS 32.768 kHz clock.

REGISTER 6-1: CONTROL REG 0x07

R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OUT	SQWE	ALM1	ALM0	EXTOSC	RS2	RS1	RS0
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7 **OUT:** Level of MFP Pin bit
This bit sets the logic level on the MFP pin when not using this as a square wave output. This pin is open-drain.
1 = Pin is not asserted
0 = Pin is logic low – asserted

bit 6 **SQWE:** Square Wave Enable bit
Setting this bit enables the divided output from the crystal oscillator
1 = Enable square wave
0 = Disable square wave

bit 5 **ALM1:** Alarm 1 Enable bit
1 = Alarm 1 enabled
0 = Alarm 1 disabled

bit 4 **ALM0:** Alarm 0 Enable bit
1 = Alarm 0 enabled
0 = Alarm 0 disabled

bit 3 **EXTOSC:** External Oscillator Input bit
1 = Enable RTCC X1 pin to be driven by external 32.768 kHz source
0 = Disable external 32.768 kHz input.

bit 2 **RS2:** Digital Trimming/Digital Calibration Mode bit
This bit is used to switch between Digital Trimming and Digital Calibration mode
1 = Enable the Digital Calibration mode. Calibration signal appears on CLKOUT if SQWE is set (64 Hz nominal, see **Section 8.4 "Digital Calibration Mode"**).
0 = Disable the calibration output function, Digital trimming is enabled, see **Section 8.3 "Digital Trimming"**.

bit 1-0 **RS<1:0>:** CLKOUT Divider bits
Sets the internal divider for the 32.768 kHz oscillator to be driven to the CLKOUT. The following frequencies are available. The output is responsive to the Calibration register, see **Section 3.4 "MFP (Multifunction Pin)"**.
- 00 – 1 Hz
- 01 – 4.096 kHz
- 10 – 8.192 kHz
- 11 – 32.768 kHz

Note 1: When RS2 is set to enable the calibration output function, the RTCC counters will continue to increment.

7.0 ALARM REGISTERS

The MCP7941X family feature two independent alarms. The registers associated with the alarms are located at 0Ah-16h in the RTCC memory map.

The alarms feature independent interrupt flags and interrupt polarity. The alarms interrupt is generated on the MFP pin.

The alarm function on the MCP7941XX allows the user to load a time into a series of registers that represent a future time. When the current time reaches that set time, the alarm is activated and an interrupt can be generated. Using the alarm feature will allow the system to offload the task to checking for a specific time to the RTCC.

The alarms on the MCP7941X are not single-shot trigger, that is, the alarm will retrigger immediately if the current alarm still matches the set conditions. Clearing the ALMxIF bit while the alarm match is still TRUE will retrigger the alarm. The alarms offer programmable match conditions:

TABLE 7-1:

ALMxC<2:0>	Match Condition	Time Alarm match TRUE Duration
000	Seconds Only	1 Second
001	Minutes Only	1 Minute
010	Hours Only	1 Hour
011	Day Only	1 Day
100	Date Only	1 Day
101	Unimplemented	NA
110	Unimplemented	NA
111	Seconds, Minutes, Hour, Day, Date and Month	1 Second

For example, if the alarm is configured to match on the minutes, when the match is TRUE the alarm will retrigger until the match is FALSE. This would be similar to trying to exit an interrupt on an MCU without clearing the interrupt flag. It is suggested that the Seconds, Minutes, Hour, Day, Date and Month match condition.

Both Alarm0 and Alarm1 offer identical operation.

Note: The X variable used in this section is used to designate Alarm 0 or Alarm 1.

REGISTER 7-1: ALARM X SECONDS (0x0A/0x11)

U-0	R/W-0		R/W-0	
—	10 Seconds		Seconds	
bit 7	bit 6	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **10 SECONDS<2:0>:** Binary-Coded Decimal Value of Second’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **SECONDS<3:0>:** Binary-Coded Decimal Value of Second’s Ones Digit
Contains a value from 0 to 9

REGISTER 7-2: ALARM X MINUTES (0x0B/0x12)

U-0	R/W-0			R/W-0			
—	10 Minutes			Minutes			
bit 7	bit 6		bit 4	bit 3			bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **10 MINUTES<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINUTES<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 7-3: ALARM X HOURS (0x0C/0x13)

U-0	R/W-0	R/W-0	R/W-0	R/W-0			
—	12/24	10 Hour AM/PM	10 Hour	Hour			
bit 7	bit 6	bit 5	bit 4	bit 3			bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **12/24:** This is a copy of bit 6 in the Hours register (0x03)

bit 5 **10 HOUR AM/$\overline{\text{PM}}$**

bit 4 **10 HOUR**

bit 3-0 **HOUR<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

REGISTER 7-4: ALARM X DAY (0x0D/0x14)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	
ALMxPOL	ALMxC2	ALMxC1	ALMxC0	ALMxIF	Day	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7 **ALMxPOL:** The Asserted Level of the Alarm (1 = High, 0 = Low)

bit 6-4 **ALMxC<2:0>:** Alarm X Configuration bits
Sets the condition on what the alarm will trigger. The following options are available:
- 000 – Seconds match
- 001 – Minutes match
- 010 – Hours match (logic takes into account 12/24 operation)
- 011 – Day match. Generates interrupt at 12:00:00 AM
- 100 – Date match
- 101 – Unimplemented, do not use
- 110 – Unimplemented, do not use
- 111 – Seconds, Minutes, Hour, Day, Date and Month

bit 3 **ALMxIF:** Alarm X Interrupt Flag bit
This bit is set by hardware when an alarm condition has been generated. The bit must be cleared in software.
1 = Alarm has been triggered
0 = No alarm pending

bit 2-0 **DAY<2:0>:** Binary-Coded Decimal Value of Day
Contains a value from 1 to 7

REGISTER 7-5: ALARM X DATE (0x0E/0x15)

U-0	U-0	R/W-0		R/W-1	
—	—	10 Date		Date	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **10 DATE<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

REGISTER 7-6: ALARM X MONTH (0x0F/0x16)

U-0	U-0	U-0	R/W-0	R/W-1	
—	—	—	10 Month	Month	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **10 MONTH:** Binary-Coded Decimal Value of Month’s Tens Digit
Contains a value of 0 or 1

bit 3-0 **MONTH<3:0>:** Binary-Coded Decimal Value of Month’s Ones Digit
Contains a value from 0 to 9

8.0 SPECIAL FEATURES

8.1 Oscillator Failure Status

The MCP7941X family of devices support an on-board oscillator failure flag. In register 0x03 (Day Register – shown below), the OSCON (bit 5) provides a way to observe the current status of the oscillator.

The state of the bit indicates the oscillator status.

1 = The oscillator is running

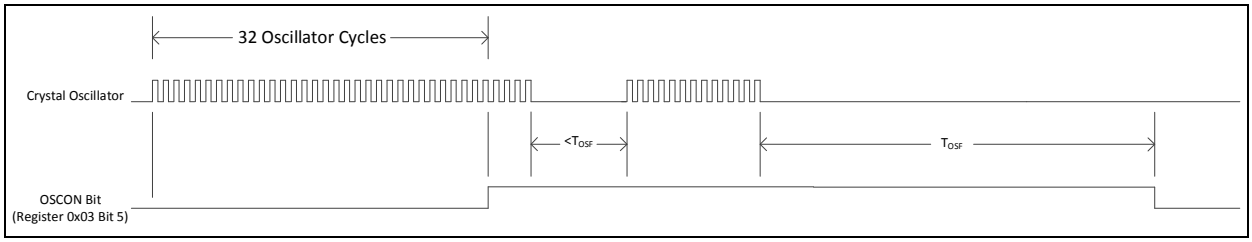
0 = The oscillator is not running

The status does not indicate that the oscillator is running accurately. The OSCON bit is set after 32 stable oscillator cycles. If the oscillator is stopped by either clearing the ST bit or the oscillator support components fail, the OSCON bit is cleared by the hardware after T_{OSF}. This is timed internally using an on-chip time-out circuit.

Figure 8-1 shows the operation.

It should be noted that this bit is both set and cleared by the RTCC hardware, and it will not show that the oscillator failed in the past. The user can poll this bit at any time to determine if the oscillator is running.

FIGURE 8-1: OSCON DIAGRAM



REGISTER 8-1: DAY 0x03

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1
—	—	OSCON	VBAT	VBATEN	Day
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2 bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **OSCON:** Oscillator Status bit
This bit is set and cleared by hardware.
1 = The external oscillator is enabled and running
0 = The external oscillator has stopped or has been disabled

bit 4 **VBAT:** External Battery Switched Flag bit.
Not used in this section.

bit 3 **VBATEN:** External Battery Enable bit
Not used in this section.

bit 2-0 **DAY<2:0>:** Not used in this section.

8.2 Unique ID

The MCP7941X features an additional 64-bit unique ID area. This is separate and in addition to the 1K of on-board EEPROM.

The unique ID is located at addresses 0xF0 through 0xF7 using the EEPROM I^2C address. Reading the unique ID requires the user to simply address these bytes.The unique ID is factory programmed on devices to provide a unique IEEE EUI-48 or EUI-64 value. In addition, customer-provided codes can also be programmed. Please contact your Microchip sales channel for more information on custom programming.

The unique ID locations are always readable.

The format of the unique ID is shown in Figure 8-2. This is an example and the OUI may change.

FIGURE 8-2: EUI-48/64 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE

Description	Unused		24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
Data	FFh	FFh	00h	04h	A3h	12h	34h	56h
Array Address	F0h	F1h	F2h	F3h	F4h	F5h	F6h	F7h

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

Description	24-bit Organizationally Unique Identifier			40-bit Extension Identifier				
Data	00h	04h	A3h	12h	34h	56h	78h	9Ah
Array Address	F0h							F7h

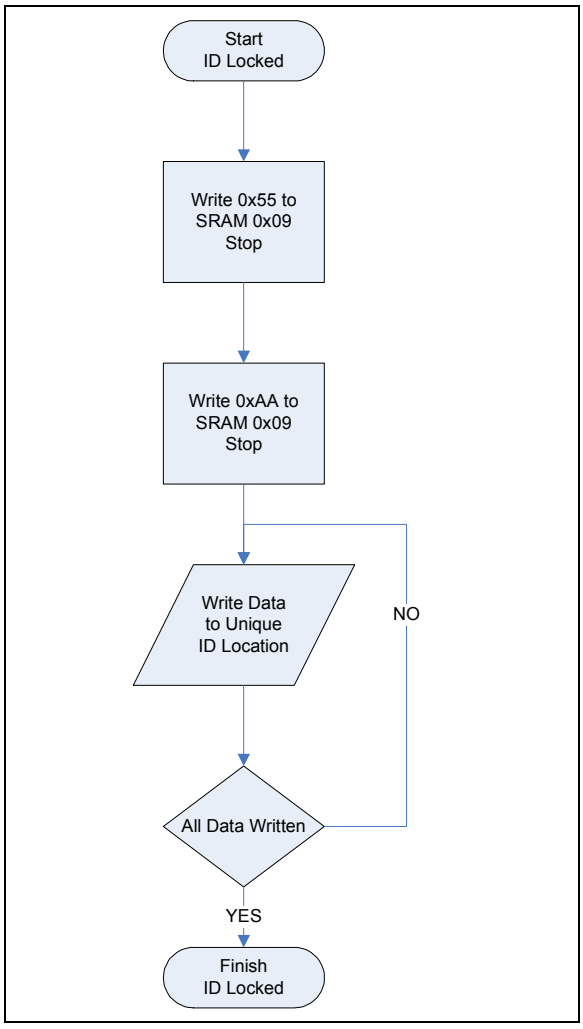
Corresponding EUI-64™ Node Address: 00-04-A3-12-34-56-78-9A

The unique ID area is protected to prevent unintended writes to these locations. The unlock sequence is detailed in **8.2.1 "Unlock Sequence"** and consists of the following sequence:

- A single write of 0x55 to RTCC Addr. 0x09. Stop
- A single write of 0xAA to RTCC Addr. 0x09. Stop

A Stop condition must be used to terminate a I^2C sequence, a Restart will not complete the sequence.

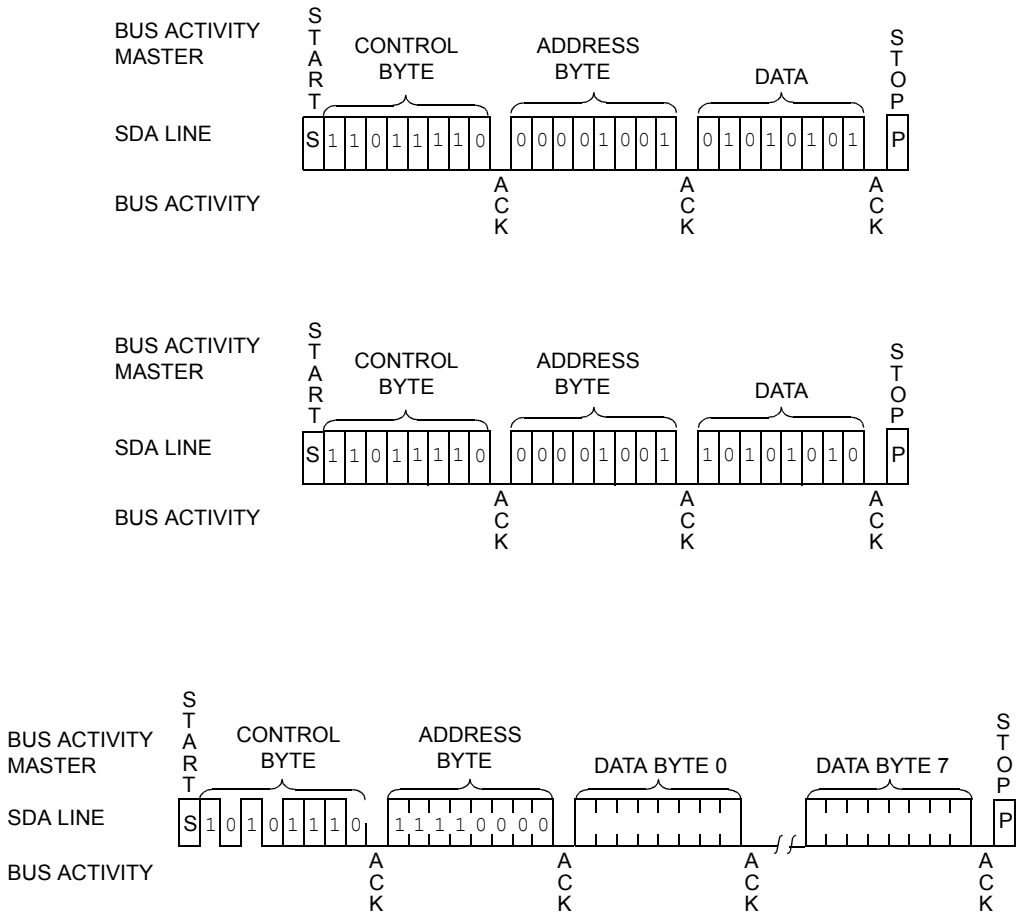
FIGURE 8-3: ID UNLOCK FLOWCHART



8.2.1 UNLOCK SEQUENCE

The I^2C bus sequence to unlock the unique ID locations is show in Figure 8-4. This example shows all eight locations being written, any location may be written individually.

FIGURE 8-4: UNIQUE ID UNLOCK SEQUENCE



REGISTER 8-2: UNLOCK ID 0x09

W-0							
UNIQUE UNLOCK ID SEQUENCE							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7-0 **UNLOCK ID:** This is the unlock sequence address. To unlock write access to the unique ID area in the EEPROM, a sequence must be written to this address in separate commands. The process is shown in Figure 8-4.

8.3 Digital Trimming

The MCP7941X uses digital trimming to correct for inaccuracies of the input clock source (either externally driven or from a crystal). These inaccuracies are due to crystal, capacitor and temperature variations. This enables the user to compensate for differences in temperature over the operating conditions of the device, offering higher time accuracy over an uncalibrated RTCC. Digital trimming is always enabled in the MCP794XX device. Digital trimming is achieved by digitally modifying the number of clock cycles per minute to achieve PPM level adjustments in the internal timing function of the MCP7941X. The amount by which the MCP794XX adjusts the time is determined by the value loaded into the calibration register. A value of 0x00 in the calibration register results in no time adjustment. The Calibration value is maintained during a VCC power-fail if the backup supply is enabled. Digital trimming is also performed during this time. The same calibration value is used until it is changed by the system firmware.

REGISTER 8-3: CALIBRATION 0x08

R/W-0	
CALSIGN	CALIBRATION
bit 7	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7 **CALSIGN:** Sign of Calibration, allows for positive and negative calibration

bit 6-0 **CALIBRATION<6:0>:** Calibration Value bits

Note 1: This is an 8-bit register that is used to add or subtract clocks from the RTCC counter every minute. The MSB is the sign bit and indicates if the count should be added or subtracted. The remaining 7 bits, with each bit adding or subtracting two clocks, give the user the ability to add or subtract up to 254 clocks per minute. Each bit represents ±1.017 ppm.

The MSB of the Calibration register is the sign bit, with a '1' indicating a negative PPM calibration and a '0' indicating a positive PPM calibration. The calibration value can range from 0 to 127, combined with the sign bit this gives the MCP7941X the ability to calibrate ±129 ppm of combined error. The calibration is performed on the minute rollover.

Given that each bit provides ±2 internal clocks of trimming, the effective PPM of each bit is ±1.017 ppm.

The calibration value is determined by measuring the error over a period of time. If the time is running fast then a positive calibration is loaded into the Calibration register. Conversely, if the time is running slow, a negative calibration is loaded.

Example: Time is running fast five seconds per day.

Five seconds per day can be expressed in PPM using Equation 8-1.

EQUATION 8-1:

$$PPM = \frac{(Seconds\ per\ day \times 1x10^{6})}{24 \times 60 \times 60}$$

Giving

$$58PPM = \frac{(5x10^{6})}{(86400)}$$

Calibration register Value

$$57 = \frac{58PPM}{1.017PPM}$$

In this example, the calibration value to be loaded is 57. The same method can be used if the MCP7941X is running slow.

8.4 Digital Calibration Mode

The MCP7941X utilizes digital trimming to correct for inaccuracies of the input clock source. However, as this internal trimming is performed on the minute rollover, a Digital Calibration mode is available. Using this mode the oscillator frequency can be directly observable.

The internal timing function can be monitored using the MFP open-drain output pin by setting bit<6:0> (SQWE) and bits<2:0> (RS2, RS1, RS0) of the control register (see Section 6.0, Control register). Note that the MFP output waveform is disabled when the MCP7941X is running in VBAT mode. With the SQWE bit set to '1', and the RS2 bit set to '1' the Digital Calibration mode is enabled.

Unlike digital trimming previously described, the calibration setting is continuously applied and affects every cycle of the output waveform. This results in the modulation of the frequency of the output waveform based upon the setting of the Calibration register.

Using this setting, the calibration function can be expressed as:

$$T_{output} = (2 * (256 +/- (2 * CALREG))) T_{input}$$

where:

T_{output} = clock period of MFP output signal

T_{input} = clock period of input signal

CALREG = decimal value of the Calibration register setting, and the sign is determined by the MSB of the Calibration register.

Since the calibration is done every cycle, the frequency of the output MFP waveform is constant. With a crystal frequency of exactly 32.768 kHz the output on the MFP pin will be 64 Hz. Deviation of the crystal frequency will shift this frequency.

8.5 Multifunction PIN (MFP)

Pin 7 is a multifunction pin and supports the following functions:

- The value of the OUT bit determines the logic level of the I/O. This is only available when operating from VCC.
- Alarm Outputs – Available when operating from VCC or backup power supply
- FOUT mode – driven from a FOSC divider – Not available when operating from backup power supply (CLKOUT mode)

The internal control logic for the MFP is connected to the switched internal supply bus, this allows operation in VBAT mode. The Alarm Output is the only mode that operates when operating from backup power supply, other modes are suspended, see Table 8-2.

The following diagram shows how the internal MFP control logic is implemented. This pin in an open-drain and can be left floating if it is not being used.

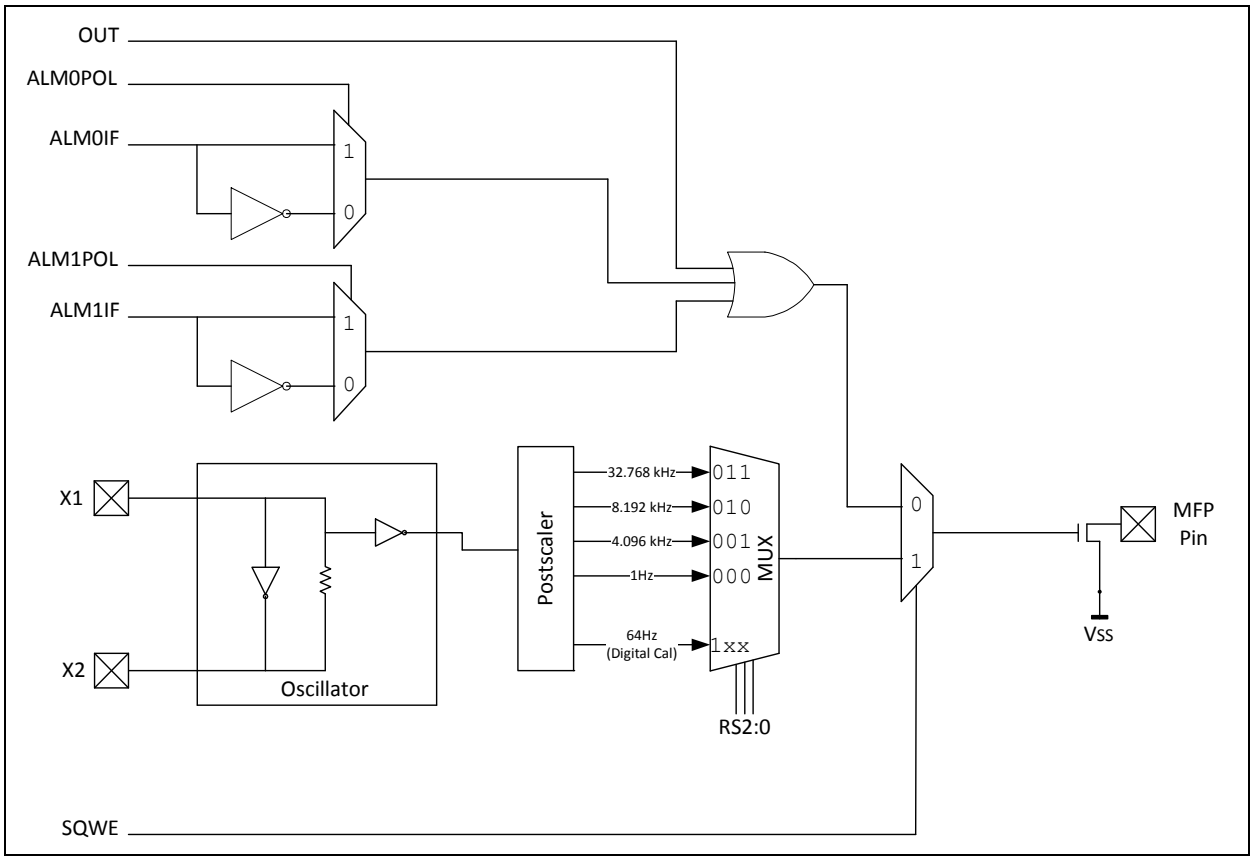
When the MFP is used for CLKOUT mode of operation the following frequencies are available.

TABLE 8-1: CLKOUT DIVIDER

RS2	RS1	RS0	CLKOUT Frequency
0	0	0	32.768 kHz*
0	0	1	8.192 kHz
0	1	0	4.096 kHz
0	1	1	1Hz

Note: *Not effected by calibration

FIGURE 8-5: MFP FUNCTIONAL BLOCK DIAGRAM



8.6 Battery Backed Operation

The MCP7941X features an internal power switch that can power the clock and the SRAM in the event that the VCC supply is not available. The voltage applied to the VBAT pin serves as the backup supply. To enable the external battery switchover operation, bit 3 VBATEN (Day Register) must be set. Setting this bit enables the path from the VBAT pin to the internal power switch.

A 1K series resistor is recommended between the external battery and the VBAT pin to limit the current to the internal switch circuit. Additionally, an 100 pF capacitor is required between the VBAT pin and VSS.

This is shown in Figure 1-1.

The VTRIP is the voltage at which the internal switch operates the device from the VBAT supply. When it falls below VTRIP, the system will continue to operate the RTCC and SRAM using the VBAT supply. When VCC is above VTRIP the device is operated using the main supply. The following conditions apply:

TABLE 8-2: MFP FUNCTION WITH SUPPLY

Supply Condition	Read/Write Access	Powered By	CLKOUT	Alarms	Time Keeping
VCC < VTRIP	No	VBAT	No	Yes	Yes
VCC > VTRIP	Yes	VCC	Yes	Yes	Yes

If the battery backup feature is not being used, the VBAT pin should be connected to GND.

For more information on VBAT conditions, see AN1365, *"RTCC Best Practices"*.

REGISTER 8-4: DAY 0x03

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	
—	—	OSCON	VBAT	VBATEN	Day	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5 **OSCON:** Oscillator Status bit
Not Used in this section.

bit 4 **VBAT:** External Battery Switched Flag bit
Not Used in this section.

bit 3 **VBATEN:** External Battery Enable bit
1 = The internal battery switch over is connected to the VBAT pin
0 = VBAT pin is disconnected and the only current drain on the external battery is the VBAT pin leakage

bit 2-0 **DAY<2:0>:** Not Used in this section

8.6.1 POWER-DOWN TIME-STAMP REGISTERS

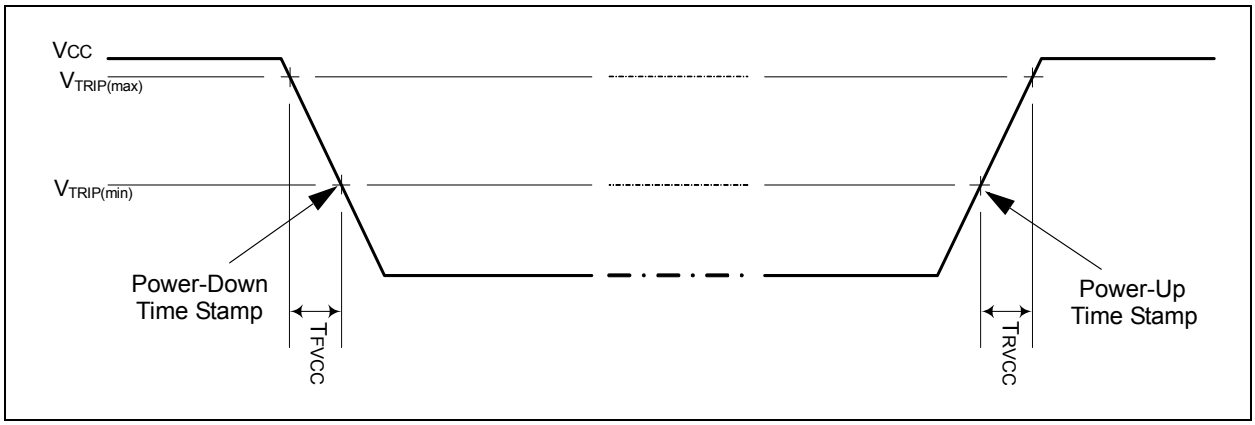
The MCP7941X family of RTCC devices feature a power-fail time-stamp feature. This feature will store the time at which VCC crosses the VTRIP voltage and is shown in Figure 8-6. To use this feature, a VBAT supply must be present and the oscillator must also be running. The month through minutes are saved.

There are two separate sets of registers that are used to record this information:

- The first set, located at 0x18 through 0x1B, is loaded at the time when VCC falls below VTRIP and the RTCC operates on the VBAT. The VBAT (Day register bit 4) bit is also set at this time.
- The second set of registers, located at 0x1C through 0x1F, is loaded at the time when VCC is restored and the RTCC switches to VCC.

The power-fail time-stamp registers are cleared when the VBAT (Day register bit 4) bit is cleared in software. Only the first power-down and power-up time-stamps are saved by the RTCC.

FIGURE 8-6: POWER-FAIL GRAPH



Note:	It is strongly recommended that the time saver function only be used when the oscillator is running. This will ensure accurate functionality.

REGISTER 8-5: MINUTES 0x18

U-0	R/W-0			R/W-0	
—	10 Minutes			Minutes	
bit 7	bit 6		bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **10MINUTES<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINUTES<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 8-6: HOURS 0x19

U-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **12/$\overline{24}$:** This is a copy of the status of the bit in register 0x03:6 at the time of the event

bit 5 **10 HOUR AM/$\overline{PM}$**

bit 4 **10 HOUR**

bit 3-0 **HOUR<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

REGISTER 8-7: DATE 0x1A

U-0	U-0	R/W-0		R/W-0	
—	—	10 Date		Date	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-4 **10 DATE<1:0>:** Binary-Coded Decimal Value of Date’s Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATE<3:0>:** Binary-Coded Decimal Value of Date’s Ones Digit
Contains a value from 0 to 9

REGISTER 8-8: MONTH 0x1B

R/W-0		R/W-0	R/W-0	
Day		10 Month	Month	
bit 7	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7-5 **DAY<2:0>:** Binary-Coded Decimal Value of Day. Contains a value from 1 to 7.

bit 4 **10 MONTH:** Binary-Coded Decimal Value of Month’s Ones Digit
Contains a value of 0 or 1

bit 3-0 **MONTH<3:0>:** Binary-Coded Decimal Value of Month’s Ones Digit
Contains a value from 0 to 9

8.6.2 POWER-UP TIME-STAMP REGISTERS

Note:	It is strongly recommended that the time saver function only be used when the oscillator is running. This will ensure accurate functionality.

REGISTER 8-9: MINUTES 0x1C

U-0	R/W-0			R/W-0			
—	10 Minutes			Minutes			
bit 7	bit 6		bit 4	bit 3			bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6-4 **10 MINUTES<2:0>:** Binary-Coded Decimal Value of Minute’s Tens Digit
Contains a value from 0 to 5

bit 3-0 **MINUTES<3:0>:** Binary-Coded Decimal Value of Minute’s Ones Digit
Contains a value from 0 to 9

REGISTER 8-10: HOURS 0x1D

U-0	R/W-0			R/W-0			
—	12/$\overline{24}$	10 Hour AM/$\overline{PM}$	10 Hour	Hour			
bit 7	bit 6	bit 5	bit 4	bit 3			bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	“0” = Bit is clear	“X” = Bit is unknown

bit 7 **Unimplemented:** Read as ‘0’

bit 6 **12/$\overline{24}$:** This is a copy of the status of the bit in register 0x03:6 at the time of the event

bit 5 **10 HOUR AM/$\overline{PM}$**

bit 4 **10 HOUR**

bit 3-0 **HOUR<3:0>:** Binary-Coded Decimal Value of Hour’s Ones Digit
Contains a value from 0 to 9

REGISTER 8-11: DATE 0x1E

U-0	U-0	R/W-0		R/W-0	
—	—	10 Date		Date	
bit 7	bit 6	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **10 DATE<1:0>:** Binary-Coded Decimal Value of Date's Tens Digit
Contains a value from 0 to 3

bit 3-0 **DATE<3:0>:** Binary-Coded Decimal Value of Date's Ones Digit
Contains a value from 0 to 9

REGISTER 8-12: MONTH 0x1F

R/W-0		R/W-0	R/W-0	
Day		10 Month	Month	
bit 7	bit 5	bit 4	bit 3	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7-5 **DAY<2:0>:** Binary-Coded Decimal Value of Days
Contains a value from 1 to 7

bit 4 **10 MONTH:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value of 0 or 1

bit 3-0 **MONTH<3:0>:** Binary-Coded Decimal Value of Month's Ones Digit
Contains a value from 0 to 9

9.0 I²C BUS CHARACTERISTICS

9.1 I²C Interface

The MCP7941X supports a bidirectional 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as transmitter, and a device receiving data as receiver. The bus has to be controlled by a master device which generates the Start and Stop conditions, while the MCP7941X works as slave. Both master and slave can operate as transmitter or receiver but the master device determines which mode is activated.

9.1.1 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 9-1).

9.1.1.1 Bus not Busy (A)

Both data and clock lines remain high.

9.1.1.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

9.1.1.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

9.1.1.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the master device.

9.1.1.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge signal after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The MCP7941X does not generate any EEPROM Acknowledge bits if an internal programming cycle is in progress. The user may still access the SRAM and RTCC registers during an EEPROM write.

A device that acknowledges must pull down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by NOT generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (MCP7941X) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 9-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

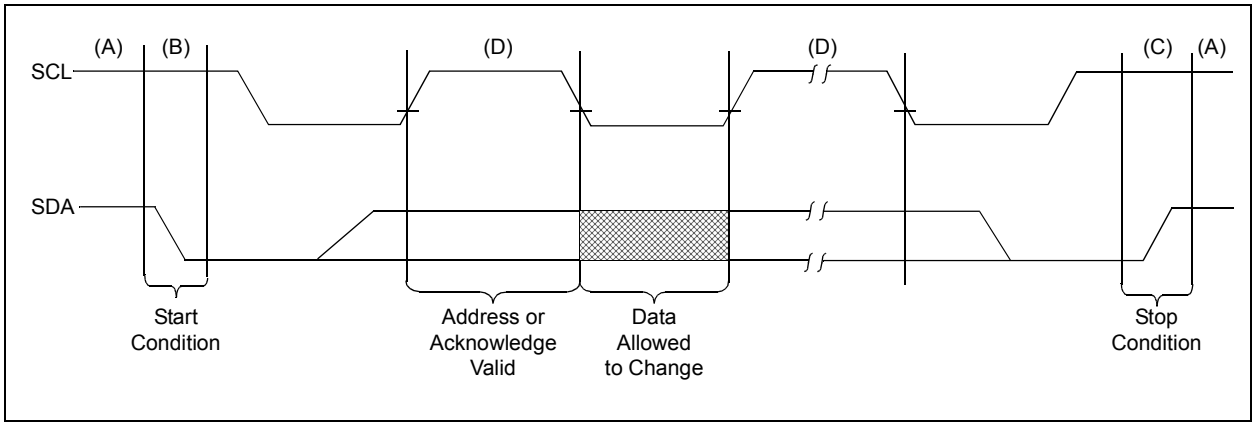
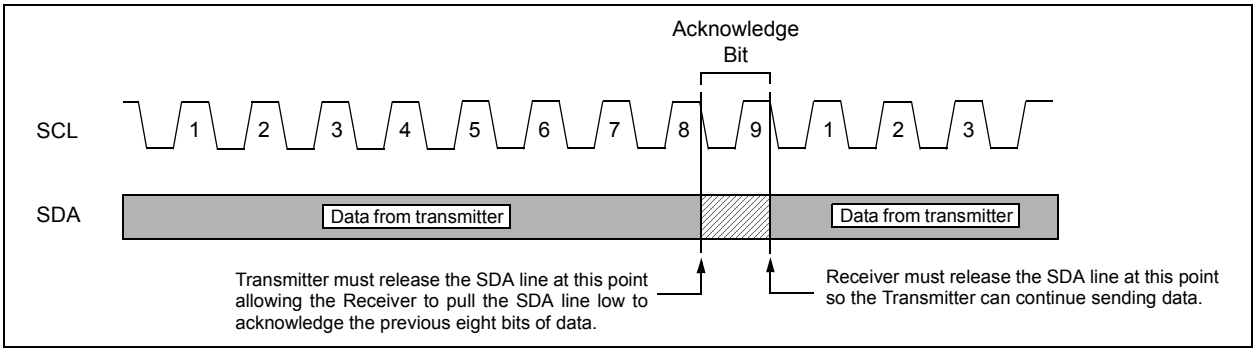


FIGURE 9-2: ACKNOWLEDGE TIMING



9.1.2 DEVICE ADDRESSING AND OPERATION

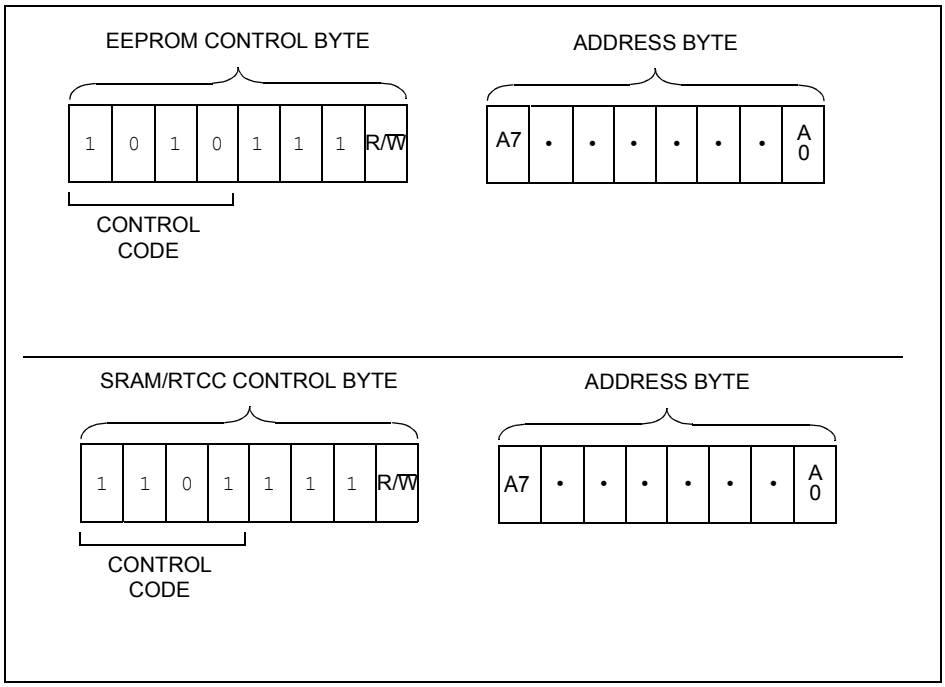
A control byte is the first byte received following the Start condition from the master device (Figure 9-2). The control byte consists of a control code; for the MCP7941X this is set as '1010111X' for read (0xAF) and write (0xAE) operations for the EEPROM.

The control byte for accessing the SRAM and RTCC registers are set to '1101111X' (0xDF for a read, 0xDE for a write). The RTCC registers and the SRAM share the same address space.

The last bit of the control byte defines the operation to be performed. When set to a '1' a read operation is selected, and when set to a '0' a write operation is selected. The next byte received defines the address of the data byte (Figure 9-3). The upper address bits are transferred first, followed by the Least Significant bits (LSb).

Following the Start condition, the MCP7941X monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving an '1010111X' or '1101111X' code, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the MCP7941X will select a read or write operation.

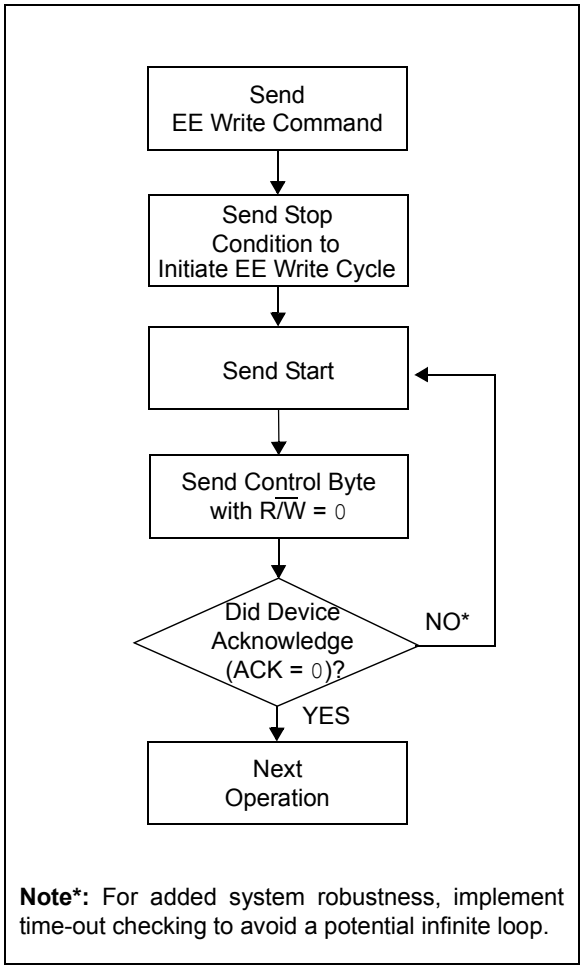
FIGURE 9-3: CONTROL BYTE AND ADDRESS SEQUENCE BIT ASSIGNMENTS



9.1.3 ACKNOWLEDGE POLLING

Since the device will not acknowledge an EEPROM command during an EEPROM write cycle, this can be used to determine when the cycle is complete. This feature can be used to maximize bus throughput. Once the Stop condition for a Write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a Start condition, followed by the control byte for a Write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK, and the master can then proceed with the next Read or Write command. See Figure 9-4 for the flow diagram.

FIGURE 9-4: ACKNOWLEDGE POLLING FLOW



Note*: For added system robustness, implement time-out checking to avoid a potential infinite loop.

Note: For added systems robustness, it is recommended that time-out functionality be implemented in the acknowledge polling routine to avoid potentially hanging the system by entering an infinite loop. This can easily be done by designing in a maximum number of loops the routine will execute, or through the use of a hardware timer

If a time out occurs, polling should be aborted by sending a Stop condition. A user-generated error-handling routine can then be called, allowing the system to recover in a manner appropriate for the application.

10.0 ON-BOARD MEMORY

The MCP7941X has both on-board EEPROM memory and battery-backed SRAM. The SRAM is arranged as 64 bytes and is retained when the VCC supply is removed, provided the VBAT supply is present and enabled. The EEPROM is organized as 128 x 8 bytes. The EEPROM is nonvolatile memory and does not require the VBAT supply for retention.

10.1 SRAM/RTCC

FIGURE 10-1: SRAM/RTCC BYTE WRITE

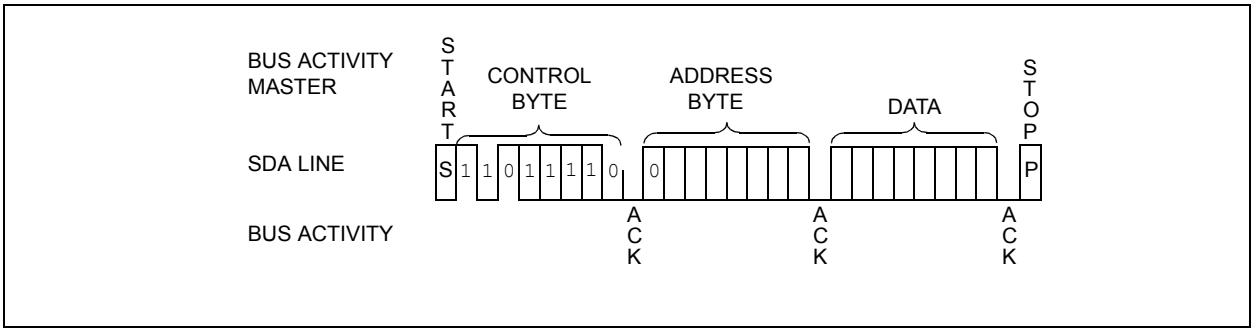
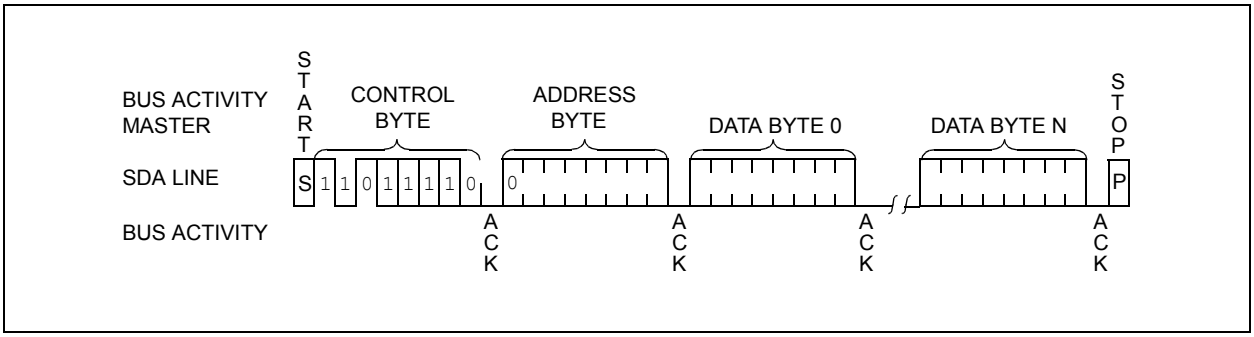


FIGURE 10-2: SRAM/RTCC MULTIPLE BYTE WRITE



The 64 bytes of user SRAM are at location 0x20h and can be accessed during the time when the RTCC is being internally updated. Upon POR, the SRAM will be in an undefined state.

Writing to the SRAM and RTCC is accomplished in a similar way to writing to the EEPROM (as described later in this document) with the following considerations:

- There is no page. The entire 64 bytes of SRAM or 32 bytes of RTCC register can be written in one command.
- The SRAM allows an unlimited number of read/write cycles.
- The RTCC and SRAM are not accessible when the device is running on the external VBAT supply.
- The RTCC and SRAM are separate blocks. The SRAM array may be accessed during an RTCC update.
- Read and write access is limited to either the RTCC register block or the SRAM array. The Address Pointer will rollover to the start of the addressed block.
- Data written to the RTCC and SRAM are on a per byte basis.

Note: Entering an address past 0x5F for an SRAM operation will result in the MCP7941X not acknowledging the address.

10.2 EEPROM

The MCP794XX features 1Kbits of internal high endurance EEPROM. This EEPROM block features an 8-byte page.

10.2.1 BLOCK PROTECTION

The EEPROM does not support a hardware write protection pin, however, software block protection is available to the user and is configured using the STATUS register.

10.2.2 STATUS REGISTER

The STATUS register is in the nonvolatile EEPROM array. To access the STATUS register, the address of 0xFFh is written to and read from. ACK polling may be used to determine if the write is complete. The bits in this register are defined as:

- Bit 3:2 (BP<1:0>) are the EEPROM array block protection bits. If an attempt is made to perform a write to an area of EEPROM that is protected, the MCP794XX will acknowledge but the write will not take place. These bits are in the nonvolatile EEPROM array. This allows protection of the following areas:

TABLE 10-1: BLOCK PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	None
0	1	Upper 1/4 (60h-7Fh)
1	0	Upper 1/2 (40h-7Fh)
1	1	All (00h-7Fh)

- The unused bits are reserved at this time and read as '0'.
- With the current address read operation, the address is not incremented. Consequently, the subsequent reads are done from the same location.

If multiple bytes are loaded to the STATUS register, only the last byte is written. The write to the STATUS register is initiated by the I^2C Stop condition.

REGISTER 10-1: STATUS REGISTER 0xFF

U	U	U	U	R/W-0	R/W-0	U	U
—	—	—	—	BP1	BP0	—	—
bit 7				bit 3	bit 2		bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	"0" = Bit is clear	"X" = Bit is unknown

bit 7-4 **Unimplemented:** Read as '0'

bit 3-2 **BP<1:0>:** EEPROM Array Block Protection bits

bit 1-0 **Unimplemented:** Read as '0'

10.2.3 EEPROM BYTE WRITE

Following the Start condition from the master, the control code and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the master is the word address and will be written into the Address Pointer of the MCP7941X. After receiving another Acknowledge signal from the MCP7941X, the master device transmits the data word to be written into the addressed memory location. The MCP7941X acknowledges again and the master generates a Stop condition. This initiates the internal write cycle, and, during this time, the MCP7941X does not generate Acknowledge signals for EEPROM Write commands. Access to the RTCC/SRAM registers is possible during an EEPROM write cycle.

If an attempt is made to write to an address and the protection is set then the device will acknowledge the command but no write cycle will occur, no data will be written, and the device will immediately accept a new command. After a byte Write command, the internal address counter will point to the address location following the one that was just written.

10.2.4 EEPROM PAGE WRITE

The write control byte, word address, and the first data byte are transmitted to the MCP7941X in the same way as in a byte write. But instead of generating a Stop condition, the master transmits up to seven additional bytes (MCP7941X has an 8-byte page), which are temporarily stored in the on-chip page buffer and will be written into memory after the master has transmitted a Stop condition. After receipt of each word, the three lower Address Pointer bits are internally incremented by one. If the master should transmit more than eight bytes prior to generating the Stop condition, the address counter will roll over and the data received previously will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 10-4).

Note: Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being transmitted. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or ‘page size’) and end at addresses that are integer multiples of [page size - 1]. If a page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

Note: Addressing undefined EEPROM locations will result in the MCP7941X not acknowledging the address.

FIGURE 10-3: EE BYTE WRITE

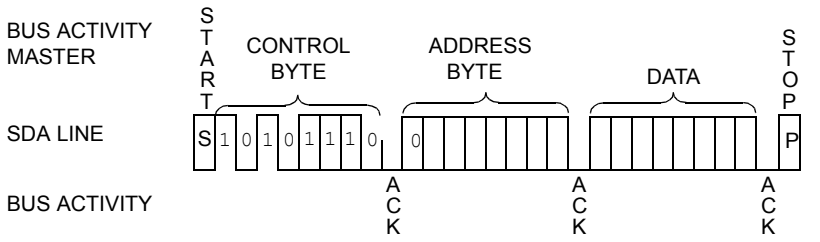
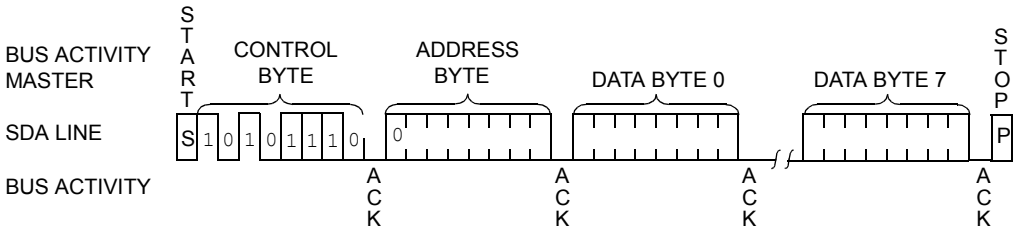


FIGURE 10-4: EE PAGE WRITE



10.2.5 READ OPERATION

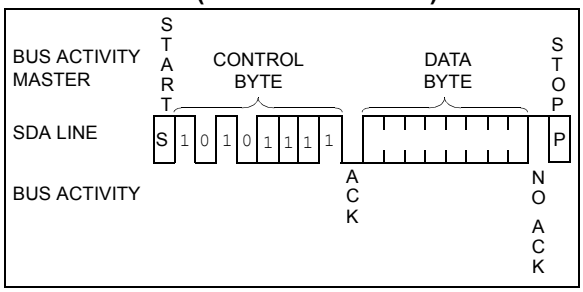
Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

10.2.5.1 Current Address Read

The MCP7941X contains an address counter that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1. In the case of a page write, if the last byte written is the last byte of a page, the next address location would be the first byte of the same page written.

Upon receipt of the control byte with R/$\overline{W}$ bit set to one, the MCP7941X issues an Acknowledge and transmits the 8-bit data word. The master will not acknowledge the transfer but does generate a Stop condition and the MCP7941X discontinues transmission (Figure 10-1).

FIGURE 10-1: CURRENT ADDRESS READ (EEPROM SHOWN)



10.2.5.2 Random Read

Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the MCP7941X as part of a write operation (R/$\overline{W}$ bit set to '0'). After the word address is sent, the master generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the master issues the control byte again but with the R/$\overline{W}$ bit set to a one. The MCP7941X will then issue an Acknowledge and transmit the 8-bit data word. The master will not acknowledge the transfer but it does generate a Stop condition which causes the MCP7941X to discontinue transmission (Figure 10-2). After a random Read command, the internal address counter will point to the address location following the one that was just read.

10.2.5.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the MCP7941X transmits the first data byte, the master issues an Acknowledge as opposed to the Stop condition used in a random read. This Acknowledge directs the MCP7941X to transmit the next sequentially addressed 8-bit word (Figure 10-3). Following the final byte transmitted to the master, the master will NOT generate an Acknowledge but will generate a Stop condition. To provide sequential reads, the MCP7941X contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows the entire memory contents to be serially read during one operation. The internal Address Pointer will automatically roll over to the start of the Block.

FIGURE 10-2: RANDOM READ (EEPROM SHOWN)

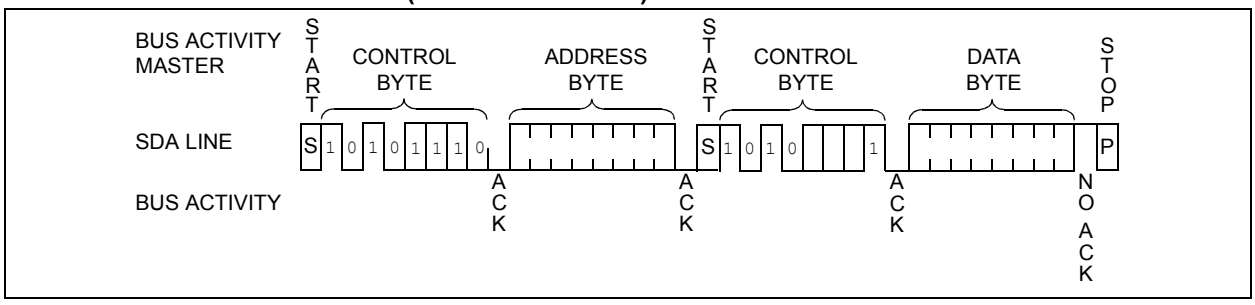
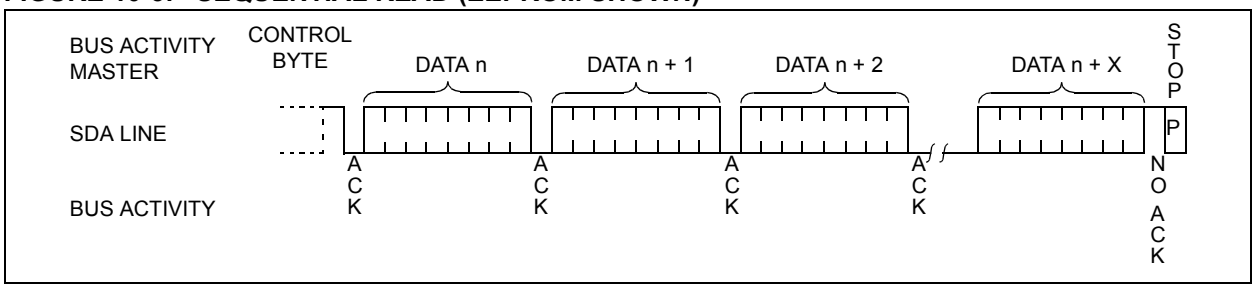


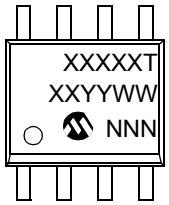
FIGURE 10-3: SEQUENTIAL READ (EEPROM SHOWN)



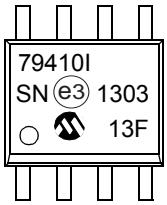
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

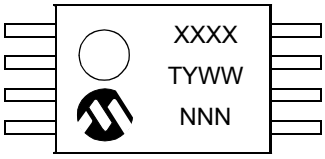
8-Lead SOIC (3.90 mm)



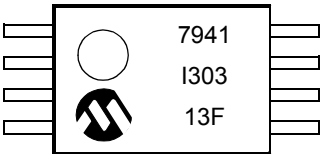
Example:



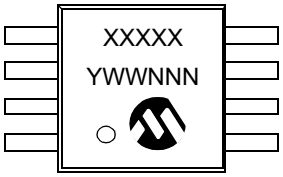
8-Lead TSSOP



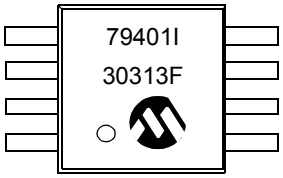
Example:



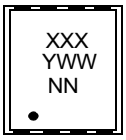
8-Lead MSOP



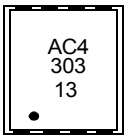
Example:



8-Lead 2x3 TDFN



Example:



Part Number	1st Line Marking Codes		
	TSSOP	MSOP	TDFN
MCP79410	7941	79410T	AAP
MCP79411	9411	79411T	AAQ
MCP79412	9412	79412T	AAR

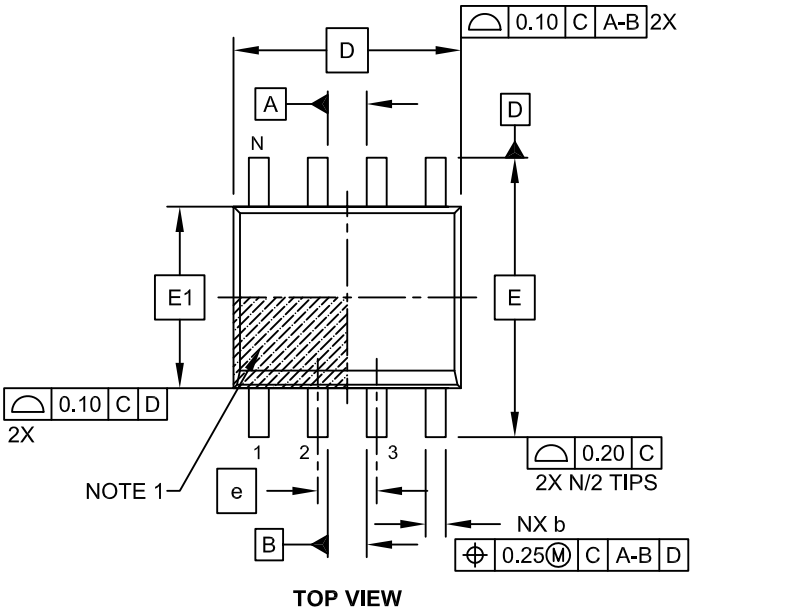
T = Temperature grade
NN = Alphanumeric traceability code

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

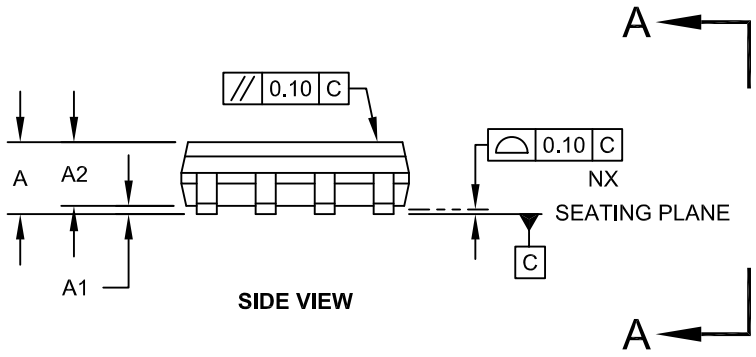
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

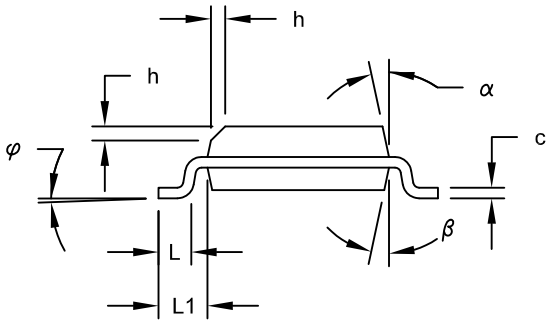
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

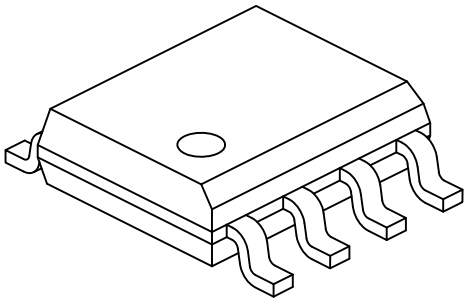


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

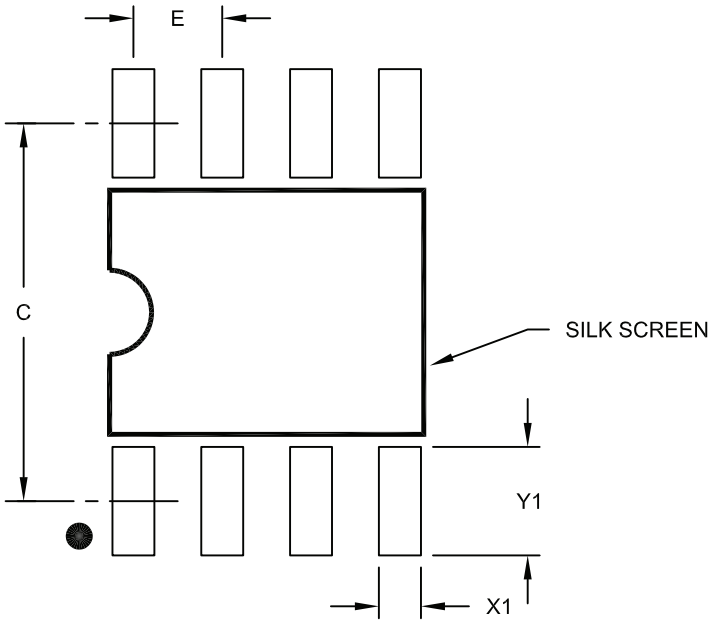
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

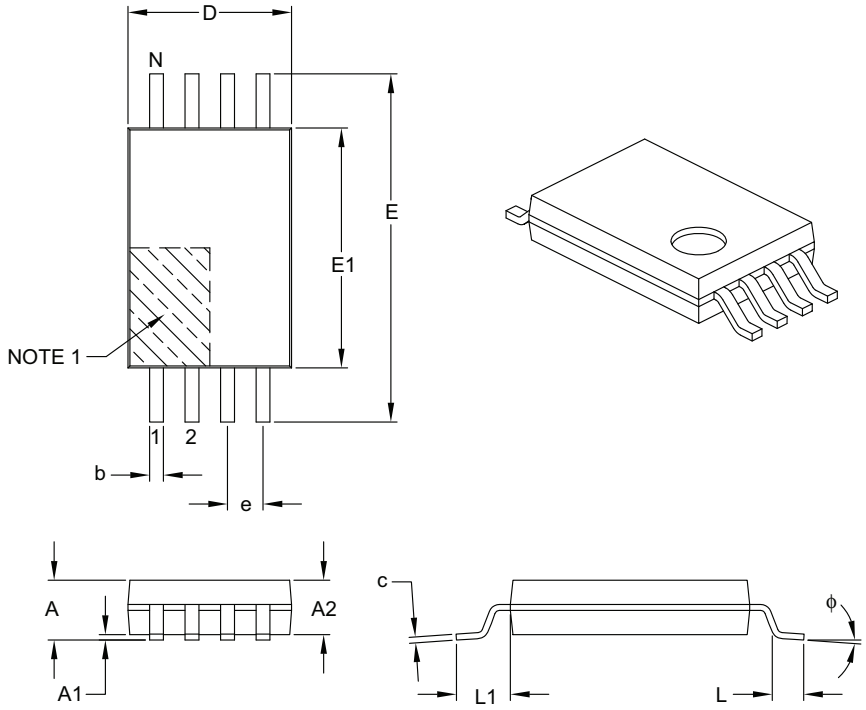
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

Notes:

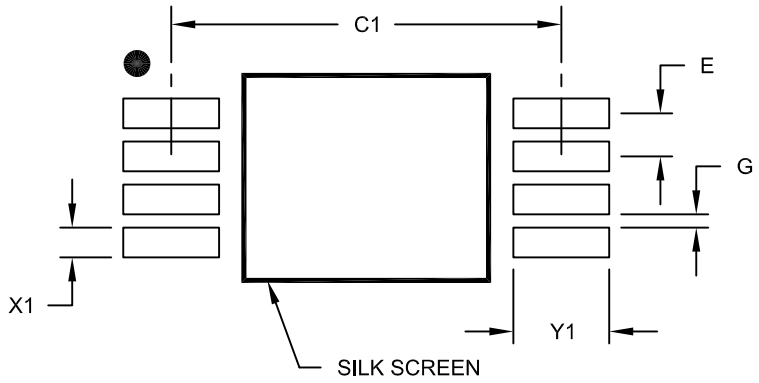
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

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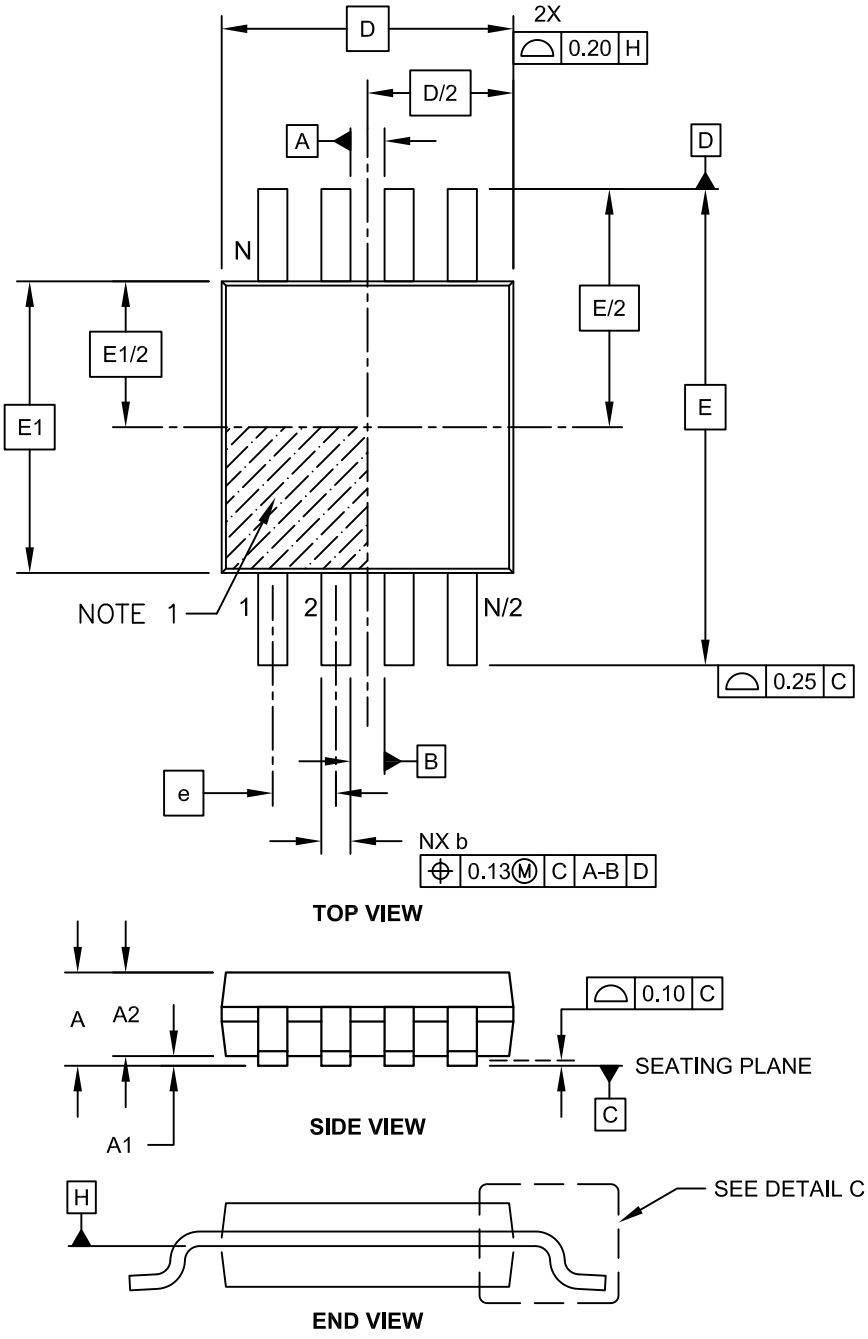
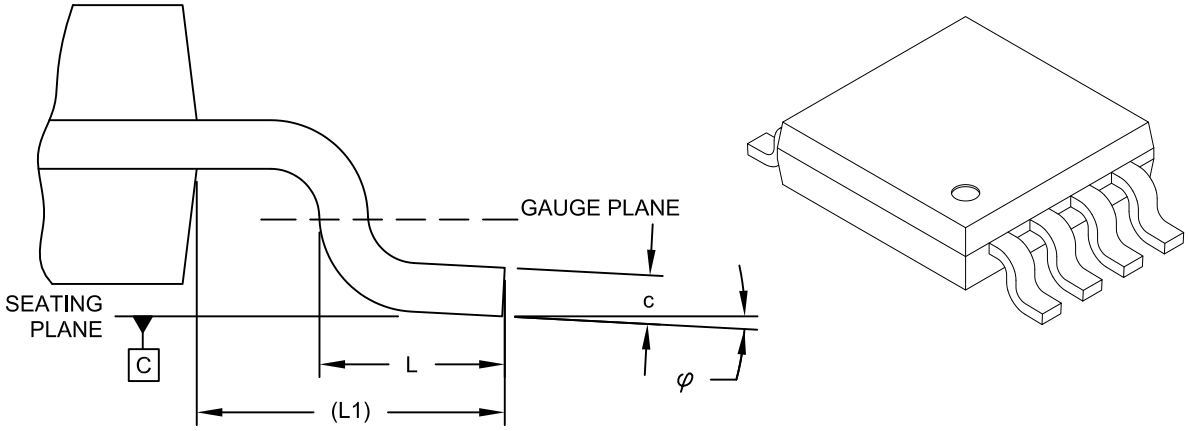


Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

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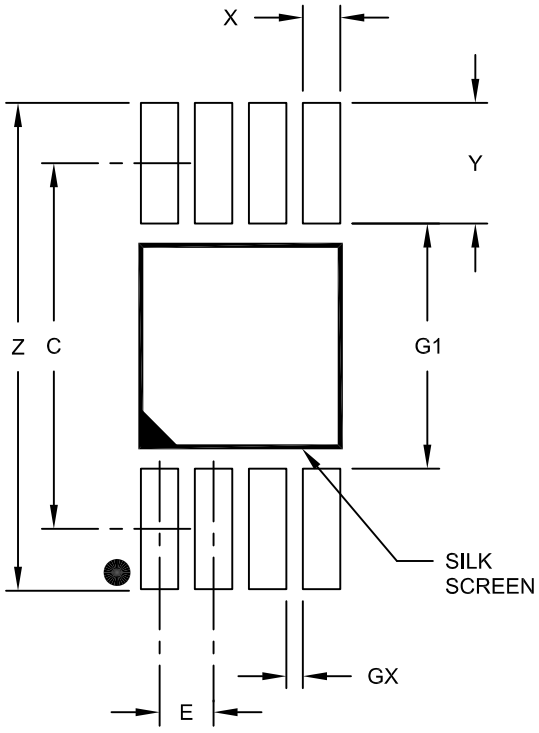

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

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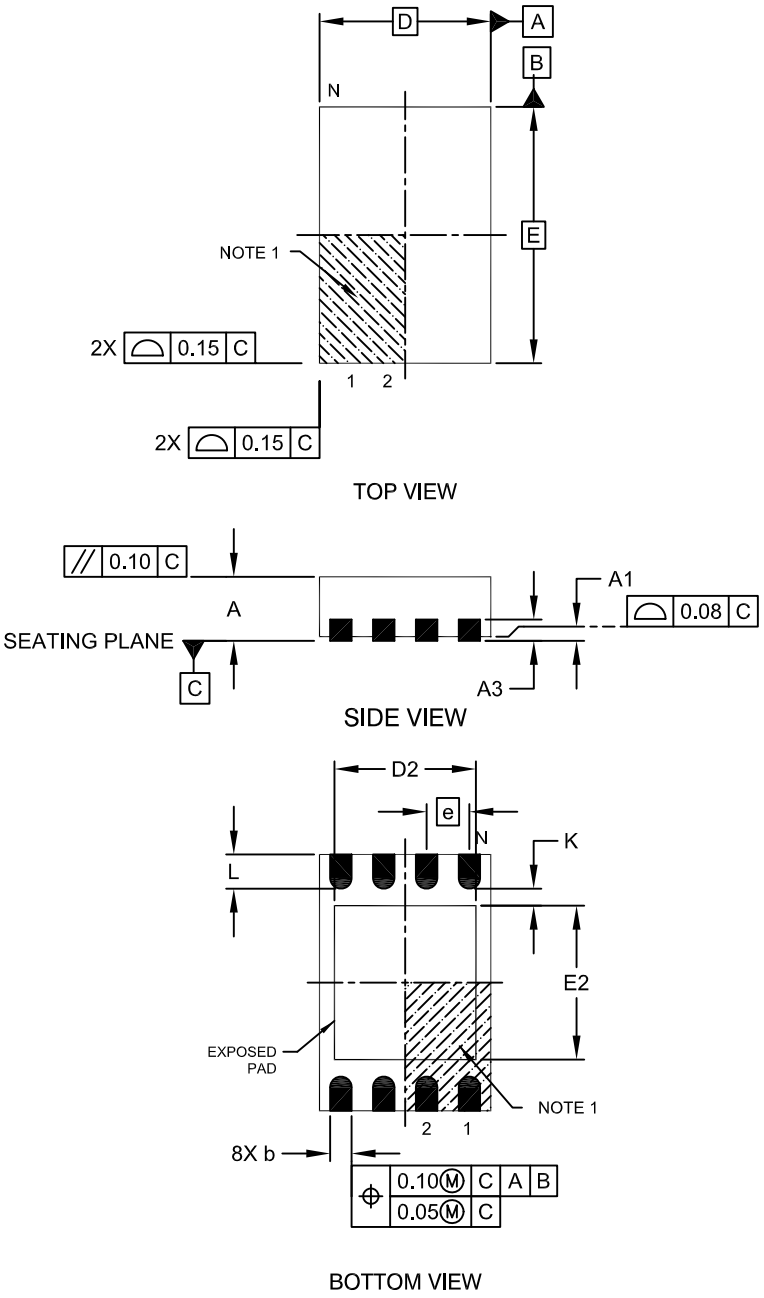

Microchip Technology Drawing No. C04-129C

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75mm Body [TDFN]

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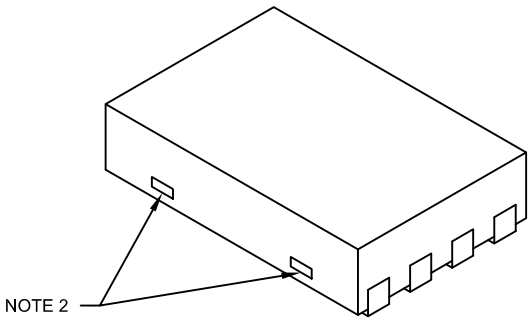


Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.50 BSC	
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		2.00 BSC	
Overall Width	E		3.00 BSC	
Exposed Pad Length	D2	1.20	-	1.60
Exposed Pad Width	E2	1.20	-	1.60
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

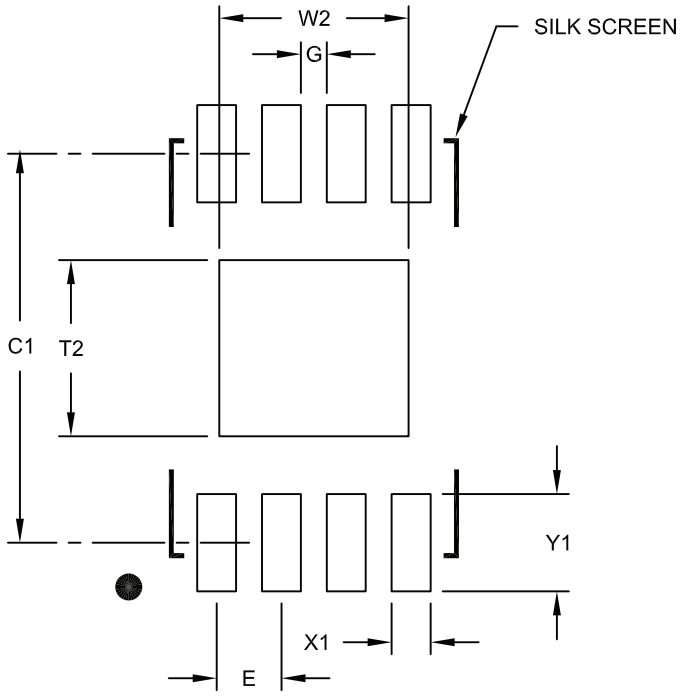
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129C Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.75 mm Body [TDFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			1.46
Optional Center Pad Length	T2			1.36
Contact Pad Spacing	C1		3.00	
Contact Pad Width (X8)	X1			0.30
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2129A

APPENDIX A: REVISION HISTORY

Revision A (10/2010)

Original release of this document.

Revision B (03/2011)

Minor typographical edits;

Added Appendix B: Device Errata

Revision C (07/2011)

Updated Section 4.2.6, Crystal Specs; Revised Figure 4-4.

Revision D (12/2011)

Added DC/AC Char. Charts

Revision E (04/2013)

Revised Features page; Revised Schematic, Block Diagram; Added detailed descriptions for Registers.

Minor updates to the overall content.

APPENDIX B: DEVICE ERRATA

Devices with silicon revision prior to A4 (date code prior to 11/10) have an errata where the AM/PM bit (Bit 5 in register 02h) may be flipped if the oscillator is stopped. This is coincident with the OSCON bit getting cleared.

This can occur due to the following conditions:

- The oscillator is stopped on the application.
- The oscillator is stopped by clearing the ST bit (Bit 7 in register 00h).
- The external CMOS source is stopped in EXTOSC mode.

The work-around is to determine when the OSCON bit is cleared and check in software for AM/PM bit corruption.

Devices with silicon revision A4 or later (date code after 11/09) do not have this issue.

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Device	Temperature Range	Package

Device:	MCP79410	=	1.8V - 5.5V I²C™ Serial RTCC
	MCP79410T	=	1.8V - 5.5V I²C Serial RTCC (Tape and Reel)
	MCP79411	=	1.8V - 5.5V I²C Serial RTCC, EUI-48™
	MCP79411T	=	1.8V - 5.5V I²C Serial RTCC, EUI-48™ (Tape and Reel)
	MCP79412	=	1.8V - 5.5V I²C Serial RTCC, EUI-64™
	MCP79412T	=	1.8V - 5.5V I²C Serial RTCC, EUI-64™ (Tape and Reel)
Temperature Range:	I	=	-40°C to +85°C
Package:	SN	=	8-Lead Plastic Small Outline (3.90 mm body)
	ST	=	8-Lead Plastic Thin Shrink Small Outline (4.4 mm)
	MS	=	8-Lead Plastic Micro Small Outline
	MNY(1)	=	8-Lead Plastic Dual Flat, No Lead

Note 1: "Y" indicates a Nickel Palladium Gold (NiPdAu) finish.

Examples:

a) MCP79410-I/SN: Industrial Temperature, SOIC package.

b) MCP79410T-I/SN: Industrial Temperature, SOIC package, Tape and Reel.

c) MCP79410T-I/MNY: Industrial Temperature, TDFN package, Tape and Reel.

d) MCP79411-I/SN: Industrial Temperature, SOIC package, EUI-48™.

e) MCP79411-I/MS: Industrial Temperature MSOP package, EUI-48™.

f) MCP79412-I/SN: Industrial Temperature, SOIC package, EUI-64™.

g) MCP79412-I/ST: Industrial Temperature, TSSOP package, EUI-64™.

h) MCP79412T-I/ST: Industrial Temperature, TSSOP package, Tape and Reel, EUI-64™.

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- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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