

3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

General Description

The MAX4271/MAX4272/MAX4273 comprise a complete family of integrated 3V to 12V hot-swap controllers. They allow the safe insertion and removal of circuit cards into live backplanes.

The discharged filter capacitors of the circuit card provide a low impedance to the live backplane. High in-rush currents from the backplane to the circuit card can burn up connectors and components, or momentarily collapse the backplane power supply leading to a system reset. This family of hot-swap controllers prevents such problems by regulating the current to a preset limit when the board is plugged in, allowing the system to stabilize safely. After the startup cycle is completed, two on-chip comparators provide DualSpeed/BiLevel™ protection against short circuits, load glitches, and overcurrent conditions. In the event of a fault condition, the load is disconnected. Fault recovery is handled by unlatching (MAX4271), autoretry (MAX4272), or programmed (MAX4273) methods.

The MAX4271 family includes many integrated features that reduce component count and design time. An on-board charge pump provides the gate drive for a low-cost, external n-FET. Integrated features like startup current regulation and current glitch protection eliminate external timing resistors and capacitors. Also featured are an open-drain status output to indicate a fault condition, and an adjustable overcurrent response time.

The MAX4271 (latched fault protection) and MAX4272 (autoretry fault protection) come in 8-pin SO packages. The MAX4273 (full function) comes in the space-saving 16-pin QSOP package and 16-pin SO package. All parts are specified across the extended temperature range, and have an absolute maximum rating of 15V to provide extra protection against inductive kickback during board removal.

DualSpeed/BiLevel is a trademark of Maxim Integrated Products.

Features

- ◆ Provide Safe Hot Swap for +3V to +12V Power Supplies with Few External Components
- ◆ Unique Current Regulation Architecture Minimizes n-FET Linear Mode Duration
- ◆ Autoretry Feature (MAX4272/MAX4273)
- ◆ DualSpeed/BiLevel Current Limit Protects Against Current Glitches and Short Circuits
- ◆ Power-On RESET (MAX4273)
- ◆ 15V Absolute Maximum Rating Protects Against Inductive Kickbacks During Board Removal
- ◆ Internal Charge Pump Generates Gate Drive for External n-MOSFET
- ◆ Status Output Pin Indicates Fault/Safe Condition
- ◆ Space-Saving 8-Pin SO, 16-Pin QSOP Packages

Applications

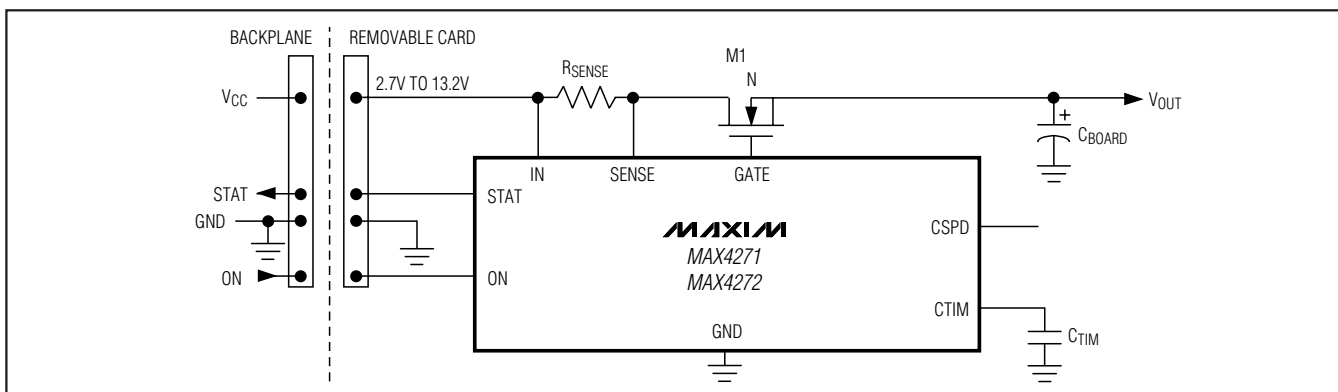
| | |
|-----------------------|---------------------|
| Base Stations | Network Routers and |
| RAID | Switches |
| Remote-Access Servers | ISDN |

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|------------|----------------|-------------|----------|
| MAX4271ESA | -40°C to +85°C | 8 SO | S8-1 |
| MAX4272ESA | -40°C to +85°C | 8 SO | S8-1 |
| MAX4273EEE | -40°C to +85°C | 16 QSOP | E16-1 |
| MAX4273ESE | -40°C to +85°C | 16 SO | E16-1 |

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

ABSOLUTE MAXIMUM RATINGS

| | |
|--|---|
| IN to GND | +15V |
| STAT, OUTC, LLMON, AUXVCC to GND | -0.3V to +14V |
| GATE to GND | -0.3V to ($V_{IN} + 8.5V$) |
| GATE to LLMON (Note 1) | -1V to +8.5V |
| INC, ON to GND (Note 2) | -1V to +14V |
| CEXT to GND | -8.5V to ($V_{IN} + 0.3V$) |
| CSPD, CTON, REF to GND | -0.3V to the lower of ($V_{IN} + 0.3V$) or +12V |
| VSENSE, RTH, CTIM to GND | -0.3V to ($V_{IN} + 0.3V$) |

| | |
|--|-----------------------------------|
| Current into INC, ON (Note 2) | $\pm 2mA$ |
| Current into Any Other Pin | $\pm 50mA$ |
| Continuous Power Dissipation ($T_A = +70^\circ C$) | |
| 8-Pin SO (derate 5.9mW/ $^\circ C$ above +70 $^\circ C$) | 471mW |
| 16-Pin QSOP (derate 8.3mW/ $^\circ C$ above +70 $^\circ C$) | 667mW |
| 16-Pin SO (derate 8.7mW/ $^\circ C$ above +70 $^\circ C$) | 696mW |
| Operating Temperature Range | -40 $^\circ C$ to +85 $^\circ C$ |
| Storage Temperature Range | -65 $^\circ C$ to +150 $^\circ C$ |
| Lead Temperature (soldering, 10s) | +300 $^\circ C$ |

Note 1: GATE can be pulled below LLMON, but current must be limited to 2mA.

Note 2: INC and ON can be pulled below ground. Limiting the current to 2mA ensures that these pins are never lower than about -0.8V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{IN} = +2.7V$ to +13.2V, $T_A = -40^\circ C$ to +85 $^\circ C$, unless otherwise noted. Typical values are at $V_{IN} = +5V$ and $T_A = +25^\circ C$.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS | |
|-------------------------------|---------------|---|---------------------------------|------------------------------|------|------|---------|----|
| POWER SUPPLIES | | | | | | | | |
| Input Voltage Range | V_{IN} | | | 2.7 | | 13.2 | V | |
| Supply Current | I_Q | $V_{ON} = V_{IN}$ | | | 0.6 | 1 | mA | |
| CURRENT CONTROL | | | | | | | | |
| Slow Comparator Threshold | $V_{SC,TH}$ | $V_{IN} - V_{SENSE}$ | $T_A = +25^\circ C$ | 45 | 50 | 55 | mV | |
| | | | $T_A = T_{MIN}$ to T_{MAX} | 43.5 | | 56 | | |
| Slow Comparator Response Time | t_{CSPD} | CSPD = floating | | 10 | 20 | 40 | μs | |
| | | CSPD = 100nF to GND | | 10 | 20 | 40 | ms | |
| Fast Comparator Threshold | $V_{FC,TH}$ | MAX4273 only | 5k Ω on RTH to V_{IN} | $T_A = +25^\circ C$ | 45 | 50 | 55 | mV |
| | | | 75k Ω on RTH to V_{IN} | $T_A = T_{MIN}$ to T_{MAX} | 43.5 | | 56 | |
| | | | | $T_A = +25^\circ C$ | 675 | 750 | 825 | |
| | | | $T_A = T_{MIN}$ to T_{MAX} | 650 | | 840 | | |
| | | RTH = GND | | 180 | 200 | 220 | | |
| | | MAX4271/MAX4272 | | | | | | |
| Fast Comparator Response Time | t_{FCD} | 10mV overdrive, from overload condition to gate discharging | | | 350 | | ns | |
| SENSE Input Bias Current | $I_{B,SENSE}$ | $V_{SENSE} = V_{IN}$ | | | 0.2 | 10 | μA | |
| MOSFET DRIVER | | | | | | | | |
| Startup Period (Notes 4, 5) | t_{START} | MAX4271/MAX4272 $C_{TIM} = 100nF$ | | 21 | 31 | 41 | ms | |
| | | MAX4273 $C_{TON} = 100nF$ | | 21 | 31 | 41 | | |
| | | No capacitor | | | 5.5 | | μs | |
| Gate Charge Current | I_{GATE} | GATE = IN (Note 6) | | | 100 | | μA | |

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MAX4271/MAX4272/MAX4273

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = +2.7V$ to $+13.2V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{IN} = +5V$ and $T_A = +25^{\circ}C$.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|------------------------|---|--------------------|-----|---------|-----------|
| Slow Turn-Off Time | $t_{SLOW,OFF}$ | Time from trigger to $V_{GATE} < 0.1V$ (triggered by either the ON input or the slow comparator), $C_{GATE} = 1000pF$ to GND | | 60 | | μs |
| Fast Turn-Off Time | $t_{FAST,OFF}$ | Time from current overload to $V_{GATE} < 0.1V$ (triggered by the fast comparator, during normal operation), $C_{GATE} = 1000pF$ to GND | | 15 | | μs |
| Maximum Gate Protection Voltage | | Voltage at which internal zener clamp circuitry is triggered, measured with respect to V_{IN} (MAX4271/MAX4272), measured with respect to V_{LLMON} (MAX4273) | | 6.7 | 7.5 | V |
| Minimum Gate Drive Voltage | | Measured with respect to V_{IN} , $I_{GATE} = 8.5\mu A$ | $V_{IN} \geq 5V$ | 5 | | V |
| | | | $V_{IN} \geq 2.7V$ | 2.7 | | |
| Gate Discharge Current | $I_{GATE,DIS}$ | During fast discharge, due to a fast comparator fault in normal operation | 0.4 | 1 | 2.75 | mA |
| | | During startup (current regulation provided by fast comparator) | 25 | 70 | 195 | |
| | | During normal discharge, due to a slow comparator fault in normal mode, or by ON going low | 75 | 200 | 550 | μA |
| LLMON Overvoltage Threshold | | Startup is initiated only after V_{LLMON} is less than this voltage (MAX4273) | 0.1 | | | V |
| GATE Overvoltage Threshold | | Startup is initiated only after V_{GATE} is less than this voltage | 0.1 | | 0.6 | V |
| LLMON Impedance | | Impedance to GND, after a fault (MAX4273) | | 1 | | $k\Omega$ |
| REFERENCE (MAX4273) | | | | | | |
| Output Voltage | V_{REF} | No load, $V_{IN} = 5V$ | 1.164 | 1.2 | 1.236 | V |
| Line Regulation | $\Delta V_{REF, LINE}$ | $2.7V \leq V_{IN} \leq 13.2V$, no load | | 1 | 8 | mV |
| Load Regulation | $\Delta V_{REF, LOAD}$ | $I_{REF} = 0$ to $100\mu A$, $V_{IN} = 5V$ | | 0.6 | 3 | mV |
| ON AND RESET COMPARATORS | | | | | | |
| Threshold Voltage | | $V_{IN} = 5V$, rising threshold at ON or INC | 0.575 | 0.6 | 0.625 | V |
| Hysteresis | V_{HYST} | | | 3 | | mV |
| Power-Supply Rejection Ratio | PSRR | $2.7V \leq V_{IN} \leq 13.2V$ | | | ± 1 | mV/V |
| Propagation Delay | $t_{D,COMP}$ | 10mV overdrive, ON going positive or negative, INC going negative | | 10 | | μs |
| | | INC going positive | 100 | 150 | 200 | ms |

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = +2.7V$ to $+13.2V$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $V_{IN} = +5V$ and $T_A = +25^{\circ}C$.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------|---|------|-------|------|---------|
| Input Voltage Range | | Input can be driven to the absolute maximum limit without false output inversion | -0.1 | | 13.2 | V |
| Input Bias Current | $I_{B,COMP}$ | | | 0.001 | 1 | μA |
| ON Pulse Width Low (Note 7) | $t_{RESTART}$ | To unlatch a fault MAX4271, MAX4273 with $C_{TIM} = IN$ | 20 | | | μs |
| DIGITAL OUTPUTS (STAT, OUTC) | | | | | | |
| Output Leakage Current | | $V_{STAT} \leq 13.2$, $V_{OUTC} \leq 13.2$ | | | 1 | μA |
| Output Voltage Low | V_{OL} | $I_{SINK} = 1mA$ | | | 0.4 | V |
| RETRY TIMING (MAX4272, MAX4273) | | | | | | |
| Retry Timeout Period | t_{RETRY} | 100nF capacitor on C_{TIM} (Note 5) | 0.5 | 1 | 2 | s |
| Default Retry Timeout Period | t_{RETRY} (default) | $C_{TIM} =$ no connection | | 176 | | μs |
| UNDERVOLTAGE LOCKOUT (UVLO) | | | | | | |
| Threshold | V_{UVLO} | Startup is initiated when this threshold is exceeded at IN | 2.25 | | 2.67 | V |
| Hysteresis | $V_{UVLO,HYST}$ | | | 100 | | mV |
| Delay | $t_{D,UVLO}$ | Time the input voltage must exceed undervoltage lockout before startup is initiated | 100 | 150 | 200 | ms |

Note 3: All devices are 100% tested at $T_A = +25^{\circ}C$. All temperature limits are guaranteed by design.

Note 4: Startup period is the time during which the slow comparator is ignored and the fast comparator regulates the sense current. It is measured from the time ON is brought high.

Note 5: Inferred from test with $C_{TON} = 10nF$ (MAX4273) and $C_{TIM} = 1nF$.

Note 6: The current available at GATE is a function of V_{GATE} (see *Typical Operating Characteristics*).

Note 7: Guaranteed by design.

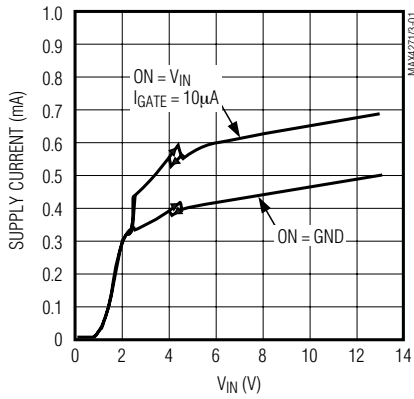
3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

Typical Operating Characteristics

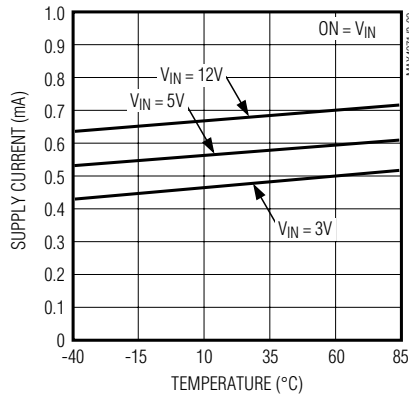
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MAX4271/MAX4272/MAX4273

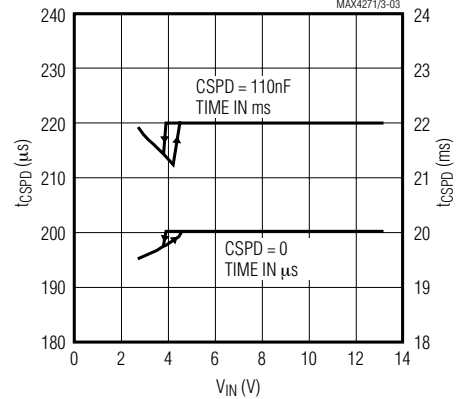
SUPPLY CURRENT vs. INPUT VOLTAGE



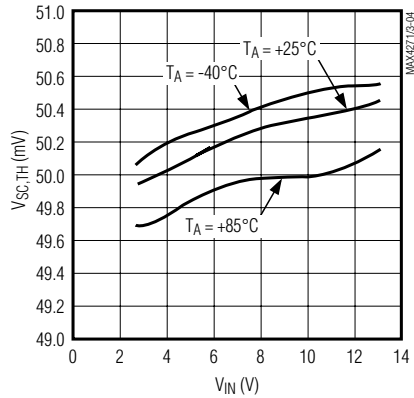
SUPPLY CURRENT vs. TEMPERATURE



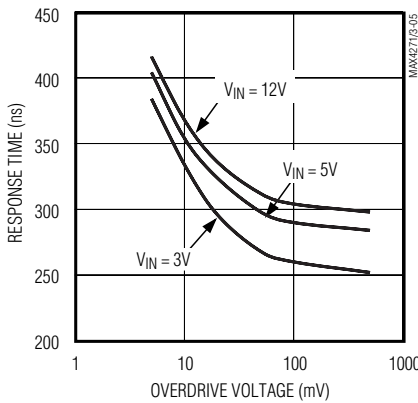
SLOW COMPARATOR RESPONSE TIME vs. INPUT VOLTAGE



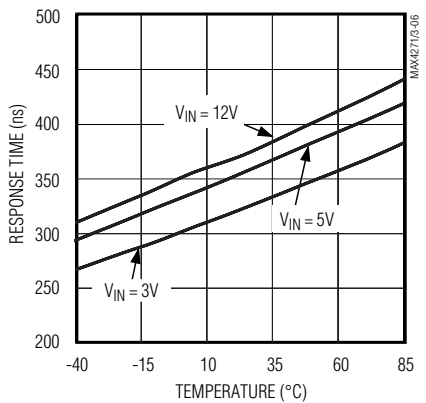
SLOW COMPARATOR THRESHOLD vs. INPUT VOLTAGE



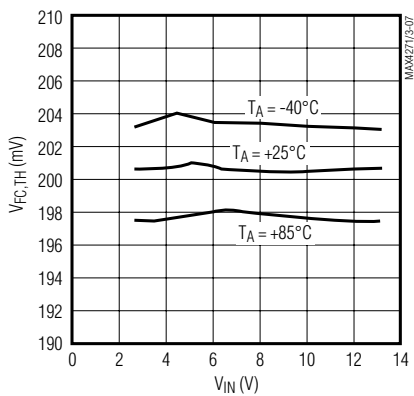
FAST COMPARATOR RESPONSE TIME vs. OVERDRIVE VOLTAGE



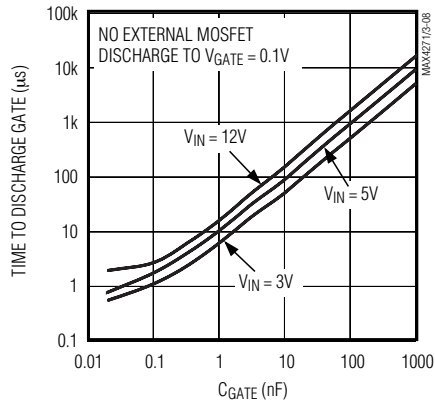
FAST COMPARATOR RESPONSE TIME vs. TEMPERATURE



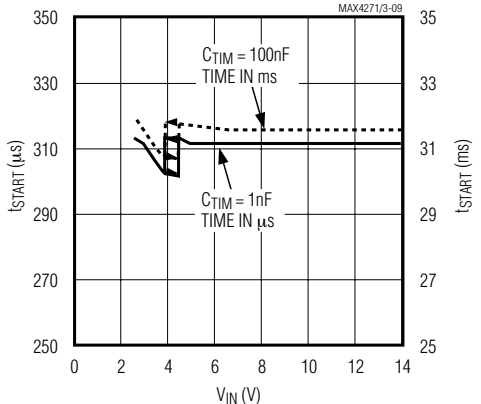
FAST COMPARATOR THRESHOLD vs. INPUT VOLTAGE



TIME TO DISCHARGE GATE vs. CGATE



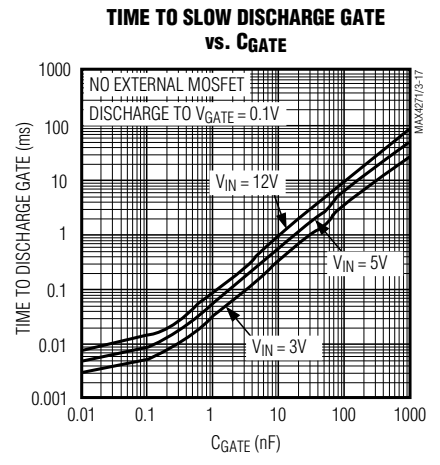
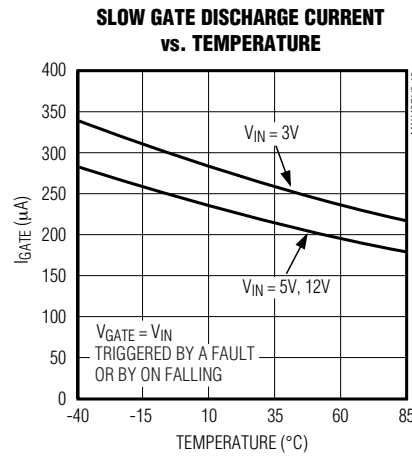
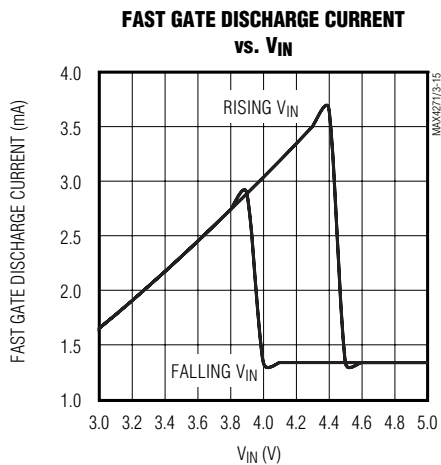
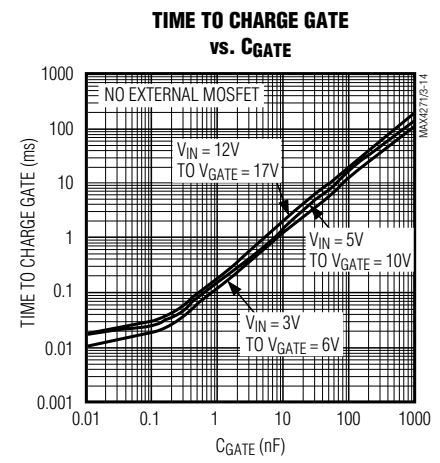
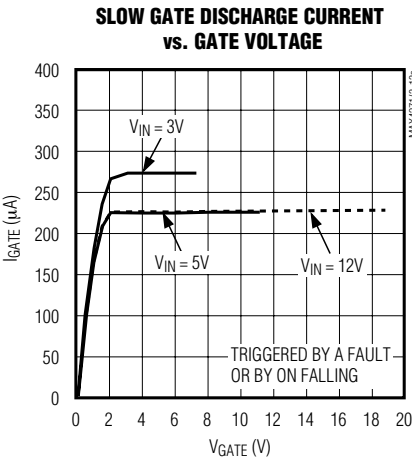
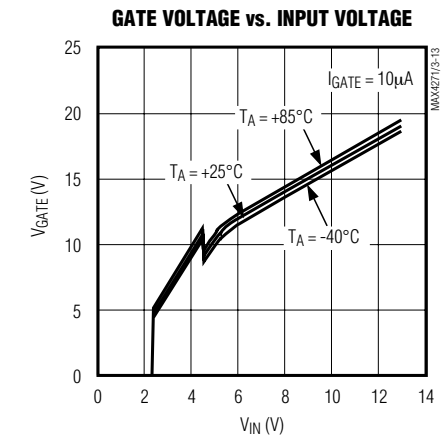
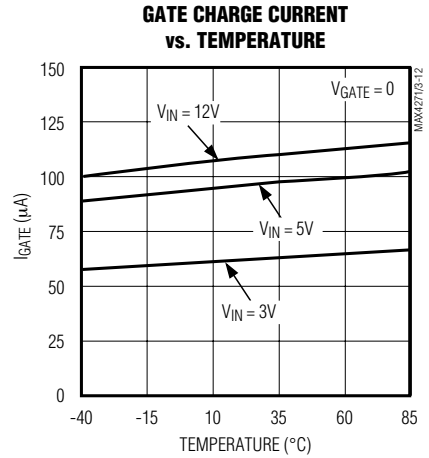
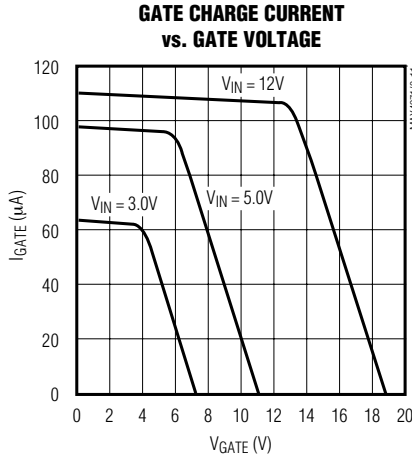
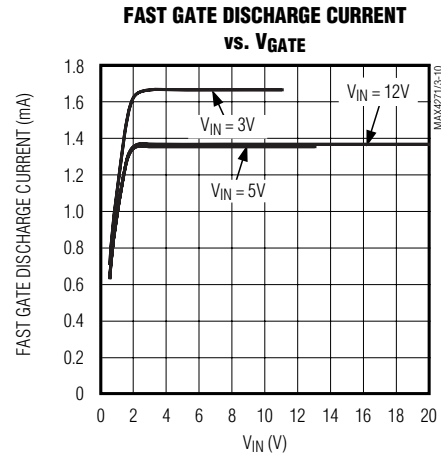
STARTUP PERIOD vs. INPUT VOLTAGE



3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

Typical Operating Characteristics (continued)

($V_{IN} = 5V$, $R_{SENSE} = 100m\Omega$, $C_{BOARD} = 47\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

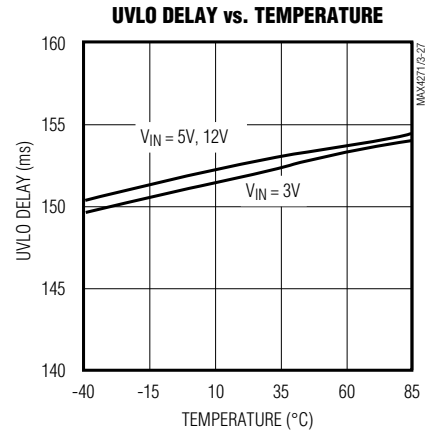
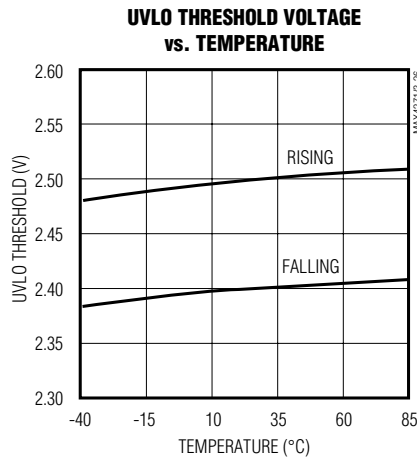
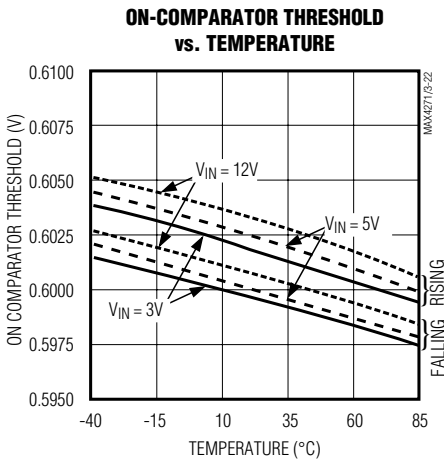
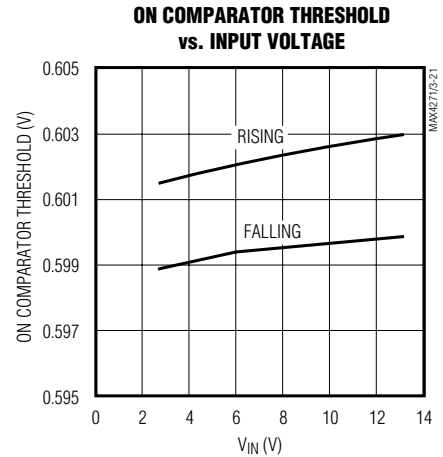
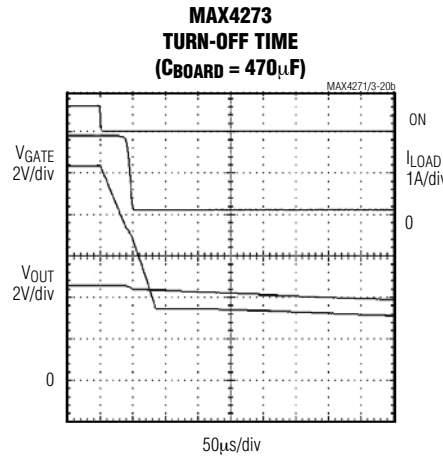
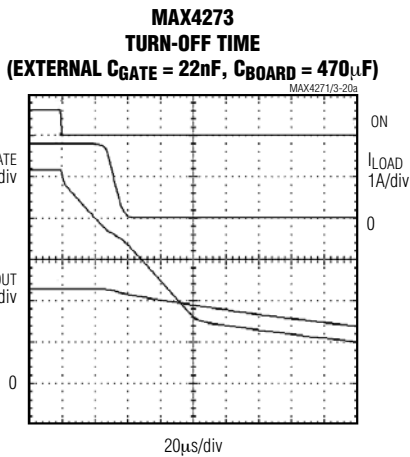
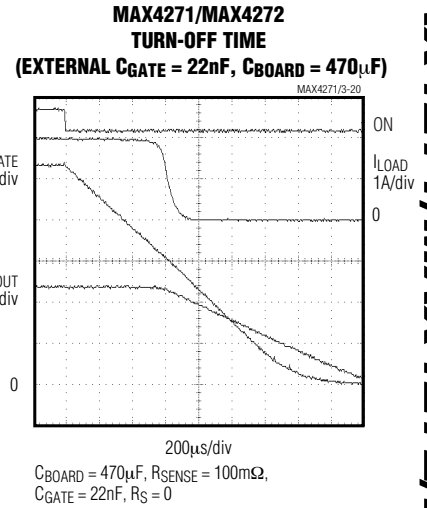
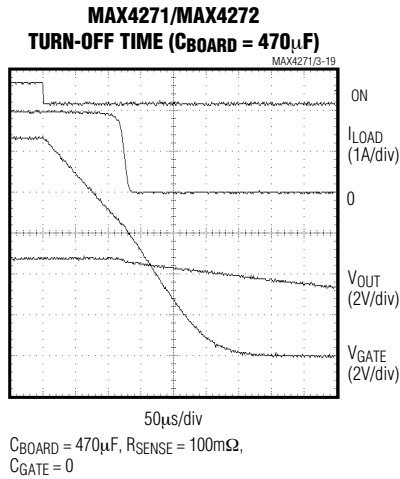
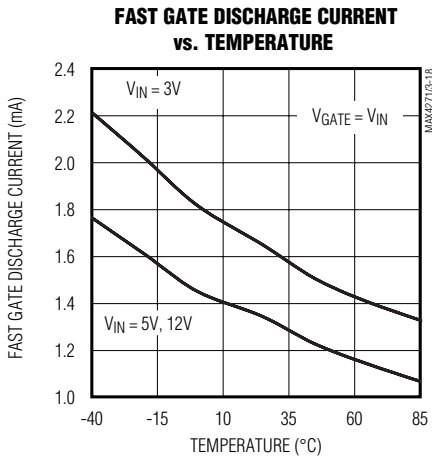


3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

Typical Operating Characteristics (continued)

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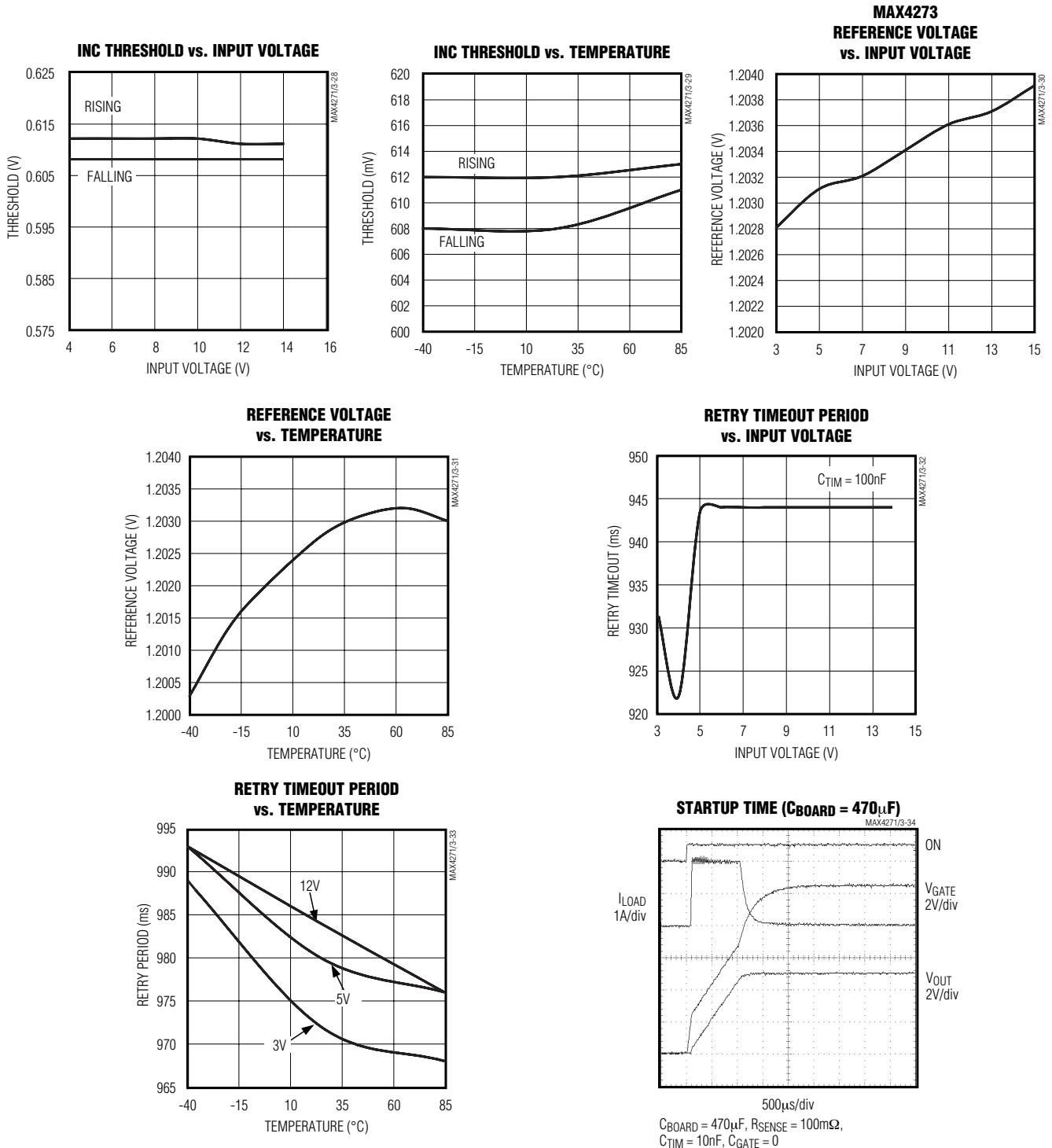
MAX4271/MAX4272/MAX4273



3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

Typical Operating Characteristics (continued)

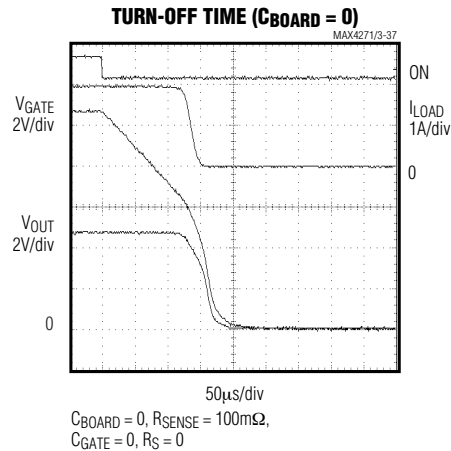
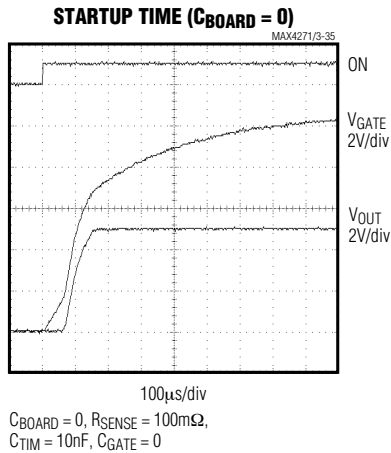
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3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

Typical Operating Characteristics (continued)

($V_{IN} = 5V$, $R_{SENSE} = 100m\Omega$, $C_{BOARD} = 47\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

| PIN | | | FUNCTION |
|--------------------|---------|--------|--|
| MAX4271 MAX4272 | MAX4273 | NAME | |
| — | 1 | RTH | Current-Sense Threshold Setting Input. Connect a resistor from RTH to V_{IN} to set the fast comparator threshold. Bypass to V_{IN} with 0.1µF. Connect RTH to V_{IN} to disable both the fast comparator and current regulation at startup. Short RTH to GND for a 200mV threshold. See <i>Fast Comparator Threshold</i> section. |
| — | 2 | AUXVCC | Auxiliary Supply Input. Supply input for short-circuit switchover. To use this, connect a 1µF capacitor from AUXVCC to GND; otherwise, leave floating. See <i>Auxiliary VCC</i> section. |
| 1 | 3 | IN | Input Voltage. Connect to +2.7V to +13.2V supply; 15V absolute maximum voltage rating. |
| 2 | 4 | SENSE | Current-Sense Resistor Voltage Input. R_{SENSE} is connected from IN to SENSE. |
| 3 | 5 | GATE | Gate Drive Output. Connect to gate of external N-channel pass transistor. |
| — | 6 | CEXT | External Gate Capacitance Connection. Connect a capacitor from CEXT to GATE to increase the gate charging time. This pin goes high impedance during a fast comparator fault for fast discharge. |
| — | 7 | LLMON | Load Line Monitor. Connect to the source of the external N-channel MOSFET. The external FET is turned on only when the load voltage is less than 100mV. |
| 4 | 8 | GND | Ground |
| — | 9 | CTON | Startup Timer Input. Leave floating or connect the timing capacitor from CTON to GND. See <i>Startup and Retry Timers</i> section. |
| 5 | 10 | CSPD | Slow Comparator Speed Setting. Leave floating or connect the timing capacitor from CSPD to GND. See <i>Slow Comparator Response Time</i> section. |

3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

Pin Description (continued)

| PIN | | | FUNCTION |
|--------------------|---------|------|---|
| MAX4271 MAX4272 | MAX4273 | NAME | |
| 6 | 11 | CTIM | Startup and Retry Timers Input. Controls the startup time and the autoretry time (32x startup time) in the MAX4272, only the autoretry time in the MAX4273, and only the startup time in the MAX4271. Leave floating or connect the timing capacitor from CTIM to GND. Connect to IN for latched mode (this prevents autoretry in MAX4273). See <i>Startup and Retry Timers</i> section. |
| 7 | 12 | STAT | Status Output. High indicates startup completed with no fault (Table 1). STAT is an open-drain output. |
| 8 | 13 | ON | ON Comparator Input. Connect high for normal operation; connect low to force the MOSFET off. Comparator threshold $V_{TH,ON} = 0.6V$ allows for precise control over shutdown feature. Pulse ON low for 20 μ s min to unlatch after a fault (MAX4273 in latched mode, or MAX4271). Negative pulses are ignored during autoretry (MAX4273 in autoretry mode, or MAX4272). See <i>ON and Reset Comparators</i> section. |
| — | 14 | REF | 1.2V Reference Output. Do not bypass with a capacitor to GND. |
| — | 15 | INC | Uncommitted Comparator Input. Controls OUTC. |
| — | 16 | OUTC | Uncommitted Comparator Output. OUTC goes high 150ms after INC goes high. OUTC goes low immediately after INC goes low. OUTC is an open-drain output. |

Detailed Description

The MAX4271/MAX4272/MAX4273 are circuit breaker ICs designed for hot-swap applications where a line card is inserted into a live backplane. Normally, when a line card is plugged into a live backplane, the card's discharged filter capacitors provide a low impedance that can momentarily cause the main power supply to collapse. The MAX4271/MAX4272/MAX4273 are designed to reside either in the backplane or in the removable card to provide inrush current limiting and short-circuit protection. This is achieved by using an external N-channel MOSFET, an external current-sense resistor, and two on-chip comparators. Figures 1 and 2 show the functional diagrams.

The timing and voltage levels for several critical parameters can be adjusted with external resistors, external capacitors, or by pin strapping. The timing components are optional; without them, the part is set to its nominal values, as shown in the *Electrical Characteristics*. The parameters that can be adjusted are:

- Current-limit threshold
- Slow comparator response time
- Startup timer
- Fast comparator threshold

- Autoretry timeout period (time the part is shut down after an overcurrent event)
- Fault management (latched/autoretry)
- Current overload threshold

Startup Mode

CTIM (MAX4271/MAX4272) or CTON (MAX4273) sets the startup period (see *Startup and Retry Timers*). The startup period begins after three conditions are met:

- 1) 150ms after V_{IN} exceeds the UVLO threshold (see *Over/Undervoltage Lockouts*)

AND

- 2) 10 μ s after $V_{ON} > 0.6V$

AND

- 3) The device is no longer in retry mode.

During startup, the slow comparator is disabled and the inrush current can be limited in two ways:

- 1) Slow ramping of the current to the load by controlling the external MOSFET gate voltage

OR

- 2) Limiting the current to the load by regulating the voltage across the external current-sense resistor

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MAX4271/MAX4272/MAX4273

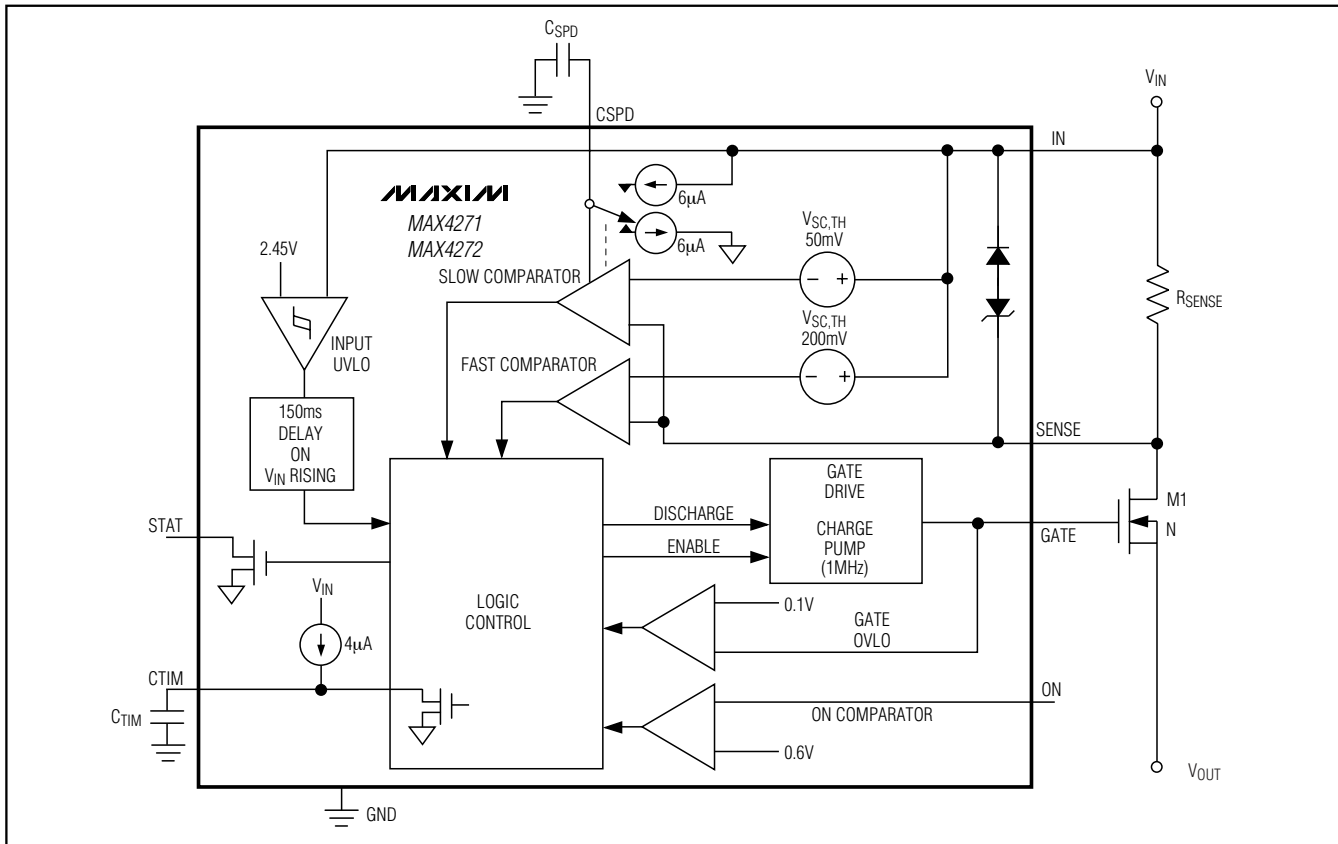


Figure 1. MAX4271/MAX4272 Functional Diagram

Unlike other circuit breaker ICs, the MAX4271/MAX4272/MAX4273 regulate the current to a preset level instead of completely turning off the external N-FET if an overcurrent condition occurs during startup.

In startup mode, the gate drive current is limited to 100 μ A and decreases with the increase of the gate voltage (see Gate Charge Current vs. Gate Voltage in the *Typical Operating Characteristics*). This allows the controller to slowly enhance the MOSFET. If the fast comparator detects an overcurrent, the gate voltage is momentarily discharged with a fixed 70 μ A current until the load current through the sense resistor (R_{SENSE}) decreases below its threshold point. This effectively regulates the inrush current during startup. Figure 3 shows the startup waveforms. STAT goes high at the end of the startup period if no fault condition is present.

Normal Operation (DualSpeed/BiLevel)

In normal operation (after the startup timer has expired), protection is provided by turning off the external MOSFET when a fault condition is encountered. DualSpeed/BiLevel fault protection incorporates two comparators with different thresholds and response times to monitor the current:

- 1) **Slow comparator.** This comparator has an externally set response time (from 20 μ s to seconds) and a fixed 50mV threshold voltage. The slow comparator ignores low-amplitude momentary current glitches. After an extended overcurrent condition, a fault is generated and the MOSFET gate is slowly discharged.
- 2) **Fast comparator.** This comparator has a fixed 350ns response time and a 200mV threshold voltage (adjustable from 50mV to 750mV in MAX4273). The fast comparator turns off the MOSFET immediately after it detects a large amplitude event such as a short circuit.

3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

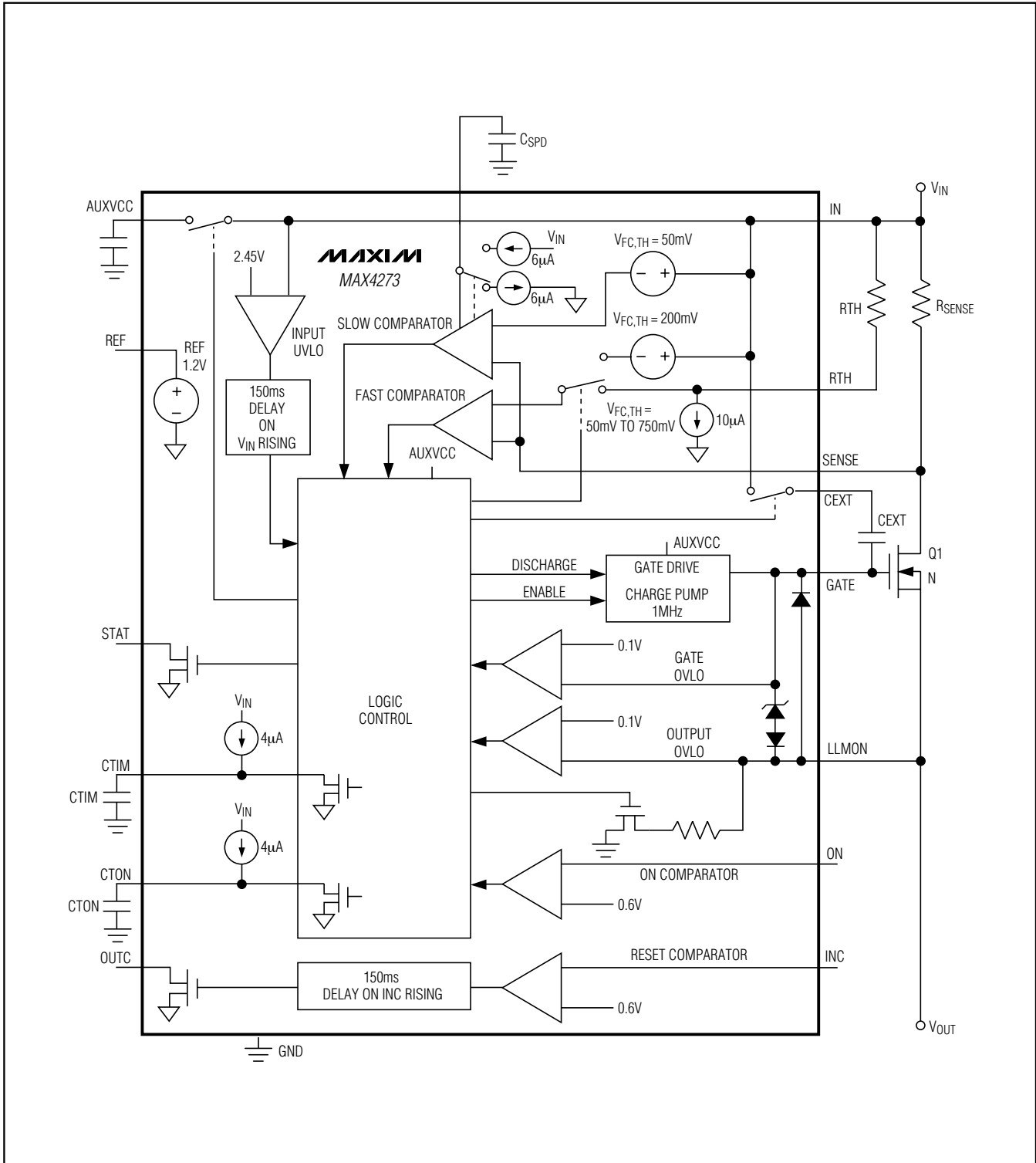


Figure 2. MAX4273 Functional Diagram

3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

In each case, when a fault is encountered, the status pin (STAT) goes low, and for the MAX4273, the device discharges the output voltage through a $1k\Omega$ resistor from LLMON to GND. After a fault, the MAX4271 stays latched off and the MAX4272 enters retry mode, while the MAX4273 has selectable latched or retry mode. Figure 4 shows the waveforms of a fault condition.

BiLevel Fault Protection

Slow Comparator

The slow comparator is disabled at startup while the external MOSFET is turning on. This allows the part to ignore the higher-than-normal inrush current charging the board capacitors when a card is first plugged in.

If the slow comparator detects an overload condition while in normal operation (after startup is completed), it turns off the external MOSFET by discharging the gate capacitance with a $200\mu A$ current. The slow comparator threshold is set at $50mV$ and has a default delay of $20\mu s$ (CSPD floating), allowing it to ignore power-supply glitches and noise. The response time can be lengthened with an external capacitor at CSPD (Figure 10).

If the overcurrent condition is not continuous, then the duration above the threshold minus the duration below must be greater than $20\mu s$ (or the external programmed value) for the device to trip. When the current is above the threshold, CSPD is charged with a $6\mu A$ current source. A fault is detected when CSPD is charged to

the trip point of $1.2V$. Therefore, a pulsing current with a duty cycle of 50% or greater (i.e., the current is above the threshold level > 50% of the time) is considered a fault condition even if it is never higher than the threshold for longer than the slow comparator's set response time.

The discharge rate depends on the N-FET gate capacitance and the external capacitance at GATE. In the MAX4273, CEXT remains connected and capacitance to this point has to be discharged by the same current. This increases the discharge time. Once the fault condition is detected, the STAT pin goes low and the device goes into retry or latched mode.

Fast Comparator

The fast comparator behaves differently according to the operating mode.

During startup, the fast comparator is part of a simple current regulator. When the sensed current is above the fast comparator threshold, the gate is discharged with a $70\mu A$ current source. When the sensed current drops below the threshold, the charge pump turns on again. The sensed current will rise and fall near the threshold due to the fast comparator and charge-pump propagation delay. The gate voltage will be roughly sawtooth shaped, and the load current will present a 20% ripple. The ripple can be reduced by adding a capacitor from GATE to GND.

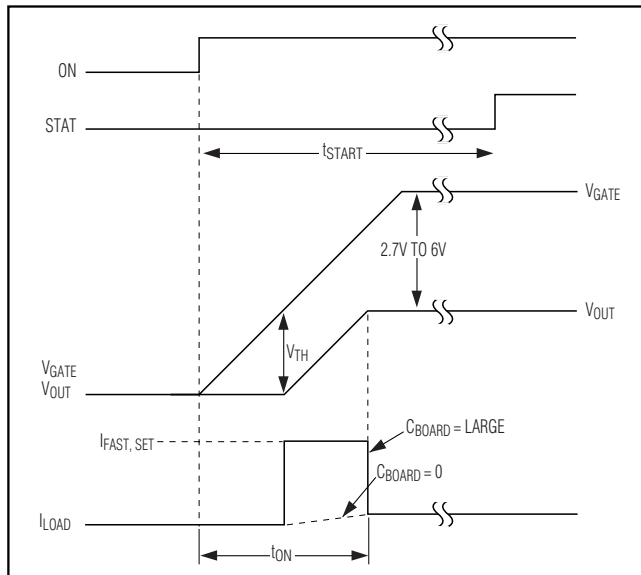


Figure 3. Startup Waveforms

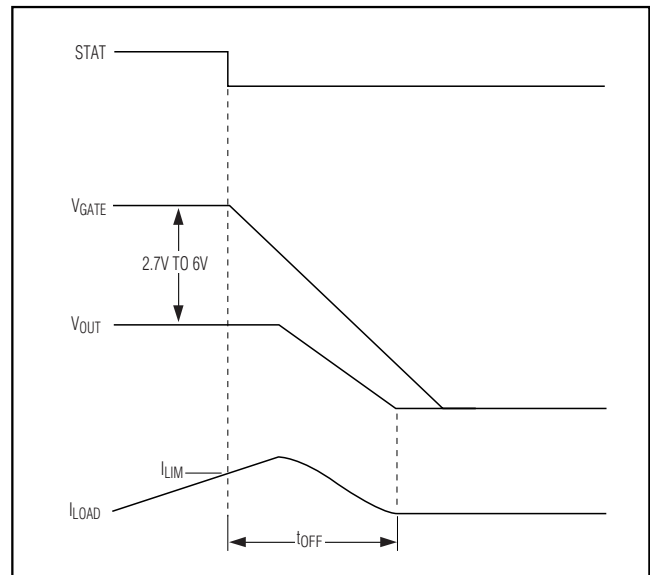


Figure 4. Response to a Fault Condition

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If the sensed current is still high after the startup timer expires, the MOSFET gate is discharged completely as described below.

In normal operation (after startup), the fast comparator is used as an emergency off switch. If the load current reaches the fast comparator threshold, the device quickly forces the MOSFET off completely. This could happen in the event of a serious current overload or a dead short. The fast comparator has a 350ns response time and discharges GATE with a 1mA current. Given a 1000pF gate capacitance and 12V gate voltage, the MOSFET will be off in about 12 μ s. Any additional capacitance connected between GATE and GND to slow down the startup time also increases the turn-off time.

In the MAX4273, CEXT goes high impedance during the fast discharge. This reduces the effective capacitance on GATE if a capacitor is used between GATE and CEXT, and allows the MOSFET to quickly turn off. In turn, this allows adjustment of the MOSFET charging time without affecting the fast discharge rate, although it does affect the slow discharge rate.

The MAX4271/MAX4272 fast comparator threshold is set to four times the slow comparator threshold (i.e., 200mV). The MAX4273 fast comparator threshold is set to 200mV by connecting RTH to GND, is disabled by connecting RTH to IN, or is adjustable by an external resistor connected to IN (see *Fast Comparator Threshold (RTH)*).

Latched/Autoretry

The MAX4271 MOSFET driver stays latched off after a fault condition until it is reset by a negative-going pulse on the ON pin. The MAX4272 is periodically turned on after a fault condition with a timeout duration set by an external timing capacitor on CTIM. The MAX4273 has a selectable latched mode or retry mode. Connect CTIM to IN to set the device in latched mode, or use an external capacitor at CTIM to set the retry timeout.

Pulse ON low for 20 μ s (min) to restart after a fault (MAX4271/MAX4273 in latched mode). Negative pulses are ignored during autoretry (MAX4273 in autoretry mode, or MAX4272).

The capacitor on CTIM affects the MAX4272's retry timeout period (time the part is shut down after an overcurrent event) and the startup time (see the *Electrical Characteristics*). The retry timeout period is fixed at 32 times the startup time in order to minimize power dissipation in the external MOSFET in case of a short-circuit condition (see *MOSFET Thermal Considerations*). This is not an issue for parts latched off during a fault condition since they stay off until commanded on. The MAX4273 configured in retry mode has a separate startup timer capacitor (CTON) and retry timeout capacitor (CTIM). This allows the user to change the ratio between startup time and retry timeout period.

Status Output

The status output is an open-drain output that goes low under the following conditions:

- During the UVLO delay period
- In startup
- Forced off (ON < 0.6V)
- In an overcurrent condition
- In the retry timeout period (or latched off, for the latched parts)

STAT is high only if the part is in normal mode and no faults are present (Table 1). Figure 5 shows the status (STAT) output timing diagram.

Over/Undervoltage Lockouts

The UVLO prevents the MAX4271/MAX4272/MAX4273 from turning on the external MOSFET until V_{IN} exceeds the lockout threshold (2.25V min) for 150ms. The UVLO protects the external MOSFET from insufficient gate drive voltage. The 150ms timeout ensures that the board is fully plugged into the backplane and that V_{IN}

Table 1. Status Output Truth Table

| IN UVLO DELAY PERIOD | PART IN STARTUP | ON PIN | OVERCURRENT CONDITION | PART IN RETRY-TIMEOUT PERIOD (OR LATCHED OFF DUE TO OVERCURRENT CONDITION) | STAT PIN (STATUS) |
|----------------------|-----------------|--------|-----------------------|--|-------------------|
| Yes | X | X | X | X | Low |
| X | Yes | X | X | X | Low |
| X | X | Low | X | X | Low |
| X | X | X | Yes | X | Low |
| X | X | X | X | Yes | Low |
| No | No | High | No | No | High |

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MAX4271/MAX4272/MAX4273

is stable. Any input voltage transient at IN below the UVLO threshold will reset the device and initiate a start-up sequence.

These devices also have an overvoltage lockout (OVLO) feature that prevents the device from restarting after a fault condition if the discharge has not been completed. VGATE has to be discharged to below 0.1V. Additionally, the MAX4273 LLMON pin discharges the load line with a 1kΩ pulldown and prevents startup until the load voltage is below 0.1V.

Since the MAX4271/MAX4272 do not monitor the output voltage, a startup sequence can be initiated while the board capacitance is still charged.

A large board capacitance or a short startup period may prevent the MAX4272 from charging completely in one startup period. The MAX4272 responds to these conditions by charging the capacitor with bursts defined by a tON duty cycle and a period of tON + tRETRY. The charging will be complete after several retries unless the resistive load or current load excessively discharges the board capacitance during the retry timeout. This feature applies to the MAX4273 if LLMON is left floating or is connected to GND. To prevent multiple charging bursts, ensure that the tON timer exceeds the minimum time required to complete the charge of the board capacitance (see *Component Selection*).

Gate Overvoltage Protection

New-generation MOSFETs have an absolute maximum rating of ±8V for the gate-to-source voltage (VGS). To protect these MOSFETs, the MAX4271/MAX4272 limit the gate-to-drain voltage (the MAX4273 limits the gate-to-source voltage) to +7.5V with an internal zener diode. No protection is provided for negative VGS (MAX4271/MAX4272). If GATE can be discharged to ground faster than the output voltage, an external small-signal protection diode (D1) can be used, as shown in Figure 6. The MAX4273 has the protection diode internal.

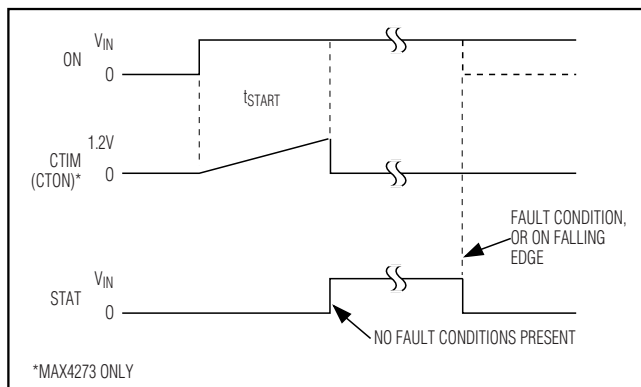


Figure 5. Status (STAT) Output Timing Diagram



Applications Information

Component Selection

N-Channel MOSFET

Select the external N-channel MOSFET according to the application's current level. Table 2 lists some recommended components. The MOSFET's on-resistance (RDS(ON)) should be chosen low enough to have a minimum voltage drop at full load to limit the MOSFET power dissipation. High RDS(ON) can cause output ripple if the board has pulsing loads or triggers an external undervoltage reset monitor at full load. Determine the device power-rating requirement to accommodate a short circuit on the board at startup with the device

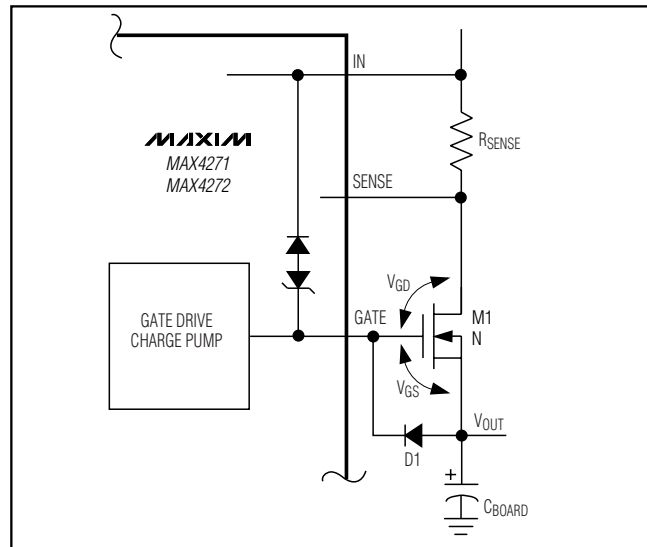


Figure 6. External Gate-Source Protection

Table 2. Recommended N-Channel MOSFETs

| PART NUMBER | MANUFACTURER | DESCRIPTION |
|-------------|-------------------------|-------------------|
| IRF7413 | International Rectifier | 11mΩ, 8 SO, 30V |
| IRF7401 | | 22mΩ, 8 SO, 20V |
| IRL3502S | | 6mΩ, D2PAK, 20V |
| MMSF3300 | Motorola | 20mΩ, 8 SO, 30V |
| MMSF5N02H | | 30mΩ, 8 SO, 20V |
| MTB60N05H | | 14mΩ, D2PAK, 50V |
| FDS6670A | Fairchild | 10mΩ, 8 SO, 30V |
| NDS8426A | | 13.5mΩ, 8 SO, 20V |
| FDB8030L | | 4.5mΩ, D2PAK, 30V |

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configured in automatic retry mode (see *MOSFET Thermal Considerations*).

Using the MAX4271/MAX4273 in latched mode allows the consideration of MOSFETs with higher $R_{DS(ON)}$ and lower power ratings. A MOSFET can typically withstand single-shot pulses with higher dissipation than the specified package rating. Low MOSFET gate capacitance is not necessary since the inrush current limiting is achieved by limiting the gate dv/dt . Table 3 lists some recommended manufacturers and components.

Sense Resistor

The slow comparator threshold voltage is set at 50mV. Select a sense resistor that causes a 50mV voltage drop at a current level above the maximum normal operating current; typically, set the overload current at 1.2 to 1.5 times the nominal load current. The fast comparator threshold is typically set at 200mV. This will set the fault current limit at four times the overload current limit. The MAX4273 fast comparator threshold can be set between 50mV and 750mV; see Table 4 for a detailed listing.

Choose the sense resistor power rating according to the device configuration. If no retry mode is selected, $P_{RSENSE} = (I_{OVERLOAD})^2 \times R_{SENSE}$; if retry is selected, then $P_{RSENSE} = (I_{FAULT})^2 \times R_{SENSE} \times (t_{ON}/t_{RETRY})$.

Fast Comparator Threshold (RTH) (MAX4273)

The fast comparator threshold is determined by the external resistor connected at RTH. To select threshold voltages between 50mV and 750mV, use resistor values between 5k Ω and 75k Ω according to Figure 7.

Resistor values between 200 Ω and 5k Ω are not recommended. Setting the threshold voltage of the fast comparator below 50mV will effectively override the slow comparator operation. The MAX4273 fast comparator can be disabled by shorting the RTH pin to V_{IN} ($V_{IN} - 25mV$ or less). Ground RTH to set the threshold to 200mV internally.

Startup and Retry Timers (CTIM, CTON)

The startup (t_{START}) and retry (t_{RETRY}) timers are determined by the capacitors connected at CTIM and CTON. The capacitor connected to CTIM has two functions for the three devices as follows:

| DEVICE | CTIM FUNCTION |
|---------|-----------------------------------|
| MAX4271 | Startup time |
| MAX4272 | Startup time and sets retry timer |
| MAX4273 | Sets retry timer |

Table 3. Component Manufacturers

| COMPONENT | MANUFACTURER | PHONE | WEB |
|-----------------|-------------------------|--------------|-----------------------|
| Sense Resistors | Dale-Vishay | 402-564-3131 | www.vishay.com |
| | IRC | 704-264-8861 | www.irctt.com |
| MOSFETS | Fairchild | 888-522-5372 | www.fairchildsemi.com |
| | International Rectifier | 310-322-3331 | www.irf.com |
| | Motorola | 602-244-3576 | www.mot-sps.com/ppd/ |

Table 4. Current Levels vs. RSENSE

| R_{SENSE} (m Ω) | PART NUMBER | OVERLOAD THRESHOLD SET BY SLOW COMPARATOR (A) | FAULT CURRENT THRESHOLD SET BY FAST COMPARATOR (A) |
|---------------------------|-----------------|---|--|
| 10 | MAX4271/MAX4272 | 5 | 20 |
| | MAX4273 | 5 | 5 to 75 |
| 50 | MAX4271/MAX4272 | 1 | 4 |
| | MAX4273 | 1 | 1 to 15 |
| 100 | MAX4271/MAX4272 | 0.5 | 2 |
| | MAX4273 | 0.5 | 0.5 to 7.5 |

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CTON determines the maximum time allowed to complete turn-on for the MAX4273. The default values for turn-on time (tON) and tRETRY are chosen by leaving these pins floating; they are 10μs and 320μs, respectively. These are also the minimum values (not controlled and dependent on stray capacitance). Longer timings are determined by the size of the capacitor according to Figure 8, and can be determined in Table 5, which lists the startup and retry timing parameters.

Set the tON timer long enough to allow for the MOSFET to be enhanced and the load capacitor to be charged completely.

There are two ways of completing the startup sequence. **Case A** describes a startup sequence that does not use the current-limiting feature and slowly turns on the MOSFET by limiting the gate dv/dt. **Case B** uses the current-limiting feature and turns on the MOSFET as fast as possible while still preventing a high inrush current.

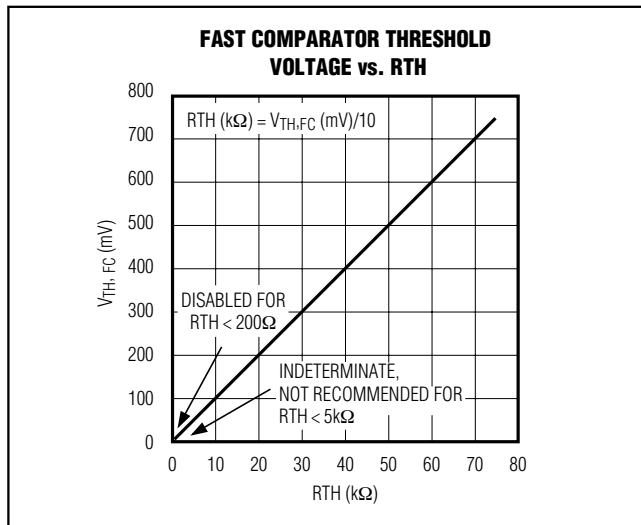


Figure 7. Fast Comparator Threshold vs. RTH

Case A. Startup Without Current Regulation

There are three ways to turn on the MOSFET without reaching the fast comparator current limit:

- 1) If the board capacitance is small, the inrush current is low.
- 2) If the gate capacitance is high, the MOSFET turns on slowly.
- 3) The fast comparator can be disabled (MAX4273 only).

In all three cases, tON is determined only by the charge required to enhance the MOSFET. Effectively, the small gate-charging current limits the output voltage dv/dt. This time can be extended by connecting an external capacitor between GATE and GND (MAX4271/MAX4272) (Figure 9) or between GATE and CEXT (MAX4273). The turn-on time is dominated by the external gate capacitance if this value is considerably higher than the MOSFET gate capacitance. Table 6 shows the timing required to enhance the recommended MOSFET with or without the external capacitor; Figure 3 shows the related waveforms and timing diagrams. (See Time to Charge Gate vs. CGATE and Startup Time with CBOARD = 0 in the *Typical Operating Characteristics*.) Remember that a high gate capacitance also increases the turn-off time (tOFF), except in the case of a MAX4273 fast fault.

If an external gate capacitor is not used, RS is not necessary. RS prevents MOSFET self-oscillations that can occur when CGATE is high while CBOARD is low.

Electrical characteristics as specified by the manufacturer's data sheet are:

FDS6670A: C_{ISS} = 3200pF, Q_{T(MAX)} = 50nC, R_{DS(ON)} = 8.2mΩ

IRF7401: C_{ISS} = 1600pF, Q_{T(MAX)} = 48nC, R_{DS(ON)} = 22mΩ

MMSF5N03HD: C_{ISS} = 1200pF, Q_{T(MAX)} = 21nC, R_{DS(ON)} = 40mΩ

Table 5. Startup and Retry Timing Parameters

| PART | tON | | tRETRY | |
|----------|--------------|-----------------------------|--------------------|---|
| | DEFAULT (μs) | EXTERNALLY SET | DEFAULT (μs) | EXTERNALLY SET |
| MAX4271 | 10 | tON (ms) = 0.31 × CTIM (nF) | No retry available | |
| MAX4272 | 10 | tON (ms) = 0.31 × CTIM (nF) | 320 | tRETRY (ms) = 32 × tON = 10 × CTIM (nF) |
| MAX4273* | 10 | tON (ms) = 0.31 × CTON (nF) | 320 | tRETRY (ms) = 10 × CTIM (nF) |

*MAX4273 retry feature disabled by connecting CTIM to VIN.

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Table 6. “No-Overcurrent” Turn-On Timing (Startup Without Current Limit)

| DEVICE | C _{GATE} (nF) | MOSFET t _{ON} (ms) | | | MOSFET t _{OFF} (ms) | | |
|---------------------------------|------------------------|-----------------------------|----------------------|-----------------------|------------------------------|----------------------|-----------------------|
| | | V _{IN} = 3V | V _{IN} = 5V | V _{IN} = 12V | V _{IN} = 3V | V _{IN} = 5V | V _{IN} = 12V |
| Fairchild FDS6670A | 0 | 0.22 | 0.16 | 0.19 | 0.07 | 0.13 | 0.145 |
| | 22 | 2.3 | 2 | 3.2 | 0.54 | 1.1 | 1.95 |
| International Rectifier IRF7401 | 0 | 0.175 | 0.130 | 0.16 | 0.075 | 0.13 | 0.16 |
| | 22 | 1.9 | 1.8 | 3.5 | 0.54 | 1.1 | 2.0 |
| Motorola MMSF5N03HD | 0 | 0.101 | 0.074 | 0.073 | 0.033 | 0.067 | 0.085 |
| | 22 | 2.0 | 1.8 | 3.2 | 0.470 | 1.0 | 1.95 |

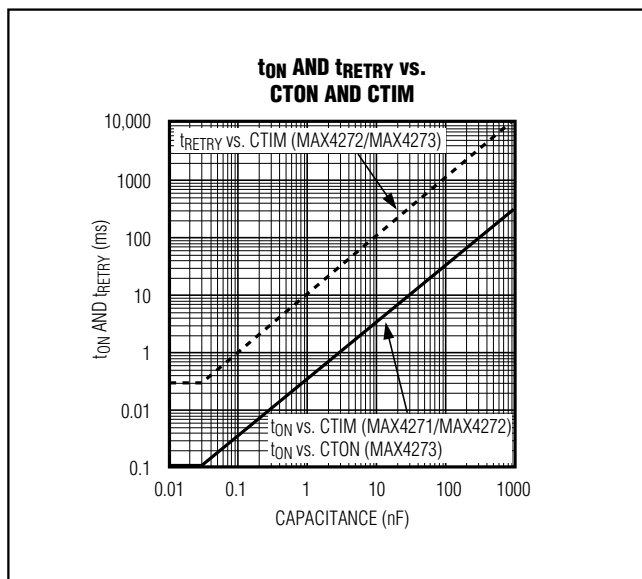


Figure 8. Startup and Retry Timeout

Case B. Startup With Current Regulation

In applications where the board capacitance (C_{BOARD}) at V_{OUT} is high, the inrush current causes a voltage drop across R_{SENSE} that exceeds the fast comparator threshold (V_{FC,TH}). In this case, the current charging C_{BOARD} can be considered constant and the turn-on time is determined by:

$$t_{ON} = C_{BOARD} \times V_{IN} / I_{FAST,SET}$$

where the maximum load current I_{FAST,SET} = V_{FC,TH} / R_{SENSE}. Figure 3 shows the waveforms and timing diagrams for a startup transient with current regulation. (See Startup Time (C_{BOARD} = 470μF) in the *Typical Operating Characteristics*.) When operating under this condition, an external gate capacitor is not required. Adding an external gate capacitor at GATE to GND reduces the regulat-

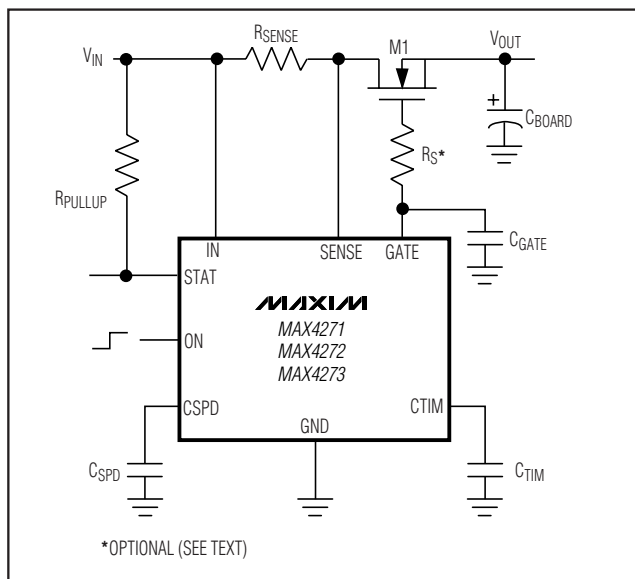


Figure 9. Operation with an External Capacitor

ed current ripple but increases t_{OFF} by increasing the gate delay (t_d) (Figure 4).

The actual startup time is determined by the longer of the two timings of Case A and Case B. Set the startup timer t_{START} at 2 × t_{ON} to guarantee enough time for the output voltage to settle; also take into consideration device parameter variation.

Retry

The retry timer defines the dead time before the IC tries to restart a startup sequence following a fault detection. This feature is available on the MAX4272/MAX4273.

Before selecting the retry timer value, determine how long a temporary high-current fault condition may be present. In the event of a permanent fault, the automatic retry will effectively force current pulses through the

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MOSFET with a duty cycle equal to t_{ON}/t_{RETRY} and with a current equal to $I_{FAST,SET}$. Therefore, particular care has to be taken when choosing between immediate retry and board space needed to manage the power dissipation capabilities of the MOSFET (see *Thermal Considerations*). The duty cycle is fixed to 1/32 for the MAX4272, but can be varied in the MAX4273 by choosing $CTIM$ and $CTON$ independently.

Additional External Gate Capacitance (CEXT)

An external gate capacitance can be connected at GATE. This increases the time required to enhance the MOSFET and further limits the output rise time. In the MAX4271/MAX4272, connect the external capacitor between GATE and GND. In the MAX4273, the external capacitor can be connected between GATE and CEXT or GND. If the capacitor is connected to CEXT, it is discharged to ground during a slow comparator fault but it is left floating during a fast comparator fault; this allows the device to turn off the external MOSFET faster during critical faults. (CEXT is biased at V_{IN} ; therefore, use a nonpolarized capacitor). Capacitance connected from GATE to CEXT does little to decrease the regulated current ripple. Add a small capacitor (5nF) from GATE to GND. See the charging and discharging time vs. C_{GATE} graphs in the *Typical Operating Characteristics*.

Slow Comparator Response Time (CSPD)

The slow comparator threshold is set at 50mV, and its response time is determined by the external capacitor connected to CSPD (Figure 10).

A minimum response time of 20 μ s (typ) is achieved by leaving this pin floating. This time is determined internally and is not affected by stray capacitance at CSPD (up to 100pF).

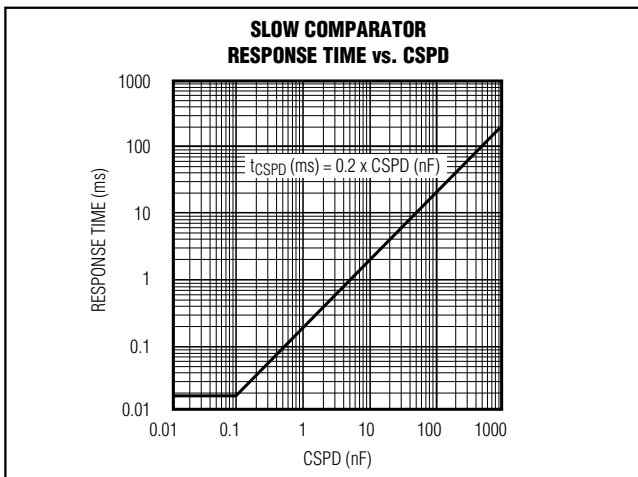


Figure 10. Slow Comparator Response Time vs. CSPD

Set the slow comparator response time to be longer than the normal operation load transients (see *Slow Comparator*).

ON and Reset Comparators

The ON comparator controls the ON/OFF function of these devices. The ON comparator is a precision voltage comparator that can be used for temperature monitoring or as an additional UVLO (Figure 11). The MAX4273 also features an uncommitted delayed comparator. This comparator can be used for voltage monitoring, power sequencing, or for generating a power-on reset signal for on-card microprocessors (Figure 12). Both comparator threshold voltages are set at $V_{REF}/2 = 0.6V$ with a 3mV (typ) hysteresis.

The uncommitted comparator OUTC output is an open-drain output, and it is asserted low when its input voltage (INC) is below the threshold voltage. It goes into a high-impedance state 150ms after the voltage has risen above the threshold. The delay for negative-going edges is 10 μ s.

Figure 13 shows the MAX4273 used to monitor precisely the temperature of an external device such as the MOSFET. This configuration uses the uncommitted comparator to set the UVLO at a higher level by running its output into the ON comparator's input.

The ON comparator initiates startup when its input voltage (V_{ON}) rises above the threshold voltage and turns off the MOSFET when the voltage falls below the threshold. The propagation delay is 10 μ s going high or low. The ON comparator is also used to reset the MAX4271/MAX4273 (when $CTIM = V_{IN}$) after a fault condition (see *Latched/Autoretry*).

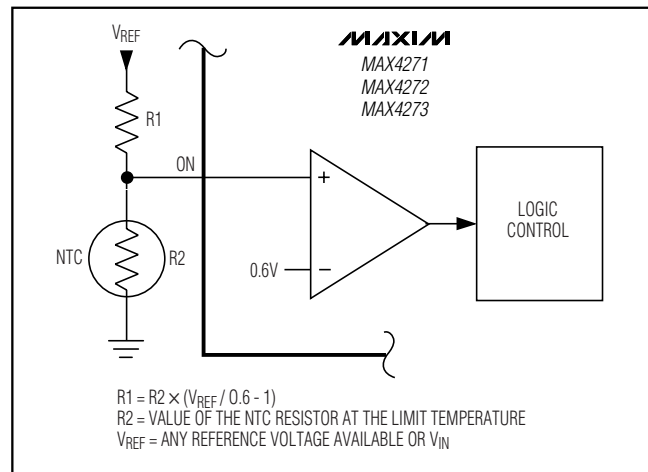


Figure 11. Temperature Monitoring and Protection

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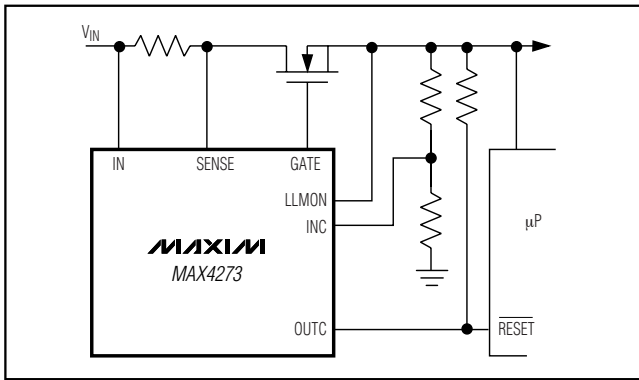


Figure 12. Power-On Reset

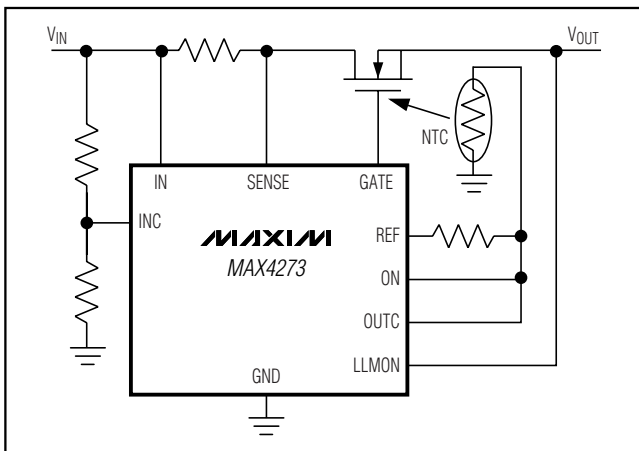


Figure 13. Power-On Reset and Temperature

The ON and INC comparator inputs and the STAT and OUTC can be pulled to voltages up to 14V independently of V_{IN} , thus allowing parts to be daisy-chained and not be turned on through the internal protection diodes. In some applications, it is useful to use connectors with staggered leads. In Figure 14, the ON pin forces the removable board to be powered up only when all connections are made.

Auxiliary VCC

The auxiliary VCC is available on the MAX4273 and is used to sustain the input voltage required for the device to operate during a short-circuit condition on the board. When a short occurs, the main system power supply could collapse and the MAX4273 will not have enough voltage to keep the gate drive operational and turn off the external MOSFET. If the fault is not removed, the system could remain in a sustained short-circuit state.

Connect a 1µF capacitor from the AUXVCC pin to GND. This capacitor will deliver the necessary energy to the

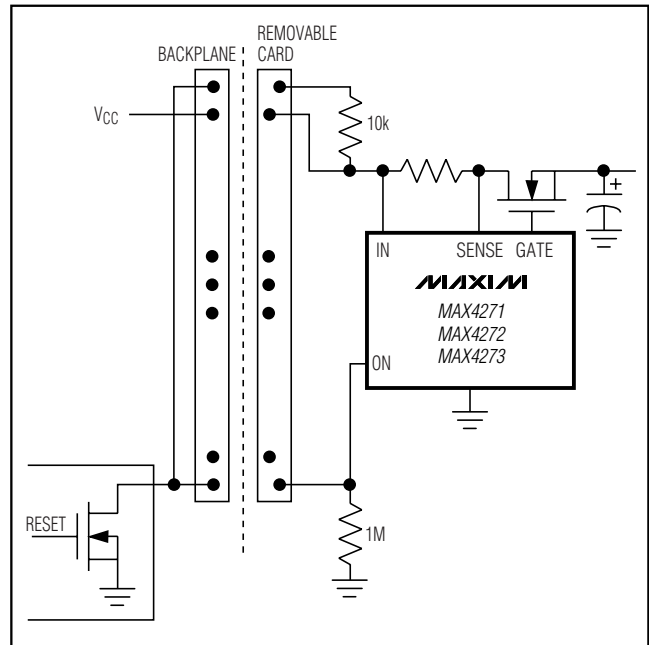


Figure 14. Fail-Safe Connector

gate drive until the MOSFET is turned off and the main supply recovers. The 1µF capacitor is charged from V_{IN} through an internal switch during normal operation.

Maximum Load Capacitance

The MAX4271/MAX4272/MAX4273 can be used on the backplane to regulate current upon insertion of a removable card (Figure 16). This allows multiple cards with different input capacitance to be inserted into the same slot even if the card doesn't have on-board hot-swap protection.

The MAX4271/MAX4272/MAX4273 current-limiting feature is active during the startup period set by CTIM. The startup period can be triggered if V_{IN} is connected to ON through a trace on the card. Once tSTART has expired (timed out), the load capacitance has to be charged or a fault condition is detected. To ensure startup with a fixed CTIM, tSTART has to be longer than the time required to charge the board capacitance. The maximum load capacitance is calculated as follows:

$$C_{BOARD} < t_{START} \times I_{FAST,SET} / V_{IN}$$

Input Transients

The voltage at V_{IN} must be above the UVLO during inrush and fault conditions. When a short condition occurs on the board, the fault current can be higher than the fast comparator current limit. The gate voltage

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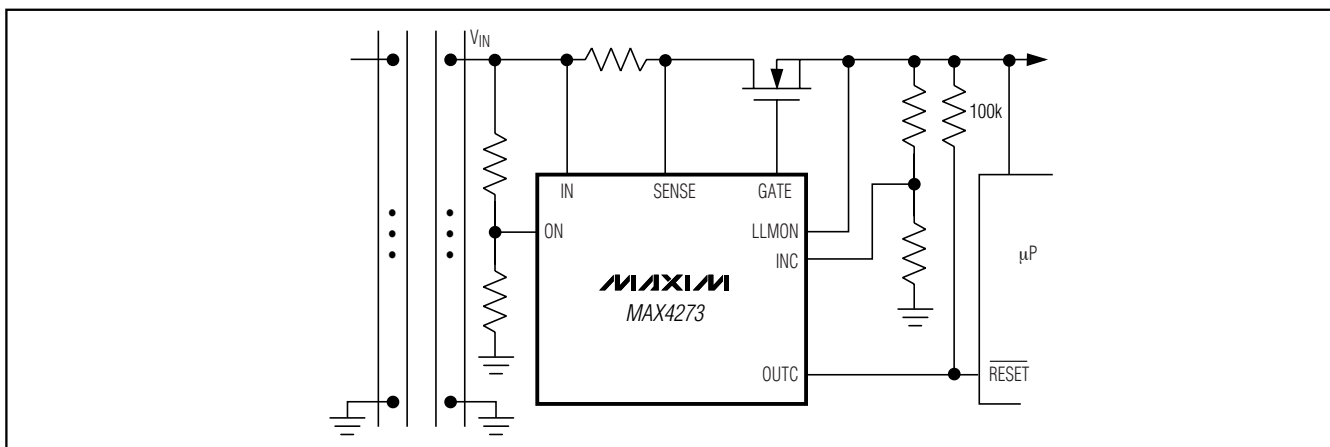


Figure 15. Adjustable Undervoltage Lockout and Output Voltage Reset Generator

is discharged immediately, but note that the MOSFET is not completely off until $V_{GS} < V_{TH}$. If the main system power supply collapses below UVLO, the MAX4271/MAX4272/MAX4273 will force the device to restart in startup mode with a 150ms delay once the supply has recovered. The main system power supply must be able to deliver this fault current without excessive voltage drop.

The MOSFET is turned off in a very short time; therefore, the resulting dv/dt can be considerable. The backplane delivering the power to the external card must have a fairly low inductance to limit the voltage transients caused by the removal of a fault. Bypassing the input with a small capacitor alleviates false UVLO trips due to these transients.

MOSFET Thermal Considerations

During normal operation, the MOSFET dissipates little power, it is fully turned on, and its $R_{DS(ON)}$ is minimal. The power dissipated in normal operation is $P_D = I_{LOAD}^2 \times R_{DS(ON)}$. A considerable amount of power is dissipated during the startup and turn-off transients. The design must take into consideration the worst-case scenario of a continuous short-circuit fault present on the board. Two cases need to be considered:

- 1) The single turn-on with the device latched after a fault (when using MAX4271 or MAX4273 in latched mode)
- 2) The continuous automatic retry (when using the MAX4272 or MAX4273 in retry mode)

Use the following equation to calculate the maximum transient thermal resistance (in $^{\circ}C/W$) required for an output short to ground:

$$Z_{\theta JA}(\max) = (T_{JMAX} - T_A) / (V_{IN} \times I_{FAST, SET})$$

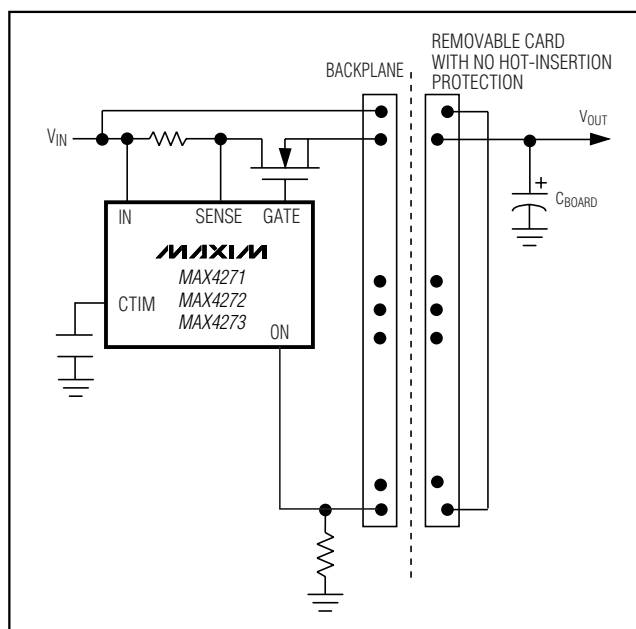


Figure 16. Using the MAX4271/MAX4272/MAX4273 on a Backplane

MOSFET manufacturers typically include curves for the transient thermal resistance, $Z_{\theta JA}$, of the package (Figure 17). Find the thermal impedance of the MOSFET by using t_{START} as the pulse duration and by choosing the single pulse curve for latched mode parts or by choosing the duty cycle = 0.03 curve for the MAX4272 (the duty cycle is fixed at 32:1). If the $Z_{\theta JA}$ required is less than that of the package, reduce t_{START} , reduce $I_{FAST, SET}$, use a heatsink on the MOSFET, or choose one with better thermal characteristics.

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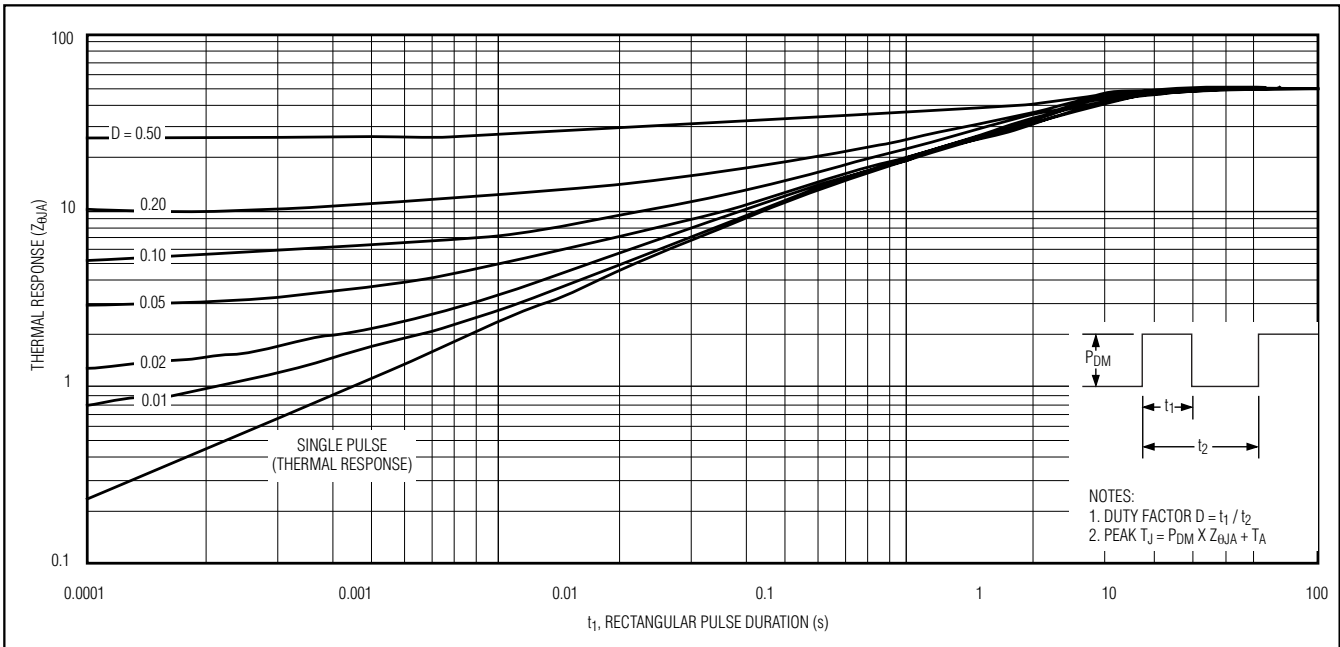


Figure 17. Example Curves (from IRF7413A) for Maximum Effective Transient Thermal Impedance, Junction to Ambient

For the MAX4273 in retry mode, the duty cycle can be adjusted. Use the MOSFET $Z_{\theta JA}$ curve and the t_{START} pulse duration to choose a maximum duty cycle, D. Calculate the retry time:

$$t_{RETRY} = t_{START} / D$$

Use Figure 8 to determine CTIM given t_{RETRY} .

Design Procedure (MAX4273)

GIVEN:

- Hot-swap 5V supply to a 1000 μ F card
- MOSFET IRF7413A: $R_{DS(on)} = 0.0135\Omega$
- Operating current = 4A
- Overload current = 5A
- System current limit = 10A
- Retry enabled

PROCEDURE:

- 1) Select the current sense resistor:
 - Slow comparator threshold = 50mV
 - Overload current = 5A
 - Current-sense resistor value = $50mV/5A = 10m\Omega$
 - The device will initiate a slow fault if the load current is greater than 5A for longer than 20 μ s after startup.
- 2) Set fast comparator threshold (RTH).

The MOSFET pulsed drain current limit is 58A. Another consideration for setting the current limit is the system requirement. Systems may glitch if 58A load transients are present. For this example, the load transient will be limited to 10A:

- System current limit = 10A
- Current-sense resistor = 10m Ω
- Fast comparator threshold = $10m\Omega \times 10A = 100mV$
- Select RTH from Figure 7, $RTH = 10k\Omega$

3) Set Startup timer.

- Startup current = System current limit = 10A
- $V_{IN} = 5V$
- $C_{BOARD} = 1000\mu F$
- $t_{ON} = 1000\mu F \times 5V / 10A = 500\mu s$
- Give a factor of 2 guardband on the startup timer.
- $t_{START} = 2 \times t_{ON} = 1.0ms$
- From Figure 8, $C_{TON} = 3000pF$.

4) Select Retry Timeout.

- $V_{IN} = 5V$.
- $I_{MAX} = 10A$.
- Peak junction temperature, $T_J = 150^\circ C_J$
- Peak ambient temperature, $T_A = 85^\circ C_A$

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Calculate the MOSFET thermal resistance required for a short to ground.

$$Z_{\theta JA} = (150^{\circ}\text{C} - 85^{\circ}\text{C}) / (5\text{V} \times 10\text{A}) = 1.30^{\circ}\text{C}/\text{W}$$

Using $t_{\text{START}} = 1\text{ms}$ as the pulse duration, use Figure 17 to select a duty cycle. The duty cycle should be about 0.01 or less. This implies $t_{\text{RETRY}} = t_{\text{START}} / 0.01 = 100\text{ms}$. From Figure 8, $C_{\text{TIM}} = 10\text{nF}$.

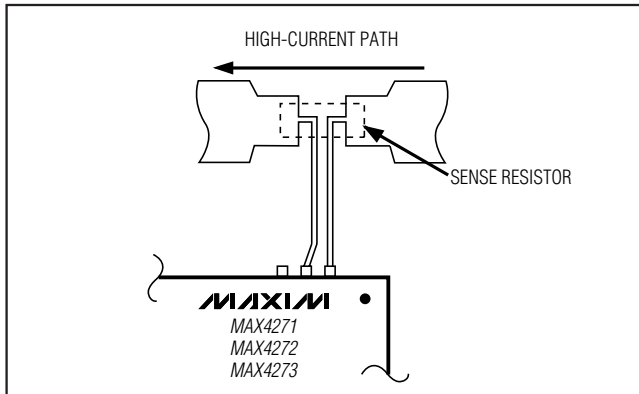


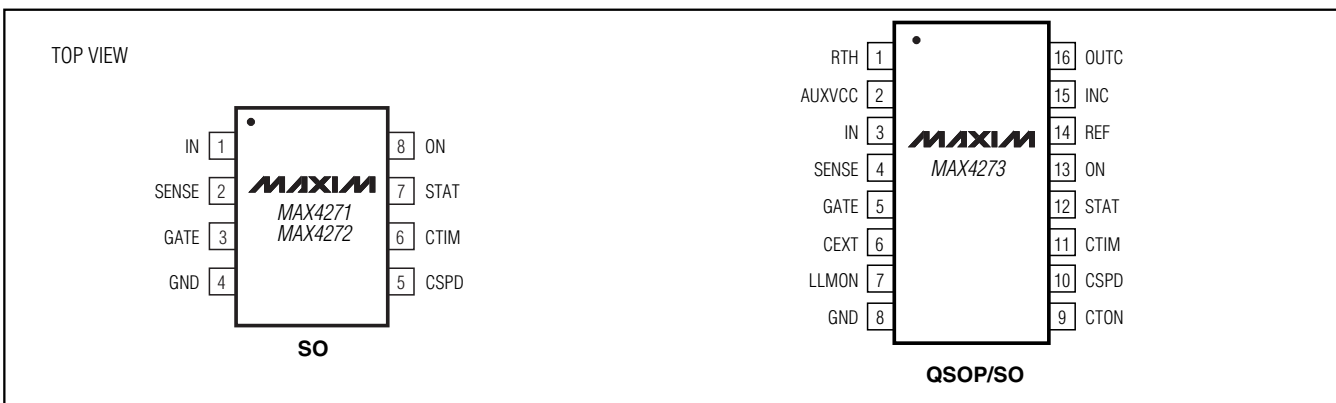
Figure 18. Kelvin Connections for the Current-Sense Resistors

Layout Considerations

To take full tracking advantage of the switch response time to an output fault condition, it is important to keep all traces as short as possible and to maximize the high-current trace dimensions to reduce the effect of undesirable parasitic inductance. Place the MAX4271/MAX4272/MAX4273 close to the card's connector. Use a ground plane to minimize impedance and inductance. Minimize the current-sense resistor trace length (<10mm), and ensure accurate current sensing with Kelvin connections (Figure 18).

When the output is short circuited, the voltage drop across the external MOSFET becomes large. Hence, the power dissipation across the switch increases, as does the die temperature. An efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Connect the two pads to the ground plane through vias, and use enlarged copper mounting pads on the top side of the board.

Pin Configurations



3V to 12V Current-Limiting Hot-Swap Controllers with Autoretry, DualSpeed/BiLevel Fault Protection

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

SOICN.EPS

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 BSC | | 1.27 BSC | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

VARIATIONS:

| DIM | INCHES | | MILLIMETERS | | N | MS012 |
|-----|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | AA |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | AB |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | AC |

NOTES:

1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR **MAXIM**

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

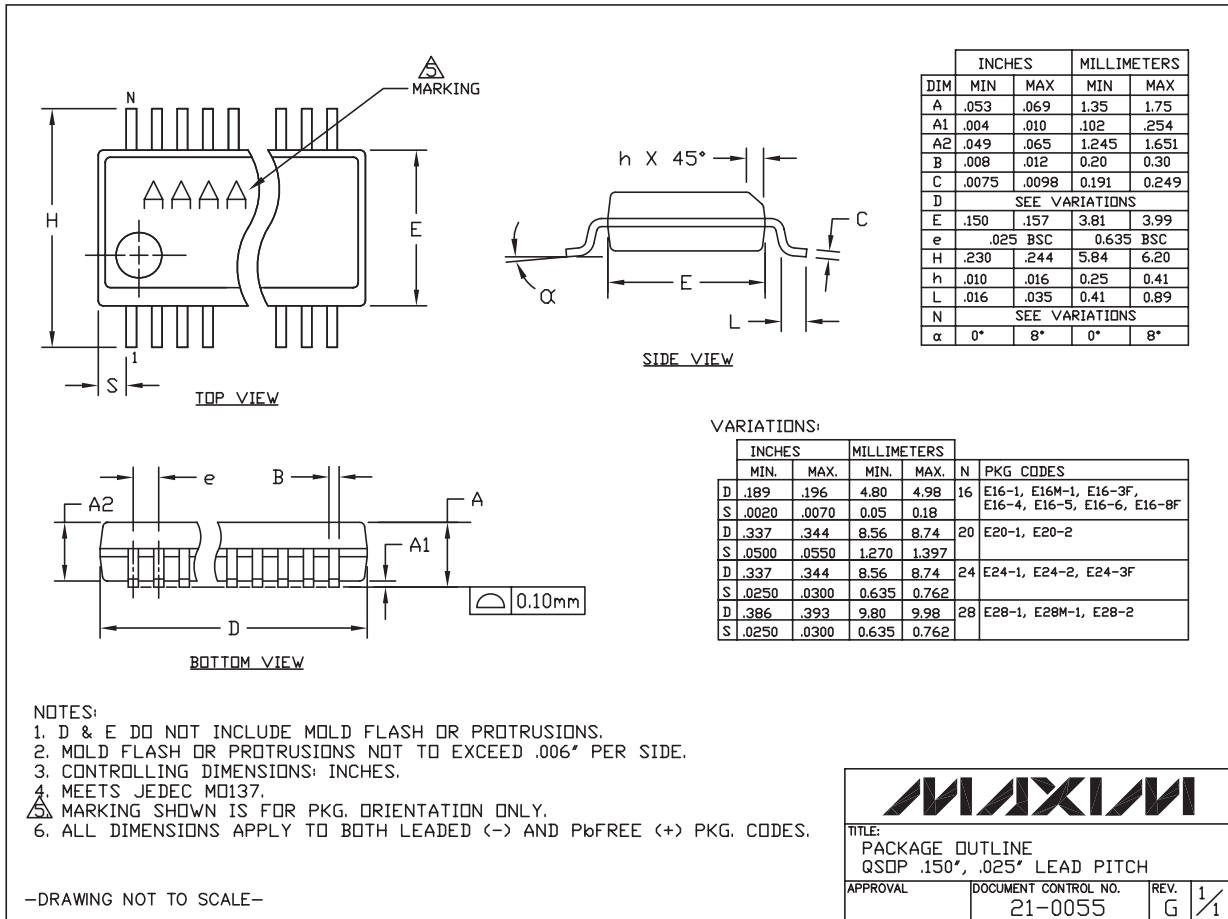
| | | |
|----------|----------------------|-------|
| APPROVAL | DOCUMENT CONTROL NO. | REV. |
| | 21-0041 | B 1/1 |

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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to www.maxim-ic.com/packages.)

MAX4271/MAX4272/MAX4273



QSDP:EPS

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Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|------------------------|----------------------|---|----------------------|
| 0 | 4/00 | Initial release | — |
| 1 | 7/00 | Removed future product designation for MAX4273 | 1 |
| 1a | 4/01 | Updated footer | 1 |
| 2 | 12/07 | Included Package codes in Ordering Information table, Updated Note 5 and Package Outlines | 1, 4, 24 |

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Тел: +7 (812) 336 43 04 (многоканальный)

Email: org@lifeelectronics.ru