

FEATURES

Low offset voltage (maximum specifications)

B-Grade: 25 μV (SOIC)

A-Grade: 50 μV (SOIC), 90 μV (MSOP)

Very low offset voltage drift

B-Grade: 0.25 $\mu\text{V}/^\circ\text{C}$ (SOIC)

A-Grade: 0.55 $\mu\text{V}/^\circ\text{C}$ (SOIC) and 1.2 $\mu\text{V}/^\circ\text{C}$ (MSOP), specified over -40°C to $+125^\circ\text{C}$, MSL1 rated

Low input bias current: 1.0 nA maximum

Low noise: 7 nV/ $\sqrt{\text{Hz}}$ typical

CMRR, PSRR, and $A_{VO} > 120$ dB minimum

Low supply current: 400 μA per amplifier typical

Wide bandwidth: 4.0 MHz

Dual-supply operation: ± 5 V to ± 15 V

Unity-gain stable

No phase reversal

APPLICATIONS

Process control front-end amplifiers

Wireless base station control circuits

Optical network control circuits

Instrumentation

Sensors and controls: thermocouples, resistor thermal detectors (RTDs), strain bridges, and shunt current measurements

Precision filters

GENERAL DESCRIPTION

The [ADA4077-2](#) is a dual amplifier featuring extremely low offset voltage and drift and low input bias current, noise, and power consumption. Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

Applications for this amplifier include sensor signal conditioning (such as thermocouples, RTDs, strain gauges), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems. The [ADA4077-2](#) is useful in line powered and portable instrumentation, precision filters, and voltage or current measurement and level setting.

Unlike the amplifiers of some competitors, the [ADA4077-2](#) is specified over the extended industrial temperature range for operation from -40°C to $+125^\circ\text{C}$ with MSL1 rating for the most demanding operating environments. It is available in 8-lead SOIC (including the B-Grade) and MSOP (A-Grade only) packages.

PIN CONNECTION DIAGRAMS

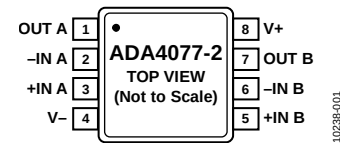


Figure 1. [ADA4077-2](#) Pin Configuration, 8-Lead MSOP

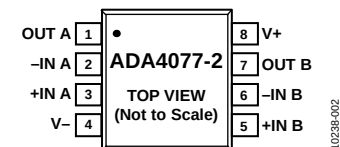


Figure 2. [ADA4077-2](#) Pin Configuration, 8-Lead SOIC_N

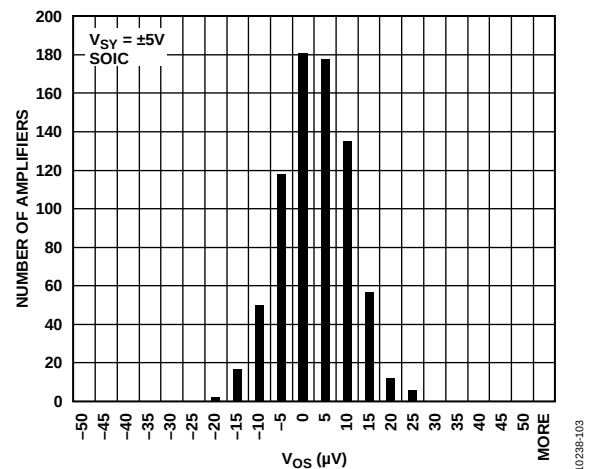


Figure 3. Offset Voltage Distribution

Table 1. Evolution of Precision Devices by Generation

Op Amp	1st	2nd	3rd	4th	5th	6th
Single	OP07	OP77	OP177	OP1177	AD8677	
Dual				OP2177		ADA4077-2
Quad				OP4177		

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REVISION HISTORY

10/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ± 5.0 V

$V_{SY} = \pm 5.0$ V, $V_{CM} = 0$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade, SOIC)	V_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10	25	μV
Offset Voltage Drift (B Grade, SOIC)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	65	$\mu\text{V}/^\circ\text{C}$
Offset Voltage (A Grade)	V_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$				
SOIC				15	50	μV
MSOP					105	μV
				50	90	μV
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			220	μV
SOIC				0.25	0.55	$\mu\text{V}/^\circ\text{C}$
MSOP				0.5	1.2	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1	-0.4	+1	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.5		+1.5	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-0.5	+0.1	+0.5	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.0		+1.0	nA
Input Voltage Range			-3.8		+3	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -3.8$ V to +3V	122	140		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2$ k Ω , $V_O = -3.0$ V to +3.0 V	121	130		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120			dB
Input Capacitance	C_{INDM}	Differential mode		3		pF
	C_{INCM}	Common mode		5		pF
Input Resistance	R_{IN}			100		M Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1$ mA	+4.1			V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+4			V
Output Voltage Low	V_{OL}	$I_L = 1$ mA			-3.5	V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			-3.2	V
Output Current	I_{OUT}	$V_{DROPOUT} < 1.6$ V		± 10		mA
Short-Circuit Current	I_{SC}	$T_A = 25^\circ\text{C}$		22		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1$ kHz, $A_V = +1$		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5$ V to ± 18 V	123	128		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120			dB
Supply Current per Amplifier	I_{SY}	$V_O = 0$ V		400	450	μA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			650	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2$ k Ω		1		V/ μs
Settling Time to 0.1%	t_s	$V_{IN} = 1$ V step, $R_L = 4$ k Ω , $A_V = -1$		2		μs
Gain Bandwidth Product	GBP	$A_V = +1$		4.0		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		μV p-p
Voltage Noise Density	e_n	$f = 1$ Hz		13		nV/ $\sqrt{\text{Hz}}$
		$f = 100$ Hz		7		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1$ kHz		3		pA/ $\sqrt{\text{Hz}}$
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	$f = 1$ kHz		-120		dB

ELECTRICAL CHARACTERISTICS, ± 15.0 V

$V_{SY} = \pm 15$ V, $V_{CM} = 0$ V, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade, SOIC)	V_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10	35	μV
Offset Voltage Drift (B Grade, SOIC)	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.1	65	$\mu\text{V}/^\circ\text{C}$
Offset Voltage (A Grade) SOIC	V_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		15	50	μV
MSOP					105	μV
Offset Voltage Drift (A Grade) SOIC	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	0.55	$\mu\text{V}/^\circ\text{C}$
MSOP				0.5	1.2	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1	-0.4	+1	nA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.5		+1.5	nA
Input Voltage Range			-0.5	+0.1	+0.5	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -13.8$ V to $+13$ V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-1.0		+1.0	nA
Large Signal Voltage Gain	A_{VO}	$R_L = 2$ k Ω , $V_O = -13.0$ V to $+13.0$ V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-13.8		+13	V
Input Capacitance	C_{INDM} C_{INCM}	Differential mode Common mode		3		pF
Input Resistance	R_{IN}			5		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1$ mA $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+14.1			V
Output Voltage Low	V_{OL}	$I_L = 1$ mA $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+14		-13.5	V
Output Current	I_{OUT}	$V_{DROPOUT} < 1.2$ V		± 10	-13.2	V
Short-Circuit Current	I_{SC}	$T_A = 25^\circ\text{C}$		22		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1$ kHz, $A_V = +1$		0.05		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = \pm 2.5$ V to ± 18 V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	123	128		dB
Supply Current per Amplifier	I_{SY}	$V_O = 0$ V $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	120	400	500	dB
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2$ k Ω		1		$\text{V}/\mu\text{s}$
Settling Time to 0.01%	t_s	$V_{IN} = 10$ V p-p, $R_L = 4$ k Ω , $A_V = -1$		9		μs
Settling Time to 0.1%	t_s	$V_{IN} = 10$ V p-p, $R_L = 4$ k Ω , $A_V = -1$		8		μs
Gain Bandwidth Product	GBP	$A_V = +1$		3.9		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.25		μV p-p
Voltage Noise Density	e_n	$f = 1$ Hz		13		nV/ $\sqrt{\text{Hz}}$
		$f = 100$ Hz		7		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1$ kHz		3		pA/ $\sqrt{\text{Hz}}$
MULTIPLE AMPLIFIERS CHANNEL SEPARATION	C_S	$f = 1$ kHz		-120		dB

ABSOLUTE MAXIMUM RATINGS**Table 4.**

Parameter	Rating
Supply Voltage	36 V
Input Voltage	$\pm V_{SY}$
Differential Input Voltage	$\pm V_{SY}$
Storage Temperature Range	
MSOP and SOIC_N Packages	–65°C to +150°C
Operating Temperature Range	–40°C to +125°C
Junction Temperature Range	
R and RM Packages	–65°C to +150°C
Lead Temperature, Soldering (10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead MSOP	190	44	°C/W
8-Lead SOIC_N	158	43	°C/W

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

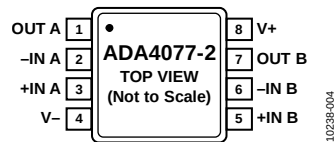


Figure 4. Pin Configuration, 8-Lead MSOP (RM Suffix)

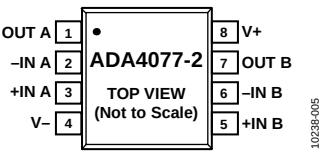


Figure 5. Pin Configuration, 8-Lead SOIC_N (R Suffix)

Table 6. ADA4077-2 Pin Function Descriptions, MSOP and SOIC

Pin No.	Mnemonic	Description
1	OUT A	Output, Channel A.
2	–IN A	Inverting Input, Channel A.
3	+IN A	Noninverting Input, Channel A.
4	V–	Negative Supply Voltage.
5	+IN B	Noninverting Input, Channel B.
6	–IN B	Inverting Input, Channel B.
7	OUT B	Output, Channel B.
8	V+	Positive Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

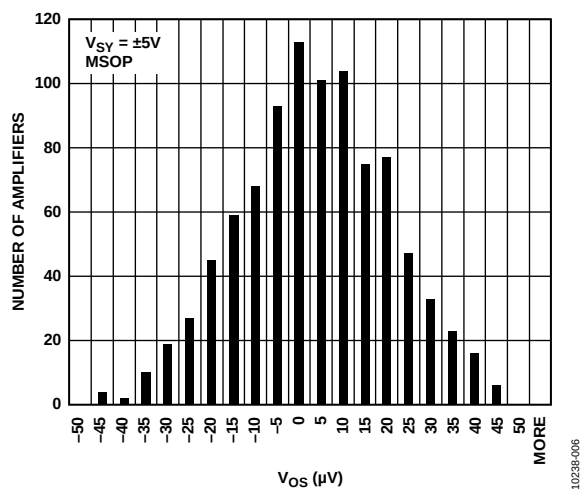


Figure 6. Offset Voltage Distribution

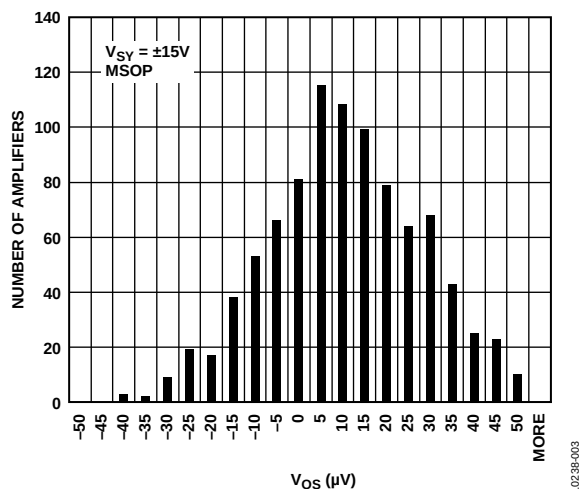


Figure 9. Offset Voltage Distribution

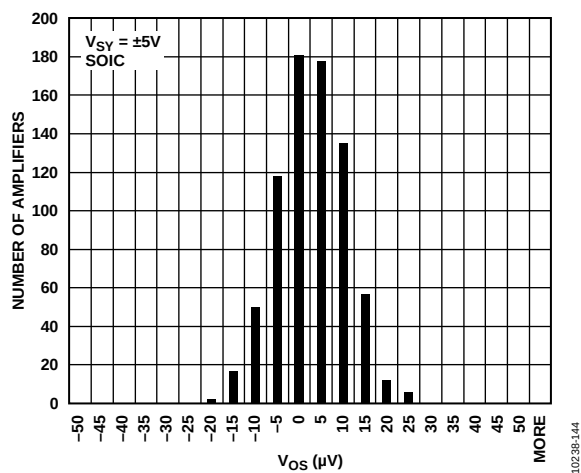


Figure 7. Offset Voltage Distribution

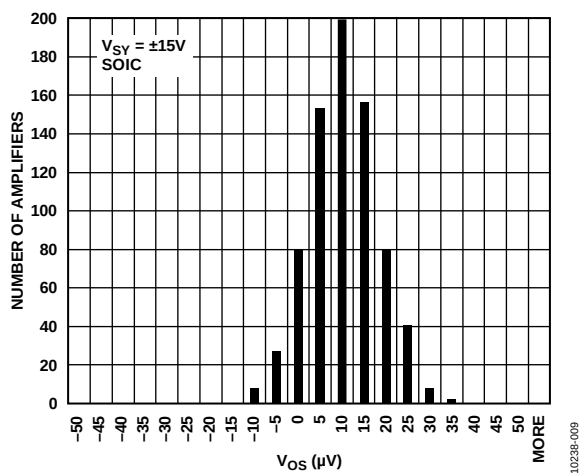


Figure 10. Offset Voltage Distribution

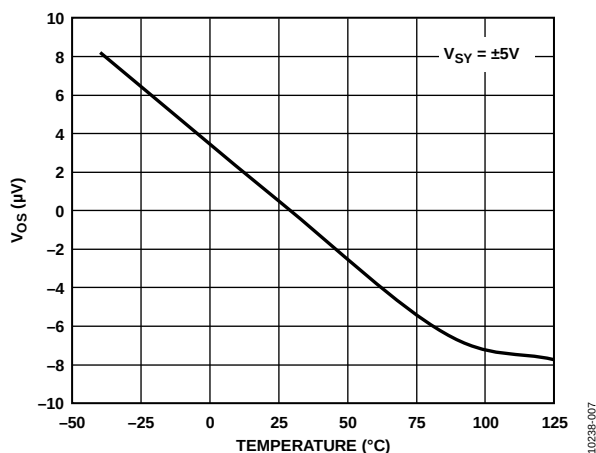


Figure 8. Offset Voltage vs. Temperature

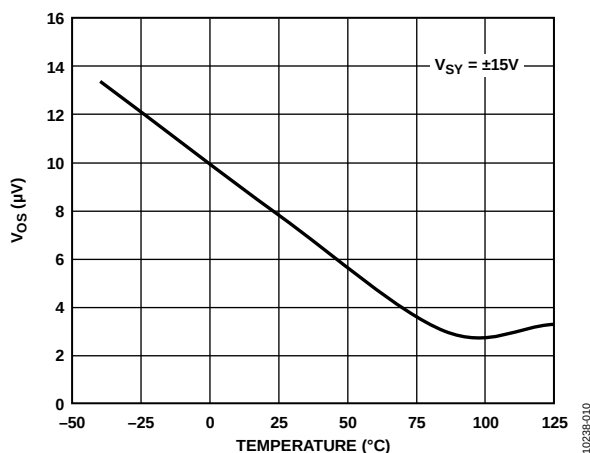


Figure 11. Offset Voltage vs. Temperature

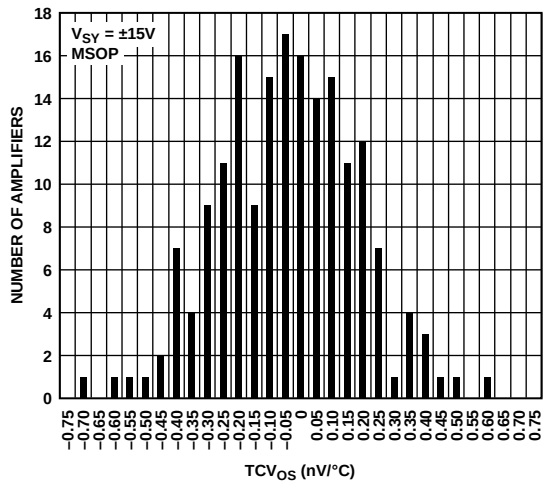


Figure 12. TCV_{OS} , MSOP

10238-130

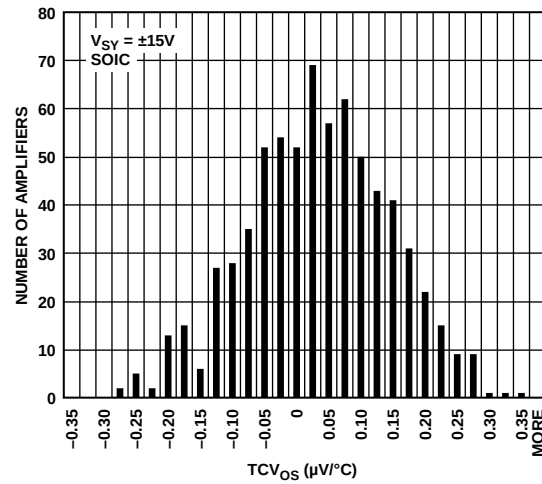


Figure 15. TCV_{OS} , SOIC

10238-008

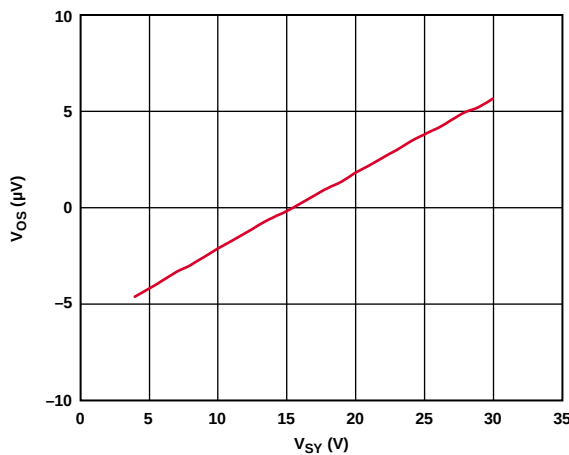


Figure 13. V_{OS} vs. Supplies

10238-134

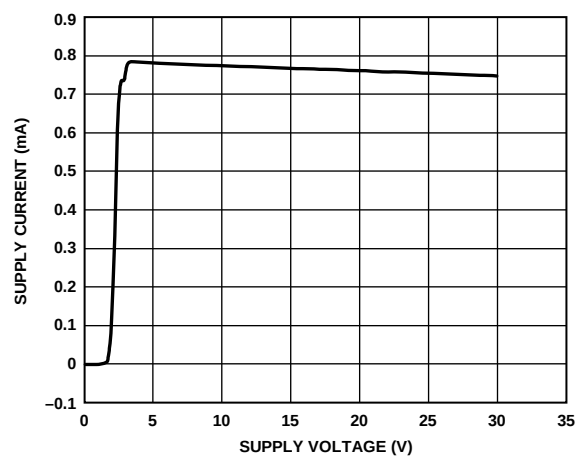


Figure 16. I_{SY} vs. V_{SY}

10238-126

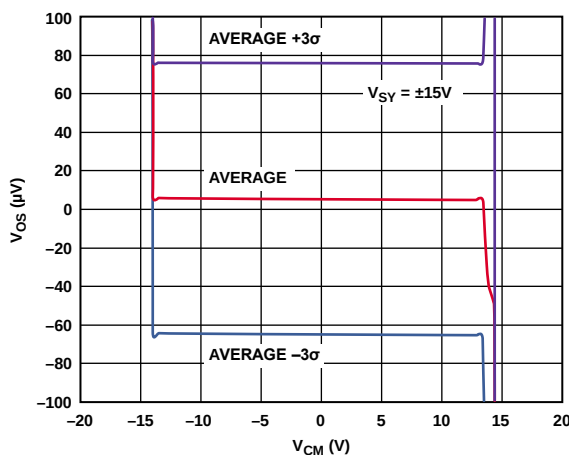


Figure 14. V_{OS} vs. V_{CM}

10238-112

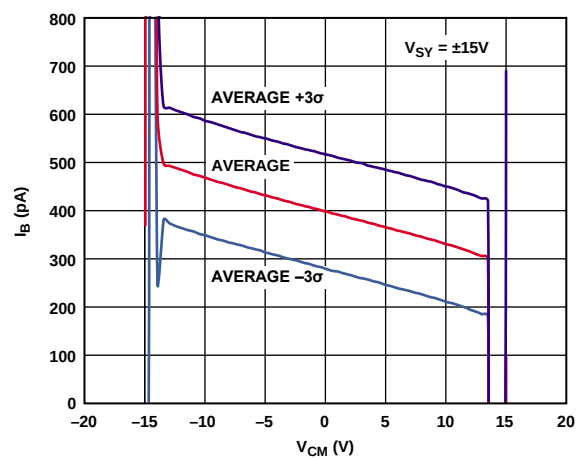


Figure 17. Input Bias Current vs. V_{CM}

10238-115

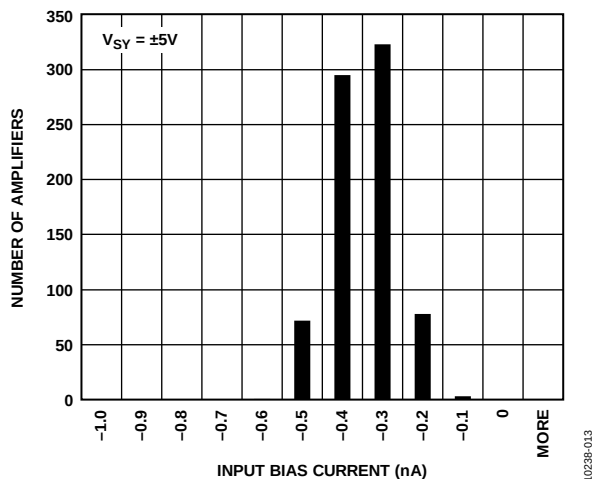


Figure 18. Input Bias Current

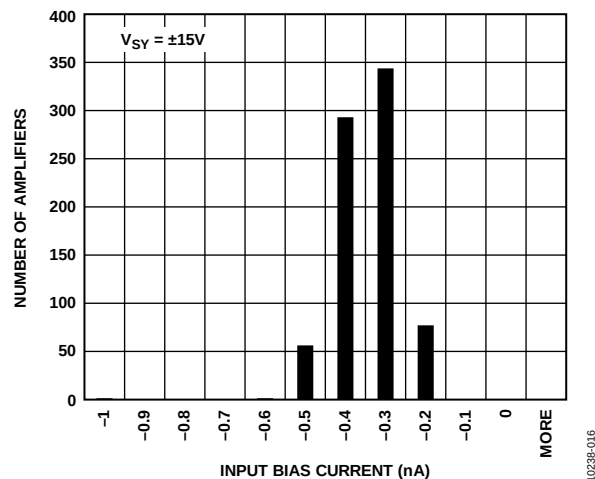


Figure 21. Input Bias Current

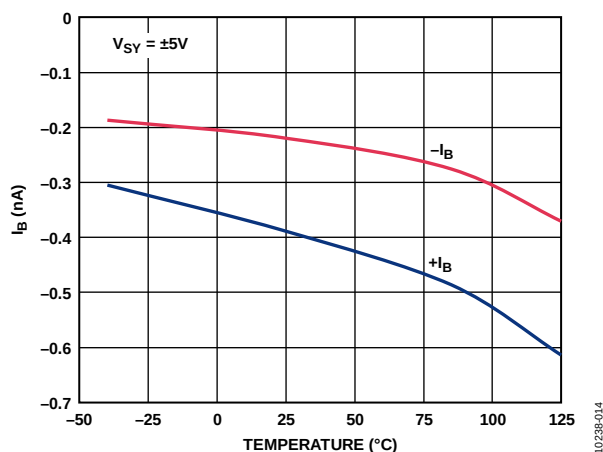


Figure 19. Input Bias Current vs. Temperature

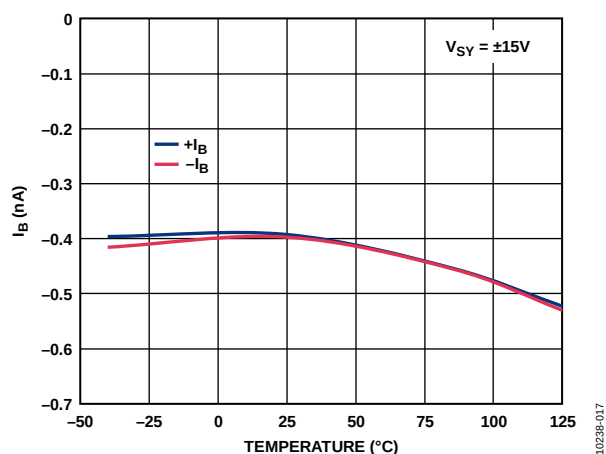
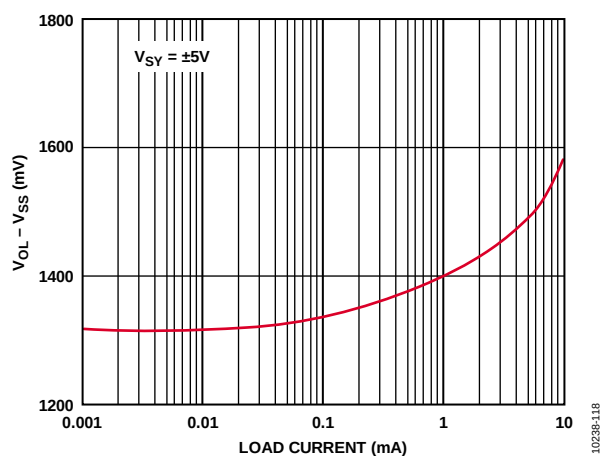
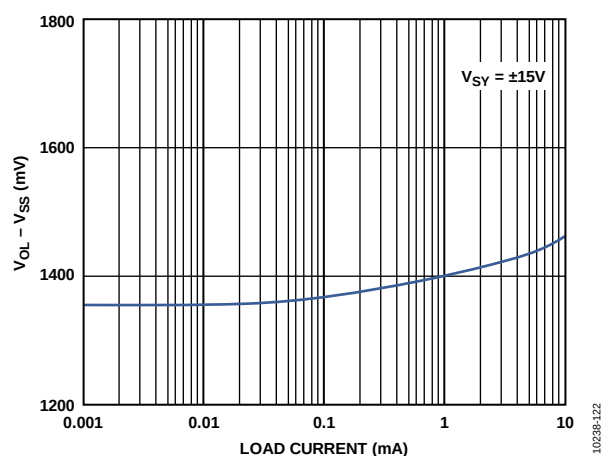


Figure 22. Input Bias Current vs. Temperature

Figure 20. V_{OL} vs. LoadFigure 23. V_{OL} vs. Load

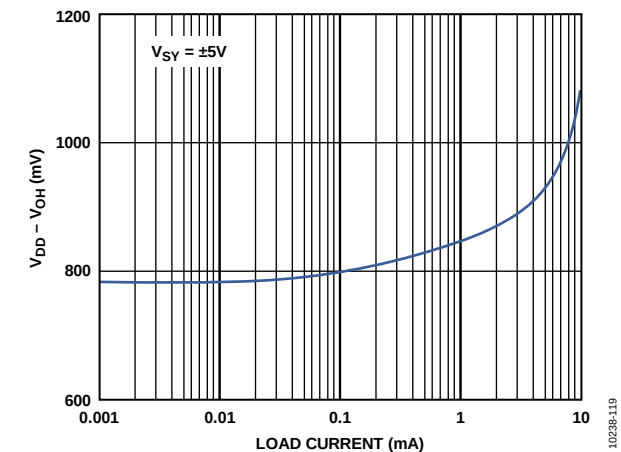


Figure 24. Output Dropout Voltage vs. Load

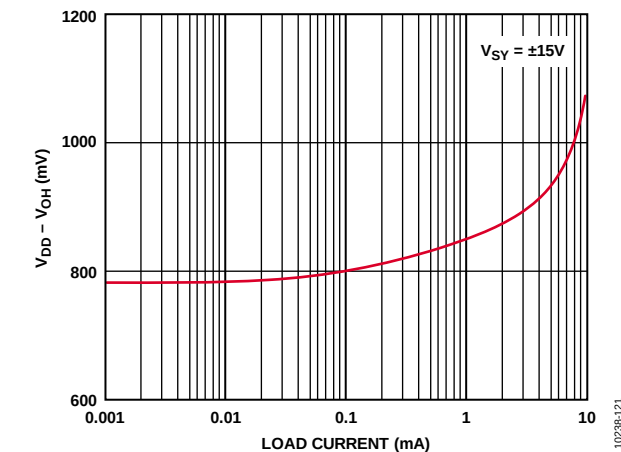


Figure 27. Output Dropout Voltage vs. Load

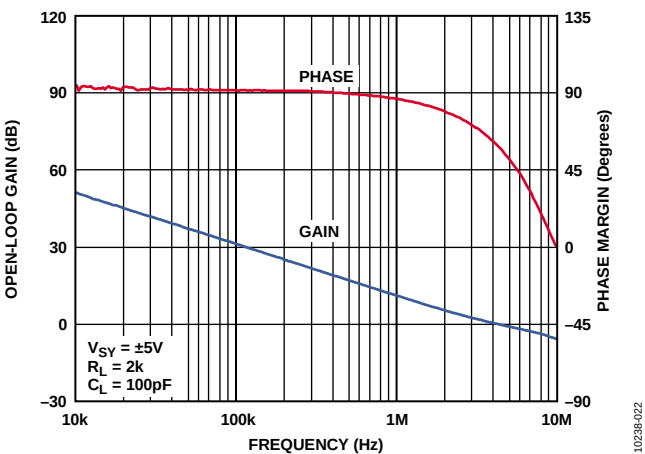


Figure 25. Open-Loop Gain and Phase vs. Frequency

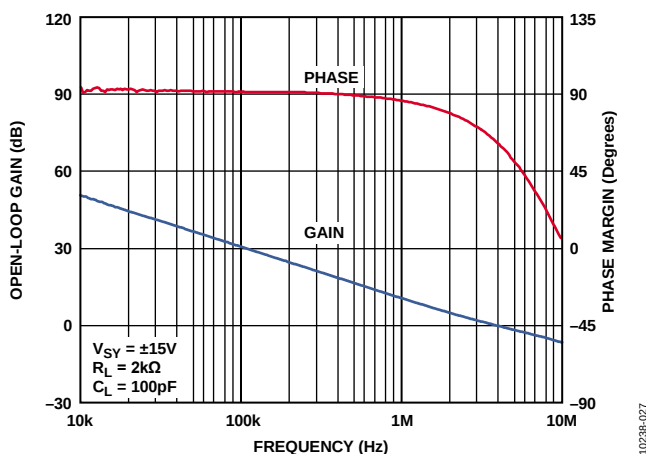


Figure 28. Open-Loop Gain and Phase vs. Frequency

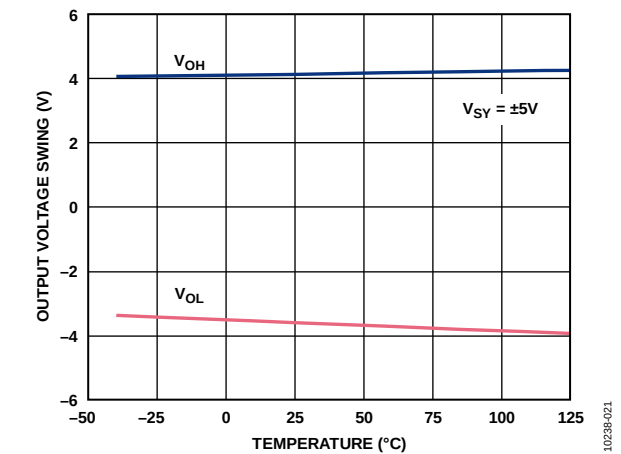


Figure 26. Output Voltage Swing vs. Temperature

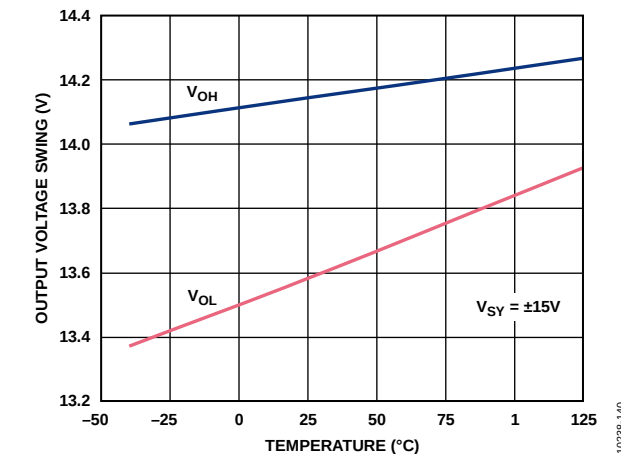
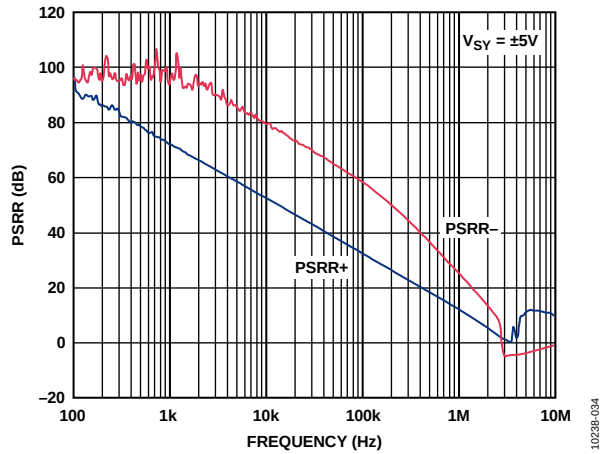
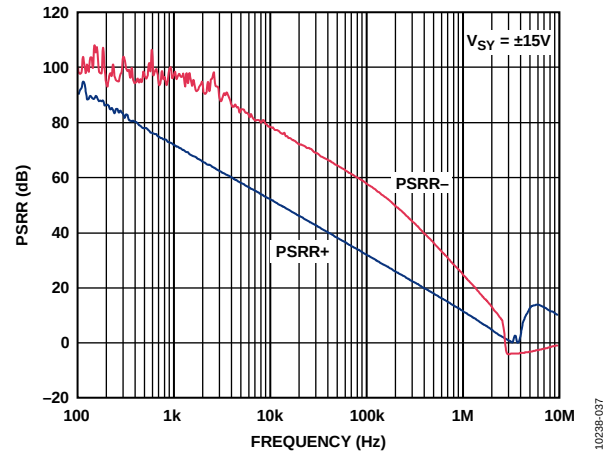


Figure 29. Output Voltage Swing vs. Temperature

Figure 30. PSRR vs. Frequency, $\pm 5\text{ V}$

10238-034

Figure 33. PSRR vs. Frequency, $\pm 15\text{ V}$

10238-037

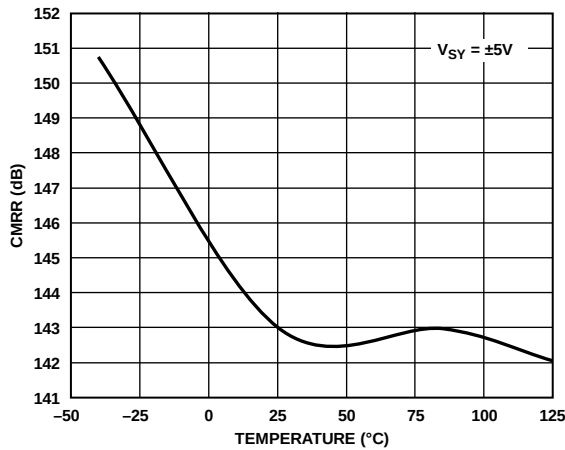


Figure 31. CMRR vs. Temperature

10238-030

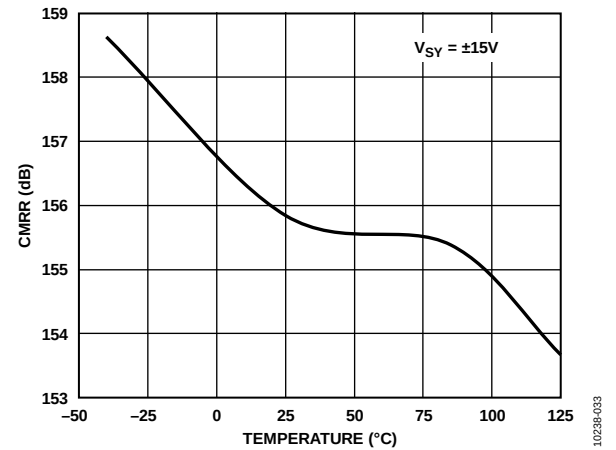


Figure 34. CMRR vs. Temperature

10238-033

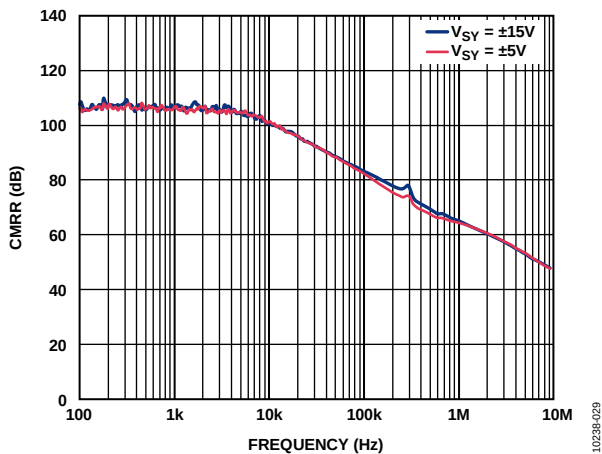


Figure 32. CMRR vs. Frequency

10238-029

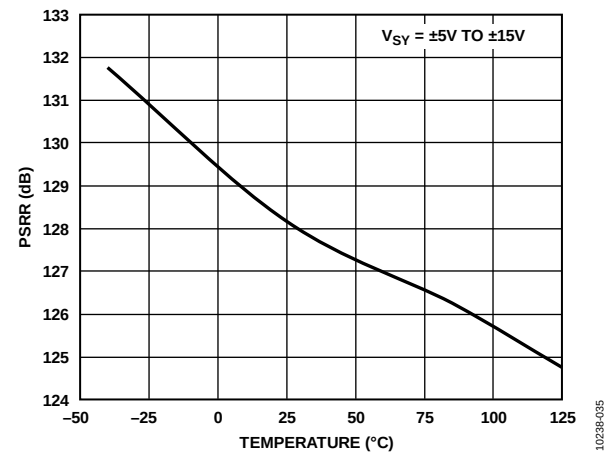


Figure 35. PSRR vs. Temperature

10238-035

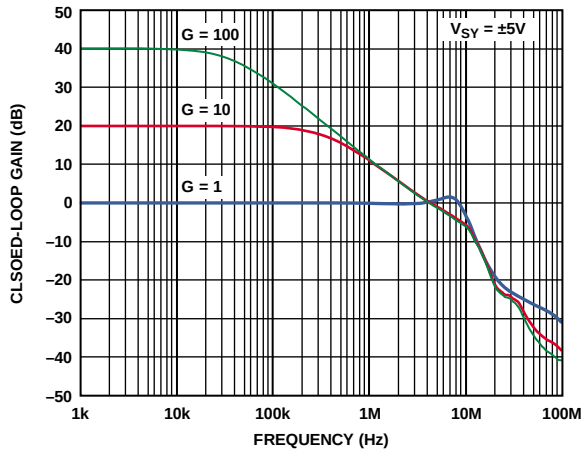


Figure 36. Closed-Loop Gain vs. Frequency

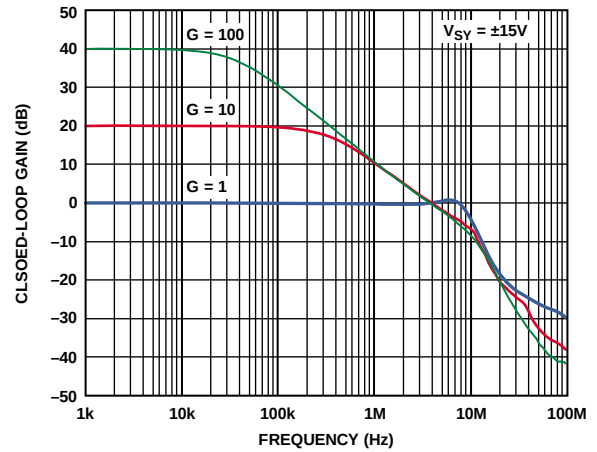


Figure 39. Closed-Loop Gain vs. Frequency

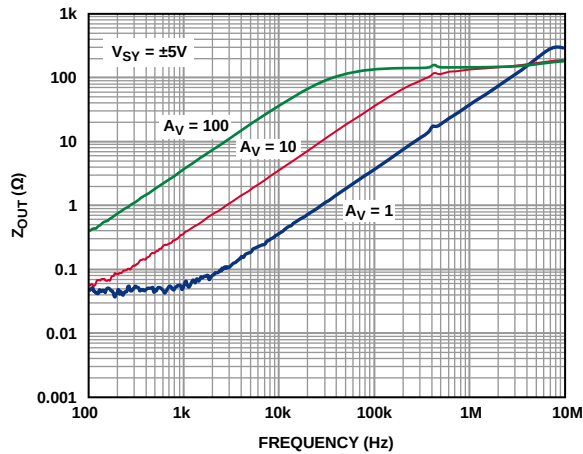


Figure 37. Output Impedance vs. Frequency

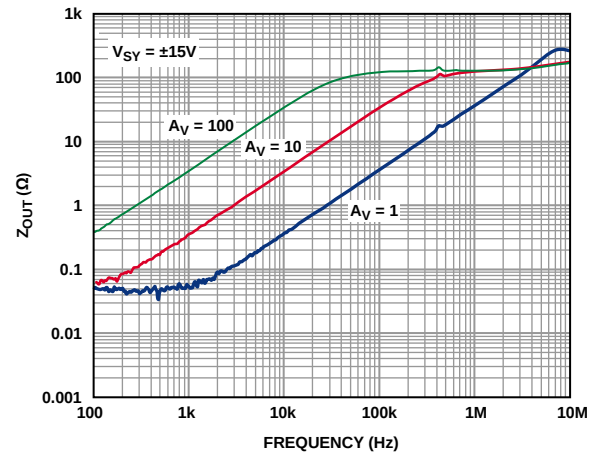


Figure 40. Output Impedance vs. Frequency

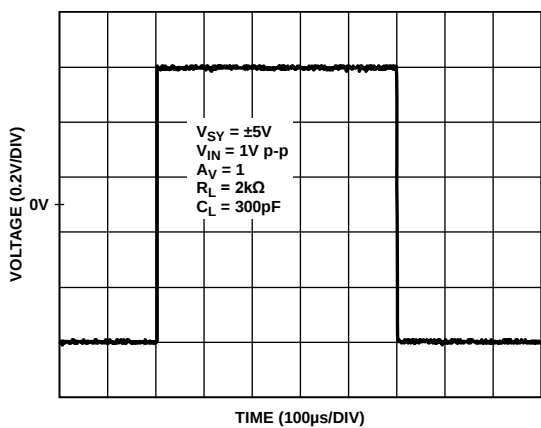


Figure 38. Large Signal Transient Response

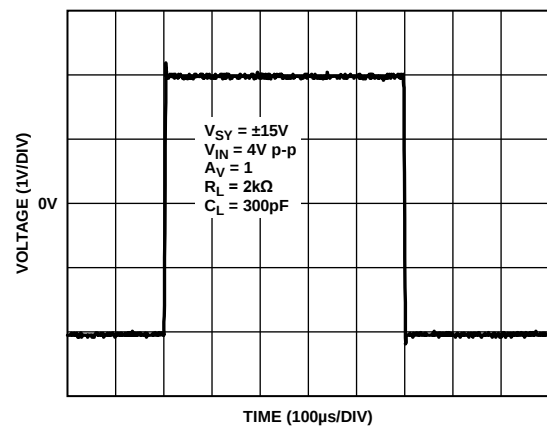


Figure 41. Large Signal Transient Response

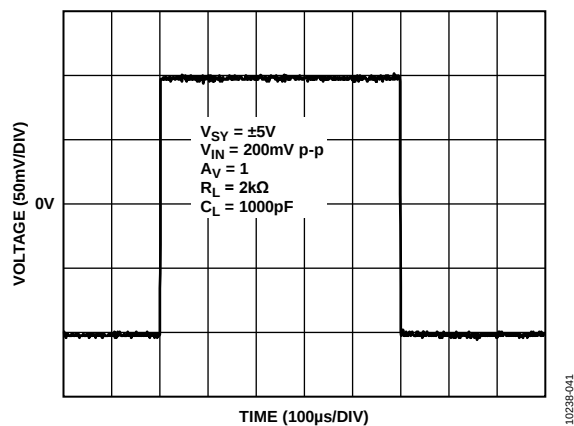


Figure 42. Small Signal Transient Response

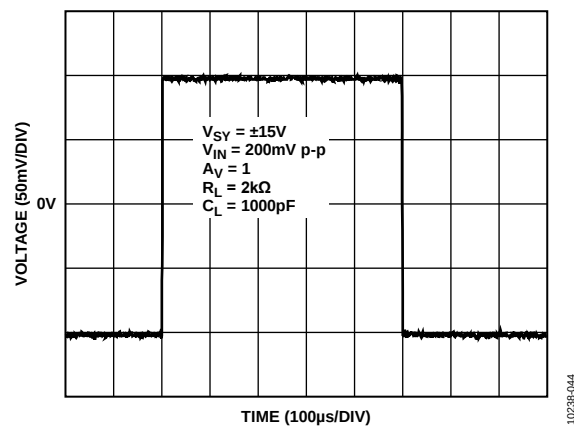


Figure 45. Small Signal Transient Response

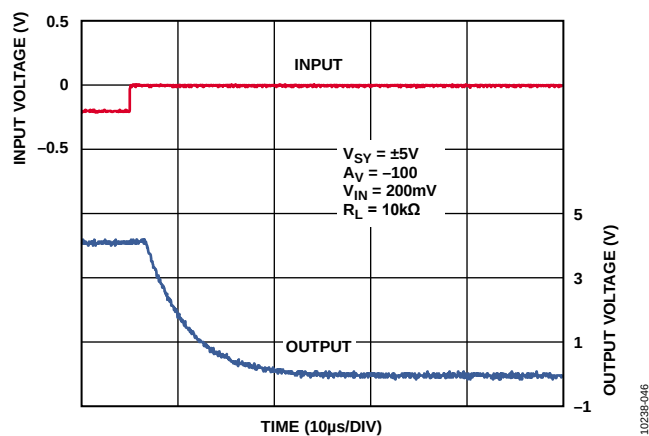


Figure 43. Positive Overload Recovery

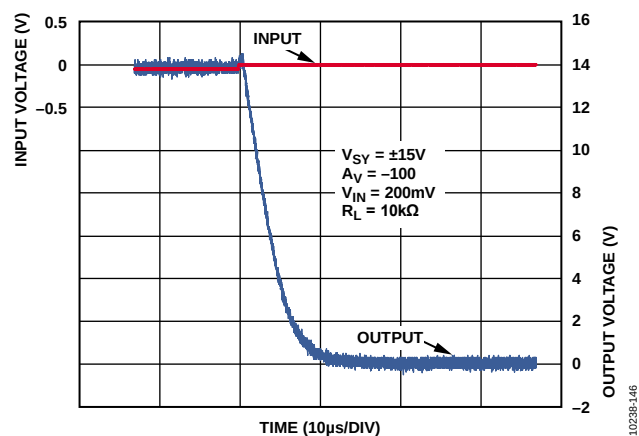


Figure 46. Positive Overload Recovery

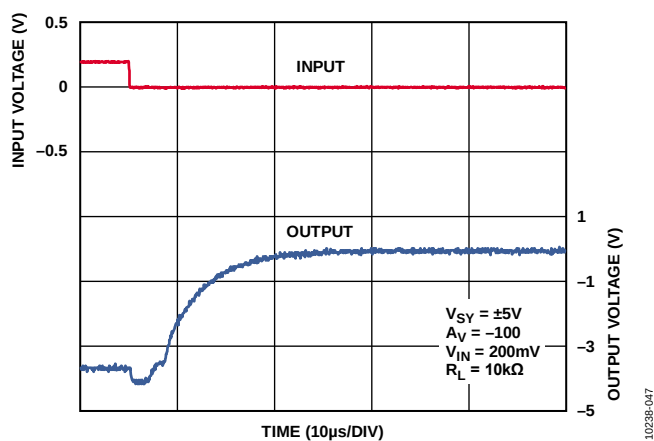


Figure 44. Negative Overload Recovery

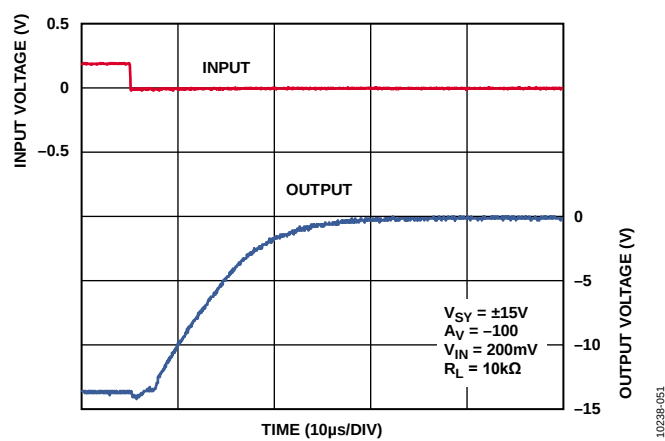


Figure 47. Negative Overload Recovery

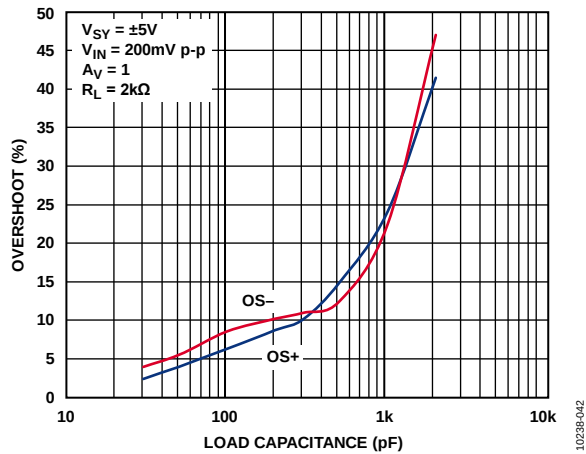


Figure 48. Small Signal Overshoot vs. Load Capacitance

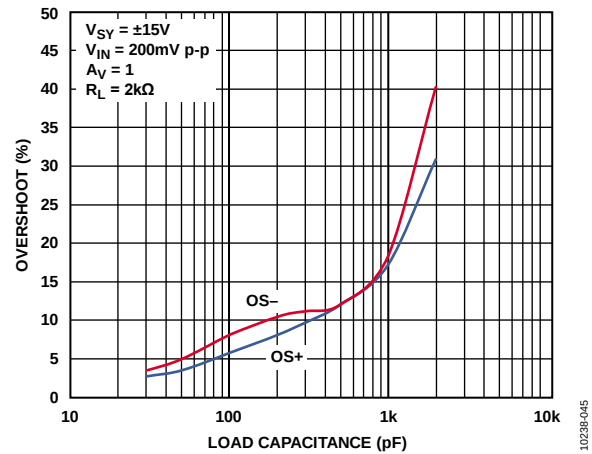


Figure 51. Small Signal Overshoot vs. Load Capacitance

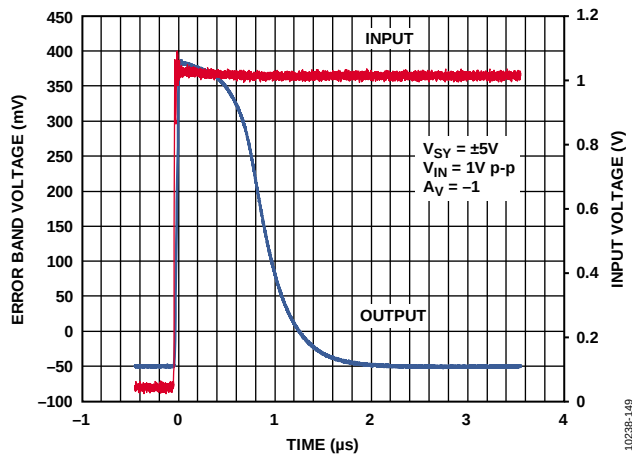


Figure 49. Positive Settling Time

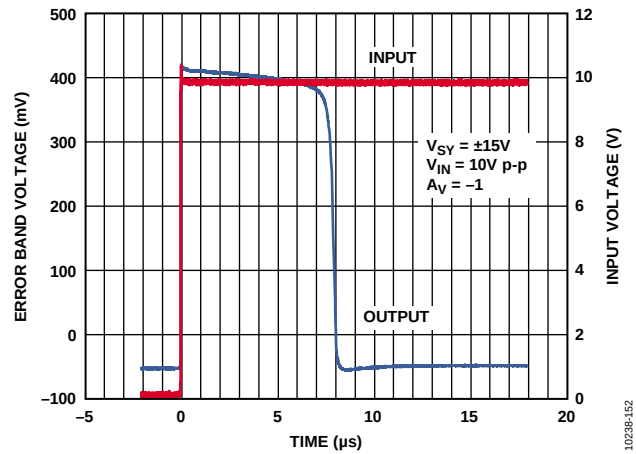


Figure 52. Positive Settling Time

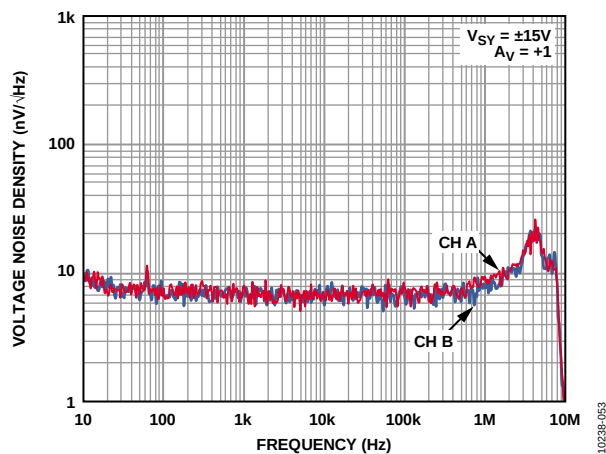


Figure 50. Voltage Noise Density vs. Frequency

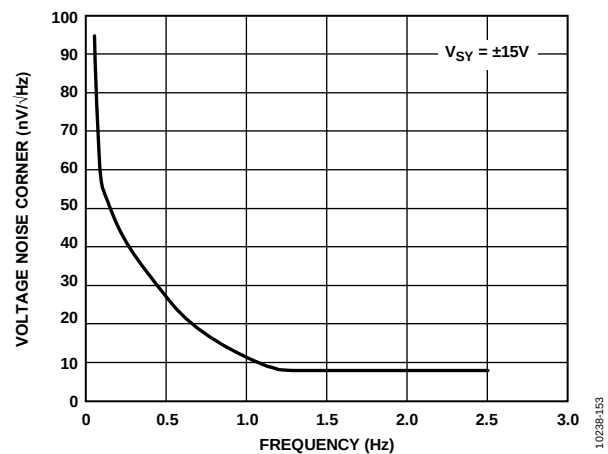


Figure 53. Voltage Noise Corner Frequency

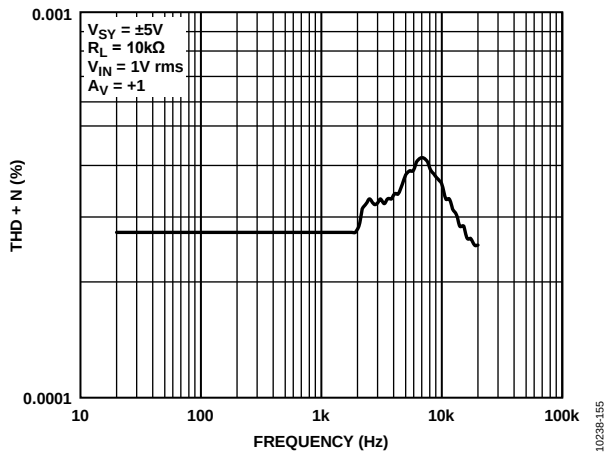


Figure 54. THD + N vs. Frequency

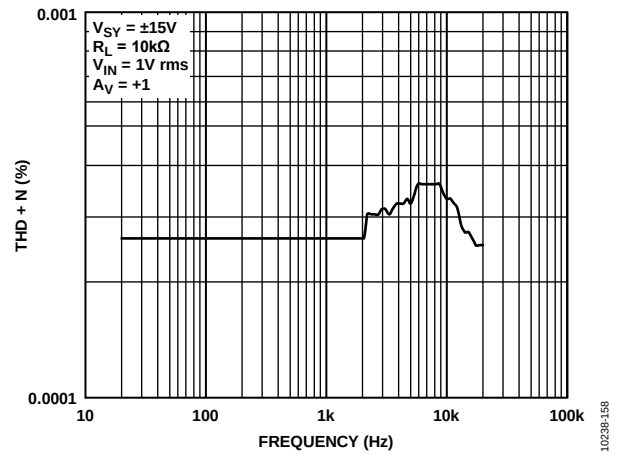


Figure 56. THD + N vs. Frequency

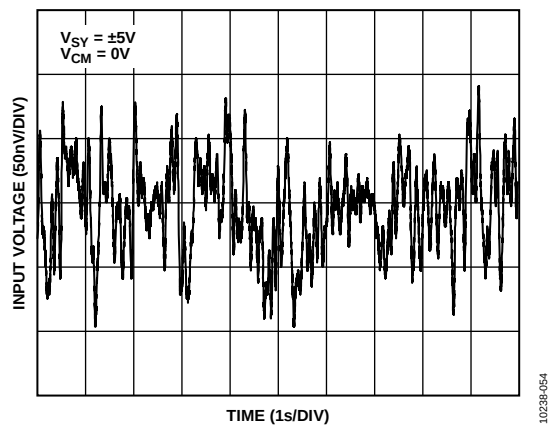


Figure 55. 0.1 Hz to 10 Hz Noise

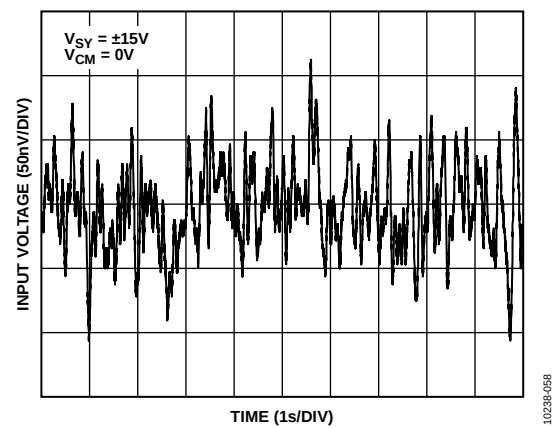


Figure 57. 0.1 Hz to 10 Hz Noise

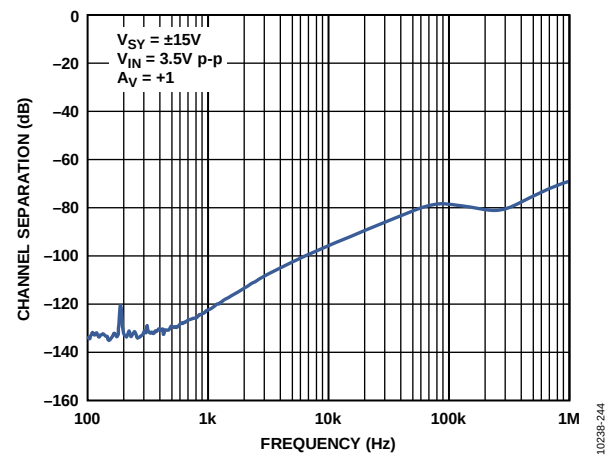


Figure 58. Channel Separation

THEORY OF OPERATION

The [ADA4077-2](#) is the sixth generation of the Analog Devices, Inc., industry-standard [OP07](#) amplifier family. The [ADA4077-2](#) is a high precision, low noise operational amplifier with a combination of extremely low offset voltage and very low input bias currents. Unlike JFET amplifiers, the low bias and offset currents are relatively insensitive to ambient temperatures, even up to 125°C.

The Analog Devices proprietary process technology and linear design expertise have produced a high voltage amplifier with superior performance to the [OP07](#), [OP77](#), [OP177](#), and [OP1177](#) in tiny, 8-lead SOIC and 8-lead MSOP packages. Despite its small size, the [ADA4077-2](#) offers numerous improvements, including low wideband noise, wide bandwidth, lower offset and offset drift, lower input bias current, and complete freedom from phase inversion.

The [ADA4077-2](#) has a specified operating temperature range of –40°C to +125°C with a MSL1 rating, which is as wide as any similar device in a plastic surface-mount package. This is increasingly important as PCB and overall system sizes continue to shrink, causing internal system temperatures to rise.

In the [ADA4077-2](#), power consumption is reduced by a factor of four from the [OP177](#), and bandwidth and slew rate have both increased by a factor of six. The low power dissipation and very stable performance vs. temperature also act to reduce warm-up drift errors to insignificant levels.

Inputs are protected internally from overvoltage conditions referenced to either supply rail. Like any high performance amplifier, maximum performance is achieved by following appropriate circuit and PCB guidelines.

PROPER BOARD LAYOUT

The [ADA4077-2](#) is a high precision device. To ensure optimum performance at the PCB level, care must be taken in the design of the board layout.

To avoid leakage currents, maintain a clean and moisture-free board surface. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

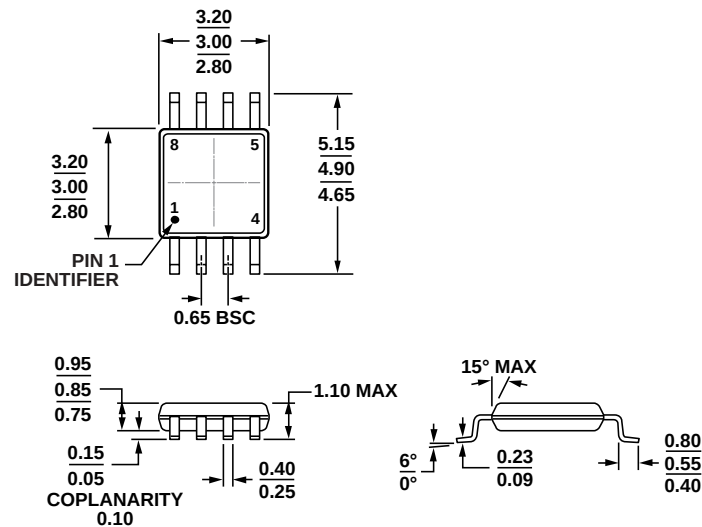
Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances caused by output current variation, such as when driving an ac signal into a heavy load. Connect bypass capacitors as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components, where possible, to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Place matching components in close proximity to each other and orient them in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and helps to maintain a constant temperature across the circuit board.

PACKAGING AND ORDERING INFORMATION

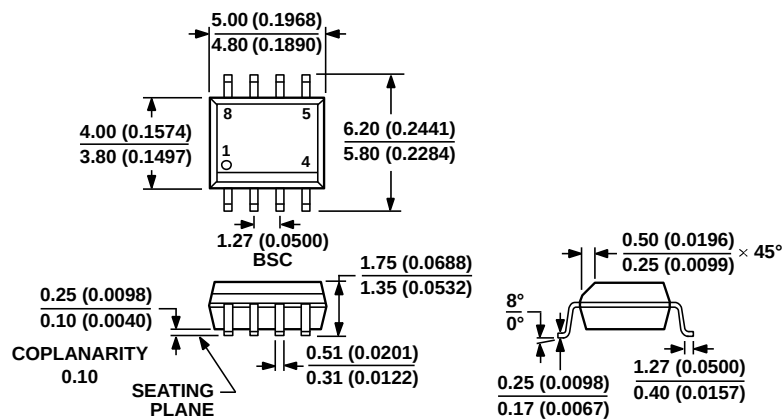
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 61. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 62. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADA4077-2-ARMZ	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARMZ-R7	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARMZ-RL	–40°C to +125°C	8-Lead Mini Small Outline Package [MSOP]	RM-8	A2X
ADA4077-2ARZ	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARZ-R7	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2ARZ-RL	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ-R7	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4077-2BRZ-RL	–40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

¹ Z = RoHS Compliant Part.

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

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- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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