15 GHz Ultra – Variable Broadband Prescaler

Features

- Wide Operating Range: 0.05 - 15 GHz
- Variable Divide Ratios: 2 to 220
- Single-Ended and/or Differential Drive
- High Input Sensitivity
- Size: 6mm x 6mm
- Single -3.3 V Power Supply
- Low SSB Phase Noise:
  - 153 dBc @ 10 kHz

Description

The MX1DS10P is a broadband 0.05GHz to 15GHz prescaler with a variable divide ratio between 2 and 1048576 (=220). All inputs and outputs are DC coupled using CML logic levels. The IC used in this part is manufactured in an advanced Silicon Germanium (SiGe) process. The part requires a single 3.3V supply and measures only 6mm x 6mm.

Application

The MX1DS10P is ideal for phase locked loops and other synthesizers requiring large and variable divide ratios. Other applications include trigger generation for high-speed measurement systems. The MX1DS10P can be employed in high frequency phase locked loops that can take advantage of the low 1/f noise of SiGe HBT's. General purpose test instrumentation systems will also benefit from the high input sensitivity and broad frequency range.

Pad Metallization

The QFN package pad metallization consists of a 300-800 micro-inch (typical thickness 435 micro-inch or 11.04um) 100% matte Sn plate. The plating covers a Cu (C194) leadframe. The packages are manufactured with a >1hr 150C annealing/heat treating process, and the matte (non-glossy) plating, specifically to mitigate tin whisker growth.

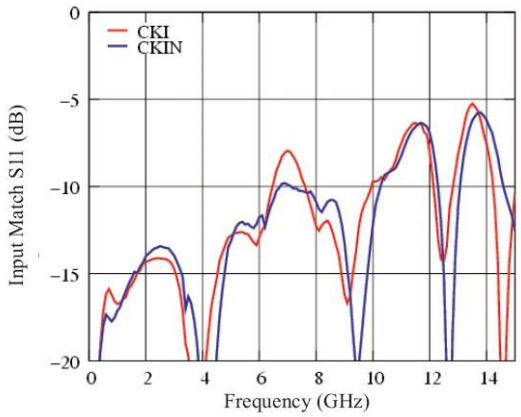
Key Specifications (T = 25˚C):
Vee = -3.3 V, Iee = 430 mA, Zo=50 Ω

Parameter	Description	Min	Typ	Max
Clkin (GHz)	Input Clock Frequency	0.05	-	15
Clkpwr (dBm)	Input Clock Power Max	-	-	10
Clkpwr (dBm)	Input Clock Power Min	-	-10	-
Dout (Vppk)	Output Voltage Swing	0.05	1	-
θjc (ºC/W)	Junction-Case Thermal Resistance	-	13	-

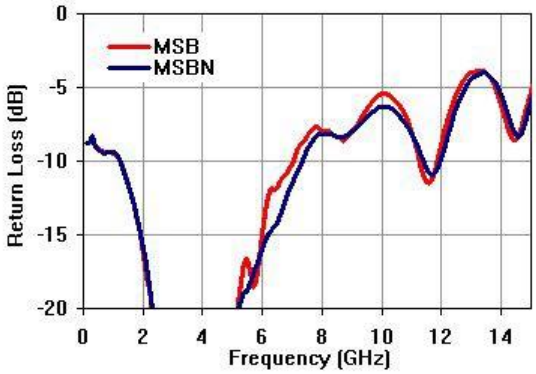
Parameter	Description	Min	Typ	Max
S11 (dB)	Input Match (Typical)	-12	-7	-5
S22 (dB)	Output Match (Typical)	-7	-5	-3

Frequency Divider Application

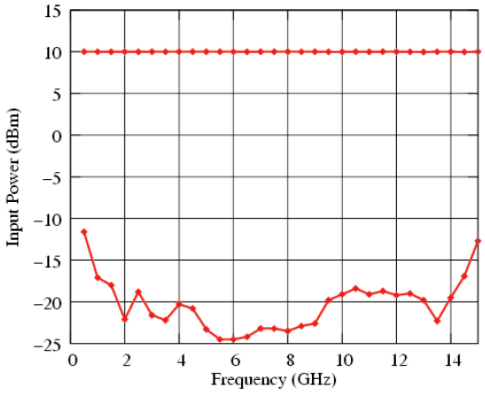
Return Loss of Differential Input Ports



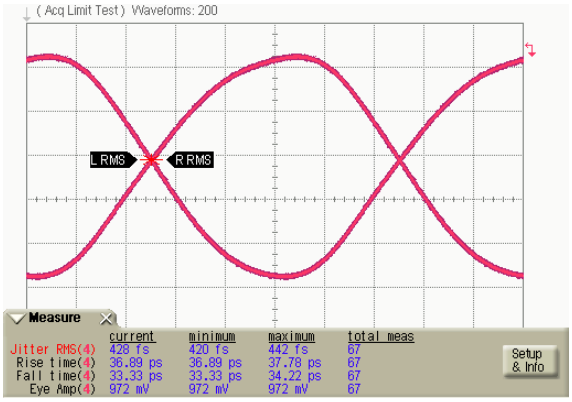
Return Loss of Differential Output Ports



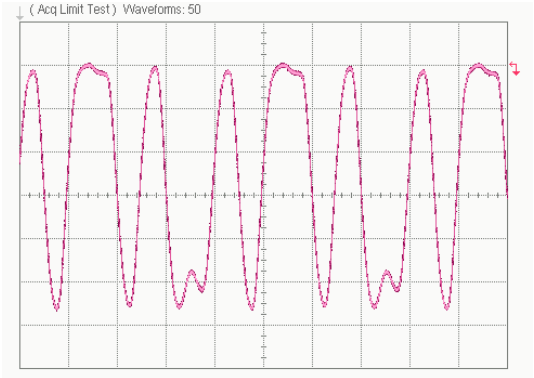
Input Sensitivity Window



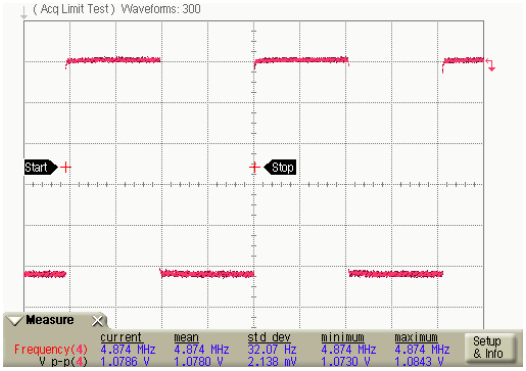
Divide-by-2 Output (Input: 10 GHz; Output: 5 GHz)



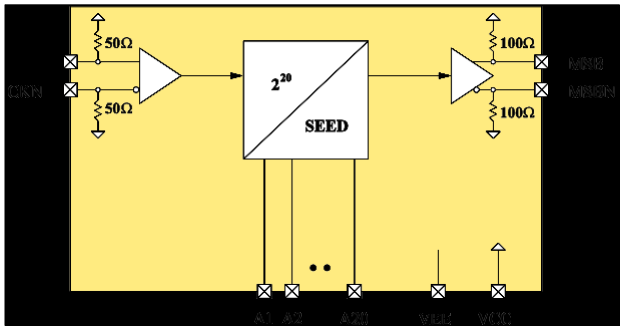
Divide-by-(8/3) Output (Input: 10 GHz; Output: 3.75 GHz)



Divide-by-2048 Output (Input: 10 GHz; Output: 4.9 MHz)



Functional Block Diagram



SEED = A1 + (A2 x 2^1) + (A3 x 2^2) + …….+ (A20 x 2^{19}) (Maximum valid SEED = 2^{19})

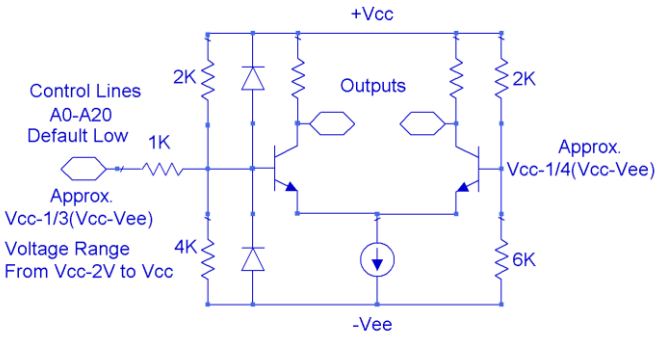
Divide Ratio = 2^{20} / SEED (Lowest valid divide ration = 2)

$Freq_{out}$ = $Freq_{clk}$ / (Divide Ratio)

Table 1: Pin Description

Port Name	Description	Notes
CK	Clock Input, Positive Terminal	CML signal levels
CKN	Clock Input, Negative Terminal	CML signal levels
MSB	Divided Output, Positive Terminal	CML signal levels
MSBN	Divided Output, Negative Terminal	CML signal levels
A1,A2…A20	Divide Ratio Selectors	Divide ratio = Value of the binary seed A1…A20
VCC	RF & DC Ground	-
VEE	-3.3 V @ 400 mA	Negative Supply Voltage
Paddle	Backside of die	Must be connected to good heatsink (see text)

Simplified Control Logic Schematic



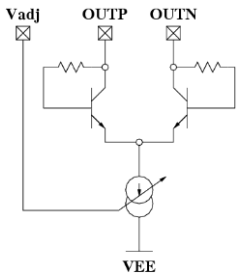
Application Notes

Divider Outputs:

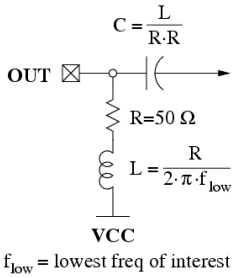
The equivalent circuit of the divider outputs is shown below. The outputs require a DC return path capable of handling ~35 mA per side. If DC coupling is employed, the DC resistance of the receiving circuits should be ~50 Ω (or less) to VCC to prevent excessive common mode voltage from saturating the prescaler outputs. If AC coupling is used, the perfect embodiment is shown in figure 2. The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.

The output amplitude can be adjusted over a 1.5:1 range by one of the two methods The Vadj pin voltage can be set to VCC for maximum amplituded or VCC-1.3 V for an amplitude ~2/3 the max swing. Voltages between these two values will produce a linear change in output swing. Alternatively, users can use a 1k potentiometer or fixed resistor tied between Vadj and VCC. Resistor values approaching 0 ohms will lead to the maximum swing, while values approaching 1k will lead to the minimum output swing. Users who only need/want the maximum swing should simply tie Vadj to VCC.

Equivalent Circuit of Output Buffer



Recommended Circuit for AC Coupled Outputs



Low Frequency Operation:

Low frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to ~50 MHz due to the 10 dBm max input power limitation.

The values of the coupling capacitors for the high-speed inputs and outputs (I/O's) are determined by the lowest frequency the IC will be operated at.

$$C >> \frac{1}{2 \bullet \pi \bullet 50\Omega \bullet f_{lowest}}$$

For example to use the device below 30 kHz, coupling capacitors should be larger than 0.1uF.

Package Heatsink:

The package backside provides the primary heat conduction path and should be attached to a good heatsink on the PC board to maximize performance. User PC boards should maximize the contact area to the package paddle and contain an array of vias to aid thermal conduction to either a backside heatsink or internal copper planes.

IC Assembly:

The device is designed to operate with either single-ended or differential inputs. Figures 1, 2 & 3 show the IC assembly diagrams for positive and negative supply voltages. In either case the supply should be capacitively bypassed to the ground to provide a good AC ground over the frequency range of interest. The backside of the chip should be connected to a good thermal heat sink.

All RF I/O's are connected to VCC through on-chip termination resistors. This implies that when VCC is not DC grounded (as in the case of positive supply), the RF I/O's should be AC coupled through series capacitors unless the connecting circuit can generate the correct levels through level shifting.

ESD Sensitivity:

Although SiGe IC's have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling.

Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 400V.

CML Logic Levels for DC Coupling (T=25˚C):

Assuming 50 Ω Terminations at Inputs and Outputs

Parameter			Minimum	Typical	Maximum
Input	Differential	Logic $Input_{high}$	Vcc	Vcc	Vcc
		Logic $Input_{low}$	Vcc - 0.05 V	Vcc - 0.3 V	Vcc - 1 V
	Single	Logic $Input_{high}$	Vcc + 0.05 V	Vcc + 0.3 V	Vcc + 1 V
		Logic $Input_{low}$	Vcc - 0.05 V	Vcc - 0.3 V	Vcc - 1 V
Output	Differential & Single	Logic $Input_{high}$	Vcc	Vcc	Vcc
		Logic $Input_{low}$	Vcc – 0.2 V	Vcc – 0.3 V	Vcc – 0.6 V

Differential versus Single-Ended:

The MX1DS10P is fully differential to maximize signal-to-noise ratios for high-speed operation. All high speed inputs and outputs are terminated to Vcc with on-chip resistors (refer to functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to V max to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

$$I\ Vdm/2 + Vcm\ I < Vcc \geq Vmax$$

where Vdm is the differential input signal and Vcm is the common-mode voltage.

In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC value of the waveform at IC should be equal to Vcc for single-ended operation. In practice, this is easily achieved with a single capacitor on the input acting as a DC block. The value of the capacitor should be large enough to pass the lowest frequencies of interest. Use the positive terminals for single-ended operation while terminating the negative terminal to Vcc.

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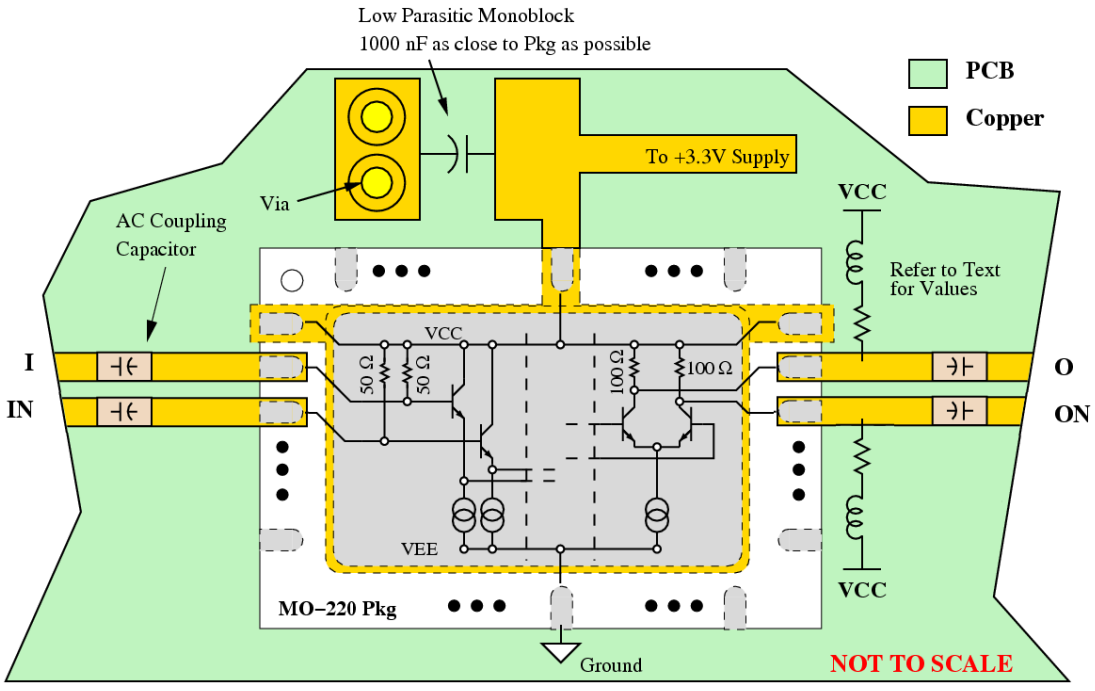
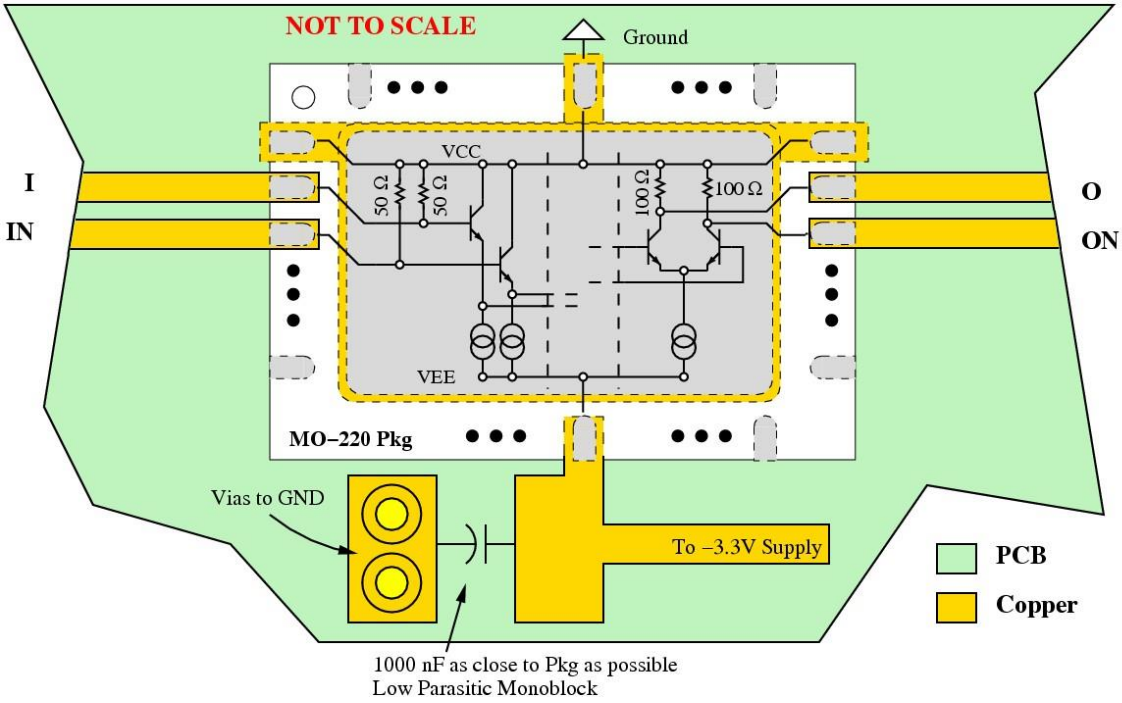
Note that a potential oscillation mechanism exists if both inputs are static and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations. Tying unused inputs directly to Vcc shorts out the internal 50Ω bias resistor, imposing a DC offset sufficient to prevent oscillations. Driving the differential inputs with DC blocks, or driving the single-ended inputs without terminating unused inputs, is not recommended without taking additional steps to eliminate the potential oscillation issues.

Positive Supply (AC Coupling)



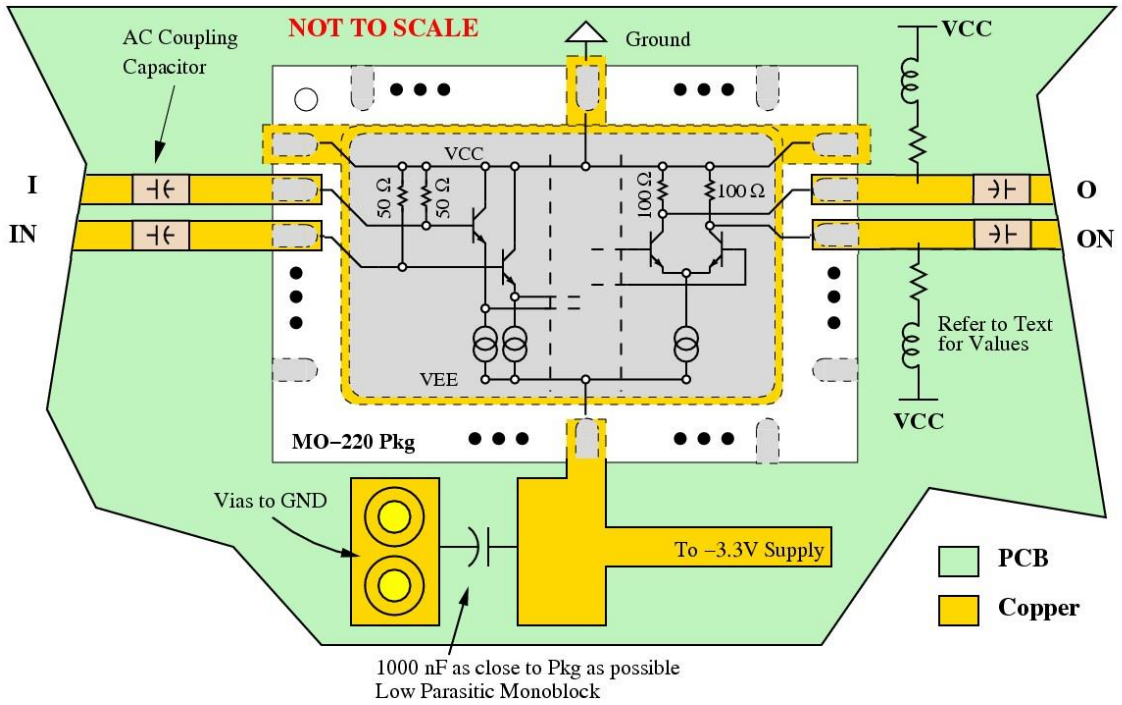
Biasing recommendations for positive supply with AC coupling applications

Negative Supply (DC Coupling)



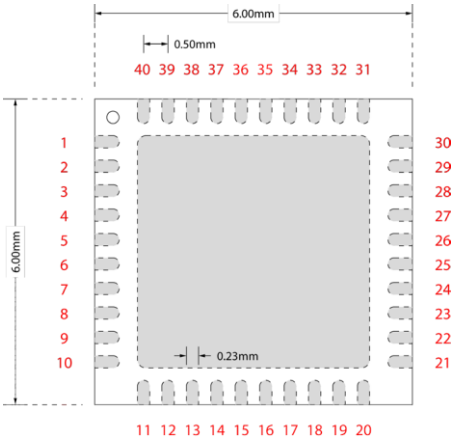
Biasing recommendations for negative supply with DC coupling applications

Negative Supply (AC Coupling)



Biasing recommendations for negative supply with AC coupling applications

MX1DS10P Physical Characteristics



Pkg size:	6.00 x 6.00 mm
Pkg size tolerance:	+/- 0.25 mm
Pkg thickness:	0.9 +/- 0.1 mm
Pad dimensions:	0.23 x 0.4 mm
Center paddle:	4.20 x 4.20 mm
JEDEC designator:	MO-220

Top View

Table 2: MX1DS10P Pin Definition

	Function	Notes
5,14,22,26,37 (Vcc)	RF and DC Ground	0 V
1,6,9,13,17,27,34 (Vee)	Negative Supply Voltage	Nominally -3.3 V
31,32,35,36	-	No Connection
2 (A4)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
3 (A5)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
4 (A6)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
7 (CKN)	Clock Input	Negative Terminal of differential input
8 (CK)	Clock Input	Positive Terminal of differential Input
10 (A7)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
11 (A8)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
12 (A9)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
15 (A10)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
16 (A11)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
18 (A12)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
19 (A13)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
20 (A14)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
21 (A15)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
23 (A16)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
24 (A17)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
25 (A18)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
28 (MSBN)	Divider Output	Negative Terminal of differential output
29 (MSB)	Divider Output	Positive Terminal of differential output
30 (A19)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
33 (A20)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
38 (A1)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
39 (A2)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
40 (A3)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1

Table 3: Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage (Vcc-Vee)	4	V
RF Input Power (CK,CKN)	10	dBm
Max DC Voltage Level (MSB, MSBN)	Vcc+1 V	V
Min DC Voltage Level (MSB, MSBN)	Vcc-1V	V
Max DC Voltage Level (A1,A2,…A20)	Vcc	V
Min DC Voltage Level (A1,A2,…A20)	Vee	V
Operating Temperature	-40 to 85	ºC
Storage Temperature	-85 to 125	ºC
Junction Temperature	125	ºC

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