MAX35104 Gas Flow Meter SoC

General Description

The MAX35104 is a gas flow meter system-on-chip (SoC) targeted as an analog front-end solution for the ultrasonic gas meter and medical ventilator markets. With a time measurement accuracy of 700ps and automatic differential time of flight (TOF), the device makes for simplified computation of gaseous flow.

Power consumption is the lowest available with ultra-low 62µA time-of-flight measurement and 125nA duty-cycled temperature measurement. Multi-hit (up to six per wave) capability with stop-enable windowing allows the device to be fine-tuned for the application. Internal analog switches, a configurable three-stage integrated operational amplifier chain amplifier, and an ultra-low input offset comparator provide the analog interface and control for a minimal electrical bill of material solution. A programmable high-voltage (up to 30V) pulse launcher provides up to 19dB of transducer launch amplitude adjustment to compensate for transducer aging and temperature, pressure, humidity affects. Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements. Built-in arithmetic logic unit provides TOF difference measurements and programmable receiver hit accumulators to minimize the host microprocessor access. For temperature measurement, the device supports a single 2-wire PT1000 platinum resistive temperature detector (RTD) or NTC thermistor. A simple 4-wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

Applications

- Ultrasonic Gas Meters
- Medical Ventilators

Benefits and Features

- High Accuracy Flow Measurement for Billing and Leak Detection
  - Time-to-Digital Accuracy Down to 700ps Measurement Range Up to 8ms
  - 2 Channels: Single-Stop Channel
- High Accuracy Temperature Measurement for Precise Flow Calculations
  - One 2-Wire Sensor: PT1000, PT500 RTD, and Thermistor Support
- Maximizes Battery Life with Low Device and Overall System Power
  - Ultra-Low 62µA TOF Measurement and 125nA Duty-Cycled Temperature Measurement
  - Event Timing Mode with Randomizer Reduces Host µC Overhead to Minimize System Power Consumption
  - 2.3V to 3.6V Single-Supply Operation
- High Integration Solution Minimizes Parts Count and Reduces BOM Cost
  - Built-In Real-Time Clock
  - Small, 5mm x 5mm, 40-Pin TQFN Package
  - -40°C to +85°C Operation

***Ordering Information* appears at end of data sheet.**

19-8501; Rev 3; 12/17

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

LIST OF FIGURES

LIST OF TABLES

LIST OF TABLES (continued)

Absolute Maximum Ratings

(Voltage relative to ground.)
Voltage Range on V_{CC} Pins .... -0.5V to +4.0V
Voltage Range on All Other
Pins (not to exceed 4.0V) .... -0.5V to (V_{CC} + 0.3V)
Voltage Range on High Voltage Pins 32V
Continuous Power Dissipation (T_A = +70ºC)
TQFN (derate 35.70mW/ºC above +70ºC) 2857.10mW

Operating Temperature Range .... -40ºC to +85ºC
Junction Temperature .... +150ºC
Storage Temperature Range .... -55ºC to +125ºC
Soldering Temperature (reflow) .... +260ºC
Lead Temperature (soldering, 10s) .... +300ºC
ESD Protection (All Pins, Human Body Model) .... ±500V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .... 28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .... 2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Recommended Operating Conditions

(T_A = -40°C to +85°C, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		2.3	3.3	3.6	V
Input Logic 1 ($\overline{RST}$, CSW, SCK, DIN, $\overline{CE}$)	V_{IH}		V_{CC} x 0.7		V_{CC} + 0.3	V
Input Logic 0 ($\overline{RST}$, CSW, SCK, DIN, $\overline{CE}$)	V_{IL}		-0.3		V_{CC} x 0.3	V
Input Logic 1 (32KX1)	$V_{IH32KX1}$		V_{CC} x 0.85		V_{CC} + 0.3	V
Input Logic 0 (32KX1)	$V_{IL32KX1}$		-0.3		V_{CC} x 0.15	V

Electrical Characteristics

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage (CSW, $\overline{RST}$, SCK, DIN, $\overline{CE}$, $\overline{CIP}$, $\overline{CIN}$)	I_L		-0.1		+0.1	µA
Output Leakage ($\overline{INT}$, $\overline{WDO}$, T1,T2)	O_L		-0.1		+0.1	µA
Output Voltage Low (32KOUT)	V_{OL32K}	2mA			0.2 x V_{CC}	V
Output Voltage High (32KOUT)	V_{OH32K}	-1mA	0.8 x V_{CC}			V
Output Voltage High (DOUT, CMP_OUT/UP_DN)	V_{OH}	-4mA	0.8 x V_{CC}			V
Output Voltage High (TC)	V_{OHTC}	V_{CC} = 3.6V, I_{OUT} = -4mA	3.4			V
Output Voltage Low ($\overline{WDO}$, $\overline{INT}$, DOUT, MP_OUT/UP_DN)	V_{OL}	4mA			0.2 x V_{CC}	V
Pulldown Resistance (TC)	R_{TC}	ITC	650	1000	1750	Ω

Electrical Characteristics (continued)

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Low (TC)	V_{ILTC}			0.36 x V_{CC}		V
Pulldown (RXP, RXN)		AFE_BP = 0, pins disabled		80		µA
Resistance (T1, T2)	R_{ON}			1.5		Ω
Input Capacitance ($\overline{CE}$, SCK, DIN, $\overline{RST}$, CSW)	C_{IN}	Not tested		7		pF
$\overline{RST}$ Low Time	t_{RST}				100	ns
CURRENT						
Standby Current	I_{DDQ}	No oscillators running			10	µA
32kHz OSC Current	I_{32KHZ}	32kHz oscillator only, V_{CC} = 3.6V		0.42	1	µA
4MHz OSC Current	I_{4MHZ}	4MHz oscillator only, V_{CC} = 3.6V		82	135	µA
Time Measurement Unit Current	I_{CCTMU}	V_{CC} = 3.3V		4.3	8	mA
Calculator Current	I_{CCCPU}			1.2	3	mA
Device Current Drain	I_{CC}	V_{CC} = 3.3V, TOF_DIFF = 2 per second, temperature = 1 per 30 seconds		62		µA
TRANSMITTER: BOOST SWITCHER						
Output Voltage Range				9 30		V
Programmable Output Voltage Step Size				1.7		V
Output Switching Frequency			100		200	kHz
Current-Limit Trip Level	V_{CS-SW}		100	150	200	mV
TRANSMITTER: FET GATE DRIVER						
External FET Gate Charge	Q_G				2	nC
Rise Time	t_R	C_L = 1nF (Figure 2, Note 3)		100		ns
Fall Time	t_F	C_L = 1nF (Figure 2, Note 3)		100		ns
TRANSMITTER: HIGH-VOLTAGE REGULATOR						
Output Voltage Range		Low		5.4		V
Output Voltage Range		High		26.4		V
Programmable Output Voltage Step Size				1.7		V
Output Voltage Accuracy				5		%
Load Regulation		I_{LOAD} = 15mA		150		mV

Electrical Characteristics (continued)

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER: PIEZO DRIVER						
Driver Output Resistance Pulling Down (n-Channel)	$R_{ON-N-PD}$	V_{IN} = 10V, I_{LD} =10mA		50		Ω
Driver Output Resistance Pulling Up (p-Channel)	$R_{ON-P-PU}$	V_{IN} = 10V, I_{LD} =10mA		50		Ω
Output Leakage Current	I_{LK-PD}			0.05		µA
Rise Time	t_{R-PD}	C_L = 1nF		100		ns
Fall Time	t_{F-PD}	C_L = 1nF		100		ns
FILTER SPECIFICATION						
Input Amplitude			1		10	mV
Differential Input Impedance				4		kΩ
Programmable Gain Resolution	Per bit			1.5		dB
COMPARATOR SPECIFICATION						
Input Offset Voltage	V_{OFFSET}	C_OFFSETUP or C_OFFSETDN register programmed to 00h		2		mV
Input Offset Step Size	V_{STEP}			1		mV
Receiver Sensitivity	V_{SENS}	Stop hit detect level	10			mV_{P-P}
ANALOG RECEIVER: BANDPASS FILTER						
Center Frequency Accuracy	f_{0A}	f = 200kHz		6		%
Q Range				4		Hz/Hz
				12		
Q Accuracy				20		%
200kHz PERFORMANCE						
A1 Differential Gain		200kHz, V_{IN} = $6mV_{P-P}$		10		V/V
UP/DN Gain Match				±1		%

Electrical Characteristics (continued)

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER		SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGA Gain	PGA[3:0] = 0000b		V_{OUT} = 600mV_{P-P}	V_{IN} = 19.0mV_{P-P}		3.16		V/V
	PGA[3:0]= 0001b			V_{IN} = 16.3mV_{P-P}		3.69		
	PGA[3:0]= 0010b			V_{IN} = 14.0mV_{P-P}		4.30		
	PGA[3:0]= 0011b			V_{IN} = 12.0mV_{P-P}		5.01		
	PGA[3:0]= 0100b			V_{IN} = 10.3mV_{P-P}		5.84		
	PGA[3:0]= 0101b			V_{IN} = 8.80mV_{P-P}		6.81		
	PGA[3:0]= 0110b			V_{IN} = 7.55mV_{P-P}		7.94		
	PGA[3:0]= 0111b			V_{IN} = 6.48mV_{P-P}		9.26		
	PGA[3:0]= 1000b			V_{IN} = 5.56mV_{P-P}		10.8		
	PGA[3:0]= 1001b			V_{IN} = 4.76mV_{P-P}		12.6		
	PGA[3:0]= 1010b			V_{IN} = 4.09mV_{P-P}		14.7		
	PGA[3:0]= 1011b			V_{IN} = 3.51mV_{P-P}		17.1		
	PGA[3:0]= 1100b			V_{IN} = 3.02mV_{P-P}		20.0		
	PGA[3:0]= 1101b			V_{IN} = 2.58mV_{P-P}		23.3		
	PGA[3:0]= 1110b			V_{IN} = 2.21mV_{P-P}		27.1		
	PGA[3:0]= 1111b			V_{IN} = 1.90mV_{P-P}		31.6		
Filter Gain at 200kHz Trim			V_{IN} = 19mV_{P-P}			1.0		V/V
Filter Gain with Bypass			V_{IN} = 19mV_{P-P}			0.01		V/V

Electrical Characteristics (continued)

(V_{CC} = +2.3V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V and T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIME MEASUREMENT UNIT						
Measurement Range	t_{MEAS}	Time of flight	4		8000	µs
Time Measurement Accuracy	t_{ACC}	Differential time measurement		700		ps
Time Measurement Resolution	t_{RES}			3.8		ps
EXECUTION TIMES						
Power-On-Reset Time		V_{CC} MIN to POR bit set		275		µs
Case Switch Time		CSW pin logic-high until CSWI bit set		20		ns
CAL Command Time		Command received until CAL bit set		1.25		ms
SERIAL PERIPHERAL INTERFACE (Figure 1 and Figure 2)						
DIN to SCK Setup	t_{DC}				20	ns
SCK to DIN Hold	t_{CDH}			2	20	ns
SCK to DOUT Delay	t_{CDD}			5	20	ns
SCK Low Time	t_{CL}	$V_{CC} \geq 3.0V$	25	4		ns
		V_{CC} = 2.3V	50	30		
SCK High Time	t_{CH}		25	4		ns
SCK Frequency	t_{SCK}				20	MHz
SCK Rise and Fall	t_R, t_F				10	ns
$\overline{CE}$ to SCK Setup	t_{CC}			5	40	ns
SCK to $\overline{CE}$ Hold	t_{CCH}				20	ns
$\overline{CE}$ Inactive Time	t_{CWH}			2	40	ns
$\overline{CE}$ to DOUT High Impedance	t_{CCZ}			5	40	ns

Note 2: All voltages are referenced to ground. Current entering the device are specified as positive and currents exiting the device are negative.

Note 3: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Recommended External Crystal Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
32kHz Nominal Frequency	f_{32K}			32.768		kHz
32kHz Frequency Tolerance	$\Delta f_{32K}/f_{32K}$	25°C	-20		+20	ppm
32kHz Load Capacitance	C_{L32K}			12.5		pF
32kHz Series Resistance	R_{S32K}				70	kΩ
4MHz Crystal Nominal Frequency	f_{4M}			4.000		MHz
4MHz Crystal Frequency Tolerance	$\Delta f_{4M}/f_{4M}$	25°C	-30		+30	ppm
4MHz Crystal Loadapacitance	C_{L4M}			12.0		pF
4MHz Crystal Series Resistance	R_{S4M}				120	Ω
4MHz Ceramic Nominal Frequency				4.000		MHz
4MHz Ceramic Frequency Tolerance		25°C	-0.5		+0.5	%
4MHz Ceramic Load Capacitance				30		pF

Timing Diagrams

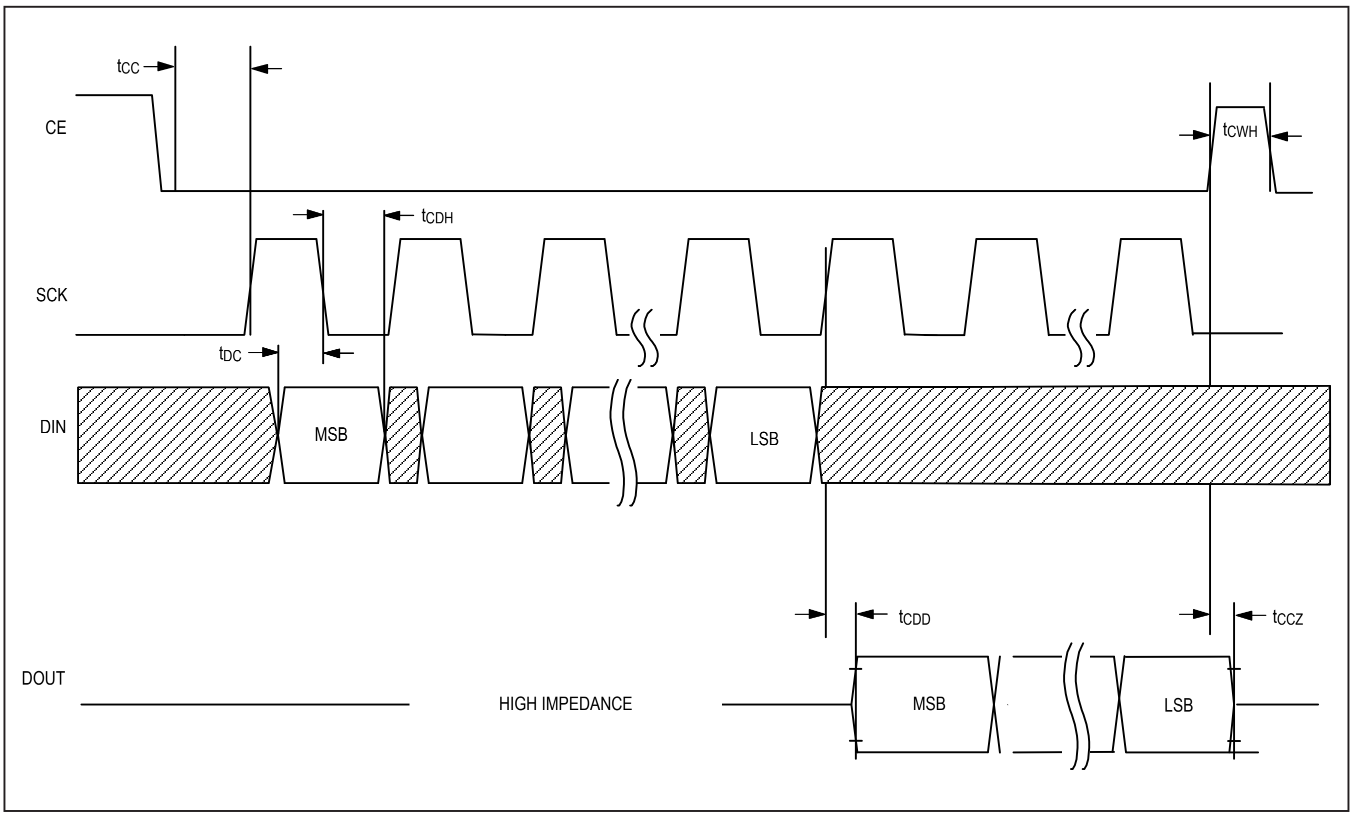


Figure 1. SPI Timing Diagram Read

Timing Diagrams (continued)

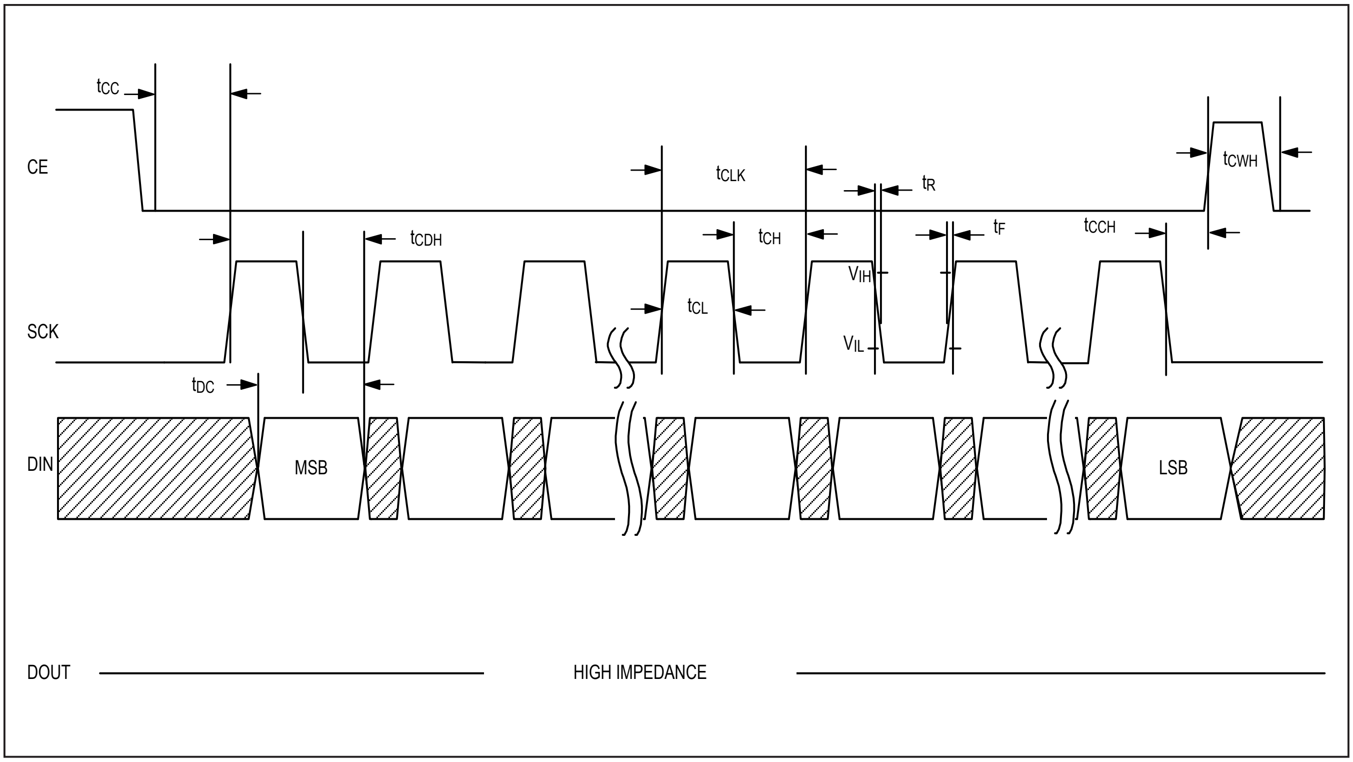
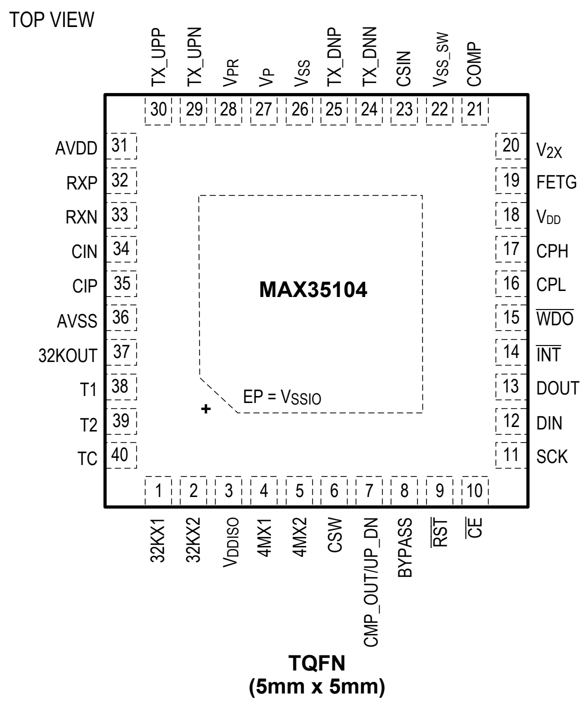


Figure 2. SPI Timing Diagram Write

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	32KX1	Connections for 32.768kHz Quartz Crystal, Connect a 12pF ceramic capacitor from each pin to ground. An external CMOS 32.768kHz signal can also drive the device. In this configuration, the 32KX1 pin is connected to the external signal and the 32KX2 pin is left unconnected.
2	32KX2	
3	V_{DDISO}	LDO Supply Voltage. This pin should be decoupled to V_{SSISO} with a 100nF ceramic capacitor (Note 1).
4	4MX1	Connections for 4MHz Quartz Crystal, connect a 12pF ceramic capacitor from each pin to ground. A ceramic resonator can also be used. An external CMOS 4MHz signal can also drive the device. In this configuration, the 4MX1 pin is connected to the external signal and the 4MX2 pin is left unconnected.
5	4MX2	
6	CSW	CMOS Digital Input Case Switch. Active high tamper detect input.
7	CMP_OUT/UP_DN	CMOS output that indicates the direction (upstream or downstream) of which the pulse launcher is currently launching pulses OR the comparator output (Note 2).
8	BYPASS	Connect this pin to ground with a 100nF ceramic capacitor to provide stability for the on-board low-dropout regulator. The effective series resistance of this capacitor needs to be in the range of 1Ω to 2Ω (Note 3).

Pin Description (continued)

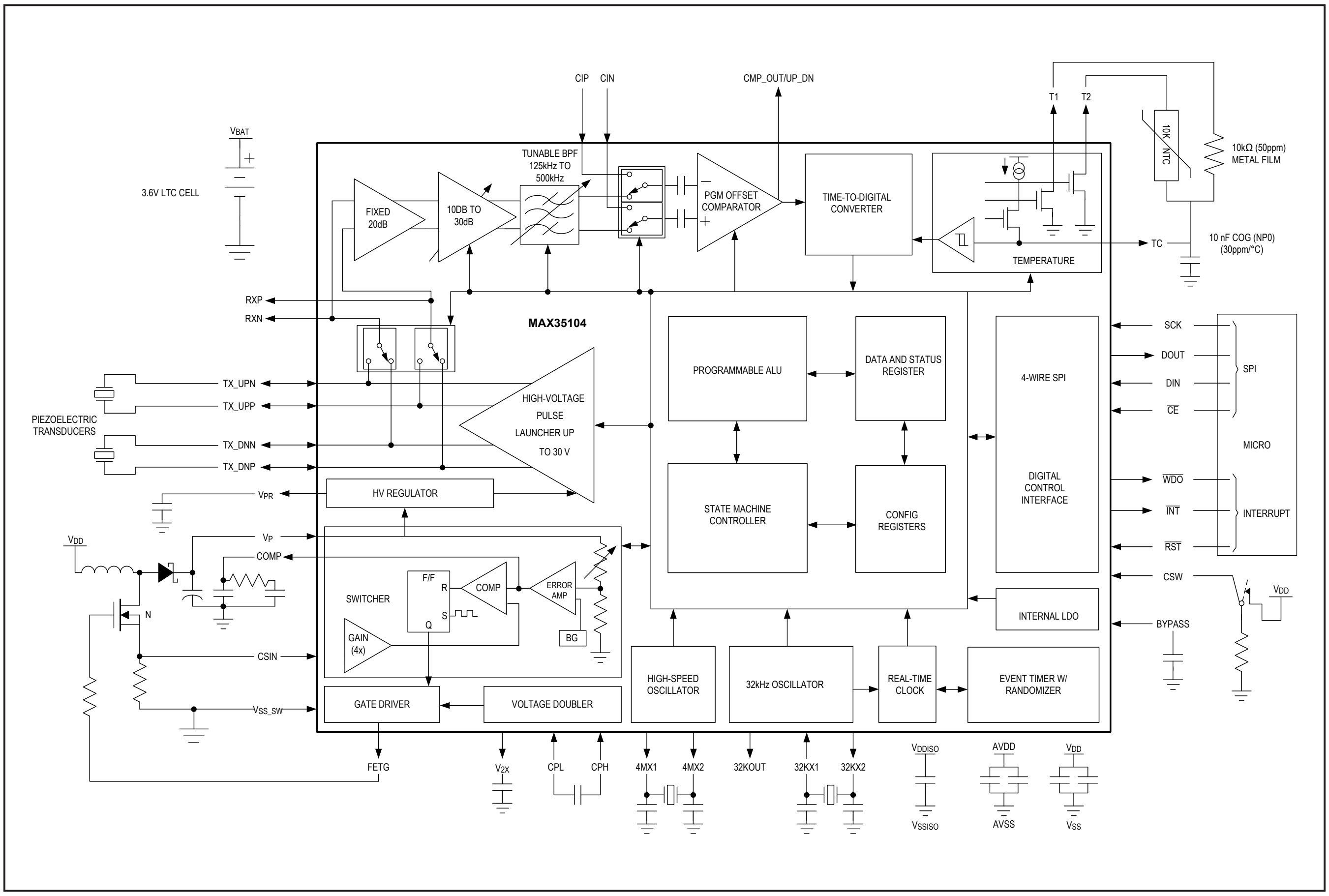
PIN	NAME	FUNCTION
9	$\overline{RST}$	Active-Low Reset (CMOS Digital Input). Performs the same function as a power-on reset (POR).
10	$\overline{CE}$	Active-Low Serial Peripheral Interface Chip Enable Input (CMOS Digital Input)
11	SCK	Serial Peripheral Interface Clock Input (CMOS Digital Input)
12	DIN	Serial Peripheral Interface Data Input (CMOS Digital Input)
13	DOUT	Serial Peripheral Interface Data Output (CMOS Output)
14	$\overline{INT}$	Active-Low, Open-Drain Interrupt Output. The pin is driven low when the device requires service from the host microprocessor.
15	$\overline{WDO}$	Active-Low, Open-Drain Watchdog Output. The pin is driven low when the watchdog counter reaches zero (if enabled).
16	CPL	Negative terminal of the flying capacitor for the voltage doubler. Connect this pin to CPH with a 100nF ceramic capacitor. (Note 4)
17	CPH	Positive terminal of the flying capacitor for the voltage doubler. Connect this pin to CPL with a 100nF ceramic capacitor. (Note 4,5)
18	V_{DD}	Supply Voltage. This pin should be decoupled to V_{SS} with a 100nF and a 22µF ceramic capacitor (Note 1).
19	FETG	PWM Modulated CMOS Gate Driver Output for External n-Channel Power Transistor used in the Boost Switcher. Place a 25Ω series resistor between this pin and the transistor gate.
20	V_{2X}	Connect this pin to ground with a 100nF ceramic capacitor to provide stability for the on-board voltage doubler (Notes 3, 4).
21	COMP	Error-Amplifier Output of Boost Converter. Connect the frequency-compensation network between COMP and AVSS. See Figure 6 (Notes 3, 4).
22	V_{SS_SW}	High-Current Ground Return for the Boost Switcher. Connect the current-sense resistor between this pin and CSIN+ (Note 4).
23	CSIN	Positive Analog Input to the Current-Sense Amplifier for the Boost Switcher. Connect the current-sense resistor between this pin and CSIN (Note 4).
24	TX_DNN	Connect to the negative terminal of the piezo transducer located downstream of the gas flow. Performs the launching and receiving functions required for a time-of-flight measurement. In the launch case, it is the negative output of the bridged differential output driver pair. In the receive case, it is the negative input of the analog differential return signal from the piezo transducer (Notes 2, 4).
25	TX_DNP	Connect to the positive terminal of the piezo transducer located downstream of the gas flow. Performs the launching and receiving functions required for a time-of-flight measurement. In the launch case, it is the positive output of the bridged differential output driver pair. In the receive case, it is the positive input of the analog differential return signal from the piezo transducer (Notes 2, 4).
26	V_{SS}	Ground Connection
27	V_P	Resulting High-Voltage Bias Generated by the Boost Switcher Circuit. Used as the supply for the high-voltage regulator and to generate the feedback voltage fed into the error-amplifier for closed loop control. (Notes 3, 4).

Pin Description (continued)

PIN	NAME	FUNCTION
28	V_{PR}	Connect this pin to ground with a 1μF ceramic capacitor to provide stability for the on-board high-voltage regulator. When the high-voltage regulator is not used and constantly disabled, short this pin to VP (Notes 3, 4).
29	TX_UPN	Connected to the negative terminal of the piezo transducer located upstream of the gas flow. Performs the launching and receiving functions required for a time-of-flight measurement. In the launch case, it is the negative output of the bridged differential output driver pair. In the receive case, it is the negative input of the analog differential return signal from the piezo transducer (Notes 2, 4).
30	TX_UPP	Connected to the positive terminal of the piezo transducer located upstream of the gas flow. Performs the launching and receiving functions required for a time-of-flight measurement. In the launch case, it is the positive output of the bridged differential output driver pair. In the receive case, it is the positive input of the analog differential return signal from the piezo transducer (Notes 2, 4).
31	AVDD	Analog Supply Voltage. This pin should be decoupled to AVSS with a 100nF ceramic capacitor (Note 1).
32	RXP	Do Not Connect (DNC) When Utilizing the Internal Analog Front-End. Positive analog output from the selected transducer's differential return signal. When used with the CIP pin provides a way to construct an external analog front-end (Note 5).
33	RXN	Do Not Connect (DNC) When Utilizing the Internal Analog Front-End. Negative analog output from the selected transducer's differential return signal. When used with the CIN pin provides a way to construct an external analog front-end (Note 5).
34	CIN	Do Not Connect (DNC) When Utilizing the Internal Analog Front-End. Negative analog input to the differential receive comparator. When used with the RXN pin provides a way to construct an external analog front-end (Note 5). OR negative analog output of selectable AFE stages (Note 2).
35	CIP	Do Not Connect (DNC) When Utilizing the Internal Analog Front-End. Positive analog input to the differential receive comparator. When used with the RXP pin provides a way to construct an external analog front-end (Note 5). OR positive analog output of selectable AFE stages (Note 2).
36	AVSS	Ground Connection
37	32KOUT	CMOS Output That Repeats the 32kHz Crystal Oscillator Frequency
38	T1	Open-Drain Probe 1 Temperature Measurement (Note 5)
39	T2	Open-Drain Probe 2 Temperature Measurement (Note 5)
40	TC	Input/Output Temperature Measurement Capacitor Connection (Note 5)
EP	V_{SSISO}	Exposed Pad, Ground Connection

Note 1: A +2.7V to +3.6V supply. Typically sourced from a single lithium cell.
Note 2: Dual functionality pin.
Note 3: Do not connect to additional non-recommended external circuitry.
Note 4: High-voltage tolerant.
Note 5: This pin can be left open circuit if not needed.

Block Diagram



Detailed Description

The MAX35104 is a gas flow meter SoC targeted as an analog front-end solution for the ultrasonic gas meter and medical ventilator markets. With a time measurement accuracy of 700ps and automatic differential Time-of-Flight measurement, the device makes for simplified computation of gaseous flow. Power consumption is the lowest available with ultra-low 62µA TOF measurement and 125nA duty-cycled temperature measurement.

Multihit (up to 6 per wave) capability with stop-enable windowing allows the device to be fine-tuned for the application. Internal analog switches, a configurable 3-stage integrated operational amplifier chain amplifier, and an ultra-low input offset comparator provide the analog interface and control for a minimal electrical bill of material solution. A programmable high-voltage (up to 30V) pulse launcher provides up to 19dB of transducer launch amplitude adjustment to compensate for transducer aging and temperature, pressure, humidity affects.

Early edge detection ensures measurements are made with consistent wave patterns to greatly improve accuracy and eliminate erroneous measurements. A built-in arithmetic logic unit provides TOF difference measurements and programmable receiver hit accumulators to minimize the host microprocessor access. For temperature measurement, the device supports a single 2-wire PT1000 platinum resistive temperature detector (RTD) or NTC thermistor. A simple 4-wire SPI interface allows any microcontroller to effectively configure the device for its intended measurement.

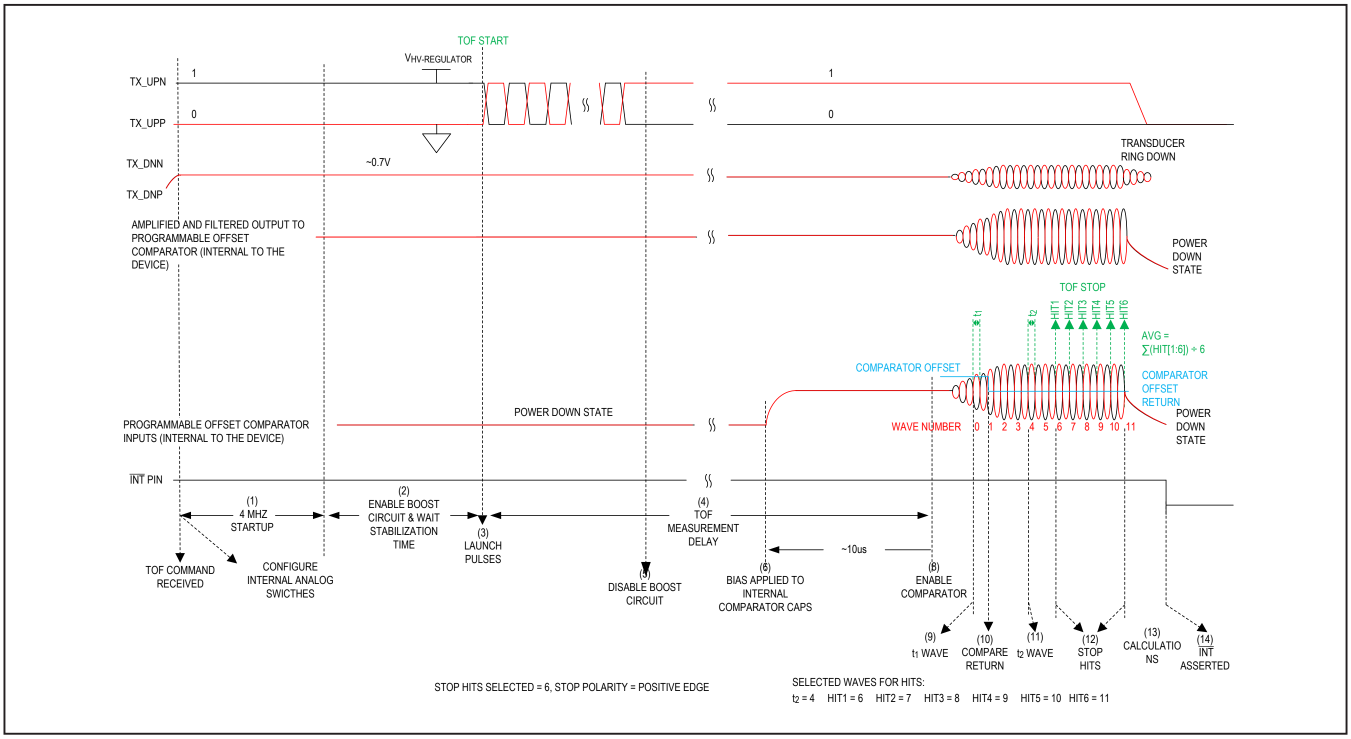


Figure 3. Time-of-Flight Up Measurement Sequence

Time-of-Flight (TOF) Measurement Operations

TOF is measured by launching pulses from one piezo-electric transducer and receiving the pulses at a second transducer. The time between when the pulses are launched and received is defined as the time of flight. The device contains the functionality required to create a string of pulses, sense the receiving pulse string, and measure the time of flight. The device can measure two separate TOFs, which are defined as TOF Up and TOF Down.

A TOF Up measurement has pulses launched from the TX_UPN and TX_UPP pins, which is connected to the downstream transducer. The ultrasonic pulse is received at the upstream transducer, which is connected to the TX_DNN and TX_DNP pins. A TOF Down measurement has pulses launched from the TX_DNN and TX_DNP pins, which is connected to the upstream transducer. The ultrasonic pulse is received at the downstream transducer, which is connected to the TX_UPN and TX_UPP pins.

TOF measurements can be initiated by sending either the TOF_UP, TOF_DN, or TOF_DIFF commands. TOF_DIFF measurements can also be automatically executed using Event Timing Mode commands EVTMG1 or EVTMG2.

The steps involved in a single TOF measurement are described below and labeled in Figure 3.

1) The 4MHz oscillator and LDO is enabled with a programmable settling delay time set by the CLK_S[2:0] bits in Calibration and Control register.
2) The boost circuit is enabled and attempts to reach the targeted set output voltage. Once at the target voltage, the stabilization time to wait before moving to the next step is set by the ST[3:0] bits in the Switcher 2 register.
3) The pulse launcher drives the appropriate TX pins with a programmable sequence of pulses. The number of pulses launched is set by the PL[7:0] bits in the TOF1 register. The frequency of these 50% duty-cycle pulses is set by the DPL[3:0] bits, also in the TOF1 register. The start of these launch pulses generates a start signal for the Time-to-Digital Converter (TDC) and is considered to be time zero for the TOF measurement. This is denoted in Figure 4.
4) After a programmable delay time set in TOF Measurement Delay register, the comparator and hit detector at the appropriate pins are enabled. This delay allows the receiver to start recording hits when the received wave is expected, eliminating possible false hits from noise in the system.
5) Once the pulse launcher has completed transmitting the sequence of pulses, the boost circuit is disabled.

6) A common mode bias is enabled on the internal capacitor connecting the output of the bandpass filter to the input of the programmable offset comparator. This bias charge time is fixed at approximately 10μs.
7) The comparator is enabled.
8) Stop hits are detected according to the programmed preferred edge of the acoustic signal sequence received at the appropriate pins according to the setting of the STOP_POL bit in the TOF1 register. When a wave received at the receiving pins exceeds the Comparator Offset Voltage, which is set in the TOF6 and TOF7 registers, this wave is detected and identified as wave number 0. The width of the wave's pulse that exceeds the Comparator Offset Voltage is measured and stored as the t_1 time.
9) The offset of the comparator then automatically and immediately switches to the Comparator Return Offset, which is set in the TOF6 and TOF7 registers.
10) The t_2 wave is detected and the width of the t_2 pulse is measured and stored as the t_2 time. The wave number for the measurement of the t_2 wave width is set by the T2WV[5:0] bits in the TOF2 register.
11) The preferred number of stop hits are then detected. For each hit, the measured TOF is stored in the appropriate HITxUPINT and HITxUPFrac or HITxDNINT and HITxDNFRAC registers. The number of hits to detect is set by the STOP[2:0] bits in the TOF2 register. The wave number to measure for each stop hit is set by the Hitx Wave Select bits in the TOF3, TOF4, and TOF5 registers.
12) After receiving all the programmed hits, the device calculates the average of the recorded hits and stores this to AVGUPINT and AVGUPFrac or AVGDNInt and AVGDNFrac. The ratio of t_1/t_2 and t_2/t_{IDEAL} are calculated and stored in the WVRUP or WVRDN register.
13) Once all the hit data, wave ratios, and averages become available in the Results registers, the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled) and remains asserted until the Interrupt Status register is accessed by the microprocessor with a Read register command.

The computation of the total time of flight is performed by counting the number of full and fractional 4MHz clock cycles that elapsed between the launch start and a hit stop as shown in Figure 4.

Table 1. Two's Complement TOF_DIFF Conversion Example

REGISTER VALUE		CONVERTER VALUE
TOF_DIFFInt (hex)	**TOF_DIFFFrac (hex)**	**TOF DIFF Value (ns)**
7FFF	FFFF	8,191,999.9962
001C	0403	7,003.9177
0001	00A1	250.6142
0000	0089	0.5226
0000	0001	0.0038
0000	0000	0.0000
FFFF	FFFF	-0.0038
FFFF	FFC0	-0.2441
FFFE	1432	-480.2780
FF1C	8001	-56,874.9962
8000	0000	-8,192,000.0000

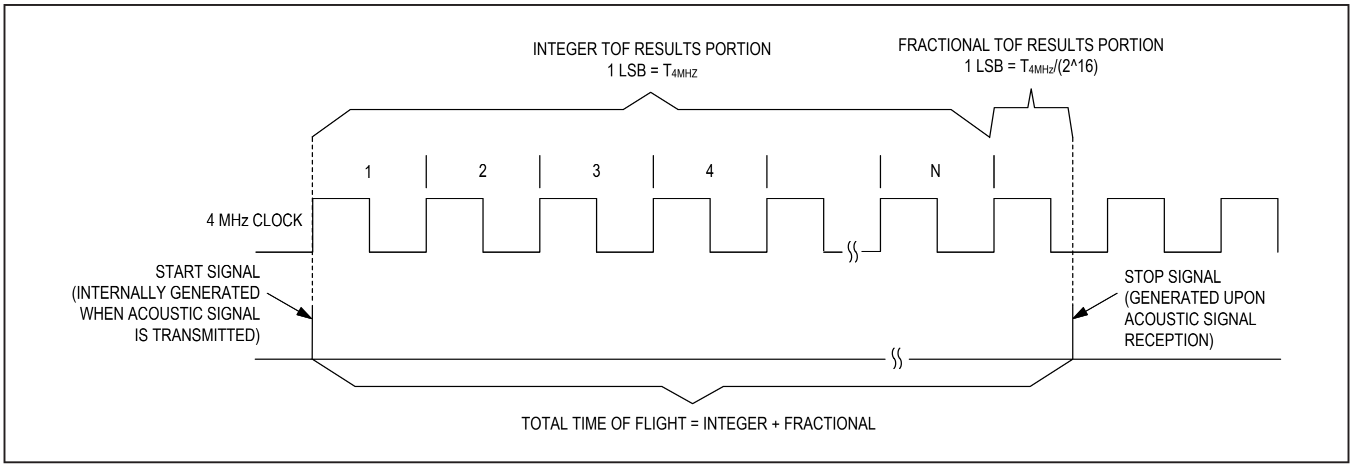


Figure 4. Start/Stop for Time-to-Digital Timing

Each TOF measurement result is comprised of an integer portion and a fractional portion. The integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHz}$ or ~ 8.19ms. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/2^{16} \times t_{4MHz}$. or ~ 249.9961 ns.

Pulse Echo TOF Mode

The device also has a pulse echo mode of operation. This mode allows time-of-flight measurements to be taken when only one transducer is used. The sole transducer transmits the high-voltage pulses and then receives the return signal. The time-of-flight measurement operation acts exactly as described in steps 1–13 except that the common mode of the AFE is applied to the same pins that transmitted the high-voltage pulses (Figure 5A).

The resulting data from the measurement is reported in the same manner as described in the TOF_UP, TOF_DOWN, or TOF_DIFF sections depending upon which command was executed.

The pulse echo mode is enabled by setting the PECHO bit in the Switcher 2 Register.

Early Edge Detect

The Early Edge Detect method of measuring the TOF of acoustic waves is used for all the TOF commands including TOF_UP, TOF_DN, and TOF_DIFF. This method allows the device to automatically control the input offset voltage of the receiver comparator so that it can provide advanced measurement accuracy. The input offset of the receiver comparator can be programmed with a range +127 LSBs if triggering on a positive edge and -127 LSBs if triggering on a negative edge, with 1 LSB = $V_{CC}/3072$. Separate input offset settings are available for the Upstream received signal and the Downstream received signal. The input offset for the Upstream received signal is programmed using the C_OFFSETUP[6:0] bits in the TOF6 register,. The input offset for the Downstream received signal is programmed using the C_OFFSETDN[6:0] bits in the TOF7 register. Once the first hit is detected, the time t_1 equal to the width of the earliest detectable edge is measured. The input offset voltage is then automatically and immediately returned to a preprogrammed comparator offset value. This return offset value has a range of +127 LSB's to -128 LSB's in 1 LSB steps and is programmed into the C_OFFSETUPR[7:0] bits in the TOF6 register for the Upstream received signal and programmed into the C_OFFSETDNR[7:0] bits in the TOF7 register. This preprogrammed comparator offset return value is provided to allow for common-mode shifts that can be present in the received acoustic wave.

The device is now ready to measure the successive hits. The next selected wave that is measured is the t_2 wave. In the example in Figure 5B, this is the 7th wave after the Early Edge Detect wave. The selection of the t_2 wave is made with the T2WV[5:0] bits in the TOF2 register.

With reference to Figure 5B, the ratio t_1/t_2 is calculated and registered for the user. This ratio allows determination of abrupt changes in flow rate, received signal strength, partially filled tube detection, and empty tube. It also provides noise suppression to prevent erroneous edge detection. Also, the ratio t_2/t_{IDEAL} is calculated and registered for the user. For this calculation, t_{IDEAL} is one-half the period of launched pulse. This ratio adds confirmation that the t_2 wave is a strong signal, which provides insight into the common mode offset of the received acoustic wave.

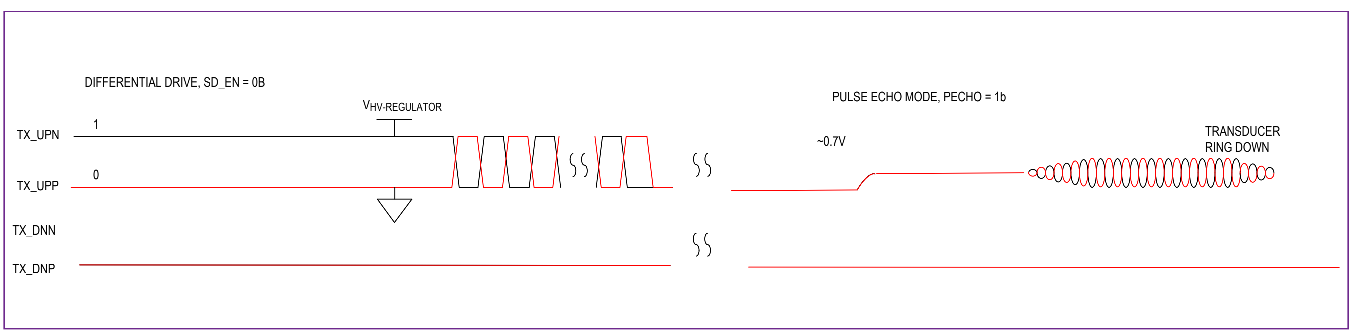


Figure 5A. Pulse Echo Measurement Mode

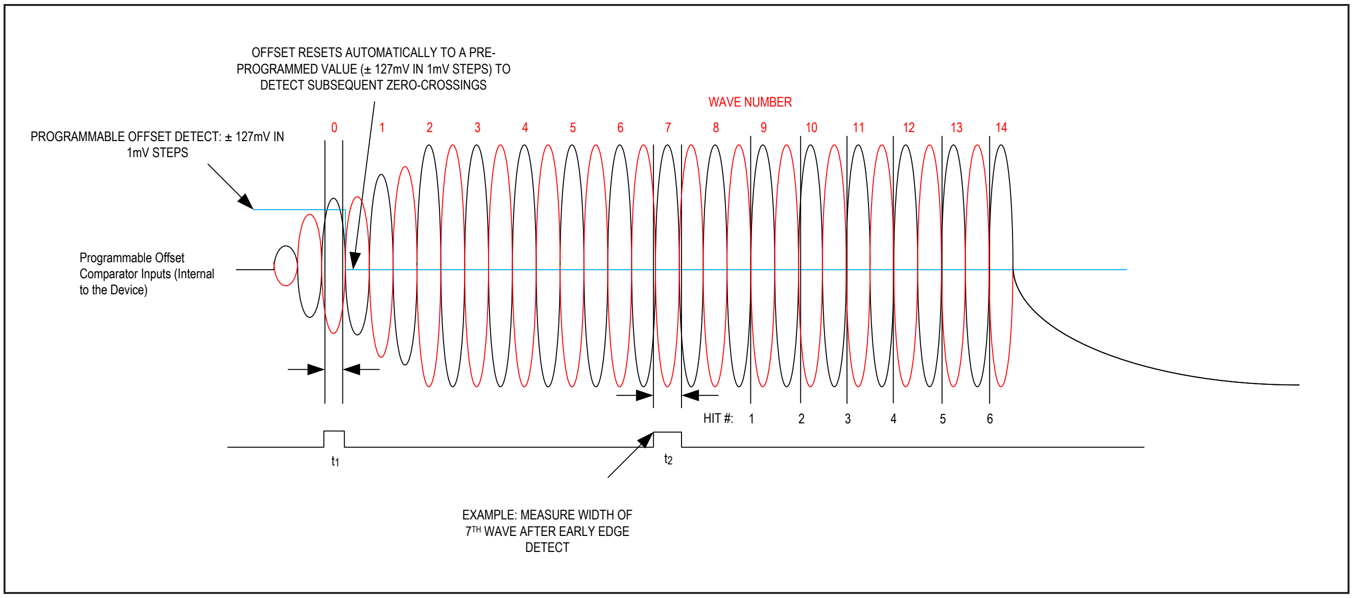


Figure 5B. Early Edge Detect Received Wave Example

TOF Error Handling

Any of the TOF measurements can result in an error. If an error occurs during the measurement, all the associated registers report FFFFh. If a TOF_DIFF is being performed, the TOF_DIFFInt and TOF_DIF_Frac registers report 7FFFh and FFFFh, respectively. The TOF_DIFF_AVG Results registers do not include the error measurement. If the measurement error is caused by the time measurement exceeding the timeout set by the TIMOUT[2:0] bits in the TOF2 register, then the TO bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ device pin is asserted (if enabled).

Step-Up DC-DC Controller

In order to increase the power transferred to the transducers during a launch sequence which is required to counteract the high attenuation factors for ultrasonic waves in gaseous mediums the device contains an integrated DC-DC Step-Up controller designed to operate in discontinuous-conduction mode (DCM boost). The controller provides adjustable-output voltage operation including programmable stabilization times with built in under voltage monitoring. The MAX35104's integrated gate driver utilizes the onboard voltage double in order to drive an external N-channel MOSFET's gate from ground to 2 x V_{DD}. The controller uses an external sense resistor to control the peak inductor current and operates at adjustable switching frequencies.

The integrated boost controller in enabled and disabled automatically by the device. The logic enables the boost before executing a time of flight command and disables the boost once the transmit pulse train is complete, see example timing in the Figure 3. The boost is disabled upon completion of the transmit pulses in order to reduce overall system power consumption as well as to eliminate any controller switching noise that would be introduced during the return signal's timing measurements.

Control and Operation

The switching frequency of the controller is programmable from 100kHz to 200kHz in 4 steps set by the SFREQ[1:0] bits in the Switcher 1 register. In order to set the output voltage the controller uses an outer loop feedback topology along with a peak current mode inner loop control.

The controller's outer loop targets an output voltage from 9V to 30V based on the programmed value set by the VS[3:0] bits in the Switcher 1 register. An internal error amplifier creates a control voltage, which generates a duty-modulated signal to control the operation of the internal gate driver used to switch the external MOSFET.

Additionally, the MOSFET's source needs an external current sense resistor, which feeds back the inductor's current per cycle as a voltage and compares with the error amplifier's output to further adjust the duty-modulated signal, thus forming an inner loop.

The controller has an undervoltage comparator that determines if the target output voltage is at target voltage, considered power good, or undervoltage. If the output voltage is below target, the switcher operates in startup limit mode that is determined by user selectable peak current limit set by the LT_S[3:0] bits in the Switcher 2 register. This is essentially a slew rate control on how fast the boost powers up and can be used to control the current signatures seen by the supply battery. After the output voltage crosses the undervoltage threshold, the switcher runs in normal duty mode. There is an additional optional peak current limit setting for the normal duty mode that is set by the LT_N[3:0] bits in the Switcher 2 register. Once in normal duty mode the device waits a programmable switcher stabilization time before a launch sequence begins. The stabilization time ensure that the controller has reaches a stable and repeatable output voltage each time it is powered. This time is set by the ST[3:0] bits in the Switcher 2 register. See Figure 6.

Compensation Component Values

In order to achieve standard operations the boost controller requires that proper loop compensation be applied to the error-amplifier output (COMP pin). The goal of the compensator design is to achieve the desired closed-loop bandwidth and sufficient phase margin at the crossover frequency of the open-loop gain-transfer function of the converter. The error amplifier included in the devices is a transconductance amplifier. Figure 6 shows the compensation network used to apply the necessary loop compensation for the example inductor and output capacitor values provided, where:

RZ = 22kΩ

CP = 470pF

CZ = 10nF

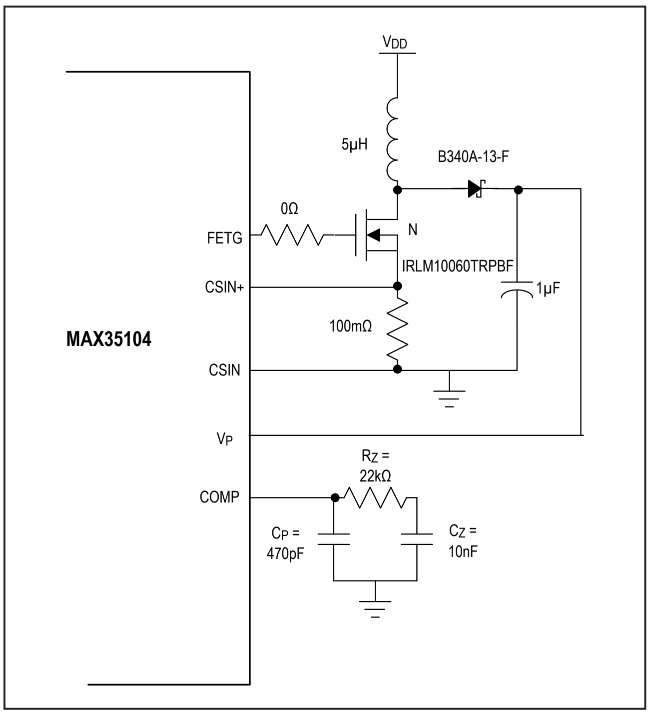


Figure 6. Boost Circuits Components

RSENSE

The external sense resistor value determines the peak allowable inductor current. For a given limit trim setting, LT_N[3:0] and LT_S[3:0] in the Switcher 2 register. Adjust the RSENSE value to adjust the peak allowable current. Select RSENSE based on the following criteria:

Resistor Value: Select an RSENSE resistor value in which the largest desired current would result in a 200mV full-scale current sense voltage. Assuming an LT_x setting of 0h, select RSENSE in accordance to the following equation and see Table 2 for examples:

RSENSE = 200mV/(Max Current)

Power Dissipation: Select a sense resistor that is rated for the max expected current and power dissipation (wattage). The sense resistor's value might drift if it is allowed to heat up excessively.

Kelvin Sense

For best performance, a Kelvin Sense arrangement is recommended for sense resistor as shown in Figure 7. In a Kelvin Sense arrangement, the voltage-sensing nodes across the sense element are placed such that they measure the true voltage drop across the sense element and not any additional excess voltage drop that can occur in the copper PCB traces or the solder mounting of the sense element. Routing the differential sense lines along the same path to the device and keeping the path short also improves the system performance. The analog differential current-sense traces should be routed close together to maximize common-mode rejection.

Power Transistor

Use an n-channel MOSFET power transistor with the MAX35104. To ensure the external n-channel MOSFET (nFET) is turned on hard, use logic-level or low-threshold nFETs such that the MAX35104's internal gate driver's 2 x V_{DD} supply voltage is sufficient for proper switching operation. nFETs provide the highest efficiency because they do not draw any DC gate-drive current. When selecting an nFET, three important parameters are the total gate charge (Qg), on-resistance ($R_{DS(ON)}$), and reverse transfer capacitance (CRSS).

Qg takes into account all capacitances associated with charging the gate. Use the typical Qg value for best results; the maximum value is usually grossly over specified since it is a guaranteed limit and not the measured value. The typical total gate charge should be 50nC or less. With larger numbers, the FETG pins may not be able to adequately drive the gate.

The two most significant losses contributing to the nFET's power dissipation are I^2R losses and switching losses. Select a transistor with low $r_{DS(ON)}$ and low CRSS to minimize these losses.

Determine the maximum required gate-drive current from the Qg specification in the nFET data sheet. The MAX35104's maximum allowed switching frequency is 200kHz, so the maximum current required to charge the nFET's gate is f(max) x Qg(typ). Use the typical Qg number from the transistor data sheet. For example, the Si9410DY has a Qg(typ) of 17nC (at V_{GS} = 5V), therefore, the current required to charge the gate is:

$$I_{GATE} (max) = (300kHz) (17nC) = 5.1mA$$

The bypass capacitor (C1) on the voltage double pin V2X must instantaneously furnish the gate charge without excessive droop (e.g., less than 200mV):

$$\Delta V2X = Qg/C1$$

Continuing with the example, $\Delta V+$ = 17nC/0.1µF = 170mV.

Figure 6 uses an IRLM10060TRPBF logic-level nFET with a guaranteed threshold voltage (V_{TH}) of 2.5V.

Table 2. RSENSE Example Values

RLIM (Ω)	LIMIT TRIM SETTING (STARTUP AND NORMAL)	CSIN TRIP VOLTAGE (V)	MAX CURRENT (A)
0.1	0	0.2	2
	1	0.4	4
	2	0.8	8
	4	1.6	16
0.25	0	0.2	0.8
	1	0.4	1.6
	2	0.8	3.2
	4	1.6	6.4
0.5	0	0.2	0.4
	1	0.4	0.8
	2	0.8	1.6
	4	1.6	3.2
1	0	0.2	0.2
	1	0.4	0.4
	2	0.8	0.8
	4	1.6	1.6
2	0	0.2	0.1
	1	0.4	0.2
	2	0.8	0.4
	4	1.6	0.8

Note: *The current must be large enough such that the switcher can reach its target output voltage (< 1s).*

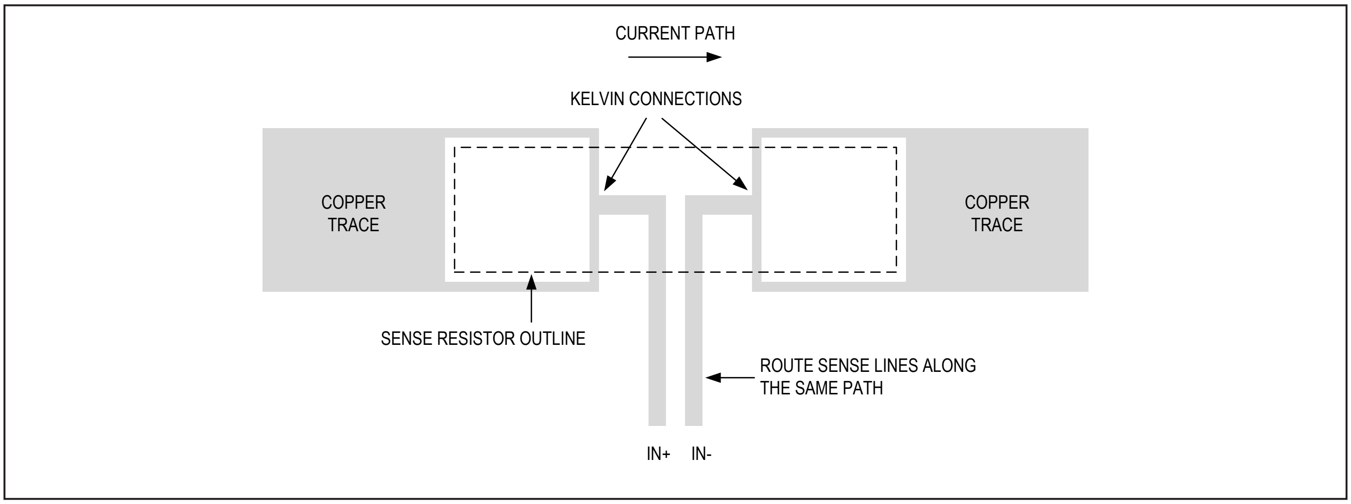


Figure 7. Kelvin Sense Connection Layout Example

Inductor (L)

Practical inductor values range from 5µH to 150µH. 56µH is a good choice for most applications. Larger inductance values tend to increase the startup time slightly, while smaller inductance values allow the coil current to ramp up to higher levels before the over current switch halts switching, increasing the ripple at light loads. Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. Make sure the inductor's saturation current rating (the current at which the core begins to saturate and the inductance starts to fall) exceeds the peak current rating set by R_{SENSE}. For highest efficiency, use a coil with low DC resistance, preferably under 20mΩ. To minimize radiated noise, use a toroid, a pot core, or a shielded coil.

Diode

The device high switching frequency demands a high-speed rectifier. Schottky diodes such as the B340A-13-F are recommended. Make sure the Schottky diode's average current rating exceeds the peak current limit set by R_{SENSE}, and that its breakdown voltage exceeds V_{OUT}.

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the ripple seen on the output voltage. Smaller-value and/or higher- ESR capacitors are acceptable for light loads or in applications that can tolerate higher output ripple. Since the output filter capacitor's ESR affects efficiency, use low-ESR capacitors for best performance.

Piezo Driver Regulator

The MAX35104 provides an internal high voltage low dropout linear regulator. The input to this regulator is the boost switcher's output and the output of the regulator supplies the high side bias used for the CMOS push pull high voltage transducer drivers. The regulator is used to provide a more stable higher bandwidth source from which the transducers can be driven. This helps mitigate any loading mismatches between the two transducers and provides a more repeatable launch signature between upstream and downstream measurements, ultimately reducing overall system error.

The high-voltage linear regulator operates from 5.4V to 27V in programmable 1.7V steps set by the VS[3:0] bits in the Switcher 1 register. There is an option to not use the high voltage regulator in the case where it is not desired and the switcher voltage is deem sufficient to drive the transducers. Disable the regulator with the HREG_EN bit in the Switcher 1 register. When disabled the VPR and VP pins must be externally shorted together.

When the regulator is enabled, its output is cycled off and on automatically by the device at the same time as the boost switcher, see example timing Figure 3.

Output Capacitor Selection

For stable operation over the full temperature range, use a low-ESR 1µF (min) 0805 ceramic output capacitor on the VPR pin. Ceramic capacitors exhibit capacitance and ESR variations over temperature. Ensure that the minimum capacitance under worst-case conditions does not drop below 1µF to ensure output stability. With a 1µF X7R dielectric, is sufficient at all operation temperatures.

Transducer Driver

The device has two integrated high voltage full-bridge transducer drivers, one for the upstream and one for the downstream transducer as shown in Figure 8. The drivers direct connect to the transducers without any external components required. The drivers can also be configured to drive the transducer in a single-ended manner. Set the single-ended drive enable bit, SD_EN, in the AFE 1 register. In this configuration, the negative terminal of the drivers are held at ground and the positive terminal is modulated between the high-voltage node and ground.

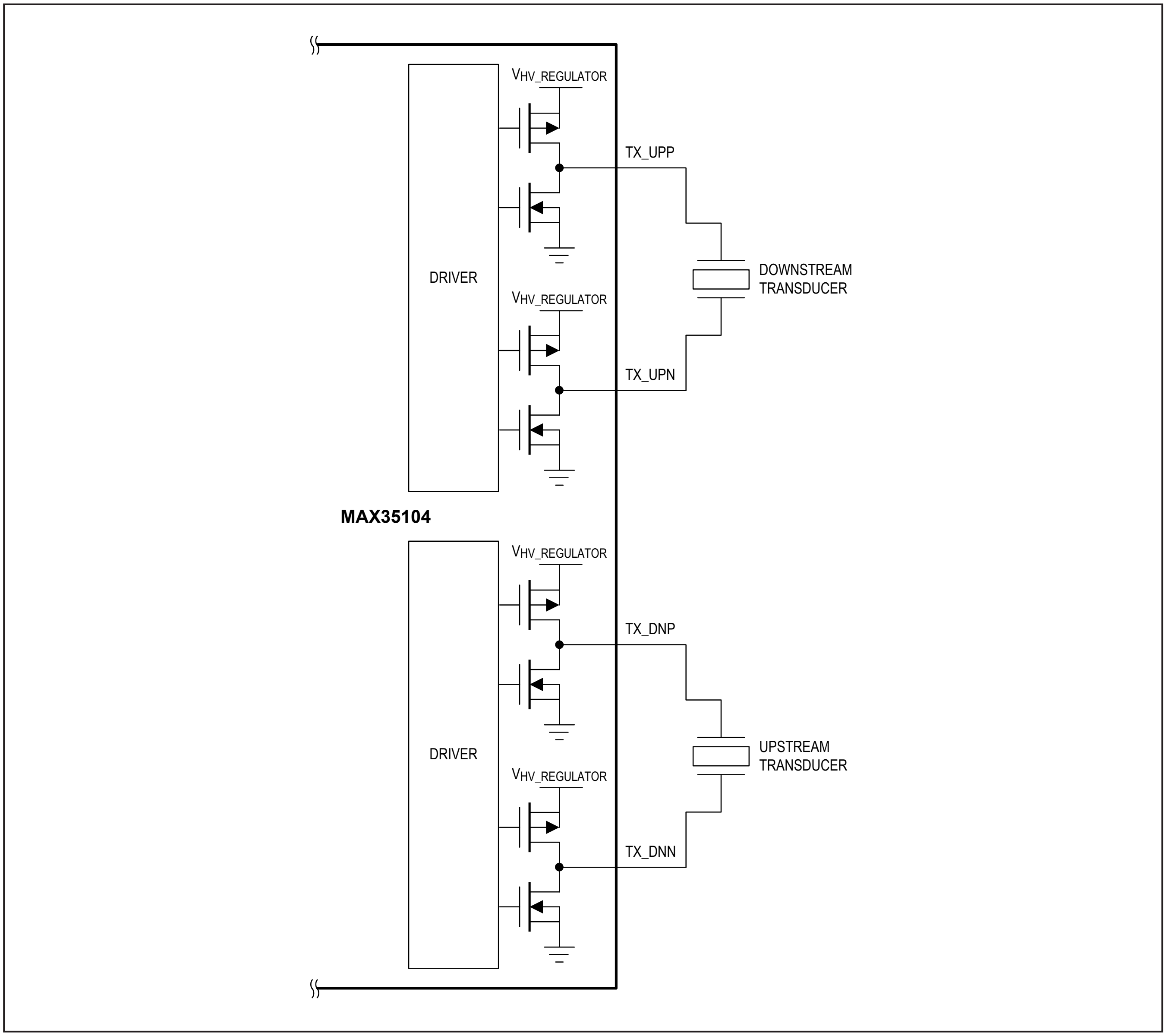


Figure 8. Piezo Driver Connection

Analog Front-End

The device has a programmable analog front-end used to condition the return signal before the signal is used to determine when the stop-hit timing should occur. This analog front-end consists of two amplifications stages, followed by a band pass filter, which feeds into the final comparator. The return signal is sampled differentially from the transducer. The entire AFE operates differentially all the way to the final comparator. By operating differently, the receive chain is less susceptible to noise injections applied to the common mode, providing an additional level of system accuracy and robustness.

The first stage is a fixed 20dB gain amplifier. An internal analog switch automatically connects the input of this amplifier to the appropriate receiving transducer. When enabled, the input is pulled to VBIAS ~0.7V through 2kΩ input resistance. The valid input range for the first amplification stage, and, therefore, the targeted return amplitude from the receiving transducer is 1mV to 10mV.

The second amplification stage is a programmable gain amplifier (PGA). The PGA is has a programmable range from 10 dB to 30dB in 1.33dB steps set by the PGA[3:0] bits in the AFE 1 register. Figure 9 shows the possible gain settings and input voltage amplitude combinations. The ideal input amplitude for the differential stop comparator is 350mV and therefore this should be the target for the output of the AFE. Table 3 shows ideals settings highlighted in green for all return signal amplitudes.

The bandpass filter is a 2-pole bandpass filter with programmable Q and center frequency. The Q of the filter can be adjusted with four programmable options in the range for 4.2 to 12 (Hz/Hz) set by the LOWQ[1:0] bits in the AFE 1 register. The center frequency is programmable from 125kHz to 500kHz in 3kHz steps set by the F0[6:0] bits in the AFE 2 register. The MAX35104 provides an integrated and automated center-frequency calibration routine that can be used to select and set the appropriate center frequency. To use this feature send the BYPASS_CALIBRATE command and wait until the complete bit is set. This routine performs the required calibration and automatically sets the F0 Adjust settings, bits F0[6:0] in the AFE 2 register to the correct value.

The bandpass filter can be bypassed as shown in Figure 9 by enabling the BP_BP bit in the AFE1 register. If the internal analog front-end is not required it can be completely bypassed by externally shorting the RNX/RXP pins to the CIN/CIP pins as shown in Figure 9 and setting the AFE_BYPASS bit in the AFE1 register. This allows for an external AFE to be constructed with external components. The CIN/CIP pins can also be used to output each stage of the AFE by setting the AFEOUT[1:0] bits in the AFE 2 register.

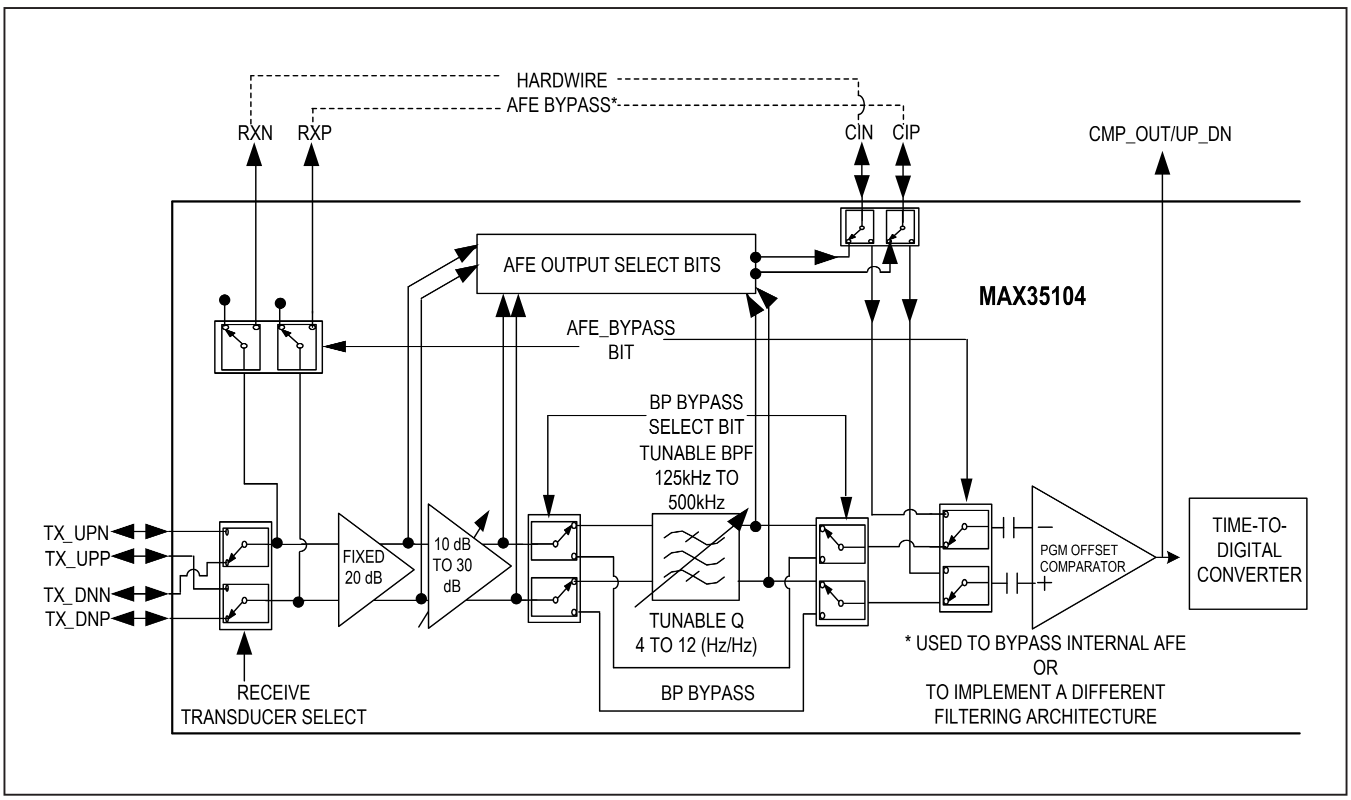


Figure 9. Analog Front-End

Table 3. Example Gain Settings

GAIN SETTINGS (V/V)	TRANSDUCER RECEIVE SIGNAL (V) 0.001	0.002	0.003	0.004	0.005	0.006	0.007	0.008	0.009	0.01
3.16	0.03	0.06	0.09	0.13	0.16	0.19	0.22	0.25	0.28	0.32
3.69	0.04	0.07	0.11	0.15	0.18	0.22	0.26	0.30	0.33	0.37
4.3	0.04	0.09	0.13	0.17	0.22	0.26	0.30	0.34	0.39	0.43
5.01	0.05	0.10	0.15	0.20	0.25	0.30	0.35	0.40	0.45	0.50
5.83	0.06	0.12	0.17	0.23	0.29	0.35	0.41	0.47	0.52	0.58
6.8	0.07	0.14	0.20	0.27	0.34	0.41	0.48	0.54	0.61	0.68
7.93	0.08	0.16	0.24	0.32	0.40	0.48	0.56	0.63	0.71	0.79
9.24	0.09	0.18	0.28	0.37	0.46	0.55	0.65	0.74	0.83	0.92
10.76	0.11	0.22	0.32	0.43	0.54	0.65	0.75	0.86	0.97	1.08
12.55	0.13	0.25	0.38	0.50	0.63	0.75	0.88	1.00	1.13	1.26
14.62	0.15	0.29	0.44	0.58	0.73	0.88	1.02	1.17	1.32	1.46
17.04	0.17	0.34	0.51	0.68	0.85	1.02	1.19	1.36	1.53	1.70
19.86	0.20	0.40	0.60	0.79	0.99	1.19	1.39	1.59	1.79	1.99
23.15	0.23	0.46	0.69	0.93	1.16	1.39	1.62	1.85	2.08	2.32
26.98	0.27	0.54	0.81	1.08	1.35	1.62	1.89	2.16	2.43	2.70
31.44	0.31	0.63	0.94	1.26	1.57	1.89	2.20	2.52	2.83	3.14

AFE OUTPUT SIGNAL (V)

Temperature Measurement Operations

A temperature measurement is a time measurement of the RC circuit connected to the temperature port device pins T1, T2, and TC. The TC device pin has a driver to charge the timing capacitor.

Figure 6 depicts a 10kΩ NTC thermistor with a 10nF NPO COG 30ppm/°C capacitor. It shows two dummy cycles with two temperature port-evaluation measurements and two real temperature port measurements.

The Dummy 1 and Dummy 2 cycles represent preamble measurements that are intended to eliminate the dielectric absorption of the temperature measurement capacitor. These Dummy cycles are executed using a thermistor Emulation resistor of 1000 Ohms internal to the device. This Dummy path allows the dielectric absorption effects of the capacitor to be eliminated without causing the thermistor to be unduly self-heated. The number of Dummy measurements to be taken ranges from 0 to 7. This parameter is configured by setting the PRECYC[2:0] bits in the Event Timing 2 register.

Following the dummy cycles, an evaluation, TXevaluate, is performed. This measurement allows the device to maximize power efficiency by evaluating the temperature of the thermistor with a coarse measurement prior to a real measurement. The coarse measurement provides an approximation to the TDC converter. During the real measurement, the TDC can then optimize its measurement parameters to use power efficiently. These evaluate cycles are automatically inserted. The time from the start of one port's temperature measurement to the next port's temperature measurement is set using with the PORTCYC[1:0] bits in the Event Timing 2 register.

Once all the temperature measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results registers. The TE bit in the Interrupt Status register is also set and the $\overline{INT}$ pin is asserted (if enabled).

Actual temperature is determined by a ratio-metric calculation. If T2 is connected to a thermistor and T1 is connected to the reference resistor (as shown in the System Diagram), then the ratio of T2/T1 = $R_{THERMISTOR}/R_{REF}$.. The ratio $R_{THERMISTOR}/R_{REF}$. can be determined by the host microprocessor and the temperature can be derived from a lookup table of Temperature vs. Resistance for the thermistor utilizing interpolation of table entries if required.

Temperature Error Handling

The temperature measurement unit can detect open and/or short circuit temperature probes. If the resultant temperature reading in less than 8μs, then the device writes a value of 0000h to the corresponding Results registers to

Table 4. Randomizer Sampling

TDF FREQUENCY (Hz)	MINIMUM NEXT SAMPLE PERIOD (S)	MAXIMUM NEXT SAMPLE PERIOD (S)	LSB WEIGHT (S)
0.50	0.082	1.00	2.0E-3
1.00	0.084	2.00	3.9E-3
1.50	0.086	2.99	5.9E-3
2.00	0.088	3.99	7.8E-3
2.50	0.090	4.99	9.8E-3
3.00	0.092	5.99	11.7E-3
3.50	0.094	6.99	13.7E-3
4.00	0.096	7.98	15.6E-3
4.50	0.098	8.98	17.6E-3
5.00	0.100	9.98	19.5E-3
5.50	0.101	10.98	21.5E-3
6.00	0.103	11.98	23.4E-3
6.50	0.105	12.97	25.4E-3
7.00	0.107	13.97	27.3E-3
7.50	0.109	14.97	29.3E-3
8.00	0.111	15.97	31.3E-3

indicate a short circuit temperature probe. If the measurement process does not discharge the TC pin below the threshold of the internal temperature comparator within 2µs of the time set by the PORTCYC[1:0] bits in the Event Timing 2 register, then an open circuit temperature probe error is declared. The MAX35104 writes a value of FFFFh to the corresponding results registers to indicate an open circuit temperature probe, the TO bit in the Interrupt Status register is set, and the $\overline{\text{INT}}$ pin is asserted (if enabled). If the temperature measurement error is caused by any other problems, then the device writes a value of FFFFh to each of the temperature port results registers indicating that all the temperature port measurements are invalid.

Event Timing Operation

The Event Timing mode of operation is an advanced feature that allows the user to configure the device to perform automatic measurement cycles. This allows the host microcontroller to enter low power mode and only awaken upon assertion of the $\overline{\text{INT}}$ pin (if enabled) when new measurement data is available. By using the TOF_DIFF and Temperature commands and configuring the appropriate TOFx registers and the Event Timing registers, the Event Timing Modes directs the device to provide complete data for a sequence of measurements captured on a cyclical basis. There are three versions of the EVTMG commands.

- EVTMG2: Performs automatic TOF_DIFF measurements. The parameters and operation of the TOF measurement are described in the Time-of-Flight Measurement section.
- EVTMG3: Performs automatic Temperature measurements. The parameters and operation of the Temperature measurements are described in the Temperature Measurement section.
- EVTMG1: Performs automatic TOF_DIFF and Temperature measurements.

Continuous Event Timing Operation

The device can be configured to continue running Event Timing sequences at the completion of any sequence. If the ET_CONT bit in the Calibration and Control register is set, the currently executing EVTMGx command continues to execute until a HALT command is received by the device. If the ET_CONT bit is clear, automatic execution of Event Timing stops after the completion of a full sequence of measurements.

Continuous Interrupt Timing Operation

When operating in Event Timing Mode, the $\overline{\text{INT}}$ pin can be asserted (if enabled) either after each TOF or Temperature measurement, or at the completion of the sequence of measurements. If the CONT_INT bit in the Calibration and Control register is set to a 1, then the $\overline{\text{INT}}$ pin is asserted (if enabled) at the completion of each TOF or Temperature command. This allows the host microcontroller to interrogate the current Event for accuracy of measurement. If the CONT_INT bit is set to a 0, then the $\overline{\text{INT}}$ pin is only asserted (if enabled) at the completion of a sequence of measurements. This allows the host microcontroller to remain in a low-power sleep mode and only wake-up upon the assertion of the $\overline{\text{INT}}$ pin.

TOF Sample Randomizer

The device has the ability to randomize the TOF samples when operating in event timing mode, given a sample frequency as selected by the TDF[3:0] bits, the subsequent samples in the sequence occur at a period ±(1/F) from the previous sample.

This is accomplished using a 9-bit linear feedback shift register (LFSR) to randomize the internals between successive samples. The feedback polynomial implemented for the LFSR is $x^9 + X^5 + 1$.

For example, if TDF[3:0] is set to 0, which is a sample frequency of 0.5s and an event timing mode is initiated, the first sample occurs 0.5s after that start. The subsequent samples occur at a time between 0.082s and 1s after the start of the previous sample, and so on. The times are start-to-start times.

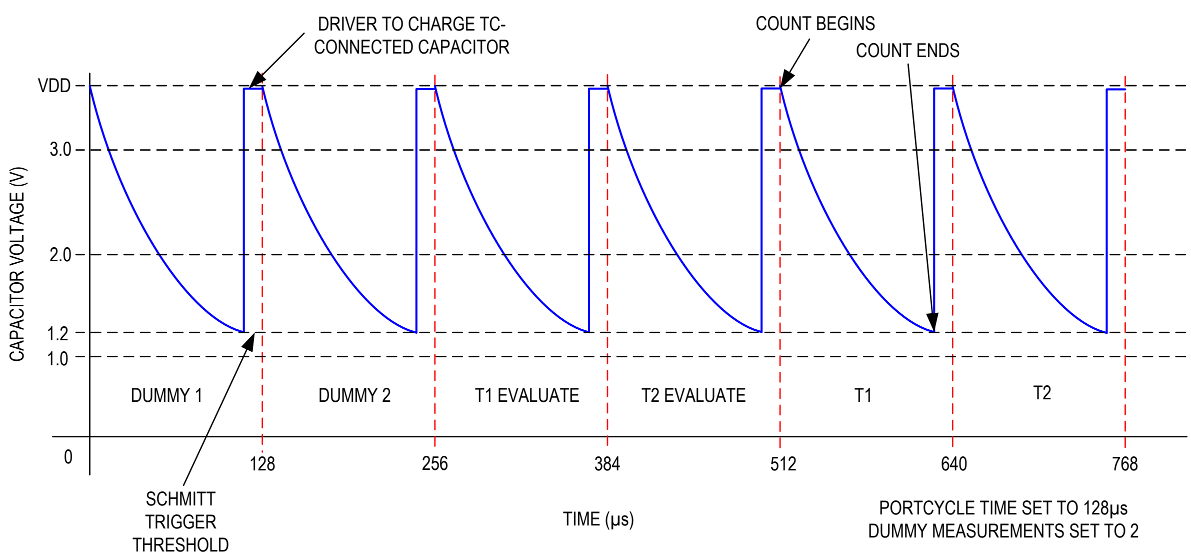


Figure 10. Temperature Command Execution Cycle Example

Error Handling During Event Timing Operation

During execution of Event Timing modes, any error that occurs during a TOF_DIFF or Temperature measurement are handled as described in the corresponding error handling sections. Calibration can also be executed during Event Timing operation, if programmed to do so with the Calibration Configuration bits in the Calibration and Control register. If a Calibration error occurs, this is handled as described in the *Error Handling during Calibration* section. If any of these errors occur, the Event Timing operation does not terminate, but continues operation.

When making TOF measurements in Event Timing Mode, the device provides additional data in the TOF_Cycle_Count/TOF_Range register that can be used to check the validity of all the TOF measurements. The TOF_Cycle_Count is the number of valid error-free TOF measurements that were recorded during an Event Timing Sequence. If a TOF error occurs, the TOF_Cycle_Count register is not incremented. The TOF_Range is the range of all valid TOF measurements that were captured during a sequence.

When making temperature measurements in Event Timing Mode, the device provides additional data in the Temp_Cycle_Count register. This count increments after every valid error-free temperature measurement and can be used to check the validity of all the temperature measurements. In addition, the Temperature Average Results registers, TxAVG, are not updated with the error measurement if a temperature error occurs during Event Timing Operation.

Event Timing Mode 2

The EVTMG2 command execution causes the TOF_DIFF command to be executed automatically with programmable repetition rates and programmable total counts as shown in Figure 11.

During execution of the EVTMG2 command, each TOF_DIFF command execution cycle causes the device to compute a TOF_DIFF measurement (AVGUP register minus AVGDN register) as well as the running average of TOF_DIFF measurements (TOFF_DIFF_AVG register). The setting of the TDF[3:0] bits in the Event Timing 1 register selects the rate at which TOF_DIFF commands are executed. The setting of the TDM[4:0] bits in the Event Timing 1 register determines the number of TOF_DIFF measurements to be taken during the sequence.

Once all the TOF_DIFF measurements in the sequence are captured, the TOF_DIFF_AVG register contains the average of the differences of the resultant AVGDN and AVGUP Results register content of each TOF_DIFF measurement. After the TOF_DIFF_AVG registers are updated, the TOF_EVTMG bit is set in the Interrupt Status register and the $\overline{\text{INT}}$ pin is asserted (if enabled).

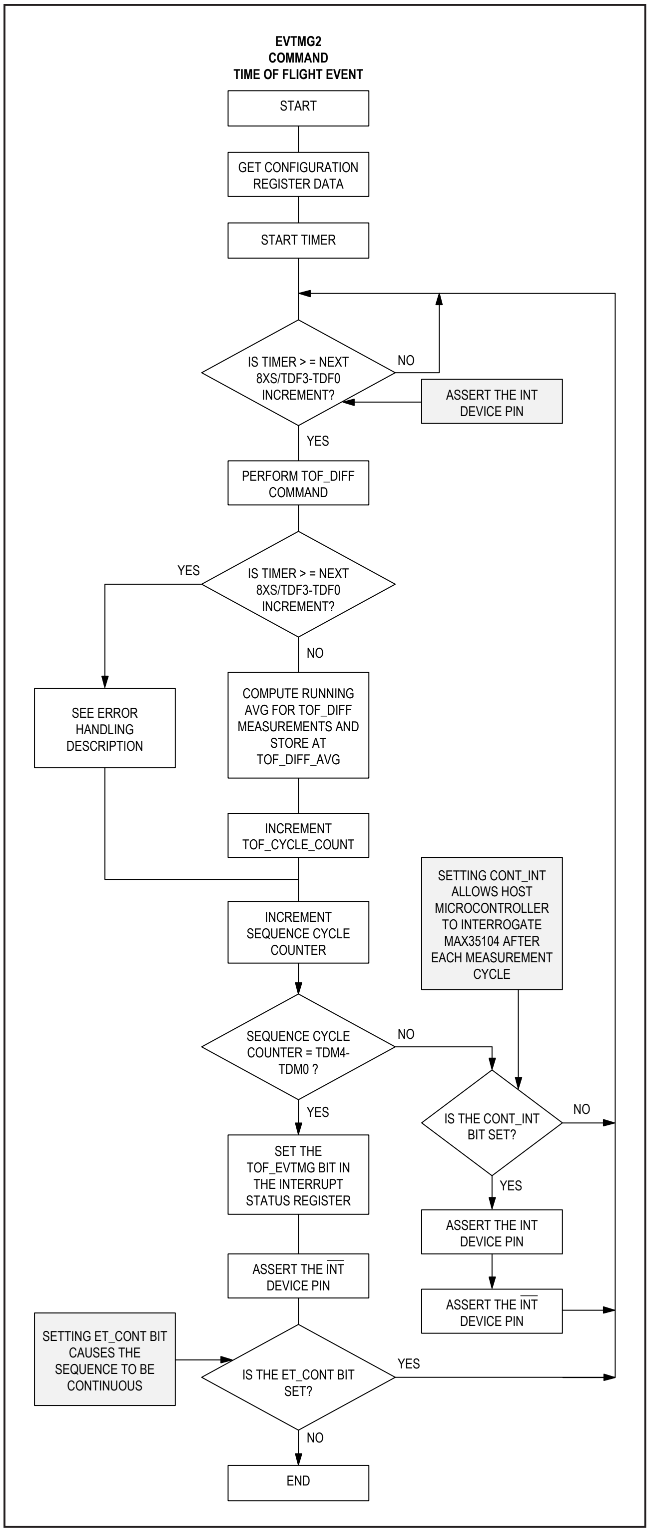


Figure 11. EVTMG2 Command

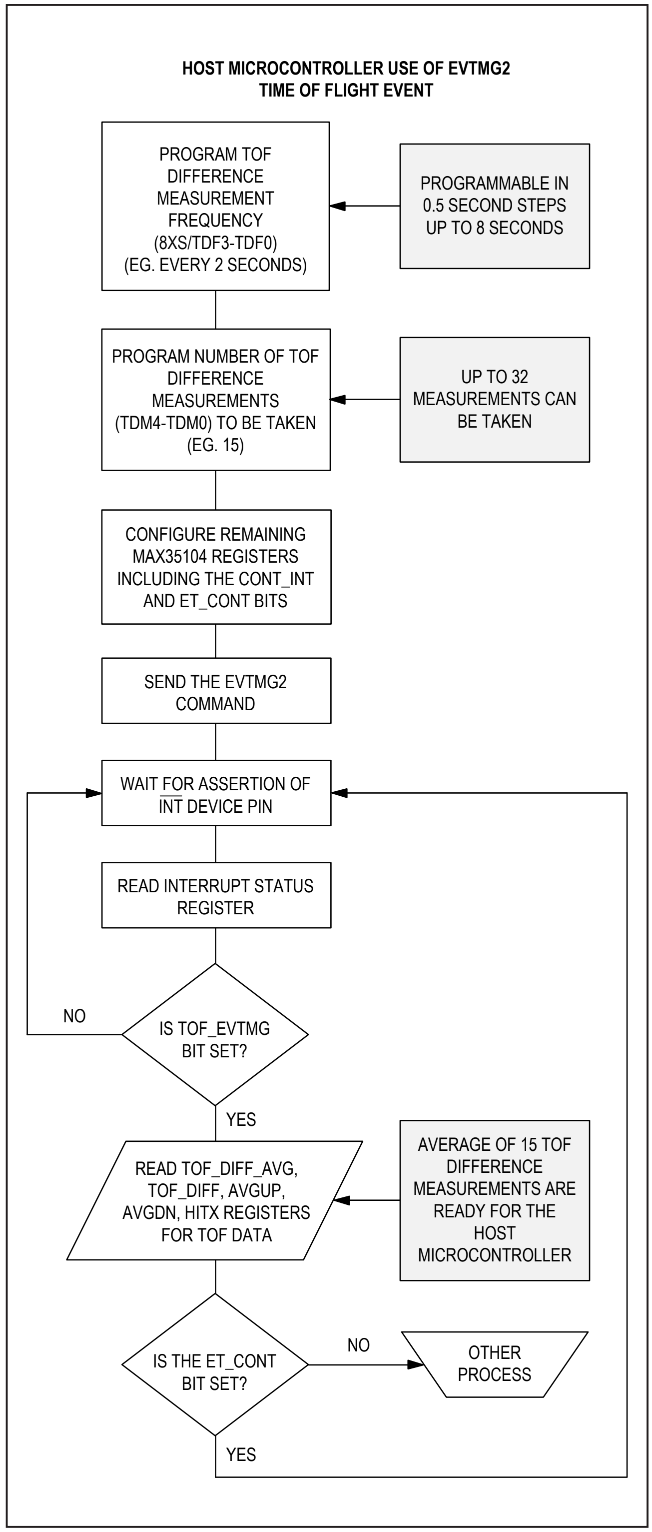


Figure 12. EVTMG2 Pseudo Code

Event Timing Mode 3

The EVTMG3 command execution causes the Temperature command to be executed automatically with programmable repetition rates and programmable total counts as shown in Figure 13.

During execution of the EVTMG3 command, each Temperature command execution cycle computes the running average of the measurement of each temperature port. The results are provided in the Tx_AVGInt and TxAVGFrac Results registers.

The setting of the TMF[5:0] bits in the Event Timing 1 register selects the rate at which Temperature commands are executed. The setting of the TMM[4:0] bits in the Event Timing 2 register determines the number of temperature measurements to be taken during the sequence.

Once all the Temperature measurements in the sequence are captured, the Tx_AVGInt and TxAVGFrac Results registers contain the average of all the temperature measurements in the sequence. After these registers are updated, the Temp_EVTMG bit is set in the Interrupt Status register and the $\overline{\text{INT}}$ pin is asserted (if enabled).

Event Timing Mode 1

The EVTMG1 command execution causes the TOF_DIFF command and the Temperature Command to be executed automatically with programmable repetition rates and programmable total counts. In essence, both the EVTMG2 and EVTMG3 commands are simultaneously executed in a synchronous manner.

Setting up the TOF measurements for automatic execution in Event Timing Mode 1 is identical to setting these up for execution with Event Timing Mode 2. Likewise, setting up the Temperature Measurements is identical to setting these up for execution using Event Timing Mode 3.

If the TOF_DIF command repetition rate and the Temperature command repetition rate cause both measurements to be required at the same time, the TOFF_DIF command takes precedent. Upon completion of the TOFF_DIFF command, the pending Temperature command is executed, as shown in Figure 15.

Once all the TOF_DIFF measurements in the sequence are complete, the TOF_EVTMG bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin asserts (if enabled). Likewise, when all the Temperature measurements in the sequence are completed, the Temp_EVTMG bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin is asserted (if enabled). It should be noted that depending upon the selected rates and number of cycles, the TOF_DIFF and Temperature measurements can complete their sequences at different times. This causes the $\overline{\text{INT}}$ pin to be asserted (if enabled) before both sequences are complete.

Calibration Operation

For more accurate results, calibration of the TDC can be performed. Calibration allows the device to perform a calibration measurement that is based upon the 32.768kHz crystal, which is the most accurate clock in the system. This calibration is used when a ceramic oscillator is used in place of an AT-cut crystal for the 4MHz reference. The device automatically generates start and stop signals based upon edges of the 32.768kHz clock. The number of 32.768kHz clock periods that are used and then averaged are selected with the CAL_PERIOD[3:0] bits in the Calibration and Control register. The TDC measures the number of 4MHz clock pulses that occur during the 32.768kHz pulses. The measured time of a 32.768kHz clock pulse is reported in the CalibrationInt and CalibrationFrac Results registers. These results can then be used as a gain factor for calculating actual Time-to-Digital converter measurement if the CAL_USE bit in the Event Timing 2 register is set.

Following is a description of an example calibration. Each TDC measurement is a 15-bit fixed-point integer value concatenated with a 16-bit fractional value binary representation of the number of t_4MHz periods that contribute to the time result, the actual period of t_4MHz needs to be known. If the CAL_PERIOD[3:0] bits in the Calibration and Control register are set to 6, then six measurements of 32.768kHz periods are measured by the TDC and then averaged. The expected measured value would be 30.5176µs/250ns = 122.0703125 t_4MHz periods. Let us assume that the 4MHz ceramic resonator is actually running at 4.02MHz. The TDC measurement unit would then measure 30.5176µs/248.7562ns = 122.6806641 t_4MHz periods and this result would be returned in the Calibration Results register. For all TDC measurements, a gain value of 122.0703125/122.6806641 = 0.995024876 would then be applied.

Calibration is performed at the following events:

- When the Calibration command is sent to the MAX35104. At the completion of this calibration, the CAL bit in the Interrupt Status register and the INT pin is asserted (if enabled).
- During Event Timing Operation, automatic calibrations can be performed before executing TOF or Temperature measurements. This is selectable with the CAL_CFG[2:0] bits in the Event Timing 2 register. Upon completion of an automatic calibration during Event Timing, the result is updated in the Calibration Results register, but the CAL bit in the Interrupt Status register is not set and the INT pin is not asserted.

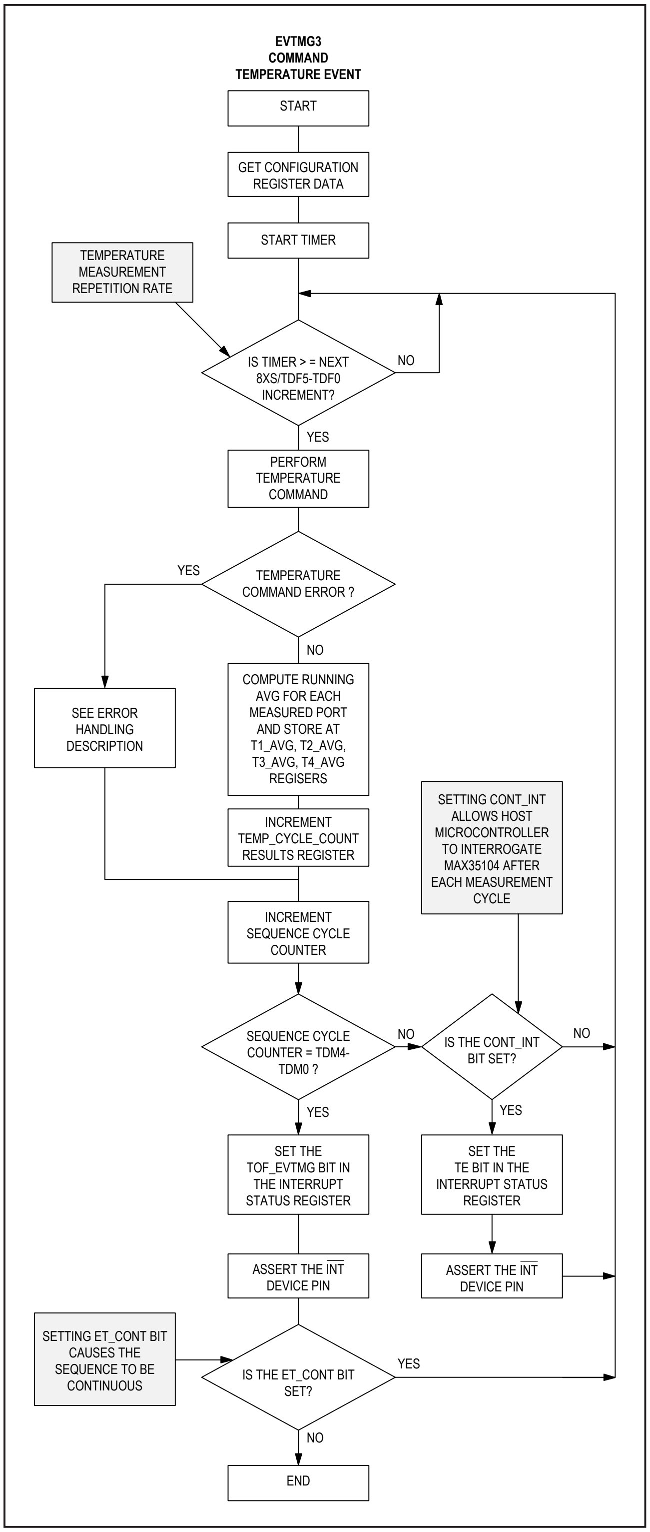


Figure 13. EVTMG3 Command

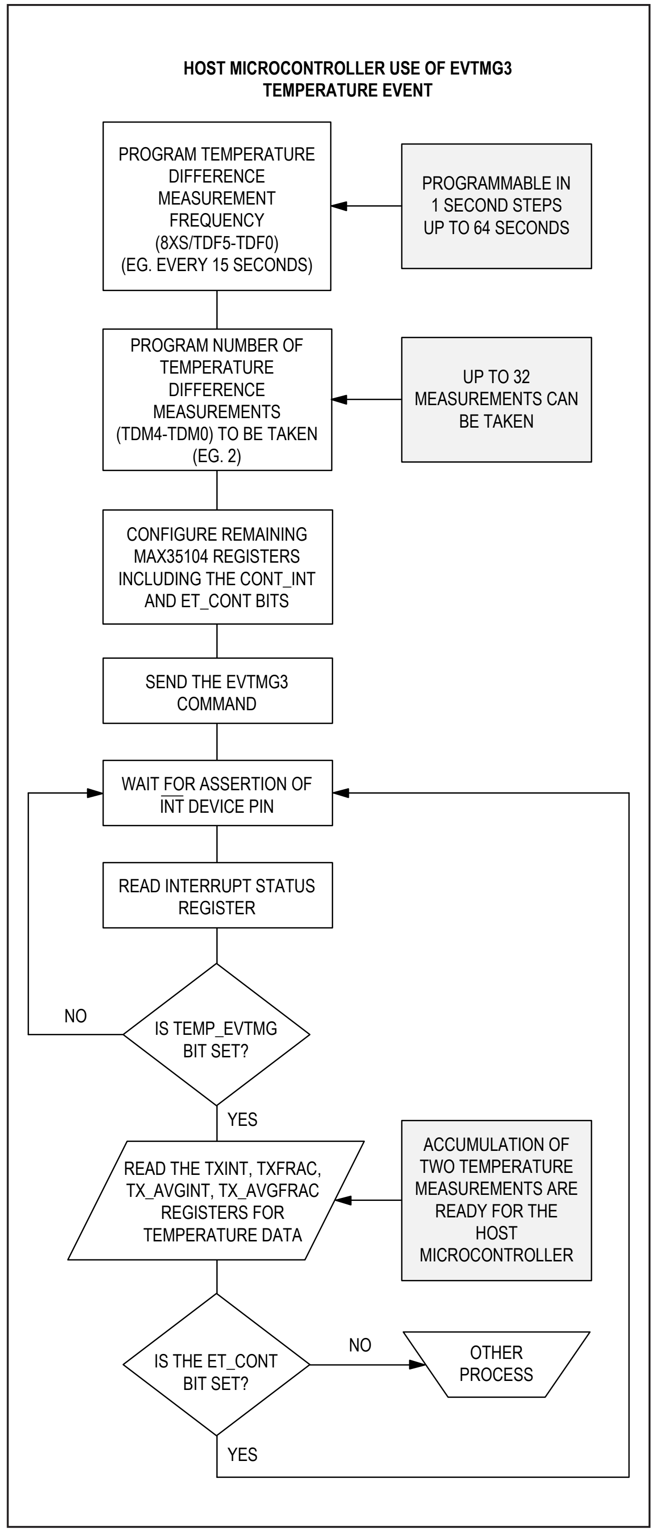


Figure 14. EVTMG3 Pseudo Code

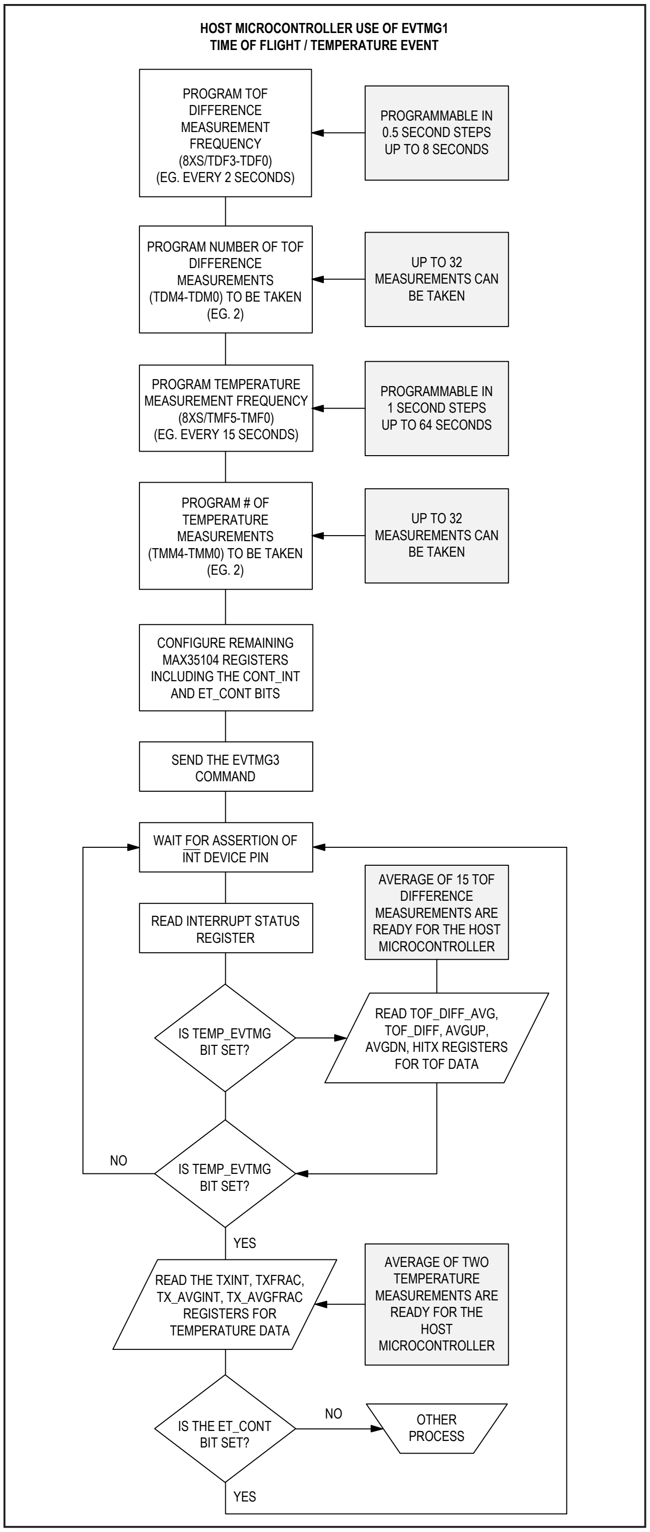


Figure 15. EVTMG1 Pseudo Code

Error Handling during Calibration

Since calibration can be set to be automatic by configuring the CAL_CFG[2:0] bits in the Event Timing 2 register, any errors that occur during the Calibrate command stop the CalibrationInt and the CalibrationFrac Results registers from being updated with new calibration coefficients. The results for the previous Calibration data remain in these two registers and be used for scaling measured results. If the calibration error is caused by the internal calibration time measurement exceeding the time set by the TIMOUT[2:0] bits in the TOF2 register, the TO bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled).

RTC, Alarm, Watchdog, and Tamper Operation

RTC Operation

The device contains a real-time clock (RTC) that is driven by the 32kHz oscillator. The time and calendar information is obtained by reading the appropriate register words. The time and calendar are set or initialized by writing the appropriate register words. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The clock/calendar provides hundredths of seconds, tenths of seconds, seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year valid up to 2100. The clock operates in either the 24-hour or the 12-hour format with AM/PM indicator. The device's RTC can be programmed for either 12-hour or 24-hour formats. If using the 24-hour format, Bit6 (12 HR MODE) of the Mins_Hrs register should be cleared to 0 and then Bit5 represents the 20-hour indicator. If using the 12-hour format, Bit6 should be set to 1 and Bit5 represents AM (if 0) or PM (if 1). The day-of-week register increments at midnight. Values that correspond to the day of week are user defined but must be sequential (i.e., if 0 equals Sunday, then 1 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Alarm Operation

The device's RTC provides one programmable alarm. The alarm is activated when either the AM1 or AM2 bits in the Real-Time Clock register are set. Based upon these bits, an alarm can occur when either the minutes and/or hours programmed in the Alarm register match the current value in the Mins_Hrs register. When an Alarm occurs, the AF bit in the Interrupt Status register is set and the $\overline{INT}$ device pin is asserted (if enabled).

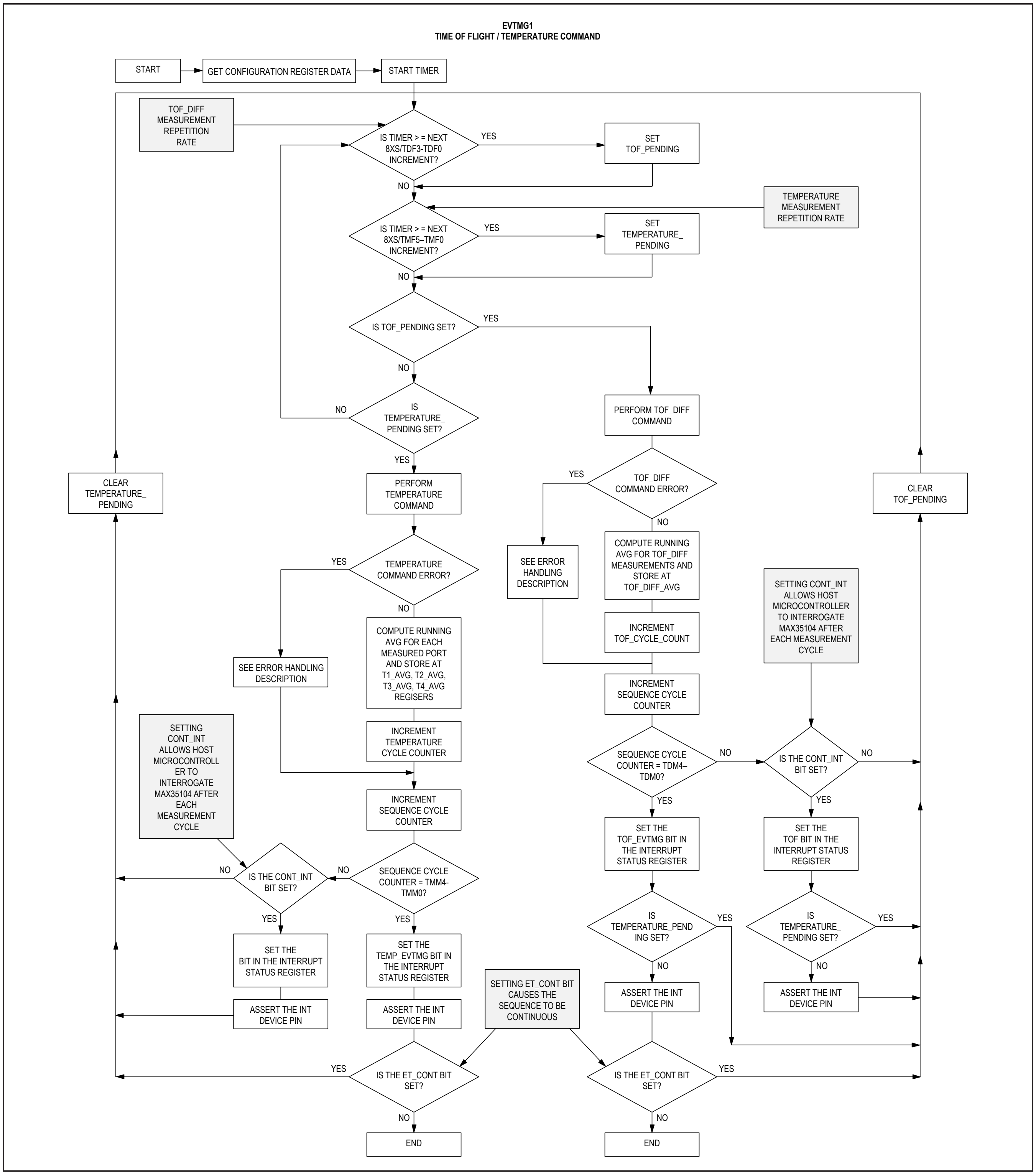


Figure 16. EVTMG1 Command

For proper alarm function, programming of the ALARM register HOURS bits must match the format (12- or 24-hour modes) used in the Mins_Hrs register.

Watchdog Operation

The device also contains a watchdog alarm. The Watchdog Alarm Counter register is a 16-bit BCD counter that is programmable in 10ms intervals from 0.01 to 99.99 seconds. A seed value can be written to this register representing the start value for the countdown. The watchdog counter begins decrementing when the WD_EN bit in the RTC register is set.

An immediate read of Watchdog Alarm Counter returns the value just written. A read after a “wait” duration causes a value “seed” minus “wait” to be returned. For example if the seed value was 28.01 seconds, an immediate read returns 28.01. A read after a 4 seconds returns 24.01 seconds. The value read out for any read operation is a snapshot obtained at the instant of a serial read operation.

A write operation to the Watchdog Alarm Counter causes a re-load with the newly written seed. When the Watchdog is enabled and a non-zero value is written into the Watchdog Alarm Counter, the Watchdog Alarm Counter decrements every 1/100 second, until it reaches zero. At this point, the WF bit in the Real Time Clock register is set and the $\overline{\text{WDO}}$ pin is asserted low for a minimum of 150ms. At the end of the pulse, the $\overline{\text{WDO}}$ pin becomes high impedance.

The WF flag remains set until cleared by writing WF to a logic 0 in the Real-Time Clock register. If the WF bit is cleared while the $\overline{\text{WDO}}$ device pin is being held low, the $\overline{\text{WDO}}$ device pin is immediately released to its high-impedance state. Writing a seed value of 0 does not cause the WF bit to be asserted.

Tamper Detect Operation

The device provides a single input that can be connected to a device case switch and used for tamper detection. Upon detection of a case switch event the CSWA in the Control Register and the CSWI bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ device pin is asserted (if enabled).

Device Interrupt Operations

The device is designed to optimize the power efficiency of a flow metering application by allowing the host microprocessor to remain in a low power sleep mode, instead of requiring the microprocessor to keep track of complex real-time events being performed by the MAX35104. Upon completion of any command, the device alerts the host microprocessor using the $\overline{\text{INT}}$ pin. The assertion of the $\overline{\text{INT}}$ pin can be used to awaken the host microprocessor from its low-power mode. Upon receiving an interrupt on the $\overline{\text{INT}}$ pin, the host microprocessor should read the Interrupt Status register to determine which tasks were completed.

Interrupt Status Register

The interrupt status register contains flags for all for all commands and events that occur within the MAX35104. These flags are set when the event occurs or at the completion of the executing command. When the Interrupt Status Register is read, all asserted bits are cleared. If another interrupt source has generated an interrupt during the read, these new flags are asserted following the read.

$\overline{\text{INT}}$ Pin

The device’s $\overline{\text{INT}}$ pin is asserted when any of the bits in the Interrupt Status register are set. The $\overline{\text{INT}}$ pin remains asserted until the Interrupt Status register is read by the user and all bits in this register are clear. For the $\overline{\text{INT}}$ pin to operate, it must first be enabled by setting the INT_EN bit in the Calibration and Control register.

Serial Peripheral Interface Operation

Four pins are used for SPI-compatible communications: DOUT (serial-data out), DIN (serial-data in), $\overline{\text{CE}}$ (chip enable), and SCK (serial clock). DIN and DOUT are the serial data input and output pins for the devices, respectively. The $\overline{\text{CE}}$ input initiates and terminates a data transfer. SCK synchronizes data movement between the master (microcontroller) and the slave (MAX35104). The SCK, which is generated by the microcontroller, is active only when $\overline{\text{CE}}$ is low and during opcode and data transfer to any device on the SPI bus. The inactive clock polarity is logic-low. DIN is latched on the falling edge of SCK. There is one clock for each bit transferred. Opcode bits are transferred in groups of eight, MSB first. Data bits are transferred in groups of 16, MSB first.

The SPI is used to access the features and memory of the MAX35104 using an opcode/command structure.

Opcode Commands

The MAX35104 supports the opcode/commands shown in Table 5.

Table 5. Opcode Commands

GROUP	COMMAND	OPCODE FIELD (HEX)
Execution Opcode Commands	TOF_Up	00h
	TOF_Down	01h
	TOF_Diff	02h
	Temperature	03h
	Reset	04h
	Bandpass_Calibrate	06h
	EVTMG1	07h
	EVTMG2	08h
	EVTMG3	09h
	HALT	0Ah
	Calibrate	0Eh
Register Opcode Commands	Read Register	94h–97h, B0h–FFh Each hex value represents the location of a single 16-bit register.
	Write Register	14h–17h, 30h–43h Each hex value represents the location of a single 16-bit register.

Execution Opcode Commands

The device supports several single byte opcode commands, which cause the MAX35104 to execute various routines. All commands have the same SPI protocol sequence as shown in Figure 17. Once all 8 bits of the opcode are received by the MAX35104 and the $\overline{CE}$ device pin is deasserted, the device begins execution of the specified command as described in that Command's description.

TOF_UP Command (00h)

The TOF_UP command generates a single TOF measurement in the upstream direction. Pulses are launched from the TX_UPP and TX_UPN pins and received by the TX_DNP and TX_DNN pins. The measured hit results are reported in the HITxUPInt and HITxUPFrac registers, with the calculated average of all the measured hits being reported in the AVGUPInt and AVGUPFrac register. The t_1/t_2 and $t2/t_{IDEAL}$ wave ratios are reported in the WVRUP register. Once all these results are stored, then the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled).

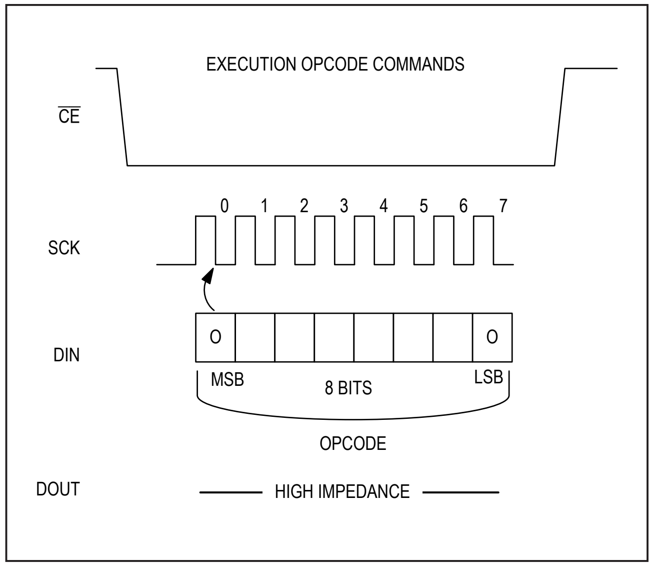


Figure 17. Execution Opcode Command Protocol

Note: The TOF_UP command yields absolute time of flight results that include circuit delays.

TOF_Down Command (01h)

The TOF_DOWN command generates a single TOF measurement in the downstream direction. Pulses are launched from the TX_DNP and TX_DNN pins and received by TX_UPP and TX_UPN pins. The measured hit results are reported in the HITxDnInt and HITxDnFrac registers, with the calculated average of all the measured hits being reported in the AVGDNInt and AVGDNFrac register. The t_1/t_2 and t_2/t_{IDEAL} wave ratios are reported in the WVRDN register. Once all these results are stored, the TOF bit in the Interrupt Status register is set and the $\overline{INT}$ pin is asserted (if enabled).

Note: The TOF_Down command yields absolute time of flight results that include circuit delays.

TOF_DIFF Command (02h)

The TOF_DIFF command performs back-to-back TOF_UP and TOF_DN measurements as required for a metering application. The TOF_UP sequence is followed by the TOF_DN sequence. The time between the start of the TOF_UP measurement and the start of the TOF_DN measurement is set by the TOF_CYC[2:0] bits in the TOF2 register. Upon completion of the TOF_DN measurement, the results of AVGUP minus AVGDN is computed and stored at the TOF_DIFFInt and TOF_DIFFFrac Results register locations. Once these results are stored, then the

TOF bit in the Interrupt Status register is set and the INT pin is asserted (if enabled).

Temperature Command (03h)

The Temperature command initiates a temperature measurement sequence as described in the *Temperature Measurement Operations* section. The characteristics the temperature measurement sequence depends upon the settings in the Event Timing 1 Register, and Event Timing 2 register. Once all the measurements are completed, the times measured for each port are reported in the corresponding TxInt and TxFrac Results Registers. The TE bit in the Interrupt Status register is also set and the INT pin is asserted (if enabled).

Reset Command (04h)

The Reset command essentially performs the same function as a POR and causes all the Configuration registers to be set to their POR values and all the Results registers and the Interrupt Status register to be cleared and set to zero.

Initialize Command (05h)

The Initialize command recalls POR values for registers 14h–17h.

Bandpass Calibrate Command (06h)

The Bandpass Calibrate command is used to automatically program the bandpass filter's center frequent. This command should be run before any TOF commands are executed (if the bandpass is enabled). To execute this command, first select the desired launch frequency by setting the DPL[3:0] bits in the TOF1 register. Upon execution of this command, the device uses internally generated signals at the set launch frequency to stimulate the bandpass filter and selects the correct center frequency values for the F0 Adjust bits, F0[6:0] in the AFE 2 register.

EVTMG1 Command (07h)

After issuing the Bandpass Calibrate command, an additional 5mA ICC current is active until the CE pin is toggled. Note: The Bandpass Calibrate command is not available for 1MHz pulse lauch divider setting, DPL[3:0] = 1.

The EVTMG1 command initiates the event timing mode 1 advanced automatic measurement feature. This timing mode performs automatic TOF_DIFF and Temperature measurements as described in the Event Timing Operations section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 Register, Event timing 2 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

EVTMG2 Command (08h)

The EVTMG2 command initiates the event timing mode 2 advanced automatic measurement feature. This timing mode performs automatic TOF_DIFF measurements as described in the Event Timing Operations section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

EVTMG3 Command (09h)

The EVTMG3 command initiates the event timing mode 3 advanced automatic measurement feature. This timing mode performs automatic Temperature measurements as described in the Event Timing Operations section. The duration of the automatic measurements depends upon the settings in the Event Timing 1 register, Event timing 2 register, CONT_INT and ET_CONT bits in the Calibration and Control register.

HALT Command (0Ah)

The HALT command is sent to the device to stop any of the three EVTMG1/2/3 commands. All register data content is frozen and the SPI is then made available for access by the host microcontroller for commands, memory access, and register access. The HALT command takes time to execute. Because the EVTMGx commands are composed of multiple TOF_DIFF and Temperature commands, the HALT command causes the device to evaluate its own state and complete the currently executing TOF_DIFF or Temperature command. Once the HALT command has completed, all registers are updated and the device sets the Halt bit in the Interrupt Status register and then asserts the INT device pin (if enabled). The host microprocessor reads the Interrupt Status register to determine the interrupt source.

Calibrate Command (0Eh)

The Calibrate command performs the calibration routine as described in the *Calibration Operation* section. When the Calibrate command has completed the measurement, the Calibration Results register contains the measured 32kHz period measurement value, the device sets the Cal bit in the Interrupt Status register and then asserts the INT device pin (if enabled). The host microprocessor reads the Interrupt Status register to determine the interrupt source and then reads the Calibration Results register to calculate the 4MHz ceramic oscillator gain factor.

Register Opcode Commands

To manipulate the register memory, there are two commands supported by the device: Read register and Write register. Each register accessed with these commands is 16 bits in length. These commands are used to access all sections of the memory map including the RTC and Watchdog registers, Configuration registers, Conversion Results registers, and Status registers. The Conversion Results registers and the Interrupt Status register of the Status registers are all read only.

Read Register Command

The opcode must be clocked into the DIN device pin before the DOUT device pin produces the register data. Figure 18 shows the SPI protocol sequence.

The Read Register command can also be used to read consecutive addresses. In this case, the data bits are continuously delivered in sequence starting with the MSB of the data register that is addressed in the opcode, and continues with each SCK rising edge until the $\overline{CE}$ device pin is deasserted as shown in Figure 19. The address counter is automatically incremented.

Write Register Command

This command applies to all writable registers. See the *Register Memory Map* for more detail. Figure 20 shows the SPI protocol sequence.

The Write Register command can also be used to write consecutive addresses. In this case, the data bits are continuously received on the DIN device pin and bound for the initial starting address register that is addressed in the opcode. The address counter is automatically incremented after each 16 bits of data and wraps around to the beginning of the Configuration/Results register memory map if the SCK device pin is continually clocked and the $\overline{CE}$ device pin remains asserted as shown in Figure 21.

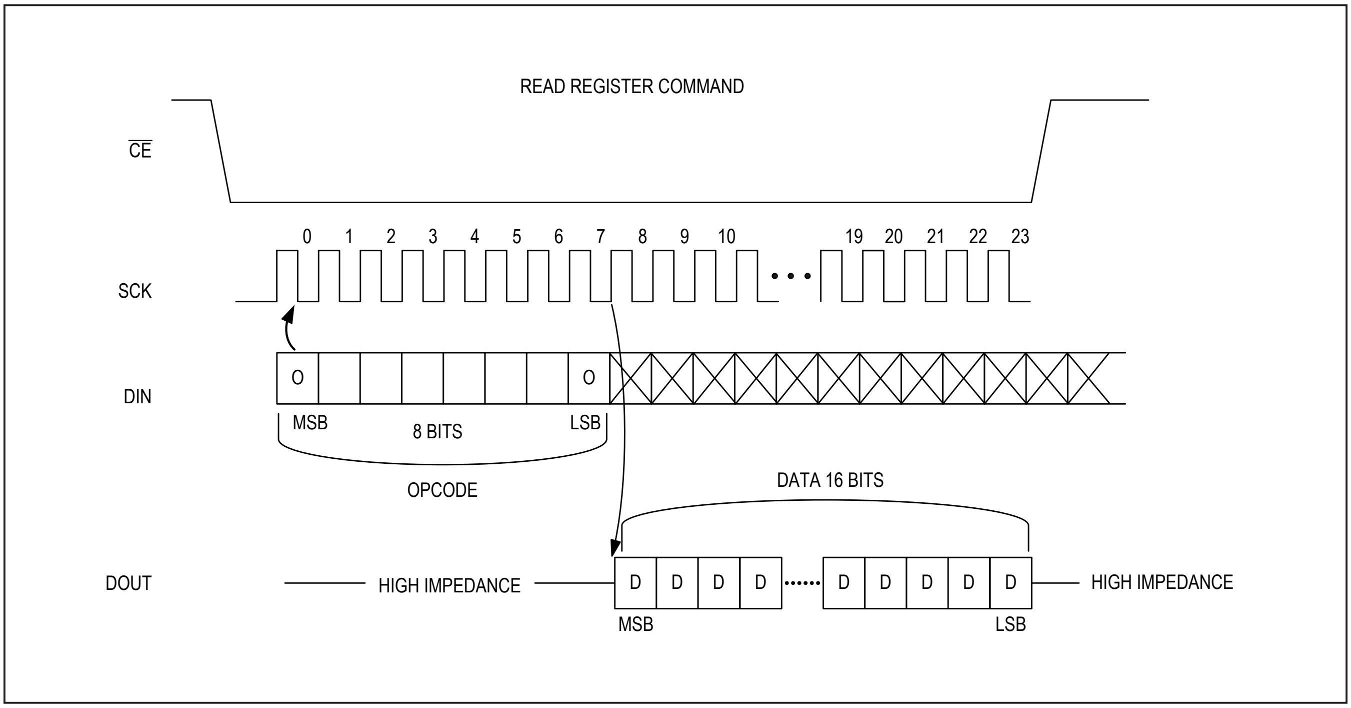


Figure 18. Read Register Opcode Command Protocol

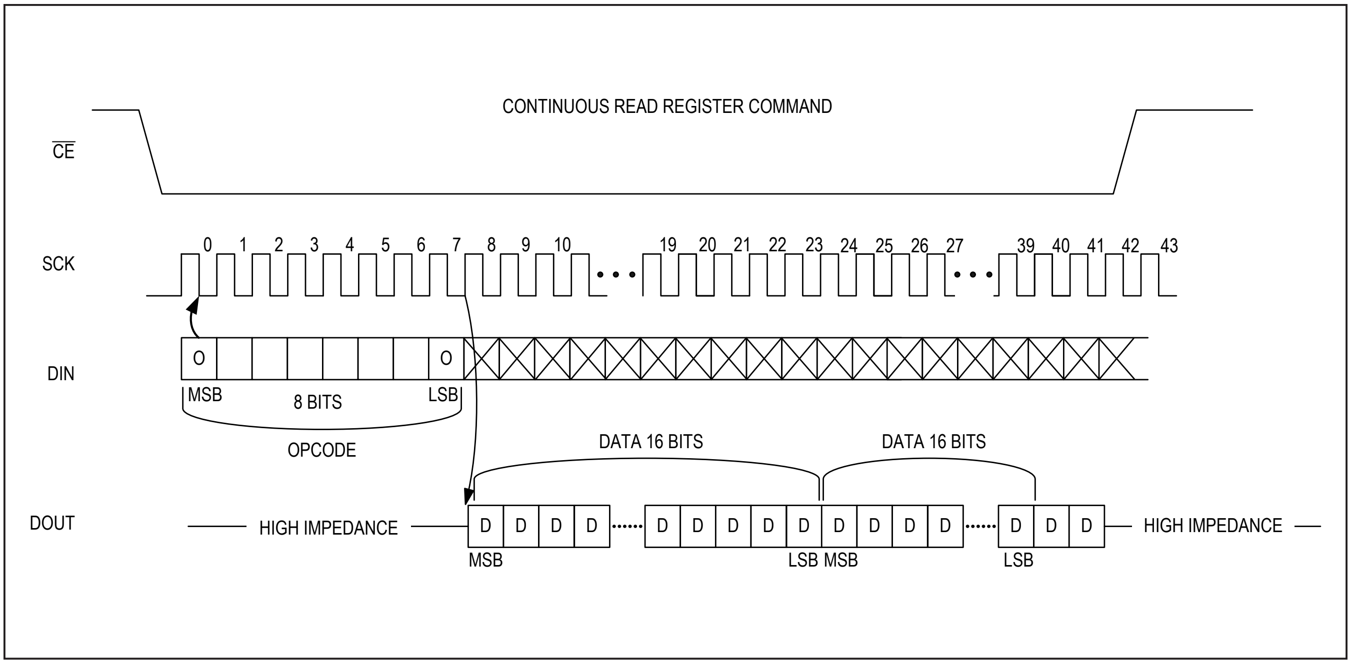


Figure 19. Continuous Read Register Opcode Command Protocol

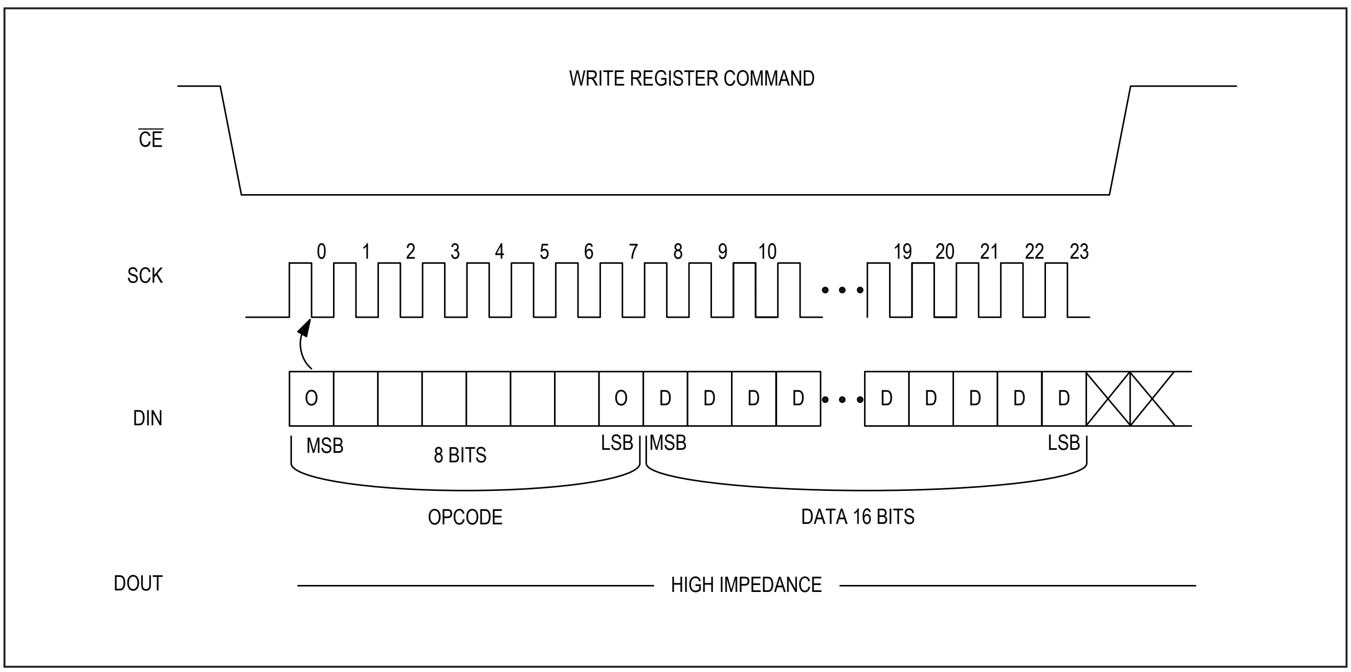


Figure 20. Write Register Opcode Command Protocol

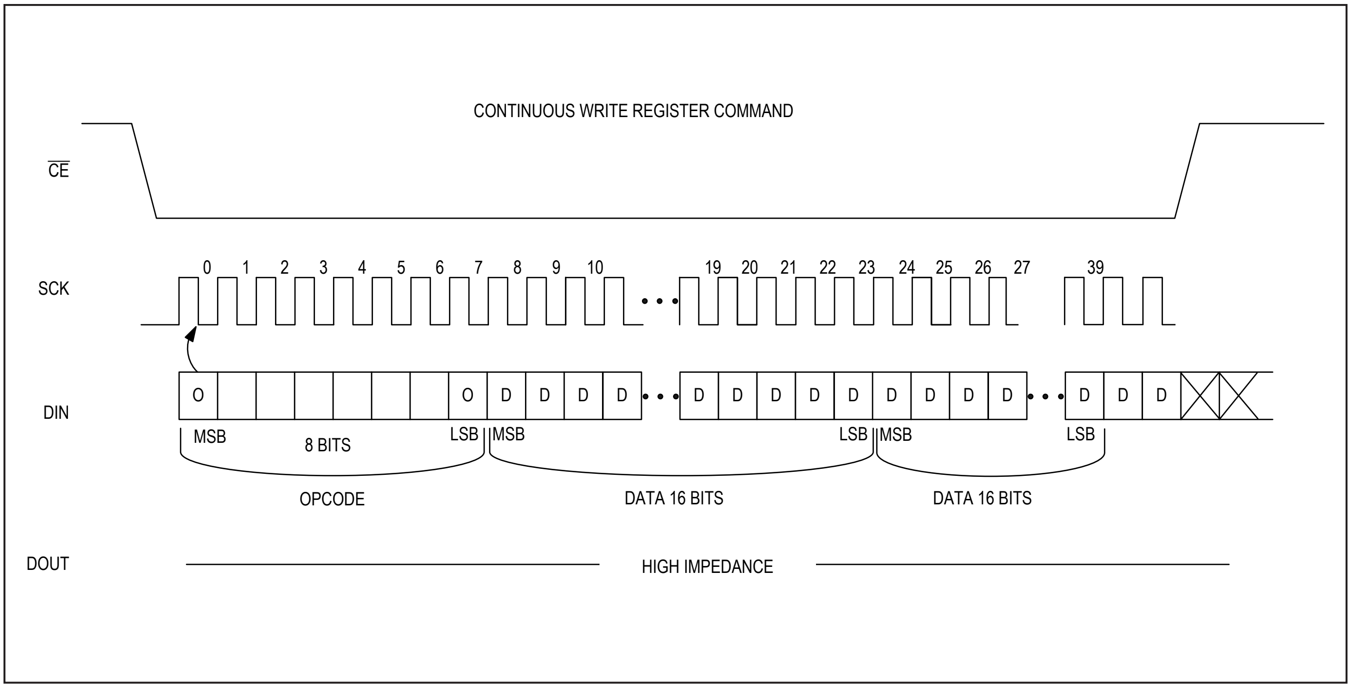


Figure 21. Continuous Write Register Opcode Command Protocol

Register Memory Map

Table 6 shows the registers that are accessed by the Read register command and the Write register command. "X" represents a reserved bit. Following a reset, all configuration variables are set to their POR default value. The RTC, Results, Interrupt Status, and Control registers are all 0000h following a reset.

Table 6. Register Memory Map

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]								BITS[7:0]							
RTC AND WATCHDOG REGISTERS																		
B0h	30h	Seconds	Tenths of Seconds				Hundredth Seconds				10 Seconds				Seconds			
B1h	31h	Mins_Hrs	10-Minutes				Minutes				0	12hr	20hr /AM/PM	10hr	Hours			
B2h	32h	Day_Date	Day								10-Date				Date			
B3h	33h	Month_ Year	10-Month				Month				10-Year				Year			
B4h	34h	Watchdog Alarm Counter	Tenths of Seconds				Hundredths of Seconds				10 Seconds				Seconds			
B5h	35h	Alarm	10-Minutes				Minutes				0	12hr	20hr /AM /PM	10hr	Alarm Hours			
CONFIGURATION REGISTERS																		
94h	14h	Switcher 1	SFREQ 1	SFREQ 0	HREG_ D	0	X	X	X	X	DFREQ1	DREEQ0	1	1	VS3	VS2	VS1	VS0
95h	15h	Switcher 2	LT_N3	LT_N2	LT_N1	LT_N0	LT_S3	LT_S2	LT_S1	LT_S0	ST3	ST2	ST1	ST0	LT_50D	0	0	PECHO
96h	16h	AFE1	AFE_ BP	0	0	0	0	SD_EN	AFEOU1	AFEOUT0	0	WRITE BACK VALUES READ						
97h	17h	AFE2	4M_ BP	F06	F05	F04	F03	F02	F01	F00	PGA3	PGA2	PGA1	PGA0	LOWQ1	LOWQ0	0	BP_BP
B6h	36h		Reserved															
B7h	37h		Reserved															
B8h	38h	TOF1	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	DPL3	DPL2	DPL1	DPL0	STOP_ POL	X	X	X
B9h	39h	TOF2	STOP2	STOP1	STOP0	T2WV5	T2WV4	T2WV3	T2WV2	T2WV1	T2WV0	TOF_ CYC2	TOF_ CYC1	TOF_ CYC0	EN_ UP_DN	TIMOUT 2	TIMOUT 1	TIMOUT 0
BAh	3Ah	TOF3	X	X	Hit1WV 5	Hit1WV 4	Hit1WV 3	Hit1WV 2	Hit1WV 1	Hit1WV 0	X	X	Hit2WV 5	Hit2WV 4	Hit2WV 3	Hit2WV 2	Hit2WV 1	Hit2WV 0
BBh	3Bh	TOF4	X	X	Hit3WV 5	Hit3WV 4	Hit3WV 3	Hit3WV 2	Hit3WV 1	Hit3WV 0	X	X	Hit4WV 5	Hit4WV 4	Hit4WV 3	Hit4WV 2	Hit4WV 1	Hit4WV 0
BCh	3Ch	TOF5	X	X	Hit5WV 5	Hit5WV 4	Hit5WV 3	Hit5WV 2	Hit5WV 1	Hit5WV 0	X	X	Hit6WV 5	Hit6WV 4	Hit6WV 3	Hit6WV 2	Hit6WV 1	Hit6WV 0
BDh	3Dh	TOF6	C_OFF SETRU P 7	C_OFF SETRU P6	C_OFF SETRU P5	C_OFF SETRU P4	C_OFF SETRU P3	C_OFF SETRU P2	C_OFF SETRU P1	C_OFF SETRU P0	C_OFF SETUP7	C_OFF SETUP6	C_OFF SETUP5	C_OFF SETUP4	C_OFF SETUP3	C_OFF SETUP2	C_OFF SETUP1	C_OFF SETUP0

Table 6. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]								BITS<7:0>							
BEh	3Eh	TOF7	C_OFFSETRDN7	C_OFFSETRDN6	C_OFFSETRDN5	C_OFFSETRDN4	C_OFFSETRDN3	C_OFFSETRDN2	C_OFFSETRDN1	C_OFFSETRDN0	C_OFFSETDN7	C_OFFSETDN6	C_OFFSETDN5	C_OFFSETDN4	C_OFFSETDN3	C_OFFSETDN2	C_OFFSETDN1	C_OFFSETDN0
BFh	3Fh	Event Timing 1	TDF3	TDF2	TDF1	TDF0	TDM4	TDM3	TDM2	TDM1	TDM0	TMF5	TMF4	TMF3	TMF2	TMF1	TMF0	X
C0h	40h	Event Timing 2	TMM4	TMM3	TMM2	TMM1	TMM0	Cal_Use	Cal_AUTO	Cal_CFG1	Cal_CFG0	X	X	PRECYC2	PRECYC1	PRECYC0	PORTCYC1	PORTCYC0
C1h	41h	TOF Measurement Delay	DLY15	DLY14	LY13	DLY12	DLY11	DLY10	DLY9	DLY8	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0
C2h	42h	Calibration and Control	X	X	X	X	CMP_EN	CMP_SEL	INT_EN	ET_CONT	CONT_INT	CLK_S2	CLK_S1	CLK_S0	Cal_Period3	Cal_Period2	Cal_Period1	Cal_Period0
C3h	43h	Real Time Clock	X	X	X	X	X	X	X	X	X	32K_BP	32K_EN	EOSC	AM2	AM1	WF	WD_EN
CONVERSION RESULTS REGISTERS																		
C4h	Read Only		WVRUP															
C5h	Read Only		Hit1UpInt															
C6h	Read Only		Hit1UpFrac															
C7h	Read Only		Hit2UpInt															
C8h	Read Only		Hit2UpFrac															
C9h	Read Only		Hit3UpInt															
CAh	Read Only		Hit3UpFrac															
CBh	Read Only		Hit4UpInt															

Table 6. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]	BITS[7:0]
CCh	Read Only		Hit4UpFrac	
CDh	Read Only		Hit5UpInt	
CEh	Read Only		Hit5UpFrac	
CFh	Read Only		Hit6UpInt	
D0h	Read Only		Hit6UpFrac	
D1h	Read Only		AVGUPInt	
D2h	Read Only		AVGUPFrac	
D3h	Read Only		WVRDN	
D4h	Read Only		Hit1DnInt	
D5h	Read Only		Hit1DnFrac	
D6h	Read Only		Hit2DnInt	
D7h	Read Only		Hit2DnFrac	
D8h	Read Only		Hit3DnInt	
D9h	Read Only		Hit3DnFrac	
DAh	Read Only		Hit4DnInt	
DBh	Read Only		Hit4DnFrac	
DCh	Read Only		Hit5DnInt	

Table 6. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]	BITS[7:0]
DDh	Read Only		Hit5DnFrac	
DEh	Read Only		Hit6DnInt	
DFh	Read Only		Hit6DnFrac	
E0h	Read Only		AVGDNInt	
E1h	Read Only		AVGDNFrac	
E2h	Read Only		TOF_DIFFInt	
E3h	Read Only		TOF_DIFFFrac	
E4h	Read Only		TOF_Cycle_Count	
E5h	Read Only		TOF_DIFF_AVGInt	
E6h	Read Only		TOF_DIFF_AVGFrac	
E7h	Read Only		T1Int	
E8h	Read Only		T1Frac	
E9h	Read Only		T2Int	
EAh	Read Only		T2Frac	
EFh	Read Only		Temp_Cycle_Count	
F0h	Read Only		T1_AVGInt	
F1h	Read Only		T1_AVGFrac	

Table 6. Register Memory Map (continued)

READ OPCODE	WRITE OPCODE	NAME	BITS[15:8]								BITS[7:0]							
F2h	Read Only		T2_AVGInt															
F3h	Read Only		T2_AVGFrac															
F8h	Read Only		CalibrationInt															
F9h	Read Only		CalibrationFrac															
FAh	Read Only		Reserved															
FBh	Read Only		Reserved															
FCh	Read Only		Reserved															
FDh	Read Only		Reserved															
STATUS REGISTERS																		
FEh	Read Only	Interrupt Status	TO	AF	X	TOF	TE	LDO	TOF_ EVTMG	Temp_ EVTMG	X	Cal	Halt	CSWI	INIT	POR	X	X
FFh	7Fh	Control	X	X	X	X	X	X	AFA	CSWA	X	X	X	X	X	X	X	X

RTC and Watchdog Register Descriptions

Table 7. RTC Seconds Register

RTC SECONDS REGISTER		
WRITE OPCODE **30h**	**READ OPCODE** **B0h**	**POR DEFAULT VALUE** **0000h**

Bit	15	14	13	12	11	10	9	8
Name	Tenths of Seconds				Hundredths of Seconds			

Bit	7	6	5	4	3	2	1	0
Name	0	10 Seconds			Seconds			

BIT	NAME	DESCRIPTION
15:12	Tenths of Seconds	Range 0 to 9
11:8	Hundredths of Seconds	Range 0 to 9
7	0	This bit always returns 0
6:4	10 Second	Range 0 to 5
3:0	Seconds	Range 0 to 9

Table 8. RTC Mins_Hrs Register

RTC MINS_HRS REGISTER		
WRITE OPCODE **31h**	**READ OPCODE** **B1h**	**POR DEFAULT VALUE** **0000h**

Bit	15	14	13	12	11	10	9	8
Name	0	10 Minutes			Minutes			

Bit	7	6	5	4	3	2	1	0
Name	0	12/24	20HR/AM/PM	10HR	Hours			

BIT	NAME	DESCRIPTION
15	0	This bit always returns 0
14:12	10 Minutes	Range 0 to 5
11:8	Minutes	Range 0 to 9
7	0	This bit always returns 0
6	12/24	1 = 12-Hour Mode 0 = 24-Hour Mode This bit is write only
5	20HR/AM/PM	In 12-Hour Mode 1 = PM 0 = AM In 24-Hour Mode: 20 Hour Digit
4	10HR	
3:0	Hours	Range 0 to 9

Table 9. RTC Day_Date Register

RTC DAY_DATE REGISTER								
WRITE OPCODE 32h			**READ OPCODE** B2h		**POR DEFAULT VALUE** 0000h			
Bit	15	14	13	12	11	10	9	8
Name	0	0	0	0	0	Day		
Bit	7	6	5	4	3	2	1	0
Name	0	0	10 Date		Date			

BIT	NAME	DESCRIPTION
15:11	0	These bits always return 0
10:8	Day	Range 0 to 7
7:6	0	These bits always return 0
5:4	10 Date	Range 0 to 3
3:0	Date	Range 0 to 9

Table 10. RTC Month_Year Register

RTC MONTH_YEAR REGISTER								
WRITE OPCODE 33h			**READ OPCODE** B3h		**POR DEFAULT VALUE** 0000h			
Bit	15	14	13	12	11	10	9	8
Name	0	0	0	10 Month	Month			
Bit	7	6	5	4	3	2	1	0
Name	10 Year				Year			

BIT	NAME	DESCRIPTION
15:13	0	These bits always return 0.
12	10 Month	Range 0 to 1
11:8	Month	Range 0 to 9
7:4	10 Year	Range 0 to 9
3:0	Year	Range 0 to 9

Table 11. Watchdog Alarm Counter Register

WATCHDOG ALARM COUNTER REGISTER								
WRITE OPCODE 34h			READ OPCODE B4h		POR DEFAULT VALUE 0000h			
Bit	15	14	13	12	11	10	9	8
Name	Tenths of Seconds				Hundredths of Seconds			
Bit	7	6	5	4	3	2	1	0
Name	10 Seconds				Seconds			

BIT	NAME	DESCRIPTION
15:12	Tenths of Seconds	Range 0 to 9
11:8	Hundredths of Seconds	Range 0 to 9
7:4	10 Second	Range 0 to 9
3:0	Seconds	Range 0 to 9

Table 12. Alarm Register

ALARM REGISTER								
WRITE OPCODE 35h			READ OPCODE B5h		POR DEFAULT VALUE 0000h			
Bit	15	14	13	12	11	10	9	8
Name	X	10 Minutes			Minutes			
Bit	7	6	5	4	3	2	1	0
Name	X	12/24	20HR/AM/PM	10HR	Hours			

BIT	NAME	DESCRIPTION
15	X	Reserved
14:12	10 Minutes	Range 0 to 5
11:8	Minutes	Range 0 to 9
7	X	Reserved
6	12/24	1 = 12-Hour Mode 0 = 24-Hour Mode This bit is write only
5	20HR/AM/PM	In 12-Hour Mode 1 = PM 0 = AM In 24-Hour Mode: 20 Hour Digit
4	10HR	
3:0	Hours	Range 0 to 9

Configuration Register Descriptions

Table 13. Switcher 1 Register

SWITCHER 1 REGISTER								
WRITE OPCODE 14h		READ OPCODE 94h		POR VALUE 0030h				
Bit	15	14	13	12	11	10	9	8
Name	SFREQ1	SFREQ0	HREG_D	0	X	X	X	X
Bit	7	6	5	4	3	2	1	0
Name	DFREQ1	DFREQ0	1	1	VS3	VS2	VS1	VS0

BIT	NAME	DESCRIPTION		
15:14	SFREQ [1:0]	**Switcher Control Frequency:** These 2 bits are used to control the switching frequency of the switcher boost circuit.		
		SFREQ1	**SFREQ0**	**SWITCHING FREQUENCY (kHz)**
		0	0	100
		0	1	125
		1	0	166
		1	1	200
13	HREG_D	**High Voltage Regulator Disable:** This bit powers down the high voltage regulator in the case where it is not desired and the switcher voltage is deem sufficient to drive the piezos. In such a case, the VPR and VP pins must be externally shorted together. When set to 0 the high voltage regulator is enabled. When set to 1 it is disabled.		
12	0	**Zero**: This bit must always be written to 0b when accessing this register. **WARNING:** Writing this bit to a non-zero value causes undesired device operation.		
11:8	X	Reserved		
7:6	DREQ[1:0]	**Doubler Control Frequency**: These 2 bits are used to control the switching frequency of the doubler circuit.		
		DREQ1	**DREQ0**	**SWITCHING FREQUENCY (kHz)**
		0	0	100
		0	1	125
		1	0	166
		1	1	200

Table 13. Switcher 1 Register (continued)

BIT	NAME	DESCRIPTION
5:4	11	**One**: These bits must always be written to 11b when accessing this register. **WARNING:** Writing these bits to a non-one value causes undesired device operation.
3:0	VS[3:0]	**Voltage Select:** This is a hex value that controls the switcher and high voltage regulator output target voltage:

VS0[3:0]	DESCRIPTION			
	REGULATOR TARGET (V)	SWITCHER TARGET (V)	MAX FET DUTY CYCLE (%)	
			LT_50D = 0b	LT_50D = 1b
0000b	5.4	9	50	50
0001b	5.4	9	50	50
0010b	5.4	9	50	50
0011b	5.4	9	50	50
0100b	5.4	9	50	60
0101b	7.2	10.8	50	63
0110b	9	12.6	50	65
0111b	11.4	15	50	68
1000b	13.2	16.8	50	70
1001b	15.6	19.2	50	73
1010b	17.4	21	50	73
1011b	19.2	22.8	50	78
1100b	21.6	25.2	50	80
1101b	23.4	27	50	83
1110b	25.2	28.8	50	85
1111b	27	30.6	50	90

Table 14. Switcher 2 Register

SWITCHER 2 REGISTER								
WRITE OPCODE 15h		READ OPCODE 95h		POR VALUE 44E0h				
Bit	15	14	13	12	11	10	9	8
Name	LT_N3	LT_N2	LT_N1	LT_N0	LT_S3	LT_S2	LT_S1	LT_S0
Bit	7	6	5	4	3	2	1	0
Name	ST3	ST2	ST1	ST0	LD_50D	0	0	PECHO

BIT	NAME	DESCRIPTION	
15:12	LT_N[3:0]	**Limit trim Normal Operation:** After the output voltage crosses the undervoltage good threshold, which is the programmed voltage select output, the switcher runs in normal duty mode. Four bits control the max inductor current in normal duty mode. The bits must be set in the one-hot pattern shown below.	
		LT_N[3:0]	0000b = Loop conditions determine max 0001b = 0.2V/RSENSE = MAX CURRENT 0010b = 0.4V/RSENSE = MAX CURRENT 0100b = 0.8V/RSENSE = MAX CURRENT 1000b = 1.6V/RSENSE = MAX CURRENT
11:8	LT_S[3:0]	**Limit trim Startup:** During power up, a soft-start must be initiated as the inductor can saturate from a maxed out duty cycle arising from the large error between target and the output voltage. Four bits control the max inductor current. The bits must be set in the one-hot pattern shown below.	
		LT_S[3:0]	0000b = No limit 0001b = 0.2V/RSENSE = MAX CURRENT 0010b = 0.4V/RSENSE = MAX CURRENT 0100b = 0.8V/RSENSE = MAX CURRENT 1000b = 1.6V/RSENSE = MAX CURRENT

Table 14. Switcher 2 Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="18">7:4</td><td rowspan="18">ST[3:0]</td><td colspan="2">Switcher Stabilization Time: This is a hex number that selects the time allotted for the stabilization of the output voltage of the switcher. This count begins once the under voltage comparator determines the target output voltage is within the defined specifications. After the stabilization time expires the launch pulses are then transmitted.
The time is based upon the 32.768 KHz crystal.</td></tr>
<tr><td>ST[3:0]</td><td>STABILIZATION TIME</td></tr>
<tr><td>0000b</td><td>64µs</td></tr>
<tr><td>0001b</td><td>128µs</td></tr>
<tr><td>0010b</td><td>192µs</td></tr>
<tr><td>0011b</td><td>256µs</td></tr>
<tr><td>0100b</td><td>320µs</td></tr>
<tr><td>0101b</td><td>384µs</td></tr>
<tr><td>0110b</td><td>473µs</td></tr>
<tr><td>0111b</td><td>512µs</td></tr>
<tr><td>1000b</td><td>768µs</td></tr>
<tr><td>1001b</td><td>1.02ms</td></tr>
<tr><td>1010b</td><td>1.25ms</td></tr>
<tr><td>1011b</td><td>1.50ms</td></tr>
<tr><td>1100b</td><td>2.05ms</td></tr>
<tr><td>1101b</td><td>4.10ms</td></tr>
<tr><td>1110b</td><td>8.19ms</td></tr>
<tr><td>1111b</td><td>16.4ms</td></tr>
<tr><td>3</td><td>LT_50D</td><td colspan="2">LIMIT TRIM 50% Disable: This bit disables the 50% MAX duty cycle applied to the switcher FET.
When set to 0 the switcher FET’s applied MAX duty cycle will never exceed a 50%
When set to a 1 the switcher FET’s applied MAX duty cycle will dependent upon the settings in the Launch Voltage Select, VS[3:0], bit field in the Switcher 1 Register.</td></tr>
<tr><td>2:1</td><td>0</td><td colspan="2">Zero: These bits must always be written to 00b when accessing this register.
WARNING: Writing these bits to a non-zero value will cause undesired device operation</td></tr>
<tr><td>0</td><td>PECHO</td><td colspan="2">Pulse Echo enable: This bit enables the pulse echo mode of the device. In pulse echo mode the launch transducer is also the receive transducer.
When set to 1 the device operates in pulse echo mode.
When set to 0 the device operates in normal time of flight mode.</td></tr>
</table>

Table 15. AFE 1 Register

AFE 1 REGISTER		
WRITE OPCODE **16h**	**READ OPCODE** **96h**	**POR VALUE** **04Xxh**

Bit	15	14	13	12	11	10	9	8
Name	AFE_BP	0	0	0	0	SD_EN	AFEOUT1	AFEOUT0

Bit	7	6	5	4	3	2	1	0
Name	0	WRITE BACK READ VALUES						

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>15</td><td>AFE_BP</td><td colspan="3">Analog Front-End Bypass: This bit is used to remove the entire analog front-end signal chain, including both gain stages and the bandpass filter, from the return signal-chain path.
When set to 1, externally connecting the RXN/RXP pins to the CIN/CIP pins is required.
When set to 0 the return signals are routed to the first gain stage of the analog front-end.</td></tr>
<tr><td>14:11</td><td>0</td><td colspan="3">Zero: These bits must always be written to 0000b when accessing this register.
WARNING: Writing these bits to a non-zero value will cause undesired device operation</td></tr>
<tr><td>10</td><td>SD_EN</td><td colspan="3">Single Ended Drive Enable: This bit enables the transmitted square wave to be driven in a single ended manner. When set to 0, the transmitted square wave will be driven differentially.</td></tr>
<tr><td rowspan="6">9:8</td><td rowspan="6">AFEOUT[1:0]</td><td colspan="3">Analog Front End Output: These bits enable the AFE signals to be output on the CIP/CIN pins according to the following stage output</td></tr>
<tr><td>AFEOUT1</td><td>AFEOUT0</td><td>DESCRIPTION</td></tr>
<tr><td>0</td><td>0</td><td>CIP/CIN output disabled</td></tr>
<tr><td>0</td><td>1</td><td>Route bandpass filter out</td></tr>
<tr><td>1</td><td>0</td><td>Route programmable gain amplifier out</td></tr>
<tr><td>1</td><td>1</td><td>Route fixed gain amplifier out</td></tr>
<tr><td>7</td><td>0</td><td colspan="3">Zero: This bit must always be written to 0b when accessing this register.
WARNING: Writing this b it to a non-zero value will cause undesired device operation</td></tr>
<tr><td>6:0</td><td>WB</td><td colspan="3">Write Back: This bit field must be written back to the initial value that is read from the device after a POR, before it is modified. When writing this register a POR read must occur first and the value of these 7 bits must be stored in the host microcontroller. Any future writes to this register must write this 7-bit bit-field to the value that was initially read.
WARNING :Writing these bits to a value that does not match the initial POR read value will cause undesired device operation</td></tr>
</table>

Table 16. AFE 2 Register

AFE 2 REGISTER		
WRITE OPCODE 17h	**READ OPCODE 97h**	**POR VALUE 0000h**

Bit	15	14	13	12	11	10	9	8
Name	4M_BP	F06	F05	F04	F03	F02	F01	F00

Bit	7	6	5	4	3	2	1	0
Name	PGA3	PGA2	PGA1	PGA0	LOWQ1	LOWQ0	0	BP_BP

BIT	NAME	DESCRIPTION
15	4M_BP	**4MHz Bypass:** This bit, when set, allows an external CMOS-level 4.0 MHz signal to be applied to the 4MX1 device pin. The internal 4MHz oscillator is bypassed and the external signal is driven into the device's core.
14:8	F0[6:0]	**F0 Adjust:** This is a hex value that adjusts the center frequency of the bandpass filter. Use the Bandpass Calibrate Command (06h) and the device will automatically select the best center frequency based upon the selected launch frequency. These bits will be set automatically by the device.
7:4	PGA[3:0]	**Gain Select:** This is a hex value that selects the gain for the programmable gain amplifier:

PGA[3:0]	AMPLIFIER GAIN	
	dB	**V/V**
0000b	10	3.16
0001b	11.33	3.69
0010b	12.66	4.30
0011b	13.99	5.01
0100b	15.32	5.83
0101b	16.65	6.80
0110b	17.98	7.93
0111b	19.31	9.24
1000b	20.64	10.76
1001b	21.97	12.55
1010b	23.30	14.62
1011b	24.63	17.04
1100b	25.96	19.86
1101b	27.29	23.15
1110b	28.62	26.98
1111b	29.95	31.44

Table 16. AFE 2 Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">LOWQ[1:0]</td><td colspan="3">BPF Q Select: These 2 bits are used to lower the Q factor of the filter</td></tr>
<tr><td>LOWQ1</td><td>LOWQ2</td><td>FILTER Q (Hz/Hz)</td></tr>
<tr><td>0</td><td>0</td><td>12</td></tr>
<tr><td>0</td><td>1</td><td>7.4</td></tr>
<tr><td>1</td><td>0</td><td>5.3</td></tr>
<tr><td>1</td><td>1</td><td>4.2</td></tr>
<tr><td>1</td><td>0</td><td colspan="3">Zero: This bit must always be written to 0b when accessing this register.
WARNING :Writing this bit to a non-zero value will cause undesired device operation</td></tr>
<tr><td>0</td><td>BP_BP</td><td colspan="3">Bandpass Filter Bypass: This bit is used to remove the tunable bandpass filter from the return signal-chain path. When the bandpass filter is bypassed, the return signals present at the input of the tunable bandpass filter are routed directly to programmable offset comparator.
When set to 0 the BPF is used to condition the return signal. When set to 1 the BPF is bypassed.</td></tr>
</table>

Table 17. TOF1 Register

<table>
<tr><th colspan="9">TOF1 REGISTER</th></tr>
<tr><td colspan="9"></td></tr>
<tr><td colspan="2">WRITE OPCODE
38h</td><td colspan="2">READ OPCODE
B8h</td><td colspan="5">POR DEFAULT VALUE
0000h</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Name</td><td>PL7</td><td>PL6</td><td>PL5</td><td>PL4</td><td>PL3</td><td>PL2</td><td>PL1</td><td>PL0</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Name</td><td>DPL3</td><td>DPL2</td><td>DPL1</td><td>DPL0</td><td>STOP_POL</td><td>X</td><td>X</td><td>X</td></tr>
</table>

Table 17. TOF1 Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>15:8</td><td>PL[7:0]</td><td colspan="2">Pulse Launcher Size: This is a hex value that defines the number of pulses that are launched from the pulse launcher during transmission. The range of this hex value is 00h–FFh. When PL[7:0] is set to 00h, the Pulse Launcher is disabled. Up to 127 pulses can be launched. When PL7 is set, the pulse count is clamped at 127.</td></tr>
<tr><td rowspan="8">7:4</td><td rowspan="8">DPL[3:0]</td><td colspan="2">Pulse Launch Divider: This is a hex value that defines the divider ratio of the internal clock signal used to drive the Pulse Launch signal. The 4 MHz external reference oscillator is used as the source for the internal clock reference. The internal reference clock is first divided by 2 to produce a 2MHz clock. The range of this hex value is 1h to Fh, resulting in a range of division from ÷2 to ÷16 of the 2 MHz clock. A value of 0h is not supported and should not be programmed.

Pulse Launch Frequency = 2MHz / (1+DPL[3:0])</td></tr>
<tr><td>DPL[3:0]</td><td>PULSE LAUNCH FREQUENCY</td></tr>
<tr><td>0000b</td><td>RESERVED</td></tr>
<tr><td>0001b</td><td>1MHz</td></tr>
<tr><td>0002b</td><td>666kHz</td></tr>
<tr><td>. . .</td><td>. . .</td></tr>
<tr><td>1110b</td><td>133.33kHz</td></tr>
<tr><td>1111b</td><td>125kHz</td></tr>
<tr><td>3</td><td>STOP_POL</td><td colspan="2">Stop Polarity: This bit defines the edge sensitivity of the internal programmable stop comparator. The comparator generates a stop condition for the internal TDC time count on the rising slope of the received signal if this bit is set to 0. The comparator generates a stop condition for the internal TDC time count on the falling slope of the received signal if this bit is set to 1.</td></tr>
<tr><td>2:0</td><td>X</td><td colspan="2">Reserved</td></tr>
</table>

Table 18. TOF2 Register

TOF2 REGISTER								
WRITE OPCODE 39h		**READ OPCODE B9h**		**POR DEFAULT VALUE 0000h**				
Bit	15	14	13	12	11	10	9	8
Name	STOP2	STOP1	STOP0	T2WV5	T2WV4	T2WV3	T2WV2	T2WV1
Bit	7	6	5	4	3	2	1	0
Name	T2WV0	TOF_CYC2	TOF_CYC1	TOF_CYC0	X	TIMOUT2	TIMOUT1	TIMOUT0

BIT	NAME	DESCRIPTION			
15:13	STOP[2:0]	**Stop Hits:** These bits set the number of stop hits to be expected and measured.			
		STOP2	**STOP1**	**STOP0**	**DESCRIPTION**
		0	0	0	1 Hit
		0	0	1	2 Hits
		0	1	0	3 Hits
		0	1	1	4 Hits
		1	0	0	5 Hits
		1	0	1	6 Hits
		1	1	0	6 Hits
		1	1	1	6 Hits
12:7	T2WV[5:0]	**Wave Selector for t_2:** These bits determine the wave number for which t_2 is measured. To ensure measurement accuracy, the first wave measurable after the Early Edge Detect is Wave 2. Waves are numbered as depicted in Figure 5B.			
		T2WV[5:0] (decimal)		**DESCRIPTION**	
		0 through 2		Wave 2	
		3		Wave 3	
		4		Wave 4	
		5 through 63		Wave 5 through 63	

Table 18. TOF2 Register (continued)

BIT	NAME	DESCRIPTION
6:4	TOF_CYC [2:0]	**TOF Duty Cycle:** These bits determine the time delay between successive executions of TOF measurements. It is the Start-to-Start time of automatic execution of the TOF_UP and the TOF_DN and is applicable only for the TOF_DIFF command. It is based upon the 32.768kHz crystal. If the actual TOF of the acoustic path exceeds the programmed Start-to-Start time in this setting, then the TOF Duty Cycle performs as if the bit setting is 000b.

TOF_CYC[2:0]	DESCRIPTION		
	32kHz CLOCK CYCLES(decimal)	TYPICAL TIME	4MHz ON BETWEEN TOF_UP AND TOF_DOWN
000b	0	0µs	Yes
001b	4	122µs	Yes
010b	8	244µs	Yes
011b	16	488µs	Yes
100b	24	732µs	Yes
101b	32	976µs	Yes
110b	546	16.65ms	No
111b	655	19.97ms	No

BIT	NAME	DESCRIPTION
3	X	Reserved
2:0	TIMOUT [2:0]	**Timeout:** These bits force a timeout in the Time-To-Digital measurement block. If the hit required to measure t_1, t_2, or Hit1 thru Hit6 of the received signal does not occur in this time, the TO bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ pin is asserted (if enabled). Additionally, any of the Conversion Results registers read FFFFh if the data for that register is invalid. In addition, if resultant temperature readings exceed the timeout value set by these bits, then the device writes a value of FFFFh to the corresponding T1, T2, T3, T4 Results register to indicate an open circuit temperature probe.

TIMOUT2	TIMOUT1	TIMOUT0	DESCRIPTION
0	0	0	128µs
0	0	1	256µs
0	1	0	512µs
0	1	1	1024µs
1	0	0	2048µs
1	0	1	4096µs
1	1	0	8192µs
1	1	1	16384µs

Table 19. TOF3 Register

TOF3 REGISTER								
WRITE OPCODE **3Ah**		**READ OPCODE** **BAh**		**POR DEFAULT VALUE** **0000h**				
Bit	15	14	13	12	11	10	9	8
Name	X	X	Hit1WV5	Hit1WV4	Hit1WV3	Hit1WV2	Hit1WV1	Hit1WV0
Bit	7	6	5	4	3	2	1	0
Name	X	X	Hit2WV5	Hit2WV4	Hit2WV3	Hit2WV2	Hit2WV1	Hit2WV0

BIT	NAME	DESCRIPTION	
15:14	X	Reserved	
13:8	HIT1WV[5:0]	**Hit1 Wave Select**: These bits select the wave number for which the Hit1 stop time is measured. Wave Numbers are depicted in Figure 5B. The Hit1 Wave Select value must be at least 1 greater than the Wave Selected for t_2, which is configured in the TOF2 register. For example, if the Wave Selector for t_2 is set to wave number 7, then the Hit1 Wave Select must be set to deselect wave number 8 or greater. The earliest wave for which Hit1 can be measured is Wave 3.	
		HIT1WV[5:0] (decimal)	**DESCRIPTION**
		0 to 3	Wave 3
		4	Wave 4
		5	Wave 5
		6 to 63	Wave 6 to 63
7:6	X	Reserved	
5:0	HIT2WV[5:0]	**Hit2 Wave Select:** These bits select the wave number for which the Hit2 stop time is measured. Wave numbers are depicted in Figure 5B. The Hit2 Wave Select value must be at least 1 greater than the Hit1 Wave Select value. For example, if Hit1 Wave Select value is set to measure wave number 9, then the Hit2 Wave Select must be set to detect wave number 10 or greater. The earliest wave for which Hit2 can be measured is Wave 4.	
		HIT2WV[5:0] (decimal)	**DESCRIPTION**
		0 to 4	Wave 4
		5	Wave 5
		6	Wave 6
		7 to 63	Wave 7 to 63

Table 20. TOF4 Register

TOF4 REGISTER								
WRITE OPCODE 3Bh		READ OPCODE BBh		POR DEFAULT VALUE 0000h				
Bit	15	14	13	12	11	10	9	8
Name	X	X	Hit3WV5	Hit3WV4	Hit3WV3	Hit3WV2	Hit3WV1	Hit3WV0
Bit	7	6	5	4	3	2	1	0
Name	X	X	Hit4WV5	Hit4WV4	Hit4WV3	Hit4WV2	Hit4WV1	Hit4WV0

BIT	NAME	DESCRIPTION	
15:14	X	Reserved	
13:8	HIT3WV[5:0]	**Hit3 Wave Select:** These bits select the wave number for which the Hit3 stop time is measured. Wave numbers are depicted in Figure 5B. The Hit3 Wave Select value must be at least 1 greater than the Hit2 Wave Select value. For example, if the Hit2 Wave Select value is set to measure wave number 10, then the Hit3 Wave Select must be set to detect wave number 11 or greater. The earliest wave for which Hit3 can be measured is Wave 5.	
		HIT3WV[5:0] (decimal)	**DESCRIPTION**
		0 to 5	Wave 5
		6	Wave 6
		7	Wave 7
		8 to 63	Wave 8 to 63
7:6	X	Reserved	
5:0	HIT4WV[5:0]	**Hit4 Wave Select:** These bits select the wave number for which the Hit4 stop time is measured. Wave numbers are depicted in Figure 5B. The Hit4 Wave Select value must be at least 1 greater than the Hit3 Wave Select value. For example, if the Hit3 Wave Select value is set to measure wave number 11, then the Hit4 Wave Select must be set to detect wave number 12 or greater. The earliest wave for which Hit4 can be measured is Wave 6.	
		HIT4WV[5:0] (decimal)	**DESCRIPTION**
		0 to 6	Wave 6
		7	Wave 7
		8	Wave 8
		9 to 63	Wave 9 to 63

Table 21. TOF5 Register

TOF5 REGISTER								
WRITE OPCODE 3Ch		READ OPCODE BCh		POR DEFAULT VALUE 0000h				
Bit	15	14	13	12	11	10	9	8
Name	X	X	Hit5WV5	Hit5WV4	Hit5WV3	Hit5WV2	Hit5WV1	Hit5WV0
Bit	7	6	5	4	3	2	1	0
Name	X	X	Hit6WV5	Hit6WV4	Hit6WV3	Hit6WV2	Hit6WV1	Hit6WV0

BIT	NAME	DESCRIPTION	
15:14	X	Reserved	
13:8	HIT5WV [5:0]	**Hit5 Wave Select**: These bits select the wave number for which the Hit5 stop time is measured. Wave numbers are depicted in Figure 5B. The Hit5 Wave Select value must be at least 1 greater than the Hit4 Wave Select value. For example, if the Hit4 Wave Select value is set to measure wave number 12, then the Hit5 Wave Select must be set to detect wave number 13 or greater. The earliest wave for which Hit5 can be measured is Wave 7.	
		HIT5WV[5:0] (decimal)	**DESCRIPTION**
		0 to 7	Wave 7
		8	Wave 8
		9	Wave 9
		10 to 63	Wave 10 to 63
7:6	X	Reserved	
5:0	HIT5WV [5:0]	**Hit6 Wave Select:** These bits select the wave number for which the Hit6 stop time is measured. Wave numbers are depicted in Figure 5B. Hit6 Wave Select value must at least 1 greater than the Hit5 Wave Select value. For example, if Hit5 Wave Select value is set to measure wave number 13, then the Hit6 Wave Select must be set to detect wave number 14 or greater. The earliest wave for which Hit6 can be measured is Wave 8.	
		HIT4WV[5:0] (decimal)	**DESCRIPTION**
		0 to 8	Wave 8
		9	Wave 9
		10	Wave 10
		11 to 63	Wave 11 to 63

Table 22. TOF6 Register

TOF6 REGISTER								
WRITE OPCODE 3Dh			**READ OPCODE BDh**		**POR DEFAULT VALUE 0000h**			
Bit	15	14	13	12	11	10	9	8
Name	C_OFFSET UPR7	C_OFFSET UPR6	C_OFFSET UPR5	C_OFFSET UPR4	C_OFFSET UPR3	C_OFFSET UPR2	C_OFFSET UPR1	C_OFFSET UPR0
Bit	7	6	5	4	3	2	1	0
Name	X	C_OFFSET UP6	C_OFFSET UP5	C_OFFSET UP4	C_OFFSET UP3	C_OFFSET UP2	C_OFFSET UP1	C_OFFSET UP0

BIT	NAME	DESCRIPTION	
15:8	C_OFFSETUPR[7:0]	**Comparator Return Offset Upstream:** When the device is measuring the t_2 wave, the programmed receive comparator offset is returned to a common mode voltage automatically after the Early Edge, t_1, is detected. The actual offset return voltage is dependent upon and scales with the voltage present at the V_{CC} pins. The following formula defines the Comparator Return Offset voltage setting, where C_OFFSETUPR is a two's-complement number: $\text{Comparator Return Offset Voltage} = V_{CC} \times \frac{1152 + \text{C\_OFFSETUPR}}{3072}$ $\text{where 1 LSB} = \frac{V_{CC}}{3072}$	
		C_OFFSETUPR[6:0]	**OFFSET (LSBs)**
		7Fh to 01h	127 to 1
		00h	0
		80h to FFh	-128 to -1
7	X	Reserved	

Table 22. TOF6 Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="3">6:0</td><td rowspan="3">C_OFFSETUP [6:0]</td><td colspan="2">Comparator Offset Upstream: These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the Early Edge wave, t_1. The actual common mode voltage is dependent upon and scales with the voltage present at the V_{CC} pins.

When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection of the zero crossing of the received acoustic wave, then the Comparator Offset is a positive value. When the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection of the zero crossing of the received acoustic wave, then the Comparator Offset is a negative value.

The following formulas define the Comparator Offset voltage setting

$$\text{STOP\_POL} = 0 \text{ Comparator Offset Voltage} = V_{CC} \times \frac{1152 + \text{C\_OFFSETUP}}{3072}$$
$$\text{STOP\_POL} = 1 \text{ Comparator Offset Voltage} = V_{CC} \times \frac{1151 - \text{C\_OFFSETUP}}{3072}$$
$$\text{where 1 LSB} = \frac{V_{CC}}{3072}$$</td></tr>
<tr><td>C_OFFSETUP[6:0]</td><td>OFFSET (LSBs)</td></tr>
<tr><td>00h to 7Fh</td><td>0 to 127</td></tr>
</table>

Table 23. TOF7 Register

TOF7 REGISTER		
WRITE OPCODE **3Eh**	**READ OPCODE** **BEh**	**POR DEFAULT VALUE** **0000h**

Bit	15	14	13	12	11	10	9	8
Name	C_OFFSET DNR7	C_OFFSET DNR6	C_OFFSET DNR5	C_OFFSET DNR4	C_OFFSET DNR3	C_OFFSET DNR2	C_OFFSET DNR1	C_OFFSET DNR0
Bit	7	6	5	4	3	2	1	0
Name	X	C_OFFSET DN6	C_OFFSET DN5	C_OFFSET DN4	C_OFFSET DN3	C_OFFSET DN2	C_OFFSET DN1	C_OFFSET DN0

BIT	NAME	DESCRIPTION
15:8	C_OFFSETDNR [7:0]	**Comparator Return Offset Downstream:** When the device is measuring the t2 wave, the programmed receive comparator offset is returned to a common mode voltage automatically after the Early Edge, t_1, is detected. The actual offset return voltage is dependent upon and scales with the voltage present at the V_{CC} pins. The following formula defines the Comparator Return Offset voltage setting, where C_OFFSETDNR is a two's-complement number: $\text{Comparator Return Offset Voltage} = V_{CC} \times \frac{1152 + \text{C\_OFFSETDNR}}{3072}$ $\text{where 1 LSB} = \frac{V_{CC}}{3072}$
7	X	Reserved

C_OFFSETDNR[6:0]	OFFSET (LSBs)
7Fh to 01h	127 to 1
00h	0
80h to FFh	-128 to -1

Table 23. TOF7 Register (continued)

BIT	NAME	DESCRIPTION
6:0	C_OFFSETDN [6:0]	**Comparator Offset Downstream:** These bits define an initial selected receive comparator offset voltage for the analog receiver comparator front-end. This comparator offset is used to detect the Early Edge wave, t_1. The actual common mode voltage is dependent upon and scales with the voltage present at the V_{CC} pins. When the STOP_POL bit in the TOF1 register is set to zero indicating a rising edge detection of the zero crossing of the received acoustic wave, then the Comparator Offset is a positive value. When the STOP_POL bit in the TOF1 register is set to one indicating a falling edge detection of the zero crossing of the received acoustic wave, then the Comparator Offset is a negative value. The following formulas define the Comparator Offset voltage setting: $\text{STOP\_POL} = 0 \text{ Comparator Offset Voltage } = V_{CC} \times \frac{1152 + C_{OFFSETUP}}{3072}$ $\text{STOP\_POL} = 1 \text{ Comparator Offset Voltage } = V_{CC} \times \frac{1151 - C_{OFFSETUP}}{3072}$ $\text{where 1 LSB} = \frac{V_{CC}}{3072}$

C_OFFSETDN[6:0]	OFFSET (LSBs)
00h to 7Fh	0 to 127

Table 24. Event Timing 1 Register

<table>
<tr><th colspan="9">EVENT TIMING 1 REGISTER</th></tr>
<tr><td colspan="9"></td></tr>
<tr><td colspan="3">WRITE OPCODE
3Fh</td><td colspan="2">READ OPCODE
BFh</td><td colspan="4">POR DEFAULT VALUE
0000h</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>Name</td><td>TDF3</td><td>TDF2</td><td>TDF1</td><td>TDF0</td><td>TDM4</td><td>TDM3</td><td>TDM2</td><td>TDM1</td></tr>
<tr><td colspan="9"></td></tr>
<tr><td>Bit</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Name</td><td>TDM0</td><td>TMF5</td><td>TMF4</td><td>TMF3</td><td>TMF2</td><td>TMF1</td><td>TMF0</td><td>X</td></tr>
</table>

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="6">15:12</td><td rowspan="6">TDF[3:0]</td><td colspan="2">TOF Difference Measurement Frequency: These bits define the rate at which TOF_DIFF measurements are executed when the EVTMG1 or EVTMG2 command is executed.

Rate = 0.5s + (TDF[3:0] x 0.5s) + randomizer value</td></tr>
<tr><td>TDF[3:0] (decimal)</td><td>RATE (s)</td></tr>
<tr><td>0</td><td>0.5</td></tr>
<tr><td>1</td><td>1.0</td></tr>
<tr><td>. . .</td><td>. . .</td></tr>
<tr><td>14</td><td>7.5</td></tr>
<tr><td rowspan="6">11:7</td><td rowspan="6">TDM[4:0]</td><td colspan="2">TOF Difference Measurements: These bits define the number of TOF_DIFF measurement cycles to be executed when the EVTMG1 or EVTMG2 command is executed.

Cycles = 1+ TDM[4:0]</td></tr>
<tr><td>TDM[4:0] (decimal)</td><td>CYCLES</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>. . .</td><td>. . .</td></tr>
<tr><td>30</td><td>31</td></tr>
<tr><td rowspan="6">6:1</td><td rowspan="6">TMF[5:0]</td><td colspan="2">Temperature Measurement Frequency: These bits define the time delay between temperature cycle measurements. It is a start-cycle to start-cycle time duration at which temperature measurement cycles are executed when the EVTMG1 or EVTMG3 command is executed.

Rate = 1.0s + (TMF[3:0] * 1.0s) + randomizer value</td></tr>
<tr><td>TMF[5:0] (decimal)</td><td>RATE (S)</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>2</td></tr>
<tr><td>. . .</td><td>. . .</td></tr>
<tr><td>62</td><td>63</td></tr>
<tr><td>0</td><td>X</td><td colspan="2">Reserved</td></tr>
</table>

Table 25. Event Timing 2 Register

EVENT TIMING 2 REGISTER		
WRITE OPCODE 40h	**READ OPCODE** C0h	**POR DEFAULT VALUE** 0000h

Bit	15	14	13	12	11	10	9	8
Name	TMM4	TMM3	TMM2	TMM1	TMM0	CAL_USE	CAL_CFG2	CAL_CFG1
Bit	7	6	5	4	3	2	1	0
Name	CAL_CFG0	X	X	PRECYC2	PRECYC1	PRECYC0	PORTCYC1	PORTCYC0

BIT	NAME	DESCRIPTION	
15:11	TMM[4:0]	**Temperature Measurements:** These bits define the number of temperature measurement cycles to be executed when the EVTMG1 or EVTMG3 command is executed. Cycles = 1+ TMM[4:0]	
		TMM[4:0] (decimal)	**CYCLES**
		0	1
		1	2
		. . .	. . .
		30	31
10	CAL_USE	**Calibration Usage:** This bit, when set, causes the device to use the calibration data in the CalibrationInt and CalibrationFrac registers during measurement, averaging and accumulation of data while executing the EVTMG commands. All time measurements are scaled using the calibration factors as described by the Calibrate command.	
9:7	CAL_CFG[2:0]	**Calibration Configuration:** These bits define the point in the EVTMGx cycle/sequence where the automatic Calibration command is executed.	
		CAL_CFG[2:0]	**DESCRIPTION** During EVTMGx sequences, automatic execution of the Calibrate command occurs at:
		000b to 011b	Auto Calibration Disabled
		100b	The beginning of each TOF_DIFF cycle The beginning of each Temperature cycle
		101b	The beginning of each TOF_DIFF cycle The beginning of each Temperature sequence
		110b	Once at the beginning of each TOF_DIFF sequence The beginning of each Temperature cycle
		111b	Once at the beginning of each TOF_DIFF sequence The beginning of each Temperature sequence
6:5	X	Reserved	

Table 25. Event Timing 2 Register (continued)

BIT	NAME	DESCRIPTION			
4:2	PRECYC[2:0]	**Preamble Temperature Cycle:** These 3 bits are used to set the number of cycles to use as preamble for reducing dielectric absorption of the temperature measurement capacitor. Each cycle is comprised of one temperature measurement sequence as defined by the TP[1:0] bits.			
		PRECYC2	**PRECYC1**	**PRECYC0**	**DESCRIPTION**
		0	0	0	0 Dummy Cycle
		0	0	1	1 Dummy Cycles
		0	1	0	2 Dummy Cycles
		0	1	1	3 Dummy Cycles
		1	0	0	4 Dummy Cycles
		1	0	1	5 Dummy Cycles
		1	1	0	6 Dummy Cycles
		1	1	1	7 Dummy Cycles
1:0	PORTCYC[1:0]	**Port Cycle Time:** These two bits define the time interval between successive individual temperature port measurements. It is a start-to-start time. These bits also define the timeout function of the temperature measurement ports. See the Temperature Operation Sections for timeout details.			
		PORTCYC1	**PORTCYC0**	**DESCRIPTION (µs)**	
		0	0	128	
		0	1	256	
		1	0	384	
		1	1	512	

Table 26. TOF Measurement Delay Register

TOF MEASUREMENT DELAY REGISTER								
WRITE OPCODE 41h			**READ OPCODE C1h**		**POR DEFAULT VALUE 0000h**			
Bit	15	14	13	12	11	10	9	8
Name	DLY15	DLY14	DLY13	DLY12	DLY11	DLY10	DLY9	DLY8
Bit	7	6	5	4	3	2	1	0
Name	DLY7	DLY6	DLY5	DLY4	DLY3	DLY2	DLY1	DLY0

BIT	NAME	DESCRIPTION
15:0	DLY[15:0]	This is hexadecimal value ranging from 0000h to FFFFh (Decimal 0 to 65535). It is a multiple of the 4MHz crystal period (250ns). The minimum setting is 0064h, which is equivalent to 25µs. The analog comparator driven by the bandpass filter does not generate a stop condition until this delay, counted from the internally generated start pulse for the acoustic wave, has expired. This delay applies to Early Edge Detect wave. Care must be taken to set the TIMOUT bits in the TOF2 register so that a timeout interrupt does not occur before this delay expires.

Table 27. Calibration and Control Register

CALIBRATION AND CONTROL REGISTER								
WRITE OPCODE 42h			READ OPCODE C2h		POR DEFAULT VALUE 0000h			
Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	CMP_EN	CMP_SEL	INT_EN	ET_CONT
Bit	7	6	5	4	3	2	1	0
Name	CONT_INT	CLK_S2	CLK_S1	CLK_S0	CAL_ PERIOD3	CAL_ PERIOD2	CAL_ PERIOD1	CAL_ PERIOD0

BIT	NAME	DESCRIPTION
15:12	X	Reserved
11	CMP_EN	**Comparator/UP_DN Output Enable :** 1 = CMP_OUT/UP_DN output device pin is enabled. 0 = CMP_OUT/UP_DN output device pin is driven low.
10	CMP_SEL	**Comparator/UP_DN Output Select:** This bit selects the output function of the CMP_OUT/UP_DN pin and is only used when CMP_EN = 1. 1 = CMP_EN: The output monitors the receiver front-end comparator output. 0 = UP_DN: The output monitors the launch direction of the pulse launcher. High Output: Upstream measurement (TX_UP to TX_DN) Low Output: Downstream measurement (TX_DN to TX_UP)
9	INT_EN	**Interrupt Enable:** This bit, when set, enables the $\overline{INT}$ pin. All interrupt sources are wire-ORed to the $\overline{INT}$ pin.
8	ET_CONT	**Event Timing Continuous Operation:** This bit, when set, causes the currently executing EVTMGx command to continuously execute until the HALT command is received by the device. This bit, when cleared, causes: • The currently executing EVTMG1 command to run one sequence of TOF_DIFF measurement cycles and/or one sequence of temperature measurement. • The currently executing EVTMG2 command to run one sequence of TOF_DIFF measurements cycles. • The currently executing EVTMG3 command to run one sequence of temperature measurement cycles.
7	CONT_INT	**Continuous Interrupt:** This bit, when set, causes the currently executing EVTMGx command to assert the $\overline{INT}$ pin (if enabled) after every TOF_DIFF or Temperature measurement cycle. This allows the host microprocessor to interrogate the current Event for accuracy of measurements and hit data. When this bit is cleared, the currently executing EVTMGx command interrupt-generation behavior is controlled only by the setting of the ET_CONT bit.

Table 27. Calibration and Control Register (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th colspan="5">DESCRIPTION</th></tr>
<tr><td rowspan="11">6:4</td><td rowspan="11">CLK_S[2:0]</td><td colspan="5">Clock Settling Time: These bits define the time interval that the device waits after enabling the 4MHz clock for it to stabilize before making any measurements of time or temperature.</td></tr>
<tr><th rowspan="2">CLK_S2</th><th rowspan="2">CLK_S1</th><th rowspan="2">CLK_S0</th><th colspan="2">DESCRIPTION</th></tr>
<tr><th>32kHz CLOCK CYCLES</th><th>TYPICAL TIME</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>16</td><td>488µs</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>48</td><td>1.46ms</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>96</td><td>2.93ms</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>128</td><td>3.9ms</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>168</td><td>5.13ms</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td colspan="2">4MHz Osc On Continuously</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td colspan="2">4MHz Osc On Continuously</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="2">4MHz Osc On Continuously</td></tr>
<tr><td rowspan="8">3:0</td><td rowspan="8">CAL_PERIOD[3:0]</td><td colspan="5">4MHz Ceramic Oscillator Calibration Period: These bits define the number of 32.768kHz oscillator periods to measure for determination of the 4MHz ceramic oscillator period.

32kHz Clock Cycles = 1+ CAL_PERIOD[3:0]</td></tr>
<tr><th rowspan="2" colspan="2">CAL_PERIOD[3:0] (decimal)</th><th colspan="3">DESCRIPTION</th></tr>
<tr><th colspan="2">32kHz CLOCK CYCLES (decimal)</th><th>TYPICAL TIME (µs)</th></tr>
<tr><td colspan="2">0</td><td colspan="2">1</td><td>30.5</td></tr>
<tr><td colspan="2">1</td><td colspan="2">2</td><td>61</td></tr>
<tr><td colspan="2">. . .</td><td colspan="2">. . .</td><td>. . .</td></tr>
<tr><td colspan="2">14</td><td colspan="2">15</td><td>457.7</td></tr>
<tr><td colspan="2">15</td><td colspan="2">16</td><td>488.0</td></tr>
</table>

Table 28. Real-Time Clock Register

REAL-TIME CLOCK REGISTER		
WRITE OPCODE **43h**	**READ OPCODE** **C3h**	**POR DEFAULT VALUE** **0000h**

Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	X	X

Bit	7	6	5	4	3	2	1	0
Name	X	32K_BP	32K_EN	EOSC	AM1	AM0	WF	WD_EN

BIT	NAME	DESCRIPTION
15:7	X	Reserved
6	32K_BP	**32kHz Bypass:** This bit, when set, allows an external CMOS-level 32.768kHz signal to be applied to the 32KX1 device pin. The internal 32.768kHz oscillator is bypassed and the external signal is driven into the device's core.
5	32K_EN	**32kHz Clock Output Enable:** This bit enables the 32KOUT device pin to drive a CMOS-level square wave representation of the 32kHz crystal.
4	EOSC	**Enable Oscillator:** This active-low bit when set to logic 0 starts the real time clock oscillator. When this bit is set to logic 1, the oscillator is stopped.
3:2	AM[1:0]	**Alarm Control:** The device contains a time-of-day alarm. The alarm is activated when either the AM1 or AM2 bits are set. When the RTC's hours or minutes value increments to a value equal to the alarm settings in Alarm registers, the AF bit in the Interrupt Status register is set and the $\overline{\text{INT}}$ device pin is asserted (if enabled) and remains asserted until the Interrupt Status register is accessed by the microprocessor with a Read register command.
1	WF	**Watchdog Flag**: This bit is set when the watchdog counter reaches zero. This bit must be written to a zero to clear the bit. Writing this bit to a zero when the $\overline{\text{WDO}}$ pin is asserted low releases the $\overline{\text{WDO}}$ pin to its inactive high-impedance state.
0	WD_EN	**Watchdog Enable:** 1 = Watchdog timer is enabled. 0 = Watchdog time is disabled and the $\overline{\text{WDO}}$ pin is high impedance.

AM1	AM0	ALARM FUNCTION
0	0	No alarm
0	1	Alarm when minutes match
1	0	Alarm when hours match
1	1	Alarm when hours and minutes match

Table 29. Interrupt Status Register

INTERRUPT STATUS REGISTER								
WRITE OPCODE READ ONLY		READ OPCODE FEh		POR DEFAULT VALUE 0000h				
Bit	15	14	13	12	11	10	9	8
Name	TO	AF	X	TOF	TE	LDO	TOF_EVTMG	TEMP_EVTMG
Bit	7	6	5	4	3	2	1	0
Name	X	Cal	Halt	CSWI	X	PORX	X	X
Note: This register is read only and bits are self-clearing upon a read to this register, see the *Interrupt Operations* section for more information.								

BIT	NAME	DESCRIPTION
15	TO	**TimeOut:** The TO bit is set if any one of the t_1, t_2, Hit1 thru Hit6, or temperature measurements do not occur causing the time set by the TIMOUT[2:0] bits in the TOF2 register to elapse.
14	AF	**Alarm Flag:** Set when the RTC's hours or minutes value increments to a value equal to the alarm settings in Alarm registers.
13	X	Reserved
12	TOF	**Time of Flight:** Set when the TOF_UP, TOF_DN, or TOF_DIFF command has completed. During execution of The EVTMG1 or EVTMG2 command, this bit is set and the $\overline{INT}$ pin is asserted (if enabled) upon completion of each of the cycles of the Event defined by the TOF Difference Measurements setting if the CONT_INT bit in the Calibration and Control register has been set.
11	TE	**Temperature:** Set when the Temperature command has completed. During execution of The EVTMG1 or EVTMG3 command, this bit is set and the $\overline{INT}$ pin is asserted (if enabled) upon completion of each of the cycles of the Event defined by the Temperature Measurements setting if the CONT_INT bit in the Calibration and Control register has been set.
10	LDO	**Internal LDO Stabilized:** Set when the internal low-dropout regulator is turned on by either the LDO_Timed or LDO_ON and has stabilized.
9	TOF_EVTMG	**Event Timing TOF Completed:** Set when either the EVTMG1 or EVTMG2 commands have completed its last TOF_DIFF measurement cycle. This indicates that the data in the T1, T2, T1_AVG, and T2_AVG registers is valid.
8	TEMP_EVTMG	**Event Timing Temperature Completed:** Set when the EVTMG1 or EVTMG3 commands have completed its last temperature measurements. This indicates that the data in the T1, T2, T3, T4, T1_AVG, T2AVG, T3AVG, and T4_AVG Results registers is valid.
7	X	Reserved
6	CAL	**Calibrate:** Set after completion of the Calibrate command when the command is manually sent by the host microprocessor. When Calibration occurs as a result of the setting of the Cal_Use, Cal_AUTO and Cal_CFGx bits in the Event Timing 2 register and the device is automatically executing Calibration commands as required during execution of any of the EVTMGx commands, this bit **is not** set.
5	HALT	**HALT:** Set when the HALT command has completed
4	CSWI	**Case Switch:** Set when a high logic level is detected on the CSW device pin.
3	X	Reserved
2	POR	**Power-On-Reset:** Set when the device has been successfully powered by application of V_{CC}. Upon application of power, the SPI port is inactive until this bit has been set.
1:0	X	Reserved

Table 30. Control Register

CONTROL REGISTER								
WRITE OPCODE **FFh**		**READ OPCODE** **7Fh**			**POR DEFAULT VALUE** **000xh**			
Bit	15	14	13	12	11	10	9	8
Name	X	X	X	X	X	X	AFA	CSWA
Bit	7	6	5	4	3	2	1	0
Name	X	X	X	X	HWR3	HWR2	HWR1	HWR0

BIT	NAME	DESCRIPTION
15:10	X	Reserved
9	AFA	**Alarm Flag Arm:** This bit is set when the RTC's hours and/or minutes value matched the alarm settings in the Real-Time Clock register. This bit is set at the same time as the AF bit in the Interrupt Status register. After resetting the RTC alarm settings, a 0 must be written to this bit to re-arm the RTC Alarm. This bit can only be written to a 0.
8	CSWA	**Case Switch Arm:** This bit is set when the CSW pin detects a logic-high, indicating the MAX35104 has detected a tamper condition. This bit is set at the same time as the CSWI bit in the Interrupt Status register. Once set, this bit must be written to a 0 to re-arm the Case Switch Detection. The Case Switch Detection must be re-armed before the CSWI interrupt can be set again. This bit can only be written to a 0.
7:0	X	Reserved
3:0	HWR[3:0]	**Hardware Revision:** These 4 bits contain hardware revision code specific to the MAX35104 device. **Note:** This value can be accessed and modified. Read this register directly after a POR to get the correct hardware revision number.

Conversion Results Register Descriptions

The devices conversion results registers are all read only volatile SRAM. The POR default value for all registers is 0000h.

Table 31. Conversion Results Registers Description

<table>
<tr><th>READ-ONLY ADDRESS</th><th>REGISTER</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td rowspan="7">C4h</td><td rowspan="7">WVRUP</td><td colspan="8">Bit 15 to Bit 8 holds the 8 bit value of the pulse width ratio ($t_1 \div t_2$).for the upstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>Bit15</td><td>Bit 14</td><td>Bit 13</td><td>Bit 12</td><td>Bit 11</td><td>Bit 10</td><td>Bit 9</td><td>Bit 8</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">Bit 7 to bit 0 holds the 8 bit value of the pulse width ratio ($t_2 \div t_{IDEAL}$) where t_{IDE}AL is equal to one-half the period of the Pulse Launch Frequency for the upstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">The maximum value of each of these ratios is 1.9921875.</td></tr>
<tr><td>C5h</td><td>Hit1UPInt</td><td colspan="8">15-bit fixed-point integer value of the first hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2^{15} - 1) x t_{4MHZ}.</td></tr>
<tr><td>C6h</td><td>Hit1UPFrac</td><td colspan="8">16-bit fractional value of the first hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or (2^{16} - 1)/ 2^{16} x t_{4MHZ}.</td></tr>
<tr><td>C7h</td><td>Hit2UPInt</td><td colspan="8">15-bit fixed-point integer value of the second hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2^{15} - 1) x t_{4MHZ}.</td></tr>
<tr><td>C8h</td><td>Hit2UPFrac</td><td colspan="8">16-bit fractional value of the second hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or (2^{16} - 1)/ 2^{16} x t_{4MHZ}.</td></tr>
<tr><td>C9h</td><td>Hit3UPInt</td><td colspan="8">15-bit fixed-point integer value of the third hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2^{15} - 1) x t_{4MHZ}.</td></tr>
<tr><td>CAh</td><td>Hit3UPFrac</td><td colspan="8">16-bit fractional value of the third hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or (2^{16} - 1)/ 2^{16} x t_{4MHZ}.</td></tr>
<tr><td>CBh</td><td>Hit4UPInt</td><td colspan="8">15-bit fixed-point integer value of the fourth hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2^{15} - 1) x t_{4MHZ}.</td></tr>
<tr><td>CCh</td><td>Hit4UPFrac</td><td colspan="8">16-bit fractional value of the fourth hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or (2^{16} - 1)/ 2^{16} x t_{4MHZ}.</td></tr>
<tr><td>CDh</td><td>Hit5UPInt</td><td colspan="8">15-bit fixed-point integer value of the fifth hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or (2^{15} - 1) x t_{4MHZ}.</td></tr>
</table>

Table 31. Conversion Results Registers Description (continued)

<table>
<tr><th>READ-ONLY ADDRESS</th><th>REGISTER</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td>CEh</td><td>Hit5UPFrac</td><td colspan="8">16-bit fractional value of the fifth hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
<tr><td>CFh</td><td>Hit6UPInt</td><td colspan="8">15-bit fixed-point integer value of the sixth hit in the upstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.</td></tr>
<tr><td>D0Fh</td><td>Hit6UPFrac</td><td colspan="8">16-bit fractional value of the sixth hit in the upstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
<tr><td>D1h</td><td>AVGUPInt</td><td colspan="8">15-bit fixed-point integer value of the average of the hits recorded in the upstream direction This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.</td></tr>
<tr><td>D2h</td><td>AVGUP Frac</td><td colspan="8">16-bit fractional value of the average of the hits recorded in the upstream direction. This fractional portion is a binary representation of one t4MHz period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
<tr><td rowspan="7">D3h</td><td rowspan="7">WVRDN</td><td colspan="8">Bit 15 thru Bit 8 holds the 8 bit value of the pulse width ratio ($t_1 \div$ t2).for the downstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>Bit15</td><td>Bit 14</td><td>Bit 13</td><td>Bit 12</td><td>Bit 11</td><td>Bit 10</td><td>Bit 9</td><td>Bit 8</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">Bit 7 to bit 0 holds the 8 bit value of the pulse width ratio ($t_2 \div t_{IDEAL}$) where t_{IDEAL} is equal to one-half the period of the Pulse Launch Frequency for the downstream measurement. Each bit is weighted as follows:</td></tr>
<tr><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>1</td><td>0.5</td><td>0.25</td><td>0.125</td><td>0.0625</td><td>0.03125</td><td>0.015625</td><td>0.0078125</td></tr>
<tr><td colspan="8">The maximum value of each of these ratios is 1.9921875.</td></tr>
<tr><td>D4h</td><td>Hit1DNInt</td><td colspan="8">15-bit fixed-point integer value of the first hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.</td></tr>
<tr><td>D5h</td><td>Hit1DNFrac</td><td colspan="8">16-bit fractional value of the first hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
<tr><td>D6h</td><td>Hit2DNInt</td><td colspan="8">15-bit fixed-point integer value of the second hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.</td></tr>
<tr><td>D7h</td><td>Hit2DNFrac</td><td colspan="8">16-bit fractional value of the second hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
<tr><td>D8h</td><td>Hit3DNInt</td><td colspan="8">15-bit fixed-point integer value of the third hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.</td></tr>
</table>

Table 31. Conversion Results Registers Description (continued)

READ-ONLY ADDRESS	REGISTER	DESCRIPTION
D9h	Hit3DNFrac	16-bit fractional value of the third hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16}$ x t_{4MHZ}.
DAh	Hit4DNInt	15-bit fixed-point integer value of the fourth hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHZ}.
DBh	Hit4DNFrac	16-bit fractional value of the fourth hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16}$ x t_{4MHZ}.
DCh	Hit5DNInt	15-bit fixed-point integer value of the fifth hit in the downstream direction. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHZ}.
DDh	Hit5DNFrac	16-bit fractional value of the fifth hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16}$ x t_{4MHZ}.
DEh	Hit6DNInt	15-bit fixed-point integer value of the sixth hit in the downstream direction This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHZ}.
DFh	Hit6DNFrac	16-bit fractional value of the sixth hit in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16}$ x t_{4MHZ}.
E0h	AVGDNInt	15-bit fixed-point integer value of the average of the hit times recorded in the downstream direction This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHZ}.
E1h	AVGDN Frac	16-bit fractional value of the average of the hit times recorded in the downstream direction. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16}$ x t_{4MHZ}.
E2h	TOF_ DIFFInt	16-bit fixed-point two's-complement integer portion of the difference of the averages for the hits recorded in both the upstream and downstream directions. It is computed as: AVGUP – AVGDN This integer represents the number of t_{4MHz} periods that contribute to computation. The maximum size of the integer is 7FFFh or $(2^{15} - 1)$ x t_{4MHZ}. The minimum size of this integer is 8000h or -2^{15} x t_{4MHz}.
E3h	TOF_ DIFFFrac	16-bit fractional portion of the two's complement difference of the averages for the hits recorded in both the upstream and downstream directions. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16}$ x t_{4MHZ}.

Table 31. Conversion Results Registers Description (continued)

<table>
<tr><th>READ-ONLY ADDRESS</th><th>REGISTER</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td rowspan="12">E4h</td><td rowspan="12">TOF_ Cycle_ Count/ TOF_ Range</td><td colspan="8">Bit 15 thru Bit 8 holds the 8 bit value of the TOF_Range. The TOF_Range is an 8-bit binary integer that indicates the range of valid error-free TOF_DIFF measurements that were made during execution of either of the EVTMG1 or EVTMG2 commands. The maximum value of TOF_Range is equal to 2 times the actual pulse launch period as configured by the Pulse Launch Divider bits in the TOF1 register.</td></tr>
<tr><td>Bit15</td><td>Bit 14</td><td>Bit 13</td><td>Bit 12</td><td>Bit 11</td><td>Bit 10</td><td>Bit 9</td><td>Bit 8</td></tr>
<tr><td>MSB</td><td colspan="6">TOF_Range 8-bit binary integer</td><td>LSB</td></tr>
<tr><td colspan="8">The formulas to calculate the Range and Resolution of the TOF_Range integer for a given DPL[3:0] bit setting are shown below:
Maximum Range (μs) = DPL[3:0] + 1 Resolution = Maximum Range / 256</td></tr>
<tr><td colspan="2">DPL[3:0]</td><td colspan="2">LAUNCH FREQUENCY</td><td colspan="2">MAXIMUM RANGE (μs)</td><td colspan="2">RESOLUTION (ns)</td></tr>
<tr><td colspan="2">0001b</td><td colspan="2">1 MHz</td><td colspan="2">2</td><td colspan="2">7.8175</td></tr>
<tr><td colspan="2">0002b</td><td colspan="2">666.6kHz</td><td colspan="2">3</td><td colspan="2">11.7185</td></tr>
<tr><td colspan="2">. . .</td><td colspan="2">. . .</td><td colspan="2">. . .</td><td colspan="2">. . .</td></tr>
<tr><td colspan="2">1110b</td><td colspan="2">133.3kHz</td><td colspan="2">15</td><td colspan="2">58.59375</td></tr>
<tr><td colspan="2">1111b</td><td colspan="2">125kHz</td><td colspan="2">16</td><td colspan="2">62.5</td></tr>
<tr><td colspan="8">Bit 7 to Bit 0 holds the 8-bit value of the TOF Cycle Count. The TOF Cycle Count is an 8-bit binary integer that indicates the number of valid error-free cycles that either of the EVTMG1 or EVTMG2 commands has executed. It also represents the number of TOF_DIFF cycles that have been totaled for the purpose of averaging, which affects the results provided in the TOF_DIFF_AVGFrac and TOF_DIFF_AVGInt registers. It is incremented every time an error-free TOF_DIFF command is executed by either the EVTMG1 or EVTMG2 sequence. Because of this internal error checking, once the complete number of cycles defined by the TOF Difference Measurements bits in the Event Timing 1 register has been completed and the TOF_EVTMG bit has been set in the Interrupt Status register causing the $\overline{\text{INT}}$ device pin to be asserted (if enabled), the TOF Cycle Count may not be equal to the setting of the TOF Difference Measurements bits in the Event Timing 1 register.</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td rowspan="2"></td><td rowspan="2"></td><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>MSB</td><td colspan="6">TOF Cycle Count 8-bit binary integer</td><td>LSB</td></tr>
<tr><td>E5h</td><td>TOF_DIFF_ AVGInt</td><td colspan="8">16-bit fixed-point two's-complement integer portion of the average of the accumulated TOF_DIFF measurements. It is computed as:

This integer represents the number of t_{4MHz} periods that contribute to the computation. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$. The minimum size of this integer is 8000h or $-2^{15} \times t_{4MHZ}$.</td></tr>
<tr><td>E6h</td><td>TOF_DIFF_ AVGFrac</td><td colspan="8">16-bit fractional portion of the two's complement average of the accumulated TOF_DIFF measurements. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
</table>

Table 31. Conversion Results Registers Description (continued)

<table>
<tr><th>READ-ONLY ADDRESS</th><th>REGISTER</th><th colspan="8">DESCRIPTION</th></tr>
<tr><td>E7h</td><td>T1Int</td><td colspan="8">15-bit fixed-point integer value of the time taken to discharge the timing capacitor through the temperature sensing element connected to the T1 device pin. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.</td></tr>
<tr><td>E8h</td><td>T1Frac</td><td colspan="8">16-bit fractional value of the time taken to charge the timing capacitor through the temperature sensing element connected to the T1 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
<tr><td>EBh</td><td>T2Int</td><td colspan="8">15-bit fixed-point integer value of the time taken to charge the timing capacitor through the temperature sensing element connected to the T2 device pin. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.</td></tr>
<tr><td>ECh</td><td>T2Frac</td><td colspan="8">16-bit fractional value of the time taken to charge the timing capacitor through the temperature sensing element connected to the T2 device pin. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
<tr><td rowspan="6">EFh</td><td rowspan="6">Temp_ Cycle_ Count</td><td colspan="8">The Temp Cycle Count is an 8-bit binary integer that indicates the number of valid error-free cycles that either of the EVTMG1 or EVTMG3 commands has executed. It also represents the number of Temperature cycles that have been totaled for the purpose of averaging, which affects the results provided in the Tx_AVGFrac and Tx_AVGInt registers. It is incremented every time an error-free Temperature command is executed by either the EVTMG1 or EVTMG3 sequence. Because of this internal error checking, once the complete number of cycles defined by the Temperature Measurements bits in the Event Timing 2 register has been completed and the Temp_EVTMG bit has been set in the Interrupt Status register causing the $\overline{INT}$ device pin to be asserted (if enabled), the Temp Cycle Count may not be equal to the setting of the Temperature Measurements bits in the Event Timing 2 register.</td></tr>
<tr><td>Bit15</td><td>Bit 14</td><td>Bit 13</td><td>Bit 12</td><td>Bit 11</td><td>Bit 10</td><td>Bit 9</td><td>Bit 8</td></tr>
<tr><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>Bit 7</td><td>Bit 6</td><td>Bit 5</td><td>Bit 4</td><td>Bit 3</td><td>Bit 2</td><td>Bit 1</td><td>Bit 0</td></tr>
<tr><td>MSB</td><td colspan="6">Temp Cycle Count</td><td>LSB</td></tr>
<tr><td>F0h</td><td>T1_AVGInt</td><td colspan="8">15-bit fixed-point integer value of the average of the T1 port measurements. It is computed as:

This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.</td></tr>
<tr><td>F1h</td><td>T1_AVG Frac</td><td colspan="8">16-bit fractional portion of the average of the T1 port measurements. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.</td></tr>
</table>

Table 31. Conversion Results Registers Description (continued)

READ-ONLY ADDRESS	REGISTER	DESCRIPTION
F4h	T2_AVGInt	15-bit fixed-point integer value of the average of the T2 port measurements. It is computed as: This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.
F5h	T2_AVG Frac	16-bit fractional portion of the average of the T2 port measurements. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.
F8h	Calibration Int	15-bit fixed-point integer value of the time taken to measure the period of the 32.768kHz crystal oscillator during execution of the Calibrate command. This integer portion is a binary representation of the number of t_{4MHz} periods that contribute to the time results. The maximum size of the integer is 7FFFh or $(2^{15} - 1) \times t_{4MHZ}$.
F9h	Calibration Frac	16-bit fractional value of the time taken to measure the period of the 32.768kHz crystal oscillator during execution of the Calibrate command. This fractional portion is a binary representation of one t_{4MHz} period quantized to a 16-bit resolution. The maximum size of the fraction is FFFFh or $(2^{16} - 1)/ 2^{16} \times t_{4MHZ}$.
FAh		Reserved
FBh		Reserved
FCh		Reserved
FDh		Reserved

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX35104ETL+	-40°C to +85°C	40 TQFN-EP*
MAX35104ETL+T	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
40 TQFN-EP	T4055+2	**21-0140**	**90-0016**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/16	Initial release	—
1	6/17	Corrected measurement range and clarified notes about measurement accuracy	1, 35
2	7/17	Updated ESD specification	2
3	12/17	Corrected register address for T2, removed references to T3 and T4	71, 77, 78

LifeElectronics
Живое партнерство

ООО «ЛайфЭлектроникс» "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru