DESCRIPTION

Demonstration circuit 1249 is a PoE to 3.3V@3.0A Isolated Converter featuring the LTC4267CDHC-3. The board provides a complete IEEE 802.3af power device (PD) interface and isolated 3.3V power supply solution for use in Power-over-Ethernet (PoE) applications in a very small printed circuit board footprint.

The LTC4267-3 integrates the 25kΩ signature resistor, classification current source, thermal overload protection, signature disable and power good signal along with an undervoltage lockout optimized for use with the IEEE required diode bridge. The precision dual level input current limit allows the LTC4267-3 to charge load capacitors and interface with legacy PoE systems.

The LTC4267-3 combines the above features with a current mode switching controller designed for driving a N-channel MOSFET. It features programmable slope compensation, soft-start, and constant frequency operation, minimizing electrical noise even with light loads.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Turn-on Voltage	Input from PSE	-37V
Maximum Turn-off Voltage	Input from PSE, PD switch turns off	-31V
Minimum operating voltage	I_{OUT} = 3A	-33V
Power Converter Input operating range	V_{OUT} = 3.3V, I_{OUT} = 0 to 3.0A	-37V to -57V
Maximum Input Current	Input from PSE, PD high level current limit	375mA, typical
Maximum Output Current	V_{OUT} = 3.3V	3.0A
Output Voltage	V_{IN} = 48VDC from PSE, I_{OUT} = 3.0A	3.3V, typical
Output Regulation	Line (0% to 100% full load)	2%
	Load (0% to 100% of rated full load)	2%

QUICK START PROCEDURE

Demonstration circuit 1249 is easy to set up to evaluate the performance of the LTC4267-3. For proper equipment setup, refer to figure 1 and follow the procedure below:

1. With the power source to the PSE turned off, connect the input power supply to the board through the J1 filtered Ethernet connector.
2. In addition to a PSE, the DC1249 board can be powered by an alternate input power supply

through the VPORTP (TP16) and VPORTN (TP15) terminals. Do not connect more than one power source.

3. Connect the SIGNATURE DISABLE signal to VPORTN.
4. Turn on the PSE or alternate input power supply and increase the voltage until the power converter turns on. Be careful not to exceed 57VDC. NOTE: Make sure that the input voltage does not exceed 57VDC. If a higher voltage is required, power components with higher voltage ratings should be used.
5. Verify proper classification and signature detection.
6. Check the output voltage. It should be 3.3V, typical. If there is no output, temporarily disconnect the load to make sure that the load is not too high.
7. Once the proper output voltage is established, adjust the load current within the appropriate range and observe the output regulation, ripple voltage, efficiency and other parameters.

OPERATION

Demonstration circuit 1249 interfaces with a customer's Power-over-Ethernet test setup per Figure 1. The front end of the demo circuit implements the required Ethernet input interface transformer coupling and common-mode termination through the integrated connector J1. The demonstration circuit is set up to allow data to pass in and back out of the demo circuit while the DC1249 performs IEEE 802.3af interface functions. The Power Sourcing Equipment (PSE) is connected to J1 and the PHY is optionally connected to J2.

The PD is required to have 0.1uF of capacitance during detection; this is provided by C2. It is also required to have at least 5uF of capacitance after the in-rush circuit, provided by capacitors C1 and C9.

This demo circuit allows detection and power classification of the PD per the IEEE 802.3af specification. During the detection process of a PD, the LTC4267-3 displays the proper 25kΩ signature resistor. Signature detection may be disabled, if so desired, by pulling the SIGNATURE DISABLE line (TP10) up to VPORTP. If signature classification is disabled, all interface functions of the LTC4267-3 are disabled. Signature detection, classification and the internal power MOSFET switch are all disabled.

Note that the SIGNATURE DISABLE signal at TP10 is an open circuit. While it is true that this signal is internally pulled down within the LTC4267-3, the data sheet explicitly states that this signal must be tied to VPORTN or VPORTP. This signal is left open only for the convenience of the user when operating the demonstration circuit. The SIGNATURE DISABLE signal must be properly terminated in a production application.

Classification is programmed by the selection of a single external resistor, R17, connected to the RCLASS pin.

After detection and classification, the PD is powered up when the input voltage exceeds the LTC4267-3 turn-on under-voltage lock out (UVLO) through a dual-level current-limited power switch. While the voltage between POUT and VPORTN is above the Power Good trip point, the amperage through the power switch is held below the low-

level current limit. When the voltage between POUT and VPORTN falls below the Power Good trip point, the Power Good signal goes active low and the amperage through the power switch is held below the high-level current limit.

For the PD to remain powered on, it must present to the PSE both AC and DC components of the Maintain Power Signature (MPS). The PD must hold the DC MPS by drawing at least 10mA or the PSE may disconnect power. The DC1249 demo board does implement a minimum load option with the JP2 jumper. By enabling this jumper the the circuit will draw approximately 16.5mA to satisfy the DC disconnect requirements.

The synchronous Flyback converter operates at a typical switching frequency of 300kHz, controlled by the current mode controller portion of the LT4267-3. Galvanic isolation is achieved through transformer T1 and opto-isolator U4.

The primary side power path is comprised of C1, L1, Cin1, ½ of T1, Q2, and RCS. These components should be as close to each other as possible when laying out the printed circuit board. The secondary side power path is made up of the other ½ of T1, D1, and Cox. These parts should also be laid out as close to each other as possible, without overlapping any of the circuitry or traces of the primary side.

IN ORDER TO ENSURE PROPER OPERATION, THE DESIGNER MUST ENSURE THAT THE PD INPUT CURRENT REQUIREMENT DOES NOT EXCEED THE LTC4267-3 CURRENT LIMIT OVER THE UNIT'S OPERATING VOLTAGE RANGE.

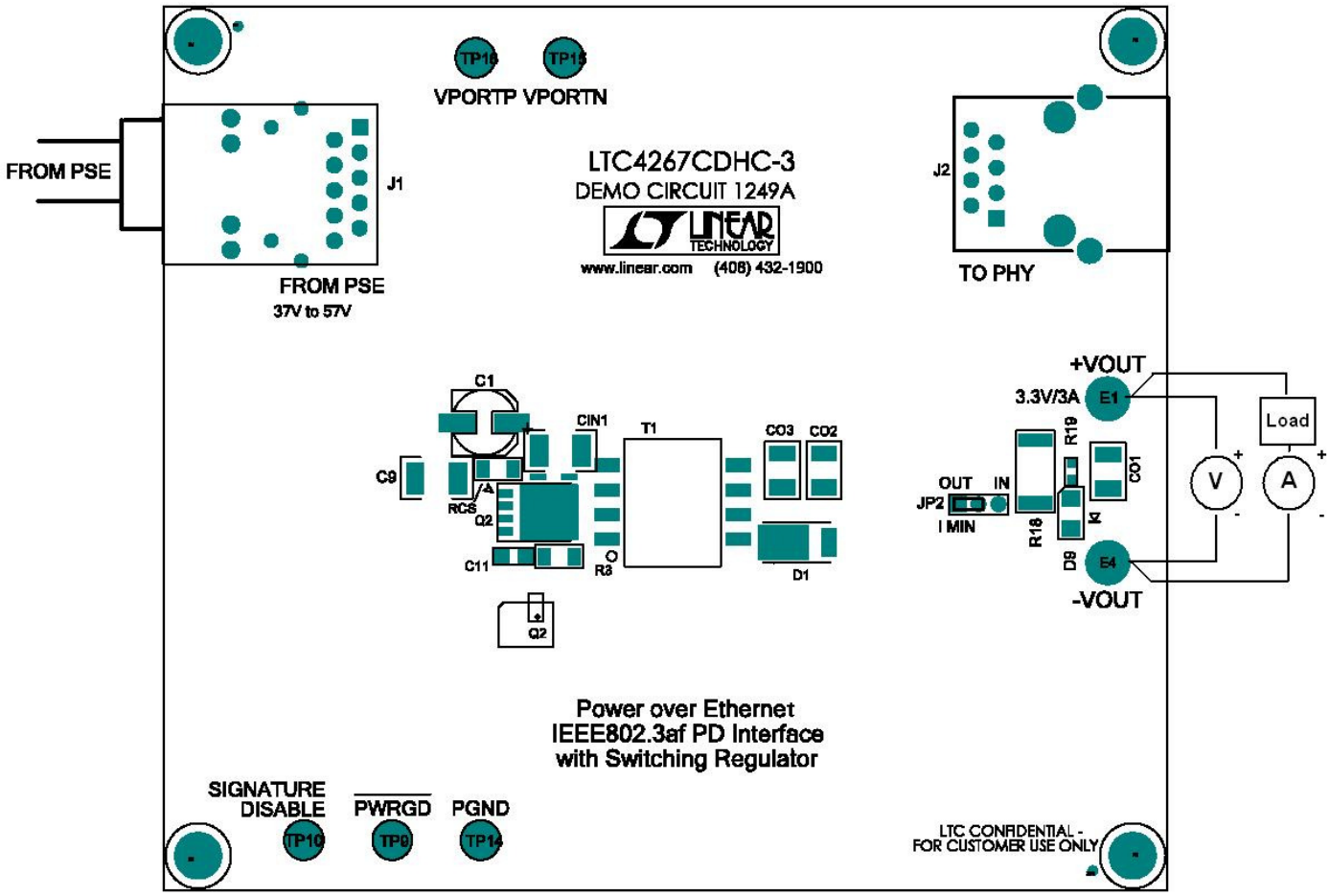
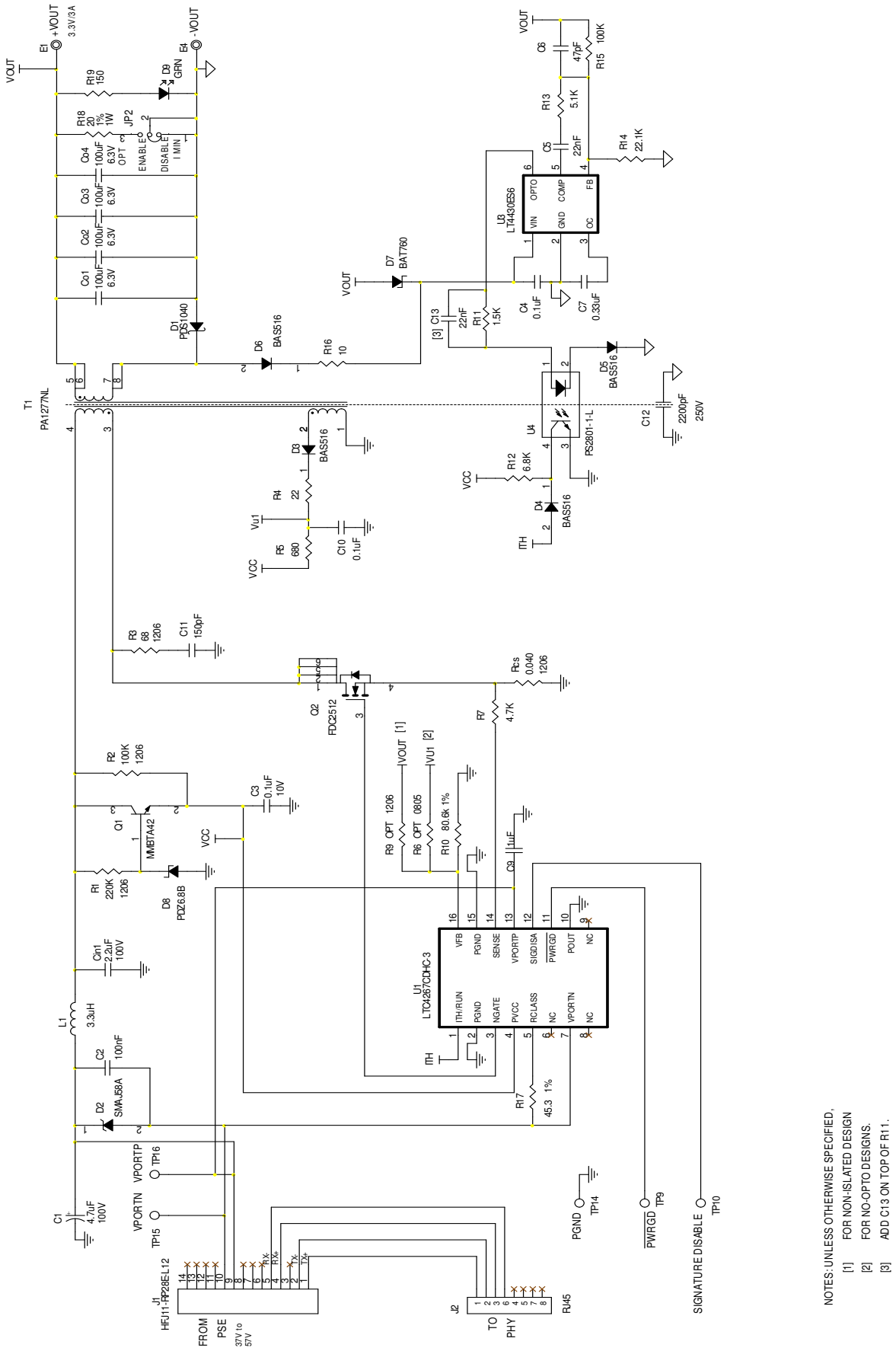


Figure 1. Proper Measurement Equipment Setup


E1 +VOUT 3.3V/3A
E4 -VOUT
VOUT
R19 150
D9 GRN
R18 20 1% 1W
JP2
ENABLE
DISABLE
I MIN
OPT
Co4 100uF 6.3V
Co3 100uF 6.3V
Co2 100uF 6.3V
Co1 100uF 6.3V
D1 PDS1040
D6 BAS516
R16 10
D7 BAT760
[3] C13 22nF
R11 1.5K
C4 0.1uF
C7 0.33uF
U3 LT4430ES6
VIN
OPTO
GND
COMP
OC
FB
C6 47pF
R15 100K
R13 5.1K
C5 22nF
R14 22.1K
D5 BAS516
C12 2200pF 250V
U4 PS2801-1-L
R12 6.8K
D4 BAS516
ITH
VCC
T1 PA1277NL
D3 BAS516
R4 22
Vu1
R5 680
C10 0.1uF
R3 68 1206
C11 150pF
Q2 FDC2512
Rcs 0.040 1206
R7 4.7K
R2 100K 1206
C3 0.1uF 10V
Q1 MMBTA42
R1 220K 1206
D8 PDZ6.8B
VOUT [1]
VU1 [2]
R9 OPT 1206
R6 OPT 0805
R10 80.6k 1%
C9 1uF
U1 LTC4267CDHC-3
VFB
PGND
SENSE
VPORTP
SIG/DISA
PWRGD
POUT
NC
ITH/RUN
PGND
NGATE
PVCC
RCLASS
NC
VPORTN
NC
Cin1 2.2uF 100V
L1 3.3uH
C2 100nF
D2 SMAJ58A
R17 45.3 1%
C1 4.7uF 100V
VPORTP TP16
VPORTN TP15
PGND TP14
PWRGD TP9
SIGNATURE DISABLE TP10
J1 HFJ11-RP28EL12
FROM PSE 37V to 57V
J2 RJ45
TO PHY
NOTES: UNLESS OTHERWISE SPECIFIED,
[1] FOR NON-ISLATED DESIGN
[2] FOR NO-OPTO DESIGNS.
[3] ADD C13 ON TOP OF R11.

ООО «ЛайфЭлектроникс» “LifeElectronics” LLC

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