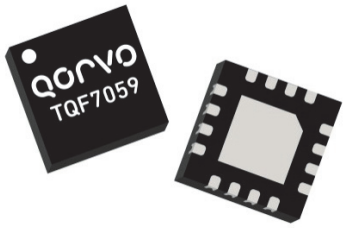
TQF7059

5 GHz WLAN Front End Module



16 Pad 3 x 3 x 0.85 mm QFN Package

General Description

The TQF7059 is a fully integrated WLAN front-end module (FEM) designed for 802.11ac applications. The TQF7059 contains a 5 GHz power amplifier, a power detector, a front-end SPDT switch, and an LNA with bypass mode. The architecture and interface are optimized to provide outstanding stable performance across temperature and voltage range for next generation, high throughput 802.11ac WLAN applications.

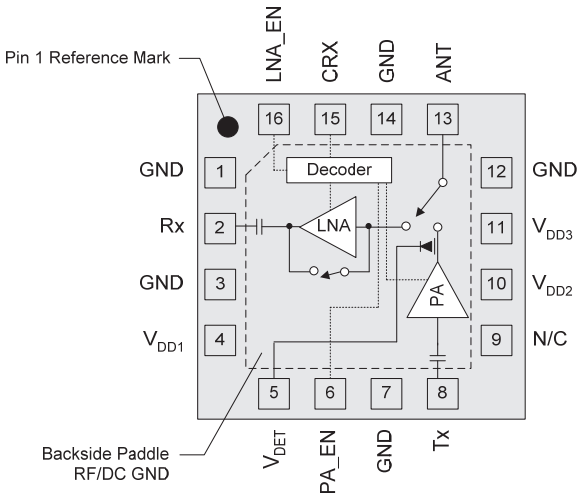
The TQF7059 FEM features CMOS compatible control voltages to facilitate ease of use. With its integrated compact design, the TQF7059 minimizes radio footprint and component count while achieving industry leading output power and EVM rivaling complex discrete high power designs.

The TQF7059 is assembled in a Pb-Free, thin profile, 16 pad, 3 mm x 3 mm x 0.85 mm QFN package.

Product Features

- Fully Integrated, 802.11a / n / ac Front-end Module
- Internally Matched Input / Output
- Integrated Power Detector
- Temperature Compensated Bias Network
- Typ. Pout=+21.5 dBm at EVM=1.8% (−35 dB) 802.11ac / MCS9 / VHT80 (+5 V)
- Typ. Pout=+23 dBm at EVM=3.0 % (−30 dB) 802.11n / MCS7 / HT40 (+5 V)
- Supply Voltage +3.3 V to +5 V
- Leadless 3 x 3 x 0.85 mm QFN Package
- Lead Free, RoHS Compliant

Functional Block Diagram



Applications

- 802.11a / n / ac Wireless LAN Systems
- CPE (Set Top Box, routers, gateways)
- WiFi Access Points and Small Cells
- Telematics
- Gaming and Infotainment
- ISM applications 5 – 6 GHz

Ordering Information

Part No.	Description
TQF7059	2500 Pieces on a 7” reel (standard)
TQF7059-PCB	Assembled Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−40 to +150 °C
RF Input Power, CW, 50Ω, T=25 °C	+5 dBm
Case Temperature Survival	−40 to +100 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{DD1}, V_{DD2}, V_{DD3}	+3.15	+5.0	+5.25	V
T_{AMB}	−30	25	+85	°C
Tj (for > 10^6 hours MTTF)			170	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications − Overall Module

Parameter	Conditions (1)	Min	Typ	Max	Units
Quiescent Current	Pout = −10 dBm, 11ac, MCS9, HT80		180		mA
Operating Current	Pout = +20.5 dBm, 11ac, MCS9, HT80		300		mA
PA Enable Control Voltage, V_{IH}	Input Voltage for High State	+1.8	+3.0	V_{DD1}	V
PA Enable Control Voltage, V_{IL}	Input Voltage for Low State		0	+0.45	V
Control Current, I_{IH}				100	µA
TX Shutdown Current			8		µA
TX Turn on/off time	10 – 90%		<0.4		µs
TX Rise/Fall time	10 – 90%		<0.4		µs
Thermal Resistance, θ_{jc}	Junction to backside paddle		27		°C/W

Notes:
1. Test conditions unless otherwise noted: V_{DD1}, V_{DD2}, V_{DD3} =+5.0 V, Temp=+25°C.

Logic Truth Table

5 GHz FEM	PA_EN	LNA_EN	CRX
Shutdown	0	0	0
Rx - Bypass Mode	0	0	1
RX- Normal Mode	0	1	1
TX Mode	1	0	0

Electrical Specifications – Transmit (Tx)

Parameter	Conditions	Min	Typ	Max	Units
Operational Freq. Range		4900		5925	MHz
TX Gain	Small Signal		31		dB
	Pout =+21dBm		31		dB
Small Signal TX Gain Out of Band	1600 – 1960 MHz		−35		dB
	3200 – 3900 MHz		2		
	7000 MHz		20		
PA Noise Figure	Noise Figure		4		dB
TX Harmonics (2fo)	Pout = +25 dBm, 11a, 6 Mbps, 20 MHz		−33		dBm/MHz
TX Harmonics (3fo)	Pout = +25 dBm, 11a, 6 Mbps, 20 MHz		−37		dBm/MHz
ANT-RX Isolation	When TX is ON		45		dB
Spectral Emission Mask Margin Relative to 11ac standard 11ac, MCS0, HT20	Pout = +25 dBm		3.6		dB
DEVM (11n/MCS7/HT40)	Pout = +23 dBm, 5150 – 5850 MHz		−30		dB
DEVM (11ac/MCS9/VHT80)	Pout = +16 dBm, 5150 – 5850 MHz		−37		dB
DEVM (11ac/MCS9/VHT80)	Pout = +20.5 dBm, 5150 – 5850 MHz		−36		dB
Quiescent Current	No RF		180		mA
Operating Current	Pout = +20.5 dBm,11ac, MCS9, VHT80		300		mA
Detector Voltage	No RF		0.35		V
	Pout = +25 dBm		1.0		

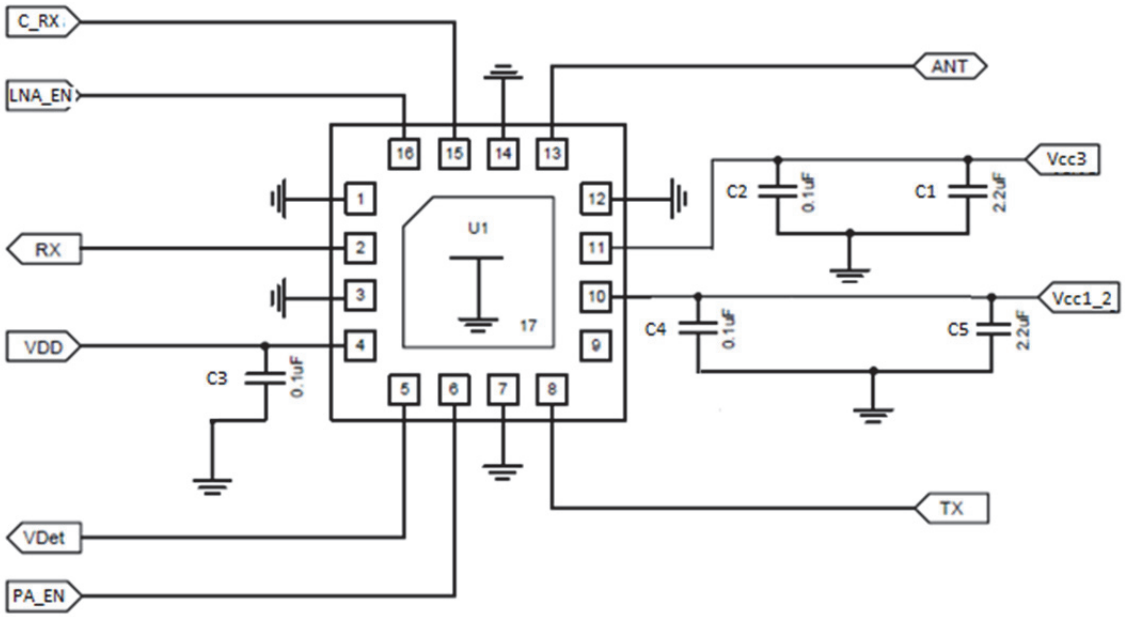
Notes:
1. Test conditions unless otherwise noted: V_{DD1}, V_{DD2}, V_{DD3}=+5.0 V, Temp.=+25 °C, −45 dB EVM source, TQF7059-PCB

Electrical Specifications – Receive (Rx)

Parameter	Conditions	Min	Typ	Max	Units
Operating Frequency		4900		5925	MHz
RX Gain – Normal Mode	ANT to RX out		13		dB
RX Gain – Bypass Mode	ANT to RX out		−7		dB
RX Flatness	Over entire, ANT to RX out	−1		1	
RX Noise Figure	Normal mode, ANT to RX out		2.1		dB
LNA Current			9		mA
IIP3 – Normal Mode	At ANT port through LNA		+4.0		dBm
IIP3 – Bypass Mode	At ANT port through LNA		+23		dBm
RX Output Return Loss	RX output in RX mode		10		dB
RX ANT Port Return Loss	ANT port in RX mode		7		dB
RX Output Return Loss	RX output in Bypass mode		12		dB
RX ANT Port Return Loss	ANT port in Bypass mode		7		dB

Notes:
1. Test conditions unless otherwise noted: V_{DD1}, V_{DD2}, V_{DD3} =+5.0 V, Temp.=+25 °C, TQF7059-PCB

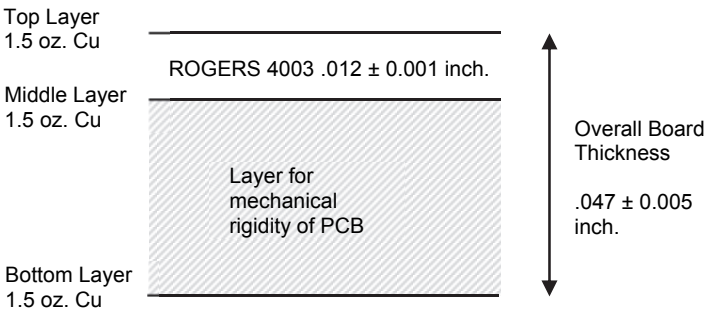
Application Circuit - TQF7059-PCB

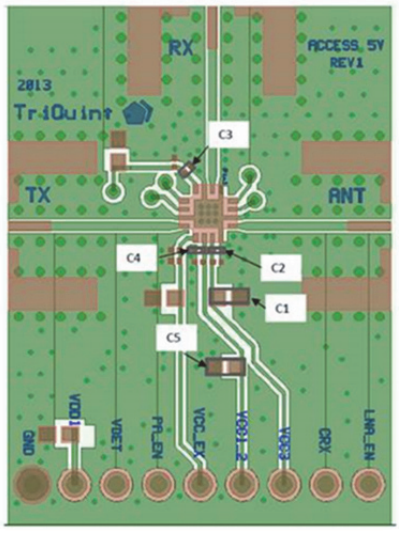


Bill of Material - TQF7059-PCB

Ref Des	Value	Description	Manuf.	Part Number
n/a	n/a	Printed Circuit Board		
U1	n/a	High Power WLAN 5GHz FEM	Qorvo	TQF7059
C1, C5	2.2 uF	Capacitor, Chip, 0402, 5%	various	
C2, C3, C4	0.1 uF	Capacitor, Chip, 0201, 5%	various	

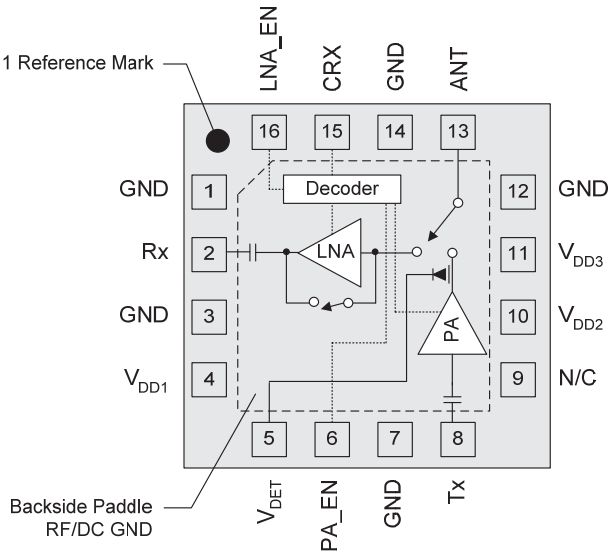
Evaluation Board PCB Information





Pin Configuration and Description

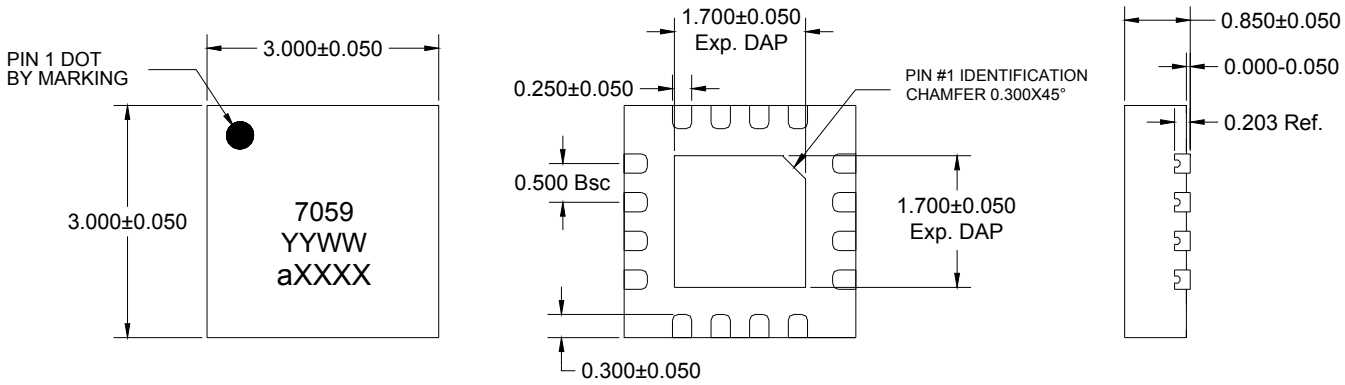
Top View



Pad No.	Label	Description
1	GND	Ground
2	Rx	Rx output, DC blocked RF I/O
3	GND	No internal connection. Recommended grounding this pin.
4	V_{DD1}	Supply pin for LNA, Logic & Bias circuits.
5	V_{DET}	Detector output voltage for 5 GHz PA
6	PA_EN	PA Enable
7	GND	No internal connection. Recommended grounding this pin.
8	Tx	5 GHz Tx PA input, DC blocked RF I/O
9	NC	No internal connection. Recommended grounding this pin.
10	V_{DD2}	Supply pin for PA 1st and 2nd stage.
11	V_{DD3}	Supply pin for PA final stage.
12	GND	No internal connection. Recommended grounding this pin.
13	ANT	Antenna pin, DC blocked RF I/O
14	GND	No internal connection. Recommended grounding this pin.
15	CRX	Control pin. Refer to logic truth table on pg. 2
16	LNA_EN	LNA Enable
Backside Pad	RF/DC GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

Package Marking and Dimensions

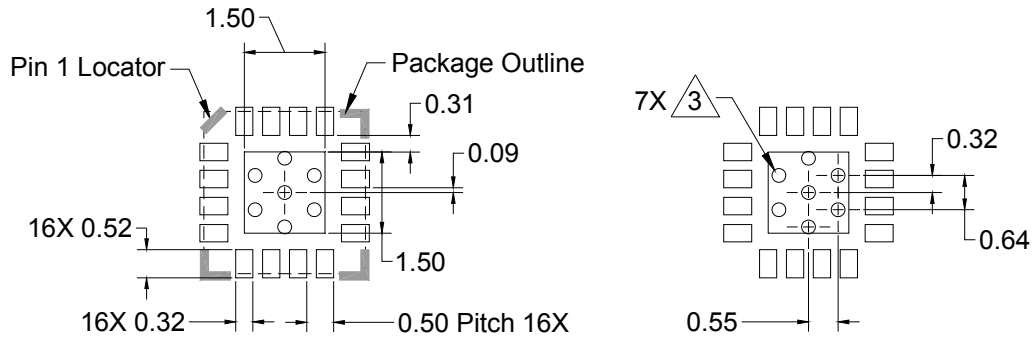
Marking: Product Identifier –"7059"
Date Code – YYWW
Lot Code – aXXXX



Top View | Bottom View | Side View

Notes:
1. All dimensions are in millimeters. Angles are in degrees.

PCB Mounting Pattern



COMPONENT SIDE

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.10").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 1	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com
Tel: 1-844-890-8163
Email: customer.support@qorvo.com

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Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru