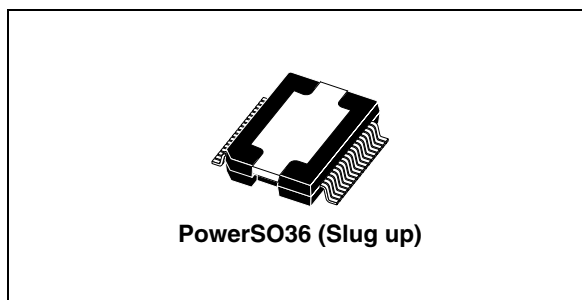


## 2 x 35 W power amplifier for car radio

### Features

- High output power capability:
  - 2 x 40 W max./4  $\Omega$
  - 2 x 35 W/4  $\Omega$  EIAJ
  - 2 x 25 W/4  $\Omega$  @14.4 V, 1 kHz, 10 %
  - 2 x 25 W/2  $\Omega$  @14.4 V, 1 kHz, 10 %
- 2  $\Omega$  driving
- Differential inputs
- Minimum external components count
- Internally fixed gain (26 dB)
- Mute function (CMOS compatible)
- Automute at minimum supply voltage detection
- Standby function
- No audible pop during mute and standby operations
- Clipping detector with programmable distortion threshold
- Protections:
  - Short circuit (out to ground, out to supply voltage, across the load)
  - Overrating chip temperature with soft thermal limiter
  - Load dump voltage
  - Fortuitous open ground
  - Loudspeaker DC current
  - ESD



### Description

The TDA7376PD is a new technology dual bridge audio amplifier in PowerSO36 package designed for car radio applications.

Thanks to the fully complementary PNP/NPN output stage configuration the TDA7376PD delivers a rail-to-rail voltage swing with no need of bootstrap capacitors.

Differential input pairs, that will accept either single ended or differential input signals, guarantee high noise immunity making the device suitable for both car radio and car boosters applications.

The audio mute control, that attenuates the output signal of the audio amplifiers, suppresses pop on - off transients and cuts any noises coming from previous stages. The standby control, that de-biases the amplifiers, reduces the cost of the power switch. The on-board programmable distortion detector allows compression facility whenever the amplifier is overdriven, so limiting the distortion at any levels inside the presettable range.

**Table 1. Device summary**

| Order code  | Package   | Packing       |
|-------------|-----------|---------------|
| TDA7376PD   | PowerSO36 | Tube          |
| TDA7376PDTR | PowerSO36 | Tape and reel |

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# 1 Block and pins connection diagrams

Figure 1. Block diagram

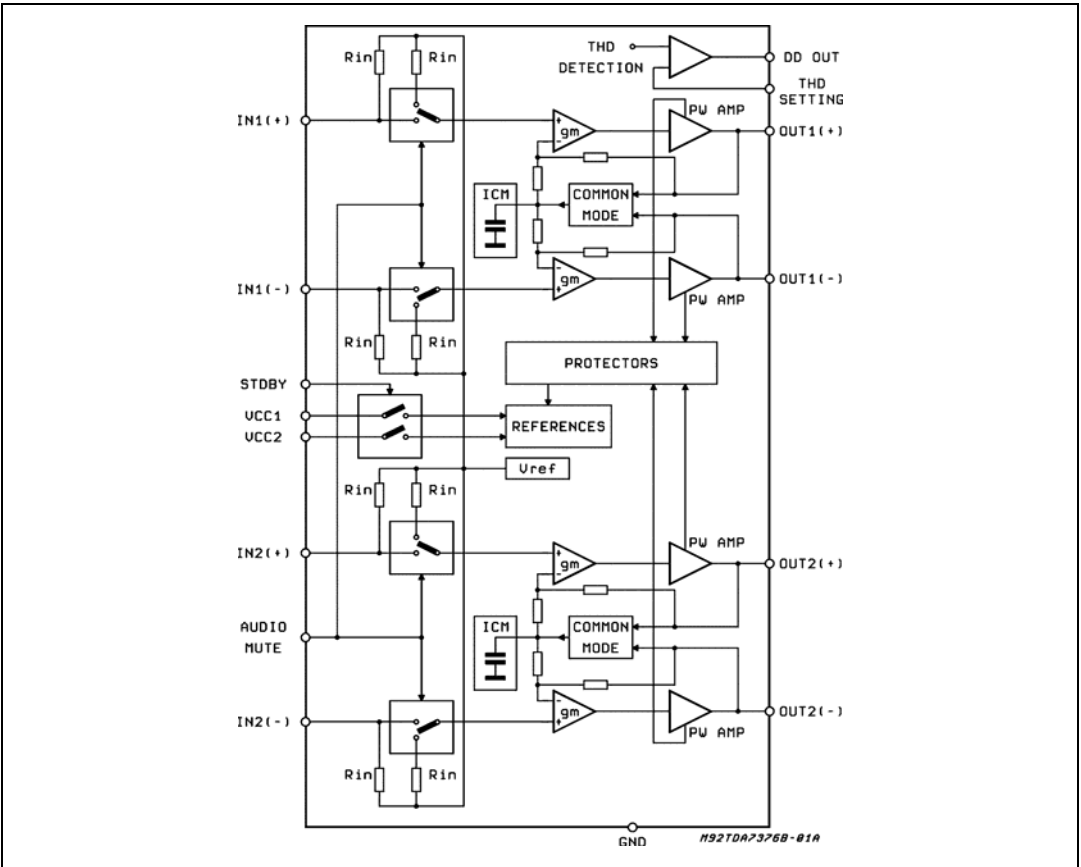
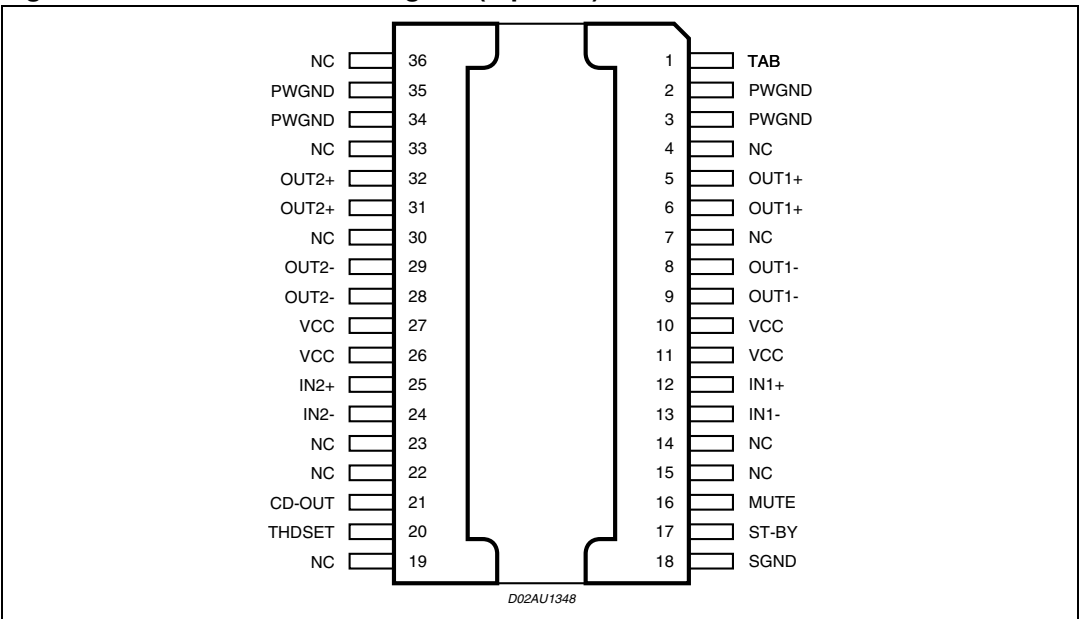


Figure 2. Pins connection diagram (top view)



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol         | Parameter                                              | Value      | Unit             |
|----------------|--------------------------------------------------------|------------|------------------|
| $V_{OP}$       | Operating supply voltage                               | 18         | V                |
| $V_S$          | DC supply voltage                                      | 28         | V                |
| $V_{peak}$     | Peak supply voltage ( $t = 50$ ms)                     | 50         | V                |
| $I_O$          | Output peak current (not repetitive $t = 100$ $\mu$ s) | 8          | A                |
|                | Output peak current (repetitive $f > 10$ Hz)           | 6          | A                |
| $P_{tot}$      | Power dissipation $T_{case} = 85^\circ\text{C}$        | 36         | W                |
| $T_{stg}, T_j$ | Storage and junction temperature                       | -40 to 150 | $^\circ\text{C}$ |

### 2.2 Thermal data

**Table 3. Thermal data**

| Symbol           | Parameter                               | Value | Unit               |
|------------------|-----------------------------------------|-------|--------------------|
| $R_{th\ j-case}$ | Thermal resistance junction-to-case Max | 2     | $^\circ\text{C/W}$ |

### 2.3 Electrical characteristics

Refer to the test circuits [Figure 15](#) and [16](#),  $V_S = 14.4$  V;  $R_L = 4$   $\Omega$ ;  $f = 1$  kHz;  $T_{amb} = 25$   $^\circ\text{C}$ , unless otherwise specified.

**Table 4. Electrical characteristics**

| Symbol        | Parameter                        | Test condition                             | Min. | Typ.         | Max. | Unit |
|---------------|----------------------------------|--------------------------------------------|------|--------------|------|------|
| $V_S$         | Supply voltage range             | -                                          | 8    | -            | 18   | V    |
| $I_d$         | Total quiescent drain current    | $R_L = \infty$                             | -    | -            | 200  | mA   |
| $V_{OS}$      | Output offset voltage            | -                                          | -    | -            | 120  | mV   |
| $P_O$         | Output power                     | THD = 10 %;                                | 23   | 25           | -    | W    |
|               |                                  | THD = 10 %; $R_L = 2$ $\Omega$             | 33   | 37           |      |      |
| $P_{O\ max}$  | Max. output power <sup>(1)</sup> | -                                          | 36   | 40           | -    | W    |
| $P_{O\ EIAJ}$ | EIAJ output power <sup>(1)</sup> | $V_S = 13.7$ V                             | 32   | 35           | -    | W    |
| THD           | Distortion                       | $P_O = 0.5$ to 10 W<br>$P_O = 0.5$ to 15 W | -    | 0.03<br>0.08 | -    | %    |
| $C_T$         | Cross talk                       | $f = 1$ kHz; $R_g$<br>$f = 10$ kHz; $R_g$  | -    | 80<br>70     | -    | dB   |

Table 4. Electrical characteristics (continued)

| Symbol               | Parameter                                 | Test condition                                                                                                            | Min. | Typ.   | Max. | Unit      |
|----------------------|-------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|------|--------|------|-----------|
| $R_{IN}$             | Input impedance                           | differential input                                                                                                        | 45   | -      | -    | $k\Omega$ |
|                      |                                           | Single Ended input                                                                                                        | 40   | -      | -    |           |
| $G_V$                | Voltage gain                              | differential input                                                                                                        | 25   | 26     | 27   | dB        |
|                      |                                           | Single Ended input                                                                                                        | 25   | 26     | 27   | dB        |
| $\Delta G_V$         | Channel gain balance                      | -                                                                                                                         | -    | -      | 1    | dB        |
| $E_{IN}$             | Input noise voltage                       | $R_g = 600 \Omega$ ; "A" weighted<br>$R_g = 600 \Omega$ ; 22 Hz to 33 kHz                                                 | -    | 3<br>4 | 6    | $\mu V$   |
| SVR                  | Supply voltage rejection                  | $f = 100 \text{ Hz}$ ; $V_r = 1 \text{ Vrms}$ ; $R_g = 0$ ;<br>$f = 10 \text{ Hz}$ ; $V_r = 1 \text{ Vrms}$ ; $R_g = 0$ ; | 45   | 55     | -    | dB        |
| BW                   | Power bandwidth                           | (-3dB)                                                                                                                    | 75   | -      | -    | kHz       |
| CMRR                 | Common mode rejection ratio               | $V_{CM} = 1 \text{ Vrms}$ input referred                                                                                  | 60   | -      | -    | dB        |
| $A_{SB}$             | Standby attenuation                       | $V_{SB} = 1.5V$ ; $P_{O \text{ ref}} = 1 \text{ W}$                                                                       | 80   | 90     |      | dB        |
| $V_{SB \text{ IN}}$  | Standby input threshold                   | -                                                                                                                         | -    | -      | 1.5  | V         |
| $V_{SB \text{ OUT}}$ | Standby output threshold                  | -                                                                                                                         | 3.5  | -      | -    | V         |
| $I_{sb}$             | Standby current consumption               | $V_{SB} = 0V$                                                                                                             | -    | -      | 20   | $\mu A$   |
| $A_M$                | Mute attenuation                          | $V_M = 1.5 \text{ V}$ ; $P_{O \text{ ref}} = 1 \text{ W}$                                                                 | -    | 85     | -    | dB        |
| $V_{M \text{ IN}}$   | Mute in threshold                         | -                                                                                                                         | -    | -      | 1.5  | V         |
| $V_{M \text{ OUT}}$  | Mute out threshold                        | -                                                                                                                         | 3.5  | -      | -    | V         |
| $I_6$                | Mute pin current                          | $V_6 = 0$ to $V_{S,}$ ; $V_{S \text{ max.}} = 18 \text{ V}$                                                               | -    | -      | 100  | $\mu A$   |
| $D_{DL}$             | Distortion detection level <sup>(2)</sup> | -                                                                                                                         | 3.5  | -      | -    | %         |
| $D_{DOUT}$           | Distortion detector output DC current     | Output low, sinked current<br>( $V_{pin10} = 1.5 \text{ V}$ )                                                             | 1    | -      | -    | mA        |
|                      |                                           | Output high, leakage current<br>( $V_{pin10} = V_S$ , @ $V_{S \text{ max}} = 18 \text{ V}$ )                              | -    | -      | 10   | $\mu A$   |

1. Saturated square wave output

2. See [Figure 3](#) for THD setting.

The TDA7376PD is equipped with a programmable clipping distortion detector circuitry that allows to signal out the output stage saturation by providing a current sinking into an open collector output ( $D_{DOUT}$ ) when the total harmonic distortion of the output signal reaches the preset level. The desired threshold is fixed through an external divider that produces a proper voltage level across the THD set pin. [Figure 3](#) shows the THD detection threshold versus the THD set voltage. Since it is essential that the THD set voltage be proportional to the supply voltage, [Figure 4](#) shows its value as a fraction of  $V_{CC}$ . The actual voltage can be computed by multiplying the fraction corresponding to the desired THD threshold by the application's supply voltage.

2.4 Electrical characteristics curves

Figure 3. Clip detector threshold vs. THD set. Figure 4. Quiescent current vs. supply voltage

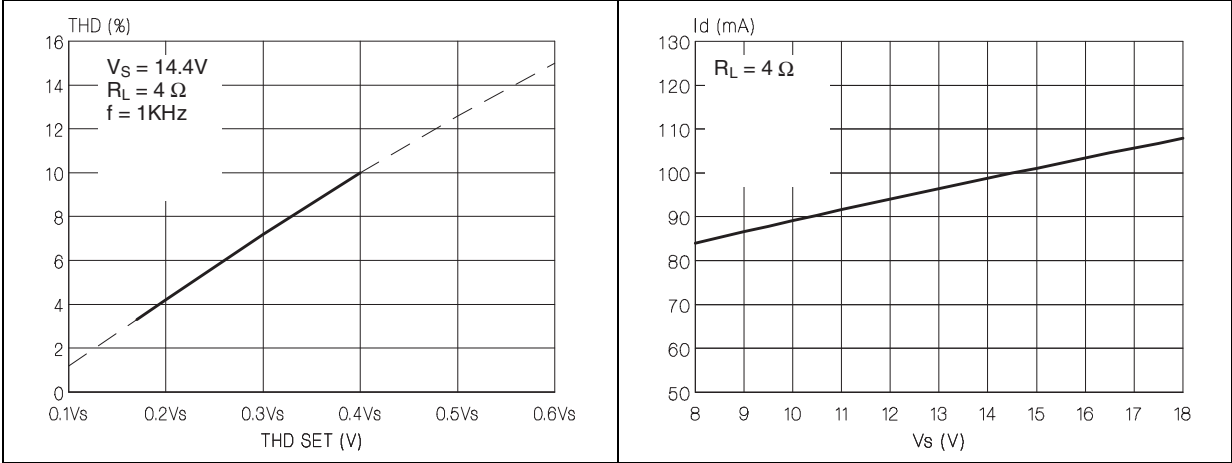


Figure 5. Output power vs. supply voltage (THD = 1 %) Figure 6. Output power vs. supply voltage (THD = 10 %)

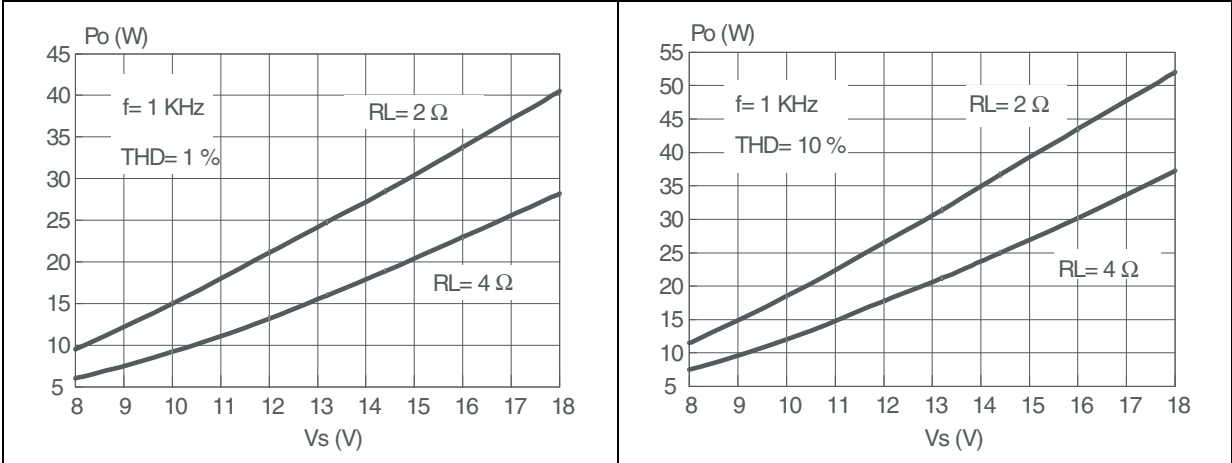


Figure 7. EIAJ power vs. supply voltage Figure 8. THD vs. frequency

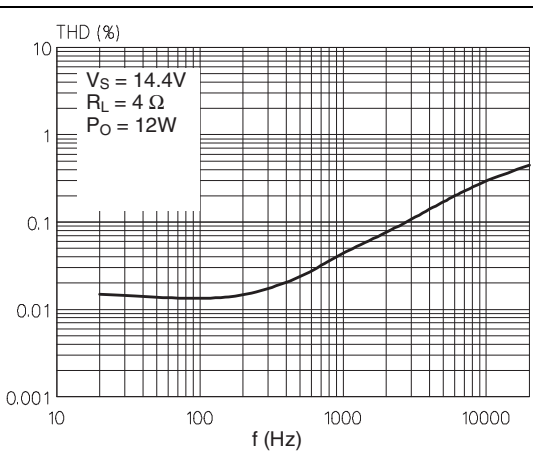
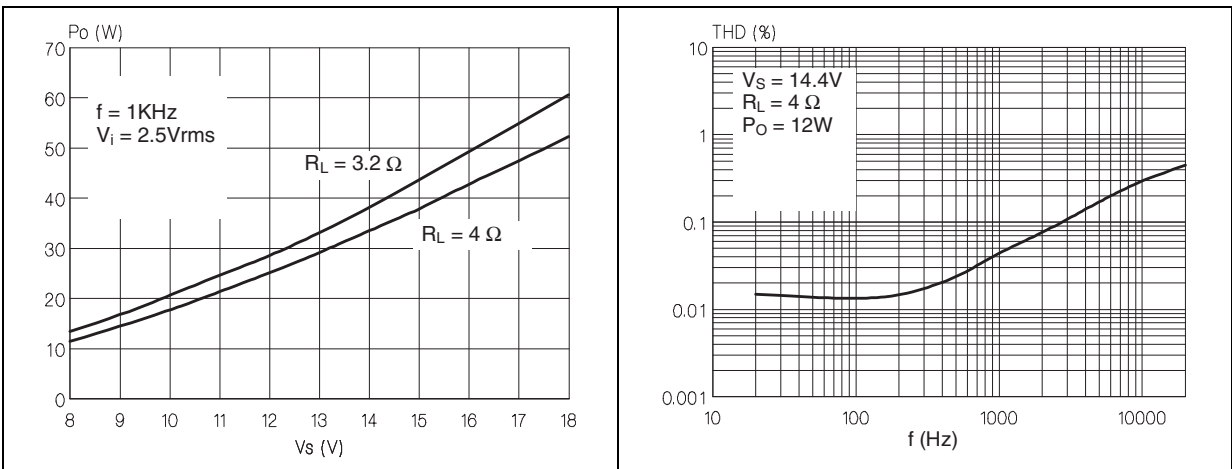




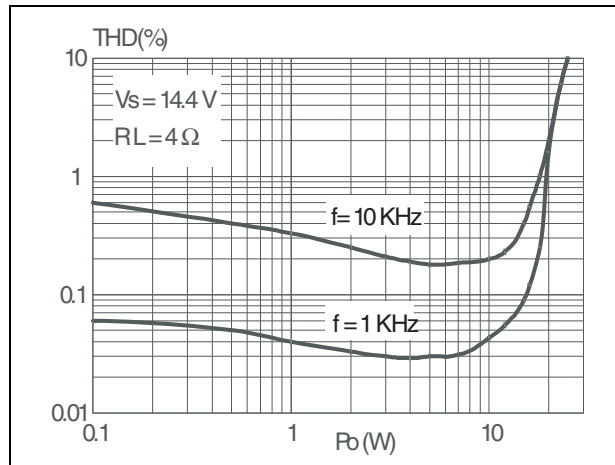
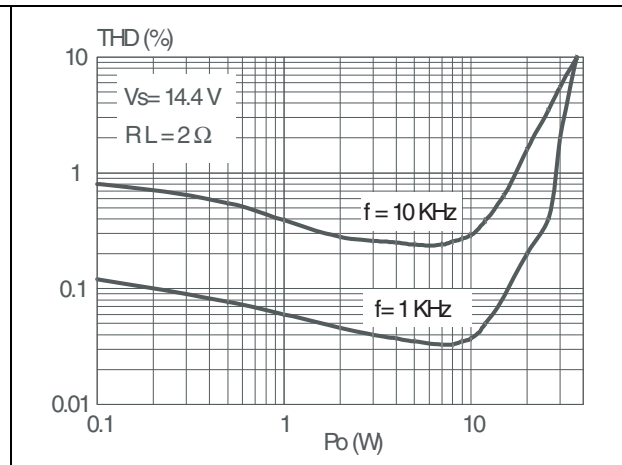
Figure 9. THD vs. output power ( $R_L = 4 \Omega$ )Figure 10. THD vs. output power ( $R_L = 24 \Omega$ )

Figure 11. Dissipated power and efficiency vs. output power

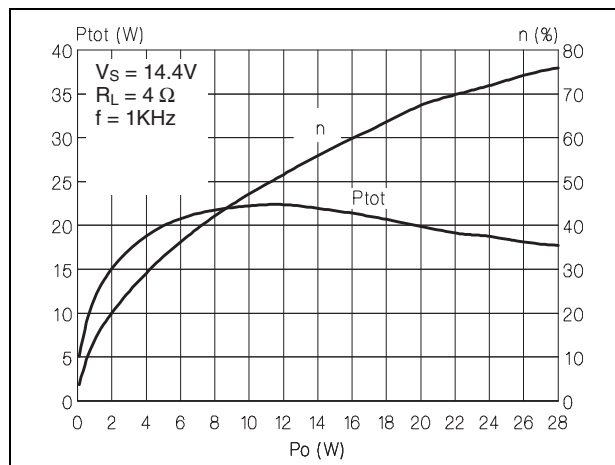


Figure 12. SVR vs. frequency

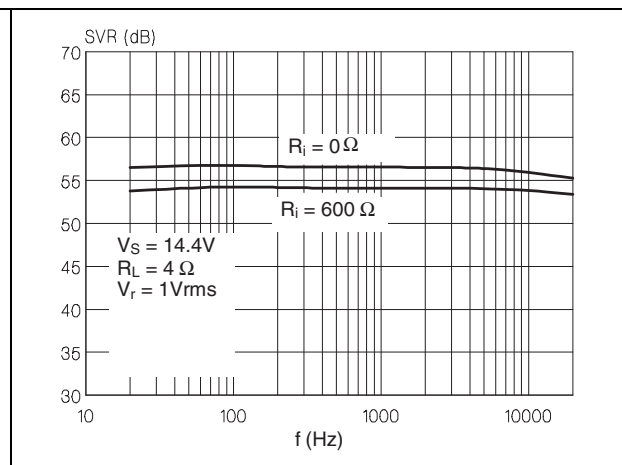


Figure 13. CMRR vs. frequency

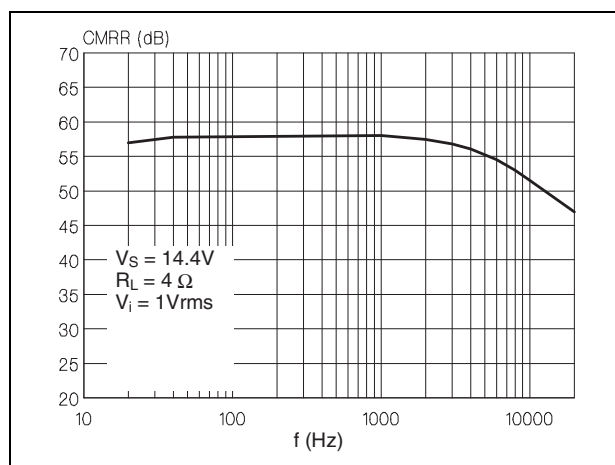
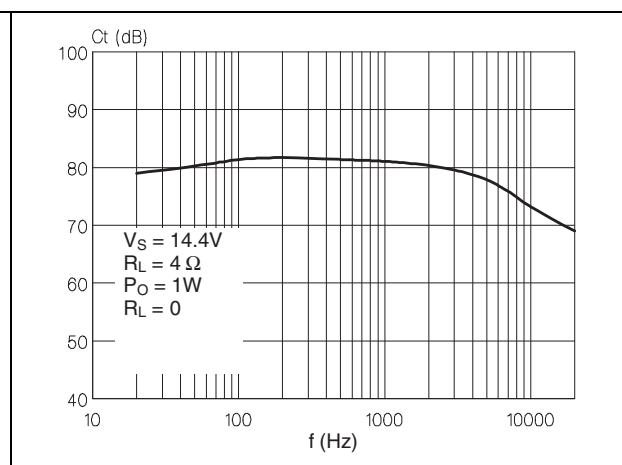


Figure 14. Crosstalk vs. frequency



## 2.5 Test and application circuits

Figure 15. Differential inputs test and application circuit

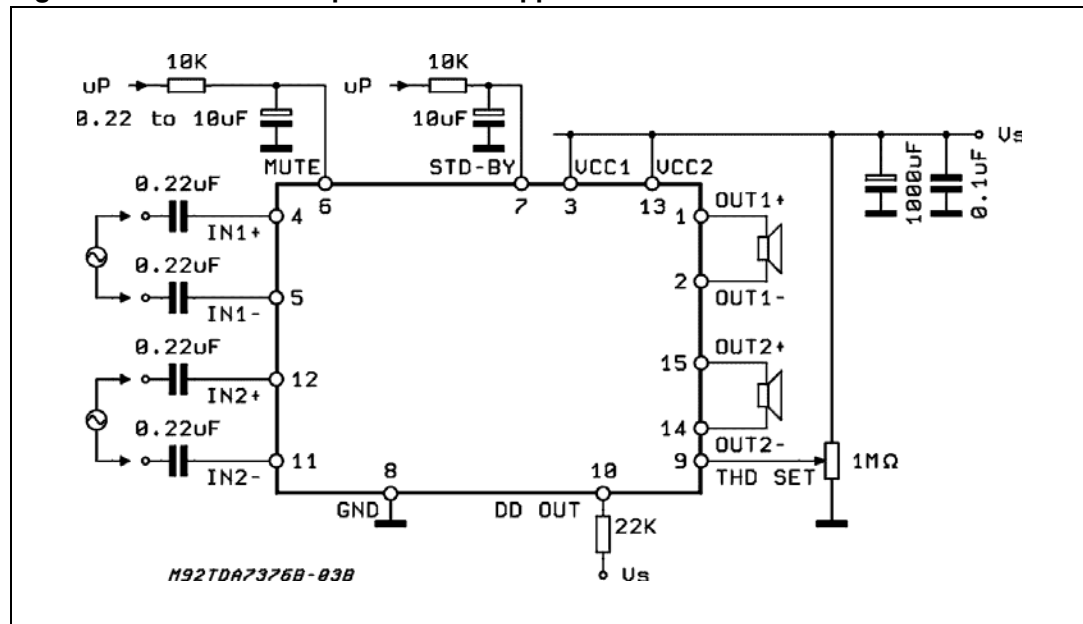


Figure 16. Single ended inputs test and application circuit

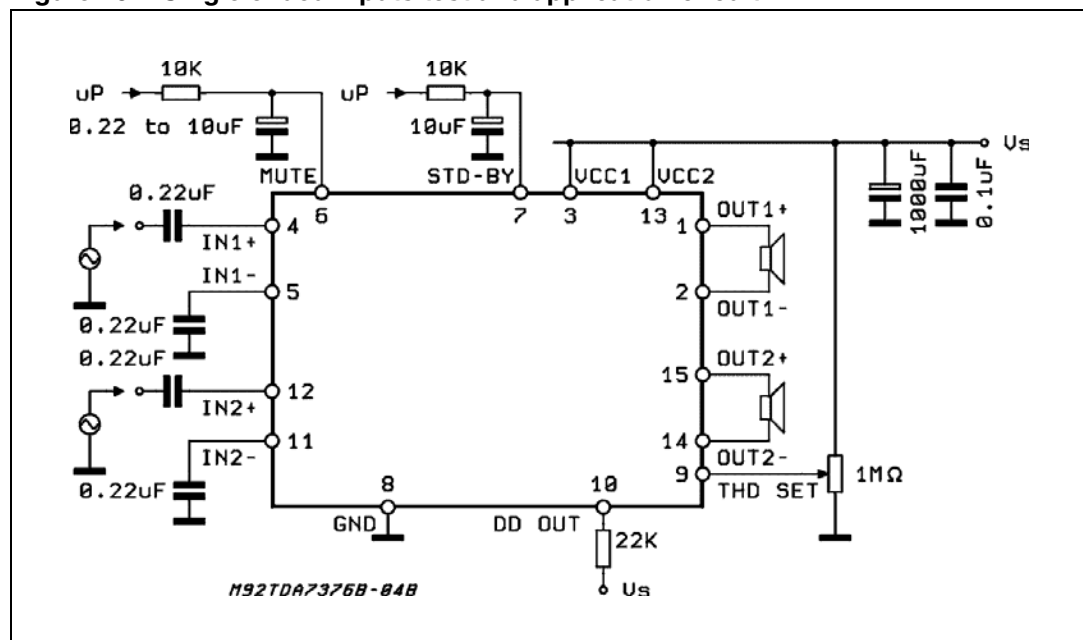
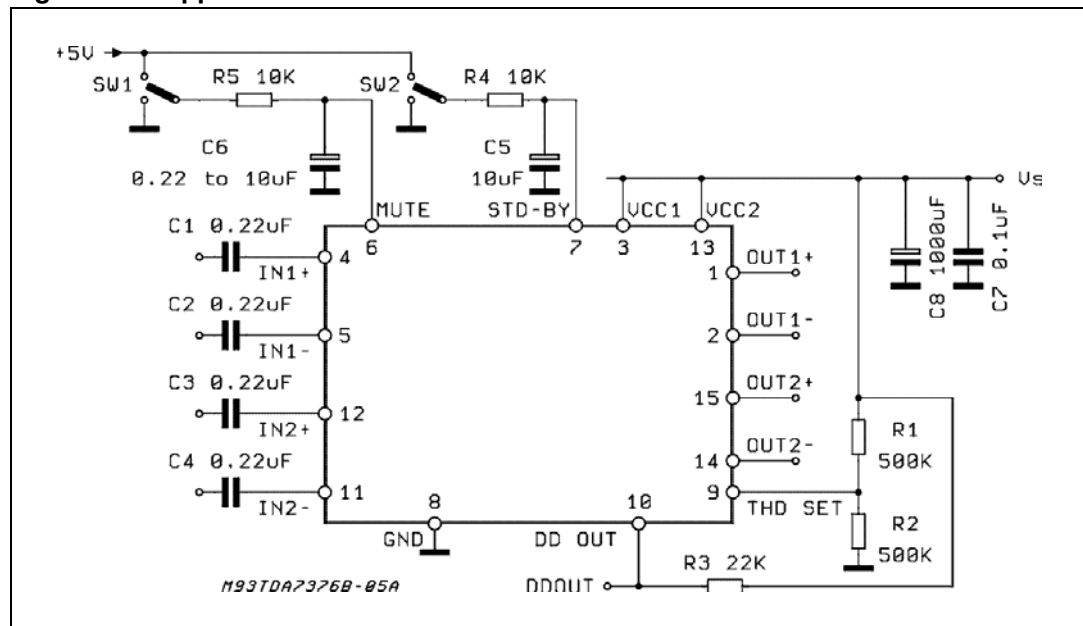


Figure 17. Application board reference circuit

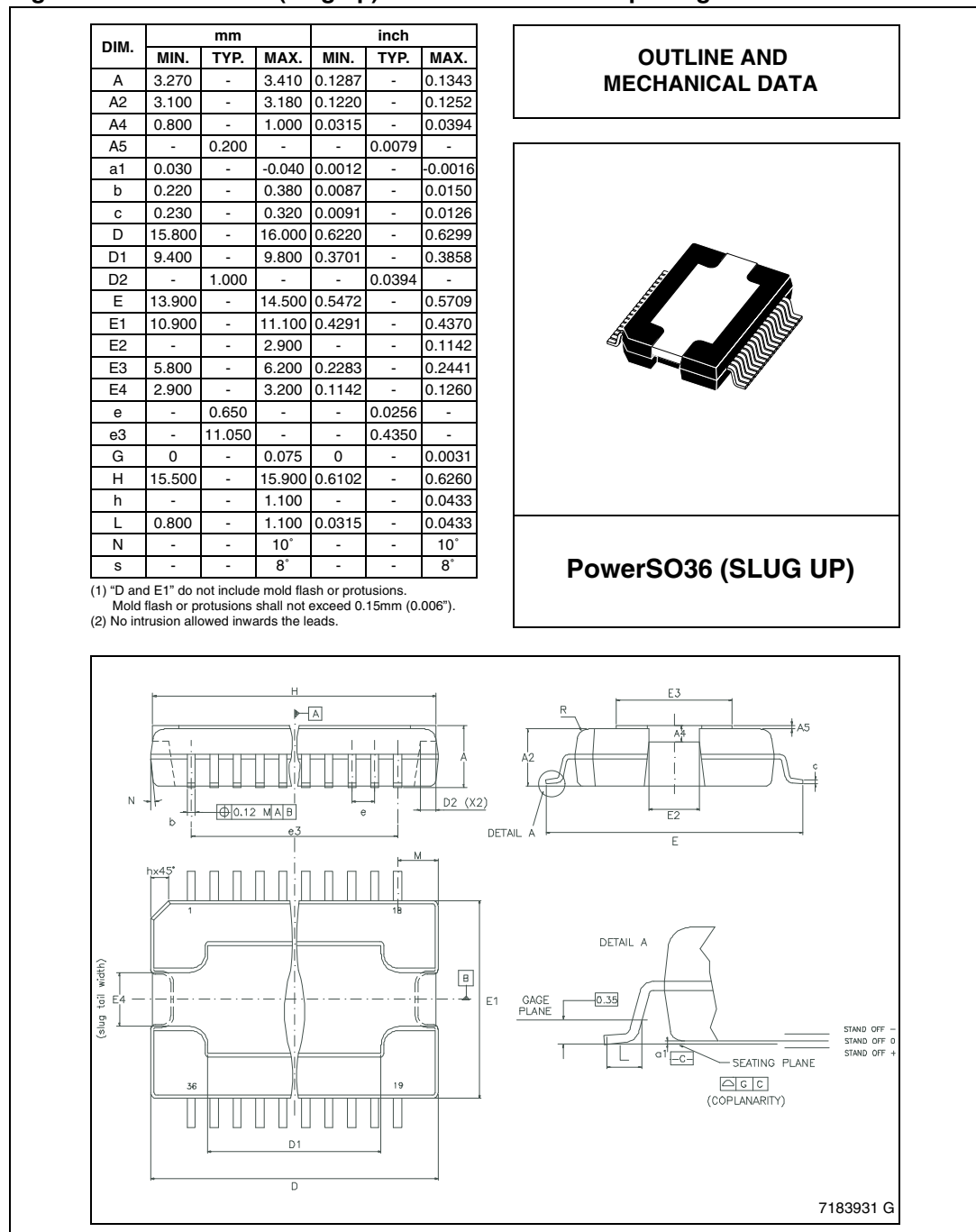


### 3 Package information

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**Figure 18. PowerSO36 (slug up) mechanical data and package dimensions**



## 4 Revision history

**Table 5. Document revision history**

| Date        | Revision | Changes                                                                                      |
|-------------|----------|----------------------------------------------------------------------------------------------|
| 13-Dec-2003 | 1        | Initial release.                                                                             |
| 16-Apr-2004 | 2        | Corrected package drawing.                                                                   |
| 11-Dec-2009 | 3        | Document reformatted.<br>Updated <a href="#">Section 3: Package information on page 12</a> . |
| 17-Sep-2013 | 4        | Updated Disclaimer.                                                                          |

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