

# LMF100

*LMF100 High Performance Dual Switched Capacitor Filter*



Literature Number: SNOSBG9A

## LMF100

# High Performance Dual Switched Capacitor Filter

### General Description

The LMF100 consists of two independent general purpose high performance switched capacitor filters. With an external clock and 2 to 4 resistors, various second-order and first-order filtering functions can be realized by each filter block. Each block has 3 outputs. One output can be configured to perform either an allpass, highpass, or notch function. The other two outputs perform bandpass and lowpass functions. The center frequency of each filter stage is tuned by using an external clock or a combination of a clock and resistor ratio. Up to a 4th-order biquadratic function can be realized with a single LMF100. Higher order filters are implemented by simply cascading additional packages, and all the classical filters (such as Butterworth, Bessel, Elliptic, and Chebyshev) can be realized.

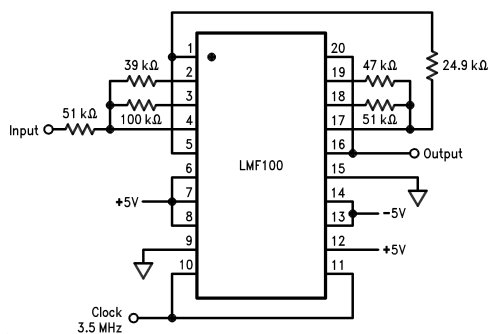
The LMF100 is fabricated on National Semiconductor's high performance analog silicon gate CMOS process,

LMCMOS™. This allows for the production of a very low off-set, high frequency filter building block. The LMF100 is pin-compatible with the industry standard MF10, but provides greatly improved performance.

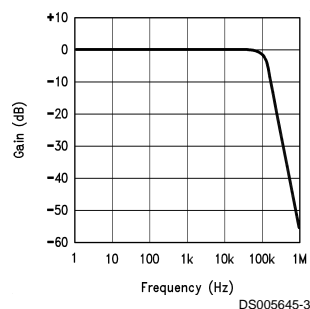
### Features

- Wide 4V to 15V power supply range
- Operation up to 100 kHz
- Low offset voltage: typically  
(50:1 or 100:1 mode): Vos1 = ±5 mV  
Vos2 = ±15 mV  
Vos3 = ±15 mV
- Low crosstalk -60 dB
- Clock to center frequency ratio accuracy ±0.2% typical
- $f_o \times Q$  range up to 1.8 MHz
- Pin-compatible with MF10

### 4th Order 100 kHz Butterworth Lowpass Filter



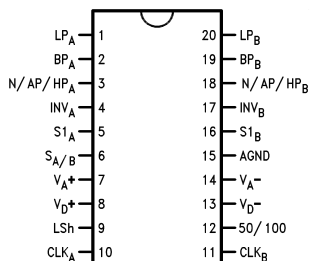
DS005645-2



DS005645-3

### Connection Diagram

#### Surface Mount and Dual-In-Line Package



DS005645-18

**Top View**  
**Order Number**  
**LMF100CCN or LMF100CIWM**  
**See NS Package Number N20A or M20B**

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 14)

Supply Voltage ( $V^+ - V^-$ )	16V
Voltage at Any Pin	$V^+ + 0.3V$ $V^- - 0.3V$
Input Current at Any Pin (Note 2)	5 mA
Package Input Current (Note 2)	20 mA
Power Dissipation (Note 3)	500 mW
Storage Temperature	150°C
ESD Susceptibility (Note 11)	2000V
Soldering Information	
N Package: 10 sec.	260°C

J Package: 10 sec. 300°C

SO Package:

Vapor Phase (60 sec.) 215°C

Infrared (15 sec.) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

## Operating Ratings (Note 1)

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
LMF100CCN	$0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
LMF100CIWM	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Supply Voltage	$4V \leq V^+ - V^- \leq 15V$

## Electrical Characteristics

The following specifications apply for Mode 1,  $Q = 10$  ( $R_1 = R_3 = 100k$ ,  $R_2 = 10k$ ),  $V^+ = +5V$  and  $V^- = -5V$  unless otherwise specified. **Boldface limits apply for  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ\text{C}$ .

Symbol	Parameter		Conditions	LMF100CCN			LMF100CIWM			Units
				Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$I_S$	Maximum Supply Current		$f_{CLK} = 250\text{ kHz}$ No Input Signal	9	13	<b>13</b>	9	<b>13</b>		mA
$f_0$	Center Frequency Range	MIN		0.1			0.1			Hz
		MAX		100			100			kHz
$f_{CLK}$	Clock Frequency Range	MIN		5.0			5.0			Hz
		MAX		3.5			3.5			MHz
$f_{CLK}/f_0$	Clock to Center Frequency Ratio Deviation		$V_{Pin12} = 5V$ or $0V$ $f_{CLK} = 1\text{ MHz}$	$\pm 0.2$	$\pm 0.8$	<b><math>\pm 0.8</math></b>	$\pm 0.2$	<b><math>\pm 0.8</math></b>		%
$\frac{\Delta Q}{Q}$	Q Error (MAX) (Note 4)		$Q = 10$ , Mode 1 $V_{Pin12} = 5V$ or $0V$ $f_{CLK} = 1\text{ MHz}$	$\pm 0.5$	$\pm 5$	<b><math>\pm 6</math></b>	$\pm 0.5$	<b><math>\pm 6</math></b>		%
$H_{OBP}$	Bandpass Gain at $f_0$		$f_{CLK} = 1\text{ MHz}$	0	$\pm 0.4$	<b><math>\pm 0.4</math></b>	0	<b><math>\pm 0.4</math></b>		dB
$H_{OLP}$	DC Lowpass Gain		$R_1 = R_2 = 10k$ $f_{CLK} = 250\text{ kHz}$	0	$\pm 0.2$	<b><math>\pm 0.2</math></b>	0	<b><math>\pm 0.2</math></b>		dB
$V_{OS1}$	DC Offset Voltage (Note 5)		$f_{CLK} = 250\text{ kHz}$	$\pm 5.0$	$\pm 15$	<b><math>\pm 15</math></b>	$\pm 5.0$	<b><math>\pm 15</math></b>		mV
$V_{OS2}$	DC Offset Voltage (Note 5)		$f_{CLK} = 250\text{ kHz}$	$\pm 30$	$\pm 80$	<b><math>\pm 80</math></b>	$\pm 30$	<b><math>\pm 80</math></b>		mV
		$S_{A/B} = V^-$		$\pm 15$	$\pm 70$	<b><math>\pm 70</math></b>	$\pm 15$	<b><math>\pm 70</math></b>		mV
$V_{OS3}$	DC Offset Voltage (Note 5)		$f_{CLK} = 250\text{ kHz}$	$\pm 15$	$\pm 40$	<b><math>\pm 60</math></b>	$\pm 15$	<b><math>\pm 60</math></b>		mV
	Crosstalk (Note 6)		A Side to B Side or B Side to A Side	-60			-60			dB
	Output Noise (Note 12)		$f_{CLK} = 250\text{ kHz}$	40			40			$\mu V$
			20 kHz Bandwidth	320			320			
			100:1 Mode	300			300			
	Clock Feedthrough (Note 13)		$f_{CLK} = 250\text{ kHz}$ 100:1 Mode	6			6			mV
$V_{OUT}$	Minimum Output Voltage Swing		$R_L = 5k$ (All Outputs)	+4.0 -4.7	$\pm 3.8$	<b><math>\pm 3.7</math></b>	+4.0 -4.7	<b><math>\pm 3.7</math></b>		V
			$R_L = 3.5k$ (All Outputs)	+3.9 -4.6			+3.9 -4.6			V
GBW	Op Amp Gain BW Product			5			5			MHz
SR	Op Amp Slew Rate			20			20			V/ $\mu s$
$I_{sc}$	Maximum Output Short	Source	(All Outputs)	12			12			mA
	Circuit Current (Note 7)	Sink		45			45			mA

## Electrical Characteristics (Continued)

The following specifications apply for Mode 1, Q = 10 ( $R_1 = R_3 = 100k$ ,  $R_2 = 10k$ ),  $V^+ = +5V$  and  $V^- = -5V$  unless otherwise specified. **Boldface limits apply for  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ C$ .

Symbol	Parameter	Conditions	LMF100CCN			LMF100CIWM			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$I_{IN}$	Input Current on Pins: 4, 5, 6, 9, 10, 11, 12, 16, 17			10			<b>10</b>		$\mu A$

## Electrical Characteristics

The following specifications apply for Mode 1, Q = 10 ( $R_1 = R_3 = 100k$ ,  $R_2 = 10k$ ),  $V^+ = +2.50V$  and  $V^- = -2.50V$  unless otherwise specified. **Boldface limits apply for  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ C$ .

Symbol	Parameter		Conditions	LMF100CCN			LMF100CIWM			Units
				Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
$I_s$	Maximum Supply Current		$f_{CLK} = 250$ kHz No Input Signal	8	12	<b>12</b>	8	<b>12</b>		mA
$f_0$	Center Frequency Range	MIN		0.1			0.1			Hz
		MAX		50			50			kHz
$f_{CLK}$	Clock Frequency Range	MIN		5.0			5.0			Hz
		MAX		1.5			1.5			MHz
$f_{CLK}/f_0$	Clock to Center Frequency Ratio Deviation		$V_{Pin12} = 2.5V$ or $0V$ $f_{CLK} = 1$ MHz	$\pm 0.2$	$\pm 1$	<b><math>\pm 1</math></b>	$\pm 0.2$	<b><math>\pm 1</math></b>		%
$\frac{\Delta Q}{Q}$	Q Error (MAX) (Note 4)		Q = 10, Mode 1 $V_{Pin12} = 5V$ or $0V$ $f_{CLK} = 1$ MHz	$\pm 0.5$	$\pm 5$	<b><math>\pm 8</math></b>	$\pm 0.5$	<b><math>\pm 8</math></b>		%
$H_{OBP}$	Bandpass Gain at $f_0$		$f_{CLK} = 1$ MHz	0	$\pm 0.4$	<b><math>\pm 0.5</math></b>	0	<b><math>\pm 0.5</math></b>		dB
$H_{OLP}$	DC Lowpass Gain		$R_1 = R_2 = 10k$ $f_{CLK} = 250$ kHz	0	$\pm 0.2$	<b><math>\pm 0.2</math></b>	0	<b><math>\pm 0.2</math></b>		dB
$V_{OS1}$	DC Offset Voltage (Note 5)		$f_{CLK} = 250$ kHz	$\pm 5.0$	$\pm 15$	<b><math>\pm 15</math></b>	$\pm 5.0$	<b><math>\pm 15</math></b>		mV
$V_{OS2}$	DC Offset Voltage (Note 5)		$f_{CLK} = 250$ kHz	$\pm 20$	$\pm 60$	<b><math>\pm 60</math></b>	$\pm 20$	<b><math>\pm 60</math></b>		mV
			$S_{A/B} = V^-$	$\pm 10$	$\pm 50$	<b><math>\pm 60</math></b>	$\pm 10$	<b><math>\pm 60</math></b>		mV
$V_{OS3}$	DC Offset Voltage (Note 5)		$f_{CLK} = 250$ kHz	$\pm 10$	$\pm 25$	<b><math>\pm 30</math></b>	$\pm 10$	<b><math>\pm 30</math></b>		mV
	Crosstalk (Note 6)		A Side to B Side or B Side to A Side	-65			-65			dB
	Output Noise (Note 12)		$f_{CLK} = 250$ kHz	25			25			$\mu V$
			20 kHz Bandwidth	250			250			
			100:1 Mode	220			220			
	Clock Feedthrough (Note 13)		$f_{CLK} = 250$ kHz 100:1 Mode	2			2			mV
$V_{OUT}$	Minimum Output Voltage Swing		$R_L = 5k$ (All Outputs)	+1.6 -2.2	$\pm 1.5$	<b><math>\pm 1.4</math></b>	+1.6 -2.2	<b><math>\pm 1.4</math></b>		V
			$R_L = 3.5k$ (All outputs)	+1.5 -2.1			+1.5 -2.1			V
GBW	Op Amp Gain BW Product			5			5			MHz
SR	Op Amp Slew Rate			18			18			V/ $\mu s$
$I_{sc}$	Maximum Output Short Circuit Current (Note 7)	Source	(All Outputs)	10			10			mA
		Sink		20			20			mA

## Logic Input Characteristics

**Boldface limits apply for  $T_{MIN}$  to  $T_{MAX}$ ; all other limits  $T_A = T_J = 25^{\circ}\text{C}$ .**

Parameter		Conditions	LMF100CCN			LMF100CIWM			Units
			Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	Typical (Note 8)	Tested Limit (Note 9)	Design Limit (Note 10)	
CMOS Clock Input Voltage	MIN Logical "1"	$V^+ = +5\text{V}, V^- = -5\text{V},$		+3.0	<b>+3.0</b>		<b>+3.0</b>		V
	MAX Logical "0"	$V_{LSh} = 0\text{V}$		-3.0	<b>-3.0</b>		<b>-3.0</b>		V
	MIN Logical "1"	$V^+ = +10\text{V}, V^- = 0\text{V},$		+8.0	<b>+8.0</b>		<b>+8.0</b>		V
	MAX Logical "0"	$V_{LSh} = +5\text{V}$		+2.0	<b>+2.0</b>		<b>+2.0</b>		V
TTL Clock Input Voltage	MIN Logical "1"	$V^+ = +5\text{V}, V^- = -5\text{V},$		+2.0	<b>+2.0</b>		<b>+2.0</b>		V
	MAX Logical "0"	$V_{LSh} = 0\text{V}$		+0.8	<b>+0.8</b>		<b>+0.8</b>		V
	MIN Logical "1"	$V^+ = +10\text{V}, V^- = 0\text{V},$		+2.0	<b>+2.0</b>		<b>+2.0</b>		V
	MAX Logical "0"	$V_{LSh} = 0\text{V}$		+0.8	<b>+0.8</b>		<b>+0.8</b>		V
CMOS Clock Input Voltage	MIN Logical "1"	$V^+ = +2.5\text{V}, V^- = -2.5\text{V},$		+1.5	<b>+1.5</b>		<b>+1.5</b>		V
	MAX Logical "0"	$V_{LSh} = 0\text{V}$		-1.5	<b>-1.5</b>		<b>-1.5</b>		V
	MIN Logical "1"	$V^+ = +5\text{V}, V^- = 0\text{V},$		+4.0	<b>+4.0</b>		<b>+4.0</b>		V
	MAX Logical "0"	$V_{LSh} = +2.5\text{V}$		+1.0	<b>+1.0</b>		<b>+1.0</b>		V
TTL Clock Input Voltage	MIN Logical "1"	$V^+ = +5\text{V}, V^- = 0\text{V},$		+2.0	<b>+2.0</b>		<b>+2.0</b>		V
	MAX Logical "0"	$V_{LSh} = 0\text{V}, V_{D^+} = 0\text{V}$		+0.8	<b>+0.8</b>		<b>+0.8</b>		V

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional. These ratings do not guarantee specific performance limits, however. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** When the input voltage ( $V_{IN}$ ) at any pin exceeds the power supply rails ( $V_{IN} < V^-$  or  $V_{IN} > V^+$ ) the absolute value of current at that pin should be limited to 5 mA or less. The sum of the currents at all pins that are driven beyond the power supply voltages should not exceed 20 mA.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation at any temperature is  $P_D = (T_{JMAX} - T_A)/\theta_{JA}$  or the number given in the Absolute Maximum Ratings, whichever is lower. For this device,  $T_{JMAX} = 125^{\circ}\text{C}$ , and the typical junction-to-ambient thermal resistance of the LMF100CCN when board mounted is  $55^{\circ}\text{C/W}$ . For the LMF100CIWM this number is  $66^{\circ}\text{C/W}$ .

**Note 4:** The accuracy of the Q value is a function of the center frequency ( $f_0$ ). This is illustrated in the curves under the heading "Typical Performance Characteristics".

**Note 5:**  $V_{OS1}$ ,  $V_{OS2}$ , and  $V_{OS3}$  refer to the internal offsets as discussed in the Applications Information section 3.4.

**Note 6:** Crosstalk between the internal filter sections is measured by applying a 1  $V_{RMS}$  10 kHz signal to one bandpass filter section input and grounding the input of the other bandpass filter section. The crosstalk is the ratio between the output of the grounded filter section and the 1  $V_{RMS}$  input signal of the other section.

**Note 7:** The short circuit source current is measured by forcing the output that is being tested to its maximum positive voltage swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output that is being tested to its maximum negative voltage swing and then shorting that output to the positive supply. These are the worst case conditions.

**Note 8:** Typicals are at  $25^{\circ}\text{C}$  and represent most likely parametric norm.

**Note 9:** Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 10:** Design limits are guaranteed to National's AOQL (Average Outgoing Quality Level) but are not 100% tested.

**Note 11:** Human body model, 100 pF discharged through a 1.5 k $\Omega$  resistor.

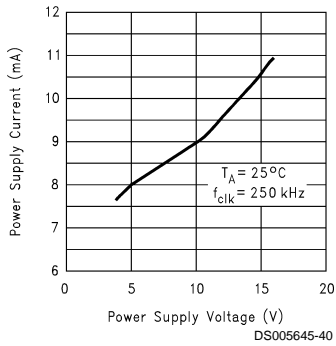
**Note 12:** In 50:1 mode the output noise is 3 dB higher.

**Note 13:** In 50:1 mode the clock feedthrough is 6 dB higher.

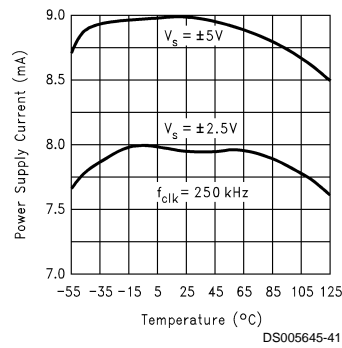
**Note 14:** A military RETS specification is available upon request.

## Typical Performance Characteristics

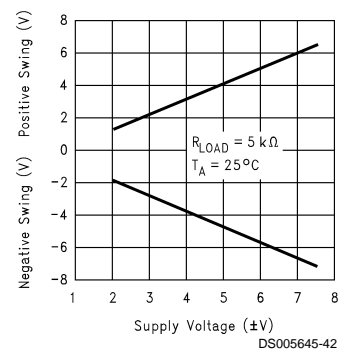
**Power Supply Current vs Power Supply Voltage**



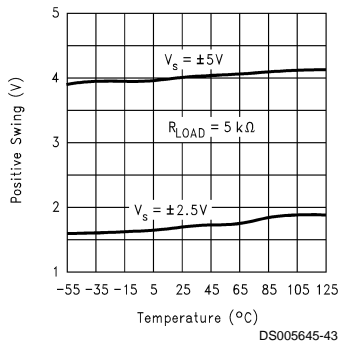
**Power Supply Current vs Temperature**



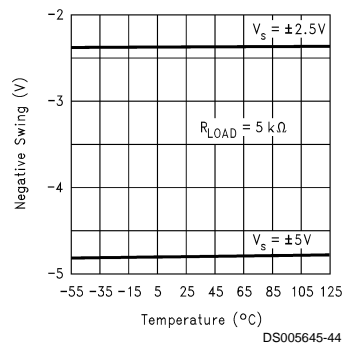
**Output Swing vs Supply Voltage**



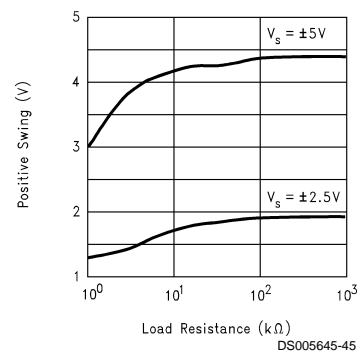
**Positive Output Swing vs Temperature**



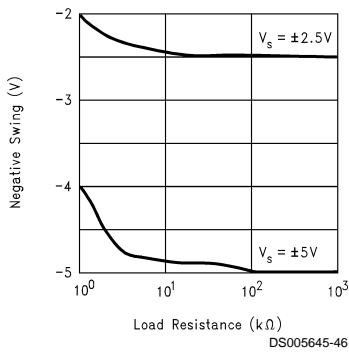
**Negative Output Swing vs Temperature**



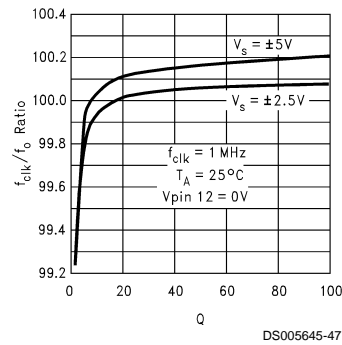
**Positive Output Voltage Swing vs Load Resistance**



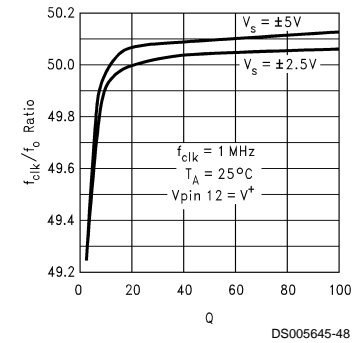
**Negative Output Voltage Swing vs Load Resistance**



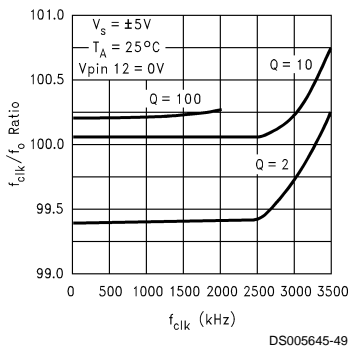
**$f_{CLK}/f_0$  Ratio vs Q**



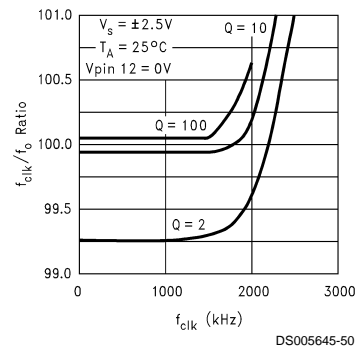
**$f_{CLK}/f_0$  Ratio vs Q**



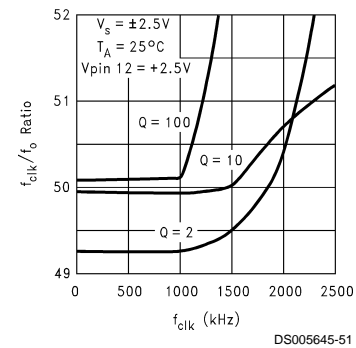
**$f_{CLK}/f_0$  Ratio vs  $f_{CLK}$**



**$f_{CLK}/f_0$  Ratio vs  $f_{CLK}$**

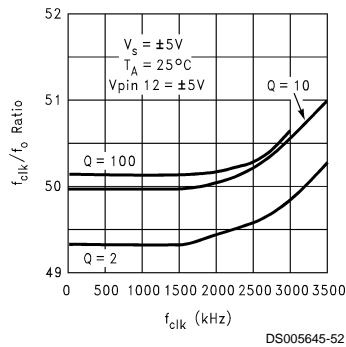


**$f_{CLK}/f_0$  Ratio vs  $f_{CLK}$**

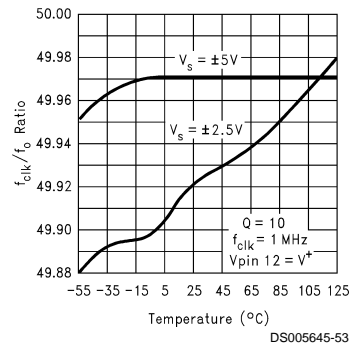


# Typical Performance Characteristics (Continued)

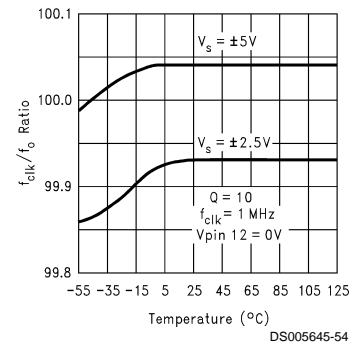
## $f_{CLK}/f_0$ Ratio vs $f_{CLK}$



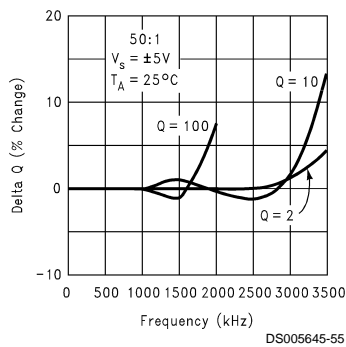
## $f_{CLK}/f_0$ Ratio vs Temperature



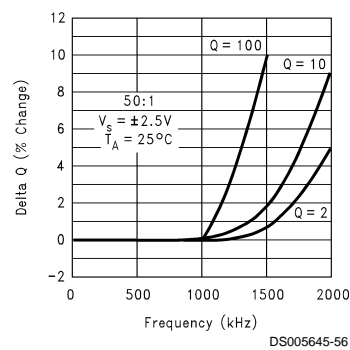
## $f_{CLK}/f_0$ Ratio vs Temperature



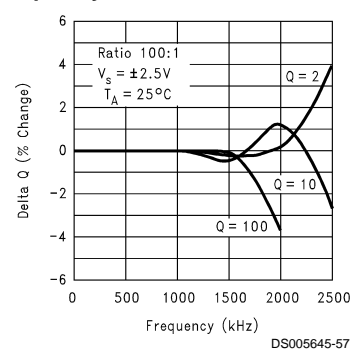
## Q Deviation vs Clock Frequency



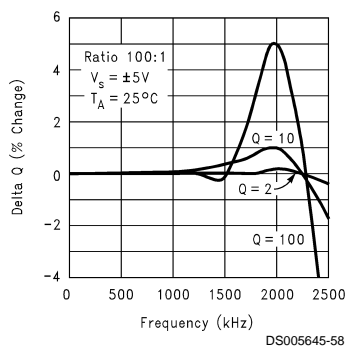
## Q Deviation vs Clock Frequency



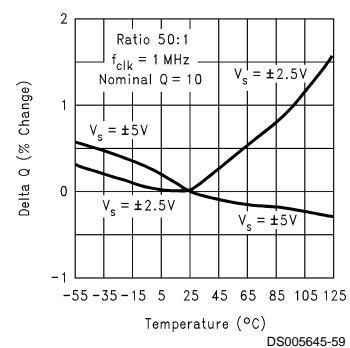
## Q Deviation vs Clock Frequency



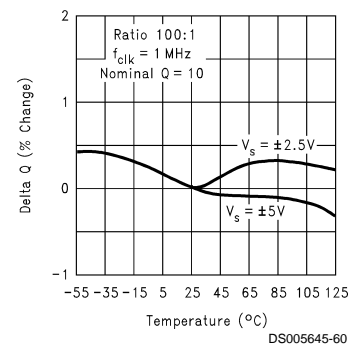
## Q Deviation vs Clock Frequency



## Q Deviation vs Temperature

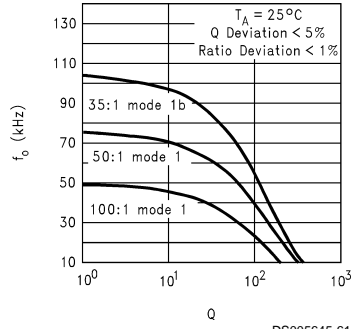


## Q Deviation vs Temperature

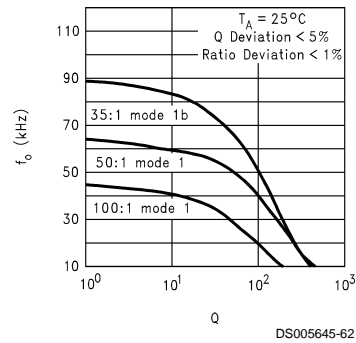


# Typical Performance Characteristics (Continued)

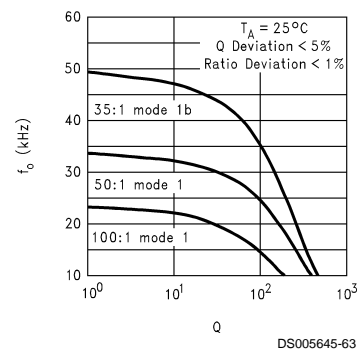
Maximum  $f_o$  vs Q at  
 $V_s = \pm 7.5V$



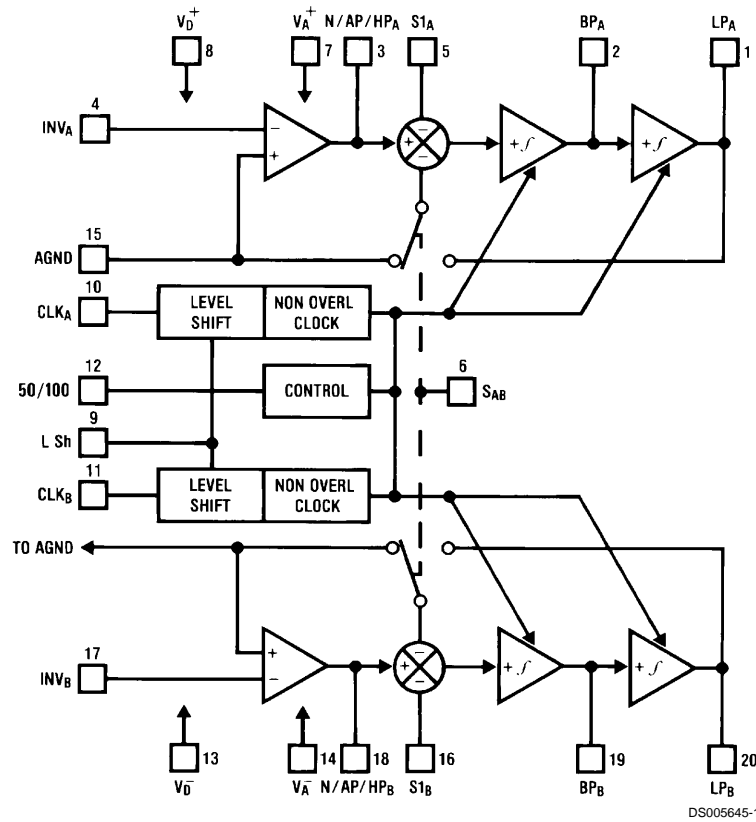
Maximum  $f_o$  vs Q at  
 $V_s = \pm 5.0V$



Maximum  $f_o$  vs Q at  
 $V_s = \pm 2.5V$



## LMF100 System Block Diagram





## Pin Descriptions

LP(1,20), BP(2,19), N/AP/HP(3,18)	The second order lowpass, bandpass and notch/allpass/highpass outputs. These outputs can typically swing to within 1V of each supply when driving a 5 k $\Omega$ load. For optimum performance, capacitive loading on these outputs should be minimized. For signal frequencies above 15 kHz the capacitance loading should be kept below 30 pF.	LSh(9)	Level shift pin. This is used to accommodate various clock levels with dual or single supply operation. With dual $\pm 5V$ supplies and CMOS ( $\pm 5V$ ) or TTL (0V–5V) clock levels, LSh should be tied to system ground.  For 0V–10V single supply operation the AGND pin should be biased at +5V and the LSh pin should be tied to the system ground for TTL clock levels. LSh should be biased at +5V for $\pm 5V$ CMOS clock levels.  The LSh pin is tied to system ground for $\pm 2.5V$ operation. For single 5V operation the LSh and $V_{D+}$ pins are tied to system ground for TTL clock levels.
INV(4,17)	The inverting input of the summing opamp of each filter. These are high impedance inputs. The non-inverting input is internally tied to AGND so the opamp can be used only as an inverting amplifier.	CLK(10,11)	Clock inputs for the two switched capacitor filter sections. Unipolar or bipolar clock levels may be applied to the CLK inputs according to the programming voltage applied to the LSh pin. The duty cycle of the clock should be close to 50%, especially when clock frequencies above 200 kHz are used. This allows the maximum time for the internal opamps to settle, which yields optimum filter performance.
S1(5,16)	S1 is a signal input pin used in modes 1b, 4, and 5. The input impedance is $1/f_{CLK} \times 1 \text{ pF}$ . The pin should be driven with a source impedance of less than 1 k $\Omega$ . If S1 is not driven with a signal it should be tied to AGND (mid-supply).	50/100(12) (Note 15)	By tying this pin to $V^+$ a 50:1 clock to filter center frequency ratio is obtained. Tying this pin at mid-supply (i.e., system ground with dual supplies) or to $V^-$ allows the filter to operate at a 100:1 clock to center frequency ratio.
$S_{A/B}$ (6)	This pin activates a switch that connects one of the inputs of each filter's second summer either to AGND ( $S_{A/B}$ tied to $V^-$ ) or to the lowpass (LP) output ( $S_{A/B}$ tied to $V^+$ ). This offers the flexibility needed for configuring the filter in its various modes of operation.	AGND(15)	This is the analog ground pin. This pin should be connected to the system ground for dual supply operation or biased to mid-supply for single supply operation. For a further discussion of mid-supply biasing techniques see the Applications Information (Section 3.2). For optimum filter performance a "clean" ground must be provided.
$V_A^+$ (7) (Note 15)	This is both the analog and digital positive supply.		
$V_D^+$ (8) (Note 15)	This pin needs to be tied to $V^+$ except when the device is to operate on a single 5V supply and a TTL level clock is applied. For 5V, TTL operation, $V_D^+$ should be tied to ground (0V).		
$V_A^-$ (14), $V_D^-$ (13)	Analog and digital negative supplies. $V_A^-$ and $V_D^-$ should be derived from the same source. They have been brought out separately so they can be bypassed by separate capacitors, if desired. They can also be tied together externally and bypassed with a single capacitor.		

**Note 15:** This device is pin-for-pin compatible with the MF10 except for the following changes:

1. Unlike the MF10, the LMF100 has a single positive supply pin ( $V_A^+$ ).
2. On the LMF100  $V_D^+$  is a control pin and is not the digital positive supply as on the MF10.
3. Unlike the MF10, the LMF100 does not support the current limiting mode. When the 50/100 pin is tied to  $V^-$  the LMF100 will remain in the 100:1 mode.

## 1.0 Definitions of Terms

**f<sub>CLK</sub>**: the frequency of the external clock signal applied to pin 10 or 11.

**f<sub>0</sub>**: center frequency of the second order function complex pole pair. f<sub>0</sub> is measured at the bandpass outputs of the LMF100, and is the frequency of maximum bandpass gain. (Figure 1).

**f<sub>notch</sub>**: the frequency of minimum (ideally zero) gain at the notch outputs.

**f<sub>z</sub>**: the center frequency of the second order complex zero pair, if any. If f<sub>z</sub> is different from f<sub>0</sub> and if Q<sub>z</sub> is high, it can be observed as the frequency of a notch at the allpass output. (Figure 13).

**Q**: “quality factor” of the 2nd order filter. Q is measured at the bandpass outputs of the LMF100 and is equal to f<sub>0</sub> divided by the –3 dB bandwidth of the 2nd order bandpass filter (Figure 1). The value of Q determines the shape of the 2nd order filter responses as shown in Figure 6.

**Q<sub>z</sub>**: the quality factor of the second order complex zero pair, if any. Q<sub>z</sub> is related to the allpass characteristic, which is written:

$$H_{AP}(s) = \frac{H_{OAP} \left( s^2 - \frac{s\omega_o}{Q_z} + \omega_o^2 \right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

where Q<sub>z</sub> = Q for an all-pass response.

**H<sub>OBP</sub>**: the gain (in V/V) of the bandpass output at f = f<sub>0</sub>.

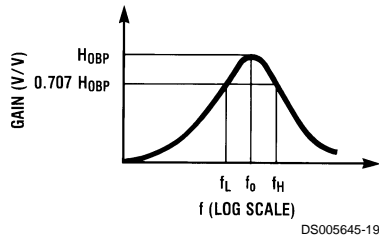
**H<sub>OLP</sub>**: the gain (in V/V) of the lowpass output as f → 0 Hz (Figure 2).

**H<sub>OHP</sub>**: the gain (in V/V) of the highpass output as f → f<sub>CLK</sub>/2 (Figure 3).

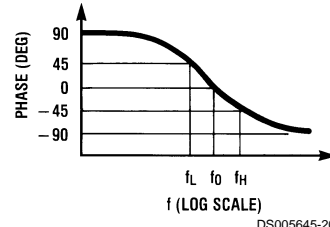
**H<sub>ON</sub>**: the gain (in V/V) of the notch output as f → 0 Hz and as f → f<sub>CLK</sub>/2, when the notch filter has equal gain above and below the center frequency (Figure 4). When the low-frequency gain differs from the high-frequency gain, as in modes 2 and 3a (Figure 10 and Figure 12), the two quantities below are used in place of H<sub>ON</sub>.

**H<sub>ON1</sub>**: the gain (in V/V) of the notch output as f → 0 Hz.

**H<sub>ON2</sub>**: the gain (in V/V) of the notch output as f → f<sub>CLK</sub>/2.



(a)



(b)

$$H_{BP}(s) = \frac{H_{OBP} \frac{\omega_o}{Q} s}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$Q = \frac{f_0}{f_H - f_L}; f_0 = \sqrt{f_L f_H}$$

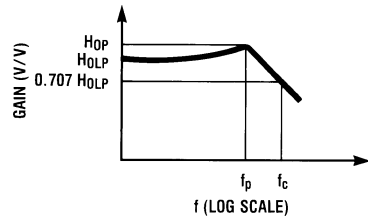
$$f_L = f_0 \left( \frac{-1}{2Q} + \sqrt{\left( \frac{1}{2Q} \right)^2 + 1} \right)$$

$$f_H = f_0 \left( \frac{1}{2Q} + \sqrt{\left( \frac{1}{2Q} \right)^2 + 1} \right)$$

$$\omega_o = 2\pi f_0$$

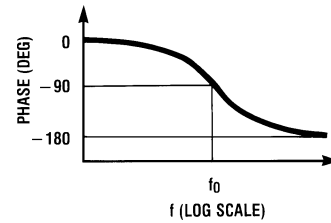
FIGURE 1. 2nd-Order Bandpass Response

## 1.0 Definitions of Terms (Continued)



DS005645-21

(a)



DS005645-22

(b)

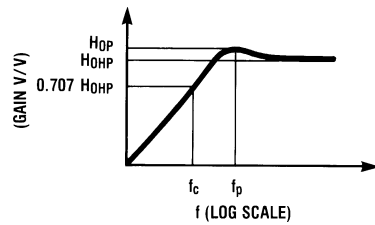
$$H_{LP}(s) = \frac{H_{OLP}\omega_o^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$f_c = f_0 \times \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$f_p = f_0 \sqrt{1 - \frac{1}{2Q^2}}$$

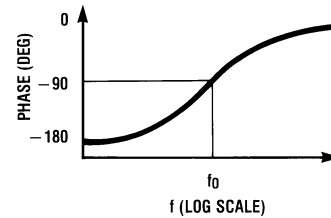
$$H_{OP} = H_{OLP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 2. 2nd-Order Low-Pass Response



DS005645-23

(a)



DS005645-24

(b)

$$H_{HP}(s) = \frac{H_{OHP}s^2}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

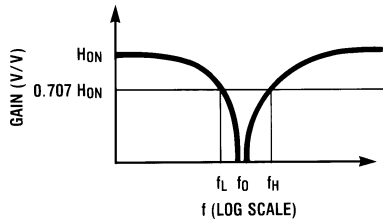
$$f_c = f_0 \times \left[ \sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}} \right]^{-1}$$

$$f_p = f_0 \times \left[ \sqrt{1 - \frac{1}{2Q^2}} \right]^{-1}$$

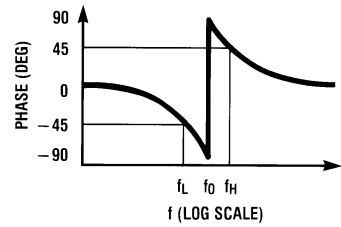
$$H_{OP} = H_{OHP} \times \frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

FIGURE 3. 2nd-Order High-Pass Response

## 1.0 Definitions of Terms (Continued)



(a)



(b)

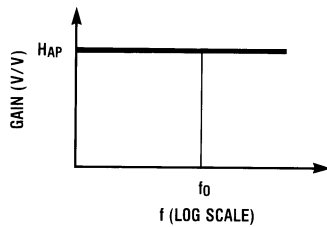
$$H_N(s) = \frac{H_{0N}(s^2 + \omega_o^2)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

$$Q = \frac{f_0}{f_H - f_L}; f_0 = \sqrt{f_L f_H}$$

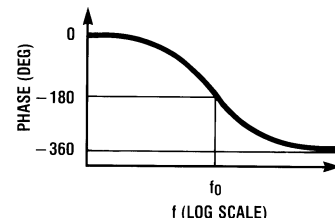
$$f_L = f_0 \left( \frac{-1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

$$f_H = f_0 \left( \frac{1}{2Q} + \sqrt{\left(\frac{1}{2Q}\right)^2 + 1} \right)$$

FIGURE 4. 2nd-Order Notch Response



(a)



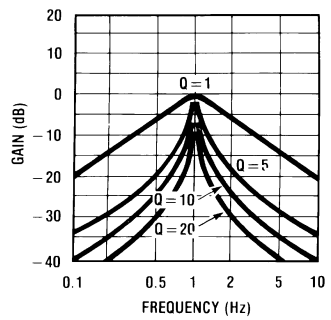
(b)

$$H_{AP}(s) = \frac{H_{0AP} \left( s^2 - \frac{s\omega_o}{Q} + \omega_o^2 \right)}{s^2 + \frac{s\omega_o}{Q} + \omega_o^2}$$

FIGURE 5. 2nd-Order All-Pass Response

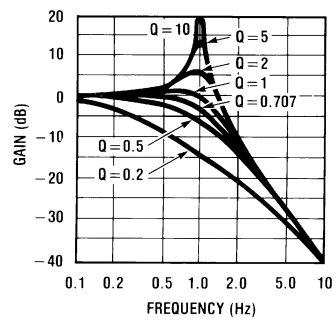
## 1.0 Definitions of Terms (Continued)

(a) Bandpass



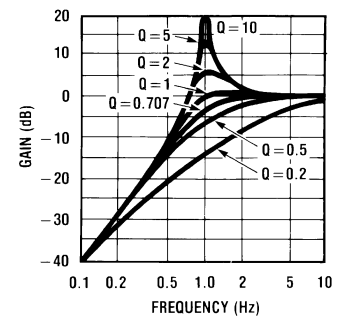
DS005645-64

(b) Low Pass



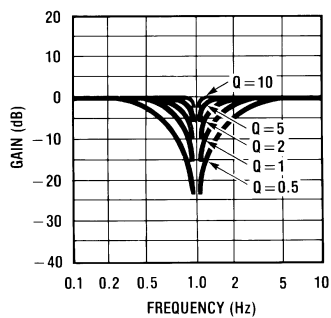
DS005645-65

(c) High-Pass



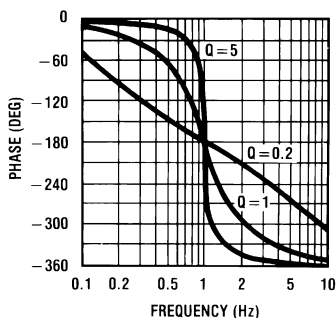
DS005645-66

(d) Notch



DS005645-67

(e) All-Pass



DS005645-68

**FIGURE 6. Response of various 2nd-order filters as a function of Q. Gains and center frequencies are normalized to unity.**

## 2.0 Modes of Operation

The LMF100 is a switched capacitor (sampled data) filter. To fully describe its transfer functions, a time domain analysis is appropriate. Since this is cumbersome, and since the LMF100 closely approximates continuous filters, the following discussion is based on the well-known frequency domain. Each LMF100 can produce two full 2nd order functions. See *Table 1* for a summary of the characteristics of the various modes.

### MODE 1: Notch 1, Bandpass, Lowpass Outputs:

$$f_{\text{notch}} = f_0 \text{ (See Figure 7)}$$

$f_0$  = center frequency of the complex pole pair

$$= \frac{f_{\text{CLK}}}{100} \text{ or } \frac{f_{\text{CLK}}}{50}$$

$f_{\text{notch}}$  = center frequency of the imaginary zero pair =  $f_0$ .

$$H_{\text{OLP}} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R_2}{R_1}$$

$$H_{\text{OBP}} = \text{Bandpass gain (at } f = f_0) = -\frac{R_3}{R_1}$$

$$H_{\text{ON}} = \text{Notch output gain as } \left. \begin{matrix} f \rightarrow 0 \\ f \rightarrow f_{\text{CLK}}/2 \end{matrix} \right\} = \frac{-R_2}{R_1}$$

$$Q = \frac{f_0}{BW} = \frac{R_3}{R_2}$$

= quality factor of the complex pole pair

BW = the -3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{\text{OLP}} = \frac{H_{\text{OBP}}}{Q} \text{ or } H_{\text{OBP}} = H_{\text{OLP}} \times Q$$

$$= H_{\text{ON}} \times Q.$$

$$H_{\text{OLP(peak)}} \cong Q \times H_{\text{OLP}} \text{ (for high Q's)}$$

### MODE 1a: Non-Inverting BP, LP (See Figure 8)

$$f_0 = \frac{f_{\text{CLK}}}{100} \text{ or } \frac{f_{\text{CLK}}}{50}$$

$$Q = \frac{R_3}{R_2}$$

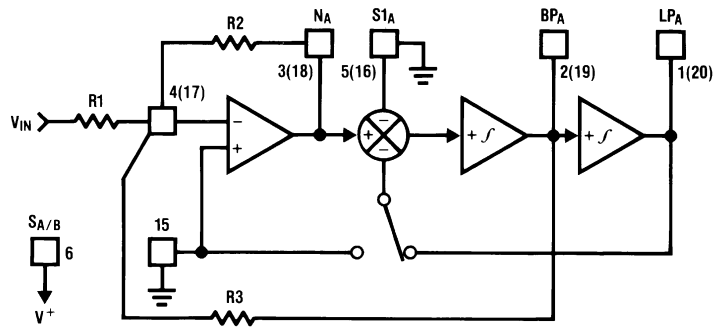
$$H_{\text{OLP}} = -1; H_{\text{OLP(peak)}} \cong Q \times H_{\text{OLP}} \text{ (for high Q's)}$$

$$H_{\text{OBP}_1} = -\frac{R_3}{R_2}$$

$$H_{\text{OBP}_2} = 1 \text{ (non-inverting)}$$

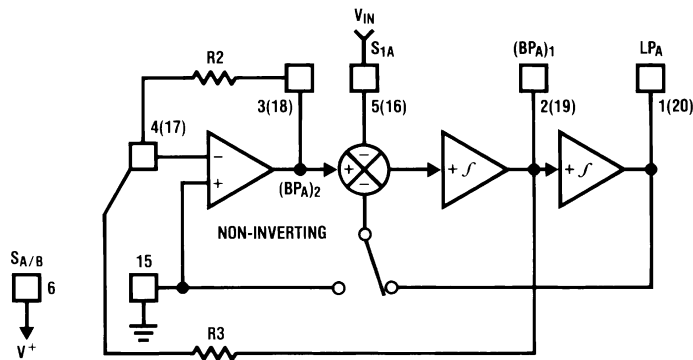
$$\text{Circuit dynamics: } H_{\text{OBP}_1} = Q$$

Note:  $V_{\text{IN}}$  should be driven from a low impedance (<1 k $\Omega$ ) source.



DS005645-11

FIGURE 7. MODE 1



DS005645-4

FIGURE 8. MODE 1a

## 2.0 Modes of Operation (Continued)

### MODE 1b: Notch 1, Bandpass, Lowpass Outputs:

$$f_{\text{notch}} = f_0 \text{ (See Figure 9)}$$

$f_0$  = center frequency of the complex pole pair

$$= \frac{f_{\text{CLK}}}{100} \times \sqrt{2} \text{ or } \frac{f_{\text{CLK}}}{50} \times \sqrt{2}$$

$f_{\text{notch}}$  = center frequency of the imaginary zero pair =  $f_0$ .

$H_{\text{OLP}}$  = Lowpass gain (as  $f \rightarrow 0$ ) =  $-\frac{R_2}{2R_1}$

$H_{\text{OBP}}$  = Bandpass gain (at  $f = f_0$ ) =  $-\frac{R_3}{R_1}$

$H_{\text{ON}}$  = Notch output gain as  $f \rightarrow 0$   
 $f \rightarrow f_{\text{CLK}}/2 \} = -\frac{R_2}{R_1}$

$$Q = \frac{f_0}{\text{BW}} = \frac{R_3}{R_2} \times \sqrt{2}$$

= quality factor of the complex pole pair

BW = the -3 dB bandwidth of the bandpass output.

Circuit dynamics:

$$H_{\text{OLP}} = \frac{H_{\text{OBP}}}{\sqrt{2} Q} \text{ or } H_{\text{OBP}} = H_{\text{OLP}} \times Q \times \sqrt{2}$$

$$H_{\text{OBP}} = \frac{H_{\text{ON}} \times Q}{\sqrt{2}}$$

$$H_{\text{OLP(peak)}} \cong Q \times H_{\text{OLP}} \text{ (for high Q's)}$$

### MODE 2: Notch 2, Bandpass, Lowpass: $f_{\text{notch}} < f_0$

(See Figure 10)

$f_0$  = center frequency

$$= \frac{f_{\text{CLK}}}{100} \sqrt{\frac{R_2}{R_4} + 1} \text{ or } \frac{f_{\text{CLK}}}{50} \sqrt{\frac{R_2}{R_4} + 1}$$

$$f_{\text{notch}} = \frac{f_{\text{CLK}}}{100} \text{ or } \frac{f_{\text{CLK}}}{50}$$

$Q$  = quality factor of the complex pole pair

$$= \frac{\sqrt{R_2/R_4 + 1}}{R_2/R_3}$$

$H_{\text{OLP}}$  = Lowpass output gain (as  $f \rightarrow 0$ )

$$= -\frac{R_2/R_1}{R_2/R_4 + 1}$$

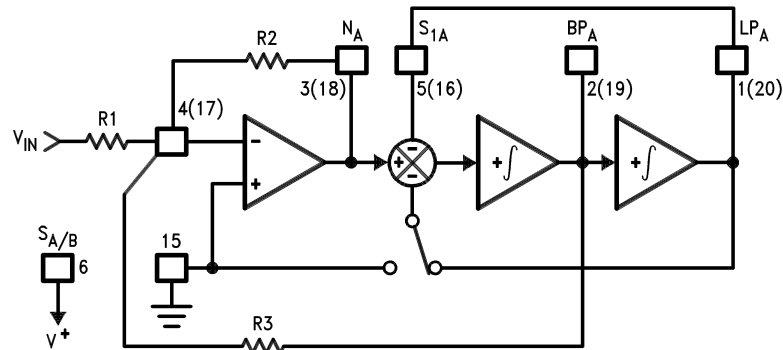
$H_{\text{OBP}}$  = Bandpass output gain (at  $f = f_0$ ) =  $-R_3/R_1$

$H_{\text{ON}_1}$  = Notch output gain (as  $f \rightarrow 0$ )

$$= -\frac{R_2/R_1}{R_2/R_4 + 1}$$

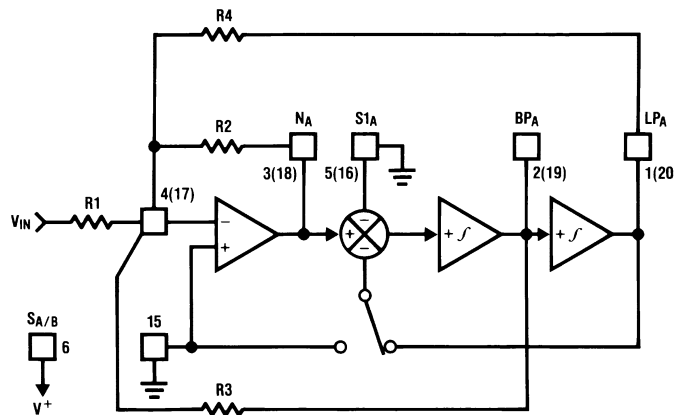
$$H_{\text{ON}_2} = \text{Notch output gain} \left( \text{as } f \rightarrow \frac{f_{\text{CLK}}}{2} \right) = -R_2/R_1$$

$$\text{Filter dynamics: } H_{\text{OBP}} = Q \sqrt{H_{\text{OLP}} H_{\text{ON}_2}} = \sqrt{H_{\text{ON}_1} H_{\text{ON}_2}}$$



DS005645-14

FIGURE 9. MODE 1b



DS005645-36

FIGURE 10. MODE 2

## 2.0 Modes of Operation (Continued)

### MODE 3: Highpass, Bandpass, Lowpass Outputs

(See *Figure 11*)

$$f_0 = \frac{f_{\text{CLK}}}{100} \times \sqrt{\frac{R_2}{R_4}} \text{ or } \frac{f_{\text{CLK}}}{50} \times \sqrt{\frac{R_2}{R_4}}$$

Q = quality factor of the complex pole pair

$$= \sqrt{\frac{R_2}{R_4}} \times \frac{R_3}{R_2}$$

$$H_{OHP} = \text{Highpass gain} \left( \text{at } f \rightarrow \frac{f_{CLK}}{2} \right) = -\frac{R2}{R1}$$

$$H_{\text{OBP}} = \text{Bandpass gain (at } f = f_0) = -\frac{R_3}{R_1}$$

$$H_{OLP} = \text{Lowpass gain (as } f \rightarrow 0) = -\frac{R_4}{R_1}$$

Circuit dynamics:  $\frac{R2}{R4} = \frac{H_{OHP}}{H_{OLP}}$ ;  $H_{OBP} = \sqrt{H_{OHP} \times H_{OLP} \times Q}$

$$H_{OLP(\text{peak})} \cong Q \times H_{OLP} \text{ (for high } Q\text{'s)}$$

$$H_{OHP}(\text{peak}) \cong Q \times H_{OHP} \text{ (for high } Q\text{'s)}$$

### MODE 3a: HP, BP, LP and Notch with External Op Amp

(See *Figure 12*)

$$f_0 = \frac{f_{\text{CLK}}}{100} \times \sqrt{\frac{R_2}{R_4}} \text{ or } \frac{f_{\text{CLK}}}{50} \times \sqrt{\frac{R_2}{R_4}}$$

$$Q = \sqrt{\frac{R_2}{R_4}} \times \frac{R_3}{R_2}$$

$$H_{OHP} = -\frac{R_2}{R_1}$$

$$H_{OBP} = -\frac{R_3}{R_1}$$

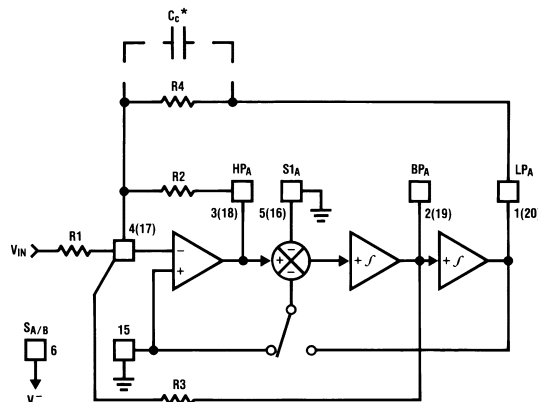
$$H_{OLP} = -\frac{R_4}{R_1}$$

$$f_n = \text{notch frequency} = \frac{f_{\text{CLK}}}{100} \sqrt{\frac{R_h}{R_l}} \text{ or } \frac{f_{\text{CLK}}}{50} \sqrt{\frac{R_h}{R_l}}$$

$$H_{ON} = \text{gain of notch at } f = f_0 = \left\| Q \left( \frac{R_g}{R_l} H_{OLP} - \frac{R_g}{R_h} H_{OHP} \right) \right\|$$

$$H_{n1} = \text{gain of notch (as } f \rightarrow 0) = \frac{R_g}{R_l} \times H_{OLP}$$

$$\begin{aligned} H_{n2} &= \text{gain of notch} \left( \text{as } f \rightarrow \frac{f_{\text{CLK}}}{2} \right) \\ &= -\frac{R_g}{R_h} \times H_{\text{OHP}} \end{aligned}$$



DS005645-5

\*In Mode 3, the feedback loop is closed around the input summing amplifier; the finite GBW product of this op amp causes a slight Q enhancement. If this is a problem, connect a small capacitor (10 pF–100 pF) across R4 to provide some phase lead.

**FIGURE 11. MODE 3**



## 2.0 Modes of Operation (Continued)

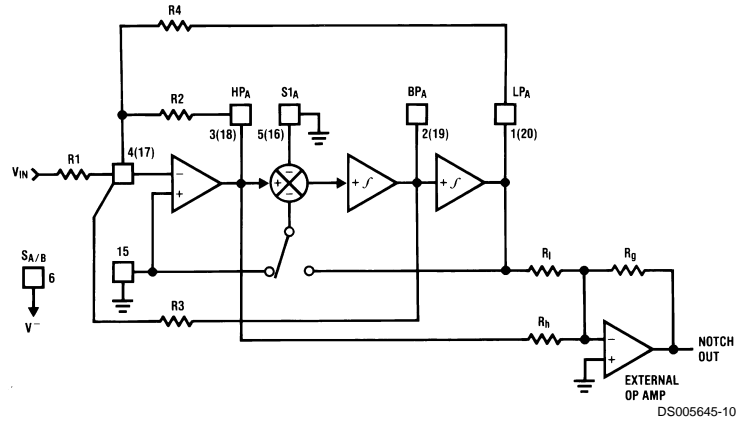


FIGURE 12. MODE 3a

### MODE 4: Allpass, Bandpass, Lowpass Outputs

(See Figure 13)

$f_0$  = center frequency

$$= \frac{f_{CLK}}{100} \text{ or } \frac{f_{CLK}}{50};$$

$f_z^*$  = center frequency of the complex zero  $\approx f_0$

$$Q = \frac{f_0}{BW} = \frac{R3}{R2};$$

$$Q_z = \text{quality factor of complex zero pair} = \frac{R3}{R1}$$

For AP output make  $R1 = R2$

$$H_{OAP}^* = \text{Allpass gain} \left( \text{at } 0 < f < \frac{f_{CLK}}{2} \right) = -\frac{R2}{R1} = -1$$

$H_{OLP}$  = Lowpass gain (as  $f \rightarrow 0$ )

$$= -\left(\frac{R2}{R1} + 1\right) = -2$$

$H_{OBP}$  = Bandpass gain (at  $f = f_0$ )

$$= -\frac{R3}{R2} \left(1 + \frac{R2}{R1}\right) = -2 \left(\frac{R3}{R2}\right)$$

Circuit dynamics:  $H_{OBP} = (H_{OLP}) \times Q = (H_{OAP} + 1)Q$

### MODE 5: Numerator Complex Zeros, BP, LP

(See Figure 14)

$$f_0 = \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 + \frac{R2}{R4}} \times \frac{f_{CLK}}{50}$$

$$f_z = \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{100} \text{ or } \sqrt{1 - \frac{R1}{R4}} \times \frac{f_{CLK}}{50}$$

$$Q = \sqrt{1 + R2/R4} \times \frac{R3}{R2}$$

$$Q_z = \sqrt{1 - R1/R4} \times \frac{R3}{R1}$$

$$H_{0z1} = \text{gain at C.Z. output (as } f \rightarrow 0 \text{ Hz)} \\ = \frac{-R2(R4 - R1)}{R1(R2 + R4)}$$

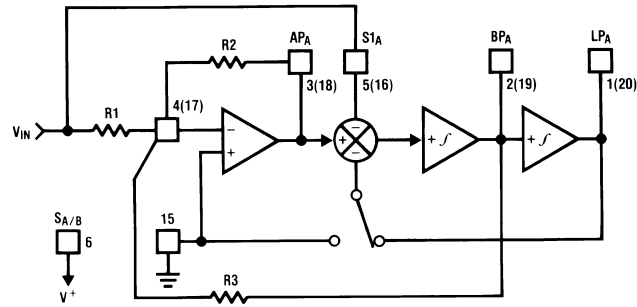
$$H_{0z2} = \text{gain at C.Z. output (as } f \rightarrow \frac{f_{CLK}}{2}) = \frac{-R2}{R1}$$

$$H_{OBP} = -\left(\frac{R2}{R1} + 1\right) \times \frac{R3}{R2}$$

$$H_{OLP} = -\left(\frac{R2 + R1}{R2 + R4}\right) \times \frac{R4}{R1}$$

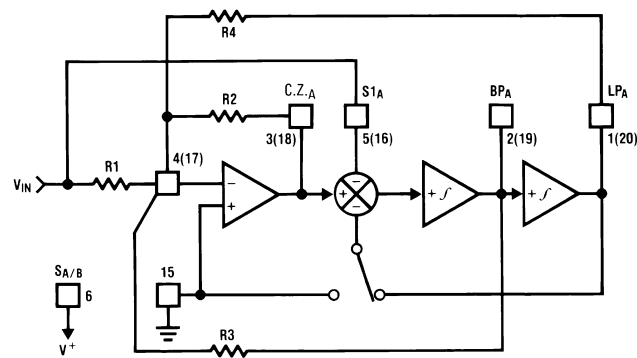
\*Due to the sampled data nature of the filter, a slight mismatch of  $f_z$  and  $f_0$  occurs causing a 0.4 dB peaking around  $f_0$  of the allpass filter amplitude response (which theoretically should be a straight line). If this is unacceptable, Mode 5 is recommended.

## 2.0 Modes of Operation (Continued)



DS005645-6

FIGURE 13. MODE 4



DS005645-15

FIGURE 14. MODE 5

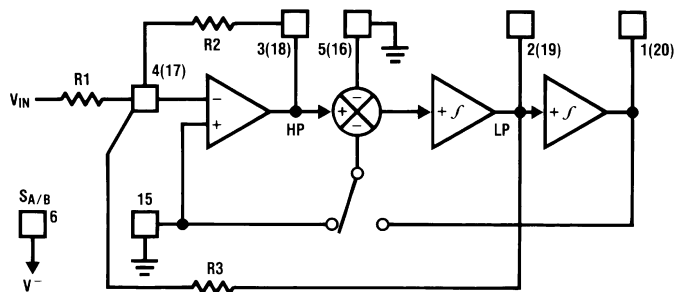
**MODE 6a: Single Pole, HP, LP Filter** (See Figure 15)

$$f_c = \text{cutoff frequency of LP or HP output}$$

$$= \frac{R_2}{R_3} \frac{f_{CLK}}{100} \text{ or } \frac{R_2}{R_3} \frac{f_{CLK}}{50}$$

$$H_{OLP} = -\frac{R_3}{R_1}$$

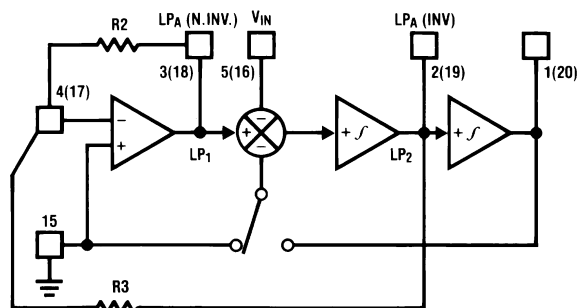
$$H_{OHP} = -\frac{R_2}{R_1}$$



DS005645-16

FIGURE 15. MODE 6a

## 2.0 Modes of Operation (Continued)



DS005645-7

FIGURE 16. MODE 6b

**MODE 6b: Single Pole LP Filter (Inverting and Non-Inverting)** (See Figure 16)

$$f_c = \text{cutoff frequency of LP outputs}$$

$$\cong \frac{R_2 f_{CLK}}{R_3 100} \text{ or } \frac{R_2 f_{CLK}}{R_3 50}$$

$$H_{OLP1} = 1 \text{ (non-inverting)}$$

$$H_{OLP2} = -\frac{R_3}{R_2}$$

**MODE 6c: Single Pole, AP, LP Filter** (See Figure 17)

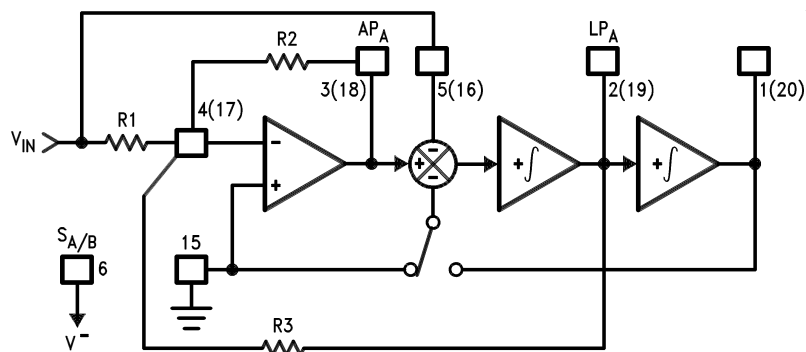
$$f_c = \frac{f_{CLK}}{50} \text{ or } \frac{f_{CLK}}{100}$$

$$H_{OAP} = 1 \text{ (as } f \rightarrow 0)$$

$$H_{OAP} = -1 \text{ (as } f \rightarrow f_{CLK}/2)$$

$$H_{OLP} = -2$$

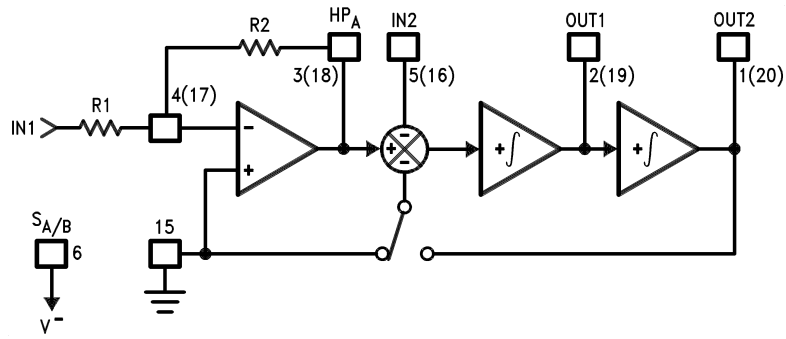
$$R_1 = R_2 = R_3$$



DS005645-17

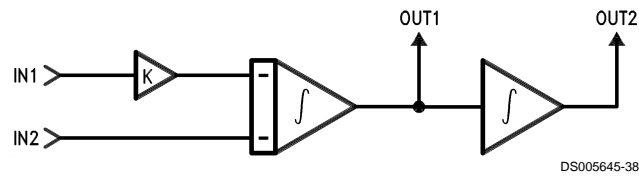
FIGURE 17. MODE 6c

## 2.0 Modes of Operation (Continued)



DS005645-37

**Equivalent Circuit**



DS005645-38

$$K = \frac{R_2}{R_1}$$

$$OUT1 = -\frac{K}{\tau} \int IN1 \, dt - \frac{1}{\tau} \int IN2 \, dt$$

$$OUT2 = \frac{1}{\tau} \int OUT1 \, dt$$

**FIGURE 18. MODE 7**

**MODE 7: Summing Integrator** (See Figure 18)

$$\begin{aligned} \tau &= \text{integrator time constant} \\ &= \frac{16}{f_{CLK}} \text{ or } \frac{8}{f_{CLK}} \end{aligned}$$

## 2.0 Modes of Operation (Continued)

**TABLE 1. Summary of Modes. Realizable filter types (e.g. low-pass) denoted by asterisks.**  
Unless otherwise noted, gains of various filter outputs are inverting and adjustable by resistor ratios.

Mode	BP	LP	HP	N	AP	Number of Resistors	Adjustable $f_{CLK}/f_0$	Notes
1	*	*		*		3	No	
1a	(2) $H_{OBP1} = -Q$ $H_{OBP2} = +1$	$H_{OLP} = +1$				2	No	May need input buffer. Poor dynamics for high Q.
1b	*	*		*		3	No	Useful for high frequency applications.
2	*	*		*		3	Yes (above $f_{CLK}/50$ or $f_{CLK}/100$ )	
3	*	*	*			4	Yes	Universal State-Variable Filter. Best general-purpose mode.
3a	*	*	*	*		7	Yes	As above, but also includes resistor-tuneable notch.
4	*	*			*	3	No	Gives Allpass response with $H_{OAP} = -1$ and $H_{OLP} = -2$ .
5	*	*			*	4	Yes	Gives flatter allpass response than above if $R_1 = R_2 = 0.02R_4$ .
6a		*	*			3	Yes	Single pole.
6b		(2) $H_{OLP1} = +1$ $H_{OLP2} = \frac{-R3}{R2}$				2	Yes	Single pole.
6c		*			*	3	No	Single pole.
7						2	Yes	Summing integrator with adjustable time constant.

## 3.0 Applications Information

The LMF100 is a general purpose dual second-order state variable filter whose center frequency is proportional to the frequency of the square wave applied to the clock input ( $f_{CLK}$ ). The various clocking options are summarized in the following table.

### Clocking Options

Power Supply	Clock Levels	LSh	$V_D^+$
-5V and +5V	TTL (0V to +5V)	0V	+5V
-5V and +5V	CMOS (-5V to +5V)	0V	+5V
0V and 10V	TTL (0V to 5V)	0V	+10V
0V and 10V	CMOS (0V to +10V)	+5V	+10V
-2.5V and +2.5V	CMOS (-2.5V to +2.5V)	0V	+2.5V
0V and 5V	TTL (0V to +5V)	0V	0V

Power Supply	Clock Levels	LSh	$V_D^+$
0V and 5V	CMOS (0V to +5V)	+2.5V	+5V

By connecting pin 12 to the appropriate dc voltage, the filter center frequency,  $f_0$ , can be made equal to either  $f_{CLK}/100$  or  $f_{CLK}/50$ .  $f_0$  can be very accurately set (within  $\pm 0.6\%$ ) by using a crystal clock oscillator, or can be easily varied over a wide frequency range by adjusting the clock frequency. If desired, the  $f_{CLK}/f_0$  ratio can be altered by external resistors as in *Figures 10, 11, 12, 13, 14, 15* and *Figure 16*. This is useful when high-order filters (greater than two) are to be realized by cascading the second-order sections. This allows each stage to be stagger tuned while using only one clock. The filter Q and gain are set by external resistor ratios.

All of the five second-order filter types can be built using either section of the LMF100. These are illustrated in *Figures 1, 2, 3, 4* and *Figure 5* along with their transfer functions and some related equations. *Figure 6* shows the effect of Q on the shapes of these curves.

### 3.0 Applications Information

(Continued)

#### 3.1 DESIGN EXAMPLE

In order to design a filter using the LMF100, we must define the necessary values of three parameters for each second-order section:  $f_0$ , the filter section's center frequency;  $H_0$ , the passband gain; and the filter's  $Q$ . These are determined by the characteristics required of the filter being designed.

As an example, let's assume that a system requires a fourth-order Chebyshev low-pass filter with 1 dB ripple, unity gain at dc, and 1000 Hz cutoff frequency. As the system order is four, it is realizable using both second-order sections of an LMF100. Many filter design texts (and National's Switched Capacitor Filter Handbook) include tables that list the characteristics ( $f_0$  and  $Q$ ) of each of the second-order filter sections needed to synthesize a given higher-order filter. For the Chebyshev filter defined above, such a table yields the following characteristics:

$$f_{0A} = 529 \text{ Hz} \quad Q_A = 0.785$$

$$f_{0B} = 993 \text{ Hz} \quad Q_B = 3.559$$

For unity gain at dc, we also specify:

$$H_{0A} = 1$$

$$H_{0B} = 1$$

The desired clock-to-cutoff-frequency ratio for the overall filter of this example is 100 and a 100 kHz clock signal is available. Note that the required center frequencies for the two second-order sections will not be obtainable with clock-to-center-frequency ratios of 50 or 100. It will be necessary to adjust

$$\frac{f_{CLK}}{f_0}$$

externally. From Table 1, we see that Mode 3 can be used to produce a low-pass filter with resistor-adjustable center frequency.

In most filter designs involving multiple second-order stages, it is best to place the stages with lower  $Q$  values ahead of stages with higher  $Q$ , especially when the higher  $Q$  is greater than 0.707. This is due to the higher relative gain at the center frequency of a higher- $Q$  stage. Placing a stage with lower  $Q$  ahead of a higher- $Q$  stage will provide some attenuation at the center frequency and thus help avoid clipping of signals near this frequency. For this example, stage A has the lower  $Q$  (0.785) so it will be placed ahead of the other stage.

For the first section, we begin the design by choosing a convenient value for the input resistance:  $R_{1A} = 20\text{k}$ . The absolute value of the passband gain  $H_{OLPA}$  is made equal to 1 by choosing  $R_{4A}$  such that:  $R_{4A} = -H_{OLPA}R_{1A} = R_{1A} = 20\text{k}$ . If the 50/100/CL pin is connected to mid-supply for nominal 100:1 clock-to-center-frequency ratio, we find  $R_{2A}$  by:

$$R_{2A} = R_{4A} \frac{f_{0A}^2}{(f_{CLK}/100)^2} = 2 \times 10^4 \times \frac{(529)^2}{(1000)^2} = 5.6\text{k} \text{ and}$$

$$R_{3A} = Q_A \sqrt{R_{2A}R_{4A}} = 0.785 \sqrt{5.6 \times 10^3 \times 2 \times 10^4} = 8.3\text{k}$$

The resistors for the second section are found in a similar fashion:

$$R_{1B} = 20\text{k}$$

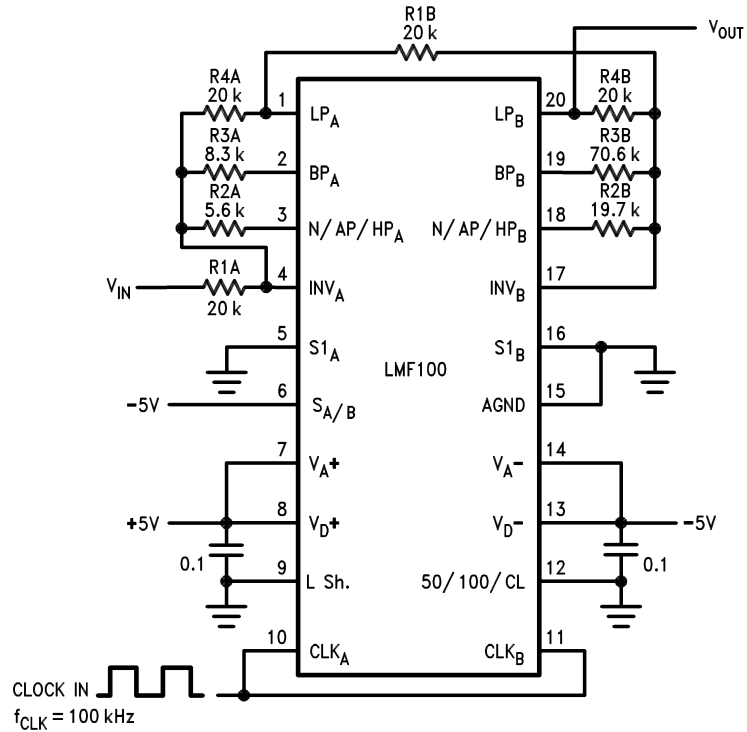
$$R_{4B} = R_{1B} = 20\text{k}$$

$$R_{2B} = R_{4B} \frac{f_{0B}^2}{(f_{CLK}/100)^2} = 20\text{k} \frac{(993)^2}{(1000)^2} = 19.7\text{k}$$

$$R_{3B} = Q_B \sqrt{R_{2B}R_{4B}} = 3.559 \sqrt{1.97 \times 10^4 \times 2 \times 10^4} = 70.6\text{k}$$

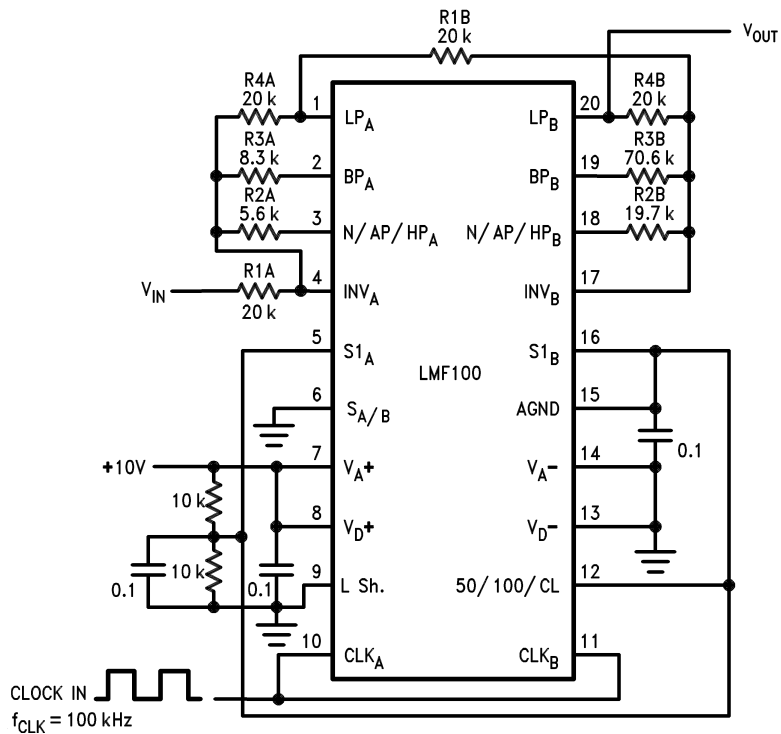
The complete circuit is shown in Figure 19 for split  $\pm 5\text{V}$  power supplies. Supply bypass capacitors are highly recommended.

### 3.0 Applications Information (Continued)



DS005645-30

**FIGURE 19. Fourth-order Chebyshev low-pass filter from example in 3.1.  $\pm 5V$  power supply. 0V–5V TTL or  $\pm 5V$  CMOS logic levels.**



DS005645-31

**FIGURE 20. Fourth-order Chebyshev low-pass filter from example in 3.1. Single  $+10V$  power supply. 0V–5V TTL logic levels. Input signals should be referred to half-supply or applied through a coupling capacitor.**

### 3.0 Applications Information (Continued)

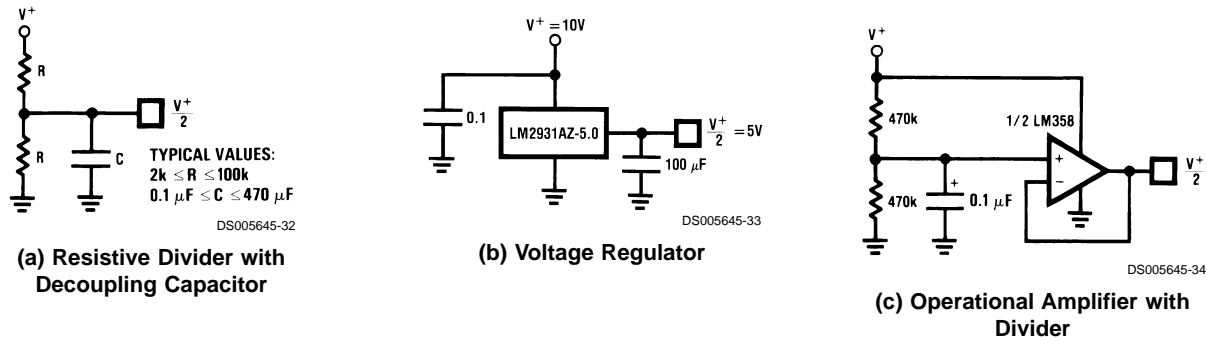


FIGURE 21. Three Ways of Generating  $V^+/2$  for Single-Supply Operation

#### 3.2 SINGLE SUPPLY OPERATION

The LMF100 can also operate with a single-ended power supply. Figure 20 shows the example filter with a single-ended power supply.  $V_{A+}$  and  $V_{D+}$  are again connected to the positive power supply (4 to 15 volts), and  $V_{A-}$  and  $V_{D-}$  are connected to ground. The  $A_{GND}$  pin must be tied to  $V^+/2$  for single supply operation. This half-supply point should be very “clean”, as any noise appearing on it will be treated as an input to the filter. It can be derived from the supply voltage with a pair of resistors and a bypass capacitor (Figure 21a), or a low-impedance half-supply voltage can be made using a three-terminal voltage regulator or an operational amplifier (Figure 21b and Figure 21c). The passive resistor divider with a bypass capacitor is sufficient for many applications, provided that the time constant is long enough to reject any power supply noise. It is also important that the half-supply reference present a low impedance to the clock frequency, so at very low clock frequencies the regulator or op-amp approaches may be preferable because they will require smaller capacitors to filter the clock frequency. The main power supply voltage should be clean (preferably regulated) and bypassed with 0.1  $\mu$ F.

#### 3.3 DYNAMIC CONSIDERATIONS

The maximum signal handling capability of the LMF100, like that of any active filter, is limited by the power supply voltages used. The amplifiers in the LMF100 are able to swing to within about 1 volt of the supplies, so the input signals must be kept small enough that none of the outputs will exceed these limits. If the LMF100 is operating on  $\pm 5$  volts, for example, the outputs will clip at about  $8V_{p-p}$ . The maximum input voltage multiplied by the filter gain should therefore be less than  $8V_{p-p}$ .

Note that if the filter  $Q$  is high, the gain at the lowpass or highpass outputs will be much greater than the nominal filter gain (Figure 6). As an example, a lowpass filter with a  $Q$  of 10 will have a 20 dB peak in its amplitude response at  $f_0$ . If the nominal gain of the filter ( $H_{OLP}$ ) is equal to 1, the gain at  $f_0$  will be 10. The maximum input signal at  $f_0$  must therefore be less than  $800 mV_{p-p}$  when the circuit is operated on  $\pm 5$  volt supplies.

Also note that one output can have a reasonable small voltage on it while another is saturated. This is most likely for a circuit such as the notch in Mode 1 (Figure 7). The notch output will be very small at  $f_0$ , so it might appear safe to apply a large signal to the input. However, the bandpass will have its maximum gain at  $f_0$  and can clip if overdriven. If one output clips, the performance at the other outputs will be degraded, so avoid overdriving any filter section, even ones whose out-

puts are not being directly used. Accompanying Figures 7, 8, 9, 10, 11, 12, 13, 14, 15, 16 and Figure 17 are equations labeled “circuit dynamics”, which relate the  $Q$  and the gains at the various outputs. These should be consulted to determine peak circuit gains and maximum allowable signals for a given application.

#### 3.4 OFFSET VOLTAGE

The LMF100's switched capacitor integrators have a slightly higher input offset voltage than found in a typical continuous time active filter integrator. Because of National's new LCMOS process and new design techniques the internal offsets have been minimized, compared to the industry standard MF10. Figure 22 shows an equivalent circuit of the LMF100 from which the output dc offsets can be calculated. Typical values for these offsets with  $S_{A/B}$  tied to  $V^+$  are:

$$V_{OS1} = \text{opamp offset} = \pm 5 \text{ mV}$$

$$V_{OS2} = \pm 30 \text{ mV at } 50:1 \text{ or } 100:1$$

$$V_{OS3} = \pm 15 \text{ mV at } 50:1 \text{ or } 100:1$$

When  $S_{A/B}$  is tied to  $V^-$ ,  $V_{OS2}$  will approximately halve. The dc offset at the BP output is equal to the input offset of the lowpass integrator ( $V_{OS3}$ ). The offsets at the other outputs depend on the mode of operation and the resistor ratios, as described in the following expressions.

##### Mode 1 and Mode 4

$$V_{OS(N)} = V_{OS1} \left( \frac{1}{Q} + 1 + \|H_{OLP}\| \right) - \frac{V_{OS3}}{Q}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

##### Mode 1a

$$V_{OS(N.INV.BP)} = \left( 1 + \frac{1}{Q} \right) V_{OS1} - \frac{V_{OS3}}{Q}$$

$$V_{OS(INV.BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N.INV.BP)} - V_{OS2}$$



### 3.0 Applications Information

(Continued)

#### Mode 1b

$$V_{OS(N)} = V_{OS1} \left( 1 + \frac{R_2}{R_3} + \frac{R_2}{R_1} \right) - \frac{R_2}{R_3} V_{OS3}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = \frac{V_{OS(N)}}{2} - \frac{V_{OS2}}{2}$$

#### Mode 2 and Mode 5

$$V_{OS(N)} = \left( \frac{R_2}{R_p} + 1 \right) V_{OS1} \times \frac{1}{1 + R_2/R_4} + V_{OS2} \frac{1}{1 + R_4/R_2} - \frac{V_{OS3}}{Q\sqrt{1 + R_2/R_4}}$$

$$R_p = R_1 \parallel R_3 \parallel R_4$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS(N)} - V_{OS2}$$

#### Mode 3

$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(BP)} = V_{OS3}$$

$$V_{OS(LP)} = V_{OS1} \left[ 1 + \frac{R_4}{R_p} \right] - V_{OS2} \left( \frac{R_4}{R_2} \right) - V_{OS3} \left( \frac{R_4}{R_3} \right)$$

$$R_p = R_1 \parallel R_2 \parallel R_3$$

#### Mode 6a and 6c

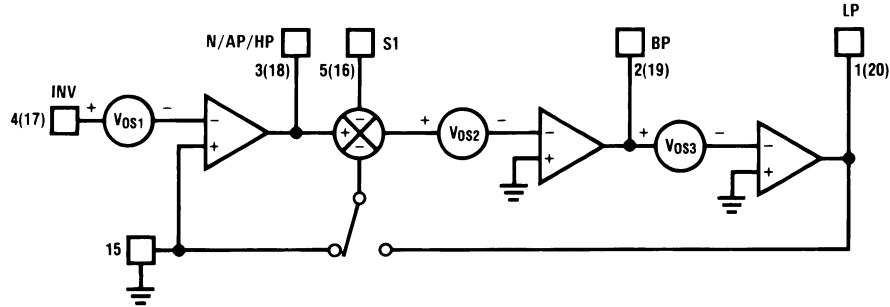
$$V_{OS(HP)} = V_{OS2}$$

$$V_{OS(LP)} = V_{OS1} \left( 1 + \frac{R_3}{R_2} + \frac{R_3}{R_1} \right) - \frac{R_3}{R_2} V_{OS2}$$

#### Mode 6b

$$V_{OS(LP (N.INV))} = V_{OS2}$$

$$V_{OS(LP (INV))} = V_{OS1} \left( 1 + \frac{R_3}{R_2} \right) - \frac{R_3}{R_2} V_{OS2}$$



DS005645-12

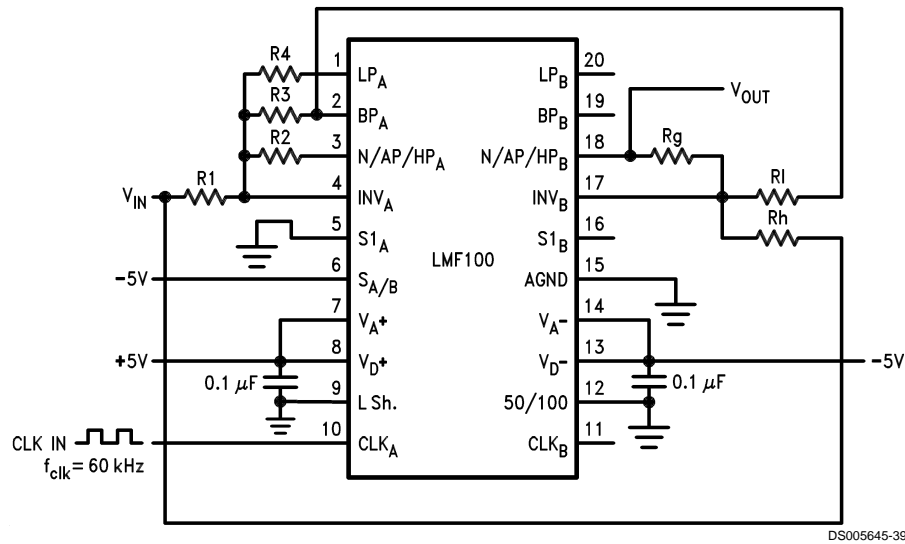
FIGURE 22. Offset Voltage Sources

In many applications, the outputs are ac coupled and dc offsets are not bothersome unless large signals are applied to the filter input. However, larger offset voltages will cause clipping to occur at lower ac signal levels, and clipping at any of the outputs will cause gain nonlinearities and will change  $f_0$  and  $Q$ . When operating in Mode 3, offsets can become excessively large if  $R_2$  and  $R_4$  are used to make  $f_{CLK}/f_0$  significantly higher than the nominal value, especially if  $Q$  is also high.

For example, *Figure 23* shows a second-order 60 Hz notch filter. This circuit yields a notch with about 40 dB of attenuation at 60 Hz. A notch is formed by subtracting the bandpass output of a mode 3 configuration from the input using the un-

used side B opamp. The  $Q$  is 10 and the gain is 1 V/V in the passband. However,  $f_{CLK}/f_0 = 1000$  to allow for a wide input spectrum. This means that for pin 12 tied to ground (100:1 mode),  $R_4/R_2 = 100$ . The offset voltage at the lowpass output (LP) will be about 3V. However, this is an extreme case and the resistor ratio is usually much smaller. Where necessary, the offset voltage can be adjusted by using the circuit of *Figure 24*. This allows adjustment of  $V_{OS1}$ , which will have varying effects on the different outputs as described in the above equations. Some outputs cannot be adjusted this way in some modes, however ( $V_{OS(BP)}$  in modes 1a and 3, for example).

### 3.0 Applications Information (Continued)



$R1 = 100 \text{ k}\Omega$   
 $R2 = 1 \text{ k}\Omega$   
 $R3 = 100 \text{ k}\Omega$   
 $R4 = 100 \text{ k}\Omega$   
 $Rg = 10 \text{ k}\Omega$   
 $Rl = 10 \text{ k}\Omega$   
 $Rh = 10 \text{ k}\Omega$

FIGURE 23. Second-Order Notch Filter

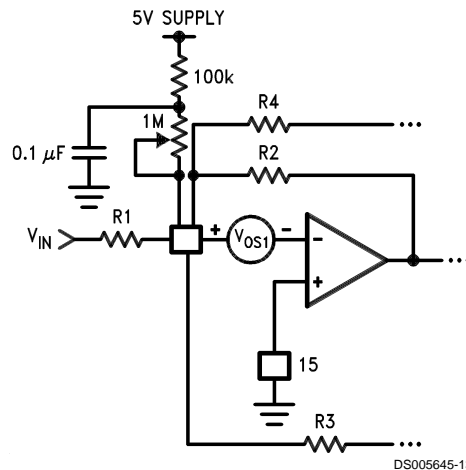


FIGURE 24. Method for Trimming  $V_{Os}$

### 3.5 SAMPLED DATA SYSTEM CONSIDERATIONS

The LMF100 is a sampled data filter, and as such, differs in many ways from conventional continuous-time filters. An important characteristic of sampled-data systems is their effect on signals at frequencies greater than one-half the sampling frequency. (The LMF100's sampling frequency is the same as its clock frequency.) If a signal with a frequency greater than one-half the sampling frequency is applied to the input of a sampled data system, it will be "reflected" to a frequency less than one-half the sampling frequency. Thus, an input signal whose frequency is  $f_s/2 + 100 \text{ Hz}$  will cause the system to respond as though the input frequency was  $f_s/2 - 100 \text{ Hz}$ . This phenomenon is known as "aliasing", and can be reduced or eliminated by limiting the input signal

spectrum to less than  $f_s/2$ . This may in some cases require the use of a bandwidth-limiting filter ahead of the LMF100 to limit the input spectrum. However, since the clock frequency is much higher than the center frequency, this will often not be necessary.

Another characteristic of sampled-data circuits is that the output signal changes amplitude once every sampling period, resulting in "steps" in the output voltage which occur at the clock rate (Figure 25). If necessary, these can be "smoothed" with a simple R-C low-pass filter at the LMF100 output.

The ratio of  $f_{CLK}$  to  $f_c$  (normally either 50:1 or 100:1) will also affect performance. A ratio of 100:1 will reduce any aliasing problems and is usually recommended for wide-band input

### 3.0 Applications Information

(Continued)

signals. In noise-sensitive applications, a ratio of 100:1 will result in 3 dB lower output noise for the same filter configuration.

The accuracy of the  $f_{\text{CLK}}/f_0$  ratio is dependent on the value of Q. This is illustrated in the curves under the heading "Typical

Performance Characteristics". As Q is changed, the true value of the ratio changes as well. Unless the Q is low, the error in  $f_{\text{CLK}}/f_0$  will be small. If the error is too large for a specific application, use a mode that allows adjustment of the ratio with external resistors.

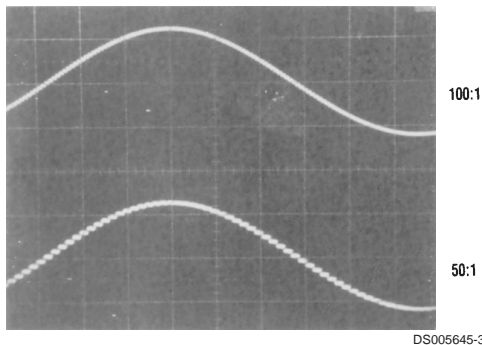
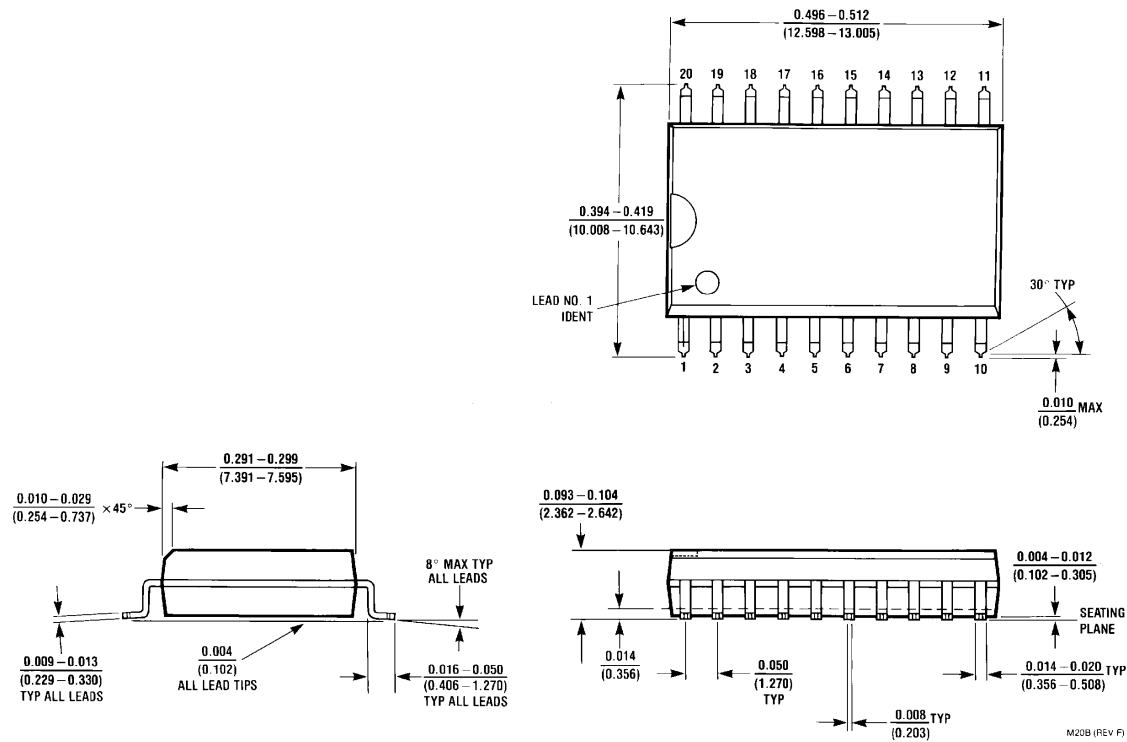
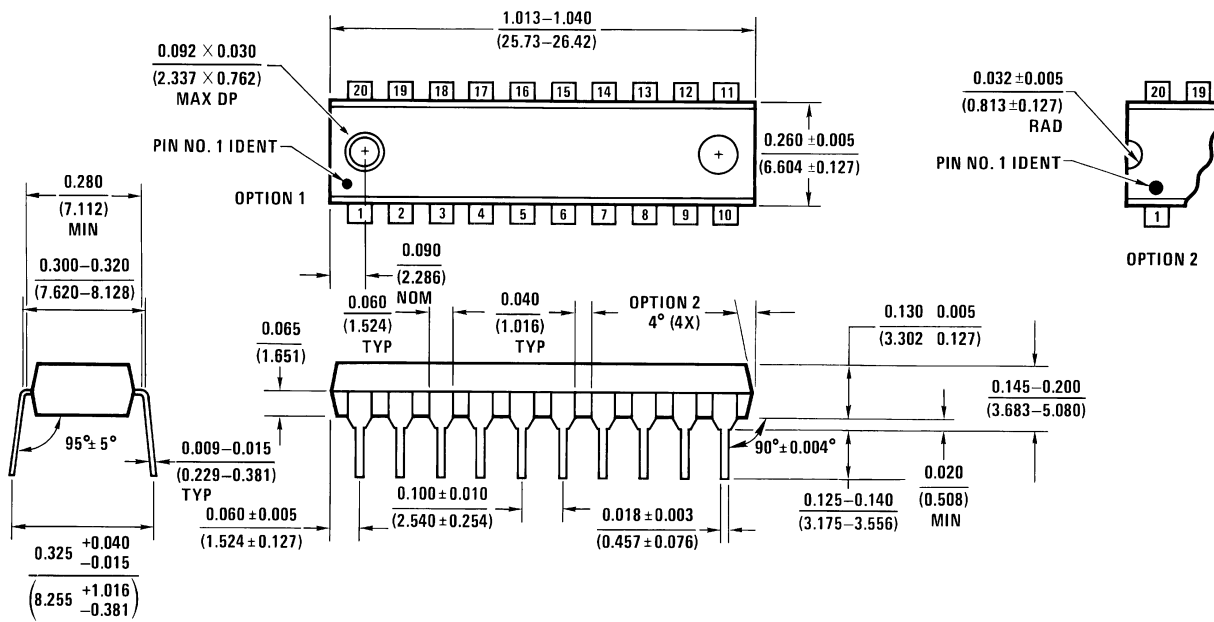


FIGURE 25. The Sampled-Data Output Waveform

**Physical Dimensions** inches (millimeters) unless otherwise noted

**Small Outline Package**  
**Order Number LMF100CIWM**  
**NS Package Number M20B**



**Molded Dual-In-Line Package (N)**  
**Order Number LMF100CCN**  
**NS Package Number N20A**

## Notes

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com  
www.national.com

**National Semiconductor Europe**  
Fax: +49 (0) 180-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: ap.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
RFID	<a href="http://www.ti-rfid.com">www.ti-rfid.com</a>
OMAP Mobile Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
Transportation and Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Video and Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>

TI E2E Community Home Page

[e2e.ti.com](http://e2e.ti.com)

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2011, Texas Instruments Incorporated

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)

[www.lifeelectronics.ru](http://www.lifeelectronics.ru)