

1.3GHz to 2.3GHz High Dynamic Range Downconverting Mixer

FEATURES

- Conversion Gain: 7.8dB at 1950MHz
- IIP3: 26.4dBm at 1950MHz
- Noise Figure: 9.6dB at 1950MHz
- 16dB NF Under +5dBm Blocking
- High Input P1dB
- 3.3V Supply, 630mW Power Consumption
- Shutdown Pin
- 50Ω Single-Ended RF and LO Inputs
- LO Inputs 50Ω Matched when Shutdown
- High Isolation LO Switch
- 0dBm LO Drive Level
- High LO-RF and LO-IF Isolation
- Small Solution Size
- 20-Lead (5mm × 5mm) QFN package

APPLICATIONS

- Wireless Infrastructure Receivers (LTE, W-CDMA, TD-SCDMA, UMTS, GSM1800)
- Point-To-Point Microwave Links
- High Dynamic Range Downmixer Applications

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DESCRIPTION

The LTC[®]5541 is part of a family of high dynamic range passive, high gain downconverting mixers covering the 600MHz to 4GHz frequency range. **The LTC5541 is optimized for 1.3GHz to 2.3GHz RF applications. The LO frequency must fall within the 1.4GHz to 2.0GHz range for optimum performance.** A typical application is a LTE or W-CDMA receiver with a 1.7GHz to 2.2GHz RF input and low-side LO.

The LTC5541 is designed for 3.3V operation, however; the IF amplifier can be powered by 5V for the highest P1dB. An integrated SPDT LO switch with fast switching accepts two active LO signals, while providing high isolation.

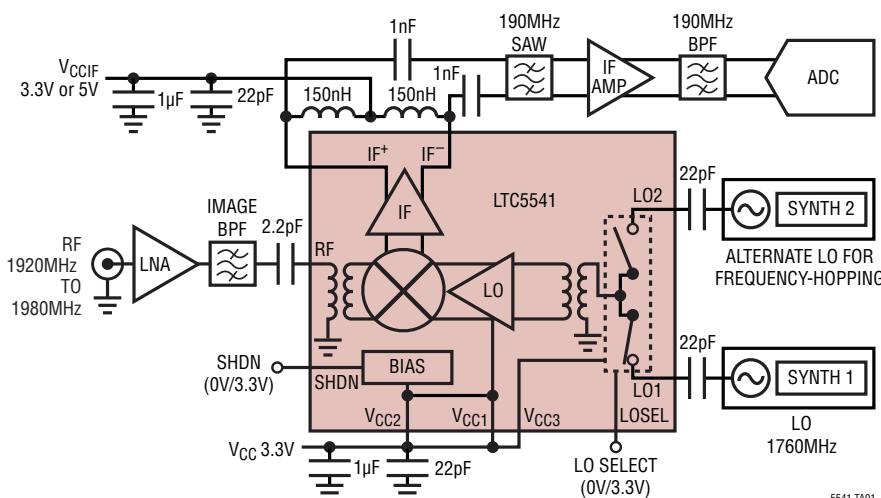
The LTC5541's high conversion gain and high dynamic range enable the use of lossy IF filters in high-selectivity receiver designs, while minimizing the total solution cost, board space and system-level variation.

High Dynamic Range Downconverting Mixer Family

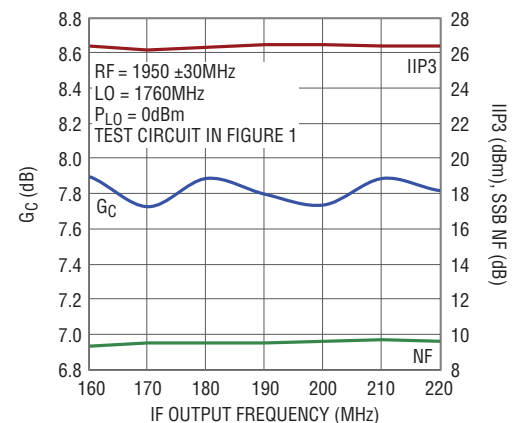
PART#	RF RANGE	LO RANGE
LTC5540	600MHz – 1.3GHz	700MHz – 1.2GHz
LTC5541	1.3GHz – 2.3GHz	1.4GHz – 2.0GHz
LTC5542	1.6GHz – 2.7GHz	1.7GHz – 2.5GHz
LTC5543	2.3GHz – 4GHz	2.4GHz – 3.6GHz

TYPICAL APPLICATION

Wideband Receiver



Wideband Conversion Gain, IIP3 and NF vs IF Output Frequency



5541 TA01

5541 TA02

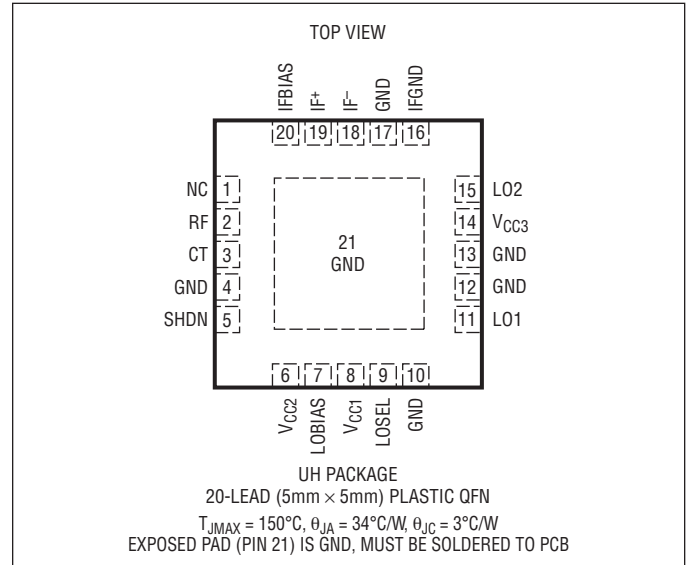
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ABSOLUTE MAXIMUM RATINGS

(Note 1)

Mixer Supply Voltage (V_{CC1} , V_{CC2}).....	3.8V
LO Switch Supply Voltage (V_{CC3}).....	3.8V
IF Supply Voltage (IF^+ , IF^-)	5.5V
Shutdown Voltage (SHDN).....	-0.3V to $V_{CC} + 0.3V$
LO Select Voltage (LOSEL).....	-0.3V to $V_{CC} + 0.3V$
LO1, LO2 Input Power (1GHz to 3GHz).....	9dBm
LO1, LO2 Input DC Voltage	$\pm 0.5V$
RF Input Power (1GHz to 3GHz)	15dBm
RF Input DC Voltage.....	$\pm 0.1V$
Operating Temperature Range	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Junction Temperature (T_J)	150°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5541IUH#PBF	LTC5541IUH#TRPBF	5541	20-Lead (5mm x 5mm) Plastic QFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V$, $V_{CCIF} = 3.3V$, SHDN = Low, $T_A = 25^{\circ}C$, $P_{LO} = 0dBm$, unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LO Input Frequency Range			1400 to 2000		MHz
RF Input Frequency Range	Low-Side LO		1600 to 2300		MHz
	High-Side LO		1300 to 1800		MHz
IF Output Frequency Range	Requires External Matching		5 to 500		MHz
RF Input Return Loss	$Z_0 = 50\Omega$, 1300MHz to 2300MHz		>12		dB
LO Input Return Loss	$Z_0 = 50\Omega$, 1400MHz to 2000MHz		>12		dB
IF Output Return Loss	Requires External Matching		>12		dB
LO Input Power	$f_{LO} = 1400MHz$ to 2000MHz	-4	0	6	dBm
LO to RF Leakage	$f_{LO} = 1400MHz$ to 2000MHz		<-32		dBm
LO to IF Leakage	$f_{LO} = 1400MHz$ to 2000MHz		<-31		dBm
LO Switch Isolation	LO1 Selected, 1400MHz < f_{LO} < 2000MHz		52		dB
	LO2 Selected, 1400MHz < f_{LO} < 2000MHz		50		dB
RF to LO Isolation	$f_{RF} = 1300MHz$ to 2300MHz		>52		dB
RF to IF Isolation	$f_{RF} = 1300MHz$ to 2300MHz		>33		dB

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AC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V$, $V_{CCIF} = 3.3V$, $SHDN = Low$, $T_A = 25^\circ C$, $P_{LO} = 0dBm$, $P_{RF} = -3dBm$ ($\Delta f = 2MHz$ for two-tone IIP3 tests), unless otherwise noted. Test circuit shown in Figure 1. (Notes 2, 3, 4)

Low-Side LO Downmixer Application: $RF = 1700$ to $2200MHz$, $IF = 190MHz$, $f_{LO} = f_{RF} - f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 1750MHz RF = 1950MHz RF = 2150MHz	6.5	8.6 7.8 7.6		dB
Conversion Gain Flatness	RF = 1950 \pm 30MHz, LO = 1760MHz, IF = 190 \pm 30MHz		\pm 0.1		dB
Conversion Gain vs Temperature	$T_A = -40^\circ C$ to $+85^\circ C$, RF = 1950MHz		-0.006		dB/ $^\circ C$
Input 3 rd Order Intercept	RF = 1750MHz RF = 1950MHz RF = 2150MHz	24.0	25.5 26.4 25.5		dBm
SSB Noise Figure	RF = 1750MHz RF = 1950MHz RF = 2150MHz		9.2 9.6 10.6	11.7	dB
SSB Noise Figure Under Blocking	$f_{RF} = 1950MHz$, $f_{LO} = 1760MHz$, $f_{BLOCK} = 2050MHz$, $P_{BLOCK} = 5dBm$		16		dB
2RF – 2LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/2$)	$f_{RF} = 1855MHz$ at $-10dBm$, $f_{LO} = 1760MHz$, $f_{IF} = 190MHz$		-67		dBc
3RF – 3LO Output Spurious Product ($f_{RF} = f_{LO} + f_{IF}/3$)	$f_{RF} = 1823.33MHz$ at $-10dBm$, $f_{LO} = 1760MHz$, $f_{IF} = 190MHz$		-73		dBc
Input 1dB Compression	RF = 1950MHz, $V_{CCIF} = 3.3V$ RF = 1950MHz, $V_{CCIF} = 5V$		11.3 14.6		dBm

High-Side LO Downmixer Application: $RF = 1300$ - $1800MHz$, $IF = 190MHz$, $f_{LO} = f_{RF} + f_{IF}$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Conversion Gain	RF = 1450MHz RF = 1600MHz RF = 1750MHz		8.9 8.4 8.0		dB
Conversion Gain Flatness	RF = 1600MHz \pm 30MHz, LO = 1790MHz, IF = 190 \pm 30MHz		\pm 0.1		dB
Conversion Gain vs Temperature	$T_A = -40^\circ C$ to $85^\circ C$, RF = 1600MHz		-0.006		dB/ $^\circ C$
Input 3 rd Order Intercept	RF = 1450MHz RF = 1600MHz RF = 1750MHz		24.5 24.6 24.3		dBm
SSB Noise Figure	RF = 1450MHz RF = 1600MHz RF = 1750MHz		9.5 9.9 9.9		dB
SSB Noise Figure Under Blocking	$f_{RF} = 1600MHz$, $f_{LO} = 1790MHz$, $f_{IF} = 190MHz$ $f_{BLOCK} = 1500MHz$, $P_{BLOCK} = 5dBm$		18		dB
2LO – 2RF Output Spurious Product ($f_{RF} = f_{LO} - f_{IF}/2$)	$f_{RF} = 1695MHz$ at $-10dBm$, $f_{LO} = 1790MHz$ $f_{IF} = 190MHz$		-69		dBc
3LO – 3RF Output Spurious Product ($f_{RF} = f_{LO} - f_{IF}/3$)	$f_{RF} = 1726.67MHz$ at $-10dBm$, $f_{LO} = 1790MHz$ $f_{IF} = 190MHz$		-74		dBc
Input 1dB Compression	RF = 1750MHz, $V_{CCIF} = 3.3V$ RF = 1750MHz, $V_{CCIF} = 5V$		11.1 14.4		dBm

DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3V$, $V_{CCIF} = 3.3V$, SHDN = Low, $T_A = 25^\circ C$, unless otherwise noted. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Requirements (V_{CC}, V_{CCIF})					
V_{CC} Supply Voltage (Pins 6, 8 and 14)		3.1	3.3	3.5	V
V_{CCIF} Supply Voltage (Pins 18 and 19)		3.1	3.3	5.3	V
V_{CC} Supply Current (Pins 6 + 8 + 14)			92	108	mA
V_{CCIF} Supply Current (Pins 18 + 19)			100	120	
Total Supply Current ($V_{CC} + V_{CCIF}$)			192	228	
Total Supply Current – Shutdown	SHDN = High			500	μA
Shutdown Logic Input (SHDN) Low = On, High = Off					
SHDN Input High Voltage (Off)		3			V
SHDN Input Low Voltage (On)				0.3	V
SHDN Input Current	$-0.3V$ to $V_{CC} + 0.3V$	-20		30	μA
Turn On Time			1		μs
Turn Off Time			1.5		μs
LO Select Logic Input (LOSEL) Low = LO1 Selected, High = LO2 Selected					
LOSEL Input High Voltage		3			V
LOSEL Input Low Voltage				0.3	V
LOSEL Input Current	$-0.3V$ to $V_{CC} + 0.3V$	-20		30	μA
LO Switching Time			50		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

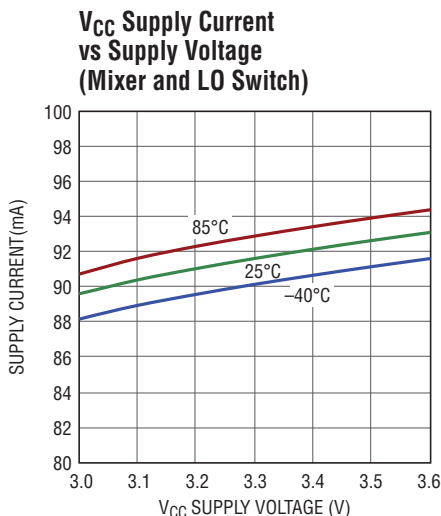
Note 2: The LTC5541 is guaranteed functional over the operating temperature range from $-40^\circ C$ to $85^\circ C$.

Note 3: SSB Noise Figure measurements performed with a small-signal noise source, bandpass filter and 6dB matching pad on RF input, bandpass filter and 6dB matching pad on the LO input, and no other RF signals applied.

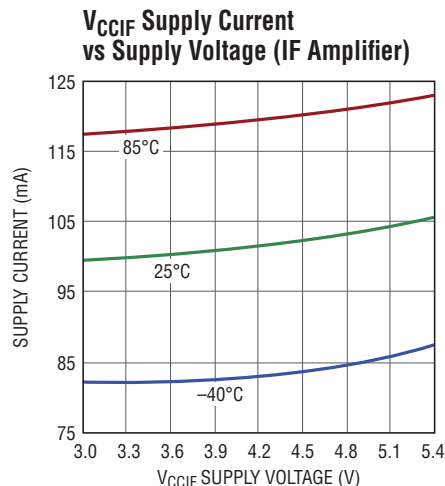
Note 4: LO switch isolation is measured at the IF output port at the IF frequency with f_{LO1} and f_{LO2} offset by 2MHz.

TYPICAL DC PERFORMANCE CHARACTERISTICS

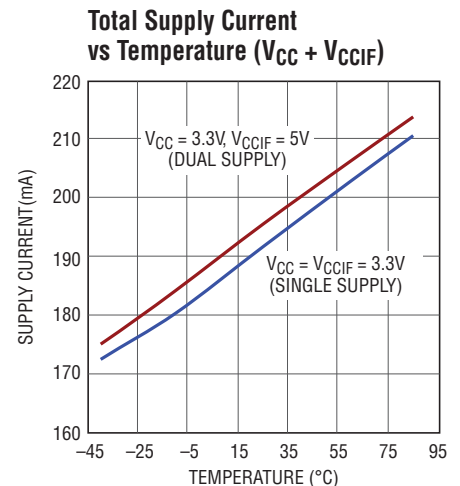
SHDN = Low, Test circuit shown in Figure 1.



5541 G01



5541 G02

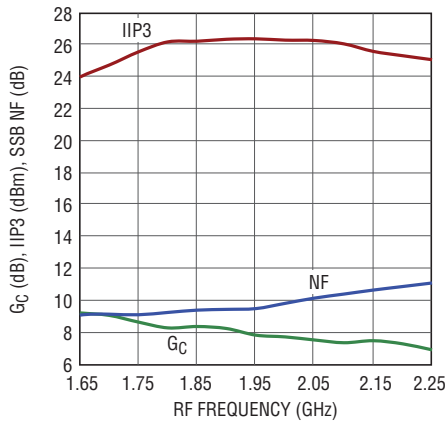


5541 G03

TYPICAL AC PERFORMANCE CHARACTERISTICS Low-Side LO

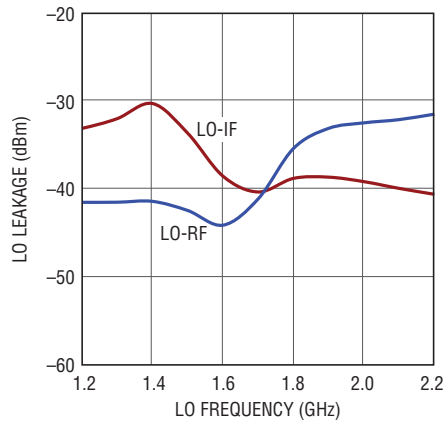
$V_{CC} = 3.3V$, $V_{CCIF} = 3.3V$, SHDN = Low, $T_A = 25^\circ C$, $P_{LO} = 0dBm$, $P_{RF} = -3dBm$ (-3dBm/tone for two-tone IIP3 tests, $\Delta f = 2MHz$), $IF = 190MHz$, unless otherwise noted. Test circuit shown in Figure 1.

Conversion Gain, IIP3 and NF vs RF Frequency



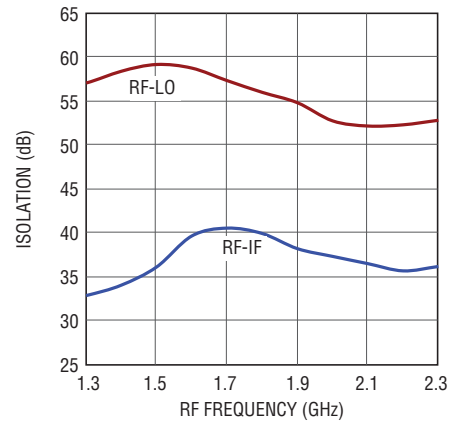
5541 G04

LO Leakage vs LO Frequency



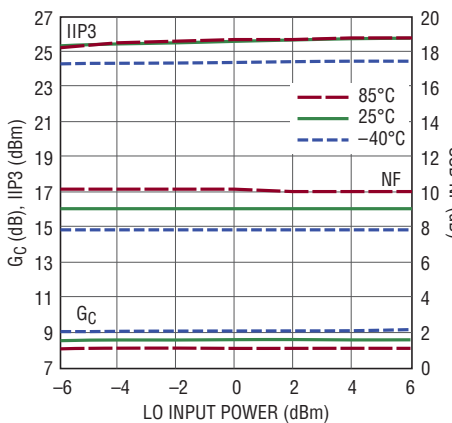
5541 G05

RF Isolation vs RF Frequency



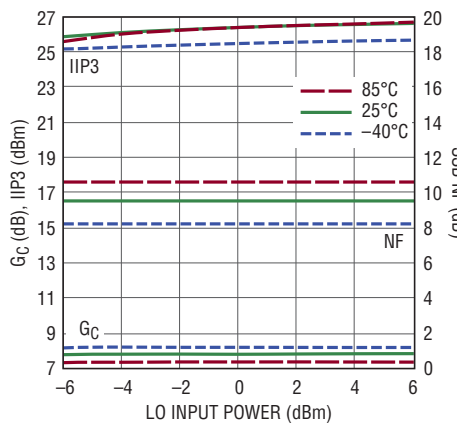
5541 G06

1750MHz Conversion Gain, IIP3 and NF vs LO Power



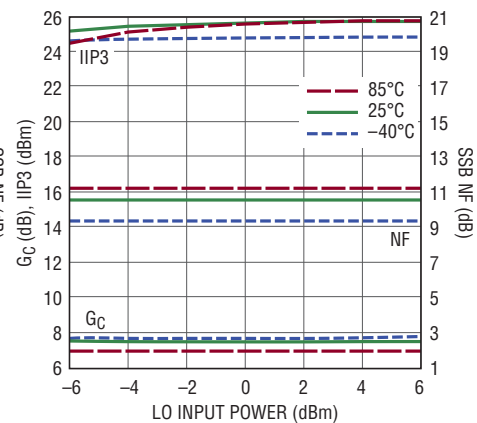
5541 G07

1950MHz Conversion Gain, IIP3 and NF vs LO Power



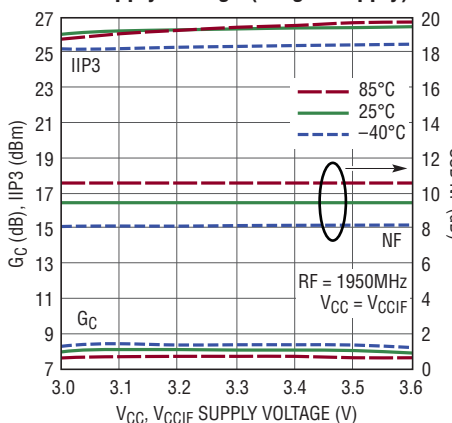
5541 G08

2150MHz Conversion Gain, IIP3 and NF vs LO Power



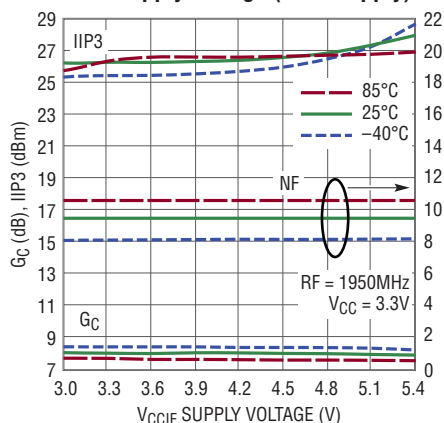
5541 G09

Conversion Gain, IIP3 and NF vs Supply Voltage (Single Supply)



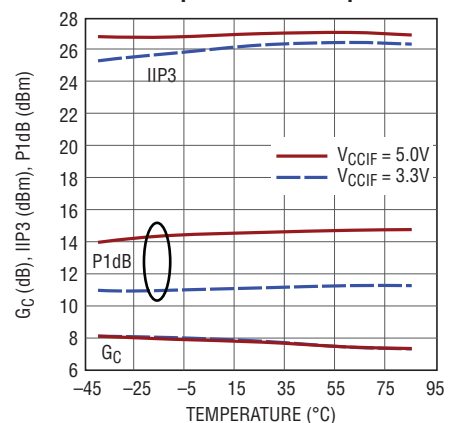
5541 G10

Conversion Gain, IIP3 and NF vs IF Supply Voltage (Dual Supply)



5541 G11

1950MHz Conversion Gain, IIP3 and RF Input P1dB vs Temperature



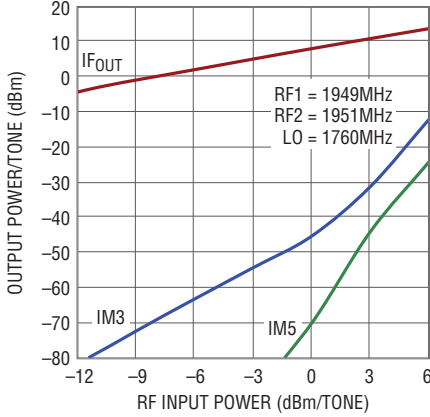
5541 G12

5541f

TYPICAL AC PERFORMANCE CHARACTERISTICS Low-Side LO (continued)

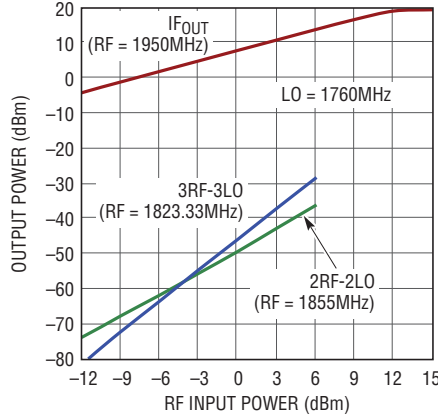
$V_{CC} = 3.3V$, $V_{CCIF} = 3.3V$, SHDN = Low, $T_A = 25^\circ C$, $P_{LO} = 0dBm$, $P_{RF} = -3dBm$ (-3dBm/tone for two-tone IIP3 tests, $\Delta f = 2MHz$), $IF = 190MHz$, unless otherwise noted. Test circuit shown in Figure 1.

2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



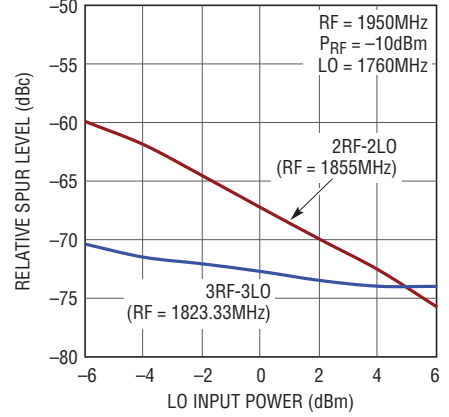
5541 G13

Single-Tone IF Output Power, 2 x 2 and 3 x 3 Spurs vs RF Input Power



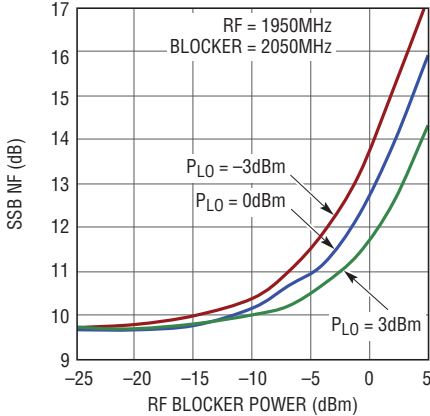
5541 G14

2 x 2 and 3 x 3 Spur Suppression vs LO Power



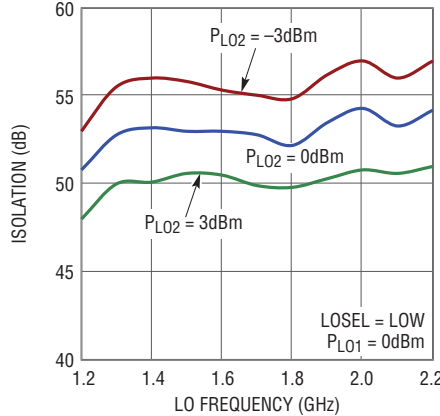
5541 G15

SSB Noise Figure vs RF Blocker Level



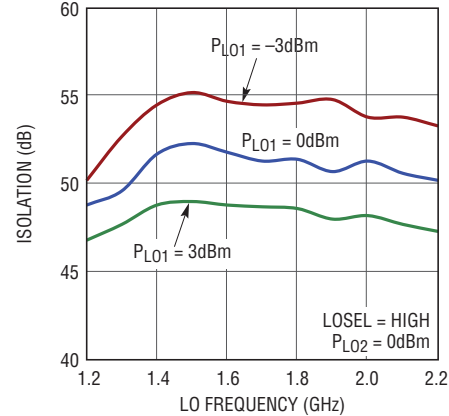
5541 G16

LO Switch Isolation vs LO Frequency—LO1 Selected



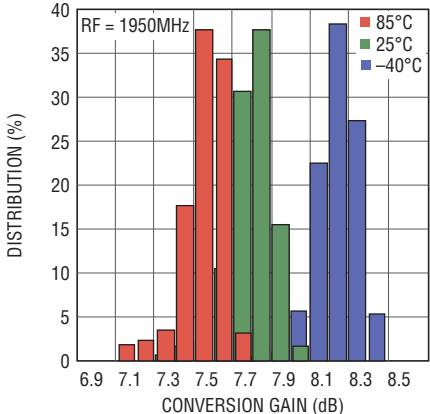
5541 G17

LO Switch Isolation vs LO Frequency—LO2 Selected



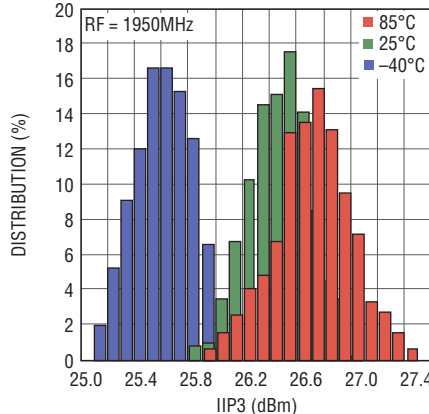
5541 G18

Conversion Gain Distribution



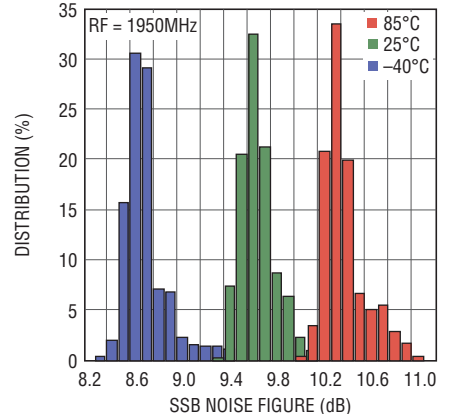
5541 G18a

IIP3 Distribution



5541 G18b

SSB Noise Figure Distribution

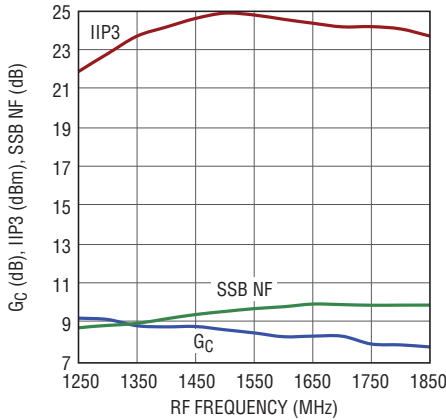


5541 G18c

TYPICAL AC PERFORMANCE CHARACTERISTICS High-Side LO

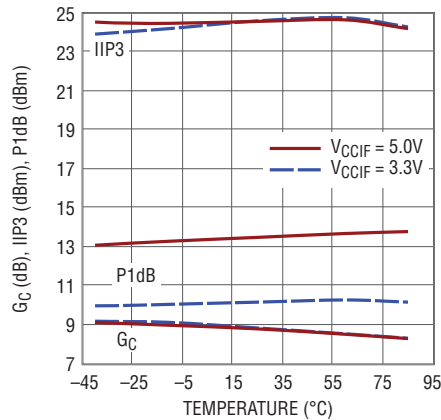
$V_{CC} = 3.3V$, $V_{CCIF} = 3.3V$, SHDN = Low, $T_A = 25^\circ C$, $P_{LO} = 0dBm$, $P_{RF} = -3dBm$ (-3dBm/tone for two-tone IIP3 tests, $\Delta f = 2MHz$), $IF = 190MHz$, unless otherwise noted. Test circuit shown in Figure 1.

Conversion Gain, IIP3 and NF vs RF Frequency



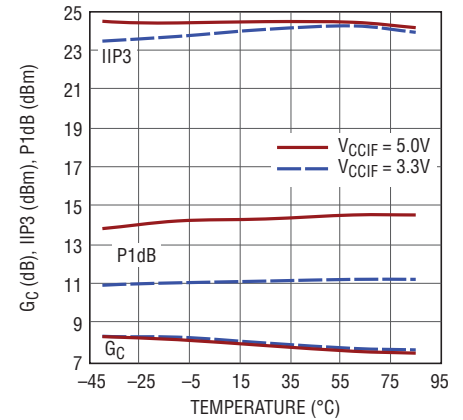
5541 G19

1450MHz Conversion Gain, IIP3 and RF Input P1dB vs Temperature



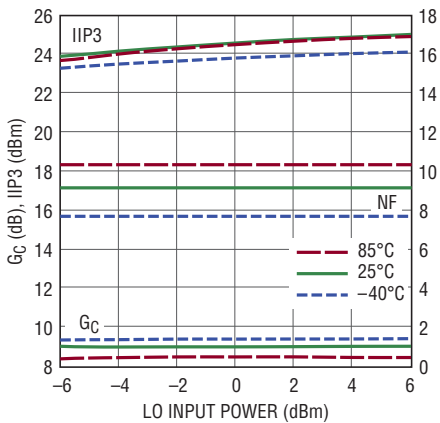
5541 G20

1750MHz Conversion Gain, IIP3 and RF Input P1dB vs Temperature



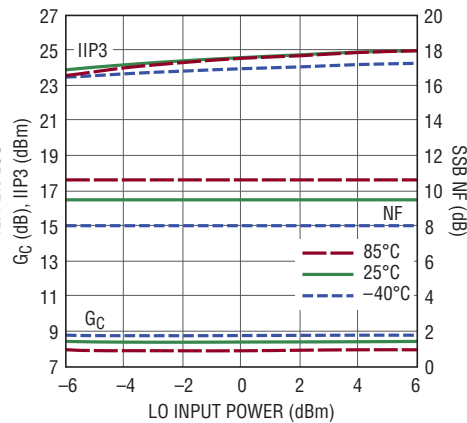
5541 G21

1450MHz Conversion Gain, IIP3 and NF vs LO Power



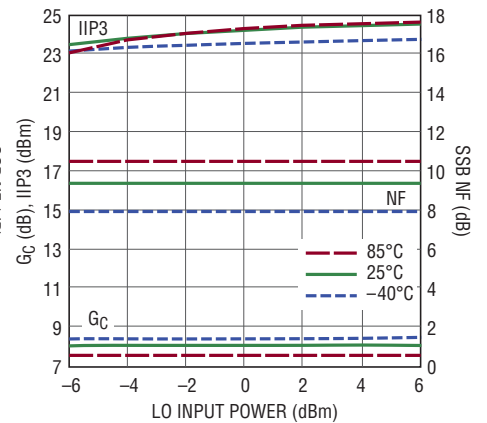
5541 G22

1600MHz Conversion Gain, IIP3 and NF vs LO Power



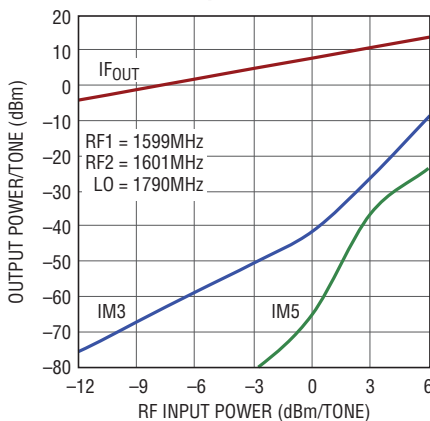
5541 G22b

1750MHz Conversion Gain, IIP3 and NF vs LO Power



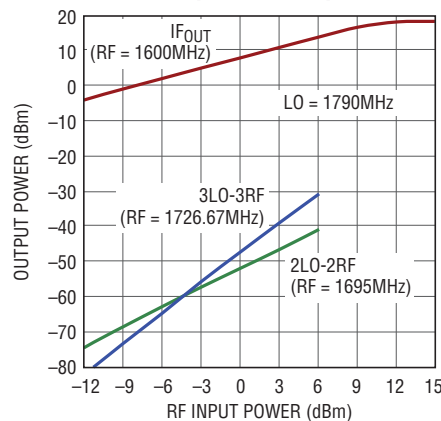
5541 G23

2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



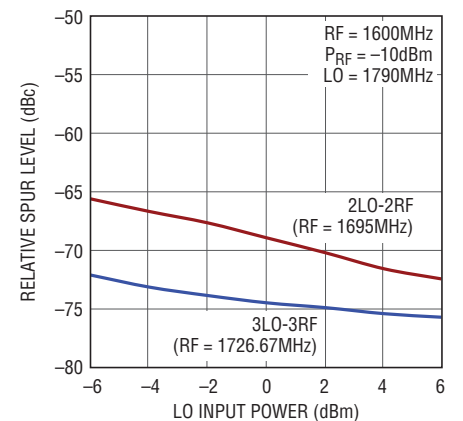
5541 G24

Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



5541 G25

2 × 2 and 3 × 3 Spur Suppression vs LO Power



5541 G26

PIN FUNCTIONS

NC (Pin 1): This pin is not connected internally. It can be left floating, connected to ground or to V_{CC} .

RF (Pin 2): Single-Ended Input for the RF Signal. This pin is internally connected to the primary side of the RF input transformer, which has low DC resistance to ground. **A series DC-blocking capacitor should be used to avoid damage to the integrated transformer.** The RF input is impedance matched, as long as the selected LO input is driven with a 0dBm \pm 6dB source between 1.4GHz and 2GHz.

CT (Pin 3): RF Transformer Secondary Center-Tap. This pin may require a bypass capacitor to ground. See the Applications Information section. This pin has an internally generated bias voltage of 1.2V. It must be DC-isolated from ground and V_{CC} .

GND (Pins 4, 10, 12, 13, 17, Exposed Pad Pin 21): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad metal of the package provides both electrical contact to ground and good thermal contact to the printed circuit board.

SHDN (Pin 5): Shutdown Pin. When the input voltage is less than 0.3V, the internal circuits supplied through pins 6, 8, 14, 18 and 19 are enabled. When the input voltage is greater than 3V, all circuits are disabled. Typical input current is less than 10 μ A. This pin must not be allowed to float.

V_{CC2} (Pin 6) and V_{CC1} (Pin 8): Power Supply Pins for the LO Buffer and Bias Circuits. These pins are internally connected and must be externally connected to a regulated 3.3V supply, with bypass capacitors located close to the pin. Typical current consumption is 92mA.

LOBIAS (Pin 7): This Pin Allows Adjustment of the LO Buffer Current. Typical DC voltage is 2.2V.

LOSEL (Pin 9): LO1/LO2 Select Pin. When the input voltage is less than 0.3V, the LO1 port is selected. When the input voltage is greater than 3V, the LO2 port is selected. Typical input current is 11 μ A for LOSEL = 3.3V. This pin must not be allowed to float.

LO1 (Pin 11) and LO2 (Pin 15): Single-Ended Inputs for the Local Oscillators. These pins are internally biased at 0V and require external DC blocking capacitors. Both inputs are internally matched to 50 Ω , even when the chip is disabled (SHDN = high).

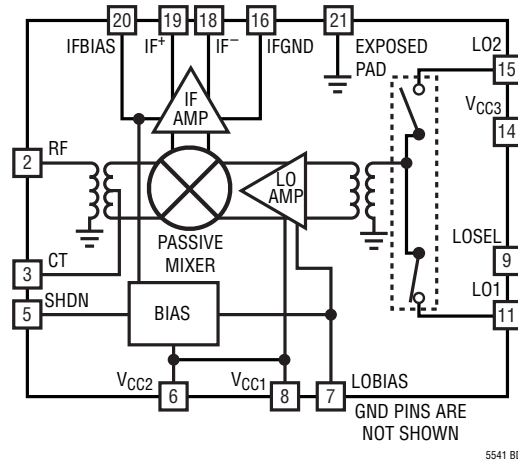
V_{CC3} (Pin 14): Power Supply Pin for the LO Switch. This pin must be connected to a regulated 3.3V supply and bypassed to ground with a capacitor near the pin. Typical DC current consumption is less than 100 μ A.

IFGND (Pin 16): DC Ground Return for the IF Amplifier. This pin must be connected to ground to complete the IF amplifier's DC current path. Typical DC current is 100mA.

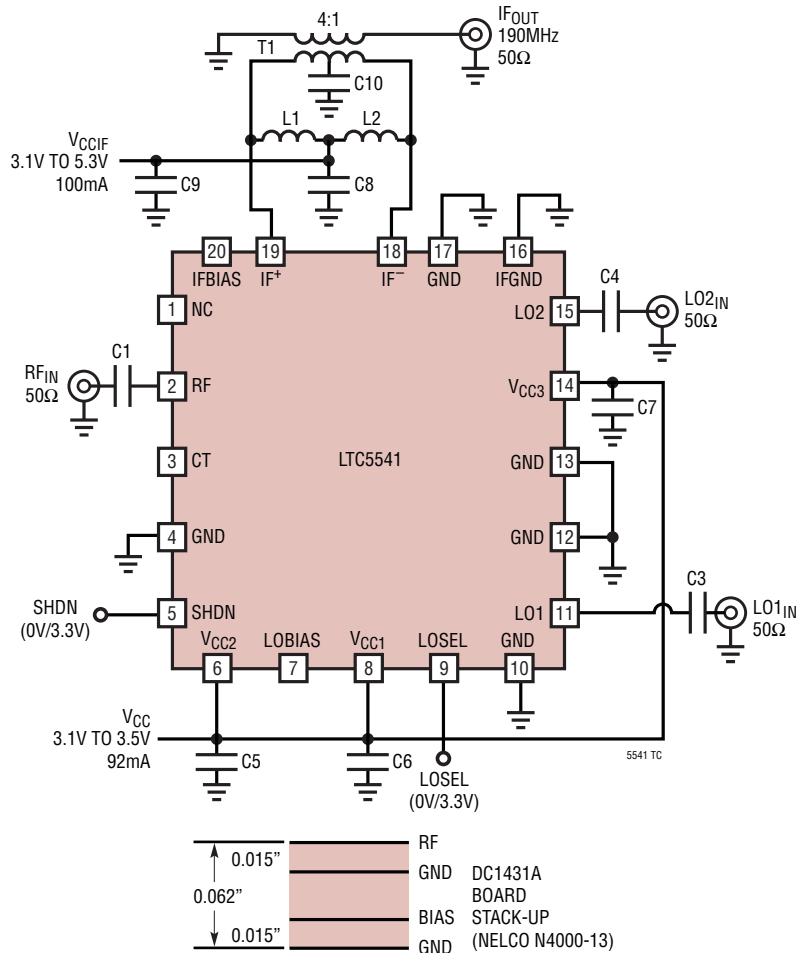
IF⁻ (Pin 18) and IF⁺ (Pin 19): Open-Collector Differential Outputs for the IF Amplifier. These pins must be connected to a DC supply through impedance matching inductors, or a transformer center-tap. Typical DC current consumption is 50mA into each pin.

IFBIAS (Pin 20): This Pin Allows Adjustment of the IF Amplifier Current. Typical DC voltage is 2.1V.

BLOCK DIAGRAM



TEST CIRCUIT



L1, L2 vs IF Frequencies	
IF (MHz)	L1, L2 (nH)
140	270
190	150
240	100
300	56
380	33

REF DES	VALUE	SIZE	COMMENTS
C1	2.2pF	0402	AVX
C3, C4, C6, C7, C8	22pF	0402	AVX
C5, C9	1μF	0603	AVX
C10	1000pF	0402	AVX
L1, L2	150nH	0603	Coilcraft 0603CS
T1 (Alternate)	TC4-1W-7ALN+ (WBC4-6TLB)		Mini-Circuits (Coilcraft)

Figure 1. Standard Downmixer Test Circuit Schematic (190MHz IF)

APPLICATIONS INFORMATION

Introduction

The LTC5541 consists of a high linearity passive double-balanced mixer core, IF buffer amplifier, high speed single-pole double-throw (SPDT) LO switch, LO buffer amplifier and bias/shutdown circuits. See Block Diagram section for a description of each pin function. The RF and LO inputs are single-ended. The IF output is differential. Low-side or high-side LO injection can be used. The evaluation circuit, shown in Figure 1, utilizes bandpass IF output matching and an IF transformer to realize a 50Ω single-ended IF output. The evaluation board layout is shown in Figure 2.

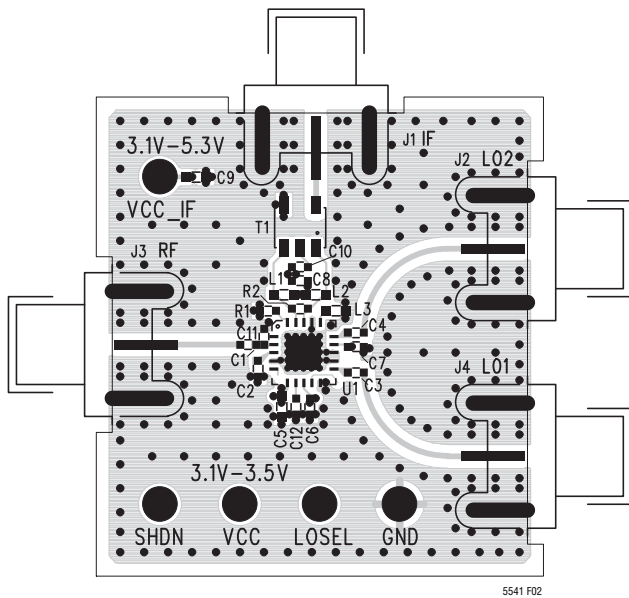


Figure 2. Evaluation Board Layout

RF Input

The mixer's RF input, shown in Figure 3, is connected to the primary winding of an integrated transformer. A 50Ω match is realized when a series capacitor, C1, is connected to the RF input. C1 is also needed for DC blocking if the RF source has DC voltage present, since the primary side of the RF transformer is DC-grounded internally. The DC resistance of the primary is approximately 3.6Ω.

The secondary winding of the RF transformer is internally connected to the passive mixer. The center-tap of the transformer secondary is connected to pin 3 (CT) to allow the connection of bypass capacitor, C2. The value of C2 is LO frequency-dependent and is not required for most

applications. When used, C2 should be located within 2mm of pin 3 for proper high-frequency decoupling. The nominal DC voltage on the CT pin is 1.2V.

For the RF input to be matched, the selected LO input must be driven. A broadband input match is realized with C1 = 2.2pF. The measured input return loss is shown in Figure 4 for LO frequencies of 1.4GHz, 1.75GHz and 2GHz. These LO frequencies correspond to the lower, middle and upper values of the LO range. As shown in Figure 4, the RF input impedance is somewhat dependent on LO frequency, although a single value of C1 is adequate to cover the 1.3GHz-2.3GHz RF band.

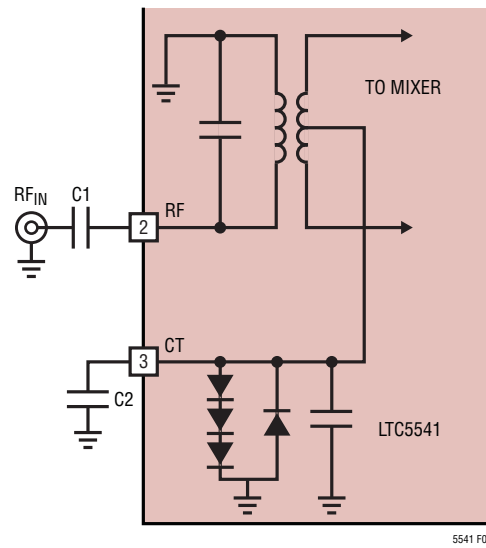


Figure 3. RF Input Schematic

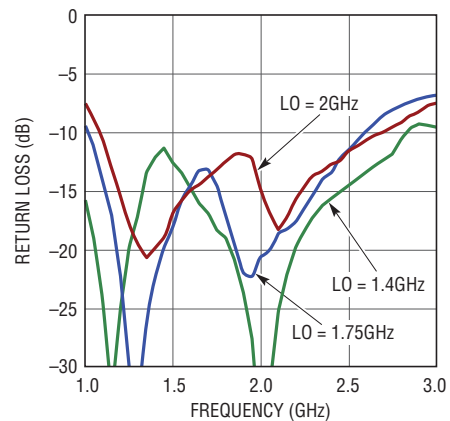


Figure 4. RF Input Return Loss

APPLICATIONS INFORMATION

The nominal LO input level is 0dBm although the limiting amplifiers will deliver excellent performance over a ± 6 dB input power range. LO input power greater than 6dBm may cause conduction of the internal ESD diodes. Series capacitors C3 and C4 optimize the input match and provide DC blocking.

The LO1 input impedance and input reflection coefficient, versus frequency, is shown in Table 3. The LO2 port is identical due to the symmetric device layout and packaging.

Table 3. LO1 Input Impedance vs Frequency (at Pin 11, No External Matching, LOSEL = Low)

FREQUENCY (GHz)	INPUT IMPEDANCE	S11	
		MAG	ANGLE
1.0	55.1 – j21.8	0.209	–65.2
1.2	34.5 – j11.4	0.225	–135.9
1.4	29.5 – j1.2	0.257	–176.1
1.6	29.6 + j6.3	0.267	+158.2
1.8	31.6 + j10.9	0.261	+141.5
2.0	33.5 + j13.7	0.255	+130.7
2.2	35.2 + j16.1	0.253	+121.6
2.4	36.9 + j17.8	0.251	+114.4
2.6	38.0 + j18.9	0.250	+110.0
2.8	38.3 + j19.5	0.254	+108.3
3.0	37.3 + j20.4	0.270	+108.5

IF Output

The IF amplifier, shown in Figure 7, has differential open-collector outputs (IF⁺ and IF[–]), a DC ground return pin (IFGND), and a pin for modifying the internal bias (IFBIAS). The IF outputs must be biased at the supply voltage (V_{CCIF}), which is applied through matching inductors L1 and L2. Alternatively, the IF outputs can be biased through the center tap of a transformer. Each IF output pin draws approximately 50mA of DC supply current (100mA total). IFGND (pin 16) must be grounded or the amplifier will not draw DC current. Grounding through inductor L3 may improve LO-IF and RF-IF leakage performance in some applications, but is otherwise not necessary. High DC resistance in L3 will reduce the IF amplifier supply current, which will degrade RF performance.

For optimum single-ended performance, the differential IF outputs must be combined through an external IF

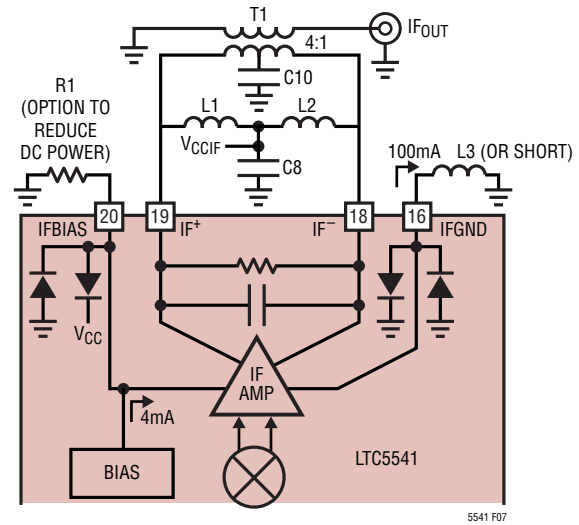


Figure 7. IF Amplifier Schematic with Bandpass Match

transformer or discrete IF balun circuit. The evaluation board (see Figures 1 and 2) uses a 4:1 ratio IF transformer for impedance transformation and differential to single-ended transformation. It is also possible to eliminate the IF transformer and drive differential filters or amplifiers directly.

The IF output impedance can be modeled as 300Ω in parallel with 2.3pF at IF frequencies. An equivalent small-signal model (including bondwire inductance) is shown in Figure 8. Frequency-dependent differential IF output impedance is listed in Table 4. This data is referenced to the package pins (with no external components) and includes the effects of IC and package parasitics.

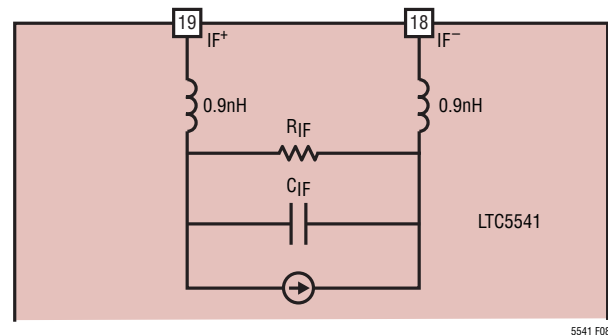


Figure 8. IF Output Small-Signal Model

APPLICATIONS INFORMATION

Bandpass IF Matching

The IF output can be matched for IF frequencies as low as 90MHz or as high as 500MHz using the bandpass IF matching shown in Figure 1 and Figure 7. L1 and L2 resonate with the internal IF output capacitance at the desired IF frequency. The value of L1, L2 is calculated as follows:

$$L1, L2 = 1/[2 \pi f_{IF}]^2 \cdot 2 \cdot C_{IF}$$

where C_{IF} is the internal IF capacitance (listed in Table 4).

Values of L1 and L2 are tabulated in Figure 1 for various IF frequencies. For IF frequencies below 90MHz, the values of L1, L2 become unreasonably high and the lowpass topology shown in Figure 9 is preferred. Measured IF output return loss for bandpass IF matching is plotted in Figure 10.

Table 4. IF Output Impedance vs Frequency

FREQUENCY (MHz)	DIFFERENTIAL OUTPUT IMPEDANCE ($R_{IF} \parallel X_{IF} (C_{IF})$)
90	329 \parallel -j769 (2.3pF)
140	314 \parallel -j494 (2.3pF)
190	305 \parallel -j364 (2.3pF)
240	310 \parallel -j288 (2.3pF)
300	303 \parallel -j226 (2.35pF)
380	289 \parallel -j175 (2.4pF)
500	273 \parallel -j118 (2.7pF)

Lowpass IF Matching

An alternative IF matching network shown in Figure 9 uses a lowpass topology, which provides excellent RF to IF and LO to IF isolation. V_{CCIF} is supplied through the center tap of the 4:1 transformer. Similar to the bandpass topology, L1 and L2 cancel out the reactive part of the internal capacitance and the impedance transformation is realized by the 4:1 transformer. This topology is preferred for low IF frequencies since L1 and L2 may be replaced with shorts. The LTC5541 demo board (see Figure 2) has been laid out to accommodate this matching topology with very few modifications.

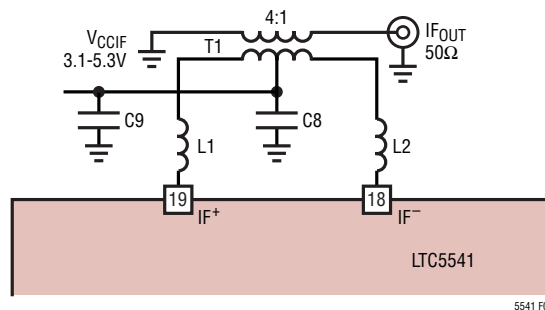


Figure 9. IF Output with Lowpass Matching

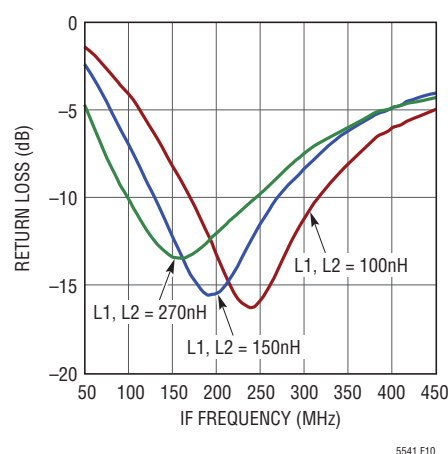


Figure 10. IF Output Return Loss

IF Amplifier Bias

The IF amplifier delivers excellent performance with $V_{CCIF} = 3.3V$, which allows the V_{CC} and V_{CCIF} supplies to be common. With V_{CCIF} increased to 5V, the RF input P1dB increases by approximately 3dB, at the expense of higher power consumption. Mixer performance at 1950MHz is shown in Table 5 with $V_{CCIF} = 3.3V$ and 5V. For the highest conversion gain, high-Q wire-wound chip inductors are recommended for L1 and L2, especially when using $V_{CCIF} = 3.3V$. Low-cost multilayer chip inductors may be substituted, with a slight reduction in conversion gain.

Table 5. Performance Comparison with $V_{CCIF} = 3.3V$ and 5V (RF = 1950MHz, Low-Side LO, IF = 190MHz)

V_{CCIF}	I_{CCIF} (mA)	G_C (dB)	P1dB (dBm)	IIP3 (dBm)	NF (dB)
3.3V	100	7.8	11.3	26.4	9.6
5V	102	7.7	14.6	27.3	9.7

APPLICATIONS INFORMATION

The IFBIAS pin (pin 20) is available for reducing the DC current consumption of the IF amplifier, at the expense of IIP3. This pin should be left open-circuited for optimum performance. The internal bias circuit produces a 4mA reference for the IF amplifier, which causes the amplifier to draw approximately 100mA. If resistor R1 is connected to pin 20 as shown in Figure 7, a portion of the reference current can be shunted to ground, resulting in reduced IF amplifier current. For example, R1 = 1kΩ will shunt away 1.5mA from pin 20 and the IF amplifier current will be reduced by 38% to approximately 62mA. The nominal, open-circuit DC voltage at pin 20 is 2.1V. Table 6 lists RF performance at 1950MHz versus IF amplifier current.

Table 6. Mixer Performance with Reduced IF Amplifier Current (RF = 1950MHz, Low-Side LO, IF = 190MHz)

V_{CCIF} = 3.3V

R1 (kΩ)	I _{CCIF} (mA)	G _c (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	100	7.8	26.4	11.4	9.6
4.7	90	7.5	26.0	11.6	9.6
2.2	81	7.4	25.3	11.7	9.5
1	62	6.9	23.4	11.7	9.7

V_{CCIF} = 5V

R1 (kΩ)	I _{CCIF} (mA)	G _c (dB)	IIP3 (dBm)	P1dB (dBm)	NF (dB)
OPEN	102	7.7	27.3	14.6	9.7
4.7	92	7.5	27.2	14.7	9.6
2.2	83	7.2	26.5	14.8	9.6
1	65	6.7	24.7	14.0	9.7

Shutdown Interface

Figure 11 shows a simplified schematic of the SHDN pin interface. To disable the chip, the SHDN voltage must be higher than 3.0V. If the shutdown function is not required, the SHDN pin should be connected directly to GND. The voltage at the SHDN pin should never exceed the power supply voltage (V_{CC}) by more than 0.3V. If this should occur, the supply current could be sourced through the ESD diode, potentially damaging the IC.

The SHDN pin must be pulled high or low. If left floating, then the on/off state of the IC will be indeterminate. If a three-state condition can exist at the SHDN pin, then a pull-up or pull-down resistor must be used.

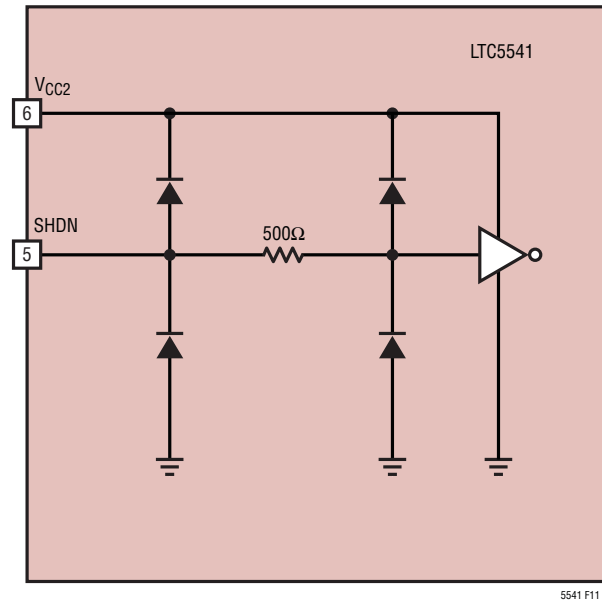


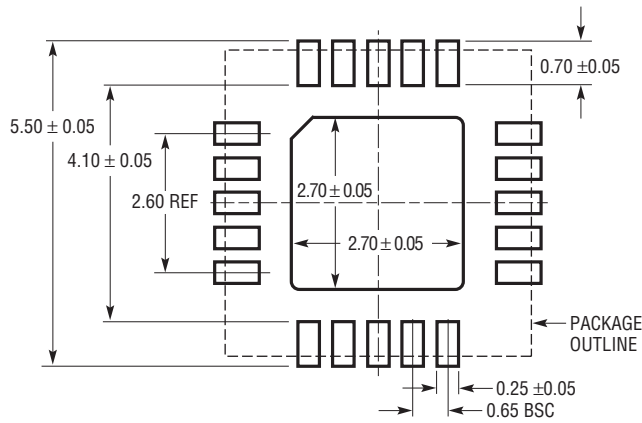
Figure 11. Shutdown Input Circuit

Supply Voltage Ramping

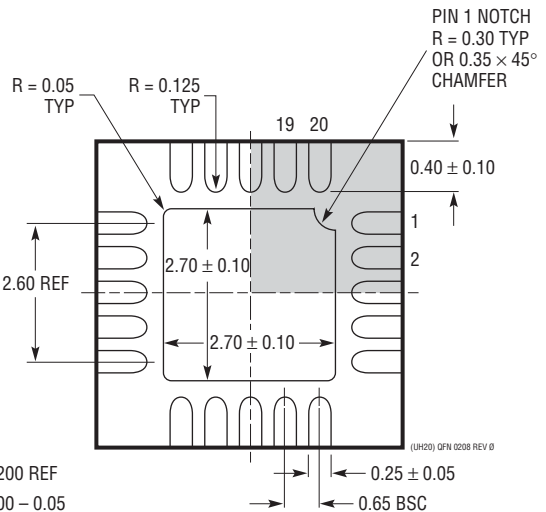
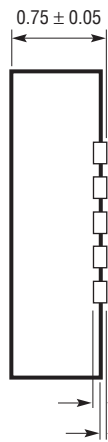
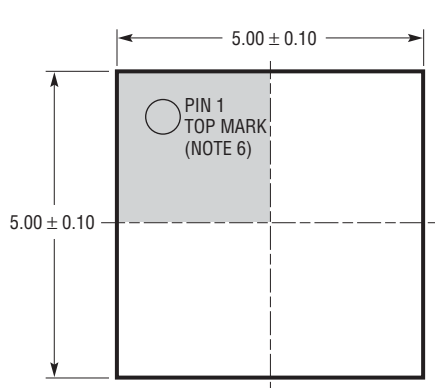
Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended.

PACKAGE DESCRIPTION

UH Package
20-Lead Plastic QFN (5mm × 5mm)
 (Reference LTC DWG # 05-08-1818 Rev 0)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

- NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
 2. DRAWING NOT TO SCALE
 3. ALL DIMENSIONS ARE IN MILLIMETERS
 4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
 5. EXPOSED PAD SHALL BE SOLDER PLATED
 6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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