

AS3415/AS3435

Integrated Active Noise Cancelling Solution with Bypass Feature

General Description

The AS3415/35 are speaker drivers with Ambient Noise Cancelling function for headsets, headphones or ear pieces. They are intended to improve quality of e.g. music listening, a phone conversation etc. by reducing background ambient noise.

The fully analog implementation allows the lowest power consumption, lowest system BOM cost and most natural received voice enhancement otherwise difficult to achieve with DSP implementations. The device is designed to be easily applied to existing architectures.

An internal OTP-ROM can be optionally used to store the microphones gain calibration settings. The AS3415/35 can be used in different configurations for best trade-off of noise cancellation, required filtering functions and mechanical designs.

The simpler feed-forward topology is used to effectively reduce frequencies typically up to 2-3 kHz. The feed-back topology with either 1 or 2 filtering stages has its strengths especially at very low frequencies. The typical bandwidth for a feed-back system is from 20Hz up to 1 kHz which is lower than the feed-forward systems.

The filter loop for both systems is determined by measurements, for each specific headset individually, and depends very much on mechanical designs. The gain and phase compensation filter network is implemented with cheap resistors and capacitors for lowest system costs.

Key Benefits & Features

The benefits and features of AS3415/35, Integrated Active Noise Cancelling Solution with Bypass Feature are listed below:

Figure 1:
Added Value of Using AS3415/35

| Benefits | Features |
|-----------------------------------|---------------------------------------|
| All ANC Topologies | Feed Forward, Feed Back and Hybrid |
| No mechanical audio bypass switch | Integrated depletion mode transistors |
| Music EQ functionality | Ultra flexible low power EQ circuit |
| Longest play time | 10mW @1.5V stereo ANC; <1µA quiescent |
| Highest audio quality | 2x24mW, 0.1% THD+N @ 32Ω, 1.5V supply |

| Benefits | Features |
|---|--|
| Smallest package | Two different packages available: <ul style="list-style-type: none"> AS3415 QFN32 [5x5mm] 0.5mm pitch AS3435 QFN36 [5x5mm] 0.4mm pitch |
| Low battery indication | LED driver with selectable driving strength |
| Different control interface options | Push Button-, Slide switch- or I ² C control interface |
| Highly innovative production trimming interface | OTP production trimming via audio interface |
| Active hearing mode with or without ANC and optional voice EQ | Monitor mode function |

Applications

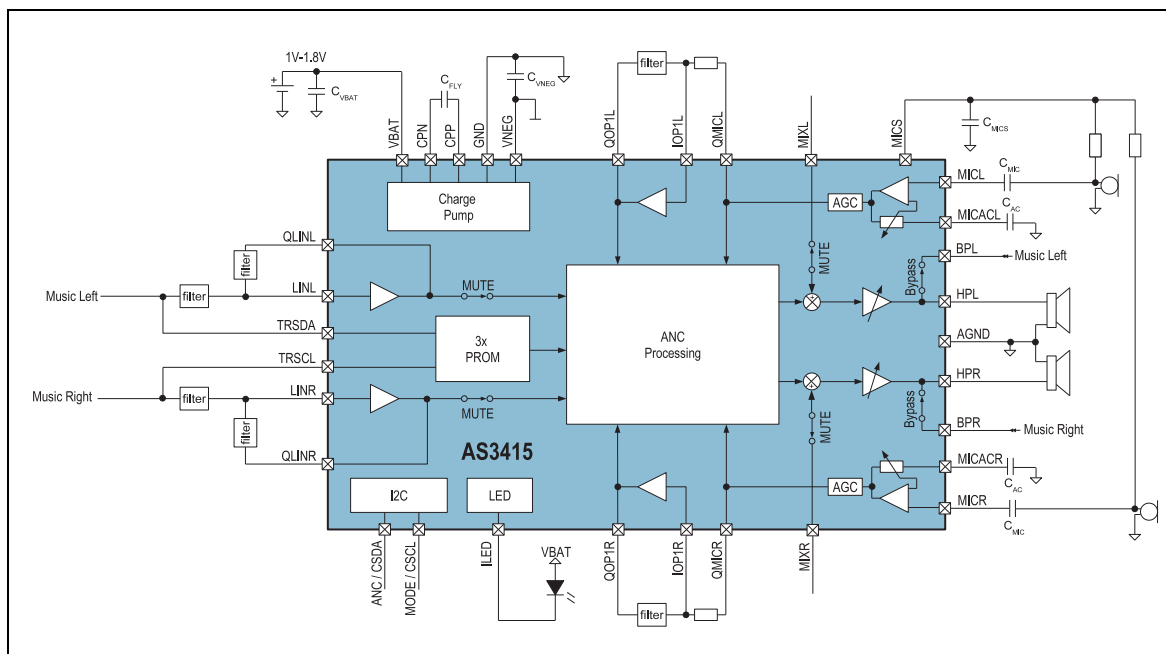
The devices are ideal for:

- Ear pieces
- Headsets
- Hands-Free Kits
- Mobile Phones
- Voice Communicating Devices

Block Diagram

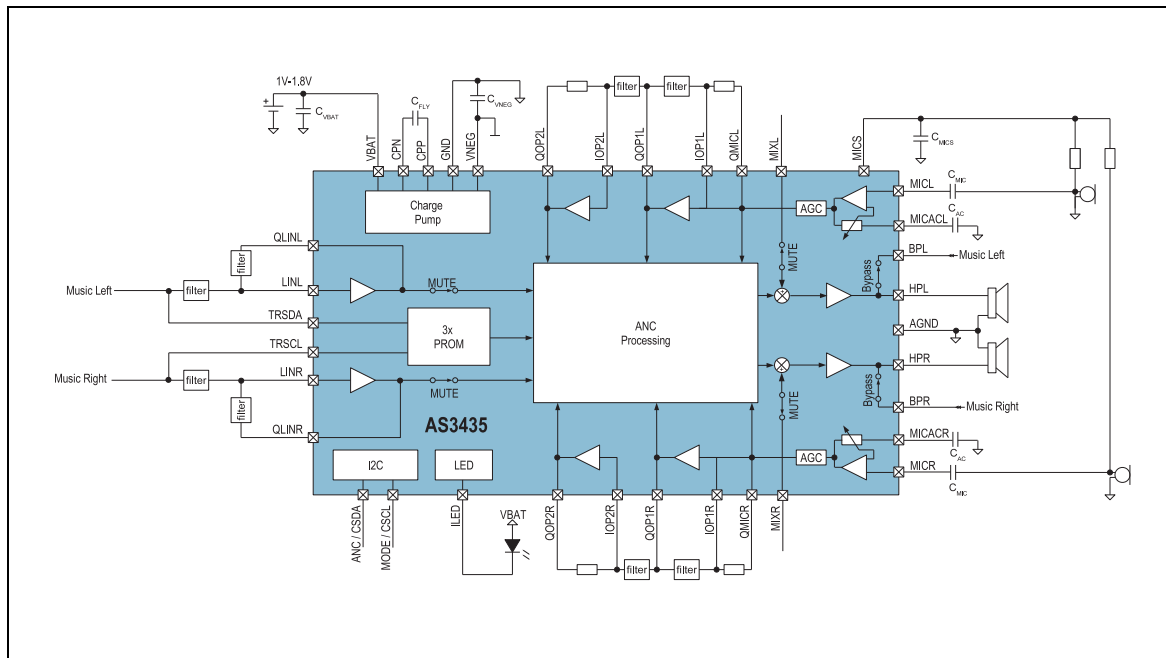
The functional blocks of AS3415/35 for reference are shown below:

Figure 2:
AS3415 Block Diagram



AS3415 Block Diagram: This figure shows the block diagram of the AS3415 with all relevant system components.

Figure 3:
AS3435 Block Diagram

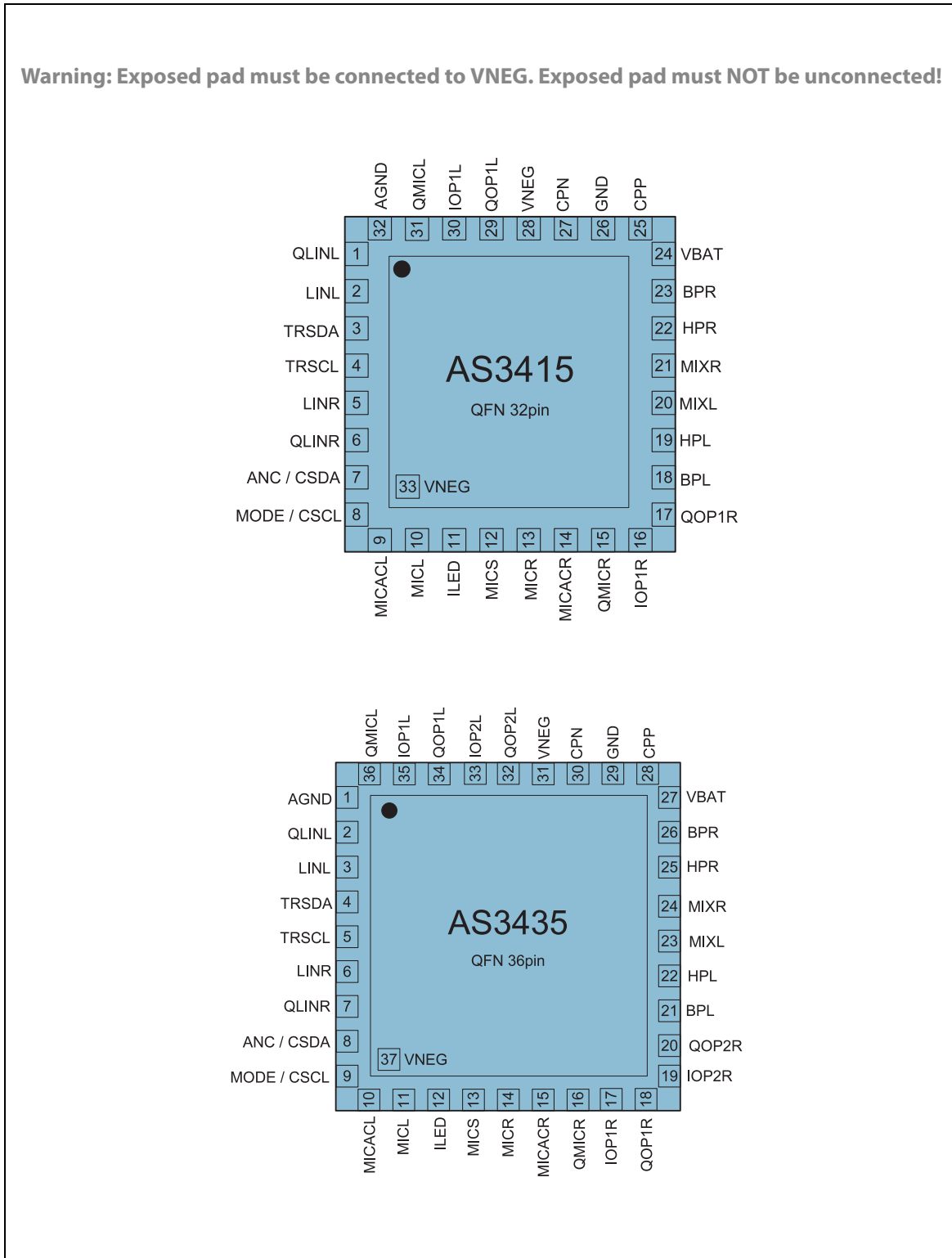


AS3435 Block Diagram: This figure shows the block diagram of the AS3435 with all relevant system components.

Pin Assignment

The AS3415 and AS3435 pin assignments are described below.

Figure 4:
Pin Assignments



Pin Assignments: Shows the pin assignment of the AS3415 and AS3435 (Top View).

Pin Description

The following figure shows the pin description for AS3415/35.

Figure 5:
Pin Description

| Pin Name | Pin Number | | Pin Type | Description |
|-------------|------------|--------|----------|---|
| | AS3435 | AS3415 | | |
| AGND | 1 | 32 | ANA OUT | Analog reference ground. Do not connect this pin to power or digital ground plane. |
| QLINL | 2 | 1 | ANA OUT | Line input EQ gain stage output left channel. |
| LINL | 3 | 2 | ANA IN | Line input EQ left channel. |
| TRSDA | 4 | 3 | ANA IN | Clock input for production trimming. Can be connected to LINL pin to enable production trimming via 3.5mm audio jack. |
| TRSCL | 5 | 4 | ANA IN | Data input for production trimming. Can be connected to LINR pin to enable production trimming via 3.5mm audio jack. |
| LINR | 6 | 5 | ANA IN | Line input EQ right channel. |
| QLINR | 7 | 6 | ANA IN | Line input EQ gain stage output right channel. |
| ANC / CSDA | 8 | 7 | DIG IN | Serial interface data for I ² C interface and ANC control to enable/disable ANC. |
| MODE / CSCL | 9 | 8 | DIG IN | Serial Interface Clock for I ² C interface and control pin for power up/down and Monitor mode. |
| MICACL | 10 | 9 | ANA OUT | Microphone preamplifier AC coupling ground terminal. This pin requires a 10 μ F capacitor connected to AGND pin. |
| MICL | 11 | 10 | ANA IN | ANC microphone input left channel. |
| ILED | 12 | 11 | ANA IN | Current sink input for on-indication LED. |
| MICS | 13 | 12 | SUP OUT | Microphone Supply output. This pin needs an output blocking capacitor with 10 μ F. |
| MICR | 14 | 13 | ANA IN | ANC microphone preamplifier input right channel. |
| MICACR | 15 | 14 | ANA OUT | Microphone preamplifier AC coupling ground terminal. This pin requires a 10 μ F capacitor connected to AGND pin. |
| QMICR | 16 | 15 | ANA OUT | ANC microphone preamplifier output right channel. |
| IOP1R | 17 | 16 | ANA IN | ANC filter OpAmp1 input right channel. |
| QOP1R | 18 | 17 | ANA OUT | ANC filter OpAmp1 output right channel. |

| Pin Name | Pin Number | | Pin Type | Description |
|----------|------------|--------|----------|--|
| | AS3435 | AS3415 | | |
| IOP2R | 19 | - | ANA IN | ANC Filter OpAmp2 input right channel. |
| QOP2R | 20 | - | ANA OUT | ANC filter OpAmp2 output right channel. |
| BPL | 21 | 18 | ANA IN | Left audio bypass terminal input. |
| HPL | 22 | 19 | ANA OUT | Headphone amplifier output left channel |
| MIXL | 23 | 20 | ANA IN | Headphone amplifier external summation input terminal left channel. |
| MIXR | 24 | 21 | ANA IN | Headphone amplifier external summation input terminal right channel. |
| HPR | 25 | 22 | ANA OUT | Headphone amplifier output right channel |
| BPR | 26 | 23 | ANA OUT | Right audio bypass terminal input. |
| VBAT | 27 | 24 | SUP IN | Positive supply terminal of IC. |
| CPP | 28 | 25 | ANA OUT | V _{NEG} charge pump flying capacitor positive terminal. |
| GND | 29 | 26 | GND | V _{NEG} charge pump ground terminal. |
| CPN | 30 | 27 | ANA OUT | V _{NEG} charge pump flying capacitor negative terminal. |
| VNEG | 31 | 28 | SUP OUT | V _{NEG} charge pump output. This pin must be connected to exposed pad of QFN package. |
| QOP2L | 32 | - | ANA OUT | ANC Filter OpAmp2 output left channel. |
| IOP2L | 33 | - | ANA IN | ANC Filter OpAmp2 input left channel. |
| QOP1L | 34 | 29 | ANA IN | Filter OpAmp1 output left channel. |
| IOP1L | 35 | 30 | ANA OUT | Filter OpAmp1 input left channel. |
| QMICL | 36 | 31 | SUP IN | ANC microphone preamplifier output left channel. |
| VNEG | 37 | 33 | SUP IN | Exposed Pad: Must be connected to VNEG pin 31(AS3435) or 28(AS3415). |

Pin Description: This table shows a detailed pin description of the AS3415 and AS3435.

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

| Parameter | Min | Max | Units | Comments |
|--|---------------|---------------|-------|---|
| Reference Ground | | | | Defined as in GND |
| Supply terminals | -0.5 | 2.0 | V | Applicable for pin VBAT |
| Ground terminals | -0.5 | 0.5 | V | Applicable for pin AGND |
| Negative terminals | -2.0 | 0.5 | V | Applicable for pins VNEG |
| Charge Pump pins | $V_{NEG}-0.5$ | $V_{BAT}+0.5$ | V | Applicable for pins CPN and CPP |
| Headphone pins | $VSS-0.5$ | $V_{BAT}+0.5$ | V | Applicable for pins HPR and HPL |
| Analog pins | $VSS-0.5$ | $V_{BAT}+0.5$ | V | Applicable for pins LINL, LINR, MICL/R, HPR, HPL, QMICL/R, QLINL/R, IOPx, QOPx, CPP, CPN, TRSCL, TRSDA, MICACL, MICACR, MIXR, MIXL, BPL, BPR and ILED |
| Control Pins | $VSS-0.5$ | 5 | V | Applicable for pins MICS, ANC/CSDA, MODE/CSCL |
| Other Pins | $VSS-0.5$ | 5 | V | Applicable for pin MICS |
| Input Current (latch-up immunity) | -100 | 100 | mA | Norm: JEDEC 17 |
| Continuous Power Dissipation ($T_A = +70^\circ\text{C}$) | | | | |
| Continuous Power Dissipation | - | 200 | mW | PT ⁽¹⁾ for QFN32/36 package |
| Electrostatic Discharge | | | | |
| Electrostatic Discharge HBM | | ± 2 | kV | Norm: JEDEC JESD22-A114C |
| Temperature Ranges and Storage Conditions | | | | |
| Junction Temperature | | +85 | °C | |
| Storage Temperature Range | -55 | +125 | °C | |
| Humidity non-condensing | 5 | 85 | % | |
| Moisture Sensitive Level | 3 | | | Represents a max. floor life time of 168h |

| Parameter | Min | Max | Units | Comments |
|--------------------------|-----|-----|-------|---|
| Package Body Temperature | | 260 | °C | The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". |

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

$V_{BAT} = 1.0V$ to $1.8V$, $T_A = -20^{\circ}C$ to $+85^{\circ}C$. Typical values are at $V_{BAT} = 1.5V$, $T_A = +25^{\circ}C$, unless otherwise specified.

Figure 7:
Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|---|---------------------------------|-----|-----------------------------|-------------|
| T_A | Ambient Temperature Range | | -20 | | +85 | $^{\circ}C$ |
| Supply Voltages | | | | | | |
| GND | Reference Ground | | 0 | | 0 | V |
| V_{BAT} | Battery Supply Voltage | Normal operation | 1.0 | | 1.8 | V |
| | | Two wire interface operation | 1.4 | | 1.8 | V |
| V_{NEG} | Charge Pump Voltage | | -1.8 | | -0.7 | V |
| V_{DELTA} | Difference of Ground Supplies GND, AGND | To achieve good performance, the negative supply terminals should be connected to a low impedance ground plane. | -0.1 | | 0.1 | V |
| Other pins | | | | | | |
| V_{MICS} | Microphone Supply Voltage | MICS | 0 | | 3.7 | V |
| V_{ANALOG} | Analog Pins | MICACL, MICACR, LINR, LINL, MIXL, MIXR, HPR, HPL, QMICL, QMICR, QLINL, QLINR, IOPx, QOPx, BPL, BPR | V_{NEG} | | V_{BAT} | V |
| $V_{CONTROL}$ | Control Pins | MODE/CSCL, ANC/CSDA | V_{NEG} | | 3.7 | V |
| V_{LED} | ILED current source | ILED | VSS | | V_{BAT} | V |
| V_{CP} | Charge Pump pins | CPN, CPP | V_{NEG} | | V_{BAT} | V |
| V_{TRIM} | Application Trim Pins | TRSCL and TRSDA | V_{NEG} -0.3 or -1.8 | | V_{BAT} +0.5 or 1.8 | V |
| V_{MIC} | Microphone Inputs | MICL and MICR | VSS | | V_{BAT} | V |
| I_{leak} | Leakage current | $V_{BAT} < 0.8V$ | | | 20 | μA |
| | | $V_{BAT} < 0.6V$ | | | 10 | μA |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|---|-----|------|-----|------|
| Block Power Requirements @ 1.5V V_{BAT} | | | | | | |
| I _{OFF} | Off mode current | MODE pin low, device switched off | | 1 | | μA |
| I _{SYS} | Reference supply current | Bias generation, oscillator, POR | | 0.46 | | mA |
| I _{VNEG} | V _{NEG} Charge Pump | | | 0.36 | | mA |
| I _{LIN} | LineIn gain stage current | No signal, stereo, normal mode | | 1.4 | | mA |
| | | No signal, stereo, ECO mode | | 1 | | mA |
| I _{MIC} | Mic gain stage current | No signal, stereo, normal mode | | 1.5 | | mA |
| | | No signal, stereo, ECO mode | | 1.1 | | mA |
| I _{HP} | Headphone stage current | No signal, normal mode | | 2.4 | | mA |
| | | No signal, ECO mode | | 2 | | mA |
| I _{MICS} | MICS charge pump current | No load | | 400 | | μA |
| I _{OP1} | OP1 supply current | OP1L and OP1R enabled, normal mode | | 1.4 | | mA |
| | | OP1L and OP1R enabled, ECO mode | | 1 | | mA |
| I _{OP2} | OP2 supply current | OP2L and OP2R enabled, normal mode | | 1.4 | | mA |
| | | OP2L and OP2R enabled, ECO mode | | 1 | | mA |
| Typical System Power Consumption | | | | | | |
| P _{FF} | Typical power consumption feed forward application | OP1L, OP1R enabled OP2L, OP2R disabled 500μA microphone load ILED disabled | | 13.5 | | mW |
| P _{FF_ECO} | Typical power consumption feed forward application in ECO mode | All blocks in ECO mode OP1L, OP1R enabled OP2L, OP2R disabled 500μA microphone load ILED disabled | | 10.5 | | mW |
| P _{FB} | Typical power consumption feed forward application | OP1L, OP1R enabled OP2L, OP2R enabled 500μA microphone load ILED disabled | | 15.5 | | mW |
| P _{FB_ECO} | Typical power consumption feedback application in ECO mode | All blocks in ECO mode OP1L, OP1R enabled OP2L, OP2R enabled 500μA microphone load ILED disabled | | 13 | | mW |

Electrical Characteristics: Shows the electrical characteristics like typical supply voltages as well as system current consumption.

Detailed Description

This section provides a detailed description of the device related components.

Audio Line Input

The chip features one stereo line input for music playback. Due to the fact that the line input gain stage operates as an inverting amplifier, with access to the negative input pin and the output pin, the gain can be freely configured. In monitor mode the line inputs can also be muted in order to interrupt the music playback and increase speech intelligibility.

Besides setting the gain with a resistor network, it is also possible to do simple EQ functions for sound enhancement. The EQ function can also be used to compensate for low frequency bass losses in ANC headset with a feed-back topology. For feed-forward headsets it can be used for sound enhancement to compensate for example a lack of bass because of physical design constraints of a headset.

Line Input Gain Setting

The line input gain can be configured with two external resistors, R_1 and R_2 , per channel as shown in [Figure 8](#). The gain can be calculated with the following formula:

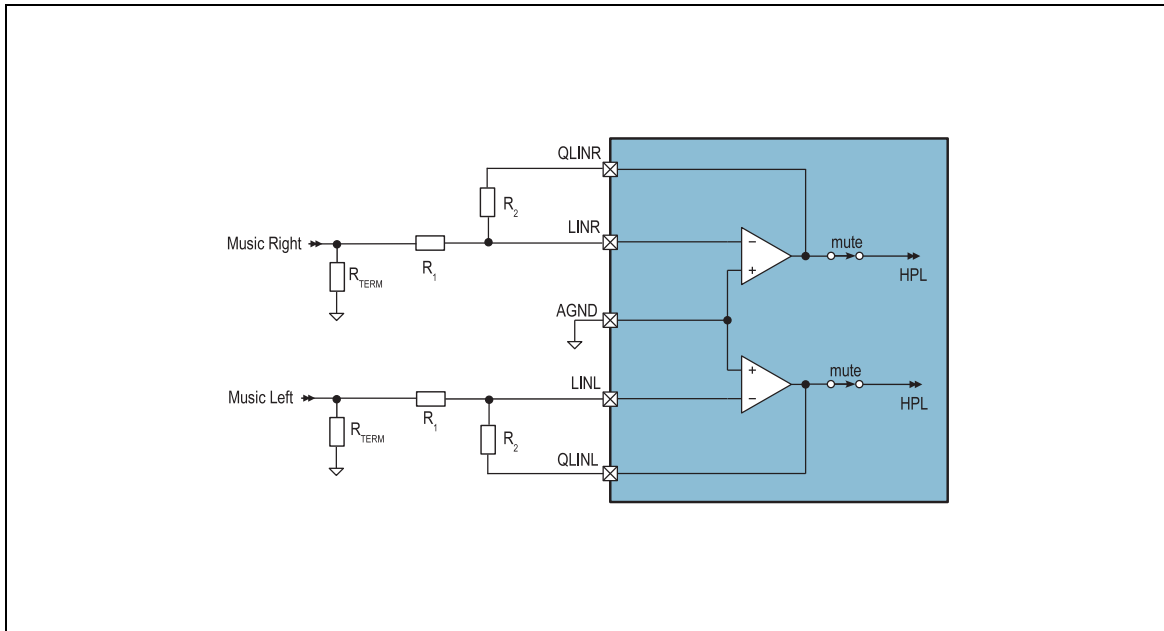
$$A_{Line} = 20 \cdot \log \frac{R_2}{R_1} \dots [\text{dB}]$$

The resistors R_1 and R_2 should be in the range from $1\text{k}\Omega$ to $100\text{k}\Omega$. If the application requires a gain of +6dB the resistor value can be calculated as follows:

$$R_2 = R_1 \cdot 10^{\frac{A_{Line}}{20}} = 10\text{k}\Omega \cdot 10^{\frac{6}{20}} = 20\text{k}\Omega$$

For this example, a resistor value for R_1 was defined as $10\text{k}\Omega$. This +6dB calculation yields a value for R_2 of $20\text{k}\Omega$.

Figure 8:
Stereo Line Input



Stereo Line Input: Internal structure of the stereo line input preamplifier.

High Pass EQ Function

If there is a high pass function desired in an application, to block very low frequencies that could harm the speaker, or eliminate little offset voltages a simple capacitor C_{HP} could do this function. The implementation is shown in Figure 10. The correct capacitor value for the desired cut-off frequency can be calculated with the following formula:

$$C_{HP} = \frac{1}{2 \cdot \pi \cdot R_1 \cdot f_{cut-off}}$$

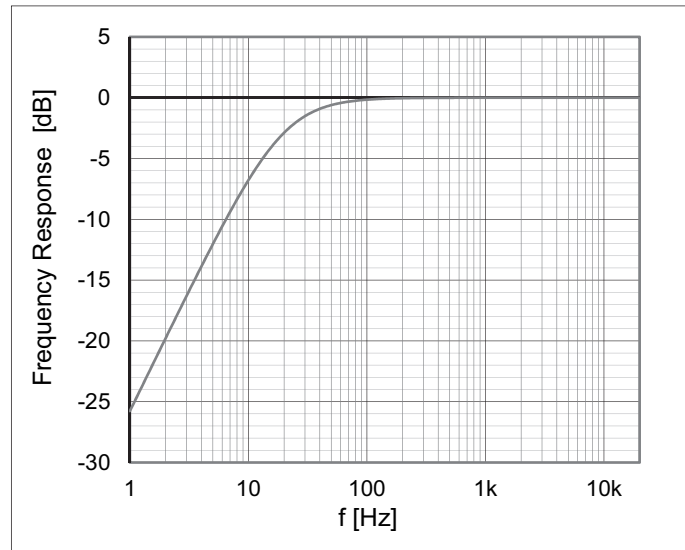
A typical cut-off frequency in an audio application is 20Hz. The resistor value of R_1 in this example is 10kΩ.

$$C_{HP} = \frac{1}{2 \cdot \pi \cdot 10k\Omega \cdot 20Hz} = 796nF$$

The result of the calculation is a capacitor with a value of 796nF. Because such a capacitor is not available on the market a capacitor close to the calculated value should be selected. This would be 750nF or 820nF.

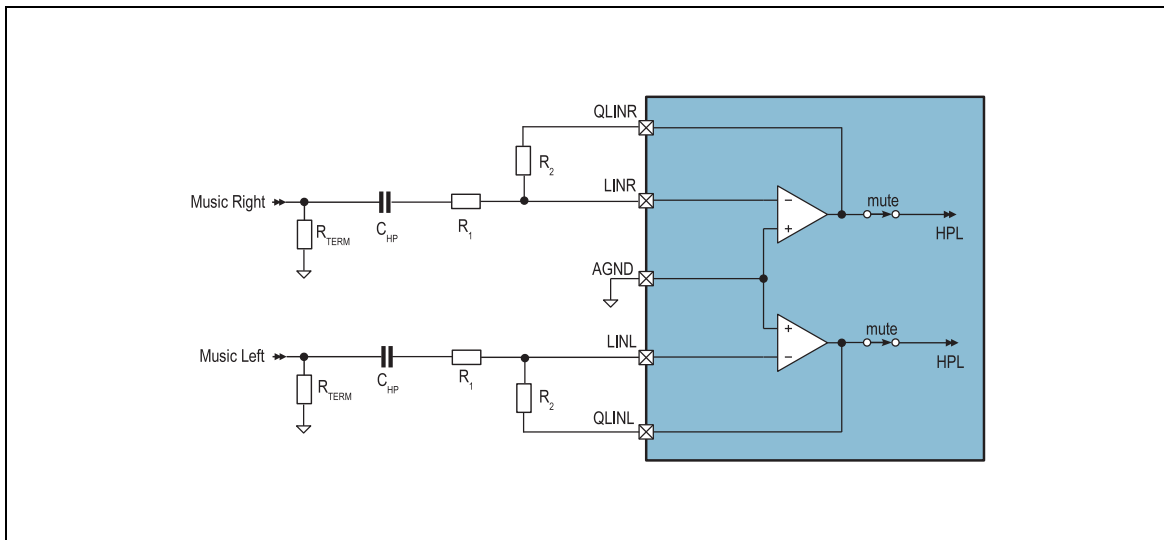
Figure 9:
Frequency Response Line Input High Pass

Frequency Response Line Input High Pass: This diagram shows the frequency response of the calculated line input high pass with $C_{HP}=820\text{nF}$ and $R_1=10\text{k}\Omega$.



The frequency response shown in Figure 9 shows the transfer function of the filter calculation. The cut-off frequency is close to 20Hz even though we selected a slightly different capacitor than the calculated one. Therefore it is no problem for an application to select an approximated component value.

Figure 10:
High Pass EQ Circuit



Stereo Line Input: This figure shows the circuit diagram for the line input high pass EQ circuit.

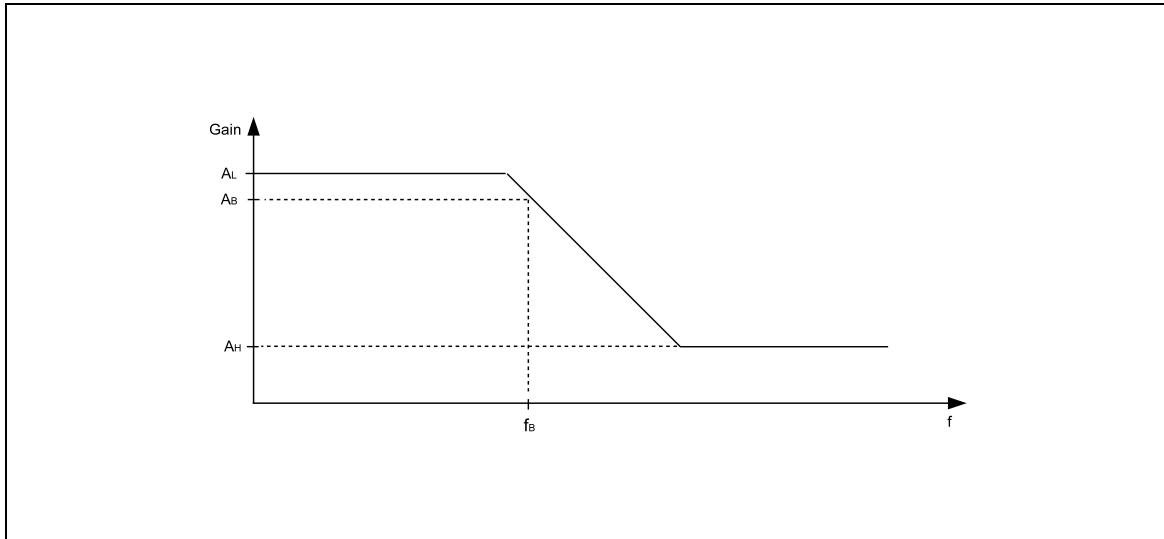
Bass Boost EQ Function

Complex EQ Filtering:

It is also possible to do even more complex EQ filtering than is shown in the example with the integrated EQ amplifier. For details please contact our local support team.

Some applications may require low frequency compensation. This function can either help to compensate low frequency losses due to an ANC feedback circuit or just to help compensate for a lack of low frequency presence in a headset. In order to amplify low frequencies there are three parameters that can be selected by the design engineer. These are shown in Figure 11 below.

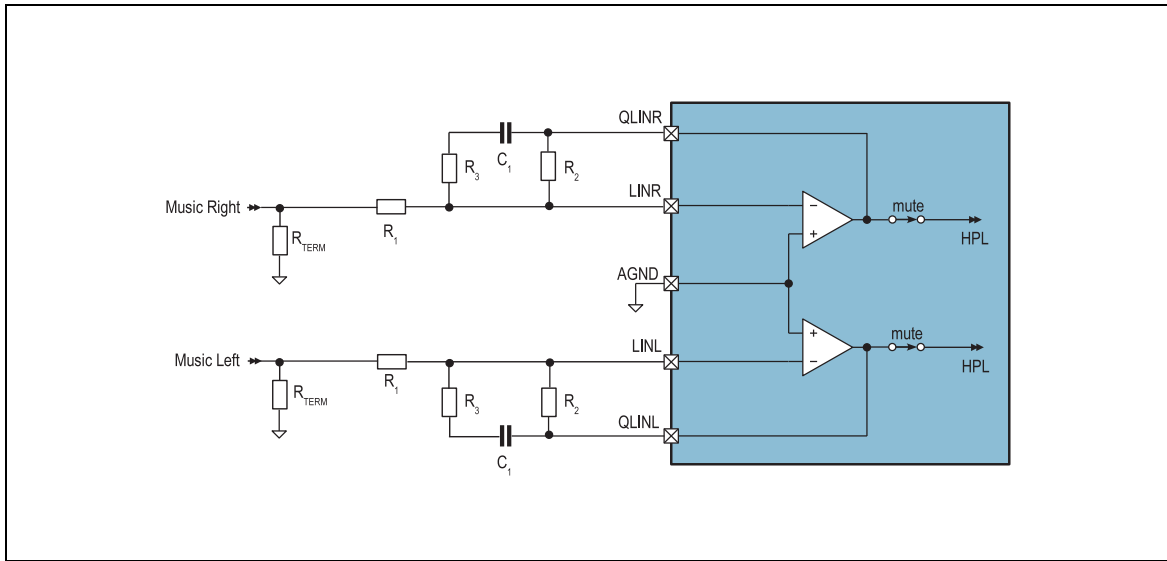
Figure 11:
Bass Boost Definition



Bass Boost Definition: This figure shows the typical shape of a bass boost transfer function with the key parameters for the definition of it.

The first parameter is the desired gain level at the lower frequencies. This parameter is called A_L and defines the gain below the defined cut-off frequency. The second parameter is A_H . This defines the gain at the higher frequencies. The boost frequency, f_B , defines the attenuation at which the low frequency starts to roll off. The design engineer can define the desired attenuation level at the boost frequency. Depending on the overall gain distribution of the system the boost frequency is not the same as the cut off frequency with 3dB attenuation. The application circuit of the bass boost function is shown in Figure 12 below.

Figure 12:
Bass Boost Circuit



Bass Boost Definition: This figure shows the circuit diagram for the line input bass boost EQ circuit.

The component values for A_L can be calculated with the following formula:

$$A_L = \frac{R_2}{R_1} \dots [\text{dB}]$$

The component values for A_H can be calculated with the following formula:

$$A_H = \frac{R_2 \cdot R_3}{R_1 \cdot (R_2 + R_3)} \dots [\text{dB}]$$

An example for a typical bass boost is 6dB gain at the low frequency. If we select for R_1 a value of 10k Ω we can calculate R_2 as follows:

$$R_2 = 10^{\frac{A_L}{20}} \cdot R_1 = 10^{\frac{6}{20}} \cdot 10\text{k}\Omega = 20\text{k}\Omega$$

In this example, the gain for the higher frequency should be 0dB. This allows us to calculate R_3 as follows:

$$R_3 = \frac{-A_H \cdot R_1 \cdot R_2}{A_H \cdot R_1 - R_2} = \frac{-10^{\frac{0}{20}} \cdot 10\text{k}\Omega \cdot 20\text{k}\Omega}{10^{\frac{0}{20}} \cdot 10\text{k}\Omega - 20\text{k}\Omega} = 20\text{k}\Omega$$

The last component to be calculated for the example is capacitor C_1 . This capacitor defines the cut-off frequency of the bass boost circuit. The desired gain level $A_{\text{cut-off}}$ at the cut-off frequency can be defined by the engineer together with the frequency. In this example, we select a cut-off frequency of 400Hz and a gain level of 5dB. Thus we get an attenuation of 1dB at a frequency of 400Hz. The necessary capacitor can be calculated with the following formula:

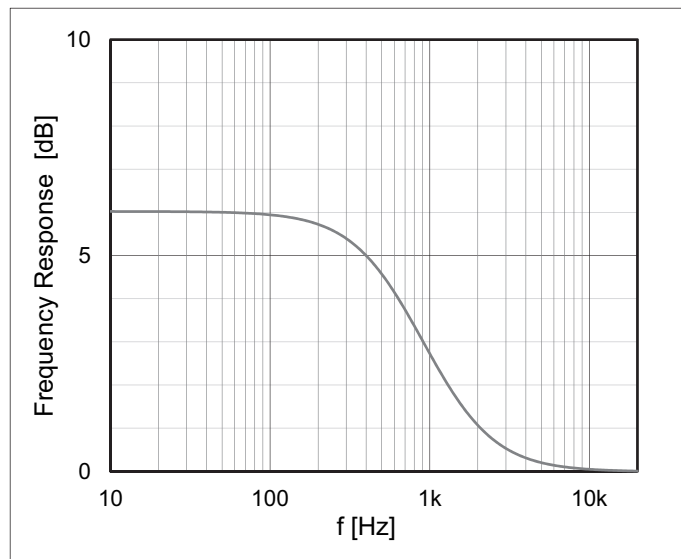
$$C_1 = \frac{\sqrt{R_2^2 - A_B^2 \cdot R_1^2}}{\sqrt{A_B^2 \cdot R_1^2 \cdot (R_2 + R_3)^2 \cdot (2 \cdot \pi \cdot f_B)^2 - R_2^2 \cdot R_3^2 \cdot (2 \cdot \pi \cdot f_B)^2}}$$

$$C_1 = \frac{\sqrt{20000^2 - 10^{\frac{5}{20}} \cdot 10000^2}}{\sqrt{\left(10^{\frac{5}{20}}\right)^2 \cdot 10000^2 \cdot (20000 + 20000)^2 \cdot 2 \cdot \pi \cdot 400 - 20000^2 \cdot 20000^2 \cdot 2 \cdot \pi \cdot 400}} = 6.3nF$$

The Spice simulation for the calculated resistor and capacitor values is shown in Figure 13. The simulation shows exactly at 400Hz an attenuation of 1dB.

Figure 13:
Frequency Response Bass Boost

Frequency Response Bass Boost: The diagram shows the Spice simulation result of the bass boost calculation example done in this chapter with $C_1=6.2nF$, $R_1=10k$, $R_2=20k\Omega$ and $R_3=20k\Omega$.



Parameter

$V_{BAT}=1.5V$, $T_A=25^{\circ}C$, $R_1=1k\Omega$, $R_2=1k\Omega$ unless otherwise specified

Figure 14:
Line Input Parameter

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|---------------------------------------|---|-----|---------------------|-----|------------|
| V_{LIN} | Input Signal Level | Gain=0dB | | $0.9 \cdot V_{BAT}$ | | V_{PEAK} |
| SNR | Signal to Noise Ratio | 10k Ω load, Gain = 0dB, $V_{BAT}=1.8V$, High Quality Mode | | 121 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.5V$ High Quality Mode | | 119 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.0V$ High Quality Mode | | 115 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.8V$, ECO Mode | | 115 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.5V$, ECO Mode | | 113 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.0V$, ECO Mode | | 109 | | dB |
| I_{LIN} | Block Current Consumption | No load, Gain = 0dB, $V_{BAT}=1.8V$, High Quality Mode | | 1.4 | | mA |
| | | No load, Gain = 0dB, $V_{BAT}=1.5V$, High Quality Mode | | 1.3 | | mA |
| | | No load, Gain = 0dB, $V_{BAT}=1.0V$, High Quality Mode | | 1.1 | | mA |
| | | No load, Gain = 0dB, $V_{BAT}=1.8V$, ECO Mode | | 1.1 | | mA |
| | | No load, Gain = 0dB, $V_{BAT}=1.5V$, ECO Mode | | 950 | | μA |
| | | No load, Gain = 0dB, $V_{BAT}=1.0V$, ECO Mode | | 700 | | μA |
| $V_{NOISE-A}$ | Input Referred Noise Floor A-Weighted | High Quality Mode | | 900 | | nV |
| | | ECO Mode | | 1.9 | | μV |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------|------------|-----|-----|-----|------------|
| V_{offset} | DC offset voltage | | | | 2 | mV |
| C_L | Load Capacitance | | | | 100 | pF |
| R_L | Load Impedance | | 1 | | | k Ω |

Line Input Parameter: This table shows the detailed electrical characteristics of the line input gain stage like maximum input signal level and audio parameter like SNR.

Figure 15:
Line Input Frequency Response

Line Input Frequency Response: The diagram shows the frequency response measurement of the line input amplifier with 0dB gain and $V_{\text{BAT}}=1.5\text{V}$, $R_1=10\text{k}\Omega$ and $R_2=10\text{k}\Omega$. The solid line represents the default high quality mode and the dashed line shows the frequency response in ECO mode.

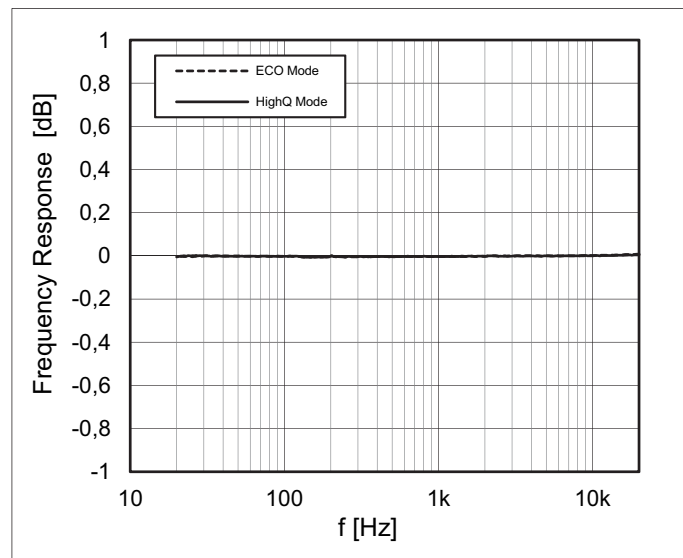
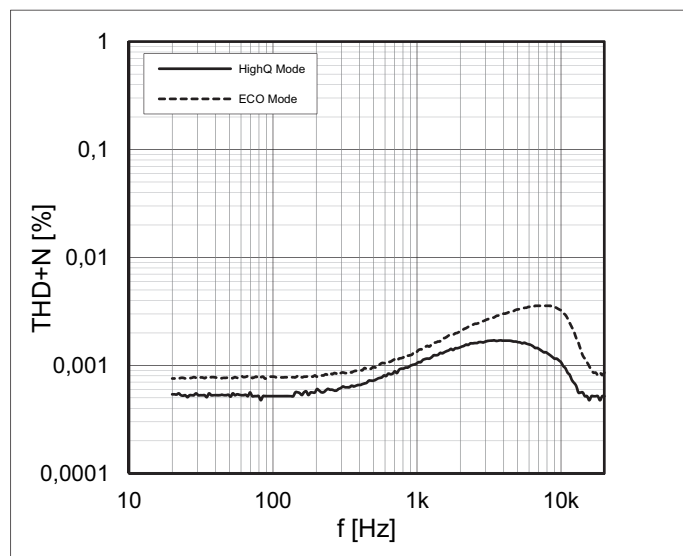


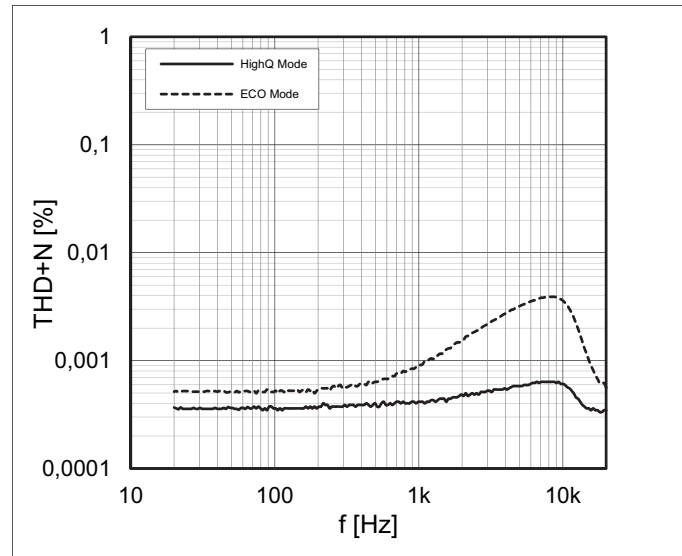
Figure 16:
Line Input THD+N vs. Frequency $V_{\text{BAT}} = 1\text{V}$

Line Input THD+N vs. Frequency: The diagram shows the A-weighted THD+N measurement of the line input amplifier with 0dB gain and $V_{\text{BAT}}=1.0\text{V}$, $R_1=10\text{k}\Omega$ and $R_2=10\text{k}\Omega$. The solid line represents the default high quality mode and the dashed line shows the frequency response in ECO mode.



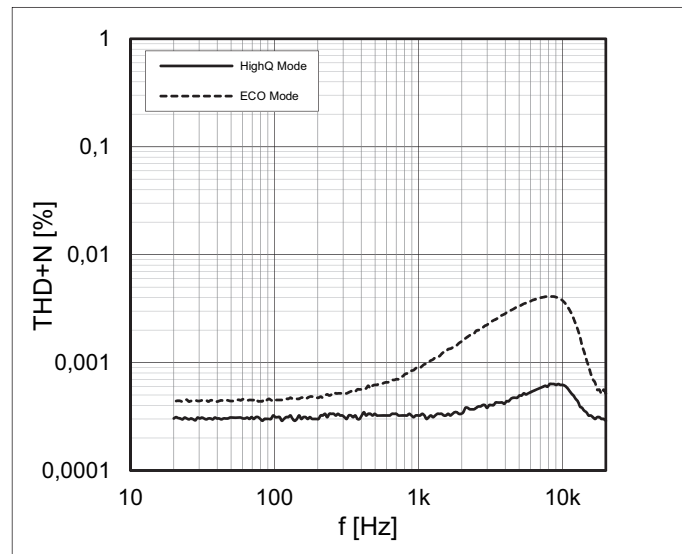
Line Input THD+N vs. Frequency: The diagram shows the A-weighted THD+N measurement of the line input amplifier with 0dB gain and $V_{BAT}=1.5V$, $R_1=10k\Omega$ and $R_2=10k\Omega$. The solid line represents the default high quality mode and the dashed line shows the frequency response in ECO mode.

Figure 17:
Line Input THD+N vs. Frequency $V_{BAT} = 1.5V$



Line Input THD+N vs. Frequency: The diagram shows the A-weighted THD+N measurement of the line input amplifier with 0dB gain and $V_{BAT}=1.8V$, $R_1=10k\Omega$ and $R_2=10k\Omega$. The solid line represents the default high quality mode and the dashed line shows the frequency response in ECO mode.

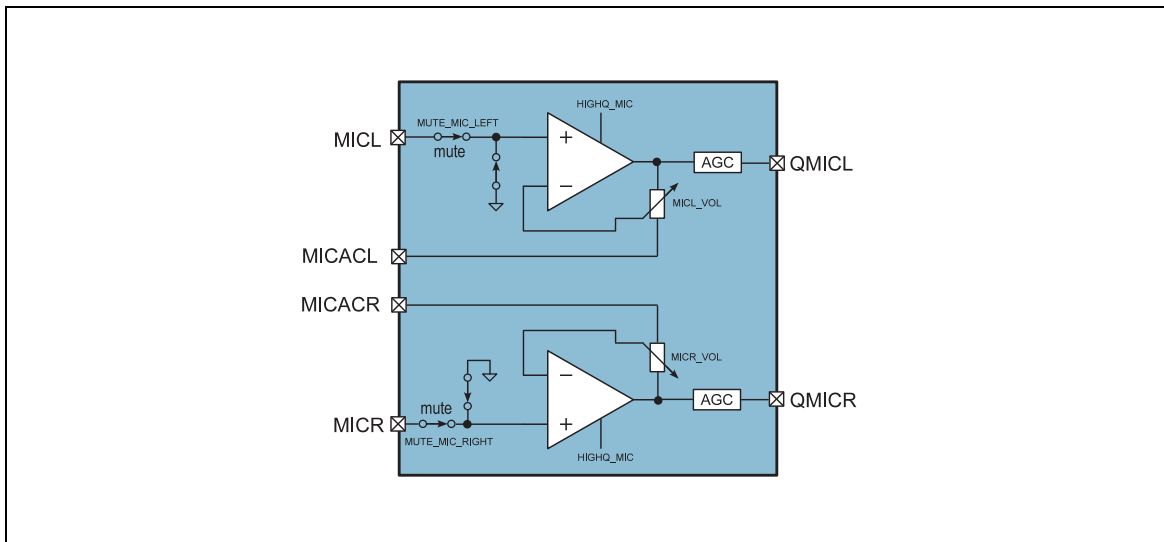
Figure 18:
Line Input THD+N vs. Frequency $V_{BAT} = 1.8V$



Microphone Inputs

The AS3415/35 offers two low noise microphone inputs with full digital control and a dedicated DC offset cancellation pin for each microphone input. In total each gain stage offers up to 63 gain steps of 0.5dB resulting in a gain range from 0dB to +31dB. The microphone gain is stored digitally during production, in OTP on the ANC chipset. Besides the standard microphone gain register for left and right channel, the chip also features two additional microphone gain registers for monitor mode. Thus, in monitor mode, a completely different gain setting for left and right microphone can be selected to implement voice filter functions to amplify the speech band for better intelligibility.

Figure 19:
Stereo Microphone Input



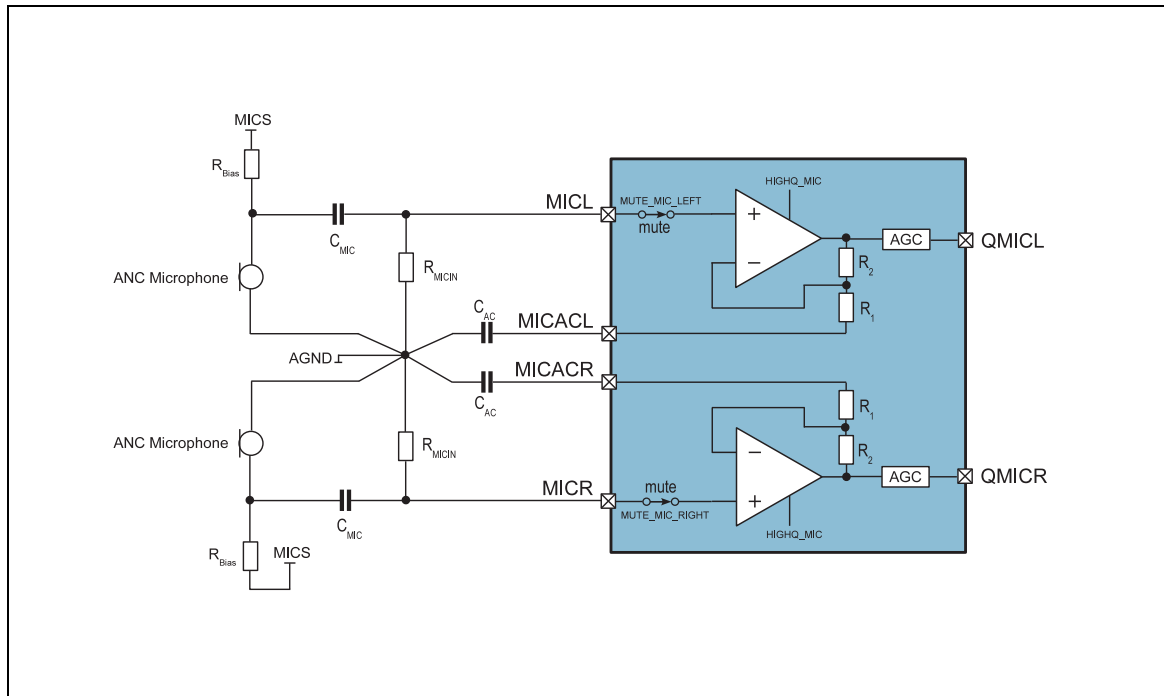
Stereo Microphone Input: This diagram shows the internal structure of the stereo microphone preamplifier including the mute switch as well as the automatic gain control (AGC).

To avoid unwanted start-up pop noise, a soft-start function is implemented for an automatic gain ramping of the device. In case of an overload condition on the microphone input (e.g. high sound pressure level), an internal state machine reduces the microphone gain automatically. For some designs it might be useful to switch off this feature. Especially in feed-back systems very often infrasound can cause an overload condition of the microphone preamplifier which results in low frequency noise which can be avoided by disabling the AGC.

Input Capacitor Selection

The microphone preamplifier needs a bias resistor (R_{Bias}) per channel as well as DC blocking capacitors (C_{MIC}). The capacitors C_{AC} are DC blocking capacitors to avoid DC amplification of the non-inverting microphone preamplifier. This capacitor has an influence on the frequency response because the internal feedback resistors create a high pass filter. The typical application circuit is shown in [Figure 20](#) with all necessary components.

Figure 20:
Microphone Capacitor Selection Circuit



Microphone Capacitor Selection Circuit: This diagram shows a typical microphone application circuit with all necessary components to operate the amplifier.

The corner frequency of this high pass filter is defined with the capacitor C_{AC} and the gain of the headphone amplifier.

[Figure 21](#) shows an overview of typical cut-off frequencies with different microphone gain settings.

Figure 21:
Microphone Cut-Off Frequency Overview

| Microphone Gain | R_1 | R_2 | $F_{cut-off}$ |
|-----------------|----------------|----------------|---------------|
| 0dB | 22.2k Ω | 0 Ω | 1.7Hz |
| 3dB | 15716 Ω | 6484 Ω | 1.9Hz |
| 6dB | 11126 Ω | 11074 Ω | 2.2Hz |

| Microphone Gain | R ₁ | R ₂ | F _{cut-off} |
|-----------------|----------------|----------------|----------------------|
| 9dB | 7877Ω | 14323Ω | 2.7Hz |
| 12dB | 5576Ω | 16623Ω | 3.5Hz |
| 15dB | 3948Ω | 18252Ω | 4.5Hz |
| 18dB | 2795Ω | 19405Ω | 6.1Hz |
| 21dB | 1979Ω | 20221Ω | 8.4Hz |
| 24dB | 1400Ω | 20800Ω | 11.5Hz |
| 27dB | 992Ω | 21208Ω | 16.3Hz |
| 30dB | 702Ω | 21498Ω | 22.7Hz |

Microphone Cut-Off frequency overview: This table shows an overview of the different cut-off frequencies with C_{AC}=10μF, C_{MIC}= 2.2μF and R_{MICIN}=22kΩ of the microphone preamplifier.

In the cut-off frequency overview, capacitor C_{AC} was defined as 10μF which results in a rather low cut-off frequency for best ANC filter design. If a different capacitor value is desired in the application, the following formula defines the transfer function of the high pass circuit of the microphone preamplifier:

$$|A| = \frac{\sqrt{4 \cdot C_{AC}^2 \cdot f^2 \cdot (R_1 + R_2)^2 \cdot \pi^2 + 1}}{\sqrt{4 \cdot C_{AC}^2 \cdot f^2 \cdot R_1^2 \cdot \pi^2 + 1}}$$

Filter Simulations:

It is important when doing the ANC filter simulations to include all microphone filter components to incorporate the gain and phase influence of these components.

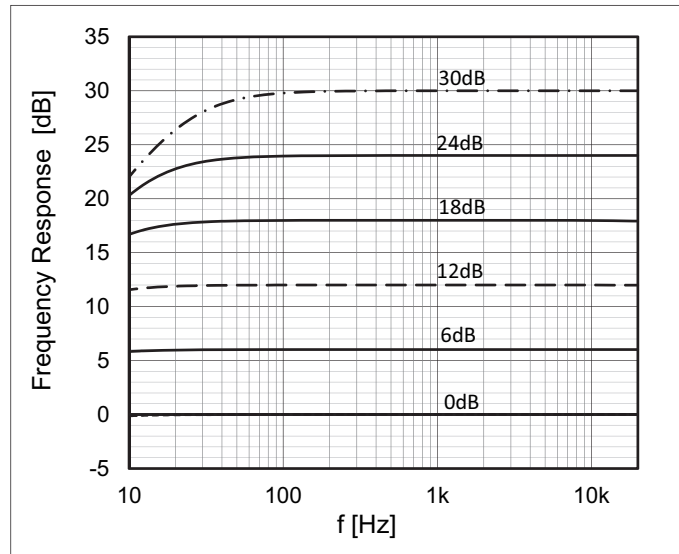
The simplified transfer function does not include the high pass filter defined by C_{MIC} and R_{MICIN}. With the recommended values of 2.2μF for C_{MIC} and 22kΩ for R_{MICIN} this filter can be neglected because of the very low cut-off frequency of 1.5Hz. The cut-off frequency for this filter can be calculated with the following formula:

$$f_{cut-off} = \frac{1}{2 \cdot \pi \cdot R_{MICIN} \cdot C_{MIC}}$$

The simulated frequency response for the microphone preamplifier with the recommended component values is shown in [Figure 22](#).

Figure 22:
Simulated Microphone Frequency Response

Microphone Frequency Response: This graph shows the frequency response of the microphone preamplifier with different gain settings with $C_{AC}=10\mu\text{F}$, $C_{MIC}=2.2\mu\text{F}$ and $R_{MICIN}=22\text{k}\Omega$.



In application with PCB space limitations it is also possible to remove the capacitors C_{AC} and connect MICACL and MICACR pins directly to A_{GND} . In this configuration AC coupling of the QMICR and QMICL signals is recommended.

Parameter

$V_{BAT}=1.5V$, $T_A=25^{\circ}C$, $C_{AC}=10\mu F$, $C_{MIC}=2.2\mu F$ and $R_{MICIN}=22k\Omega$ unless otherwise specified.

Figure 23:
Microphone Parameter

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------|---|-----|------|-----|------------|
| V_{MICIN0} | Input Signal Level | $A_{MIC} = 10dB$ | | 80 | | mV_{RMS} |
| V_{MICIN1} | | $A_{MIC} = 20dB$ | | 40 | | mV_{RMS} |
| V_{MICIN2} | | $A_{MIC} = 30dB$ | | 10 | | mV_{RMS} |
| SNR | Signal to Noise Ratio | 0dB gain, High quality mode, AGC off | | 115 | | dB |
| | | 10dB gain, High quality mode, AGC off | | 108 | | dB |
| | | 20dB gain, High quality mode, AGC off | | 98 | | dB |
| | | 0dB gain, ECO mode, AGC off | | 113 | | dB |
| | | 10dB gain, ECO mode, AGC off | | 105 | | dB |
| | | 20dB gain, ECO mode, AGC off | | 96 | | dB |
| $V_{NOISE-A}$ | A-Weighted Output Noise Floor | 0dB gain, 20Hz – 20kHz bandwidth, High quality | | 1.3 | | μV |
| | | 10dB gain, 20Hz – 20kHz bandwidth, High quality | | 4.2 | | μV |
| | | 20dB gain, 20Hz – 20kHz bandwidth, High quality | | 13 | | μV |
| | | 0dB gain, 20Hz – 20kHz bandwidth, ECO mode | | 1.6 | | μV |
| | | 10dB gain, 20Hz – 20kHz bandwidth, ECO mode | | 5.5 | | μV |
| | | 20dB gain, 20Hz – 20kHz bandwidth, ECO mode | | 16.5 | | μV |
| I_{MIC} | Block Current Consumption | No load, normal mode | | 1.4 | | mA |
| | | No load, ECO mode | | 1 | | mA |
| A_{MIC} | Programmable Gain | Discrete logarithmic gain steps | 0 | | +31 | dB |
| | Gain Step Size | | | 0.5 | | dB |
| | Gain Step Precision | | | | 0.2 | dB |
| ΔA_{MIC} | Gain Ramp Rate | V_{PEAK} related to V_{BAT} or V_{NEG} | | 1 | | ms/step |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|--------------------------|---|-----|------|-----|---------------------------|
| V_{ATTACK} | Limiter Activation Level | V_{PEAK} related to V_{BAT} or V_{NEG} 64 @ 0.5dB | | 0.67 | | 1 |
| V_{DECAY} | Limiter Release Level | | | 0.4 | | 1 |
| A_{MICLIMIT} | Limiter Minimum Gain | | | 0 | | dB |
| t_{ATTACK} | Limiter Attack Time | | | 5 | | $\mu\text{s}/\text{step}$ |
| t_{DECAY} | Limiter Decay Time | | | 1 | | ms/step |

Microphone Parameter: This table shows the detailed electrical characteristics of the microphone preamplifier gain stage.

Figure 24:
Microphone Frequency Response

Microphone Frequency Response: This graph shows the frequency response of the microphone preamplifier with different gain settings without R_{MICIN} resistor, C_{AC} capacitor (MICACx pin connected to A_{GND}) and $C_{\text{MIC}}=2.2\mu\text{F}$.

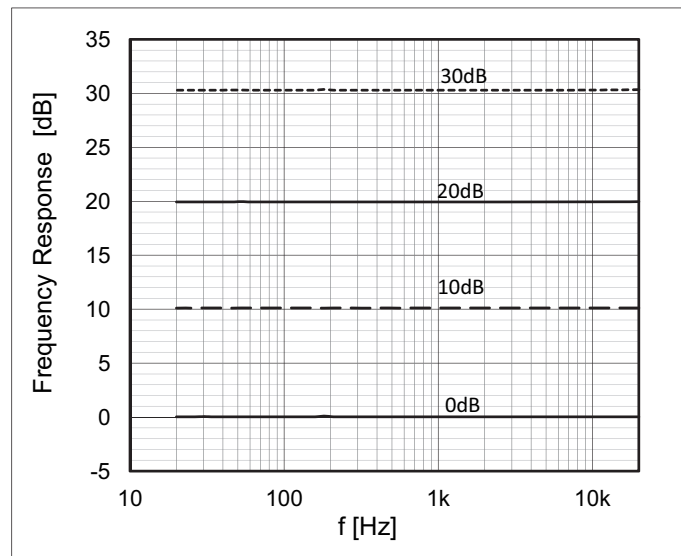


Figure 25:
Microphone THD+N vs. V_{input}

Microphone THD+N vs. V_{input} : This graph shows the A-weighted THD+N versus input voltage of the microphone preamplifier with 0dB gain and $V_{BAT}=1.5V$.

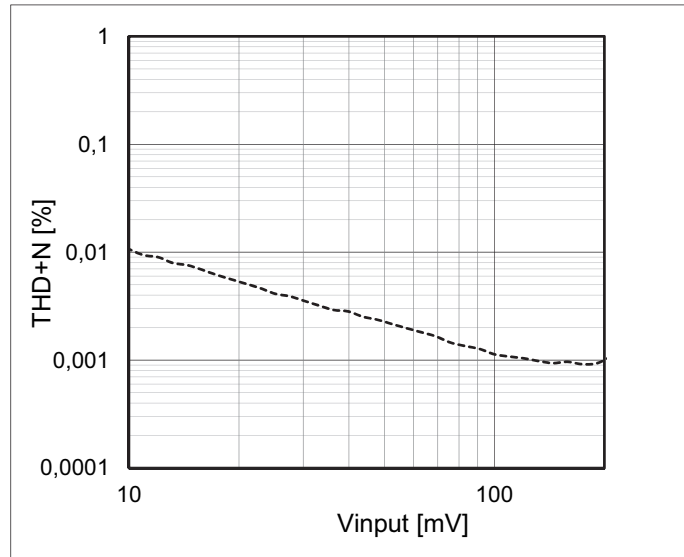
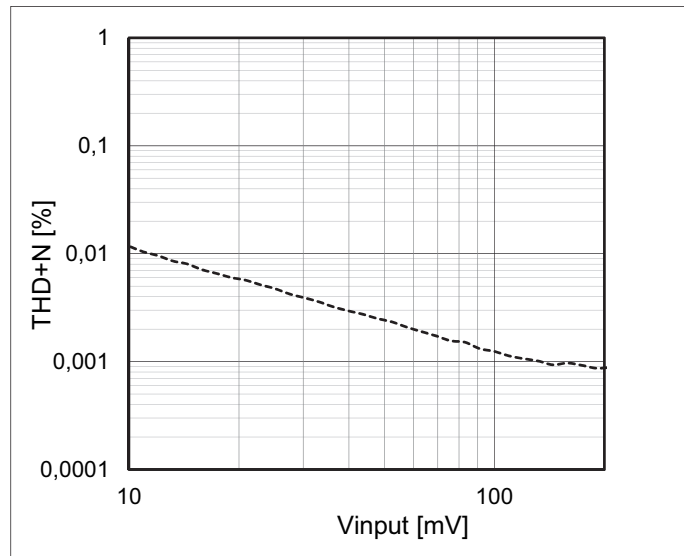


Figure 26:
Microphone THD+N vs. V_{input} ECO Mode

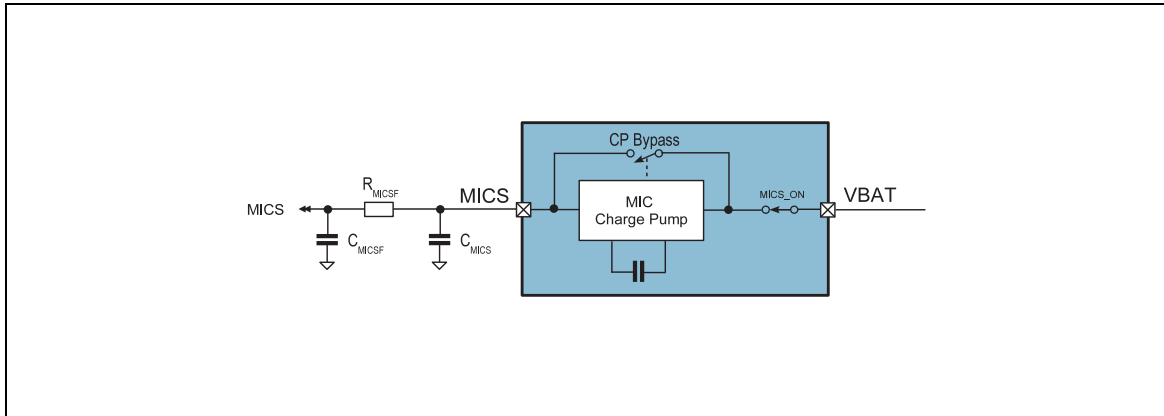
Microphone THD+N vs. V_{input} : This graph shows the A-weighted THD+N versus input voltage of the microphone preamplifier with 0dB gain and $V_{BAT}=1.5V$. The amplifier runs in ECO mode.



Microphone Supply

The AS3415/35 features an integrated microphone supply charge pump. This charge pump provides the proper microphone supply voltage for a single cell battery supply (1.5V). Since AAA batteries can operate down to 1.0V, the direct battery voltage cannot be used for microphone supply. This would reduce the sensitivity of the microphone dramatically.

Figure 27:
Microphone Supply



Microphone Supply: This block diagram shows how the integrated microphone supply works including all options for configuration like off mode and bypass mode.

Bypass Switch Operation:
When using the integrated music bypass switch you must not switch off the microphone supply!

Therefore the integrated charge pump generates a microphone supply voltage which is typically 2.7V. In case the ANC chipset is supplied with a fixed voltage e.g. 1.8V the integrated charge pump supports a mode which allows the designer to directly connect the microphone supply pin to the chip supply voltage. This can help to reduce total power consumption of the system. A third mode is available to switch off the microphone supply. This use case can occur if the headset is operated without ANC function. Please mind that you must not switch off the microphone supply at all if the integrated music bypass function is in use. The microphone supply voltage is also used to switch off the integrated music bypass switch if the AS3415/35 is in active mode.

Parameter

$V_{BAT}=1.5V$, $T_A=25^{\circ}C$, $C_{MICS} = 10\mu F$, $C_{MICSF} = 22\mu F$ and $R_{MICSF} = 220\Omega$ unless otherwise specified.

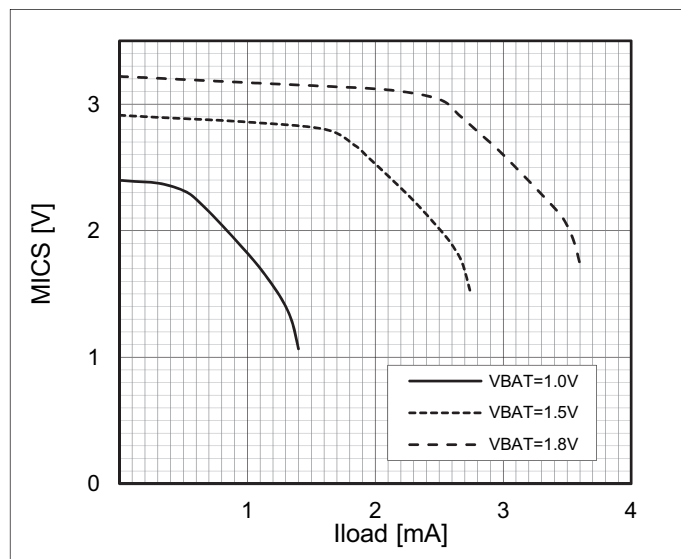
Figure 28:
Microphone Supply Parameter

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|-----------------------------|---|-----|-----|-----|---------|
| V_{MICS} | Microphone Supply Voltage | $V_{BAT} = 1.8V$, no load | | 3.2 | | V |
| | | $V_{BAT} = 1.5V$, no load | | 2.9 | | V |
| | | $V_{BAT} = 1.0V$, no load | | 2.4 | | V |
| I_{MICS} | Block Current Consumption | $V_{BAT} = 1.8V$, no load | | 500 | | μA |
| | | $V_{BAT} = 1.5V$, no load | | 410 | | μA |
| | | $V_{BAT} = 1.0V$, no load | | 300 | | μA |
| $I_{typ.}$ | Typical current consumption | 500 μA load | | 1.9 | | mA |
| $V_{Noise-A}$ | Microphone Supply Noise | A-Weighted, 500 μA load | | 1.1 | | μV |
| | | A-Weighted, 500 μA load, only C_{MICS} assembled | | 5,3 | | μV |

Microphone Supply Parameter: This table shows the detailed electrical characteristics of the microphone supply.

Figure 29:
Microphone Supply Load Characteristic

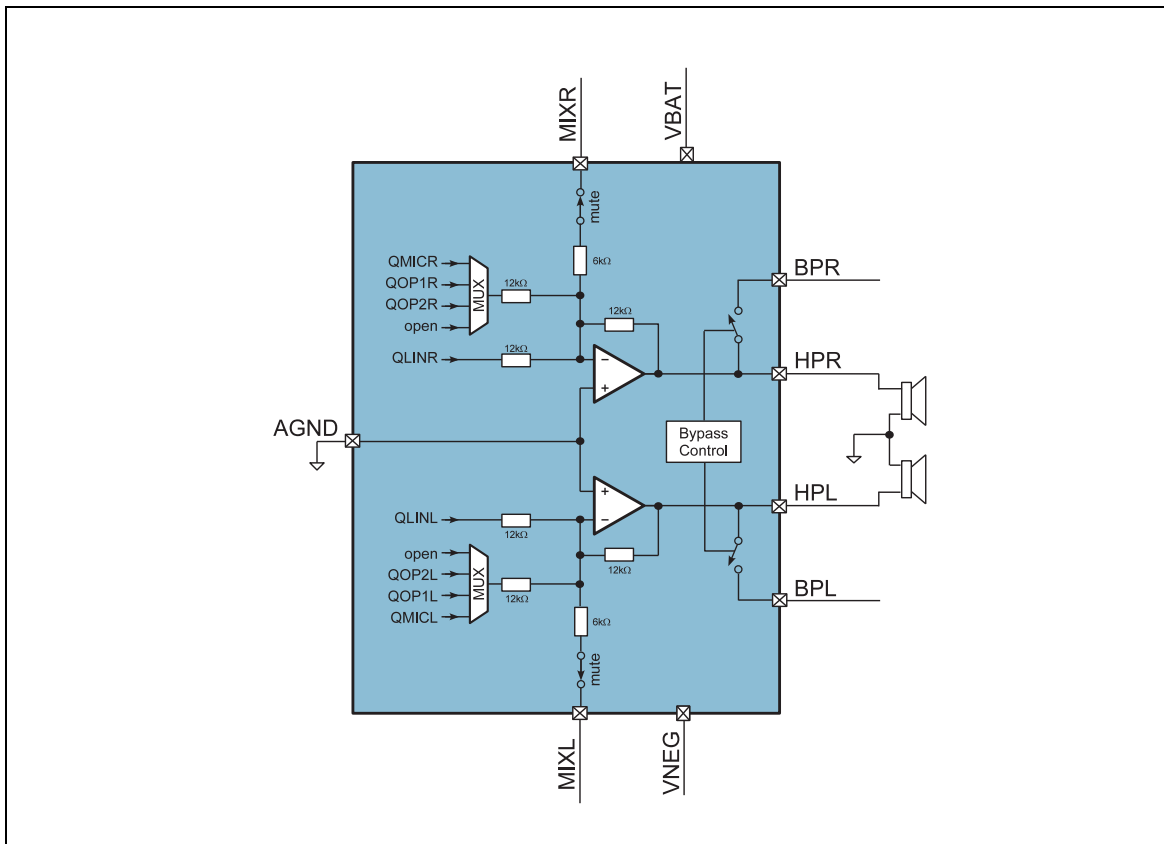
Microphone Supply Load Characteristic: This diagram shows output voltage of the microphone supply vs. output load on the microphone supply.



Headphone Amplifier

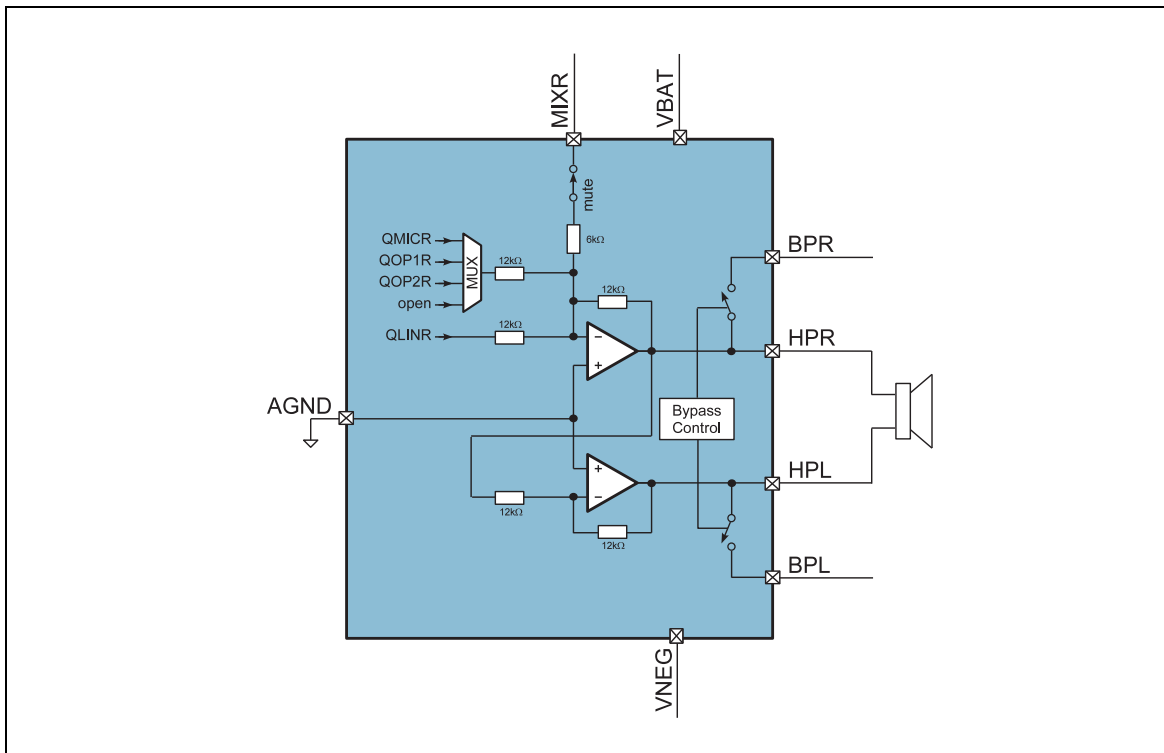
The headphone amplifier is a true ground output using V_{NEG} as negative supply. It is designed to provide the audio signal with $2 \times 34\text{mW} @ 32\Omega$. For higher output requirements, the headphone amplifier is also capable of operating in bridged mode. In this mode the left output is carrying the inverted signal of the right output shown in Figure 30. With a V_{BAT} voltage of 1.8V, a maximum output power of 120mW can be achieved in this mode. This is especially required for over ear headsets with hybrid ANC topology or any other headset with high output power requirements. The amplifier itself features various input sources. The line input signal is directly connected to the headphone amplifier. In case the application requires more complex music filtering the line input connection can be disabled and the mixer inputs MIXR and MIXL can be used to feed the music signal to the headphone amplifier. The mixer inputs have a $6\text{k}\Omega$ input resistance which gives a typical gain of 6dB with the internal $12\text{k}\Omega$ feedback resistor of the headphone amplifier. The input multiplexer supports four different input signals which can be configured according to complexity of the ANC filter.

Figure 30:
Headphone Amplifier Single Ended



Headphone Amplifier: This figure shows the block diagram of the headphone amplifier including the integrated music bypass switches as well as the summation input of the amplifier in single ended configuration.

Figure 31:
Headphone Amplifier Differential



Headphone Amplifier: This figure shows the block diagram of the headphone amplifier including the integrated music bypass switches as well as the summation input of the amplifier in differential output mode.

Parameter

$V_{BAT}=1.5V$, $T_A= 25^{\circ}C$, unless otherwise specified.

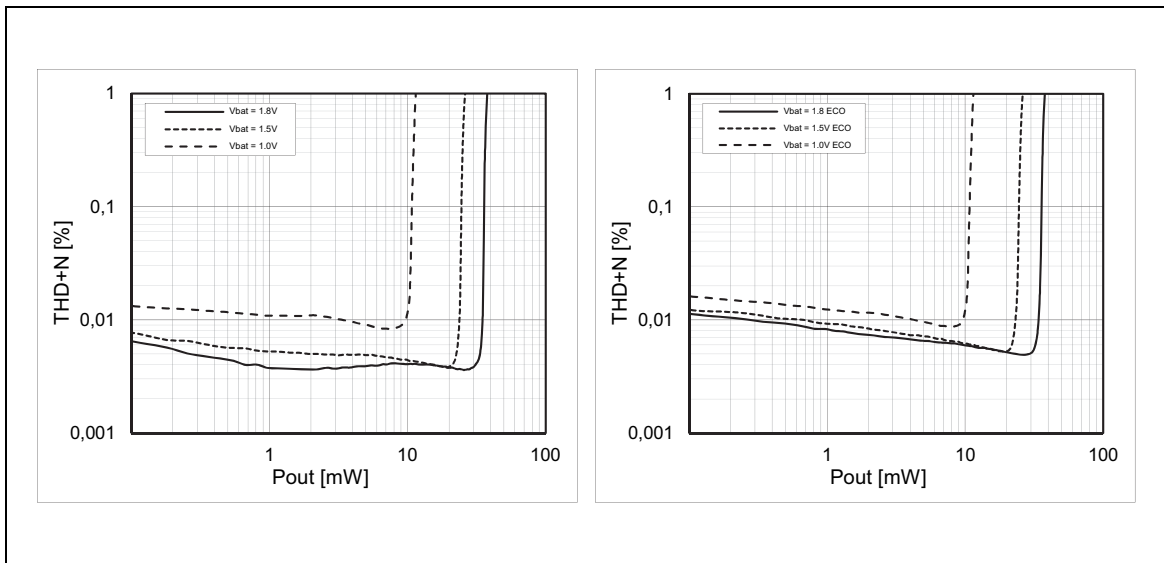
Figure 32:
Headphone Amplifier Parameter

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|----------------------------------|-------------------------------------|-----|-----|-----|----------|
| R_{L_HP} | Load Impedance | Stereo mode | 16 | 32 | | Ω |
| C_{L_HP} | Load Capacitance | Stereo mode | | | 100 | pF |
| P_{HP} | Nominal Output Power Stereo Mode | $V_{BAT} = 1.8V$, 32 Ω load | | 35 | | mW |
| | | $V_{BAT} = 1.5V$, 32 Ω load | | 24 | | mW |
| | | $V_{BAT} = 1.0V$, 32 Ω load | | 10 | | mW |
| | | $V_{BAT} = 1.8V$, 16 Ω load | | 60 | | mW |
| | | $V_{BAT} = 1.5V$, 16 Ω load | | 40 | | mW |
| | | $V_{BAT} = 1.0V$, 16 Ω load | | 16 | | mW |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|--|--|-----|-----|-----|------|
| P _{HP_BRIDGE} | Nominal Output Power Differential Mode | V _{BAT} = 1.8V, 32Ω load | | 110 | | mW |
| | | V _{BAT} = 1.5V, 32Ω load | | 75 | | mW |
| | | V _{BAT} = 1.0V, 32Ω load | | 30 | | mW |
| | | V _{BAT} = 1.8V, 16Ω load | | 150 | | mW |
| | | V _{BAT} = 1.5V, 16Ω load | | 100 | | mW |
| | | V _{BAT} = 1.0V, 16Ω load | | 35 | | mW |
| I _{HPH} | Supply current | Normal mode | | 2.4 | | mA |
| | | ECO mode | | 2 | | mA |
| P _{SRRHP} | Power Supply Rejection Ratio | 1 kHz | | 100 | | dB |
| SNR | Signal to Noise Ration | High Quality Mode, 0dB gain via MIXx input pin, 32Ω load | | 112 | | dB |
| | | ECO Mode, 0dB gain via MIXx input pin, 32Ω load | | 110 | | dB |
| Channel Separation | | 32Ω load | | -87 | | dB |
| V _{Noise-A} | Output Noise Floor A-Weighted | High Quality Mode, 32Ω load, HP_MUX = nc, Mixer input disabled, 0dB gain | | 2.8 | | μV |
| | | ECO Mode, 32Ω load, HP_MUX = nc, Mixer input disabled, 0dB gain | | 3.3 | | μV |

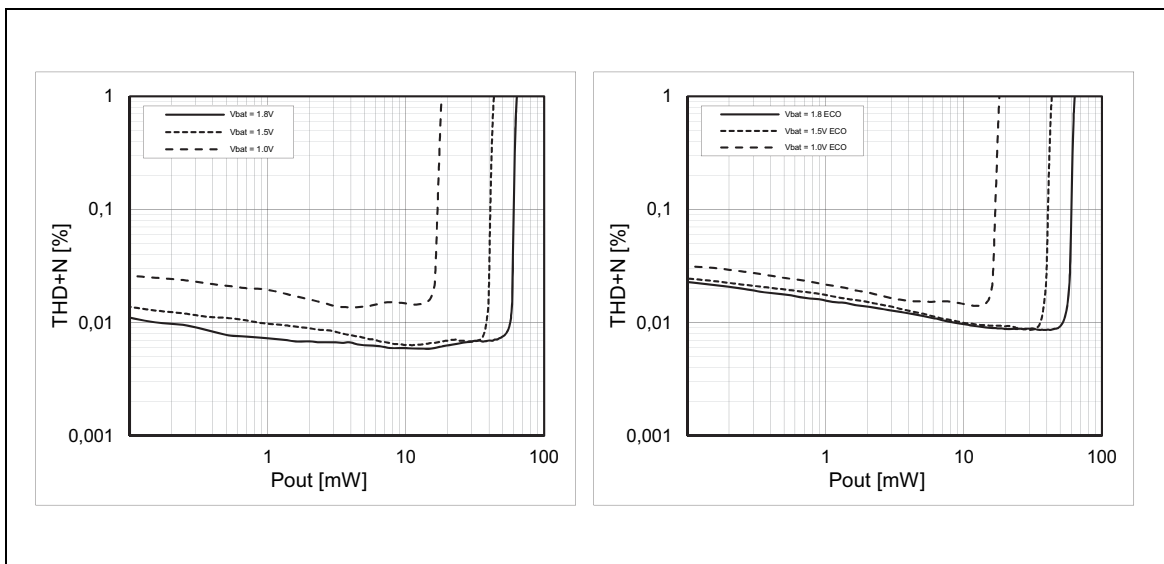
Headphone Parameter: This table shows the detailed electrical characteristics of the headphone amplifier like output power, SNR and channel separation.

Figure 33:
Headphone THD+N vs. Output Power 32Ω Stereo



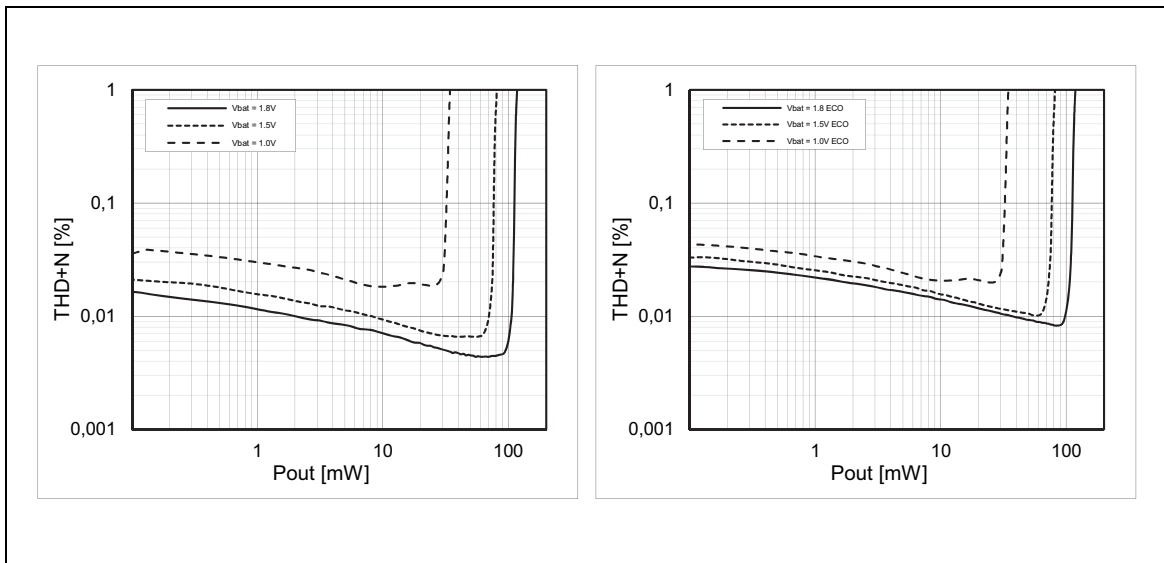
Headphone THD+N vs. Output Power: These figures shows the THD+N measurements of the headphone amplifier with different supply voltages in normal mode and ECO mode. The selected amplifier gain is 0dB with 32Ω load.

Figure 34:
Headphone THD+N vs. Output Power 16Ω Stereo



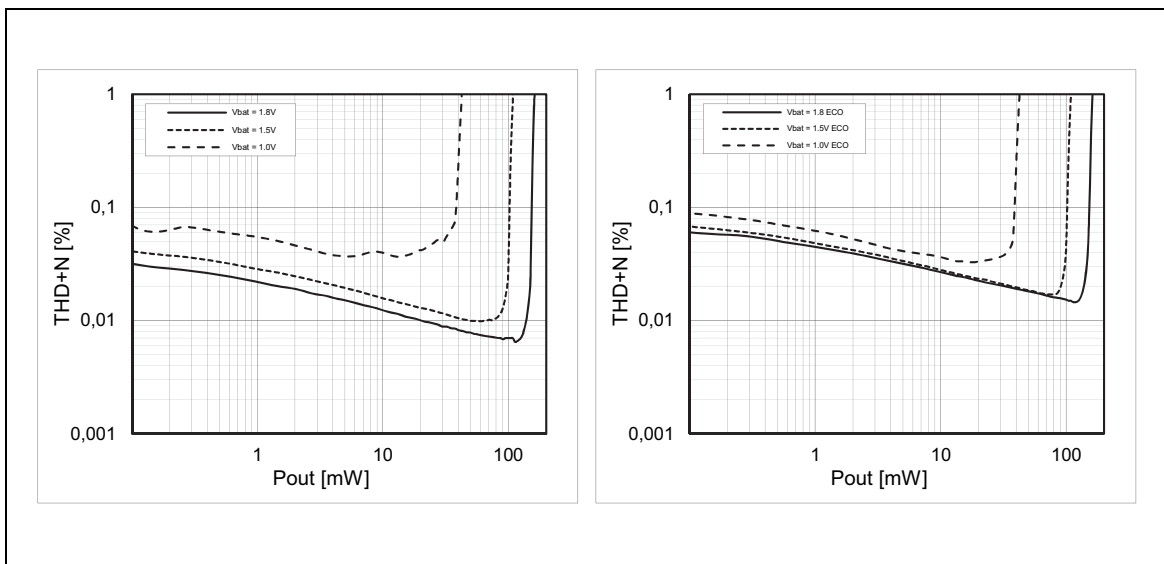
Headphone THD+N vs. Output Power: These figures shows the THD+N measurements of the headphone amplifier with different supply voltages in normal mode and ECO mode. The selected amplifier gain is 0dB with 16Ω load.

Figure 35:
Headphone THD+N vs. Output Power 32Ω Mono



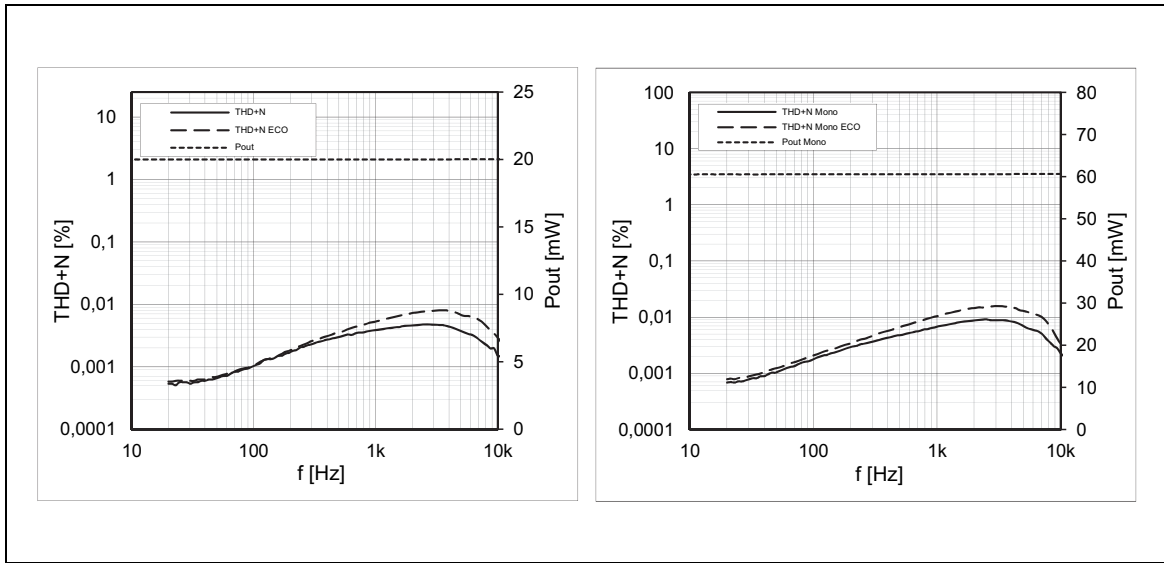
Headphone THD+N vs. Output Power: These figures show the A-weighted THD+N measurements of the headphone amplifier with different supply voltages in normal mode and ECO mode. The selected amplifier gain is 0dB with 32Ω load in mono configuration.

Figure 36:
Headphone THD+N vs. Output Power 16Ω Mono



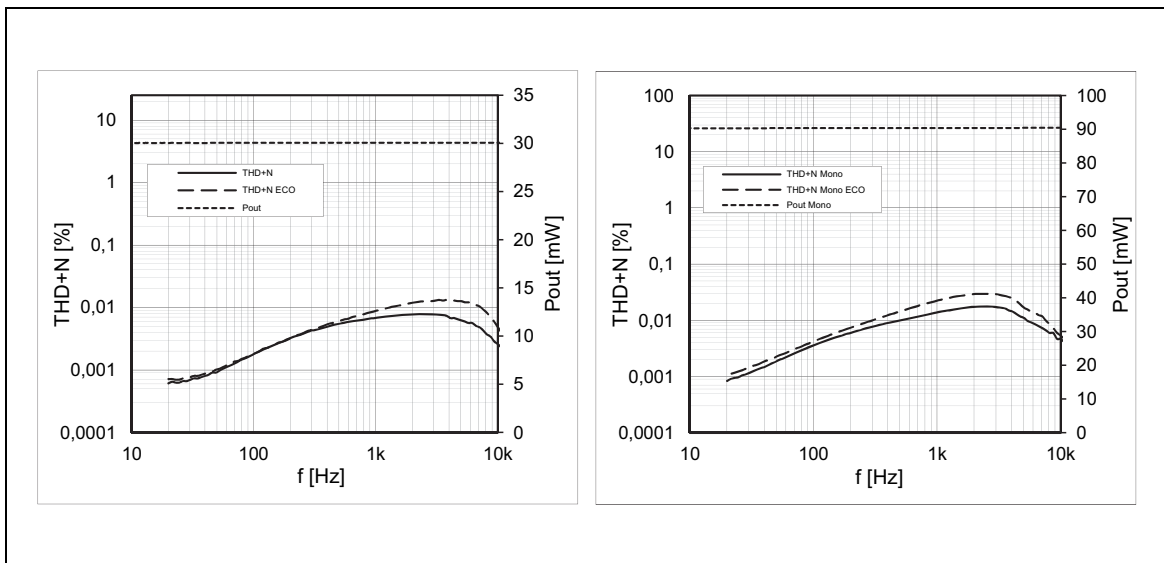
Headphone THD+N vs. Output Power: These figures show the A-weighted THD+N measurements of the headphone amplifier with different supply voltages in normal mode and ECO mode. The selected amplifier gain is 0dB with 16Ω load in mono configuration.

Figure 37:
Headphone THD+N vs. Frequency 32Ω



Headphone THD+N vs. Frequency: These figures shows the A-weighted THD+N measurements over frequency in stereo and mono differential mode. The amplifier gain is 0dB and the load in both modes is 32Ω.

Figure 38:
Headphone THD+N vs. Frequency 16Ω



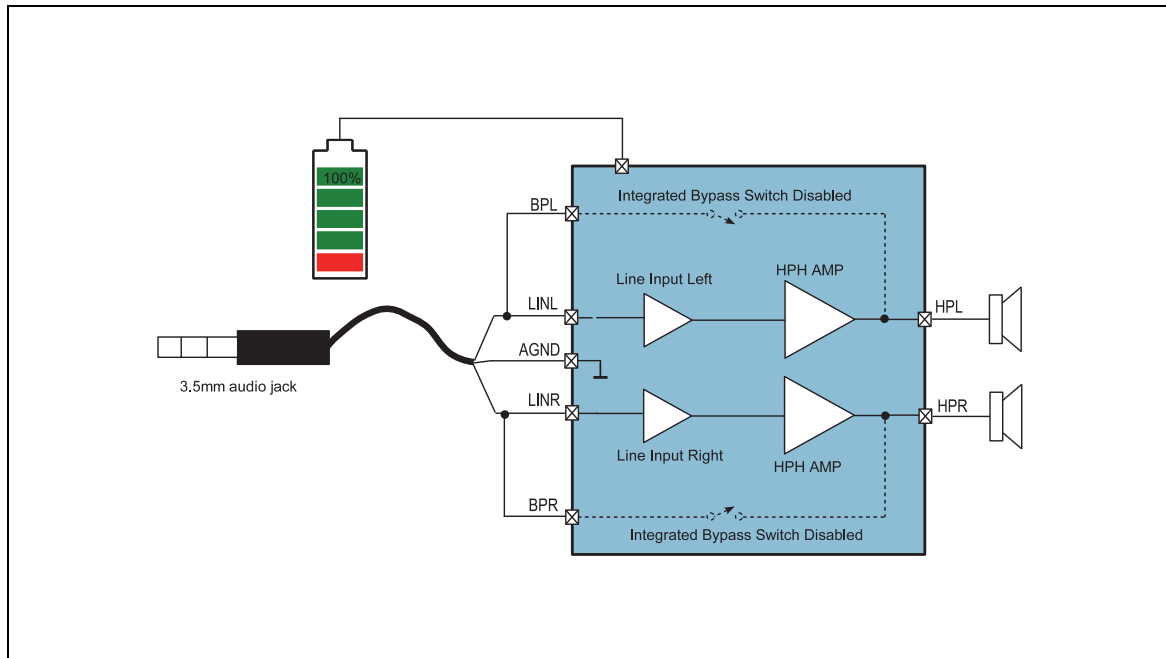
Headphone THD+N vs. Frequency: These figures shows the A-weighted THD+N measurements over frequency in stereo and mono differential mode. The amplifier gain is 0dB and the load in both modes is 16Ω.

Integrated Music Bypass Switch

If the AS3415/35 is switched off the device features a unique feature which is integrated bypass switches. These switches can be used in place of a mechanical switch to bypass the ANC chipset in off mode or if the headset runs out of battery.

Figure 39 shows the basic music playback path of the AS3415/35 with a full battery. In this mode the line input amplifier is enabled as well as the headphone amplifier. The integrated bypass switches are disabled if the device is powered.

Figure 39:
Bypass Mode Inactive

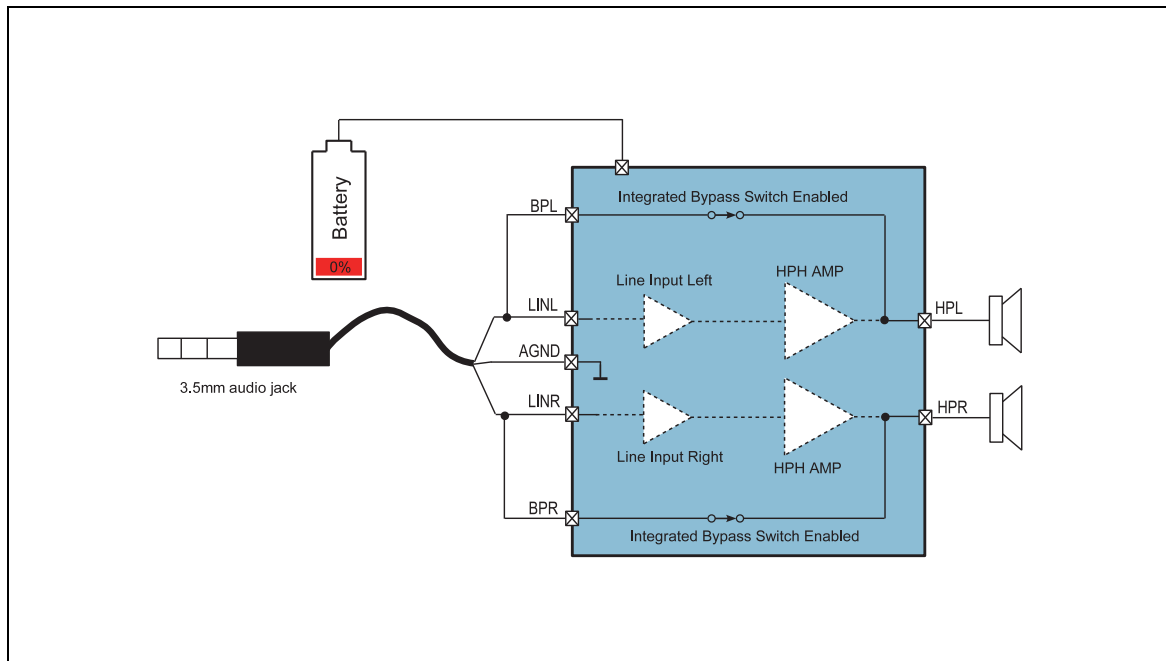


Bypass Mode Inactive: This block diagram shows the general music playback path of AS3515/35 with the integrated music bypass switches disabled.

Integrated Bypass Switch:
The integrated bypass switch works even without any battery connected to the device. It helps to reduce BOM costs and PCB area. Furthermore it facilitates new industrial designs to ANC solutions.

Figure 40 shows the AS3415/35 in off mode with an empty battery. This is basically the same use case as no battery at all. In this mode the internal bypass switch becomes active. The line input amplifier and the headphone amplifier are not powered because the headset has run out of battery and the bypass switch is active. Thus the music signal coming from the 3.5mm audio jack is routed through the ANC chipset without any power source connected to the device.

Figure 40:
Bypass Mode Active



Bypass Mode Inactive: This block diagram shows the general music playback path of AS3515/35 with the integrated music bypass switches enabled. The device has no supply any more but music playback is still possible via the internal bypass switches.

Parameter

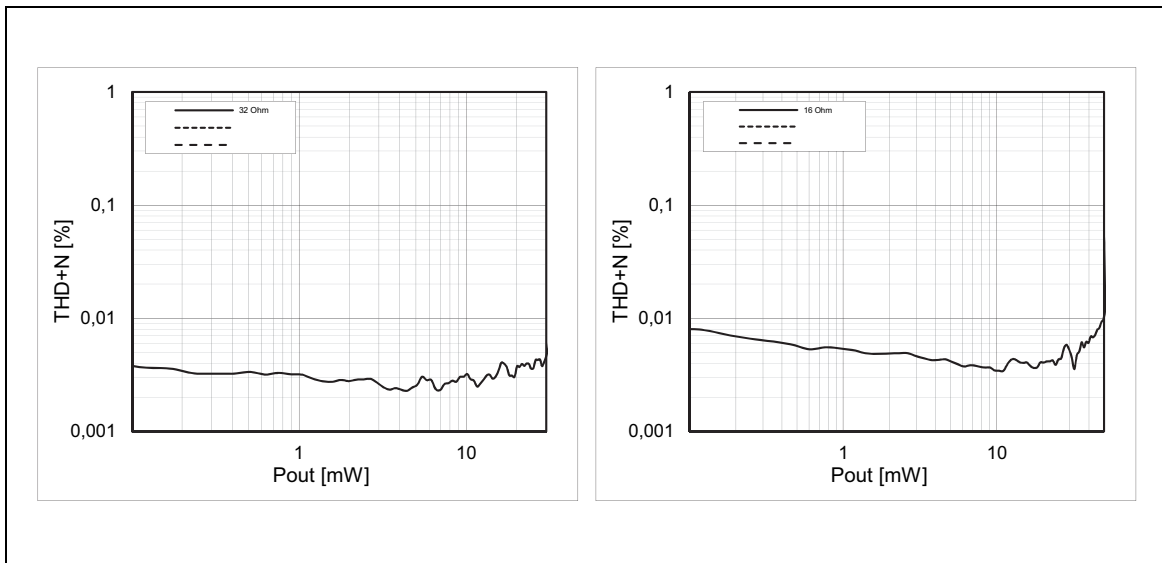
$V_{BAT}=1.5V, T_A=25^{\circ}C$, unless otherwise specified.

Figure 41:
Bypass Switch Parameter

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|---------------------------|-------------------------------------|-----|-----|-----|----------|
| R_{Switch} | Impedance | Power down | | 1.2 | | Ω |
| THD | Total Harmonic Distortion | 0dBV input signal, 32 Ω load | | -90 | | dB |
| | | 0dBV input signal, 16 Ω load | | -80 | | dB |

Bypass Switch Parameter: This table shows the detailed electrical characteristics of the integrated bypass switch.

Figure 42:
Bypass THD+N vs. Output Power

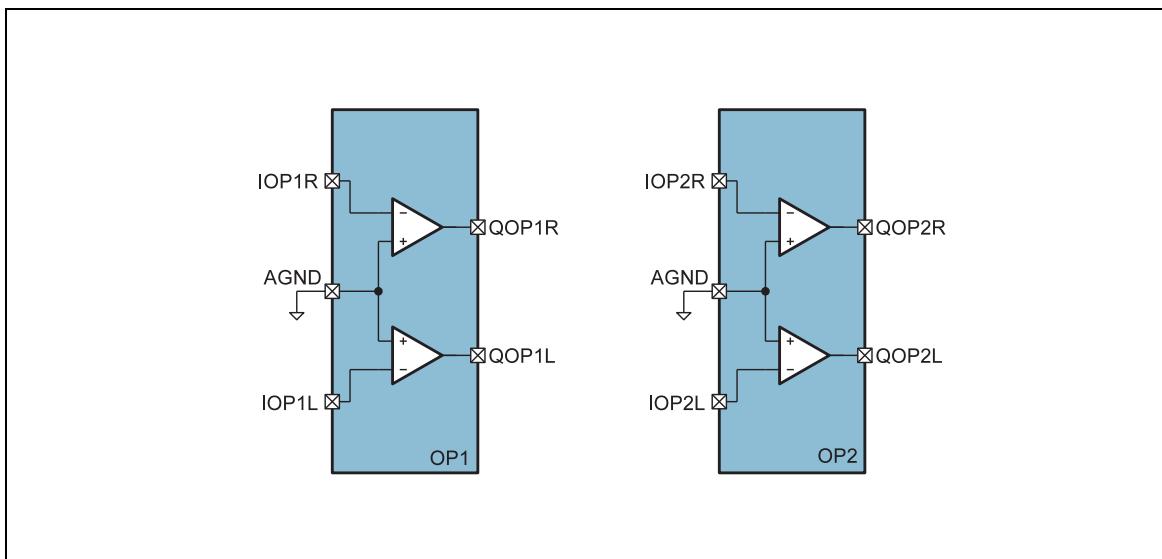


Bypass THD+N vs. Output Power: This table shows A-weighted THD+N characteristics of the integrated bypass switch.

Operational Amplifier

The AS3415 offers only one operational amplifier for feed-forward ANC. The AS3435 features a second additional operational amplifier stage to perform feed-back ANC or any other needed filtering. Both operational amplifiers stages can be activated and used individually.

Figure 43:
Operational Amplifiers



Operational Amplifier: This figure shows the block diagram of the operational amplifiers to be used for ANC filter design.

Parameter

$V_{BAT}=1.5V$, $T_A=25^{\circ}C$, $R_{input} = R_{FB} = 1k\Omega$ unless otherwise specified.

Figure 44:
Operational Amplifier Parameter

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------|---------------------------------------|---|-----|-------------------|-----------|------------|
| V_{LIN} | Input Signal Level | Gain=0dB | | 0.9* V_{BAT} | V_{BAT} | V_{PEAK} |
| SNR | Signal to Noise Ratio | 10k Ω load, Gain = 0dB, $V_{BAT}=1.8V$, High Quality Mode | | 122 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.5V$ High Quality Mode | | 121 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.0V$ High Quality Mode | | 117 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.8V$, ECO Mode | | 118 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.5V$, ECO Mode | | 117 | | dB |
| | | 10k Ω load, Gain = 0dB, $V_{BAT}=1.0V$, ECO Mode | | 113 | | dB |
| I_{LIN} | Block Current Consumption | No load, Gain = 0dB, $V_{BAT}=1.8V$, High Quality Mode | | 660 | | μA |
| | | No load, Gain = 0dB, $V_{BAT}=1.5V$, High Quality Mode | | 660 | | μA |
| | | No load, Gain = 0dB, $V_{BAT}=1.0V$, High Quality Mode | | 530 | | μA |
| | | No load, Gain = 0dB, $V_{BAT}=1.8V$, ECO Mode | | 460 | | μA |
| | | No load, Gain = 0dB, $V_{BAT}=1.5V$, ECO Mode | | 480 | | μA |
| | | No load, Gain = 0dB, $V_{BAT}=1.0V$, ECO Mode | | 360 | | μA |
| $V_{NOISE-A}$ | Input Referred Noise Floor A-Weighted | High Quality Mode | | 900 | | nV |
| | | ECO Mode | | 1.9 | | μV |
| V_{offset} | DC offset voltage | Gain = 0dB | | | 2 | mV |
| C_L | Load Capacitance | | | | 100 | pF |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|----------------|------------|-----|-----|-----|------------|
| A_{Loop} | Open Loop Gain | 100Hz | | 120 | | dB |
| R_L | Load Impedance | | 1 | | | k Ω |

Operational Amplifier: This table shows the detailed electrical characteristics of the operational amplifiers to be used for ANC signal processing.

Figure 45:
Operational Amplifier Frequency Response

Operational Amplifier Frequency Response: This graph shows the frequency response of the operational amplifiers with 0dB gain in normal and ECO mode.

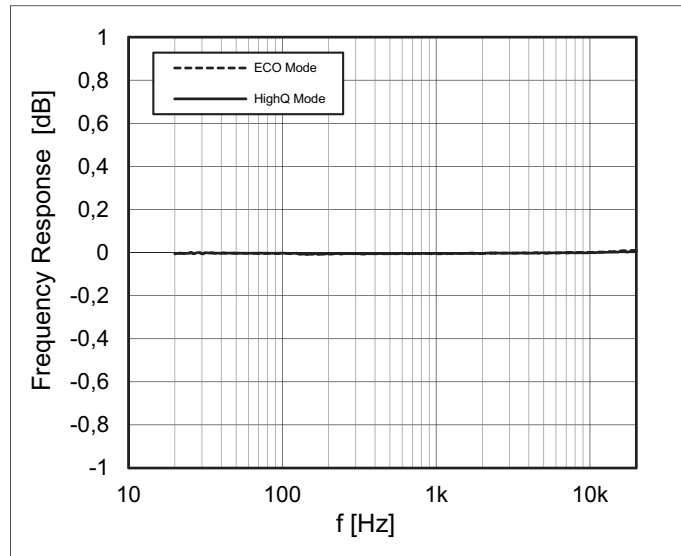


Figure 46:
Operation Amplifier THD+N vs. Frequency $V_{BAT} = 1.8V$

Operation Amplifier THD+N vs. Frequency: The diagram shows the A-weighted THD+N measurement of the line input amplifier with 0dB gain and $V_{BAT}=1.8V$.

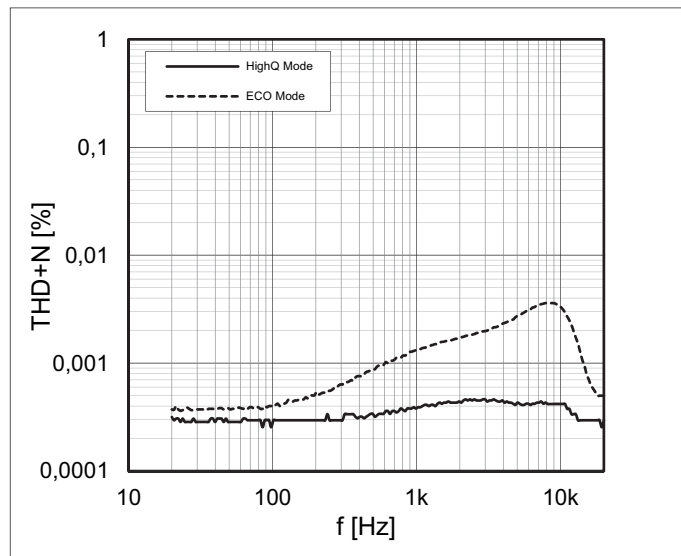


Figure 47:
Operational Amplifier THD+N vs. Frequency $V_{BAT} = 1.5V$

Operation Amplifier THD+N vs.

Frequency: The diagram shows the A-weighted THD+N measurement of the line input amplifier with 0dB gain and $V_{BAT}=1.5V$.

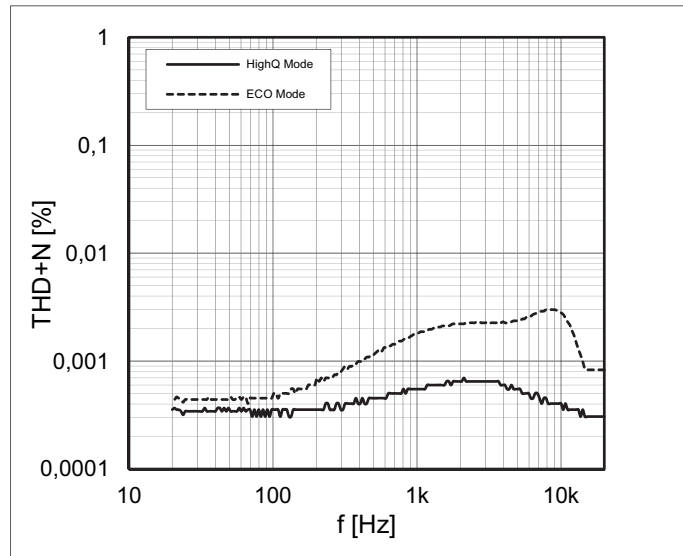
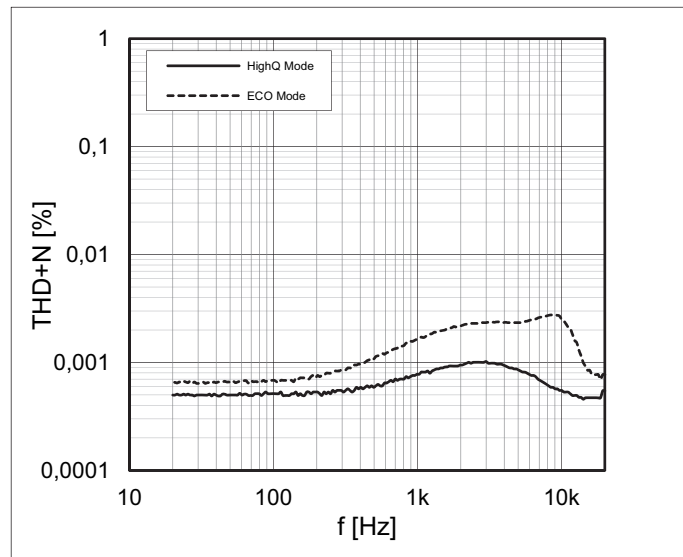


Figure 48:
Operational Amplifier THD+N vs. Frequency $V_{BAT} = 1.0V$

Operation Amplifier THD+N vs.

Frequency: The diagram shows the A-weighted THD+N measurement of the line input amplifier with 0dB gain and $V_{BAT}=1.0V$.



System

The system block handles the power up and power down sequencing as well as the mode switching.

Power Up/Down Conditions

The chip powers up when one of the following conditions is true:

Figure 49:
Power Up Conditions

| # | Source | Description |
|---|------------------------|--|
| 1 | MODE pin | In stand-alone mode, MODE pin has to be driven high for >2ms to turn on the device |
| 2 | I ² C start | In I ² C mode, an I ² C start condition turns on the device |

Power Up Conditions: This table shows the available power up conditions of the AS3415/35.

The chip automatically shuts off if one of the following conditions arises:

Figure 50:
Power Down Conditions

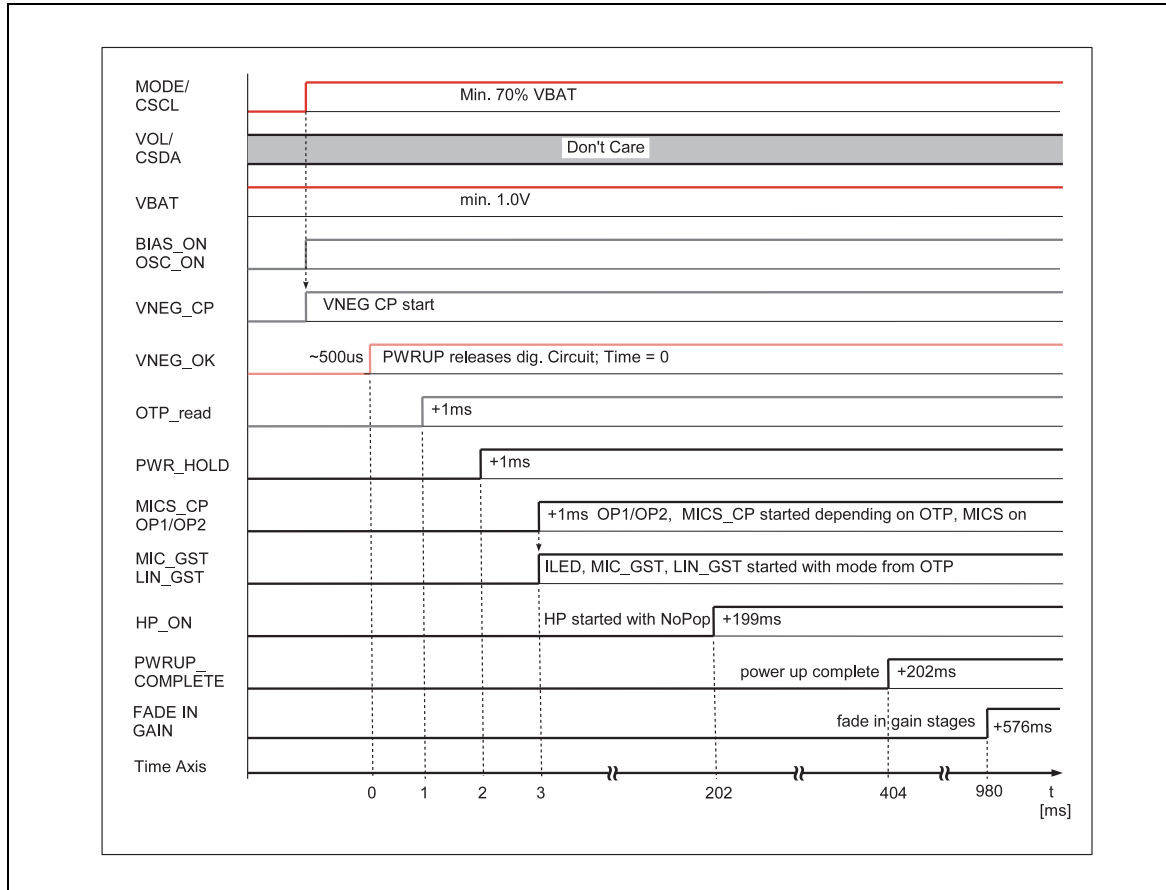
| # | Source | Description |
|---|------------------|--|
| 1 | MODE pin | Slider Mode: Mode pin has to be driven low for 10ms to turn off Push Button Mode: Mode pin has to be driven high for >2.4sec to turn off |
| 2 | Serial Interface | Power down by serial interface by clearing the PWR_HOLD bit. (Please mind that the I2C_MODE bit has to be set before clearing the PWR_HOLD bit for security reasons) |
| 3 | Low Battery | Power down if V_{BAT} is lower than the supervisor off-threshold |
| 4 | V_{NEG} CP OVC | Power down if V_{NEG} is higher than the V_{NEG} off-threshold |

Power Down Conditions: This table shows the available power down conditions of the AS3415/35.

Start-Up Sequence

The AS3515/35 has a defined startup sequence. Once the AS3415/35 MODE pin is pulled high, the device initiates the automatic startup sequence shown in Figure 51.

Figure 51:
Start-Up Sequence



Stand Alone Mode: This timing diagram shows the startup sequence of the AS3415/35 in detail.

Modes of Operation

If the AS3415/35 is in stand-alone mode (no I²C control), the device can work in different operation modes. An overview of the different operation modes is shown in [Figure 52](#).

Figure 52:
Operation Modes

| MODE | Description |
|---------|--|
| OFF | Chip is turned off. |
| ANC | Chip is turned on and active noise cancellation is active |
| MONITOR | In monitor mode, a different (normally higher) microphone preamplifier gain can be chosen to get an amplification of the surrounding noise. To get rid of the low pass filtering needed for the noise cancellation, the headphone input multiplexer can be set to a different (normally to MIC) source to increase speech intelligibility. In addition, the Line In gain can be lowered to reduce the loudness of the music currently played back. If desired the music can also be disabled completely in monitor mode. If the device is operated in I ² C mode, it is also possible to enter the monitor mode by setting the MON_MODE bit in register 0x3D. |
| PBO | The Playback Only Mode is a special mode that disables the noise cancelling function and just keeps the line input amplifier as well as the headphone amplifier active. This allows the user to make use of a possibly implemented equalizer function like bass boost just for listening to music without ANC function. |

Operation Modes: This table gives an overview of the different operation modes of the AS3415/35.

With the AS3415/35 the design engineer has different options to enter the described operation modes shown in [Figure 52](#). In addition to the different switch and push buttons connections described in the following three chapters, it is also important to configure the chipset accordingly. [Figure 53](#) shows the required register configuration settings to enable the different AS3415/35 control modes.

Figure 53:
User Interface Control Modes

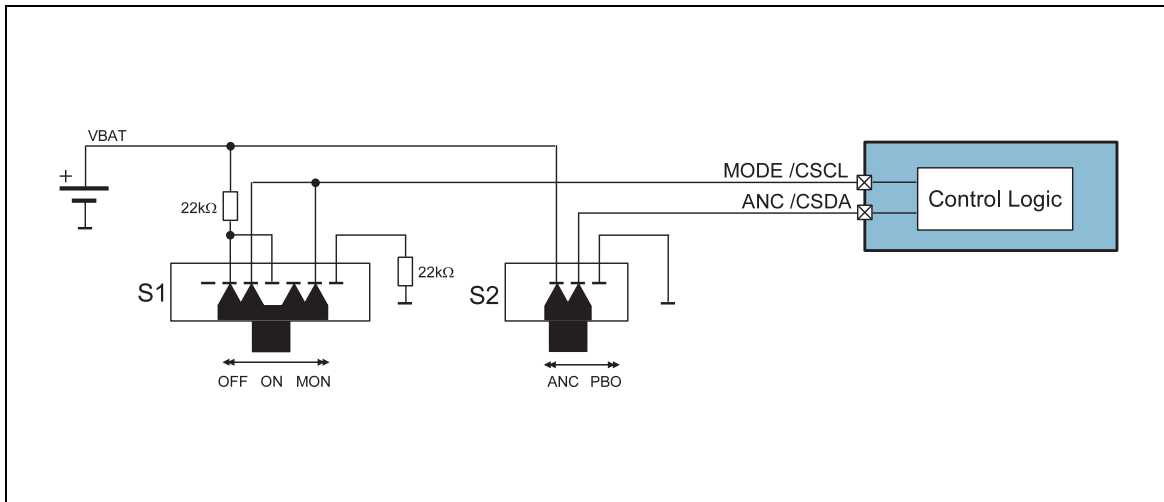
| MODE | Register Name | |
|------------------|---------------|------------|
| | SLIDE_PWR_UP | SLIDER_MON |
| Button Mode | 0 | 0 |
| Do not use | 0 | 1 |
| Slider Mode | 1 | 0 |
| Full Slider Mode | 1 | 1 |

Stand Alone Operation Mode: Shows the different operation modes that can be selected with push button control or slide switch control.

Full Slider Mode

Full Slider Mode enables the AS3415/35 to be connected to two slide switches for Power, ANC and Monitor Mode control. To enable this operation mode bits SLIDE_PWR_UP and SLIDER_MON have to be set to '1'. The typical connection of the slide switches is shown in [Figure 54](#).

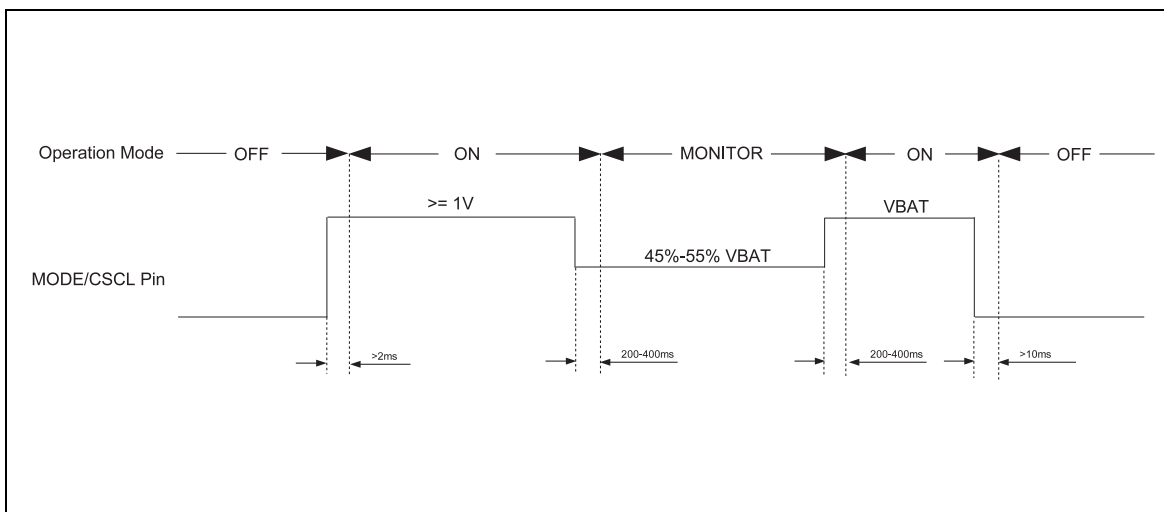
Figure 54:
Full Slider Mode



Full Slider Mode: The diagram shows the external connection of the switches in full slider mode.

In Full Slider Mode the MODE/CSCL pin can detect three different input levels to distinguish between different operating modes: On, Off and Monitor mode. The timing diagram with all relevant information is shown in [Figure 55](#).

Figure 55:
Full Slider Mode Timing Diagram

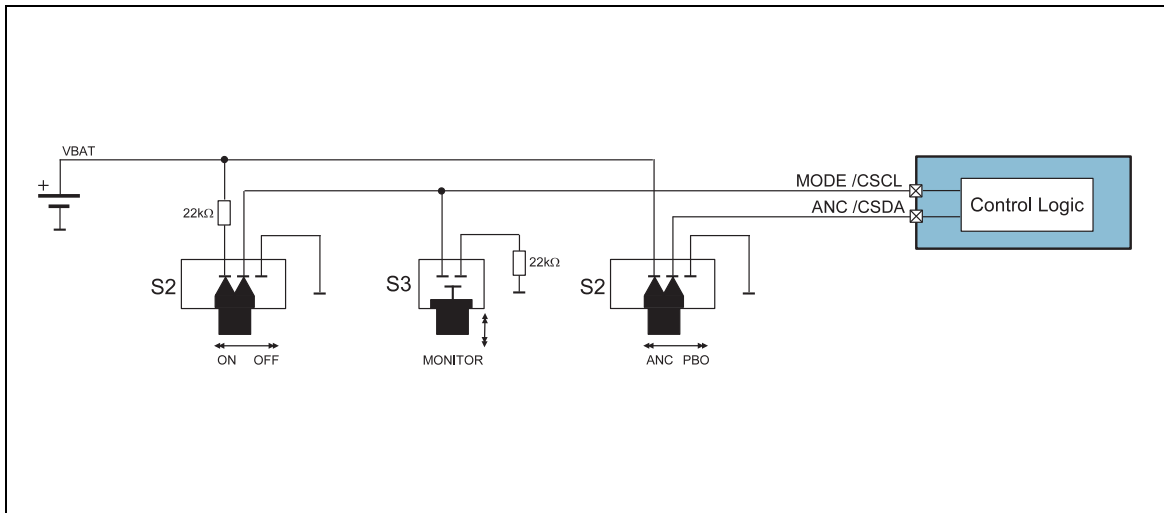


Full Slider Mode Timing Diagram: The diagram shows the necessary pin voltages and timings for different operation modes in Full Slider Mode configuration.

Slider Mode

Slider Mode is similar to Full Slider Mode with the only difference that it is possible to use a push button (S3) to enable and disable the Monitor Mode. Be aware that for Slider Mode operation bit SLIDE_PWR_UP has to be set to '1' and the SLIDER_MON bit has to be set to '0'.

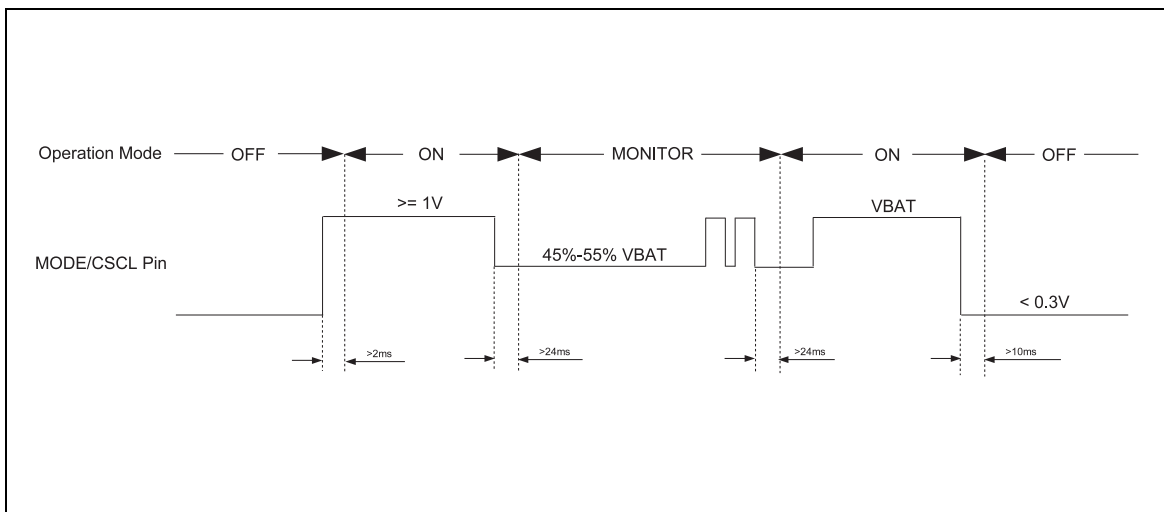
Figure 56:
Slider Mode



Slider Mode: The diagram shows the external connection of the switches and push button in slider mode.

The advantage of this mode compared to Full Slider Mode is the automatic hold function of the Monitor Mode. Once the push button S3 is pressed the device enters monitor mode. This mode stays active until the user pushes the button again.

Figure 57:
Slider Mode Timing Diagram

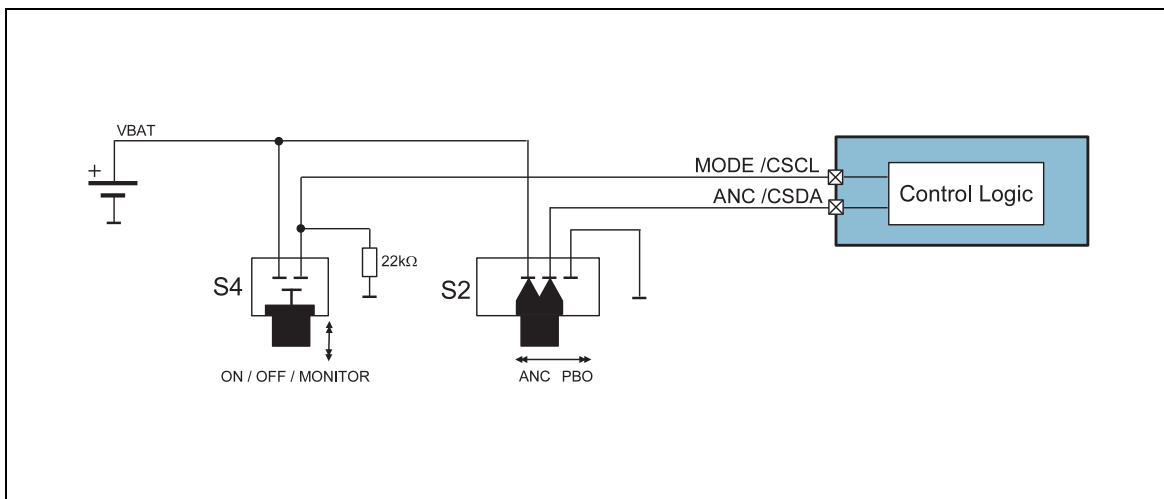


Slider Mode Timing Diagram: The diagram shows the necessary voltages and timings for different operation modes in Slider Mode configuration.

Push Button Mode

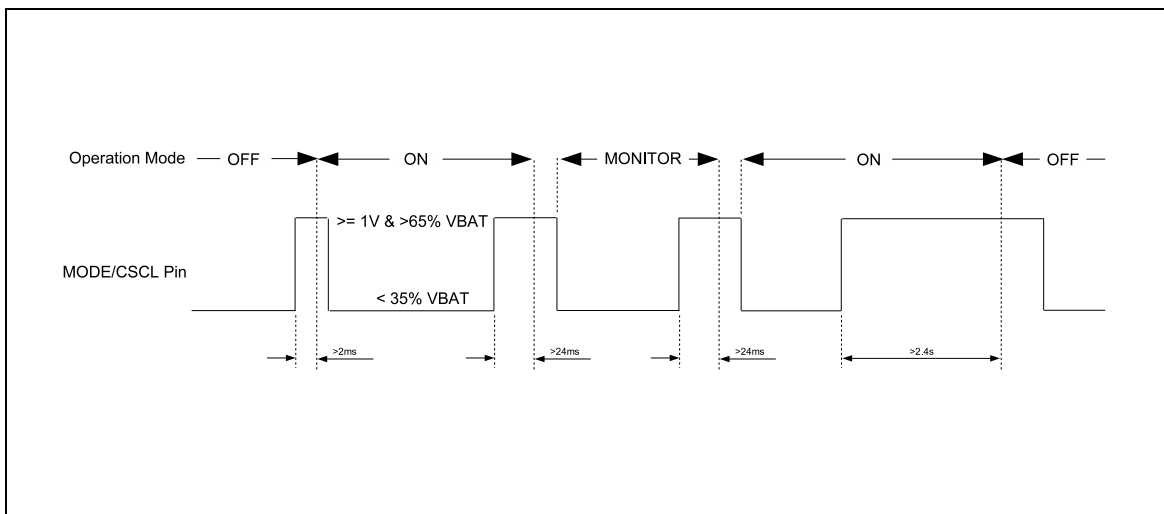
Push Button mode allows the user to control the device with a single normally open (NO) push button. A simple key press powers up the AS3515/35. Once the device is running, a long key press (~2.4 seconds) shuts the device down. As long as the device is active a short key press enters monitor mode. The monitor mode can be deactivated with a second, short key press. A timing diagram of this function is shown in Figure 60. If the monitor mode function is not desired, it is possible to deactivate the monitor mode by setting the bit DISABLE_MONITOR in register 0x15. The typical connection of the push button to the AS3415/35 is shown in Figure 58.

Figure 58:
Push Button Mode



Push Button Mode: The diagram shows the external connection of the switches and push button in slider mode.

Figure 59:
Push Button Mode Timing Diagram

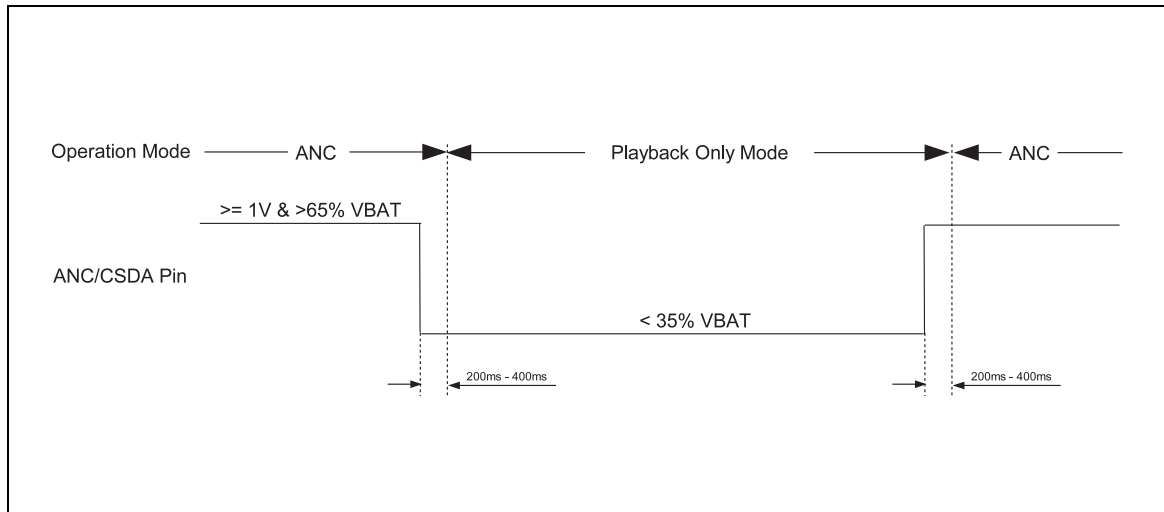


Push Button Mode Timing Diagram: The diagram shows the necessary voltages and timings for different operation modes in Push Button configuration.

Playback Only Mode

The active noise cancelling feature of the AS3415/35 can also be disabled with the ANC/CSDA pin. The ANC/CSDA pin has to be pulled high to enable the ANC function during startup (ANC MODE). If the pin is connected to ground, the chip enters playback only mode (PBO MODE) in which the ANC function is disabled. The operating mode of the line input mute switch, as well as the mixer input, can be defined in register PBO_MODE. The microphone amplifier shuts down automatically, but it is possible to control the operational amplifiers in this mode separately. Typically only the line input amplifiers and the headphone amplifier are enabled in the playback only mode. This very special mode allows the user to disable the ANC function but still use the line input equalizer function of the chipset. If this function is not desired you just need to pull the pin high through a 22kΩ resistor.

Figure 60:
Playback Only Mode Timing Diagram

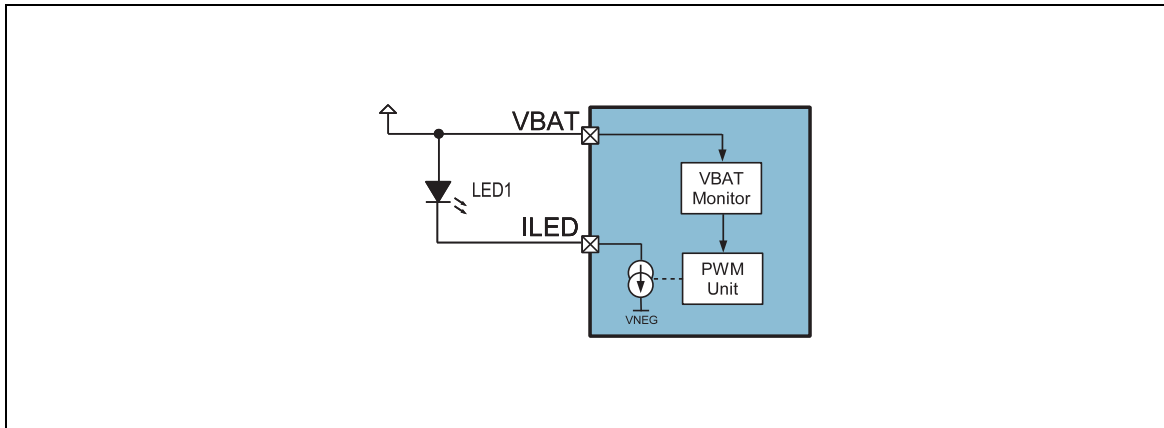


Playback Only Mode Timing Diagram: The diagram shows the necessary voltages and timings for different operation modes in Playback Only Mode.

LED Status Indication

AS3415 and AS3435 feature On-status information via the current sink pin ILED with a maximum driving strength of 2.2mA. The current can be controlled in 3 steps and be switched off by setting the PWM to 0%, 25%, 50% or 100% duty cycle of a 50kHz signal. If LOW_BAT is active, ILED switches to blinking at 1Hz, 50% duty cycle and 50% current setting. The LED can be directly connected to the AS3415/35 without the need of a current limiting resistor. The typical connection circuit is shown in [Figure 61](#).

Figure 61:
LED Status Indication Circuit



LED Status: The block diagram shows the connection of an LED which indicated the operation mode of the ANC chipset.

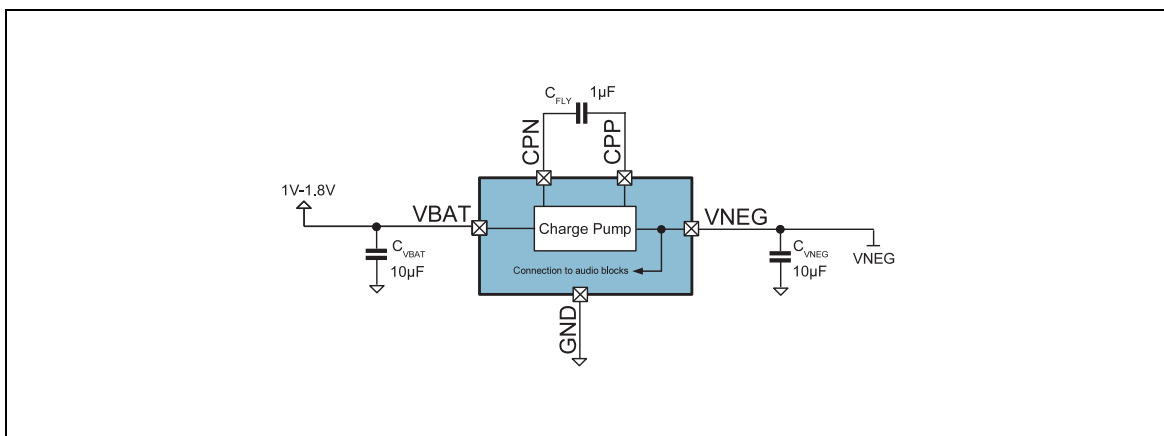
Figure 62:
Electrical Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|------------|---------------------------|-----------------|-----|-----|-----|------|
| I_{ILED} | ILED current sink current | 100% duty cycle | | 2.2 | | mA |

V_{NEG} Charge Pump

The V_{NEG} charge pump uses one external 1 μF ceramic capacitor (C_{FLY}) to generate a negative supply voltage out of the battery input voltage to supply all audio related blocks. This allows a true-ground headphone output with no more need of external DC-decoupling capacitors.

Figure 63:
V_{NEG} Charge Pump



V_{NEG} Charge Pump: This figure shows the block diagram of the V_{NEG} charge pump that supplies all audio blocks of the AS3415/35.

The charge pump typically requires an additional input capacitor, C_{VBAT} of $10\mu\text{F}$ and output capacitor, C_{VNEG} , with the same size as the input capacitor. The flying capacitor, C_{FLY} , should be $1\mu\text{F}$. If hybrid operation is desired, which means two ANC chips are working in parallel, it is possible to disable the V_{NEG} charge pump and share one charge pump for both chips. This should help to reduce the system power consumption of the headset.

Parameter

$V_{BAT}=1.5\text{V}$, $T_A=25^\circ\text{C}$, unless otherwise specified.

Figure 64:
 V_{NEG} Charge Pump Parameter

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|----------------------------|------------|------|------|------|---------------|
| V_{IN} | Input voltage | V_{BAT} | 1.0 | 1.5 | 1.8 | V |
| V_{OUT} | Output voltage | V_{NEG} | -0.7 | -1.5 | -1.8 | V |
| C_{FLY} | External flying capacitor | | | 1 | | μF |
| C_{VBAT} | V_{BAT} input capacitor | | | 10 | | μF |
| C_{VNEG} | V_{NEG} output capacitor | | | 10 | | μF |

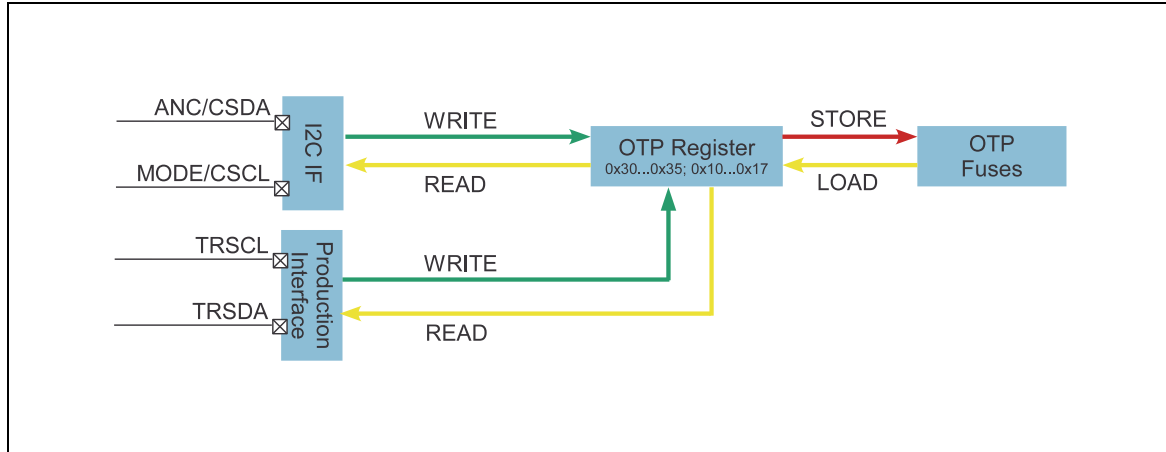
V_{NEG} Charge Pump Parameter: This table describes the electrical characteristics of the V_{NEG} charge pump.

OTP Memory & Internal Registers

The OTP (one-time programmable) memory consists of OTP registers (0x10 - 0x17 and 0x30 - 0x35) and the OTP fuses. The OTP registers can be written as often as wanted but they are volatile memory. It is possible to access the OTP registers using the I²C interface for "soft programming" the part or via the production programming interface pins (TRSDA and TRSCL). In order to store chip configuration data to the ANC chipset, the OTP registers are linked together with the OTP fuses shown in [Figure 65](#). The OTP fuse block is a shadow register of the OTP registers that are nonvolatile memory cells. These registers store chip parameters during power-down. Programming the fuses can be done three times and is a permanent change. In order to configure the ANC chipset during startup the OTP fuse content is loaded to the OTP registers. The AS3415/35 offers 3 OTP fuse sets for storing the microphone gain making it possible to change the gain 2 times for re-calibration or other purposes. In order to determine the right register settings for microphone gain in production, as well as in the engineering design phase, the non-volatile OTP registers should be used without OTP programming. This allows you to configure all registers as many times as desired to find the best microphone

gain calibration data. Once all the right register settings have been found, the OTP fuse block should be used to store these settings.

Figure 65:
Register Access



Register Access: This diagram shows the OTP and register architecture of the AS3515/35.

A single OTP cell can be programmed only once. By default, the cell is "0"; a programmed cell will contain a "1". While it is not possible to reset a programmed bit from "1" to "0", multiple OTP writes are possible, but only additional un-programmed "0"-bits can be programmed to "1".

OTP Registers & Fuses:

The OTP registers are volatile memory cells which lose the content once the device is switched off. Multiple read and write commands are possible but in order to store chip settings during power off mode, the OTP fuses have to be used.

Independent of the OTP programming, it is possible to overwrite the OTP register temporarily if the chip is controlled by a microcontroller via I²C. The chip configuration can be stored in the flash memory of the Bluetooth- or wireless chipset and can be loaded to the ANC chipset during startup of the device via the I²C interface. Because the OTP fuses upload their contents into the OTP register at power-up, the new OTP settings from the microcontroller will overwrite the default settings from the fuses. All I²C OTP registers settings can be changed as many times as desired, but will be lost at power off.

The OTP memory can be accessed in the following ways:

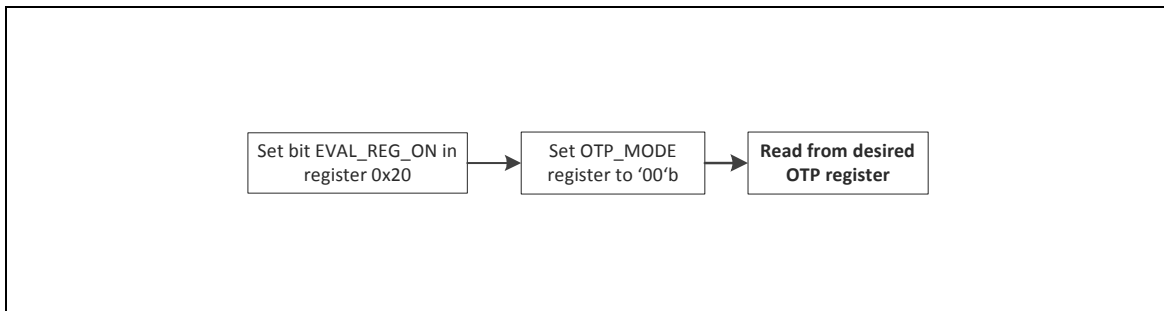
- **LOAD Operation:** The LOAD operation reads the OTP fuses and loads the contents into the OTP register. A LOAD operation is automatically executed after each power-on-reset.
- **WRITE Operation:** The WRITE operation allows a temporary modification of the OTP register. It does not program the OTP. This operation can be invoked multiple times and will remain set while the chip is supplied with power and while the OTP register is not modified with another WRITE or LOAD operation.
- **READ Operation:** The READ operation reads the contents of the OTP register, for example to verify a WRITE command or to read the OTP memory after a LOAD command.

- **STORE Operation:** The STORE operation programs the contents of the OTP register permanently into the OTP fuses. Don't use old or nearly empty batteries for programming the fuses.

OTP Read/Write and Load Access

With the OTP register architecture of the AS3415/35 it is important to know how to access the registers for reading and writing. Before an I²C read command can be sent there are two registers that have to be configured prior to the desired I²C read command. The flow chart in [Figure 66](#) show the correct read access sequence. The first step is to configure the EVAL_REG_ON register. This register enables access to the OTP_MODE register. The OTP_MODE register defines whether you want to read or write to the OTP registers. By setting the OTP_MODE register '00' we select OTP read access. Once the OTP_MODE register has been configured you can start reading from the OTP registers.

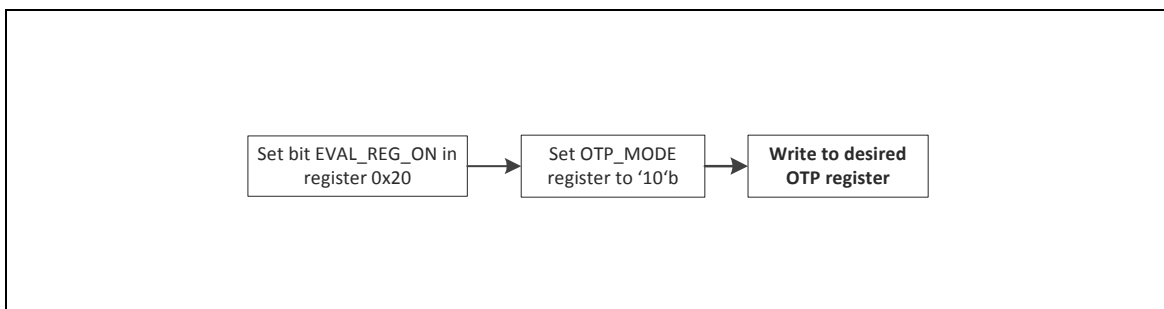
Figure 66:
OTP Read Access Flow Chart



OTP Read Access Flow Chart: This flow chart shows how to successfully read from an OTP register via the I²C or production trimming interface.

The principle for writing to a register is basically the same. The only difference is the configuration of the OTP_MODE register, shown in [Figure 67](#). The first step is to enable the OTP_MODE register by setting the EVAL_REG_ON register to '1'. The next step is to configure the OTP_MODE register to '10' in order to select OTP write access. Now you can start writing to any OTP register inside the AS3415/35.

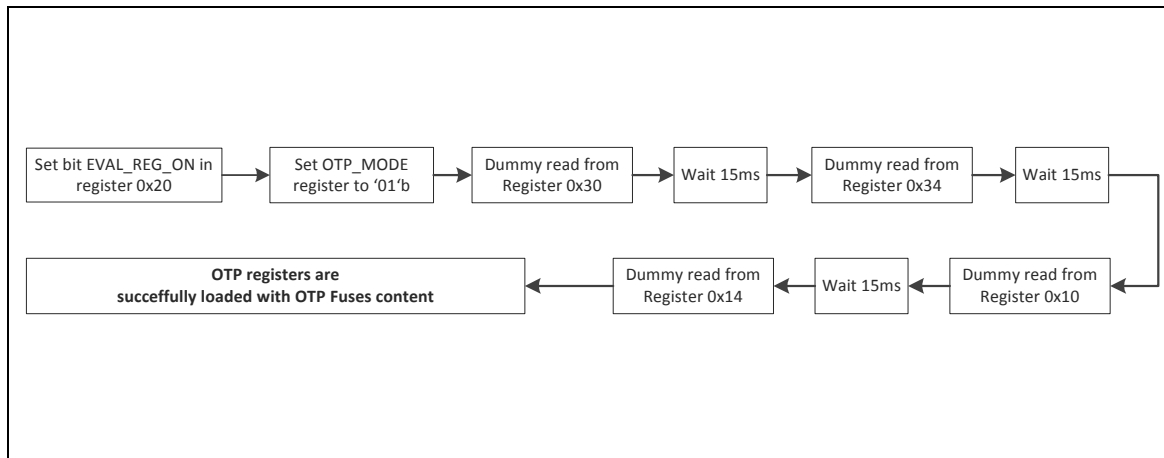
Figure 67:
OTP Write Access Flow Chart



OTP Write Access Flow Chart: This flow chart shows how to successfully write to an OTP register via the I²C or production trimming interface.

If you want to read out the OTP fuse content the OTP load function is necessary. In order to load the OTP fuse content to the OTP registers, a special sequence is necessary, as shown in [Figure 68](#).

Figure 68:
OTP Load Access Flow Chart

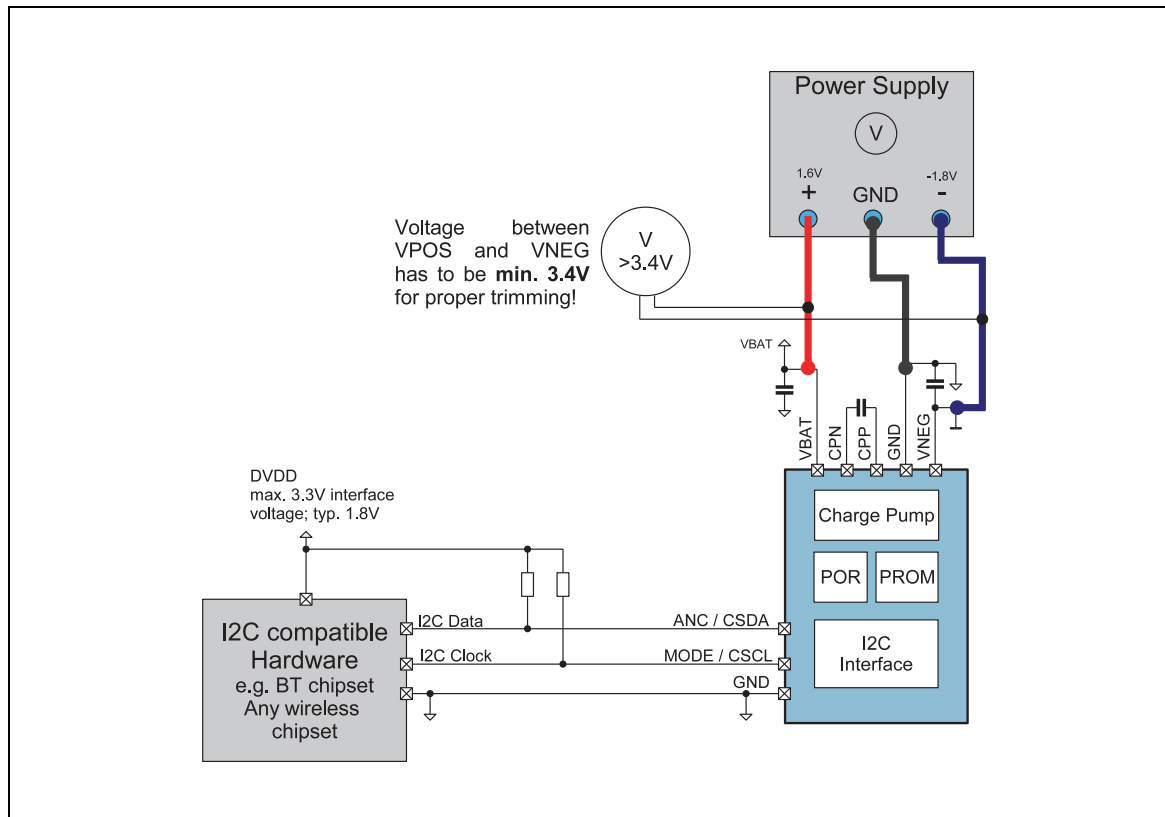


OTP Load Access Flow Chart: This flow chart shows how to successfully load the OTP fuse content back to the OTP register via the I²C or production trimming interface.

OTP Fuse Storing

Many wireless applications, like Bluetooth single chips support programmable solutions, as well as ROM versions. As such, it is necessary for ROM versions to store microphone gain compensation data and the general ANC configuration inside the ANC chip. This is necessary because there is no other way to configure the ANC chip during startup. In order to guarantee successful trimming of AS3415/35 it is necessary to provide a decent environment for the trimming process. [Figure 69](#) shows a principal block diagram for trimming the AS3415/35 properly in production using the I²C interface. The most important block is the external power supply. Usually it is possible to trim the AS3415/35 with a single supply voltage of min. 1.8V in laboratory environment, but as soon as it comes to mass production we highly recommend buffering V_{NEG} supply of the chip. As highlighted in the block diagram, it is mandatory to get a voltage difference between V_{POS} and V_{NEG} of 3.4V (minimum) to guarantee proper trimming of the device, therefore it is possible to buffer it externally with a negative power supply. The V_{NEG} voltage applied to VNEG pin must be lower than the voltage created with the charge pump. This means if the typical V_{NEG} output voltage is -1.5V you can easily apply externally -1.7V. The charge pump switches then automatically into skip mode.

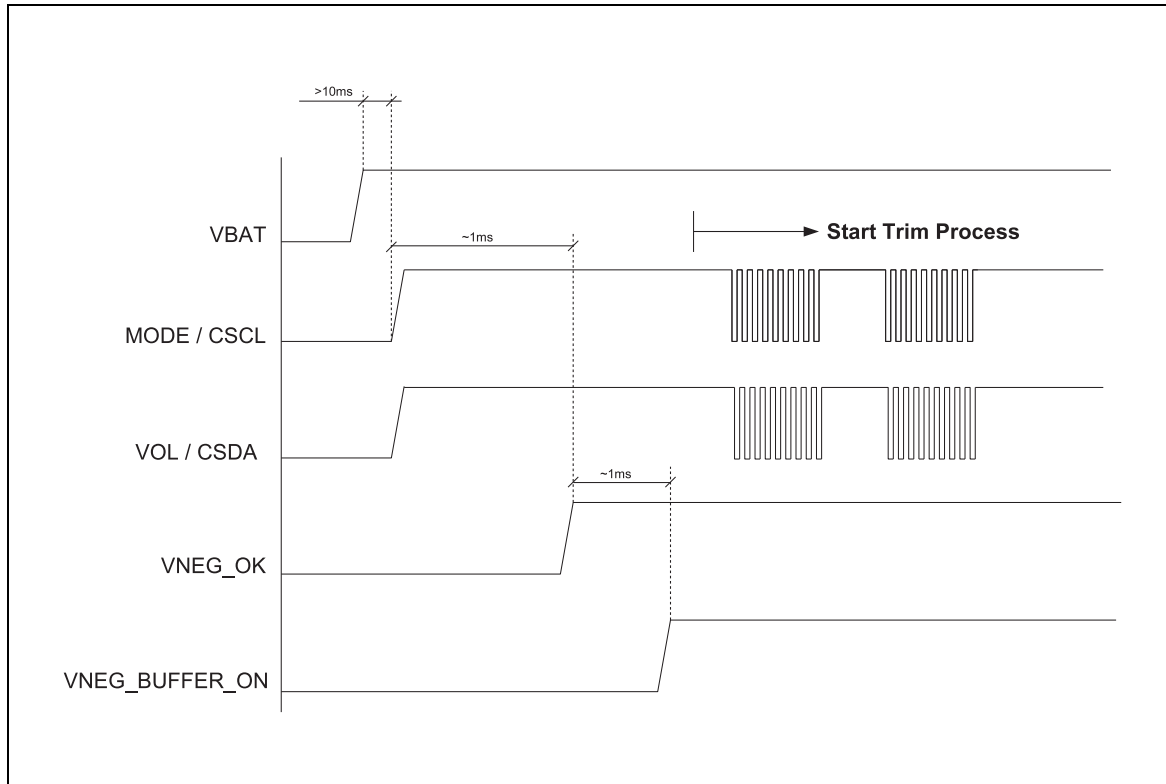
Figure 69:
Production Environment I²C Interface Trimming



I²C Trimming: This block diagram shows a general overview of the production environment when storing the register settings to the AS3415/35 using a standard I²C interface.

Timing is important, to avoid latch-up, when using an external buffer and switching on the ANC device. The timing diagram in [Figure 70](#) shows that it is important that there is a certain delay requirement between VBAT and the MODE / CSCL pin. This delay is mandatory in order to guarantee that the device starts up properly. The MODE / CSCL pin powers up the ANC device. The whole sequence to power up the internal charge pump of the AS3415/35 takes approximately 1ms. Once V_{NEG} is settled the external V_{NEG} buffer (e.g. power supply) can be enabled in order to support the charge pump especially during the trim process which can now be started.

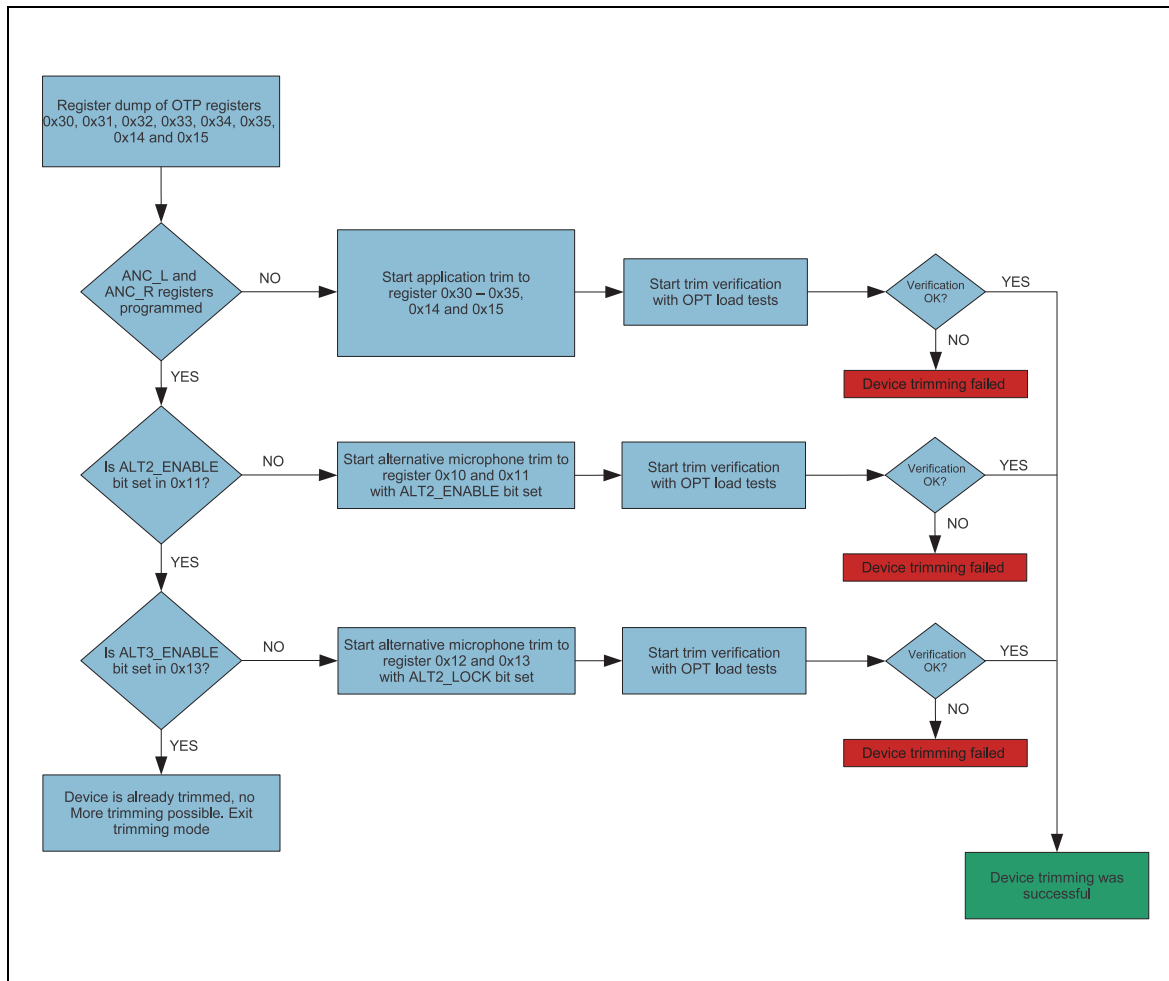
Figure 70:
Timing Diagram V_{NEG} Buffering



V_{NEG} Buffer Timing: This timing diagram shows how to buffer the V_{NEG} supply during the OTP programming process.

To guarantee a successful trimming process it is important to follow the predefined trimming sequence shown in [Figure 71](#) exactly. As a first step it is important to do a register dump of all OTP registers. This register backup in your system memory is a backup of all register settings and is necessary for verification after the trim process to make sure that all bits are trimmed correctly. Once the register dump has been done it is important to check registers 0x30 and 0x31. These registers typically indicate if the device is already trimmed or not. If both registers have the value 0x80 you can enter the trim mode and start the trimming process. Once trimming is done, the most important step is comparing the values trimmed to the device with the original register dump performed just before we started the actual trimming process. If the verification was successful we know that all bits have been trimmed correctly to AS3415/AS3435. What is important to mention is that the AS3415 and AS3435 have a couple of test bits inside which are by default set to '1'. We do not recommend overwriting these bits. Furthermore, it is important to know that it is not possible to change bits once they are trimmed. It is not possible to change a bit from '1' back to zero. If an additional trimming is done it is only possible to change bits from '0' to '1'. It is important that all necessary bits are trimmed exactly like in the block diagram shown in [Figure 71](#).

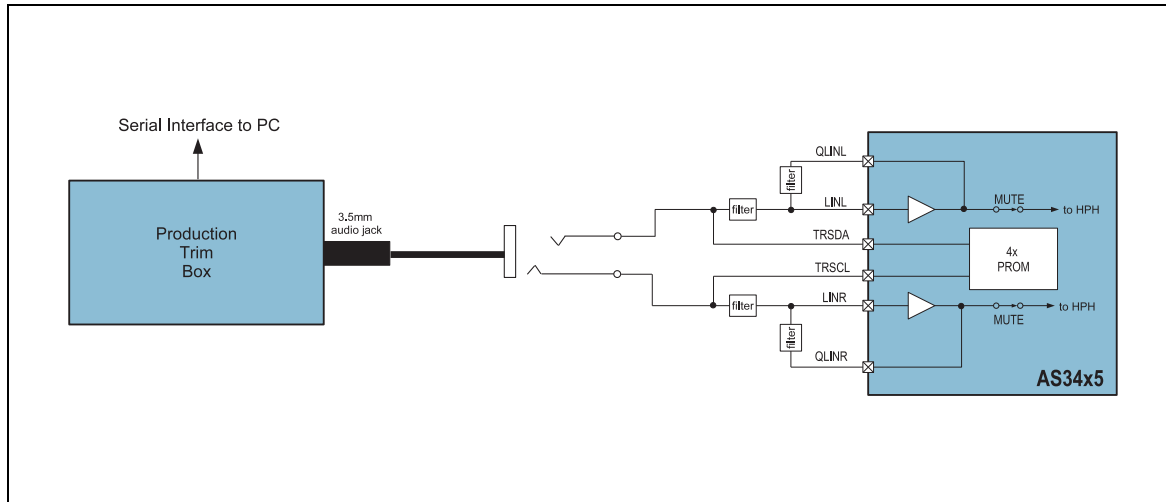
Figure 71:
OTP Programming Process



OTP Programming: This flow chart describes the OTP programming process in detail.

Besides production trimming using the I²C interface, the AS3415/35 features a second unique trimming mechanism. This very special mode enables the analog music inputs of the AS3415/35 to become a production trimming input.

Figure 72:
Production Environment Production Trim Box



Production Trim Box: This block diagram shows the connection of the Trim Box enabling the audio inputs to become a trim input for mass production.

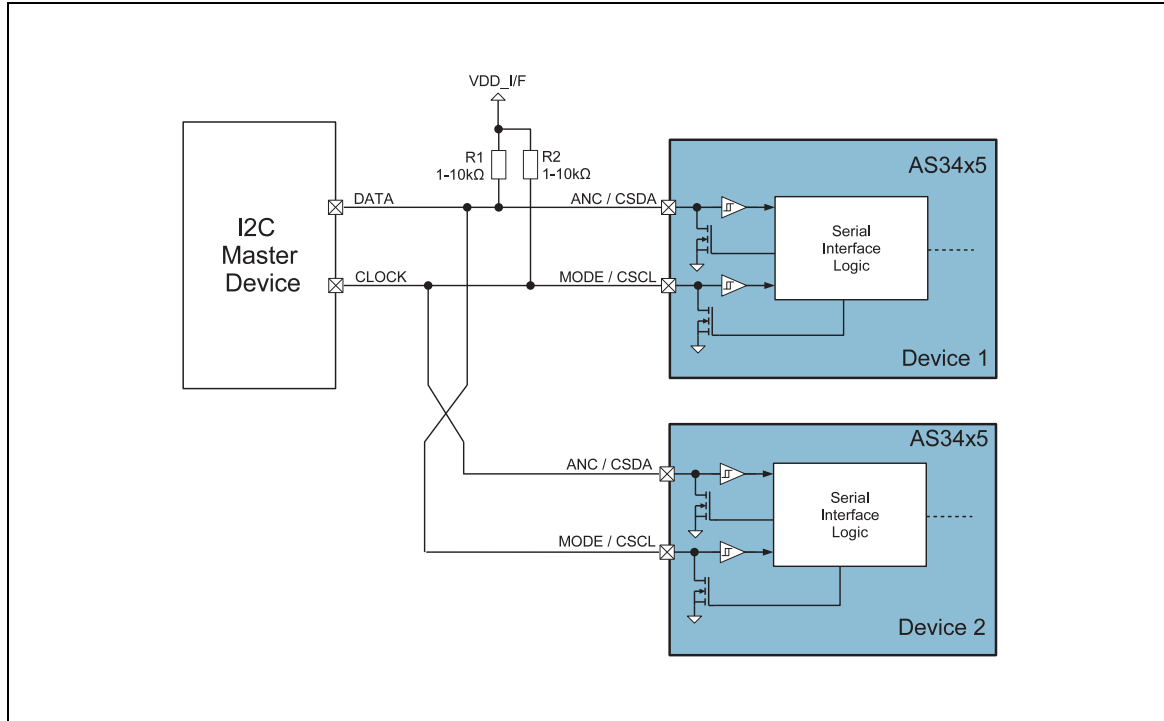
With this new system, there is no need for mechanical potentiometers any more. Up to now, operators in production use screw drivers to fine tune the ANC performance of each headset. The disadvantage of this is reliability and cost of potentiometers. Additionally, operators are not always precise in their work, thus yielding inconsistent results. With the new production trimming system from ams there are no mechanical potentiometers required. The operator connects a 3.5mm audio jack to a trimming box and this box enables the audio input of the headset to become the ANC tuning input. This new feature also helps industrial designers of headset because there are no more considerations concerning leakage holes for the old mechanical trimming. Thus, the headset can be fully assembled and ready for the ANC test system at the end of the manufacturing process. The trim box can be easily controlled with an RS232 interface so it is also possible to create fully automated trimming systems. For further details please contact our local sales office; they can provide you with source code examples and application notes.

2-Wire Serial Interface

In order to configure the device using the evaluation software or a MCU the AS3515/35 features a serial two wire interface. Some applications like hybrid systems do require two ANC chipsets in parallel; therefore the AS3515/35 supports two different slave addresses to enable communication on a single bus with two devices. The AS3515/35 features two I²C slave addresses without having a dedicated address selection pin. The selection of the I²C address is done with the interconnection of AS3515/35 to the bus lines shown in [Figure 73](#) below. The serial interface logic inside AS3515/35 is able to distinguish between a direct I²C connection to the

master or a second option where data and clock line are crossed. Therefore it is only possible to address a maximum of two AS3515/35 slaves on one I²C bus.

Figure 73:
I²C Address Selection



I²C Address Selection: This block diagram shows how to connect two AS3514/35 to an I²C master.

The I²C addresses for the devices in the different connection modes can be found in [Figure 74](#).

Figure 74:
I²C Slave Address Table

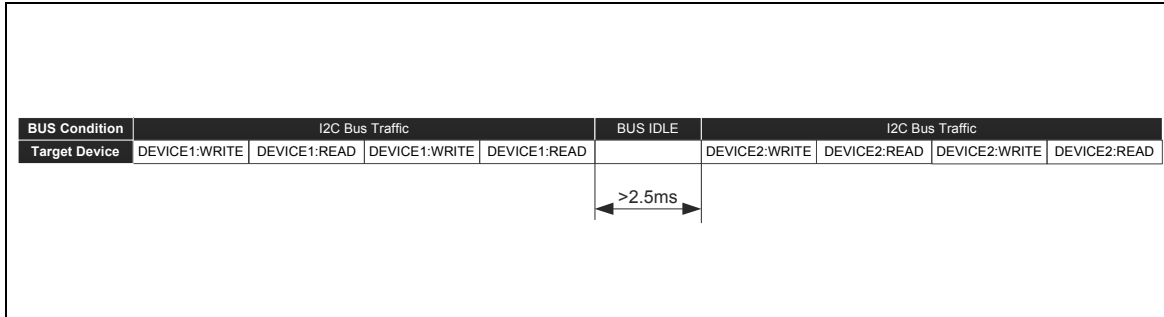
| DEVICE Number | 7 bit I ² C address | 8 Bit read address | 8 Bit write address |
|---------------|--------------------------------|--------------------|---------------------|
| 1(default) | 0x47 | 0x8F | 0x8E |
| 2 | 0x46 | 0x8D | 0x8C |

I²C Slave Address Table: Shows the two I²C addresses for the AS3515/35 depending on the master connection.

When the I²C master is accessing two devices on the bus it is important not violating the minimum bus idle time of 2.5ms. Thus, if the I²C master is communicating with device one it is not possible to read/write for example from device two right after a read/write command has been sent to device one without a minimum bus idle time of 2.5ms. Due to the reason that the AS3415/35 does not have a dedicated I²C address selection pin this idle time is necessary to recover the internal

I²C address selection block for a correct I²C slave address detection. The I²C address selection timing diagram in Figure 75 shows the necessary bus idle time.

Figure 75:
I²C Address Selection Timing



Protocol

Figure 76:
I²C Serial Interface Symbol Definition

| Symbol | Definition | RW | Note |
|----------|---------------------------------------|----|--------------------|
| S | Start condition after stop | R | 1 bit |
| Sr | Repeated start | R | 1 bit |
| DW | Device address for write | R | 1000 1110b (8Eh) |
| DR | Device address for read | R | 1000 1111b (8Fh) |
| WA | Word address | R | 8 bit |
| A | Acknowledge | W | 1 bit |
| N | No Acknowledge | R | 1 bit |
| reg_data | Register data/write | R | 8 bit |
| data (n) | Register data/read | W | 8 bit |
| P | Stop condition | R | 1 bit |
| WA++ | Increment word address internally | R | during acknowledge |
| | AS3421 AS3422 (=slave) receives data | | |
| | AS3421 AS3422 (=slave) transmits data | | |

Symbol Definition: The table shows the symbol definitions being used in the explanations for the data transfer between master and slave.

Figure 77:
Byte Write

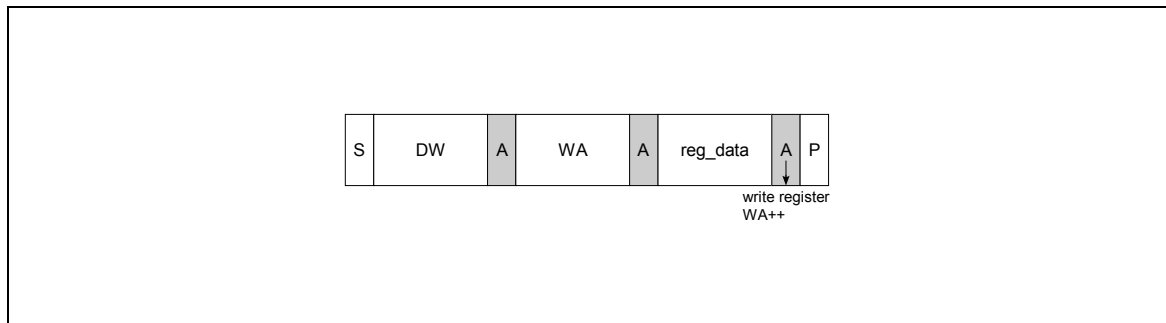
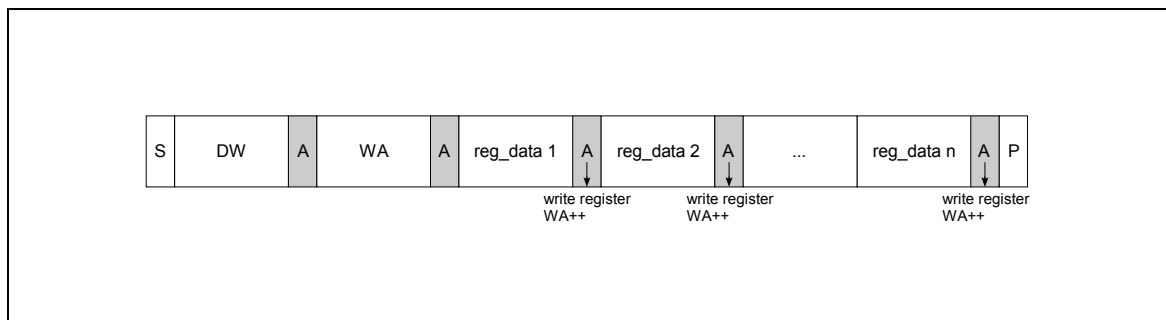


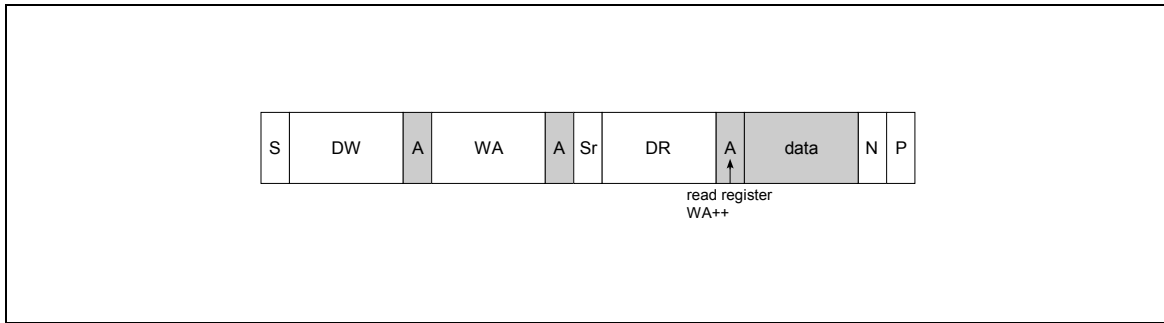
Figure 78:
Page Write



Byte Write and Page Write formats are used to write data to the slave. The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes to subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

Figure 79:
Random Read

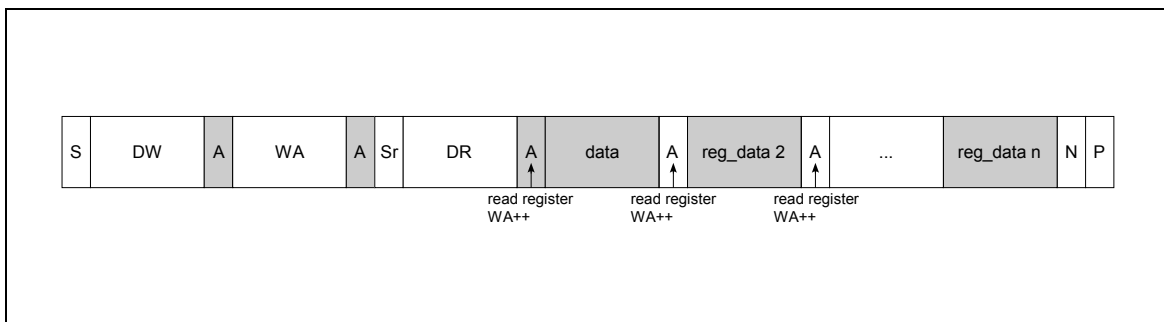


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

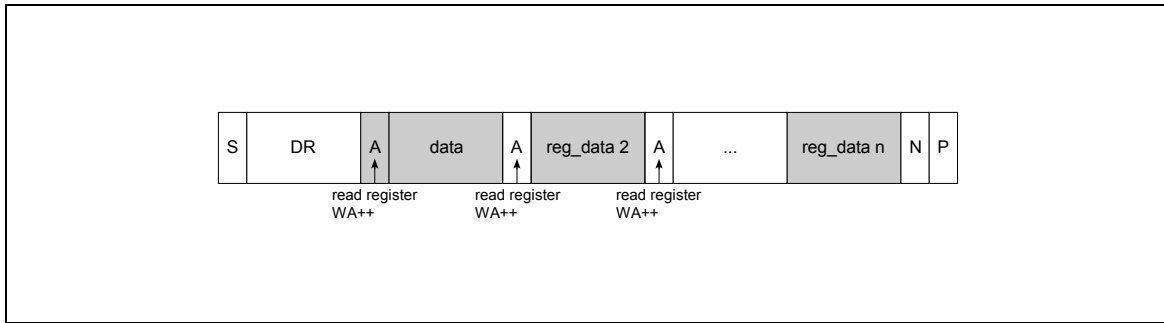
In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

Figure 80:
Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. Different from the Random Read, for a sequential read, the transferred register-data bytes are responded with an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and then generate the STOP condition.

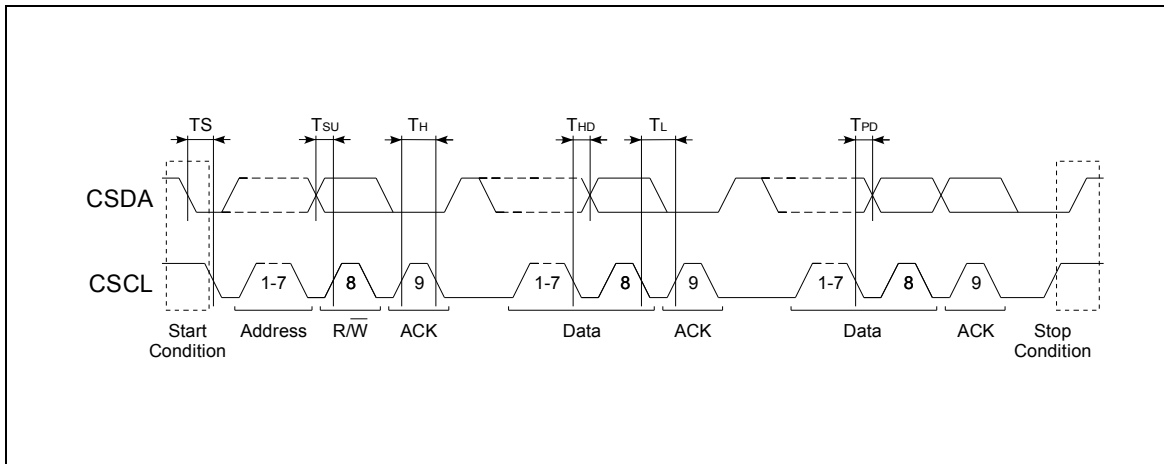
Figure 81:
Current Address Read



To keep the access time as short as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes have to be responded with an acknowledge from the master. For termination of the transmission, the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

Parameter

Figure 82:
I²C Serial Timing



$V_{BAT} \geq 1.4V^1$, $T_A=25^\circ C$, unless otherwise specified.

Figure 83:
I²C Serial Interface Parameter

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|-----------------------------|---|------|-----|------|------|
| V_{CSL} | CSCL, CSDA Low Input Level | (Max. 30% V_{BAT}) | 0 | - | 0.42 | V |
| V_{CSH} | CSCL, CSDA High Input Level | CSCL, CSDA (min 70% V_{BAT}) | 0.98 | - | | V |
| HYST | CSCL, CSDA Input Hysteresis | | 200 | 450 | 800 | mV |
| V_{OL} | CSDA Low Output Level | At 3mA | - | - | 0.4 | V |
| T_{sp} | Spike insensitivity | | 50 | 100 | - | ns |
| T_H | Clock high time | Max. 400kHz clock speed | 500 | | | ns |
| T_L | Clock low time | Max. 400kHz clock speed | 500 | | | ns |
| T_{SU} | | CSDA has to change Tsetup before rising edge of CSCL | 250 | - | - | ns |
| T_{HD} | | No hold time needed for CSDA relative to rising edge of CSCL | 0 | - | - | ns |
| TS | | CSDA H hold time relative to CSDA edge for start/stop/rep_start | 200 | - | - | ns |
| T_{PD} | | CSDA prop delay relative to low going edge of CSCL | | 50 | | ns |

1. Serial interface operates down to $V_{BAT} = 1.0V$ but with 100kHz clock speed and degraded parameters.

Register Description

Figure 84:
Register Table Overview

| Addr | Name | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | |
|-------------------------|----------|---|---------|--|----------------|---|---------|------------|-----------------|----------|
| System Registers | | | | | | | | | | |
| 20h | SYSTEM | DESIGN_VERSION<3:0> 1100 | | | | eval_reg_on | | | | PWR_HOLD |
| 21h | PWR_SET | | LOW_BAT | PWRUP COMPLETE | HPH_ON | MIC_ON | LIN_ON | MICS_CP_ON | MICS_ON | |
| 2h-2Fh | reserved | | | | | | | | | |
| OTP Registers | | | | | | | | | | |
| 10h | ANC_L2 | TEST_BIT_1 | | MICL_VOL_OTP2<5:0> Gain from MICL to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB | | | | | | |
| 11h | ANC_R2 | ALT2_ENABLE | | MICR_VOL_OTP2<5:0> Gain from MICR to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB | | | | | | |
| 12h | ANC_L3 | TEST_BIT_2 | | MICL_VOL_OTP3<5:0> Gain from MICL to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB | | | | | | |
| 13h | ANC_R3 | ALT3_ENABLE | | MICR_VOL_OTP3<5:0> Gain from MICR to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB | | | | | | |
| 14h | ANC_MODE | HPH_MUX<1:0> 0: MIC; 1: OP1; 2: OP2; 3: - | | LIN_MUTE | MIX_ENABLE | OP2L_ON | OP2R_ON | OP1L_ON | OP1R_ON | |
| 15h | MON_MODE | MON_HPH_MUX<1:0> 0: MIC; 1: OP1; 2: OP2; 3: - | | MON_LIN_MUTE | MON_MIX_ENABLE | MON_LINE_ATT<1:0> 0: 0dB 1: -24dB 2: -30dB 3: -36dB | | SLIDER_MON | DISABLE_MONITOR | |

| Addr | Name | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|-----------------------------|-----------|--------------|------------|--|-------------------|----------------|----------------|---|-------------------|
| 16h | PBO_MODE | TEST_BIT_4 | NO_PBO | PBO_LIN_MUTE | PBO_MIX_ENABLE | PBO_OP2L_ON | PBO_OP2R_ON | PBO_OP1L_ON | PBO_OP1R_ON |
| 17h | ECO | SLIDE_PWR_UP | LOWBAT_100 | ILED<1:0> 0: OFF; 1: 25%; 2: 50%; 3: 100% | | ENABLE_HPH_ECO | ENABLE_MIC_ECO | ENABLE_LIN_ECO | ENABLE_OPA_MP_ECO |
| 30h | ANC_L | TEST_BIT_3.1 | | MICL_VOL<5:0> Gain from MICL to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB | | | | | |
| 31h | ANC_R | TEST_BIT_6 | | MICR_VOL<5:0> Gain from MICR to QMICL or Mixer = 0dB...+31dB; MUTE and 63 steps of 0.5dB | | | | | |
| 32h | MIC_MON_L | | | MICL_MON<5:0> Gain from MICL to QMICL/R = 0dB...+31dB; MUTE and 63 steps of 0.5dB if MON_MODE is active | | | | | |
| 33h | MIC_MON_R | | | MICR_MON<5:0> Gain from MICL to QMICL/R = 0dB...+31dB; MUTE and 63 steps of 0.5dB if MON_MODE is active | | | | | |
| 34h | MODE_1 | MICS_CP_OFF | MICS_OFF | MIC_AGC_ON | MIC_OFF | NO_LOWBAT_OFF | CP_OFF | HPH_OFF | LIN_OFF |
| 35h | MODE_2 | TEST_BIT_7 | HP_RAMP_ON | | | MICS_DC_OFF | DELAY_HPH_MUX | HPH_MODE 0: Stereo 1: Mono Differential | I2C_MODE |
| Evaluation Registers | | | | | | | | | |
| 3Dh | EVAL | EVAL_ON | | MASTER_LIN_MUTE | MASTER_MIX_ENABLE | MON_MODE | PBO_MODE | MICL_MUTE | MICR_MUTE |
| 3Eh | CONFIG_1 | | | | | EXTBURNCLK | | | |
| 3Fh | CONFIG_2 | | | TM34 | BURNSW | TM_REG34-35 | TM_REG30-33 | OTP_MODE<1:0> 0: READ; 1: LOAD; 2: WRITE; 3: BURN | |

System Registers

Figure 85:
SYSTEM Register Description

| Name | | Address | | Default Value | |
|---|----------------|---------|--------|---|--|
| SYSTEM | | 0x20 | | 81h | |
| This register contains control bits for monitor mode, OTP register and power up/down functions. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 7:4 | DESIGN_VERSION | 1100 | R | Design version number to identify the design version of the AS3415/35. 1010: For chip version 1v0 1011: For chip version 1v1 1100: For chip version 1v2 | |
| 3 | EVAL_REG_ON | 0 | R/W | This register controls read and write access to the OTP register banks. 0: Normal operation 1: Enables writing to register 0x3D, 0x3E and 0x3F to configure the OTP and set the access mode. | |
| 2 | MONITOR_ON | 0 | R/W | This bit enables the monitor mode of AS3415/35 which can normally be enabled by pulling the MODE pin to $V_{BAT}/2$. In case an MCU is connected to the device the Monitor mode can be enabled by setting this bit. 0: Monitor mode deactivated 1: Monitor mode activated | |
| 0 | PWR_HOLD | 1 | R/W | This bit allows an MCU using the I ² C interface a power down of the AS3415/35. A start condition on the I ² C interface will wake up the device again. This function works only if the I2C_MODE bit is set before you write this register. 0: Power up hold is cleared and chip powers down 1: It is automatically set to on after power on | |

Figure 86:
PWR_SET Register Description

| Name | | Address | | Default Value | |
|---|----------|---------|--------|--|--|
| PWR_READ | | 0x21 | | 20h | |
| A readout of this register returns the status of each block of the chipset. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 6 | LOW_BAT | x | R | V_{BAT} supervisor status 0: V_{BAT} is above brown out level 1: V_{BAT} has reached brown out level | |

| Name | | Address | | Default Value | |
|---|----------------|---------|--------|--|--|
| PWR_READ | | 0x21 | | 20h | |
| A readout of this register returns the status of each block of the chipset. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 5 | PWRUP_COMPLETE | x | R | Power-Up sequencer status 0: Power-up sequence incomplete 1: Power-up sequence completed | |
| 4 | HPH_ON | 0 | R | This register returns the power status of the headphone amplifier. 0: Headphone amplifier switched off 1: Headphone amplifier switched on | |
| 3 | MIC_ON | 0 | R | This register returns the power status of the microphone preamplifier. 0: Microphone preamplifier switched off 1: Microphone preamplifier switched on | |
| 2 | LIN_ON | 0 | R | This register returns the power status of the line input amplifier. 0: Line input switched off 1: Line input switched on | |
| 1 | MICS_CP_ON | 0 | R | This register returns the power status of the microphone charge pump. 0: Microphone charge pump switched off 1: Microphone charge pump switched on | |
| 0 | MICS_ON | 0 | R | This register returns the power status of the microphone supply (MICS). 0: Microphone supply switched off 1: Microphone supply switched on | |

OTP Registers

Figure 87:
ANC_L2 Register Description

| Name | | Address | | Default Value |
|--|--------------------|----------|--------|--|
| ANC_L2 | | 0x10 | | 80h |
| The ANC_L2 Register configures the gain for the left microphone input. This register is the first alternative microphone gain register for OTP programming in case the ANC_L register is already programmed. | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | TEST_BIT_1 | 1 | R | Test register. Please do not write this register. |
| 5:0 | MICL_VOL_OTP2<6:0> | 000 0000 | R/W | Volume settings for left microphone input, adjustable in 63 steps of 0.5dB 00 0000: MUTE 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain ... 11 1110: 30.5dB gain 11 1111: 31dB gain |

Figure 88:
ANC_R2 Register Description

| Name | | Address | | Default Value |
|---|-------------|---------|--------|--|
| ANC_R2 | | 0x11 | | 00h |
| The ANC_R2 Register configures the gain for the right microphone input. This register is the first alternative microphone gain register for OTP programming in case the ANC_R register is already programmed. | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | ALT2_ENABLE | 0 | R/W | In case the register is being used for microphone programming this bit has to be set. The bit is being used by the internal state machine of the AS3415/35 to determine which alternative microphone gain register has to be used during startup. 0: Microphone registers 0x10 and 0x11 are not active 1: Microphone registers 0x10 and 0x11 are active. Gain settings in registers 0x30 and 0x31 are ignored |

| Name | | Address | | Default Value | |
|---|--------------------|----------|--------|--|--|
| ANC_R2 | | 0x11 | | 00h | |
| The ANC_R2 Register configures the gain for the right microphone input. This register is the first alternative microphone gain register for OTP programming in case the ANC_R register is already programmed. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 5:0 | MICR_VOL_OTP2<6:0> | 000 0000 | R/W | Volume settings for left microphone input, adjustable in 63 steps of 0.5dB 00 0000: MUTE 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain ... 11 1110: 30.5dB gain 11 1111: 31dB gain | |

Figure 89:
ANC_L3 Register Description

| Name | | Address | | Default Value | |
|--|--------------------|----------|--------|--|--|
| ANC_L3 | | 0x12 | | 80h | |
| The ANC_L3 Register configures the gain for the left microphone input. This register is the second alternative microphone gain register for OTP programming in case the ANC_L and ANC_L2 registers are already programmed. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | TEST_BIT_6 | 1 | R | Test register. Please do not write this register. | |
| 5:0 | MICL_VOL_OTP3<6:0> | 000 0000 | R/W | Volume settings for left microphone input, adjustable in 63 steps of 0.5dB 00 0000: MUTE 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain ... 11 1110: 30.5dB gain 11 1111: 31dB gain | |

Figure 90:
ANC_R3 Register Description

| Name | | Address | | Default Value |
|--|--------------------|----------|--------|--|
| ANC_R3 | | 0x13 | | 00h |
| <p>The ANC_R3 Register configures the gain for the right microphone input. This register is the second alternative microphone gain register for OTP programming in case the ANC_R and ANC_R2 registers are already programmed.</p> | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | ALT3_ENABLE | 0 | R/W | <p>In case the register is being used for microphone programming this bit has to be set. The bit is being used by the internal state machine of the AS3415/35 to determine which alternative microphone gain register has to be used during startup.</p> <p>0: Microphone registers 0x12 and 0x13 are not active</p> <p>1: Microphone registers 0x12 and 0x13 are active. Gain settings in registers 0x30, 0x31, 0x10 and 0x11 are ignored.</p> |
| 5:0 | MICR_VOL_OTP3<6:0> | 000 0000 | R/W | <p>Volume settings for left microphone input, adjustable in 63 steps of 0.5dB</p> <p>00 0000: 0dB 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain ... 11 1110: 30.5dB gain 11 1111: 31dB gain</p> |

Figure 91:
ANC_MODE Register Description

| Name | | Address | | Default Value |
|---|--------------|---------|--------|---|
| ANC_MODE | | 0x14 | | 00h |
| The ANC_MODE register controls various settings for the chipset in active noise cancelling mode like which amplifiers are enabled as well as which audio inputs are active. | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7:6 | HPH_MUX<1:0> | 00 | R/W | This register selects the ANC input source for the headphone amplifier in ANC mode. Depending on the register setting the outputs of microphone preamplifier, OPAMP1, OPAMP2 can be connected to the headphone amplifier input. It is also possible to disconnect all ANC input sources which is sometimes desired in monitor mode. 00: QMIC outputs are connected to HPH input 01: OP1 outputs are connected to HPH input 10: OP2 outputs are connected to HPH input 11: Nothing connected to HPH input except line input and mixer input in case they are enabled. |
| 5 | LIN_MUTE | 0 | R/W | This bit defines the status of the line input mute switch in active noise cancelling mode. If the bit is set to '1' the line input amplifier is disconnected from the headphone amplifier. 0: Line input connected to headphone amplifier 1: Line input not connected to headphone amplifier |
| 4 | MIX_ENABLE | 0 | R/W | This bit enables the headphone mixer input pin to mix external signals to the headphone amplifier in active noise cancelling mode. 0: HPH mixer input disabled 1: HPH mixer input enabled |
| 3 | OP2L_ON | 0 | R/W | This register enables the left channel of OPAMP 2 in ANC mode. 0: Left OP2 is switched off 1: Left OP2 is switched on |
| 2 | OP2R_ON | 0 | R/W | This register enables the right channel of OPAMP 2 in ANC mode. 0: Right OP2 is switched off 1: Right OP2 is switched on |
| 1 | OP1L_ON | 0 | R/W | This register enables the left channel of OPAMP 1 in ANC mode. 0: Left OP1 is switched off 1: Left OP1 is switched on |
| 0 | OP1R_ON | 0 | R/W | This register enables the right channel of OPAMP 1 in ANC mode. 0: Right OP1 is switched off 1: Right OP1 is switched on |

Figure 92:
MONITOR_MODE Register Description

| Name | | Address | Default Value | |
|--|------------------|---------|---------------|---|
| MONITOR_MODE | | 0x15 | 00h | |
| The MONITOR_MODE register controls various settings for the chipset in monitor mode like line input monitor mode attenuation as well as which audio inputs are active. | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7:6 | MON_HPH_MUX<1:0> | 00 | R/W | This register selects the ANC input source for the headphone amplifier in monitor mode. Depending on the register setting the outputs of microphone preamplifier, OPAMP1, OPAMP2 can be connected to the headphone amplifier input. 00: QMIC outputs are connected to HPH input 01: OP1 outputs are connected to HPH input 10: OP2 outputs are connected to HPH input 11: Nothing connected to HPH input except line input and mixer input in case they are enabled. |
| 6 | MON_LIN_MUTE | 0 | R/W | This bit defines the status of the line input mute switch in monitor mode. If the bit is set to '1' the line input amplifier is disconnected from the headphone amplifier. 0: Line Input Mute disabled 1: Line Input Mute enabled |
| 5 | MON_MIX_ENABLE | 0 | R/W | This bit enables the headphone mixer input pin to mix external signals to the headphone amplifier in playback only mode. 0: HPH mixer input disabled 1: HPH mixer input enabled |
| 3:2 | MON_LIN_ATT<1:0> | 00 | R/W | This register controls the line put gain in monitor mode. Per default the line input is muted. With this register it can be attenuated from -30dB up to -36dB in 6dB steps. 00: 0dB line input gain in monitor mode 01: -24dB line input gain in monitor mode 10: -30dB line input gain in monitor mode 11: -36dB line input gain in monitor mode |
| 1 | SLIDER_MON | 0 | R/W | This bit enables the Full Slider Mode configuration. Please mind that this bit must not be set without setting SLIDE_PWR_UP to '1'. 0: Slider Mode activated 1: Full Slider Mode activated |
| 0 | DISABLE_MONITOR | 0 | R/W | This bit disables the monitor mode in push button control mode. 0: Monitor mode enabled 1: Monitor mode disabled |

Figure 93:
PBO_MODE Register Description

| Name | | Address | | Default Value |
|--|----------------|---------|--------|--|
| PBO_MODE | | 0x16 | | 00h |
| The ANC_MODE register controls various settings for the chipset in playback mode like which amplifiers are enabled as well as which audio inputs are active. | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | TEST_BIT_4 | 1 | R | Test register. Please do not write this register. |
| 6 | NO_PBO | 0 | R/W | This bit disables the playback only mode function. No external pull up resistor is required on ANC / CSDA pin is necessary if this bit is set to '1' 0: Playback only mode enabled 1: Playback only mode disabled |
| 5 | PBO_LIN_MUTE | 0 | R/W | This bit defines the status of the line input mute switch in playback only mode. If the bit is set to '1' the line input amplifier is disconnected from the headphone amplifier. 0: Line Input Mute disabled 1: Line Input Mute enabled |
| 4 | PBO_MIX_ENABLE | 0 | R/W | This bit enables the eco mode of the microphone preamplifier. 0: Power save function disabled 1: Power save function enabled |
| 3 | PBO_OP2L_ON | 0 | R/W | This register enables the left channel of OPAMP 2 in playback only mode. 0: Left OP2 is switched off 1: Left OP2 is switched on |
| 2 | PBO_OP2R_ON | 0 | R/W | This register enables the right channel of OPAMP 2 in playback only mode. 0: Right OP2 is switched off 1: Right OP2 is switched on |
| 1 | PBO_OP1L_ON | 0 | R/W | This register enables the left channel of OPAMP 1 in playback only mode. 0: Left OP2 is switched off 1: Left OP2 is switched on |
| 0 | PBO_OP1R_ON | 0 | R/W | This register enables the right channel of OPAMP 1 in playback only mode. 0: Right OP2 is switched off 1: Right OP2 is switched on |

Figure 94:
ECO Register Description

| Name | | Address | Default Value | |
|--|------------------|---------|---------------|--|
| ECO | | 0x17 | 0x00 | |
| This register controls the economic (ECO) mode for all analog audio blocks. Furthermore it includes also LED control and other general settings. | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | SLIDE_PWR_UP | 0 | R/W | This bit enables the slide switch control mode of the AS3515/35. If this bit is programmed the device can be powered up and powered down via a slide switch. 0: Slide switch control disabled 1: Slide switch control enabled |
| 6 | LOWBAT_100 | 0 | R/W | This bit increases the LED low battery indication level by 100mV. 0: Default LED indication level (0.95V) 1: Increased LED indication level (1.05V) |
| 5:4 | ILED<1:0> | 00 | R/W | This register defines the driving strength of the ILED pin for LED control. 00: Current sink switched off 01: 25% 10: 50% 11: 100% |
| 3 | ENABLE_HPH_ECO | 0 | R/W | This bit enables the eco mode of the headphone amplifier. 0: Power save function disabled 1: Power save function enabled |
| 2 | ENABLE_MIC_ECO | 0 | R/W | This bit enables the eco mode of the microphone amplifier. 0: Power save function disabled 1: Power save function enabled |
| 1 | ENABLE_LIN_ECO | 0 | R/W | This bit enables the eco mode of the line input amplifier. 0: Power save function disabled 1: Power save function enabled |
| 0 | ENABLE_OPAMP_ECO | 0 | R/W | This bit enables the eco mode of the operational amplifier amplifiers for ANC filter design. 0: Power save function disabled 1: Power save function enabled |

Figure 95:
ANC_L Register Description

| Name | | Address | | Default Value | |
|---|---------------|----------|--------|--|--|
| ANC_L | | 0x30 | | 80h | |
| The ANC_L Register configures the gain for the left microphone input. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | TEST_BIT_5 | 1 | R/W | Please do not write this register. | |
| 5:0 | MICL_VOL<5:0> | 000 0000 | R/W | Volume settings for left microphone input, adjustable in 63 steps of 0.5dB 00 0000: MUTE 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain ... 11 1110: 30.5dB gain 11 1111: 31dB gain | |

Figure 96:
ANC_R Register Description

| Name | | Address | | Default Value | |
|---|-------------------|----------|--------|---|--|
| ANC_R | | 0x31 | | 0x80 | |
| The ANC_R Register configures the gain for the left microphone input. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | TEST_BIT_6 | 1 | R/W | Please do not write this register. | |
| 5:0 | MICR_VOL_OTP<5:0> | 000 0000 | R/W | Volume settings for right microphone input, adjustable in 63 steps of 0.5dB 00 0000: MUTE 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain ... 11 1110: 30.5dB gain 11 1111: 31dB gain | |

Figure 97:
MIC_MON_L Register Description

| Name | | Address | | Default Value | |
|---|---------------|---------|--------|---|--|
| MIC_MON_L | | 0x32 | | 0x00 | |
| This register controls the microphone gain in monitor mode for the left microphone channel. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 5:0 | MICL_MON<5:0> | 00 0000 | R/W | Monitor mode gain setting for left microphone input adjustable in 63 steps of 0.5dB 00 0000: MUTE 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain ... 11 1110: 30.5dB gain 11 1111: 31dB gain | |

Figure 98:
MIC_MON_R Register Description

| Name | | Address | | Default Value | |
|--|-------------------|---------|--------|--|--|
| MIC_MON_R | | 0x33 | | 0x00 | |
| This register controls the microphone gain in monitor mode for the right microphone channel. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 5:0 | MICR_MON_OTP<5:0> | 00 0000 | R/W | Monitor mode gain setting for right microphone input adjustable in 63 steps of 0.5dB 00 0000: MUTE 00 0001: 0.5dB gain 00 0010: 1dB gain 00 0011: 1.5dB gain ... 11 1110: 30.5dB gain 11 1111: 31dB gain | |

Figure 99:
MODE_1 Register Description

| Name | | Address | | Default Value | |
|---|---------------|---------|--------|---|--|
| MODE_1 | | 0x34 | | 0x00 | |
| This register controls miscellaneous settings of the AS3515/35. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 7 | MICS_CP_OFF | 0 | R/W | This bit controls the microphone supply charge pump. The microphone charge pump has a second function besides the bias voltage generation for microphones. It is also used to disable the integrated music bypass switch if the AS3415/35 is active. In case the integrated bypass switch is used in an application the MICS_CP_OFF bit must not be set to '1'. 0: Microphone supply charge pump enabled 1: Microphone supply charge pump disabled | |
| 6 | MICS_OFF | 0 | R/W | This bit controls the microphone supply. In case this bit is set to '1' the MICS pin is disconnected from the internal microphone supply. 0: Microphone supply switched on 1: Microphone supply switched off | |
| 5 | MIC_AGC_ON | 0 | R/W | This bit disables the automatic gain control of the microphone preamplifier. 0: AGC disabled 1: AGC enabled | |
| 4 | MIC_OFF | 0 | R/W | This bit powers down the microphone preamplifier. 0: Microphone preamplifier enabled 1: Microphone preamplifier disabled | |
| 3 | NO_LOWBAT_OFF | 0 | R/W | This bit disables the automatic power down function of the device with a low battery condition. 0: Low battery shutdown enabled 1: Low battery shutdown disabled | |
| 2 | CP_OFF | 0 | R/W | This bit disables the V _{NEG} charge pump in case there is already a negative supply present in a system. 0: V_{NEG} charge pump enabled 1: V _{NEG} charge pump enabled | |
| 1 | HPH_OFF | 0 | R/W | This bit allows the user to power down headphone amplifier in case it is not used in the final application in order to save system power. 0: Headphone amplifier enabled 1: Headphone amplifier disabled | |
| 0 | LIN_OFF | 0 | R/W | This bit allows the user to power down the line input preamplifier in case it is not used in the final application in order to save system power. 0: Line Input amplifier enabled 1: Line Input amplifier disabled | |

Figure 100:
MODE_2 Register Description

| Name | | Address | | Default Value |
|---|---------------|---------|--------|--|
| MODE_2 | | 0x35 | | 0x00 |
| This register controls miscellaneous settings of the AS3515/35. | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | TEST_BIT_7 | 1 | R/W | Test register. Please do not write this register. |
| 3 | MICS_DC_OFF | 0 | R/W | This bit disables the internal microphone supply discharge function if the microphone supply is switched off. 0: MICS discharge enabled 1: MICS discharge disabled |
| 2 | DELAY_HPH_MUX | 0 | R/W | With this bit it is possible to delay the HPH_MUX setting during startup of the device to avoid unwanted pop noise in case of long charging times of external components. 0: HPH_MUX_OTP delay disabled 1: HPH_MUX_OTP delay enabled |
| 1 | HPH_MODE | 0 | R/W | This register controls the operating mode of the headphone amplifier. The headphone amplifier supports single ended mode and differential mode. In differential output mode the right audio signal path is the active input signal for the headphone amplifier. 0: Stereo single ended mode 1: Mono differential mode |
| 0 | I2C_MODE | 0 | R/W | This bit enables I ² C power down of the AS3415/35. 0: I²C power down disabled 1: I ² C power down enabled via PWR_HOLD bit. |

Evaluation Registers

Figure 101:
EVAL Register Description

| Name | | Address | | Default Value |
|--|-------------------|---------|--------|---|
| EVAL | | 0x3D | | 0x00 |
| <p>This register enables miscellaneous operating modes, that are typically controlled via slide switch or push button, for evaluation purposes or MCU controlled applications.</p> | | | | |
| Bit | Bit Name | Default | Access | Bit Description |
| 7 | EVAL_ON | 0 | R/W | Function to be defined. |
| 5 | MASTER_LIN_MUTE | 0 | R/W | <p>This register is the master register for the line input mute function. No matter in what operating mode the device is working the LINE_MUTE bit overrules any other setting in any operation mode.</p> <p>0: Line Input master mute disabled 1: Line Input master mute enabled</p> |
| 4 | MASTER_MIX_ENABLE | 0 | R/W | <p>This register is the master register for the mixer input function. No matter in what operating mode the device is working the MASTER_MIX_ENABLE bit overrules any other setting in any operation mode.</p> <p>0: Line Input master mute disabled 1: Line Input master mute enabled</p> |
| 3 | MON_MODE | 0 | R/W | <p>This bit enables the monitor mode of AS3415/35 which can normally be enabled by pulling the MODE pin to $V_{BAT}/2$. In case an MCU is connected to the device the Monitor mode can be enabled by setting this bit.</p> <p>0: Monitor mode deactivated 1: Monitor mode activated</p> |
| 2 | PBO_MODE | 0 | R/W | <p>This bit enables the playback mode of AS3415/35 which can normally be enabled by pulling the ANC pin to 0V. In case an MCU is connected to the device the Monitor mode can be enabled by setting this bit.</p> <p>0: Monitor mode deactivated 1: Monitor mode activated</p> |
| 1 | MICL_MUTE | 0 | R/W | <p>This register is the master mute register for the left microphone amplifier. No matter in what operating mode the device is working the MICL_MUTE bit overrules any other setting in any operation mode.</p> <p>0: Mute disabled 1: Mute enabled</p> |
| 0 | MICR_MUTE | 0 | R/W | <p>This register is the master mute register for the left microphone amplifier. No matter in what operating mode the device is working the MICR_MUTE bit overrules any other setting in any operation mode.</p> <p>0: Mute disabled 1: Mute enabled</p> |

Figure 102:
CONFIG_1 Register Description

| Name | | Address | | Default Value | |
|---|-----------|---------|--------|---|--|
| CONFIG_1 | | 0x3E | | 0x00 | |
| This bit controls the OTP programming clock source. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 3 | EXTBURNCL | 0 | R/W | This register controls the clock source for OTP programming. Typically the internal clock is being used for OTP programming. 0: External burn clock disabled 1: External burn clock enabled | |

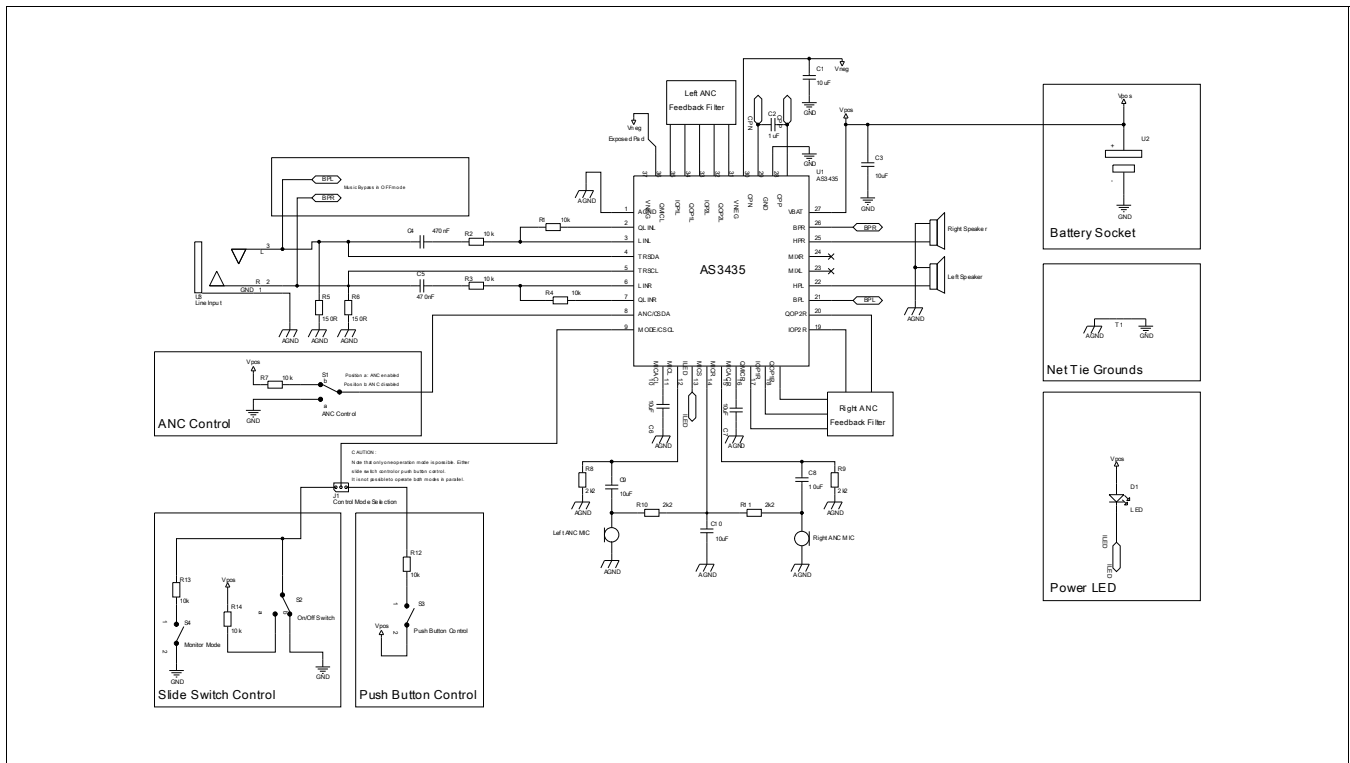
Figure 103:
CONFIG_2 Register Description

| Name | | Address | | Default Value | |
|--|-------------|---------|--------|--|--|
| CONFIG_2 | | 0x3F | | 0x00 | |
| This register controls the register access to all OTP registers. In order to get access to these registers it is necessary to set REG3F_ON bit to '1'. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 5 | TM34 | 0 | R/W | This Register defines the register bank selection for register 0x30-0x35 and 0x10-0x17. Depending on TM34 you can select either between Register bank 0x10-0x17 or 0x30h-0x34. 0: Test mode Registers 14h-17h and 10h-13h disabled test mode Registers 30h-33h and 34h-37h enabled 1: Test mode Registers 14h-17h and 10h-13h enabled test mode Registers 30h-33h and 34h-37h disabled | |
| 4 | BURNSW | 0 | R/W | This register controls the internal buffer switch from line input to V _{NEG} for V _{NEG} buffering during OTP programming. 0: BURN switch disabled 1: BURN switch enabled | |
| 3 | TM_REG34-35 | 0 | R/W | 0: Register 34h-35h disabled Register 14h-17h disabled 1: Register 34h-35h enabled Register 14h-17h enabled | |
| 2 | TM_REG30-33 | 0 | R/W | 0: Register 30h-33h disabled Register 10h-13h disabled 1: Register 30h-33h enabled Register 10h-13h enabled | |

| Name | | Address | | Default Value | |
|--|---------------|---------|--------|--|--|
| CONFIG_2 | | 0x3F | | 0x00 | |
| This register controls the register access to all OTP registers. In order to get access to these registers it is necessary to set REG3F_ON bit to '1'. | | | | | |
| Bit | Bit Name | Default | Access | Bit Description | |
| 1:0 | OTP_MODE<1:0> | 00 | R/W | This register controls the OTP access. 00: READ 01: LOAD 10: WRITE 11: BURN | |

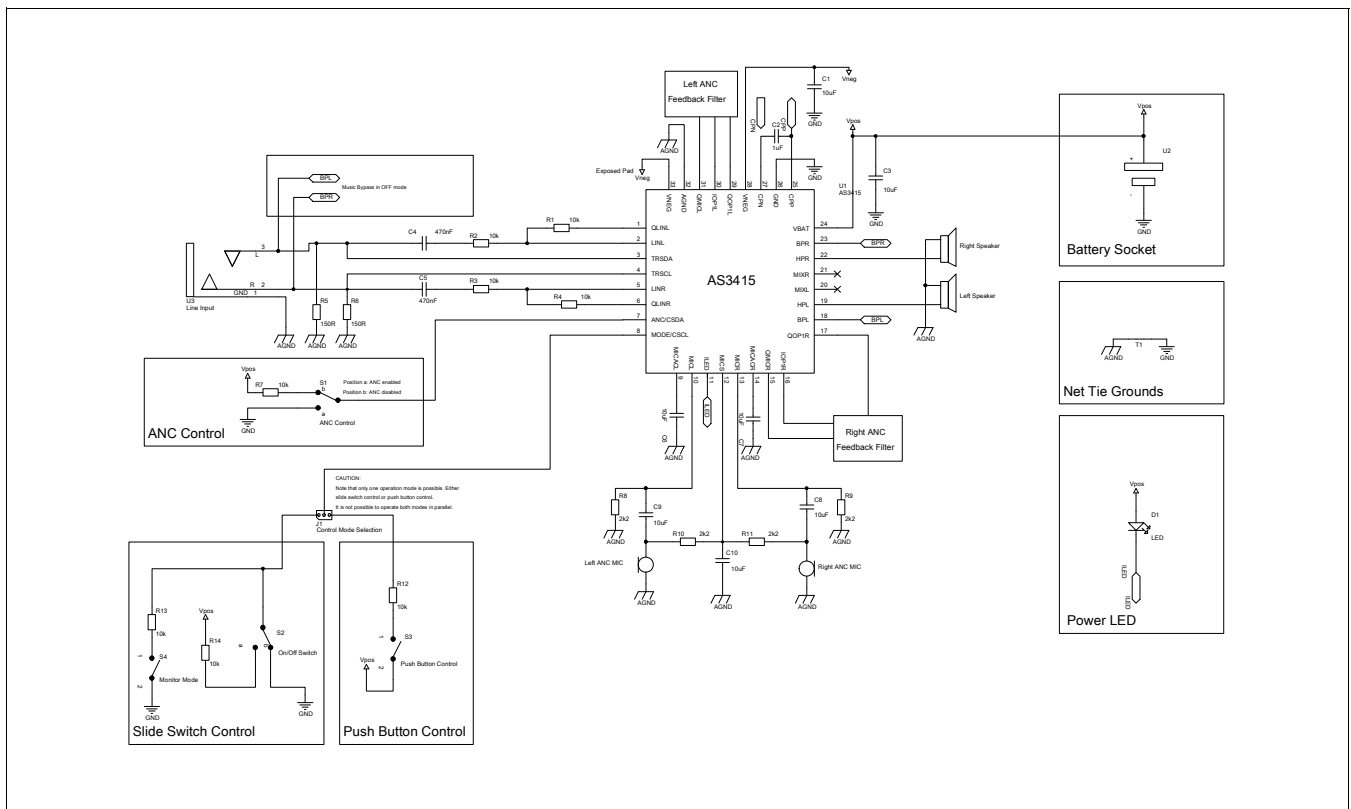
Application Information

Figure 104:
AS3435 Stereo Feedback Application Example



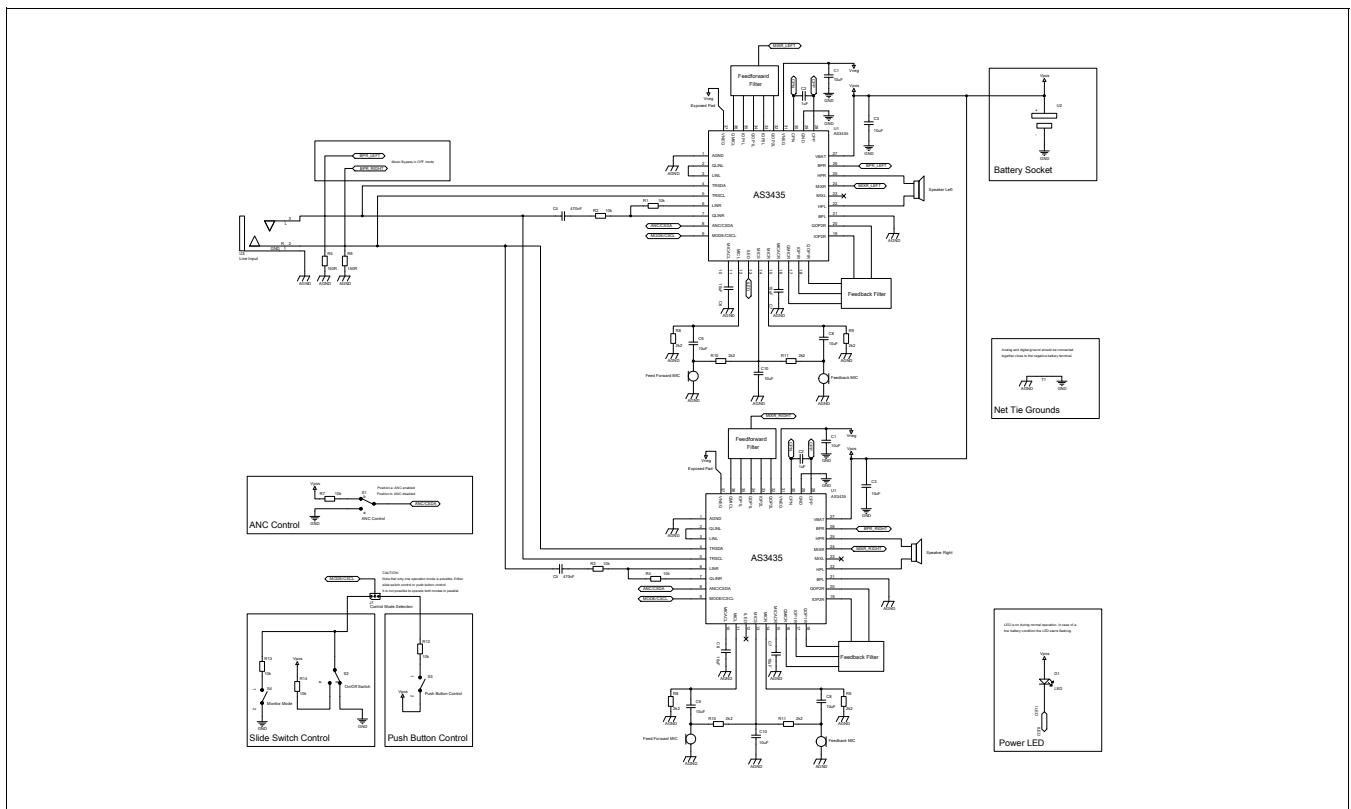
AS3435 Stereo Feedback Example: This application example shows a single AS3435 in feedback configuration with activated music bypass mode in off mode.

Figure 105:
AS3415 Stereo Feed Forward Application Example



AS3415 Stereo Feed-forward Example: This application example shows a single AS3415 in feed-forward configuration with activated music bypass mode in off mode.

Figure 106:
AS3435 Hybrid Application Example



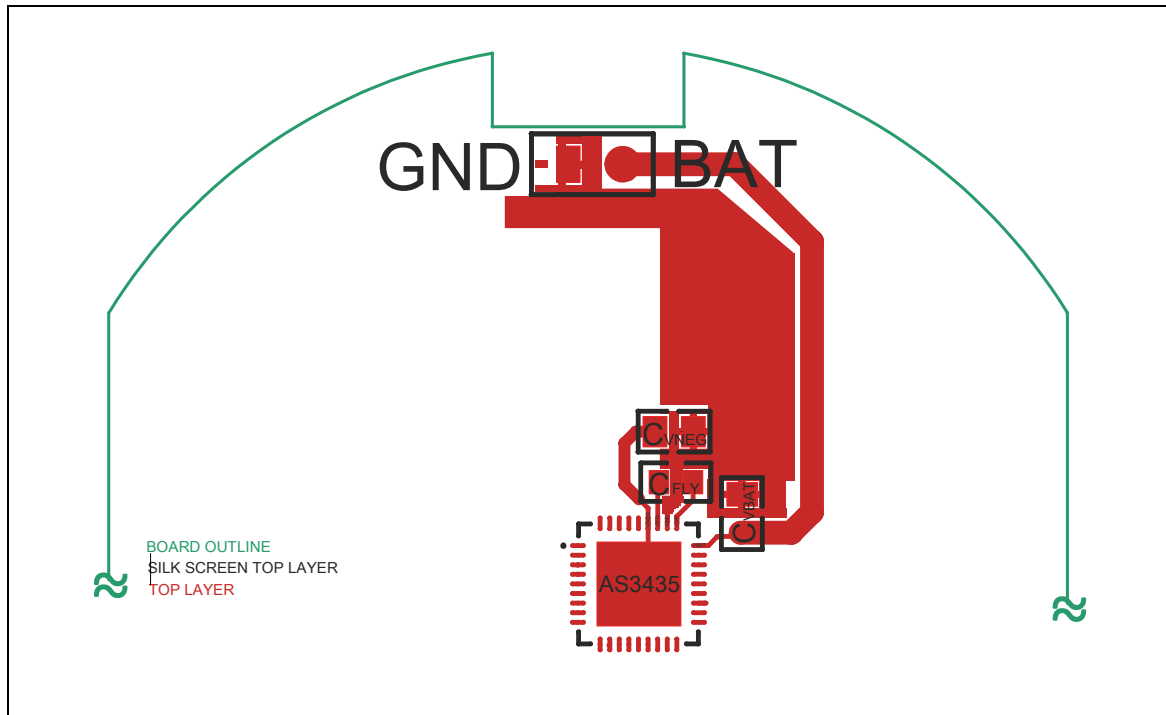
AS3435 Hybrid Example: This application example shows two AS3435 in hybrid configuration with activated music bypass mode in off mode.

PCB Layout Recommendation

Charge Pump

The Printed Circuit Board (PCB) layout of the charge pump is essential for good audio performance. The layout recommendation shown in Figure 107 shows the most important components of the charge pump. These are C_{VBAT} , C_{FLY} , C_{VNEG} and the battery terminal. To guarantee lowest output noise all three capacitors must be placed as close as possible to the related pin on the AS3435/15 as shown in Figure 1 & Figure 107. Additionally, it is recommended that the ground pins on C_{VNEG} , C_{VBAT} and the AS3435/15 charge pump pin (GND) have a short connection to each other. This will avoid distribution of high frequency switching currents over the PCB. All the ground pins should be connected with a single ground plane or at least a strong connection directly to the battery terminal. The layout example shown in Figure 107 makes use of a ground plane on the top layer that is directly connected to the negative battery terminal to feature a star shaped ground concept.

Figure 107:
Charge Pump Layout Recommendation



AS3435 Charge Pump Layout Recommendation: This diagram shows the layout recommendation of the AS3435 charge pump.

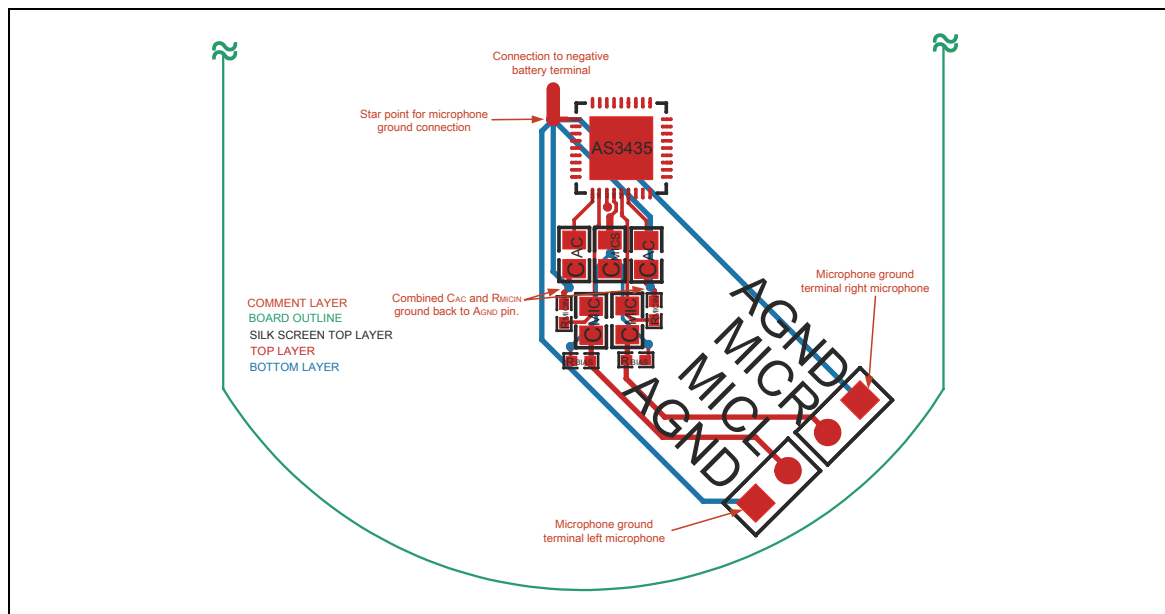
Charge Pump Ground Layout:

It is important to minimize the ground loops between all charge pump components and AGND pin. A dedicated ground plane with a connection back to the negative battery terminal should be used.

Microphone

For the microphone preamplifier layout the designer must pay special attention; the combination of bad layout and gain values up to +20dB can cause unwanted noise. To minimize noise, a layout example is shown in Figure 108 which is based on the schematic shown in Figure 20. All microphone related components which include DC blocking capacitors, bias resistors as well as high pass filter components should be placed according to Figure 108. Once the component placement is done it is important to route the different ground connections of all components correctly. For the microphone preamplifier a local star shaped ground concept should be used, with AGND pin defined as star point. Basically we have two important ground pairs. The first are the microphone grounds next to MICR and MICL terminals. These ground pins need a separate ground connection back to the AS3515/35 AGND pin. A separate left and right ground line is recommended rather than using a single microphone ground line back to the star point at AGND. The second important connections are the ground terminals of C_{AC} and R_{MICIN} . They should be fed back to the AGND pin. Figure 108 shows the separation of left and right channel. The ground pads of C_{AC} and R_{MICIN} are connected together and routed back to AGND pin of AS3415/35.

Figure 108:
Microphone Layout Recommendation



AS3415/35 Microphone Layout Recommendation: This diagram shows the layout recommendation for the AS3415/35 microphone preamplifier with all necessary peripheral components for operation.

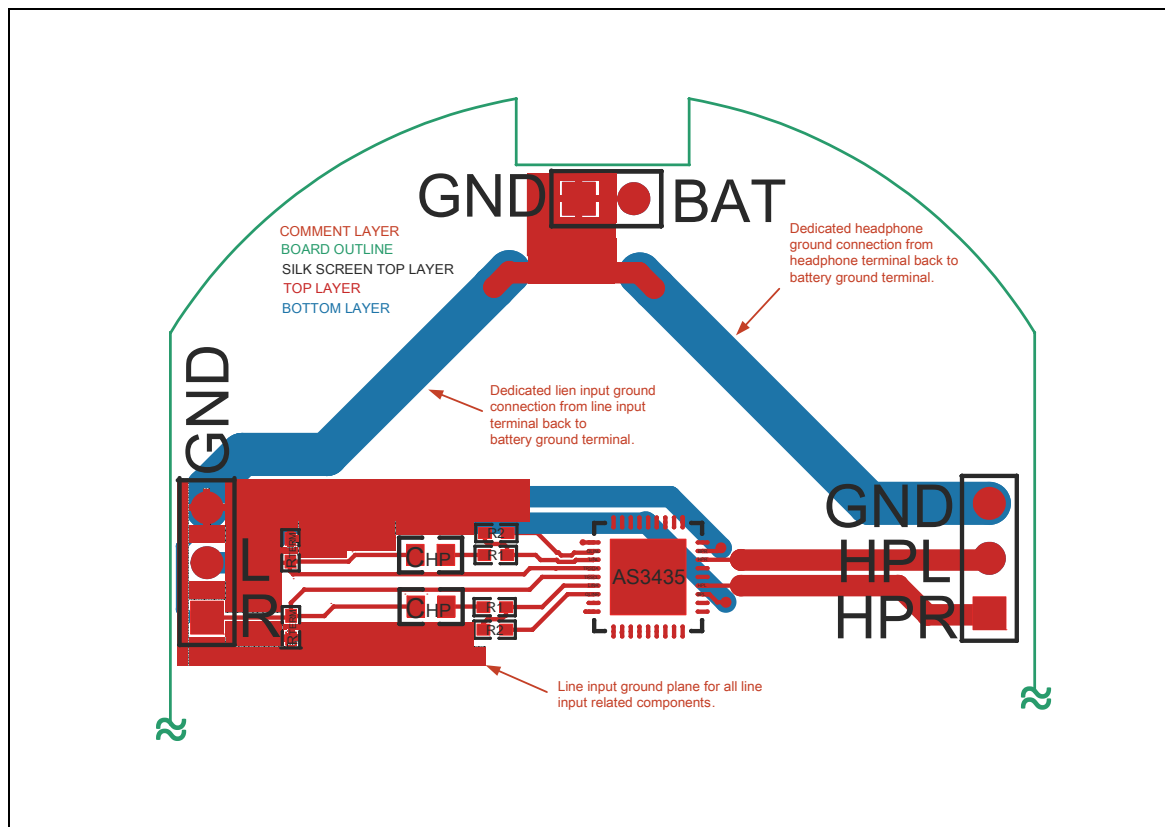
Microphone Ground Layout:

Use separate ground connections for microphone inputs back to the AGND pin. The ground connection of C_{AC} and R_{MICIN} should also make use of a dedicated connection back to AGND pin of AS3415/35.

Line Input and Headphone

The line input- and the headphone amplifier are blocks with higher system currents; therefore it is important to separate these high input and output currents from the rest of the system. The example shown in [Figure 109](#) demonstrates how to do a proper ground layout for both blocks. To separate the headphone amplifier from the rest of the system it is recommended to route a dedicated ground connection from the headphone amplifier terminal back to the battery ground terminal of the device. With this separate ground connection the high output currents of the headphone amplifier do not influence the sensitive analog ground of the chipset. The same layout technique is applicable for the line input amplifier. The line input amplifier also has higher input currents because of the 150Ω termination resistors (R_{TERM}) connected to the line input terminal shown in [Figure 10](#). To avoid unwanted ground currents influencing the sensitive analog system ground of the AS3415/35, it is recommended to route a dedicated ground connection from the line input terminal back to the negative battery terminal of the PCB. The example shows a local ground plane from the battery, to the line input terminals. Such a plane should be used for more complicated line input filters. Thus, all line input related components like R_{TERM} , C_{HP} , R_1 and R_2 as well as other additional filter components should be connected to this ground plane. The ground plane must be connected to the battery terminal, at a single point, for best grounding effect. Another important connection is the bypass connection from line input terminal to the BPL and BPR pins of the AS3415/35. This connection is active if the chip is in off mode or if the device has run out of battery. It is important to use wide signal lines for these connections. The wider these connections are, the better it is for the application. The same is true for the ground connections of the headphone amplifier and the line input amplifier. A weak signal line can directly influence the channel separation of the system. A minimum signal width of 1mm is typically recommended for the left and right audio channels and 2mm for the audio ground signals.

Figure 109:
Line Input and Headphone Layout Recommendation



AS3415/35 Line Input and HPH Layout recommendation: This diagram shows the layout recommendation of the AS3415/35 line input amplifier and the headphone amplifier.

Headphone Layout:

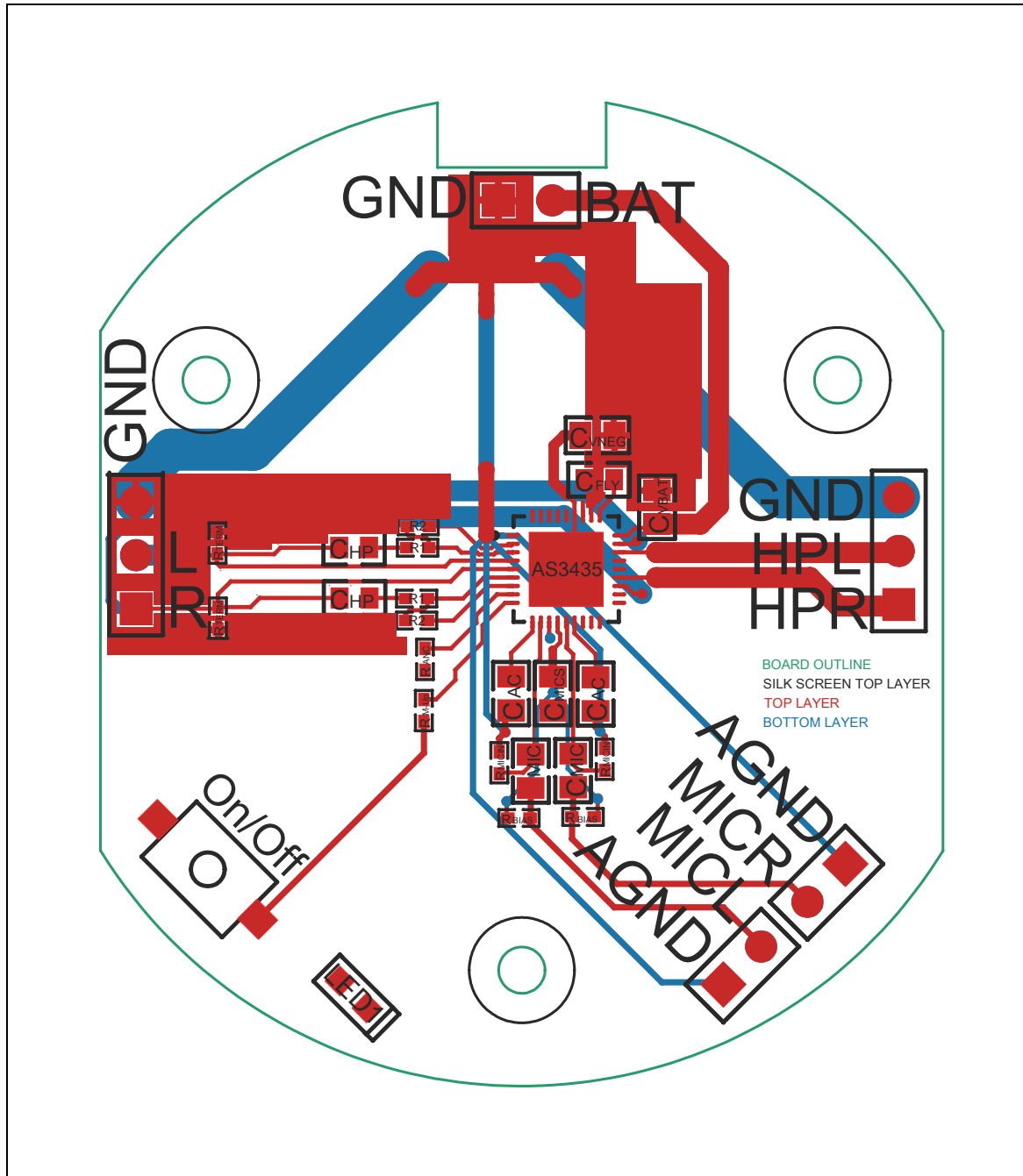
Use wide signal lines for line input ground, headphone ground and signal lines as well as for the music bypass lines. A weak signal line on any of these connections can influence channel separation of the device.

AS3435 Complete Layout Example

Layout Recommendations:
 All layout recommendations given in the examples are also applicable for the AS3415!

The combination of all layout recommendations given in the previous chapters are shown in Figure 110. It also includes a push button for on/off control and a status indication LED. It is important to say that all layout recommendations are also applicable for the AS3515.

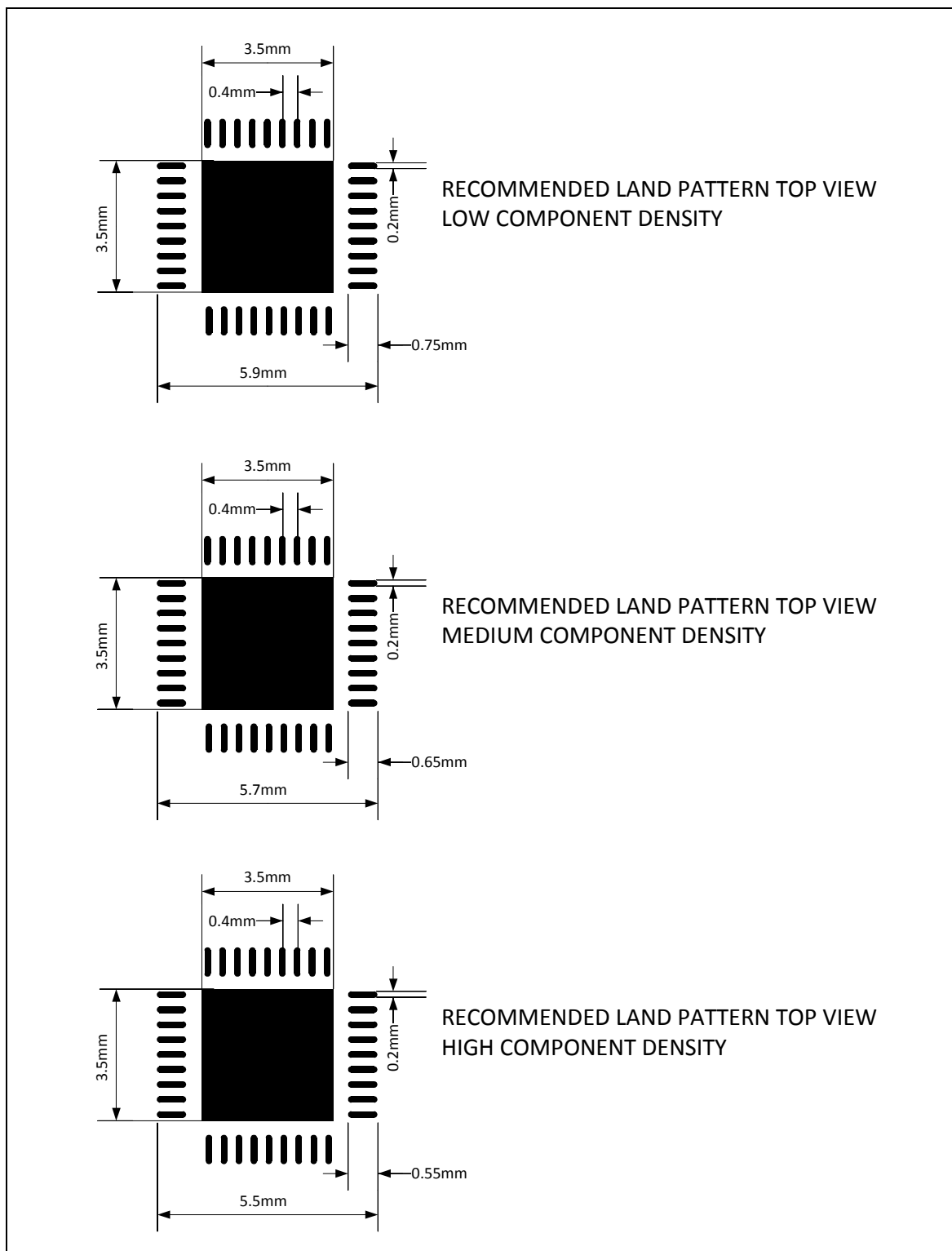
Figure 110:
 AS3435 Over the Ear Layout Example



AS3435 over the ear layout example: This diagram shows the combination of all layout recommendations of a PCB. The PCB outline is based on an over the ear headset.

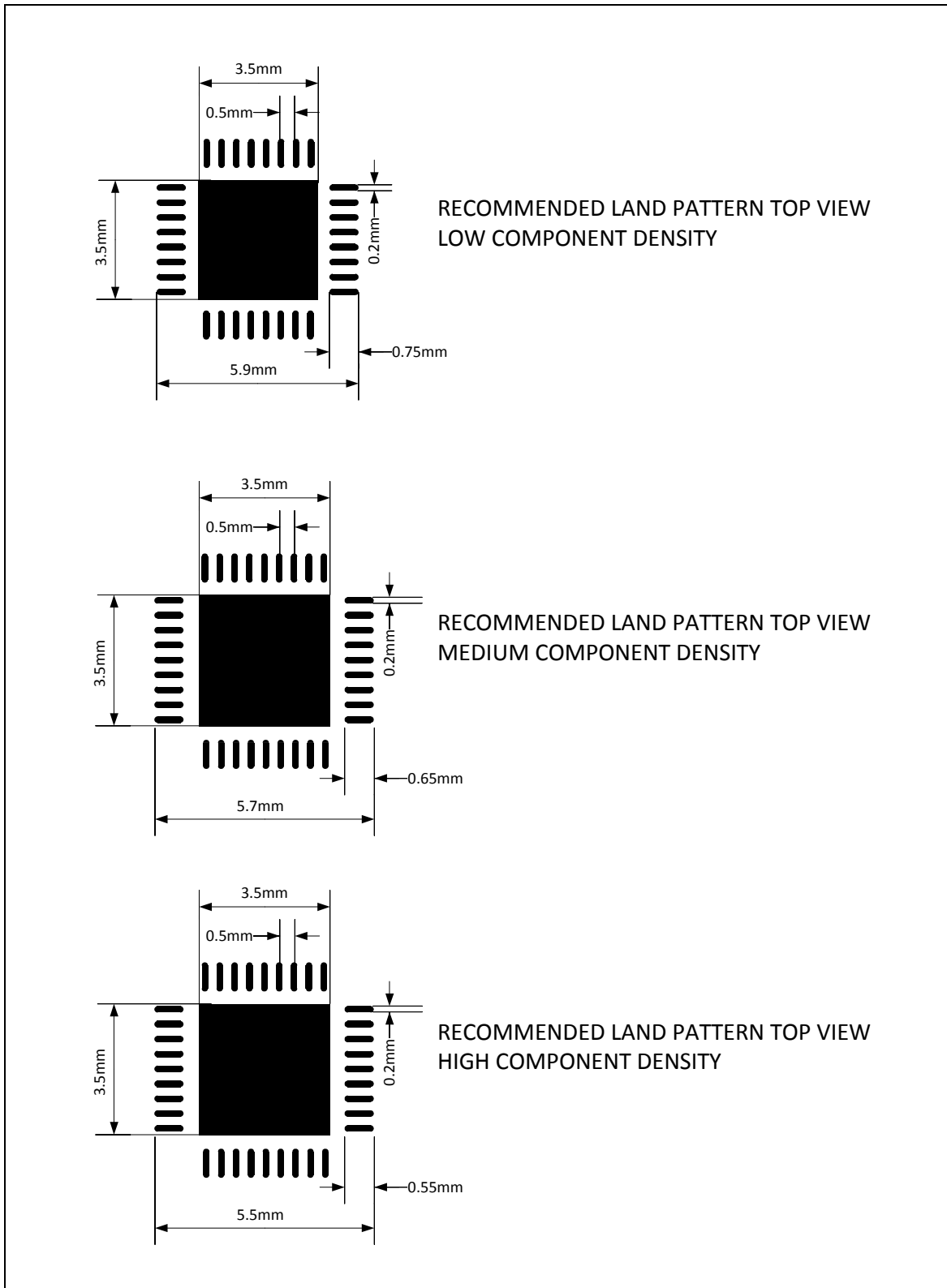
PCB Pad Layout

Figure 111:
AS3435 PCB Pad Layout Recommendation



AS3435 PCB Pad Layout: This drawing shows the PCB footprint layout recommendation for three different component density levels.

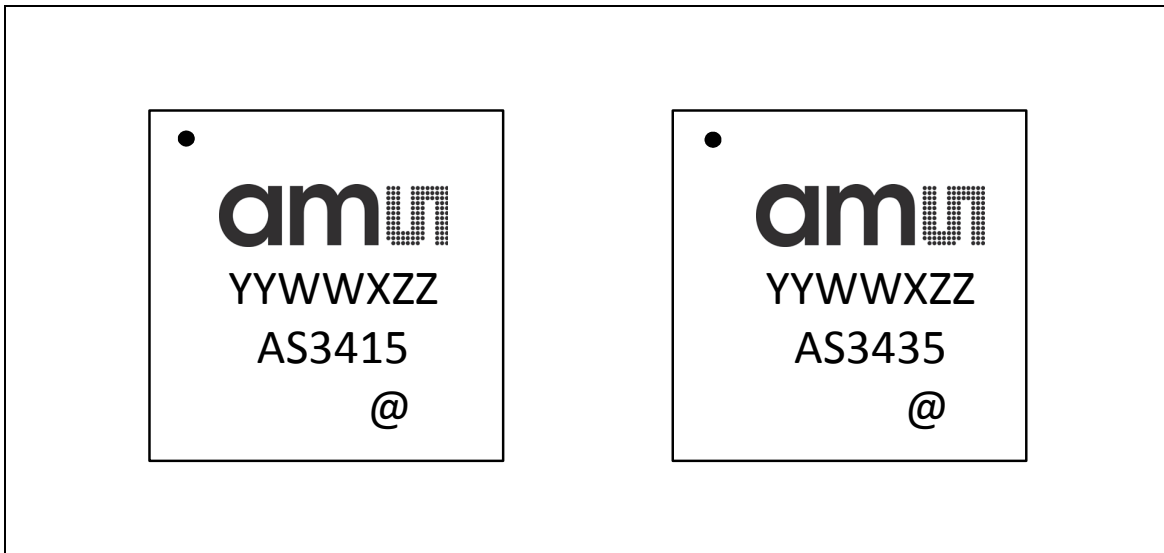
Figure 112:
AS3415 PCB Pad Layout Recommendation



AS3415 PCB Pad Layout: This drawing shows the PCB footprint layout recommendation for three different component density levels.

Package Drawings & Markings

Figure 113:
QFN Marking

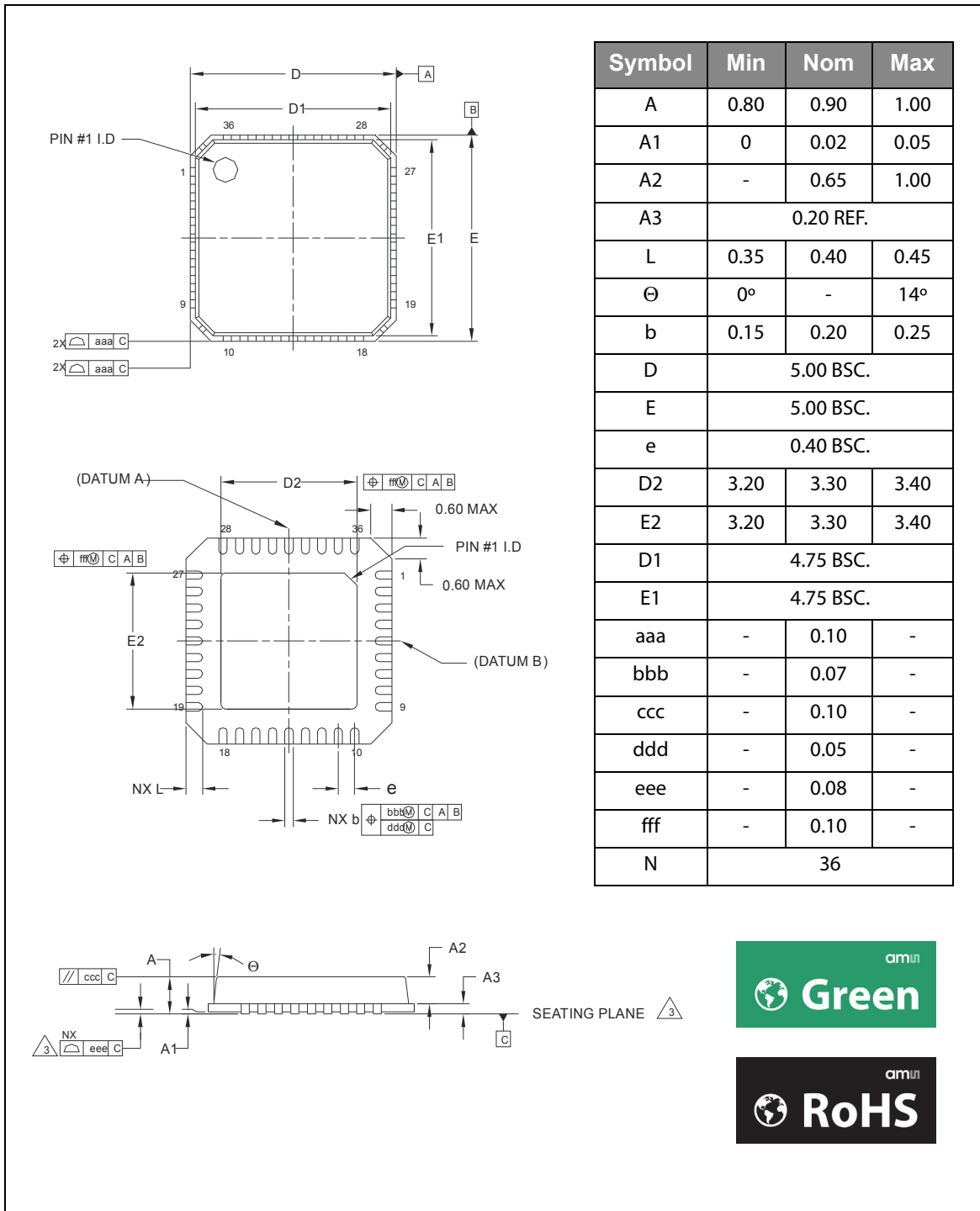


QFN Marking: Shows the package marking of the QFN product version.

Figure 114:
Package Code YYWWIZZ

| YY | WW | X | ZZ |
|-----------------------------|--------------------|------------------|--------------------------------|
| Last two digits of the year | Manufacturing week | Plant identifier | Free choice/ traceability code |

Figure 115:
AS3435, 36-pin QFN, 0.4mm Pitch

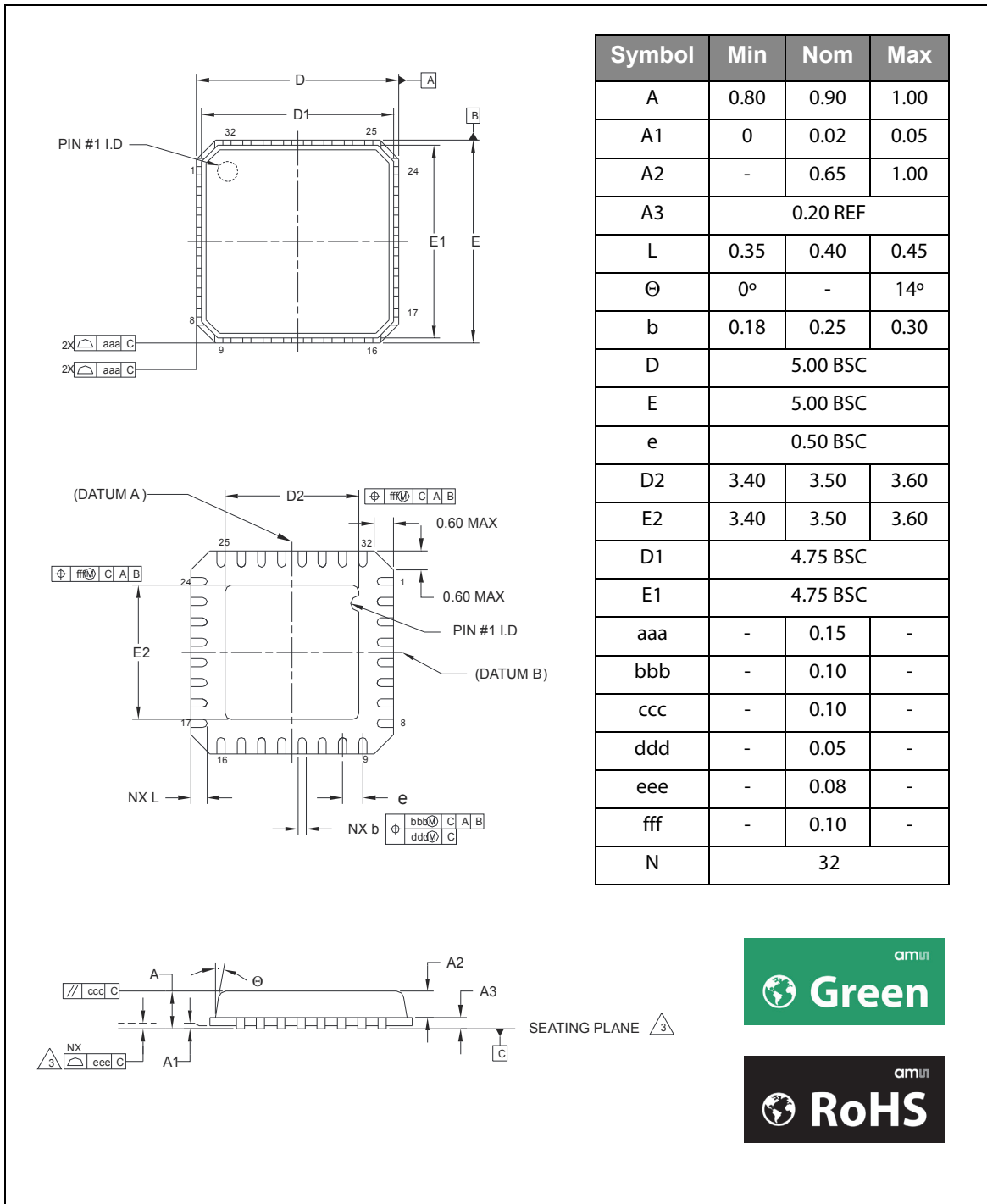


Note(s) and/or Footnote(s):

1. Dimensioning & tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.



Figure 116:
AS3415, 32-pin QFN, 0.5mm Pitch



Note(s) and/or Footnote(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Coplanarity applies to the exposed heat slug as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.



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Ordering & Contact Information

Figure 117:
Ordering Information

| Ordering Code | Description | Delivery Form | Package |
|---------------|---|---|------------------------------------|
| AS3415-EQFP | Enhanced Low Noise Active Noise Cancelling Speaker Driver | Tape & Reel dry pack with 4000 pcs per reel | QFN 32 [5.0x5.0x0.9mm] 0.5mm pitch |
| AS3415-EQFM | Enhanced Low Noise Active Noise Cancelling Speaker Driver | Tape & Reel dry pack with 500 pcs per reel | QFN 32 [5.0x5.0x0.9mm] 0.5mm pitch |
| AS3435-EQFP | Enhanced Low Noise Active Noise Cancelling Speaker Driver | Tape & Reel dry pack with 4000 pcs per reel | QFN 36 [5.0x5.0x0.9mm] 0.4mm pitch |
| AS3435-EQFM | Enhanced Low Noise Active Noise Cancelling Speaker Driver | Tape & Reel dry pack with 500 pcs per reel | QFN 36 [5.0x5.0x0.9mm] 0.4mm pitch |

Ordering Information: Shows the ordering information of the different packaging versions of the AS3415 and AS3435.

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- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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