LMC7101/LMC7101Q Tiny Low Power Operational Amplifier with Rail-to-Rail Input and Output

Check for Samples: LMC7101, LMC7101Q

FEATURES

- **Tiny 5-Pin SOT-23 Package Saves Space—Typical Circuit Layouts Take Half the Space of 8-Pin SOIC Designs**
- **Guaranteed Specs at 2.7V, 3V, 5V, 15V Supplies**
- **Typical Supply Current 0.5 mA at 5V**
- **Typical Total Harmonic Distortion of 0.01% at 5V**
- **1.0 MHz Gain-Bandwidth**
- **Similar to Popular LMC6482/LMC6484**
- **Rail-to-Rail Input and Output**
- **Temperature Range –40°C to 125°C (LMC7101Q)**

APPLICATIONS

- **Mobile Communications**
- **Notebooks and PDAs**
- **Battery Powered Products**
- **Sensor Interface**
- **Automotive Applications (LMC7101Q)**

DESCRIPTION

The LMC7101 is a high performance CMOS operational amplifier available in the space saving 5-Pin SOT-23 Tiny package. This makes the LMC7101 ideal for space and weight critical designs. The performance is similar to a single amplifier of the LMC6482/LMC6484 type, with rail-to-rail input and output, high open loop gain, low distortion, and low supply currents.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Connection Diagram

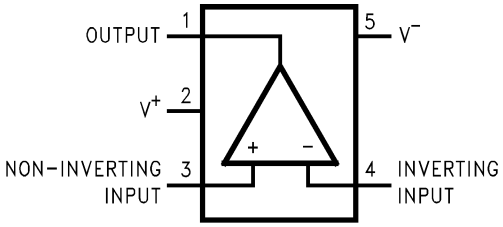


Figure 1. 5-Pin SOT-23
Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings(1)(2)

ESD Tolerance (3)	
Human Body Model	1000V
Machine Model	200V
Charged Device Model	1000V
Difference Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin	±5 mA
Current at Output Pin (4)	±35 mA
Current at Power Supply Pin	35 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (5)	150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) Human Body Model is 1.5 kΩ in series with 100 pF.
(4) Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.
(5) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Recommended Operating Conditions(1)

Supply Voltage	$2.7V \le V^+ \le 15.5V$
Temperature Range	
LMC7101AI, LMC7101BI	−40°C to 85°C
LMC7101Q	−40°C to 125°C
Thermal Resistance (θ_{JA})	
5-Pin SOT-23	325°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ(1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
V_{OS}	Input Offset Voltage Average Drift	V^+ = 2.7V	0.11	6	9	9	mV max
TCV_{OS}	Input Offset Voltage		1				µV/°C
I_B	Input Bias Current		1.0	**64**	**64**	**1000**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	**2000**	pA max
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 2.7V$ V^+ = 2.7V	70	55	50	50	dB min
V_{CM}	Input Common Mode Voltage Range	For CMRR ≥ 50 dB	0.0	0.0	0.0	0.0	V min
			3.0	2.7	2.7	2.7	V max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) When operated at temperature between −40°C and 85°C, the LMC7101Q will meet LMC7101BI specifications.

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2.7V Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
PSRR	Power Supply Rejection Ratio	V^+ = 1.35V to 1.65V V^- = −1.35V to −1.65V V_{CM} = 0	60	50	45	45	dB min
C_{IN}	Common-Mode Input Capacitance		3				pF
V_O	Output Swing	R_L = 2 kΩ	2.45	2.15	2.15	2.15	V min
			0.25	0.5	0.5	0.5	V max
		R_L = 10 kΩ	2.68	2.64	2.64	2.64	V min
			0.025	0.06	0.06	0.06	V max
I_S	Supply Current		0.5	0.81 **0.95**	0.81 **0.95**	0.81 **0.95**	mA max
SR	Slew Rate (4)		0.7				V/µs
GBW	Gain-Bandwidth Product		0.6				MHz

(4) V^+ = 15V. Connected as a voltage follower with a 10V step input. Number specified is the slower of the positive and negative slew rates. R_L = 100 kΩ connected to 7.5V. Amp excited with 1 kHz to produce V_O = 10 V_{PP}.

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
V_{OS}	Input Offset Voltage		0.11	4 **6**	7 **9**	7	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1				µV/°C
I_B	Input Current		1.0	**64**	**64**	**1000**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	**2000**	pA max
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V V^+ = 3V	74	64	60	60	db min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0.0	0.0	0.0	0.0	V min
			3.3	3.0	3.0	3.0	V max
PSRR	Power Supply Rejection Ratio	V^+ = 1.5V to 7.5V V^- = −1.5V to −7.5V V_O = V_{CM} = 0	80	68	60	60	dBmin
C_{IN}	Common-Mode Input Capacitance		3				pF
V_O	Output Swing	R_L = 2 kΩ	2.8	2.6	2.6	2.6	V min
			0.2	0.4	0.4	0.4	V max
		R_L = 600Ω	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current		0.5	0.81 **0.95**	0.81 **0.95**	0.81 **0.95**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) When operated at temperature between −40°C and 85°C, the LMC7101Q will meet LMC7101BI specifications.

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5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
V_{OS}	Input Offset Voltage	V^+ = 5V		0.11	3 **5**	7 **9**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Current			1	**64**	**64**	**1000**	pA max
I_{OS}	Input Offset Current			0.5	**32**	**32**	**2000**	pA max
R_{IN}	Input Resistance			>1				Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V LMC7101Q @ 125°C 0.2V ≤ V_{CM} ≤ 4.8V		82	65 **60**	60 **55**	60 **55**	db min
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 5V to 15V V^- = 0V, V_O = 1.5V		82	70 **65**	65 **62**	65 **62**	dB min
−PSRR	Negative Power Supply Rejection Ratio	V^- = −5V to −15V V^+ = 0V, V_O = −1.5V		82	70 **65**	65 **62**	65 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB		−0.3	−0.20 **0.00**	−0.20 **0.00**	−0.2 **0.2**	V min
				5.3	5.20 **5.00**	5.20 **5.00**	5.2 **4.8**	V max
C_{IN}	Common-Mode Input Capacitance			3				pF
V_O	Output Swing	R_L = 2 kΩ		4.9	4.7 **4.6**	4.7 **4.6**	4.7 **4.54**	V min
				0.1	0.18 **0.24**	0.18 **0.24**	0.18 **0.28**	V max
		R_L = 600Ω		4.7	4.5 **4.24**	4.5 **4.24**	4.5 **4.28**	V min
				0.3	0.5 **0.65**	0.5 **0.65**	0.5 **0.8**	V max
I_{SC}	Output Short Circuit Current	V_O = 0V 24	Sourcing	24	16 **11**	16 **11**	16 **9**	mA min
		V_O = 5V	Sinking	19	11 **7.5**	11 **7.5**	11 **5.8**	mA min
I_S	Supply Current			0.5	0.85 **1.0**	0.85 **1.0**	0.85 **1.0**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) When operated at temperature between −40°C and 85°C, the LMC7101Q will meet LMC7101BI specifications.

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	Units
THD	Total Harmonic Distortion	f = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.0 V_{PP}	0.01			%
SR	Slew Rate		1.0			V/µs
GBW	Gain Bandwidth Product		1.0			MHz

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.

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15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 15V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
V_{OS}	Input Offset Voltage			0.11				mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Current			1.0	**64**	**64**	**1000**	pA max
I_{OS}	Input Offset Current			0.5	**32**	**32**	**2000**	pA max
R_{IN}	Input Resistance			>1				Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 15V LMC7101Q @°125C 0.2V ≤ V_{CM} ≤ 14.8V		82	70 **65**	65 **60**	65 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 5V to 15V V^- = 0V, V_O = 1.5V		82	70 **65**	65 **62**	65 **62**	dB min
−PSRR	Negative Power Supply Rejection Ratio	V^- = −5V to −15V V^+ = 0V, V_O = −1.5V		82	70 **65**	65 **62**	65 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V For CMRR ≥ 50 dB		−0.3	−0.20 **0.00**	−0.20 **0.00**	−0.2 **0.2**	V min
				15.3	15.20 **15.00**	15.20 **15.00**	15.2 **14.8**	V max
A_V	Large Signal Voltage Gain (4)	R_L = 2 kΩ	Sourcing	340	80 **40**	80 **40**	80 **30**	V/mV
			Sinking	24	15 **10**	15 **10**	15 **4**	
		R_L = 600Ω	Sourcing	300	34	34	34	V/mV
			Sinking	15	6	6	6	
C_{IN}	Input Capacitance			3				pF
V_O	Output Swing	V^+ = 15V R_L = 2 kΩ		14.7	14.4 **14.2**	14.4 **14.2**	14.4 **14.2**	V min
				0.16	0.32 **0.45**	0.32 **0.45**	0.32 **0.45**	V max
		V^+ = 15V R_L = 600Ω		14.1	13.4 **13.0**	13.4 **13.0**	13.4 **12.85**	V min
				0.5	1.0 **1.3**	1.0 **1.3**	1.0 **1.5**	V max
I_{SC}	Output Short Circuit Current (5)	V_O = 0V	Sourcing	50	30 **20**	30 **20**	30 **20**	mA min
		V_O = 12V	Sinking	50	30 **20**	30 **20**	30 **20**	
I_S	Supply Current			0.8	1.50 **1.71**	1.50 **1.71**	1.50 **1.75**	mA max

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) When operated at temperature between −40°C and 85°C, the LMC7101Q will meet LMC7101BI specifications.
(4) V^+ = 15V, V_{CM} = 1.5V and R_L connect to 7.5V. For sourcing tests, 7.5V ≤ V_O ≤ 12.5V. For sinking tests, 2.5V ≤ V_O ≤ 7.5V.
(5) Do not short circuit output to V^+ when V^+ is greater than 12V or reliability will be adversely affected.

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15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 15V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (1)	LMC7101AI Limit (2)	LMC7101BI Limit (2)	LMC7101Q Limit (2) (3)	Units
SR	Slew Rate (4)	V^+ = 15V	1.1	0.5 **0.4**	0.5 **0.4**	0.5 **0.4**	V/µs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.1				MHz
φ_m	Phase Margin		45				deg
G_m	Gain Margin		10				dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 1V	37				$\frac{nV}{\sqrt{Hz}}$
I_n	Input-Referred Current Noise	f = 1 kHz	1.5				$\frac{fA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP}	0.01				%

(1) Typical Values represent the most likely parametric norm.
(2) All limits are guaranteed by testing or statistical analysis.
(3) When operated at temperature between −40°C and 85°C, the LMC7101Q will meet LMC7101BI specifications.
(4) V^+ = 15V. Connected as a voltage follower with a 10V step input. Number specified is the slower of the positive and negative slew rates. R_L = 100 kΩ connected to 7.5V. Amp excited with 1 kHz to produce V_O = 10 V_{PP}.

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2.7V Typical Performance Characteristics

V^+ = 2.7V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Open Loop Frequency Response

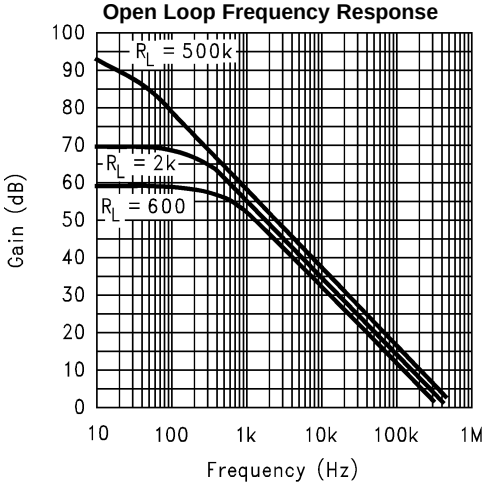


Figure 2.

Input Voltage vs. Output Voltage

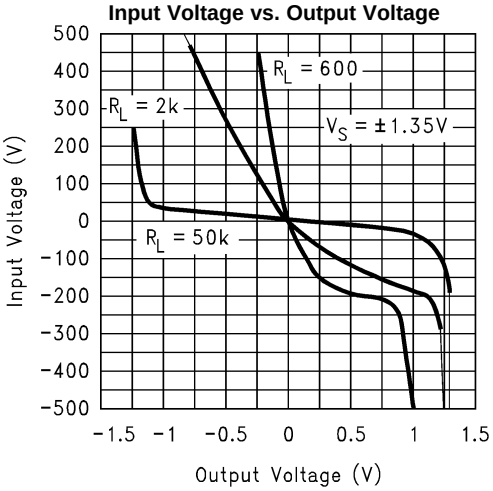


Figure 3.

Gain and Phase vs. Capacitance Load

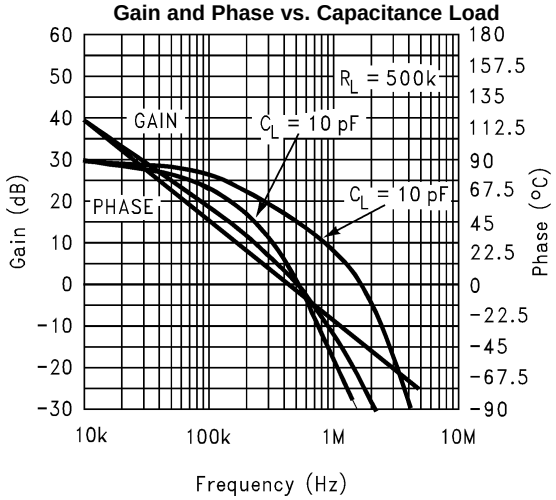


Figure 4.

Gain and Phase vs. Capacitance Load

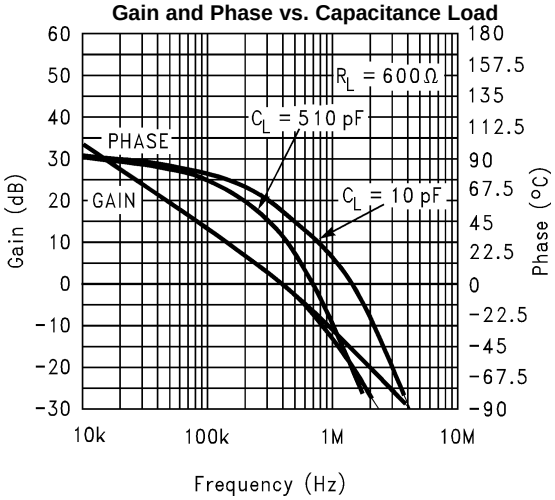


Figure 5.

dV_{OS} vs. Supply Voltage

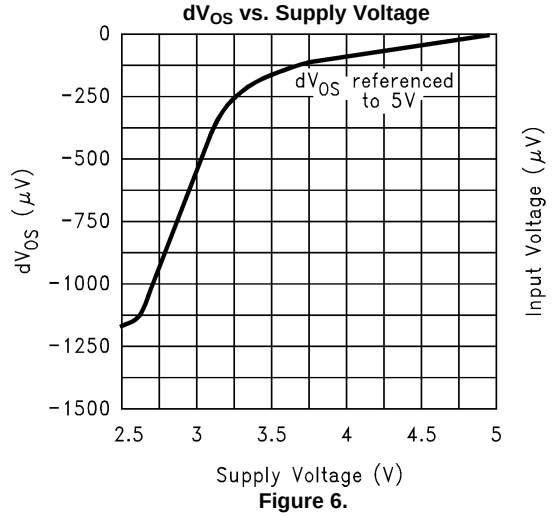


Figure 6.

dV_{OS} vs. Common Mode Voltage

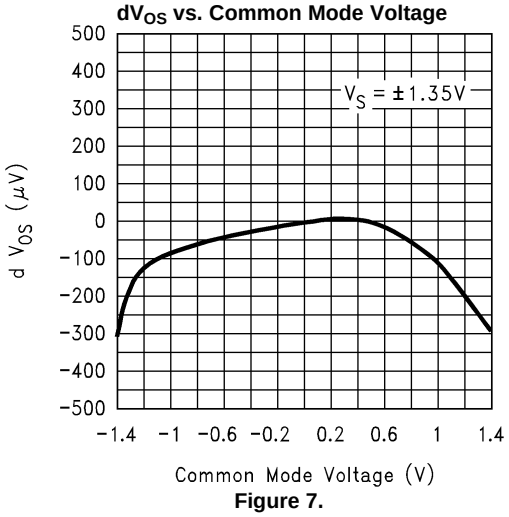


Figure 7.

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2.7V Typical Performance Characteristics (continued)

V^+ = 2.7V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Sinking Current vs. Output Voltage

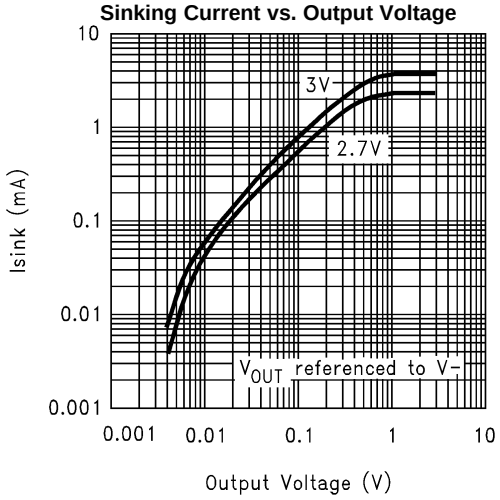


Figure 8.

Sourcing Current vs. Output Voltage

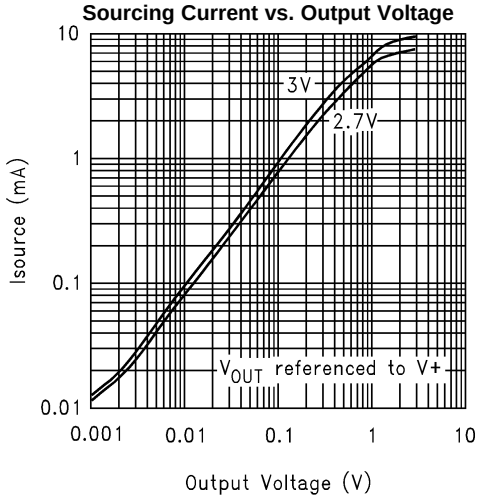


Figure 9.

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3V Typical Performance Characteristics

V^+ = 3V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Open Loop Frequency Response

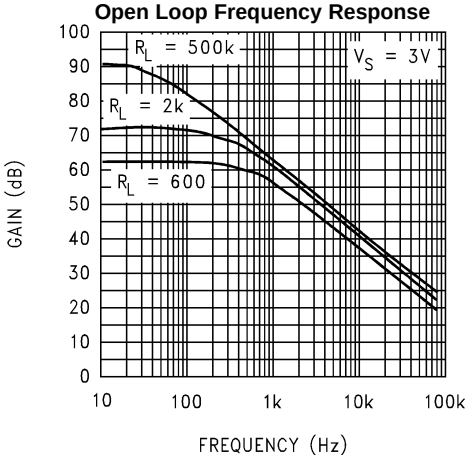


Figure 10.

Input Voltage vs. Output Voltage

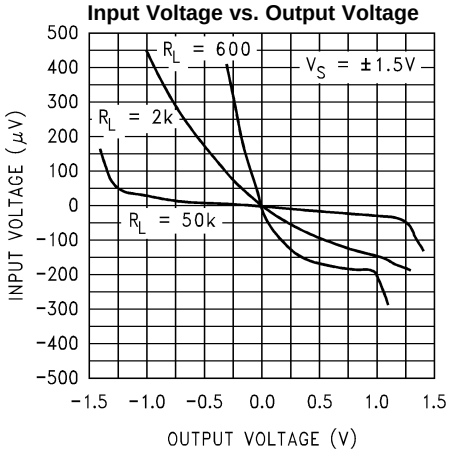


Figure 11.

Input Voltage Noise vs. Input Voltage

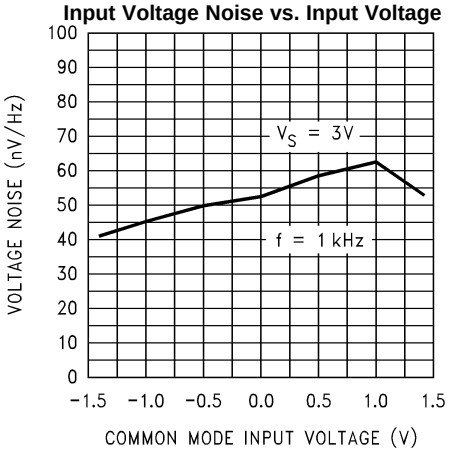


Figure 12.

Sourcing Current vs. Output Voltage

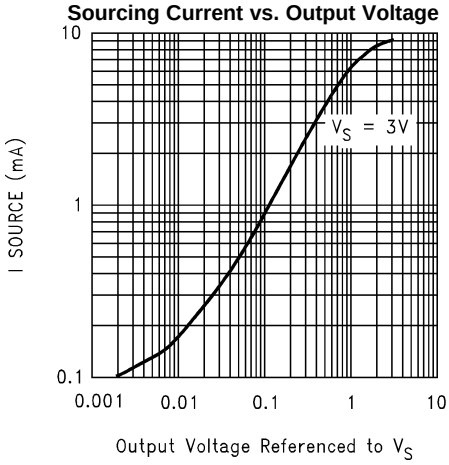


Figure 13.

Sinking Current vs. Output Voltage

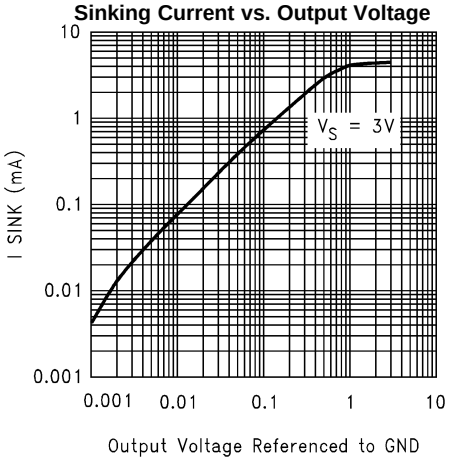


Figure 14.

CMRR vs. Input Voltage

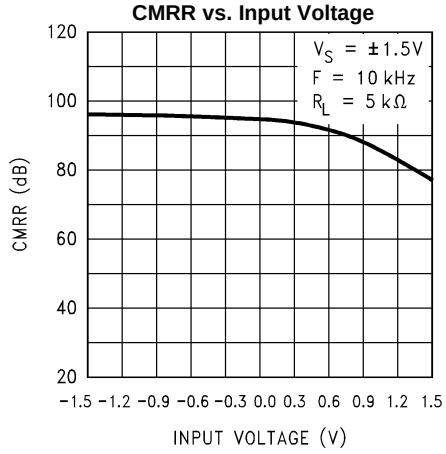


Figure 15.

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5V Typical Performance Characteristics

V^+ = 5V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Open Loop Frequency Response

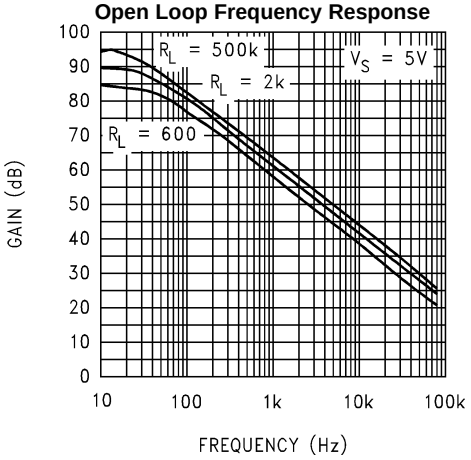


Figure 16.

Input Voltage vs. Output Voltage

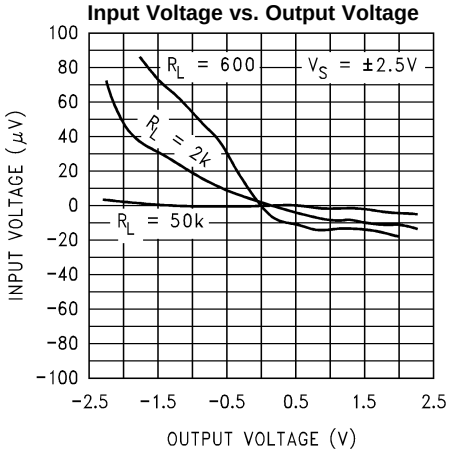


Figure 17.

Input Voltage Noise vs. Input Voltage

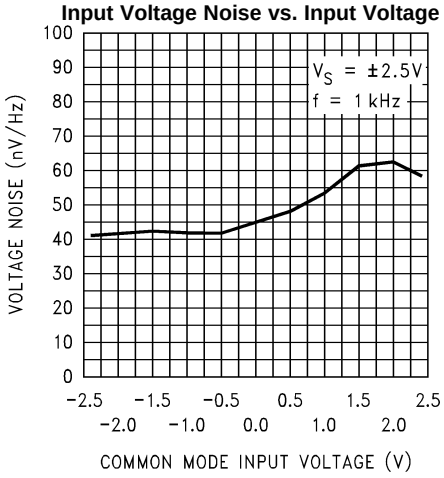


Figure 18.

Sourcing Current vs, Output Voltage

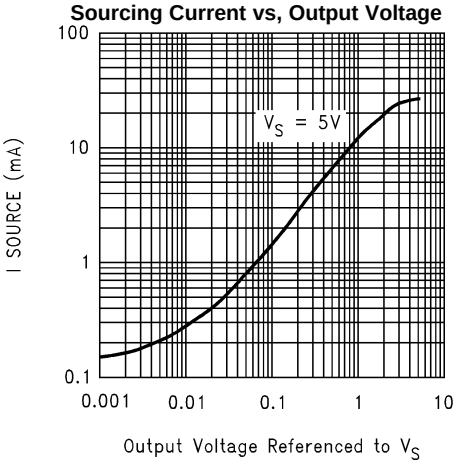


Figure 19.

Sinking Current vs. Output Voltage

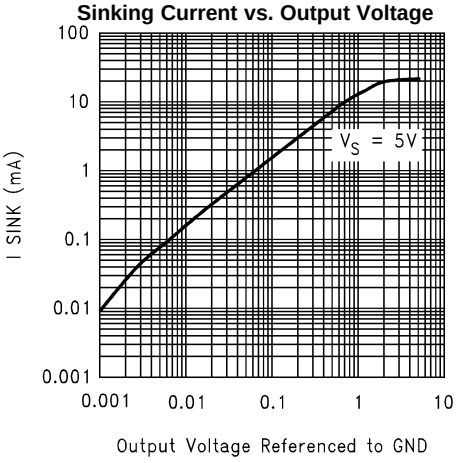


Figure 20.

CMRR vs. Input Voltage

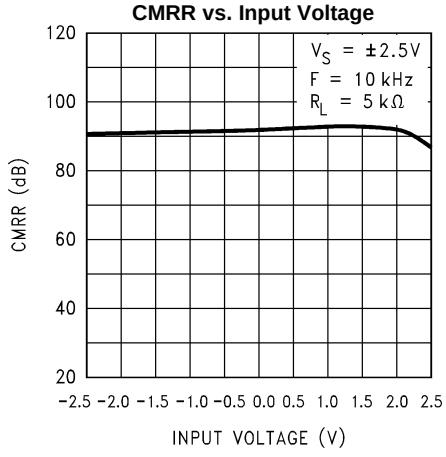


Figure 21.

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15V Typical Performance Characteristics

V^+ = +15V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Open Loop Frequency Response

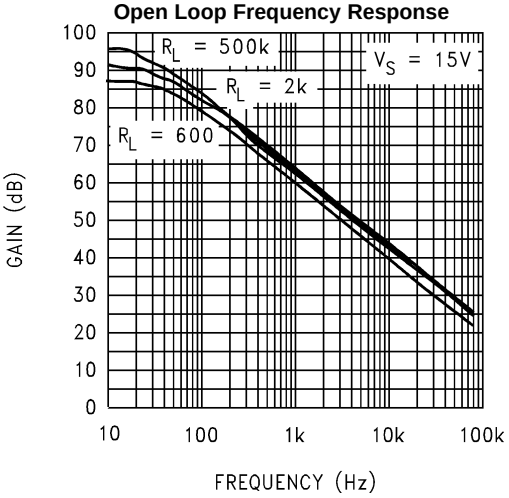


Figure 22.

Input Voltage vs. Output Voltage

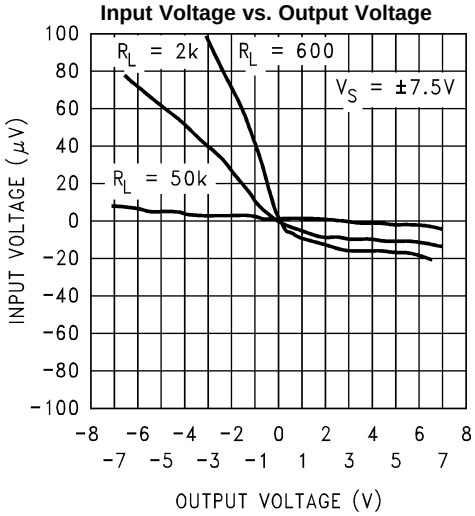


Figure 23.

Input Voltage Noise vs. Input Voltage

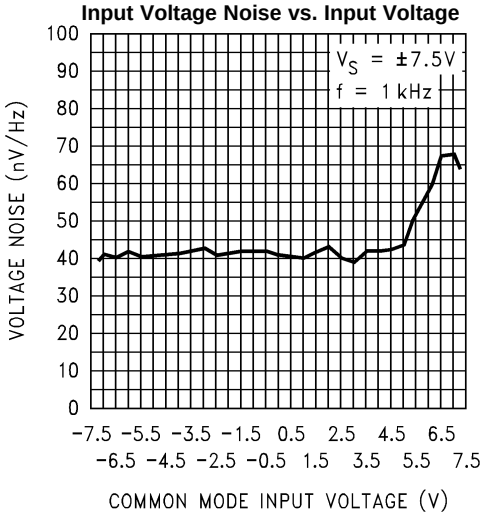


Figure 24.

Sourcing Current vs. Output Voltage

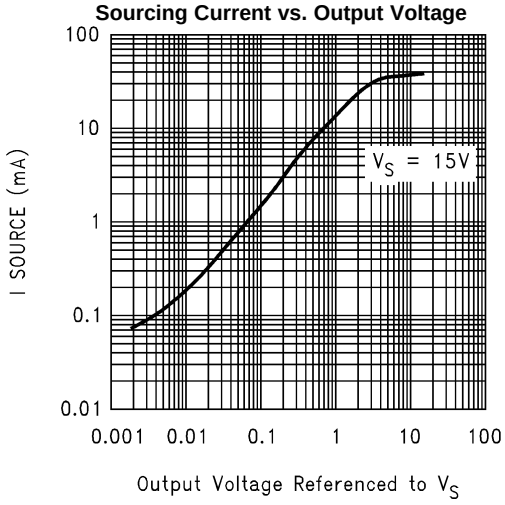


Figure 25.

15V Typical Performance Characteristics (continued)

V^+ = +15V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Sinking Current vs. Output Voltage

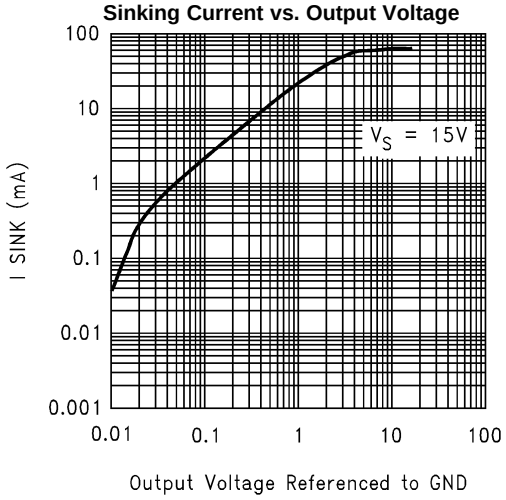


Figure 26.

CMRR vs. Input Voltage

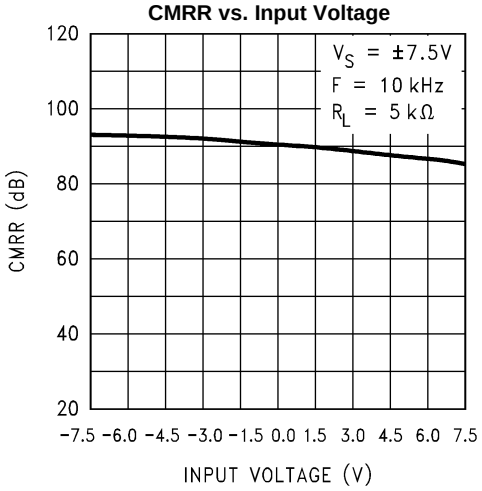


Figure 27.

Supply Current vs. Supply Voltage

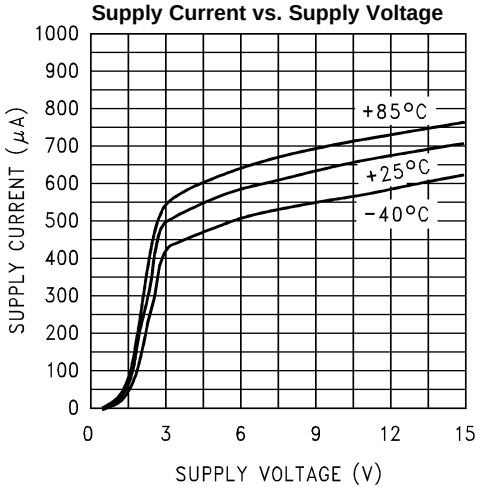


Figure 28.

Input Current vs. Temperature

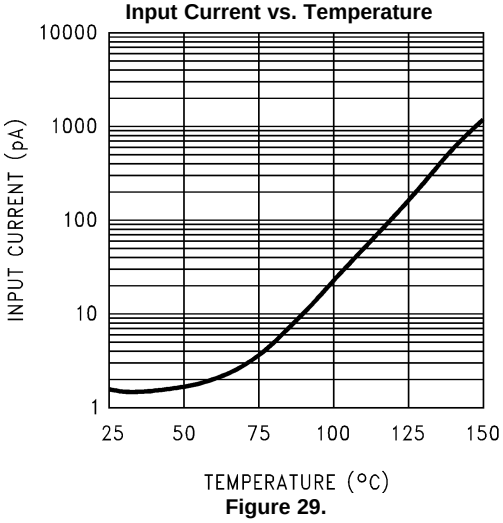


Figure 29.

Output Voltage Swing vs. Supply Voltage

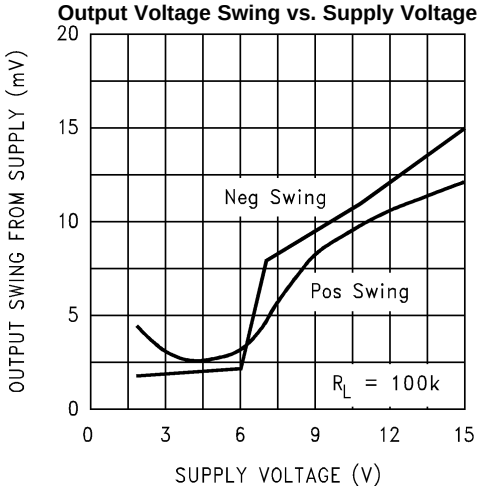


Figure 30.

Input Voltage Noise vs. Frequency

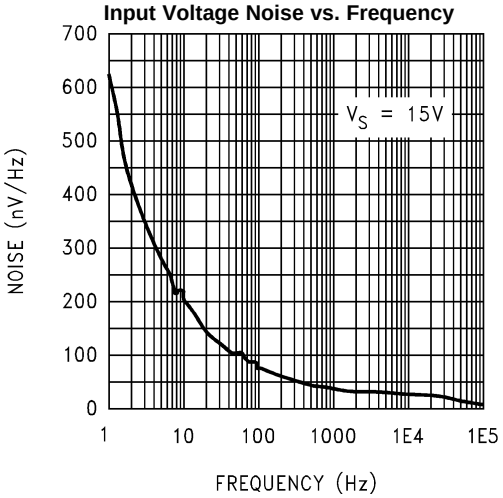


Figure 31.

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15V Typical Performance Characteristics (continued)

V^+ = +15V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Positive PSRR vs. Frequency

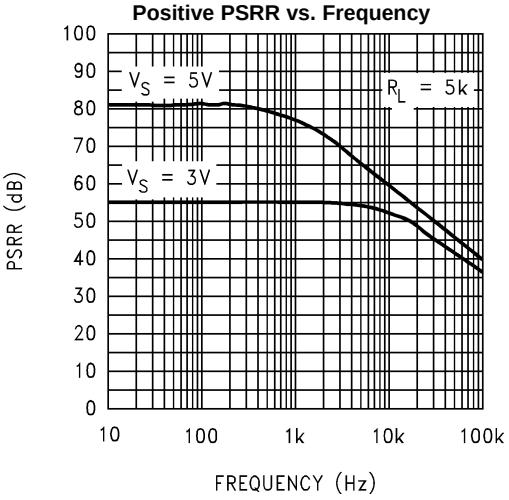


Figure 32.

Negative PSRR vs. Frequency

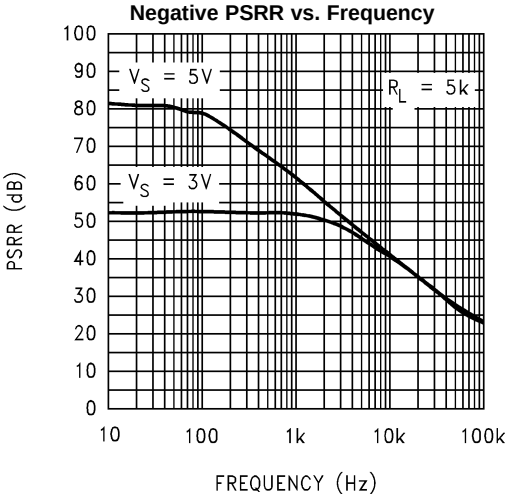


Figure 33.

CMRR vs. Frequency

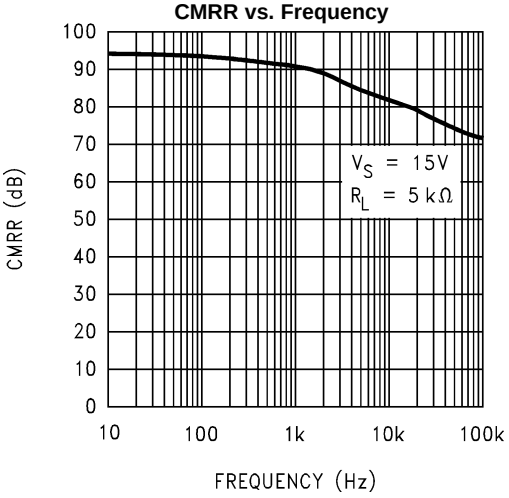


Figure 34.

Open Loop Frequency Response @ −40°C

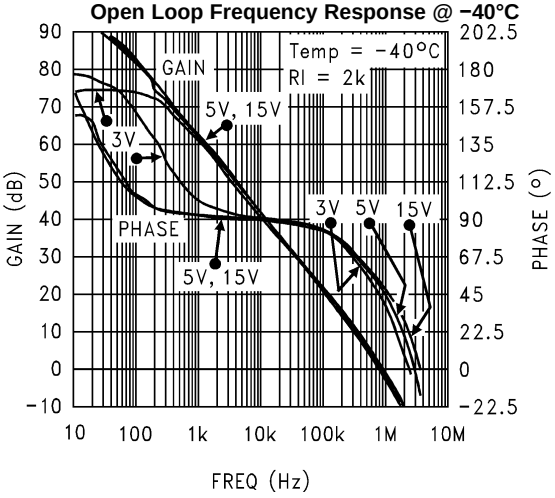


Figure 35.

Open Loop Frequency Response @ 25°C

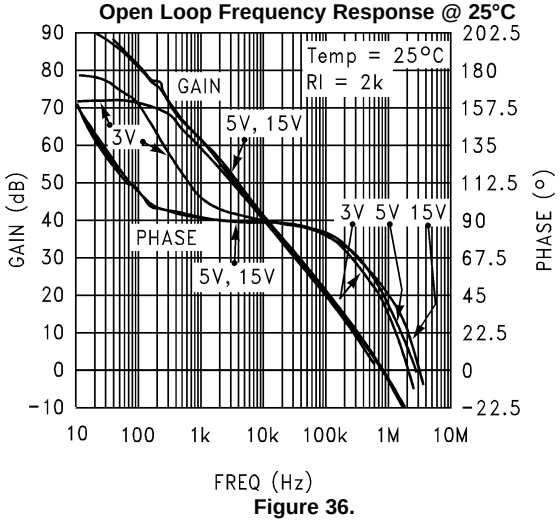


Figure 36.

Open Loop Frequency Response @ 85°C

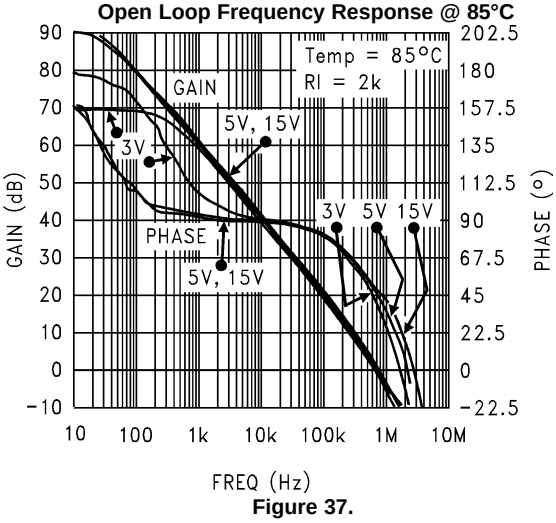


Figure 37.

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15V Typical Performance Characteristics (continued)

V^+ = +15V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Maximum Output Swing vs. Frequency

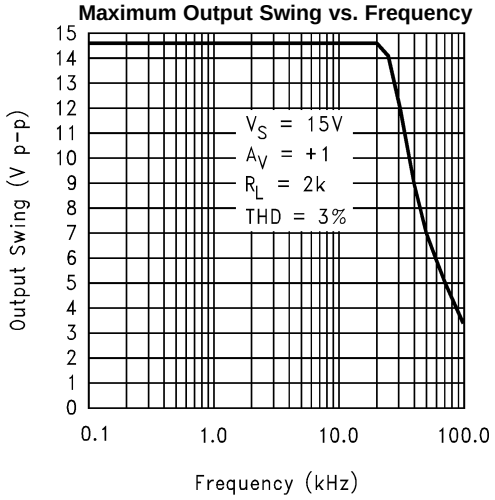


Figure 38.

Gain and Phase vs. Capacitive Load

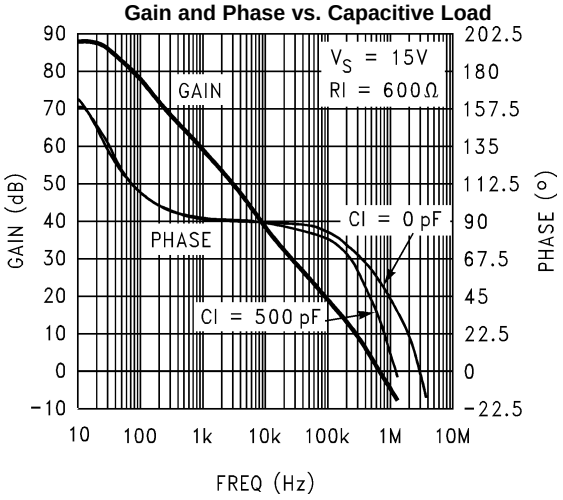


Figure 39.

Gain and Phase vs. Capacitive Load

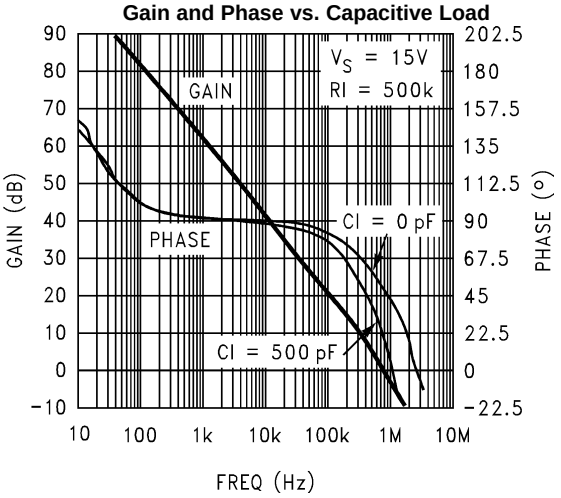


Figure 40.

Output Impedance vs. Frequency

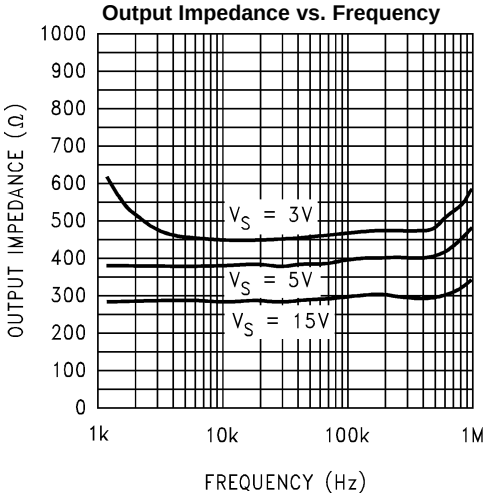


Figure 41.

Slew Rate vs. Temperature

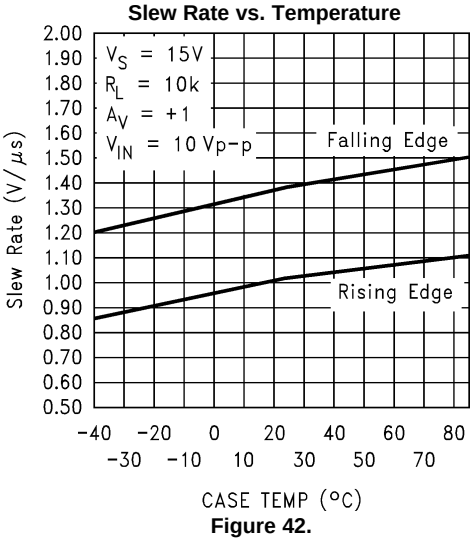


Figure 42.

Slew Rate vs. Supply Voltage

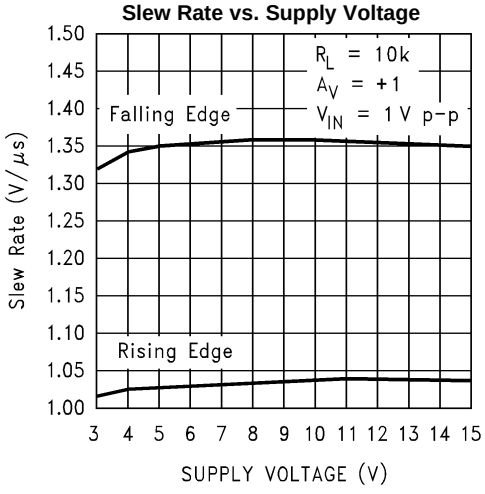


Figure 43.

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15V Typical Performance Characteristics (continued)

V^+ = +15V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Inverting Small Signal Pulse Response

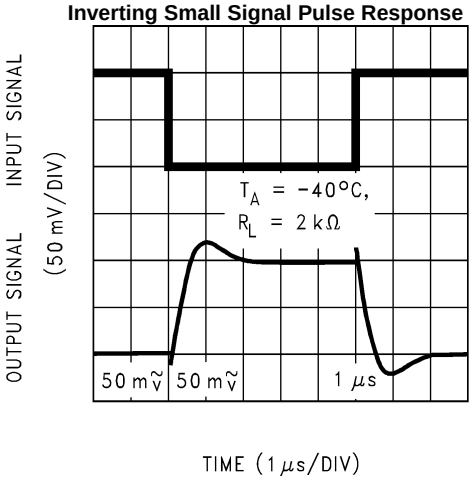


Figure 44.

Inverting Small Signal Pulse Response

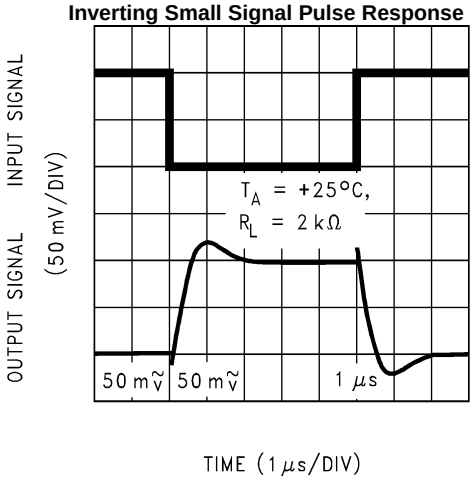


Figure 45.

Inverting Small Signal Pulse Response

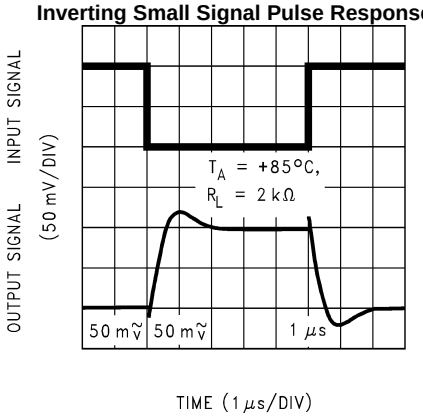


Figure 46.

Inverting Large Signal Pulse Response

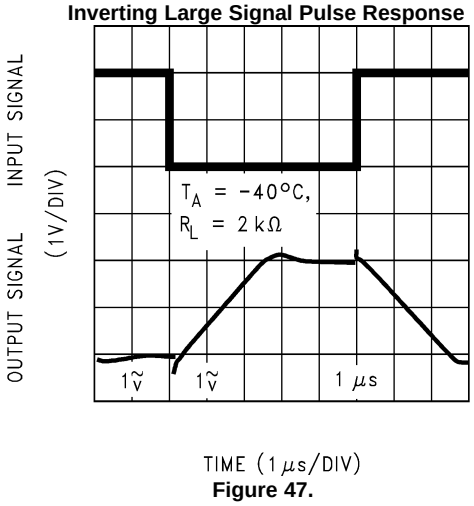


Figure 47.

Inverting Large Signal Pulse Response

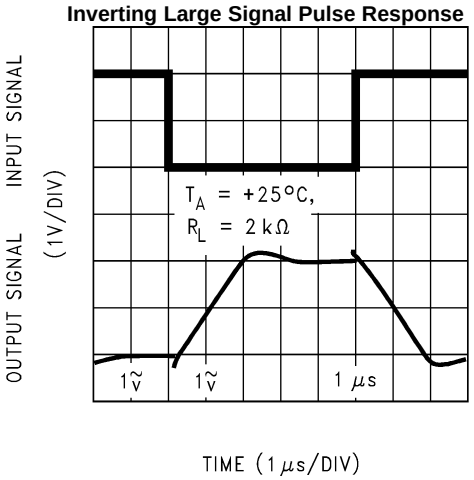


Figure 48.

Inverting Large Signal Pulse Response

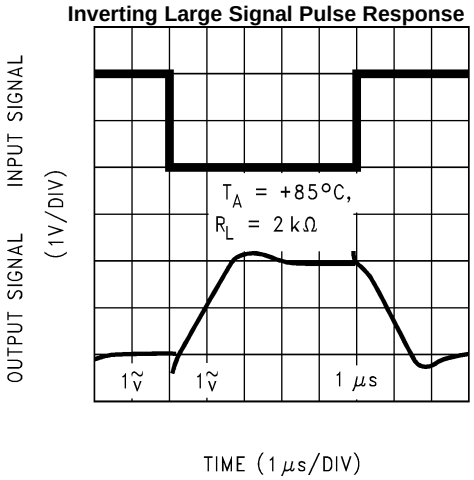


Figure 49.

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15V Typical Performance Characteristics (continued)

V^+ = +15V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Non-Inverting Small Signal Pulse Response

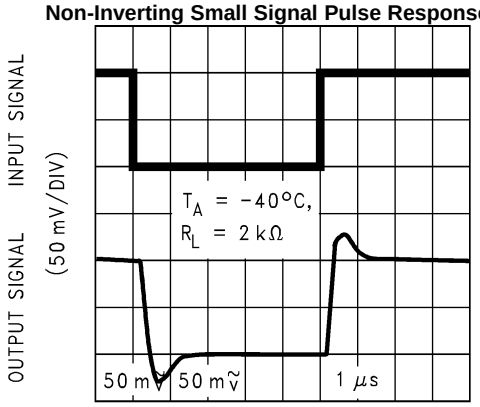


Figure 50.

Non-Inverting Small Signal Pulse Response

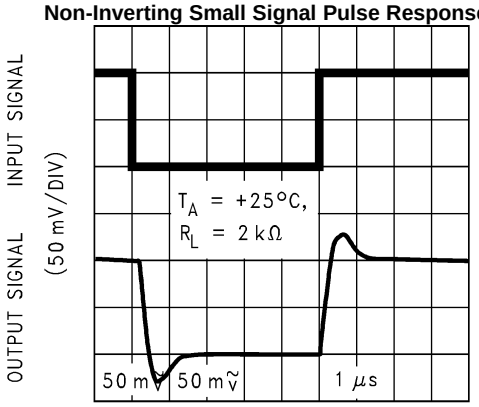


Figure 51.

Non-Inverting Small Signal Pulse Response

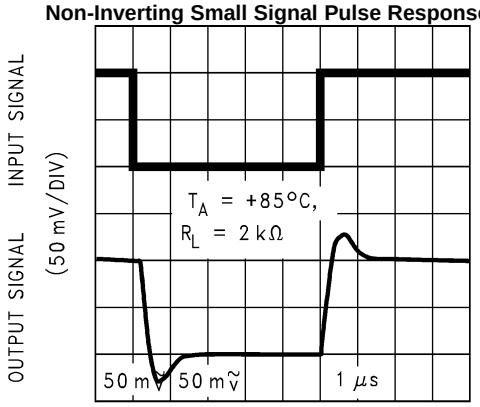


Figure 52.

Non-Inverting Large Signal Pulse Response

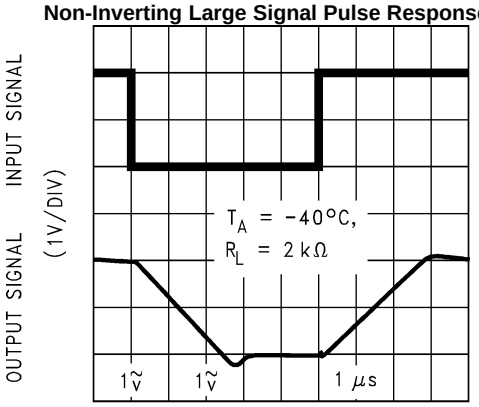


Figure 53.

Non-Inverting Large Signal Pulse Response

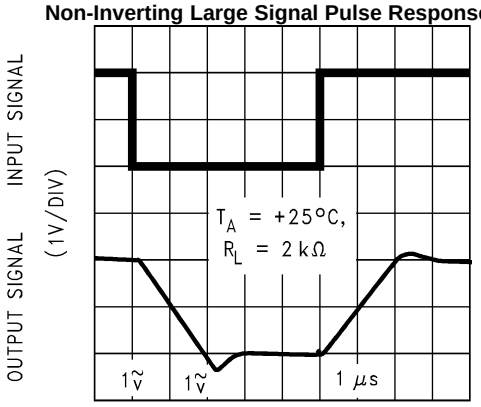


Figure 54.

Non-Inverting Large Signal Pulse Response

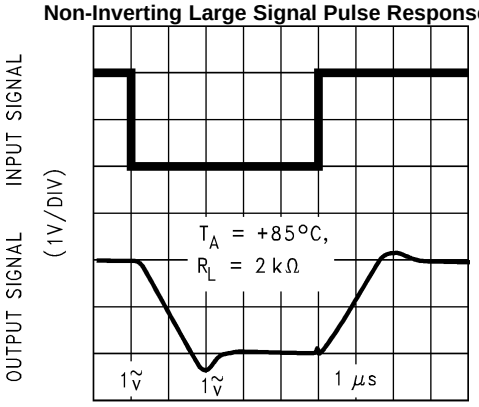


Figure 55.

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15V Typical Performance Characteristics (continued)

V^+ = +15V, V^- = 0V, T_A = 25°C, unless otherwise specified.

Stability vs. Capacitive Load

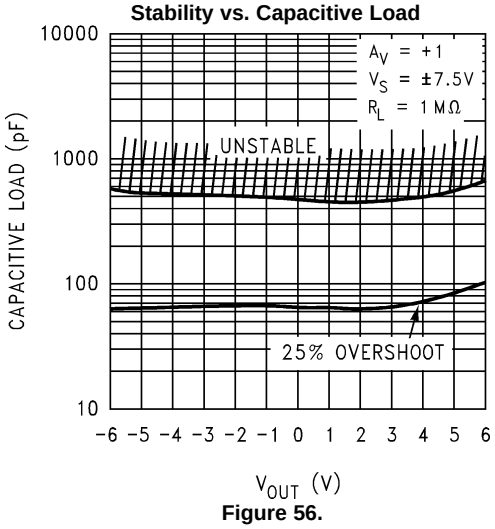


Figure 56.

Stability vs. Capacitive Load

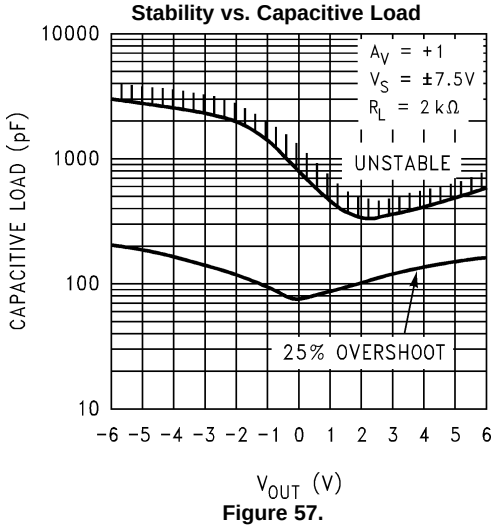


Figure 57.

Stability vs. Capacitive Load

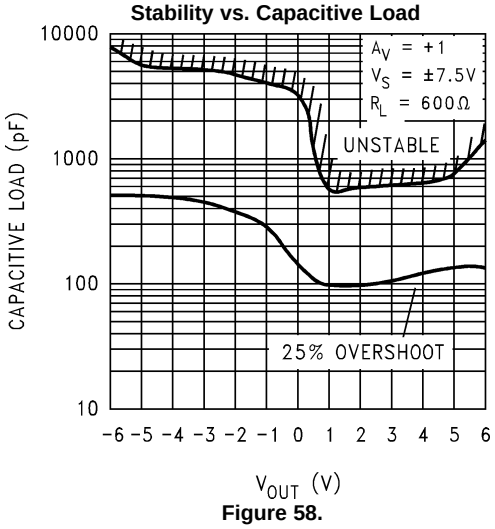


Figure 58.

Stability vs. Capacitive Load

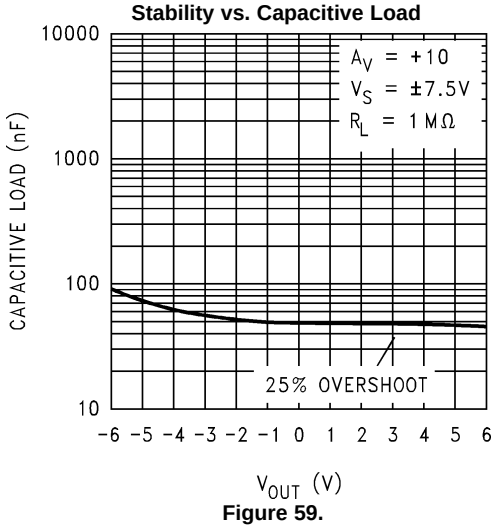


Figure 59.

Stability vs. Capacitive Load

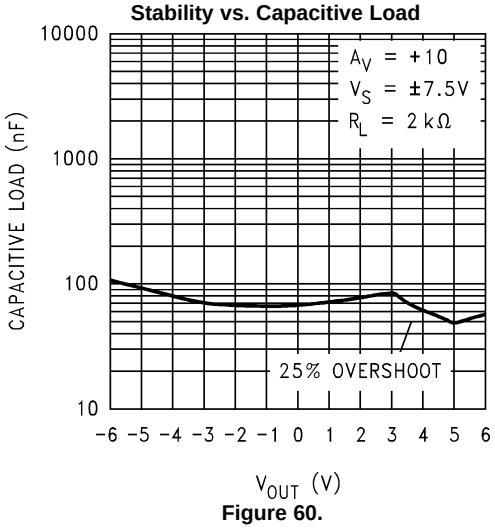


Figure 60.

Stability vs. Capacitive Load

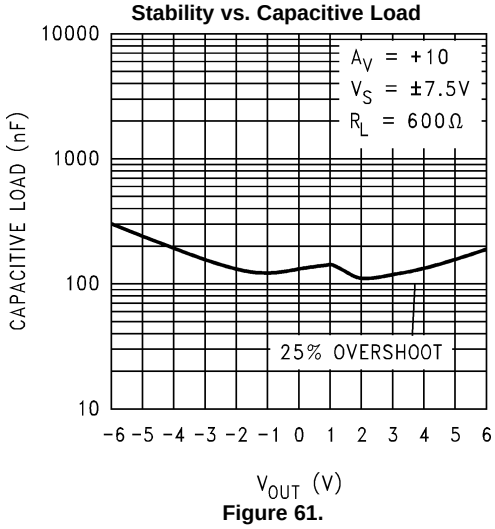


Figure 61.

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APPLICATION INFORMATION

BENEFITS OF THE LMC7101 TINY AMP

Size

The small footprint of the SOT-23-5 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height

The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

Simplified Board Layout

The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

Low THD

The high open loop gain of the LMC7101 amp allows it to achieve very low audio distortion—typically 0.01% at 10 kHz with a 10 kΩ load at 5V supplies. This makes the Tiny an excellent for audio, modems, and low frequency signal processing.

Low Supply Current

The typical 0.5 mA supply current of the LMC7101 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range

The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the voltage may vary over the life of the batteries.

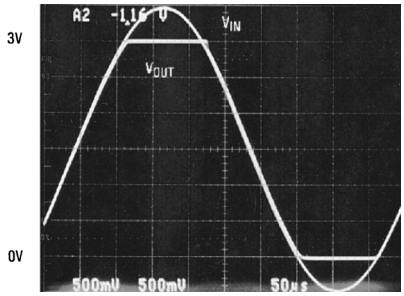
INPUT COMMON MODE

Voltage Range

The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 62 shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

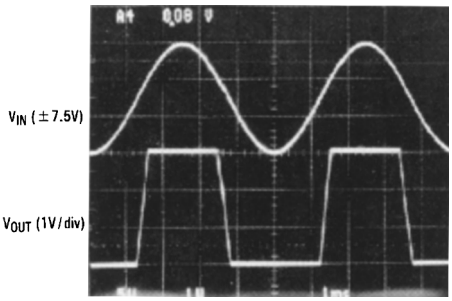
The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in Figure 63, can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

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An input voltage signal exceeds the LMC7101 power supply voltages with no output phase inversion.

Figure 62. Input Voltage



A ±7.5V input signal greatly exceeds the 3V supply in Figure 64 causing no phase inversion due to R_I.

Figure 63. Input Signal

Applications that exceed this rating must externally limit the maximum input current to ±5 mA with an input resistor as shown in Figure 64.

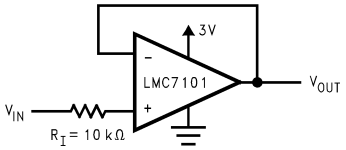


Figure 64. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

RAIL-TO-RAIL OUTPUT

The approximate output resistance of the LMC7101 is 180Ω sourcing and 130Ω sinking at V_S = 3V and 110Ω sourcing and 80Ω sinking at V_S = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

CAPACITIVE LOAD TOLERANCE

The LMC7101 can typically directly drive a 100 pF load with V_S = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op amps. The combination of the op amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 65. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

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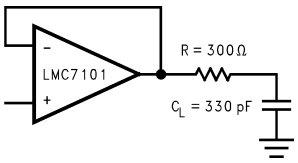


Figure 65. Resistive Isolation of a 330 pF Capacitive Load

COMPENSATING FOR INPUT CAPACITANCE WHEN USING LARGE VALUE FEEDBACK RESISTORS

When using very large value feedback resistors, (usually > 500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photo diodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 66), C_f is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad (1)$$

or

$$R_1 C_{IN} \leq R_2 C_f \quad (2)$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

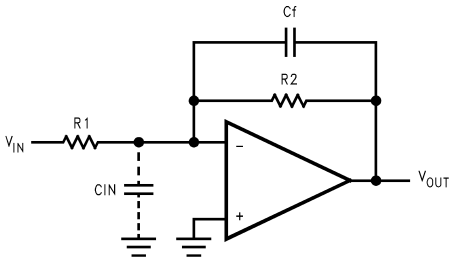


Figure 66. Cancelling the Effect of Input Capacitance

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REVISION HISTORY

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	20

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMC7101AIM5	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A00A	Samples
LMC7101AIM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A00A	Samples
LMC7101AIM5X	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A00A	Samples
LMC7101AIM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A00A	Samples
LMC7101BIM5	ACTIVE	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	A00B	Samples
LMC7101BIM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A00B	Samples
LMC7101BIM5X	ACTIVE	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	A00B	Samples
LMC7101BIM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	A00B	Samples
LMC7101QM5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT6A	Samples
LMC7101QM5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	AT6A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

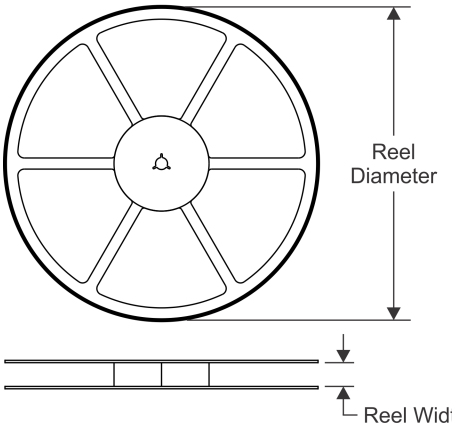
(4) Only one of markings shown within the brackets will appear on the physical device.

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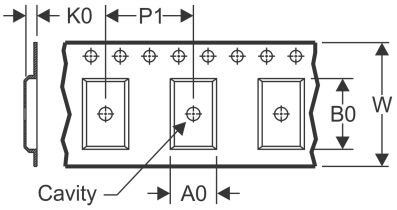
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

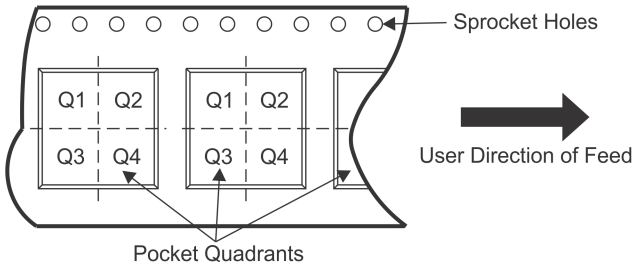


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

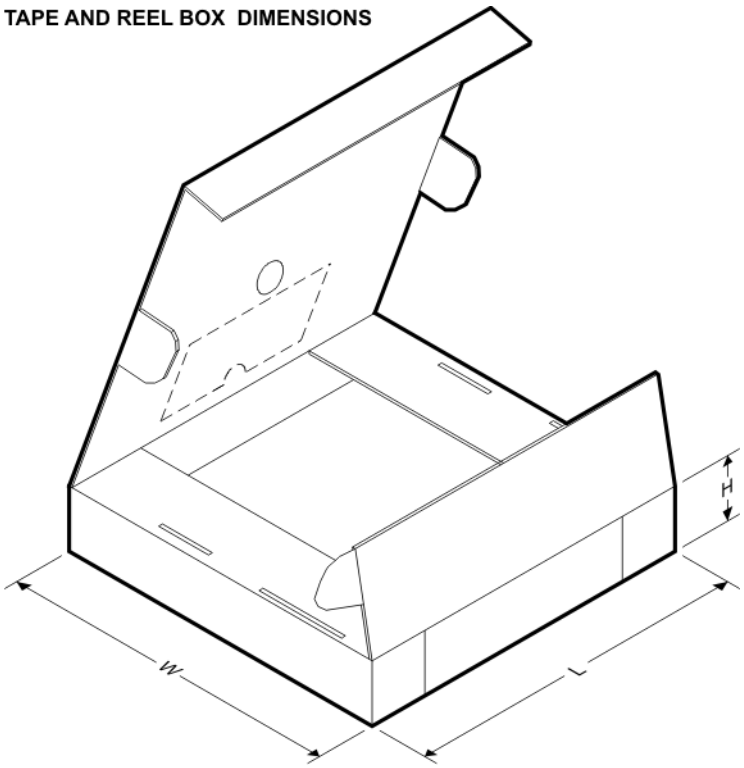
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC7101AIM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101QM5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMC7101QM5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

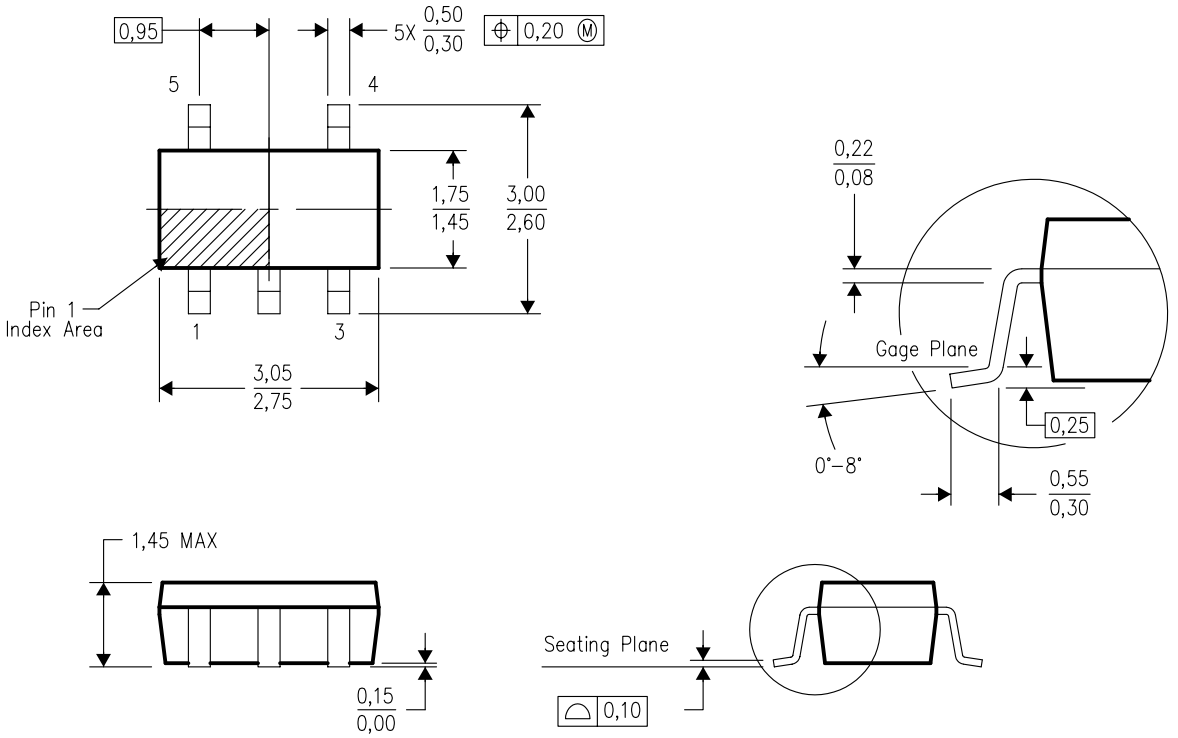
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC7101AIM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101AIM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101AIM5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101AIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101BIM5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101BIM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101BIM5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101BIM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMC7101QM5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMC7101QM5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

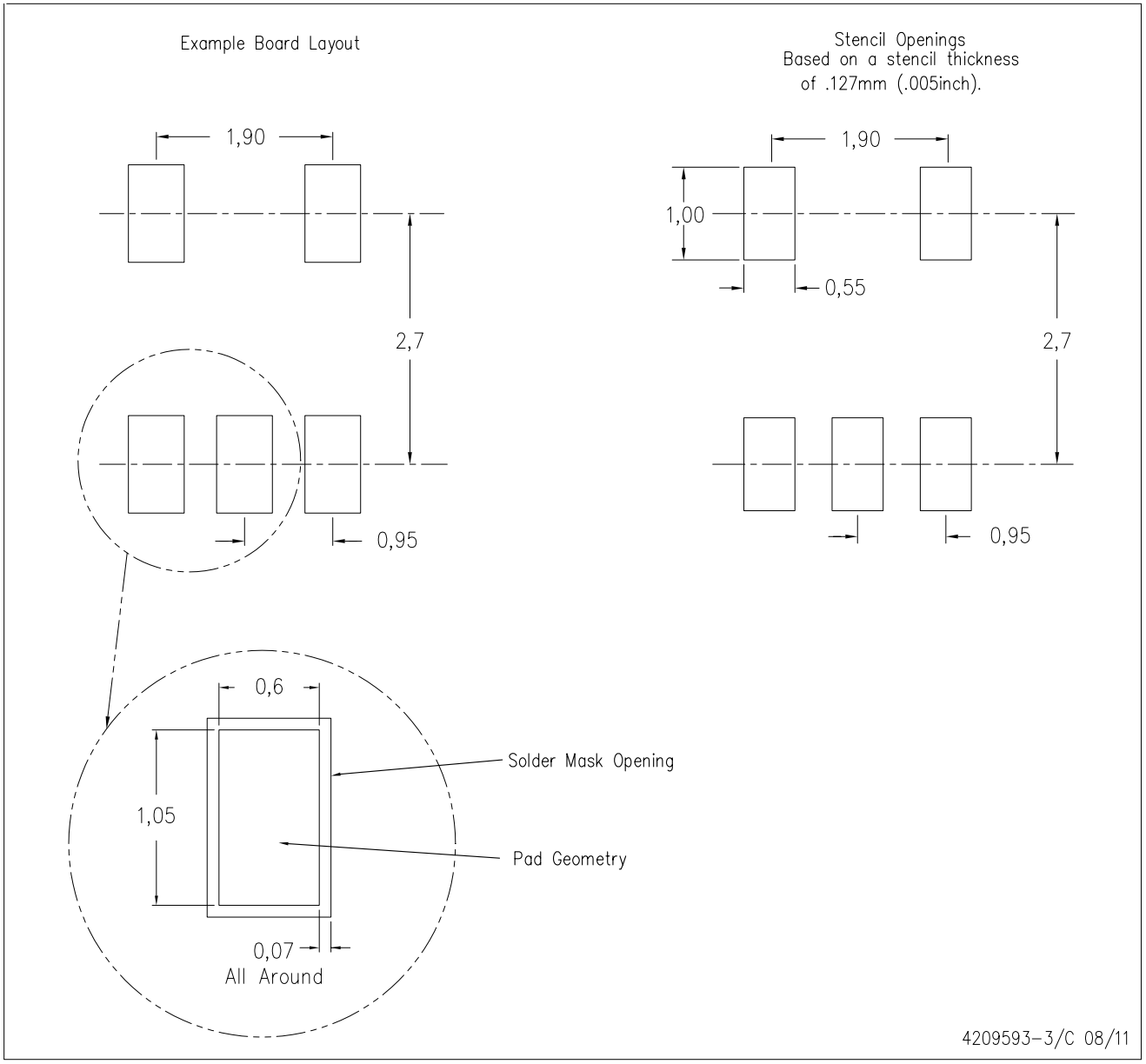
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
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