74AVC16835A

18-bit registered driver with Dynamic Controlled Outputs; 3-state

Rev. 6 — 24 September 2018 Product data sheet

1. General description

The 74AVC16835A is an 18-bit universal bus driver. Data flow is controlled by output enable ($\overline{OE}$), latch enable (LE) and clock inputs (CP).

This product is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient. See Fig. 5 for typical curves.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-1A (2.7 V to 3.6 V)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple V_{CC} and GND pins to minimize noise and ground bounce
- Power off disables 74AVC16835A outputs, permitting Live Insertion
- Integrated input diodes to minimize input overshoot and undershoot

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC16835ADGG	-40 °C to + 85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

nexperia

4. Functional diagram

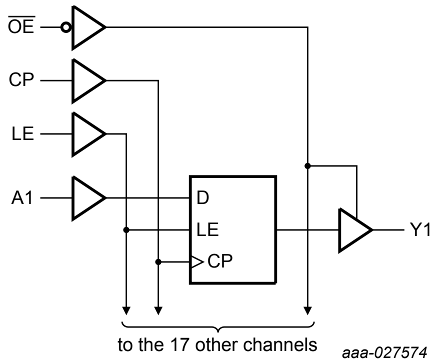


Fig. 1. Logic diagram

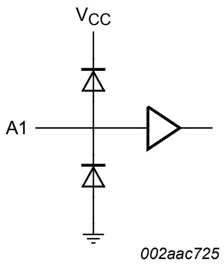


Fig. 3. Typical input (data or control)

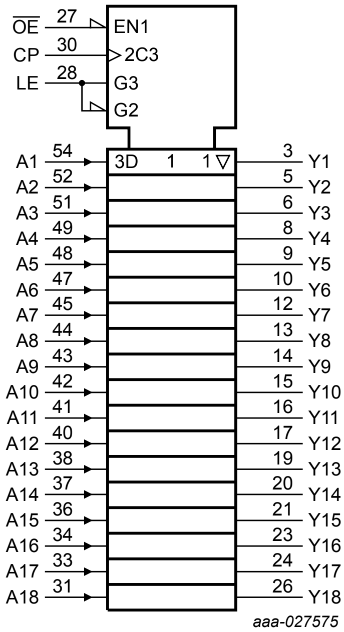


Fig. 2. Logic symbol (IEEE/IEC)

5. Pinning information

5.1. Pinning

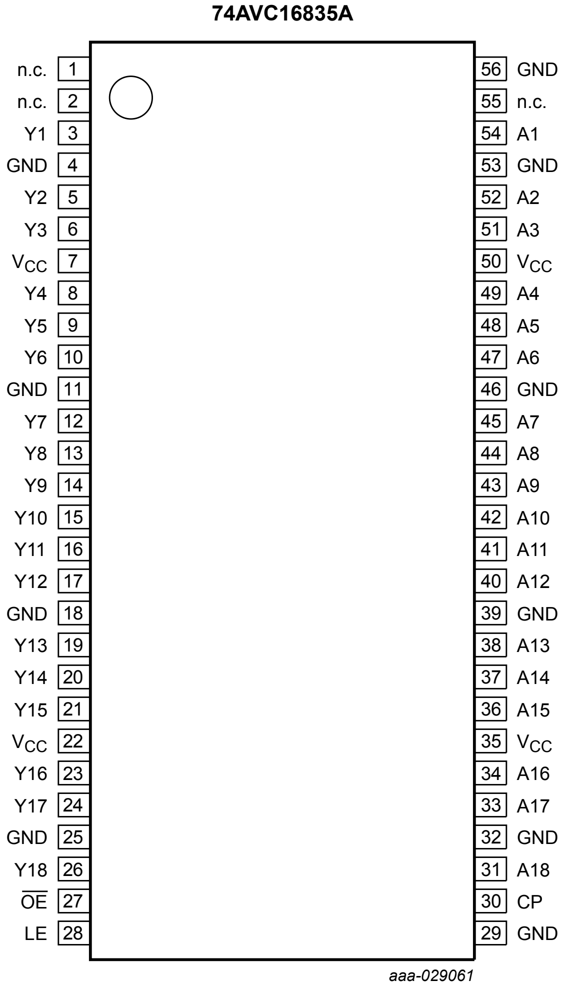


Fig. 4. Pin configuration SOT364-1 (TSSOP56)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18	54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	data inputs
Y1, Y2, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18	3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	data outputs
n.c.	1, 2, 55	not connected
LE	28	latch enable input
$\overline{OE}$	27	output enable input (active LOW)
CP	30	clock input
GND	4, 11, 18, 25, 29, 32, 39, 46, 53, 56	ground (0 V)
V_{CC}	7, 22, 35, 50	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = Don't care; Z = high-impedance OFF-state; ↑ = LOW to HIGH level transition.

Inputs				Outputs
$\overline{OE}$	LE	CP	An	Yn
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y_0 [1]
L	L	L	X	Y_0 [2]

[1] Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
[2] Output level before the indicated steady-state input conditions were established.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
V_I	input voltage		[1]	-0.5	+4.6	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or V_O < 0 V		-	±50	mA
V_O	output voltage	output HIGH or LOW	[1]	-0.5	V_{CC} + 0.5	V
		output 3-state	[1]	-0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = −40 °C to +85 °C	[2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	for low-voltage applications	1.2	-	3.6	V
		according to JEDEC Low Voltage Standards	1.65	-	1.95	V
			2.3	-	2.7	V
			3.0	-	3.6	V
V_I	input voltage		0	-	3.6	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	3.6	V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.65 V to 2.3 V	0	-	30	ns/V
		V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

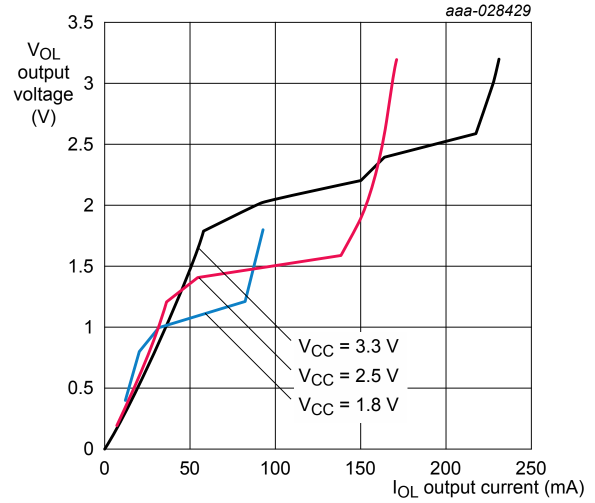
At recommended operating conditions; T_{amb} = −40 °C to +85 °C; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	0.9	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 1.65 V to 1.95 V	-	0.9	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} - 0.20	V_{CC}	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	V_{CC} - 0.45	V_{CC} - 0.10	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	V_{CC} - 0.55	V_{CC} - 0.28	-	V
		I_O = -12 mA; V_{CC} = 3.0 V	V_{CC} - 0.70	V_{CC} - 0.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	GND	0.20	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	0.10	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	0.26	0.55	V
		I_O = 12 mA; V_{CC} = 3.0 V	-	0.36	0.70	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 1.65 V to 3.6 V	-	0.1	2.5	μA
I_{OFF}	power-off leakage current	V_I or V_O = 3.6 V; V_{CC} = 0 V	-	0.1	±10	μA
I_{IHZ}/I_{ILZ}	power-off leakage current	V_{CC} = 1.65 V to 3.6 V; V_I = V_{CC} or GND	-	0.1	12.5	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND				
		V_{CC} = 1.65 V to 2.7 V	-	0.1	5	μA
		V_{CC} = 3.0 V to 3.6 V	-	0.1	10	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A				
		V_{CC} = 1.65 V to 2.7 V	-	0.1	20	μA
		V_{CC} = 3.0 V to 3.6 V	-	0.2	40	μA
C_I	input capacitance		-	3.8	-	pF

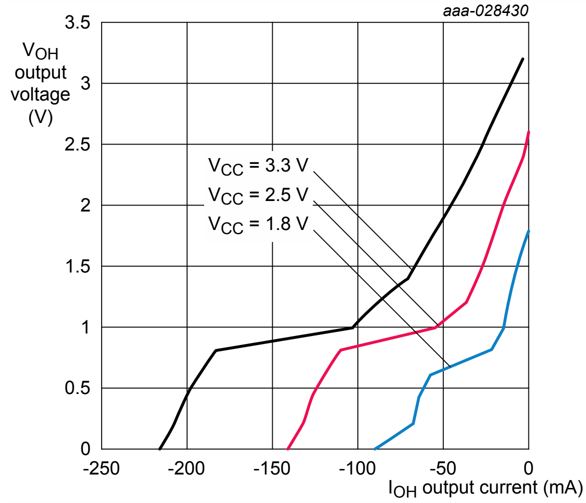
[1] All typical values are measured at T_{amb} = 25 °C.

9.1. Dynamic Controlled Output graphs

A Dynamic Controlled Output (DCO) circuit is designed in. During the transition, it initially lowers the output impedance to effectively drive the load and, subsequently, raises the impedance to reduce noise. Fig. 5 show V_{OL} vs. I_{OL} and V_{OH} vs. I_{OH} curves to illustrate the output impedance and drive capability of the circuit. At the beginning of the signal transition, the DCO circuit provides a maximum dynamic drive that is equivalent to a high drive standard output device.



a. LOW-level output current.



b. HIGH-level output current.

Fig. 5. Output current as a function of output voltage.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 12.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
t_{pd}	propagation delay	An to Yn; see Fig. 6 [2]				
		V_{CC} = 1.2 V	-	5.2	-	ns
		V_{CC} = 1.4 V to 1.6 V	1.6	3.6	5.1	ns
		V_{CC} = 1.65 V to 1.95 V	1.3	2.1	4.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	1.7	3.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.9	1.5	2.5	ns
		LE to Yn; see Fig. 7 [2]				
		V_{CC} = 1.2 V	-	4.2	-	ns
		V_{CC} = 1.4 V to 1.6 V	1.6	2.8	4.6	ns
		V_{CC} = 1.65 V to 1.95 V	1.3	2.2	4.0	ns
		V_{CC} = 2.3 V to 2.7 V	1.1	1.9	3.5	ns
		V_{CC} = 3.0 V to 3.6 V	0.9	1.6	2.9	ns
		CP to Yn; see Fig. 9 [2]				
		V_{CC} = 1.2 V	-	4.3	-	ns
		V_{CC} = 1.4 V to 1.6 V	1.6	2.9	4.6	ns
		V_{CC} = 1.65 V to 1.95 V	1.5	2.2	3.7	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	1.8	3.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.8	1.7	2.7	ns
t_{en}	enable time	$\overline{OE}$ to Yn; see Fig. 11 [2]				
		V_{CC} = 1.2 V	-	6.3	-	ns
		V_{CC} = 1.4 V to 1.6 V	2.5	4.4	7.6	ns
		V_{CC} = 1.65 V to 1.95 V	2.2	3.1	5.8	ns
		V_{CC} = 2.3 V to 2.7 V	1.5	2.5	4.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	2.1	4.0	ns
t_{dis}	disable time	$\overline{OE}$ to Yn; see Fig. 11 [2]				
		V_{CC} = 1.2 V	-	5.5	-	ns
		V_{CC} = 1.4 V to 1.6 V	2.2	4.1	7.6	ns
		V_{CC} = 1.65 V to 1.95 V	2.0	3.1	5.6	ns
		V_{CC} = 2.3 V to 2.7 V	1.2	2.2	4.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	2.6	4.8	ns
t_W	pulse width	CP HIGH or LOW; see Fig. 9.				
		V_{CC} = 1.65 V to 1.95 V	2.0	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.2	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	-	ns
		LE HIGH; see Fig. 7.				
		V_{CC} = 1.65 V to 1.95 V	2.0	-	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.2	-	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	-	-	ns

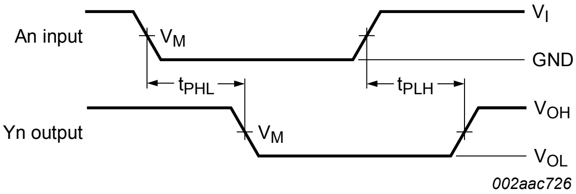
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
t_{su}	set-up time	An to CP; see Fig. 10				
		V_{CC} = 1.2 V	-	0.0	-	ns
		V_{CC} = 1.4 V to 1.6 V	0.2	0.0	-	ns
		V_{CC} = 1.65 V to 1.95 V	0.0	-0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.0	-0.2	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.0	-0.3	-	ns
		An to LE; see Fig. 8				
		V_{CC} = 1.2 V	-	1.5	-	ns
		V_{CC} = 1.4 V to 1.6 V	1.6	0.9	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.1	0.6	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.7	0.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	0.5	-	ns
t_h	hold time	An to CP; see Fig. 10				
		V_{CC} = 1.2 V	-	0.1	-	ns
		V_{CC} = 1.4 V to 1.6 V	0.7	0.3	-	ns
		V_{CC} = 1.65 V to 1.95 V	0.7	0.3	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.7	0.3	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.3	0.6	-	ns
		An to LE; see Fig. 8				
		V_{CC} = 1.2 V	-	-0.7	-	ns
		V_{CC} = 1.4 V to 1.6 V	0.0	-0.3	-	ns
		V_{CC} = 1.65 V to 1.95 V	0.2	-0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.2	0.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.3	0.8	-	ns
f_{max}	maximum frequency	CP; see Fig. 9				
		V_{CC} = 1.65 V to 1.95 V	250	-	-	MHz
		V_{CC} = 2.3 V to 2.7 V	400	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	500	-	-	MHz
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [3]				
		outputs enabled	-	25	-	pF
		outputs disabled	-	6	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

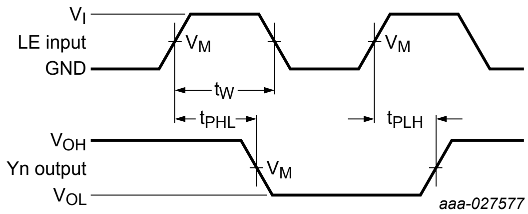
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

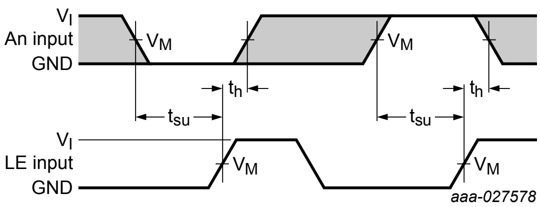
Fig. 6. Input (An) to output (Yn) propagation delay



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

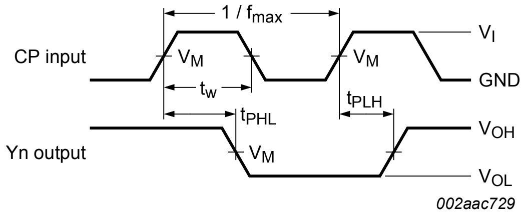
Fig. 7. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays



Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

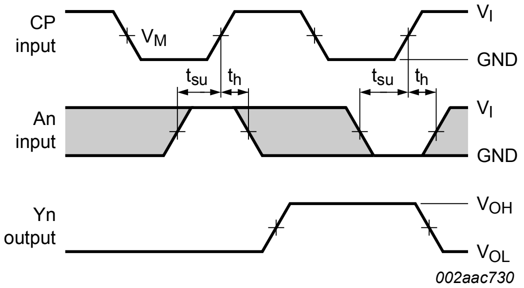
Fig. 8. Data set-up and hold times, An input to LE input



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 9. The clock (CP) to output (Yn) propagation delays, the clock pulse width and the maximum clock frequency

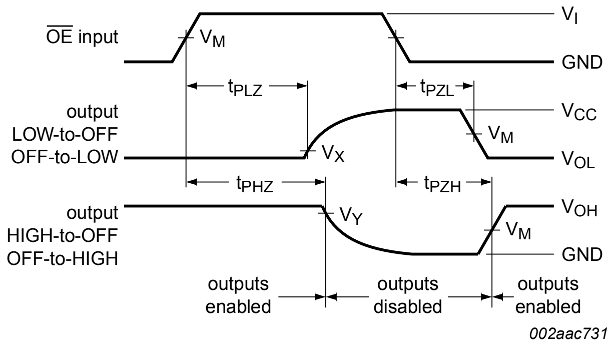


Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 10. Data set-up and hold times, An input to CP input



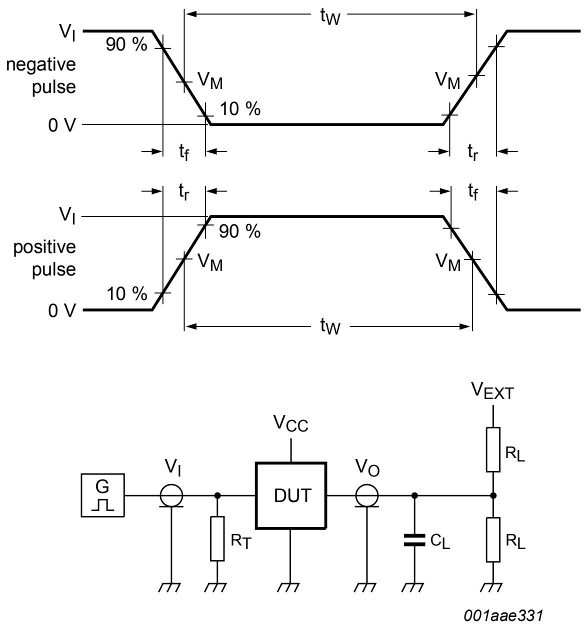
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 11. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
≤ 2.3 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.3 V to 2.7 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
3.0 V to 3.6 V	V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

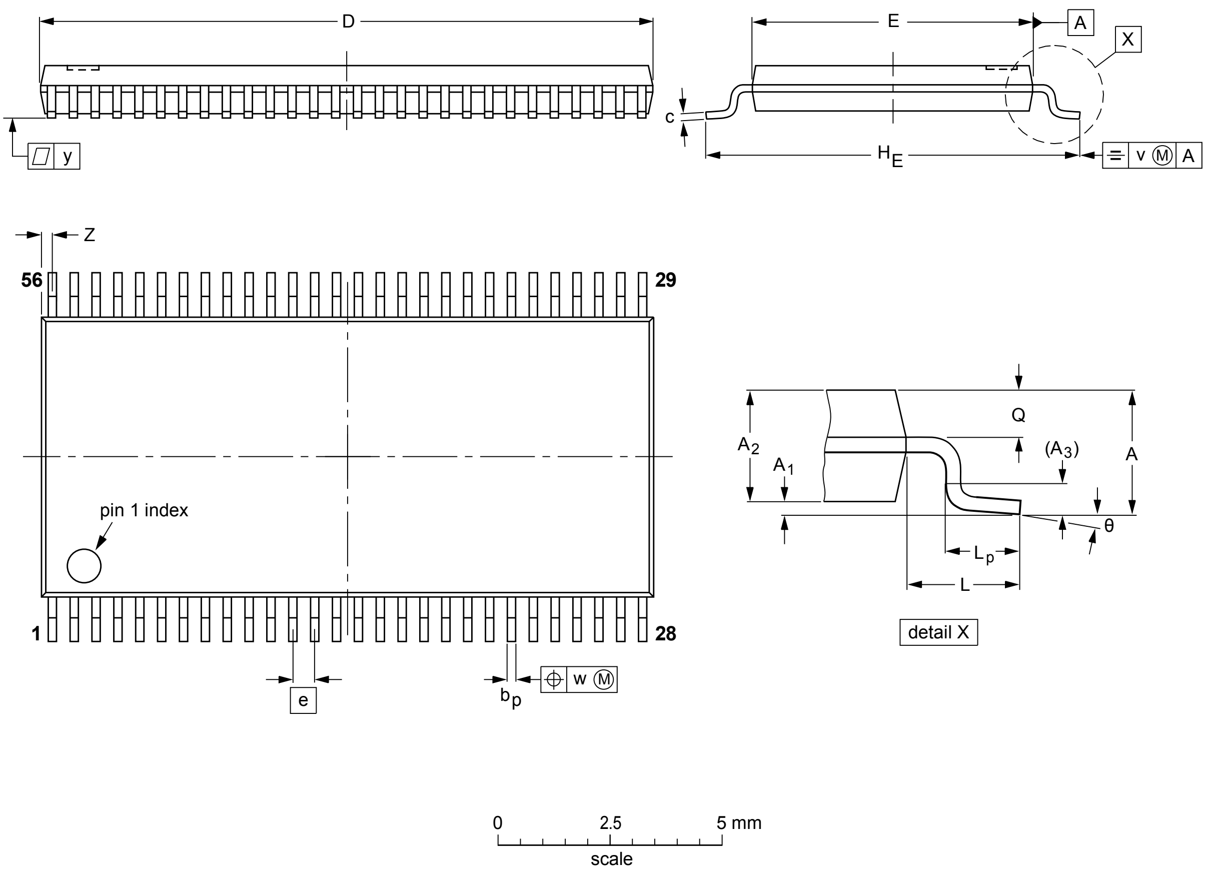
Fig. 12. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
≤ 2.3 V	V_{CC}	≤ 2.0 ns	30 pF	1000 Ω	open	2 x V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 x V_{CC}	GND
3.0 V to 3.6 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 x V_{CC}	GND

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 13. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DCO	Dynamic Controlled Output
DUT	Device Under Test

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC16835A v.6	20180924	Product data sheet	-	74AVC16835A v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74AVC16835ADGV (SOT481-2) removed.			
74AVC16835A v.5	20020315	Product data sheet	-	74AVC16835A v.4
74AVC16835A v.4	20000725	Product specification	-	74AVC16835A v.3
74AVC16835A v.3	20000502	Preliminary specification	-	74AVC16835 v.2
74AVC16835 v.2	19990405	Preliminary specification	-	74AVC_AVCH16835 v.1
74AVC_AVCH16835 v.1	19981207	Objective specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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LifeElectronics
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ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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